SNRI2023 Lab 1

CMOS Cryogenic Readout Electronics

Scuola Nazionale dei Rivelatori Innovativi 2023

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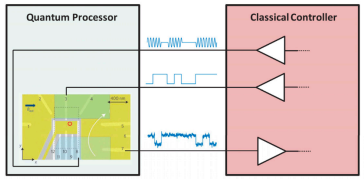
Context and Definitions

“Deep Cryogenic” electronics for Quantum technologies

- Towards the development of novel quantum sensor technologies through the consolidation and scaling up of existing and emerging technologies;
  - provide advanced enabling infrastructures and key capabilities for the development of cryogenic electronics in order to solve “the wiring bottleneck” on quantum computers;
  - cryogenic CMOS operating <4K and down to the mK pave the way for scalability into the million qubit realm.

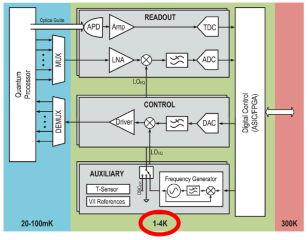
Classical Controller



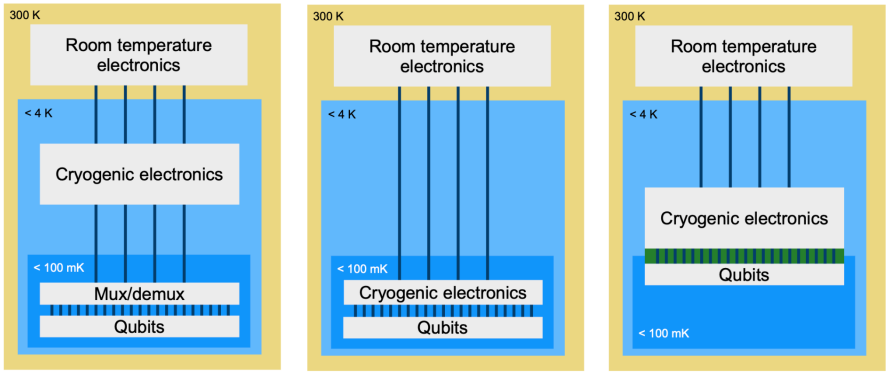
- Electronics to control and read-out the quantum processor mostly operated at room temperature (RT)
- Does not scale with the number of qubits

E. Charbon, ESSCIRC 2019.
B. Patra, *et al.*, JSSC, vol. 53, no. 1, 2018.

CMOS Integrated Controller



- More scalable approach by moving the control and read-out electronics closer to the qubits and operate it at cryogenic temperature (around 4 K)



C. Enz, A. Beckers and F. Jazaer, “MOSFET Compact Modeling down to Cryogenic Temperatures”

C. Degenhardt, “Cryogenic QUBIT Control – The Tyranny of numbers, self-heating and everything“

Context and Definitions

"Mild cryogenic" electronics for Liquid Detectors

- Rare-event search on astroparticles: neutrino physics and direct dark matter detection using liquid scintillators e.g. Liquid Xenon (LXe) and Liquid Argon (LAr);
- Single and dual-phase detectors employing (solid-state) photon sensors require front-end readout electronics operating at 165K (LXe) or 88K (LAr).

Experiment	Type	Photon detector	Area (m^2)
nEXO	LXe	SiPMs (FBK [Ch2-18], Hamamatsu [Ch2-19]), digital 3D-SiPM	5
DARWIN	LXe	PMTs, SiPMs or Hybrids (SIGHT, ABALONE)	8
TAO	LSci	FBK SiPMs	10
DarkSide-20k	LAr	SiPMs (FBK NUV-HD triple-dopant)	30
ARGO	LAr	SiPM is baseline option	200
DUNE	LAr	Light guide or trap + SiPM	10-1000

Need to commit to strong R&D programs for the development and deployment of new readout schemes suitable for future large-scale neutrino and dark matter detectors;

today's solutions are not scalable.

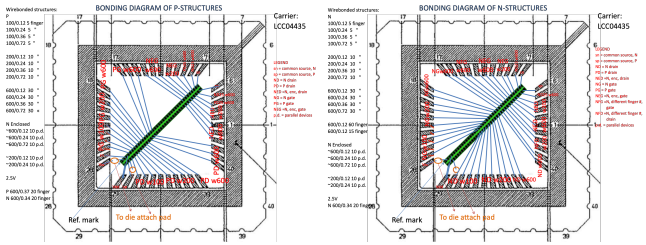
Future larger scale experiments will call for innovative cold integrated readout electronics implementing digital signal processing within the photosensor detection module.

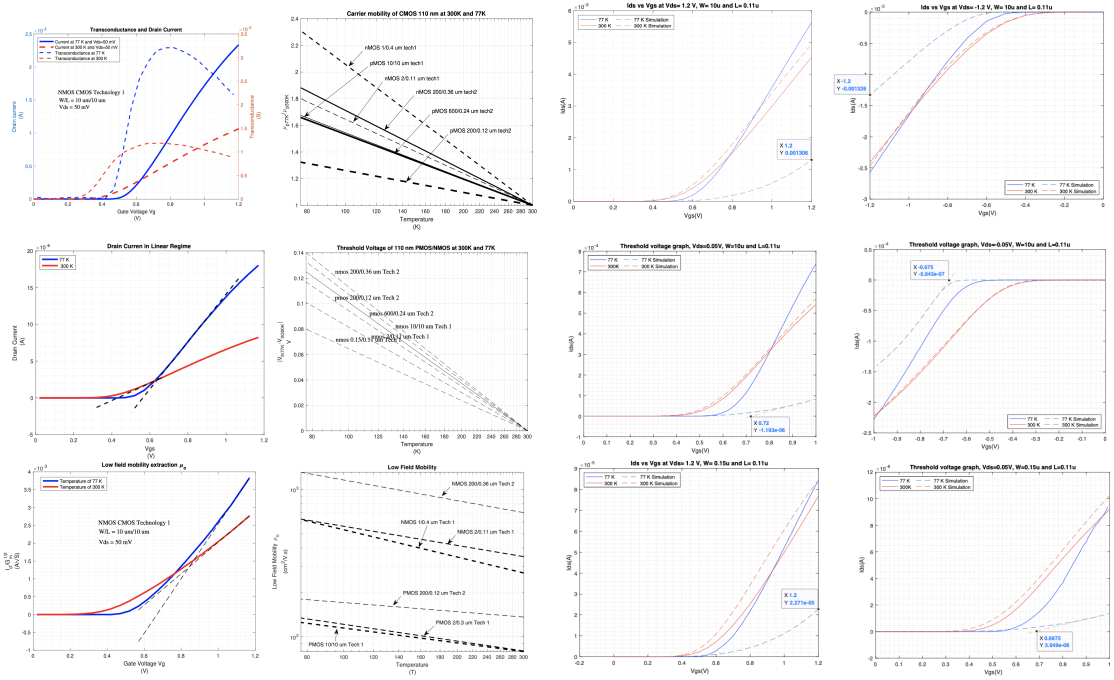
"R&D on the 5-year horizon for greater integration include (...) dedicated ASIC design; 3D-vertical integration R&D; and development of lower-power, larger-area and lower-radioactivity photodetection modules."

CMOS Cryogenic Electronics

Challenges for circuit design and operation

- CMOS Process Design Kits typically valid down to 233K (-40°C), although models scale relatively well down to 77K. This was verified with VDSM bulk and FDSOI technology nodes.
- Cold CMOS PDKs are fundamental for the development of complex mixed-signal ASICs allowing for innovative detector architecture and concepts, data transfer, readout and control.
- If no Cold PDK is available, design test structures and extract MOSFET parameters to guide the circuit design:



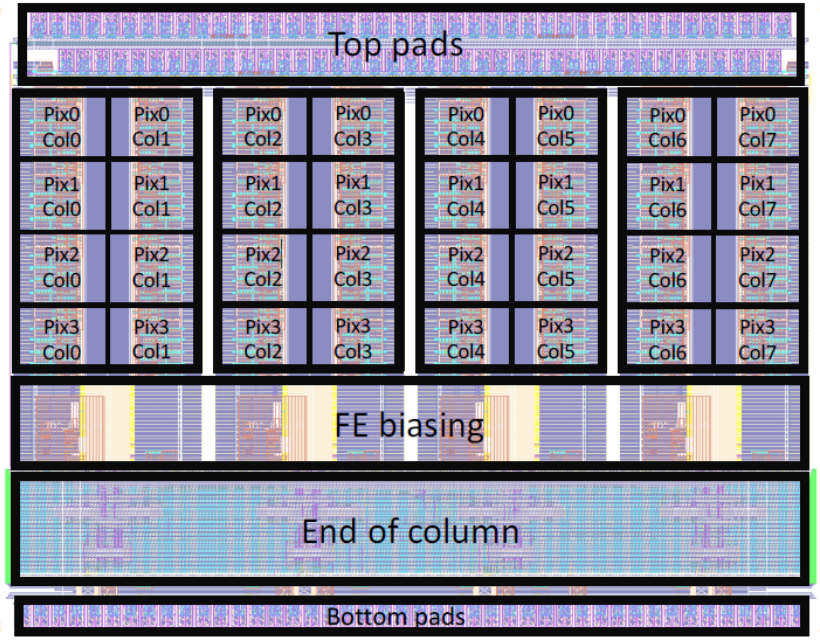


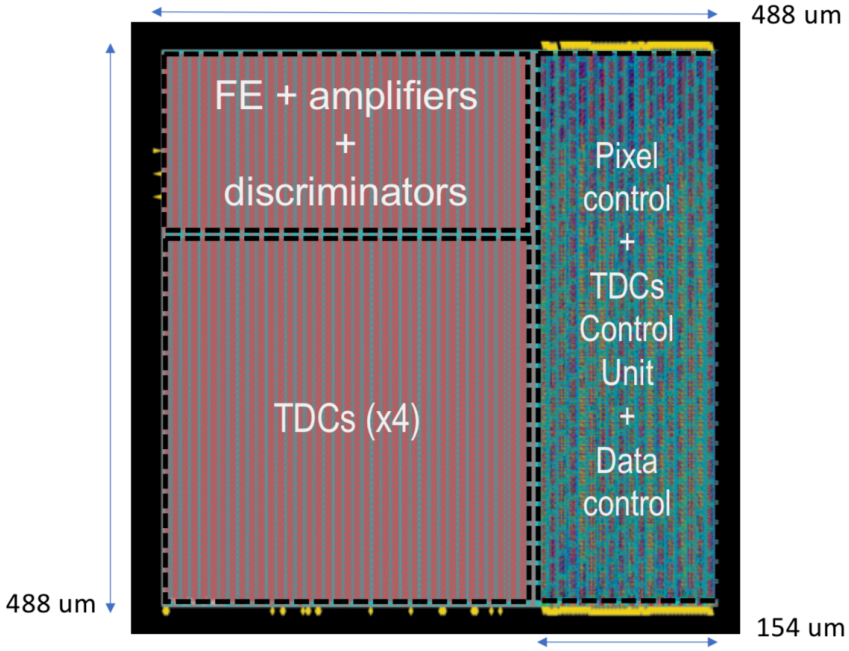
LN static setup at INFN Torino for extraction of MOSFET parameters and (plots) comparison between bulk CMOS technology nodes at 77K [extracted from PhD thesis INFN-Polito A. Martinez]

The Cold Test Vehicle: ALCOR

An ASIC for SiPM readout at Cryogenic Temperature

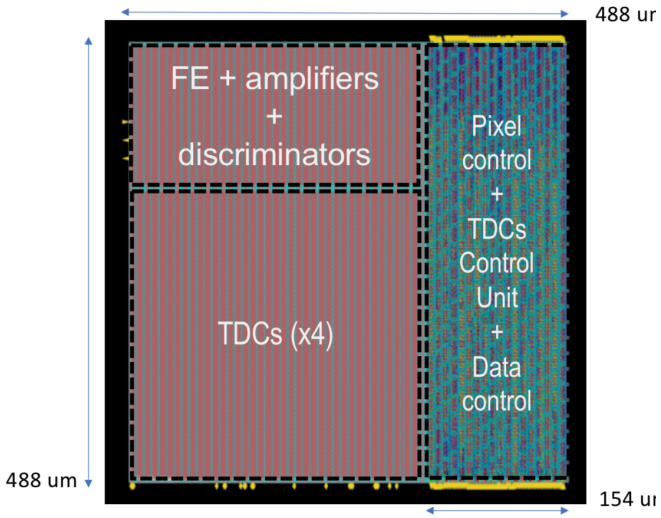
- 32-pixel matrix mixed signal ASIC (CMOS 110nm) developed by INFN, VFE optimised for **operation at 77K**
- the chip performs amplification, signal conditioning and event digitisation, and features fully digital I/O
- Single-photon time tagging mode or time and charge measurement
- 4 LVDS TX data links, SPI configuration, operation at 160/320 MHz (TDC binning 100 or 50 ps, respectively)

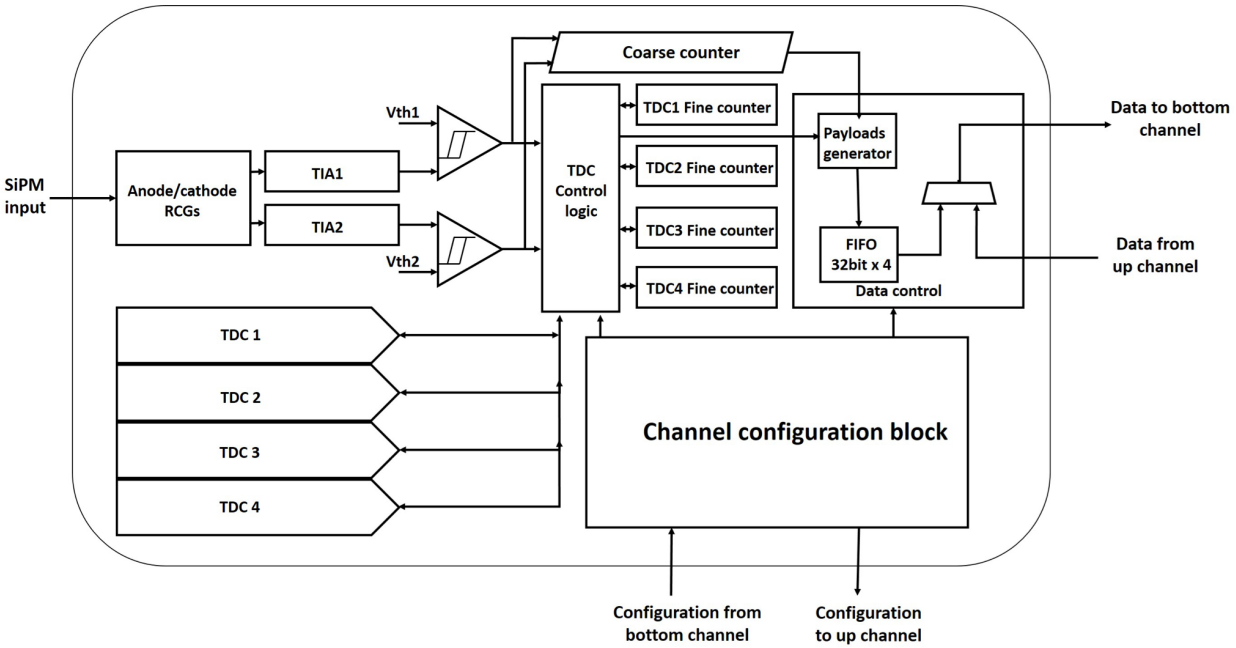




The Cold Test Vehicle: ALCOR

Pixel floorplan and Architecture



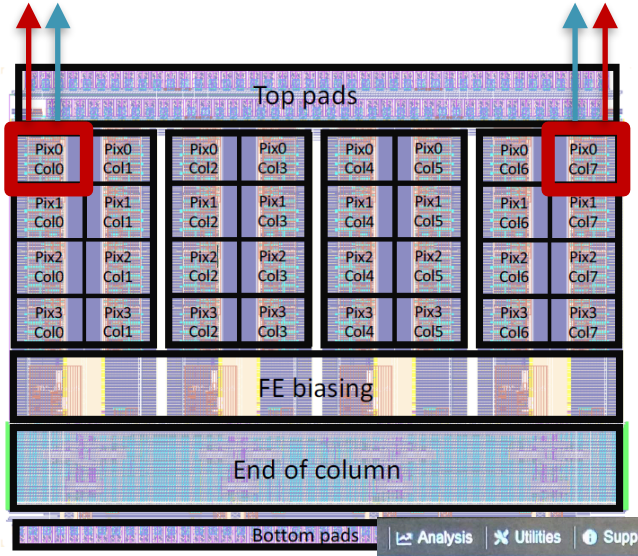


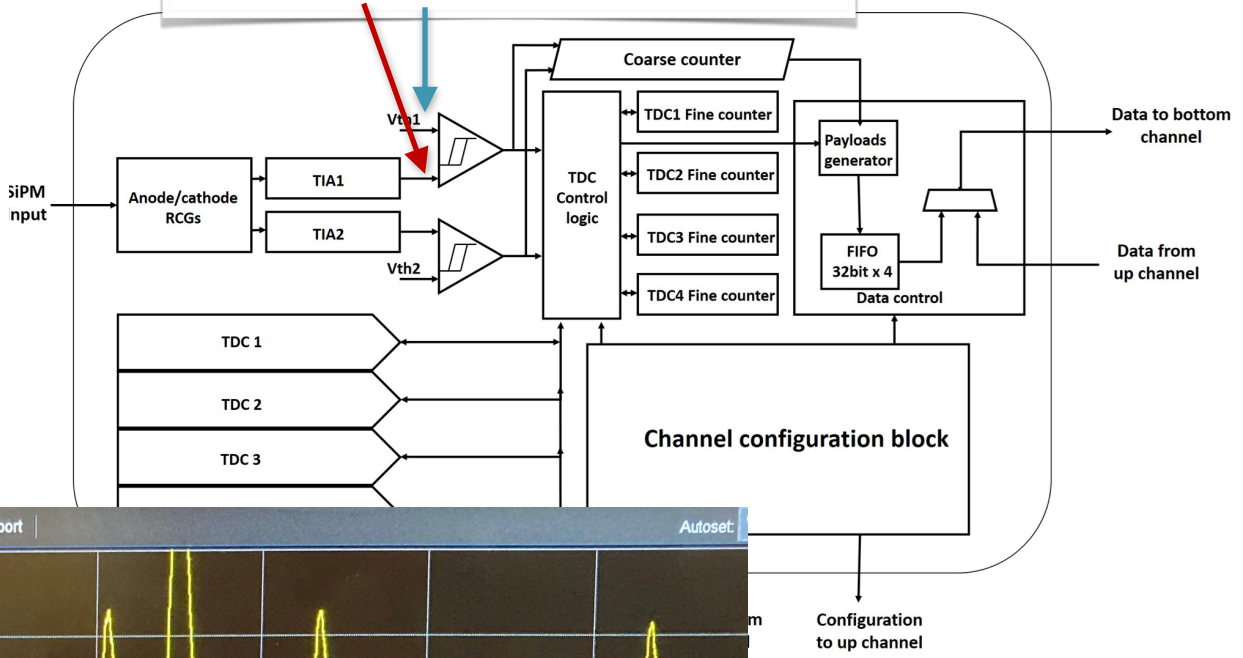
- dual-polarity RCG-based preamplifier: high bandwidth and low input-impedance (10-20 Ω)
- 2 independent post-amp branches and 4 gain settings
- Dual leading edge discriminators with **independent (and per pixel) threshold settings** (6-bit DAC)
- Pixel control logic handles quad-TDC operation, pixel configuration and data transmission

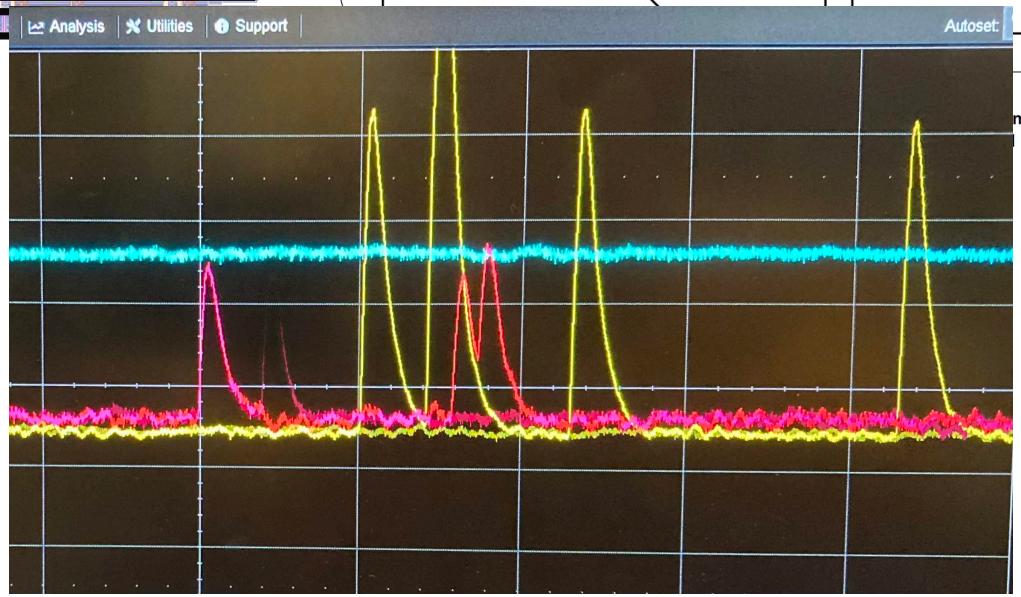
The Cold Test Vehicle: ALCOR

Pixel floorplan and Architecture

Amplifier Output and Threshold voltage are available as debug outputs for Pixels 0 and 28



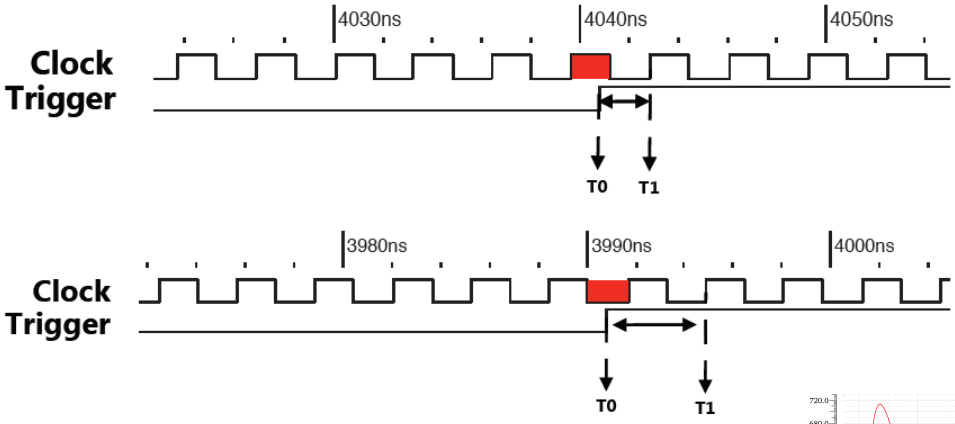


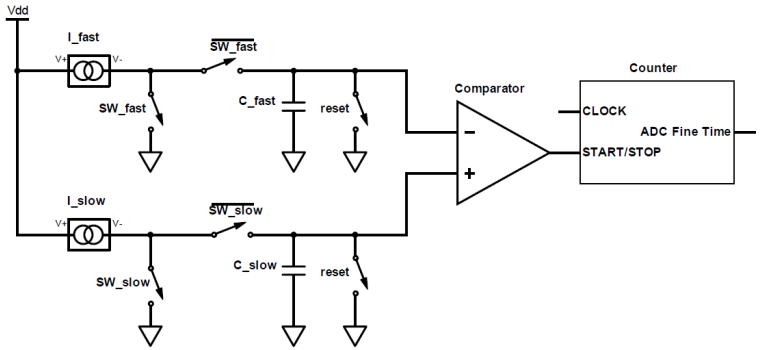


The Cold Test Vehicle: ALCOR

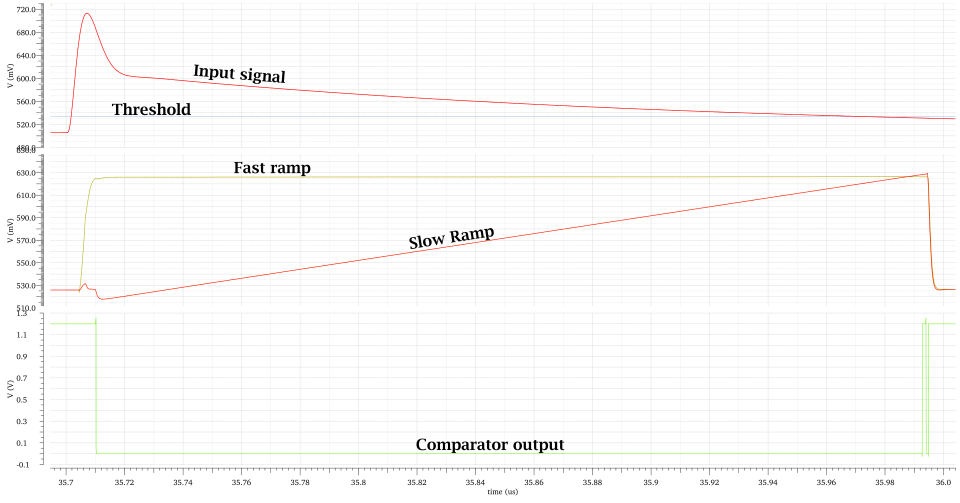
Time-to-Digital Converters

- A coarse time stamp is extracted from the system clock running up to 320 MHz
- A Low-power Analogue interpolation TDC measures phase between event trigger (T0) and clock (T1)



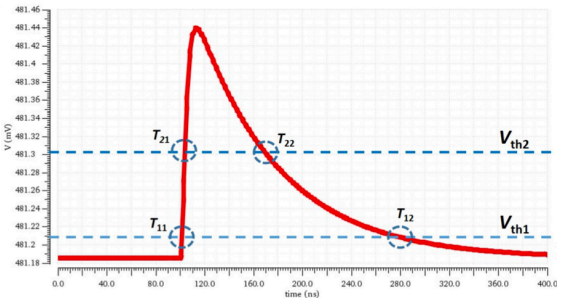


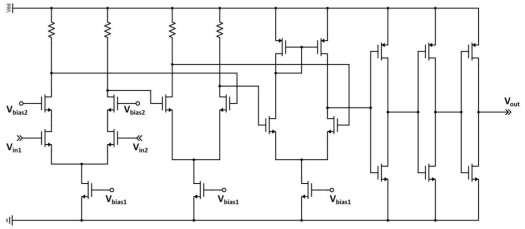
- The phase between event trigger and clock is encoded with a Time-to-Analogue Converter (TAC)
- A Wilkinson ADC is then used to digitise the voltage, generating the fine time information (Tfine)

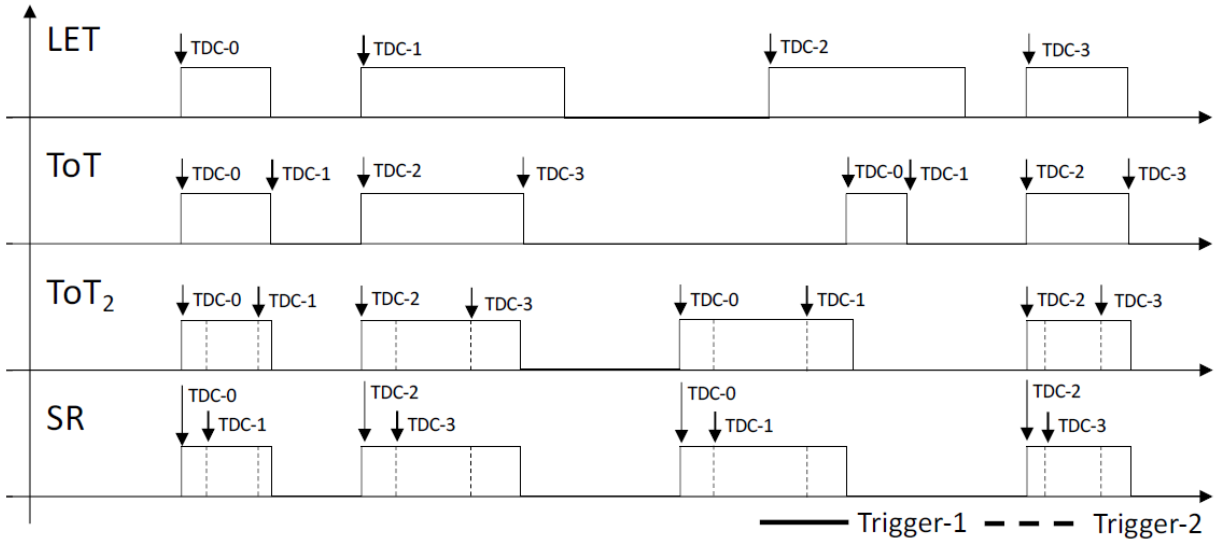


The Cold Test Vehicle: ALCOR

Pixel Operation Modes



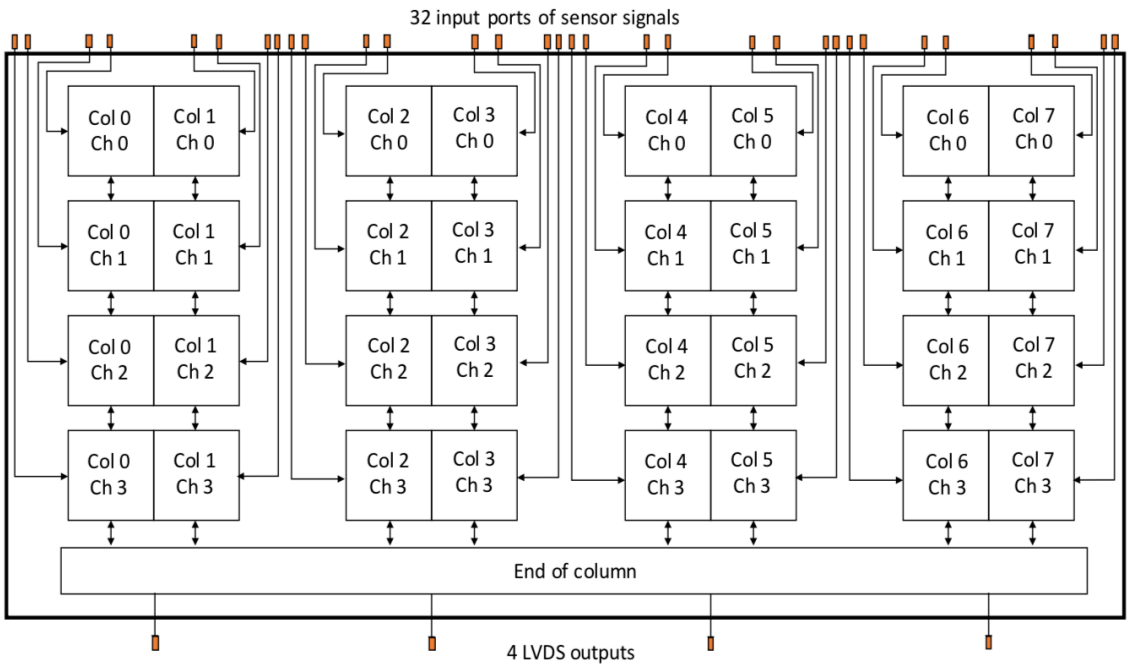




- **LET** leading edge threshold measurement, high-rate time-stamp architecture
- **TOT** Time-over-Threshold (selectable branch for falling edge measurement)
- **SR** slew-rate measurement for signal shape characterisation
- Pixel can be disabled, in normal (trigger less) acquisition mode or can be triggered by a test-pulse,
  - either generated by the on-chip calibration circuitry or propagated from the DAQ,
  - either injecting a configurable charge to the front-end or triggering asynchronously the pixel logic for characterisation and calibration of the TDCs

The Cold Test Vehicle: ALCOR

Pixel Operation Modes



- 32-pixel matrix (4×8 array) mixed-signal ASIC
- SPI-based chip configuration

Event word

Column ID	Channel ID	TDC ID	Coarse counter	Fine counter
3 bits	3 bits	2 bits	15 bits	9 bits

31 0

Status word

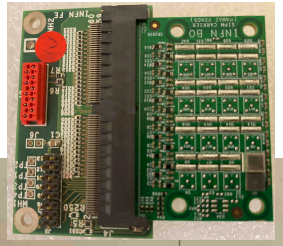
Column ID	Pixel ID	Lost event counter	Lost e.w. counter TDC1	Lost e.w. counter TDC2	Lost e.w. counter TDC3	Lost e.w. counter TDC4	SEU counter
3 bits	3 bits	6 bits	4 bits	4 bits	4 bits	4 bits	4 bits

31 0

- 64-bit (32-bit on time tagging mode) event and status data is generated on-pixel and propagated down the column
- End of Column collects digitised data from pixels and transmits it off-chip using (up to) 4 LVDS Tx links
- End of Column provides also configuration (and analogue bias) to the pixel “matrix”

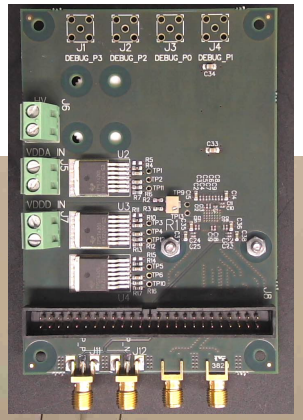
The Cold Test Setup

SiPM Carrier

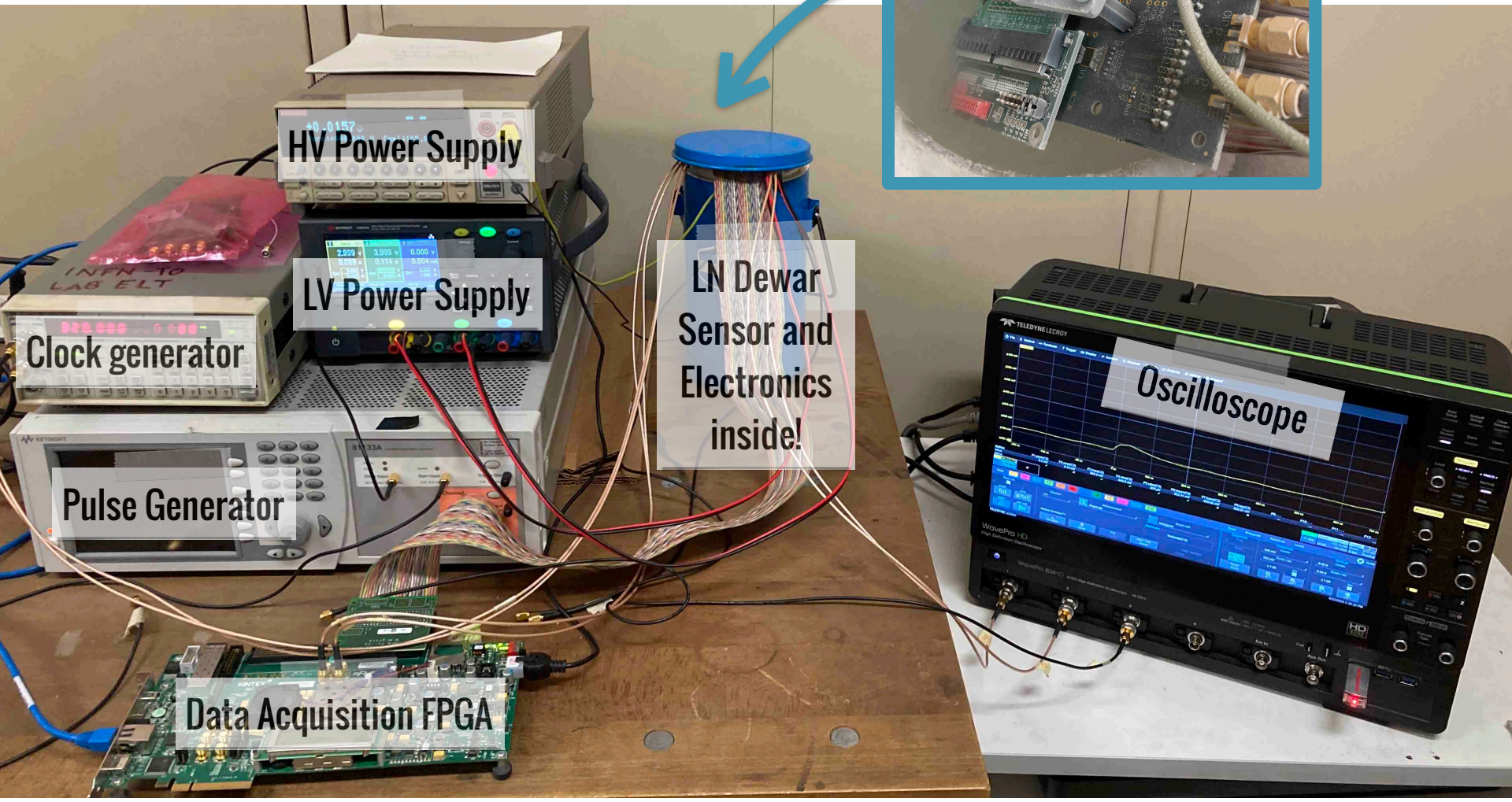


ALCOR FEB (f)

ALCOR FEB (b)

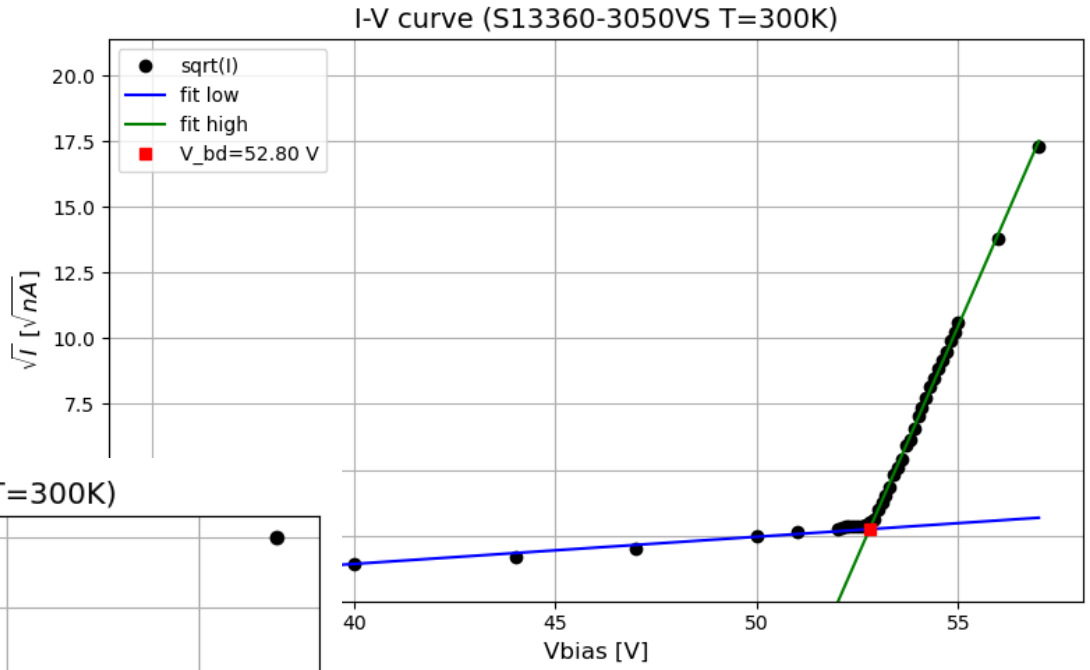


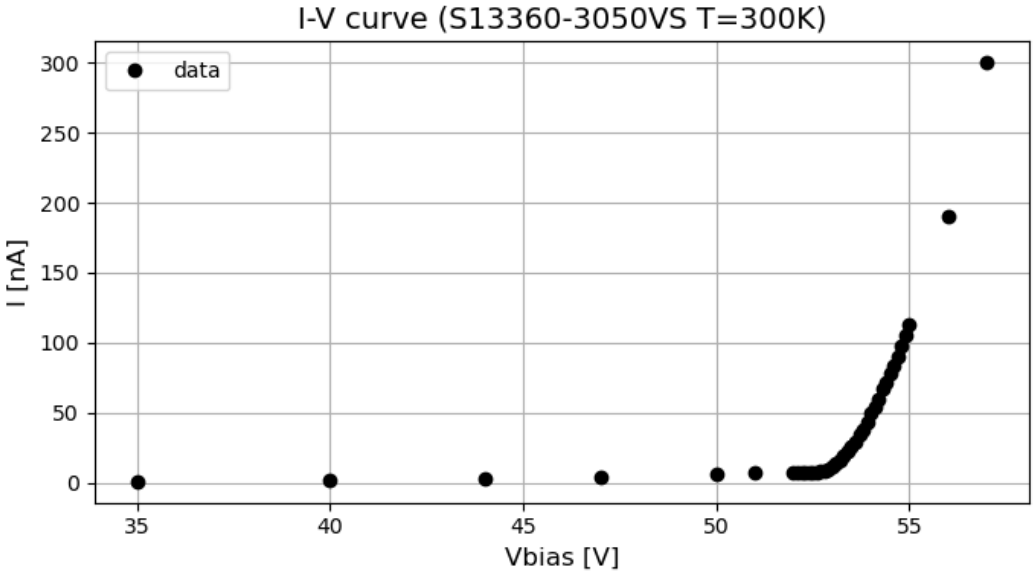
The Cold Test Setup



Laboratory Activities

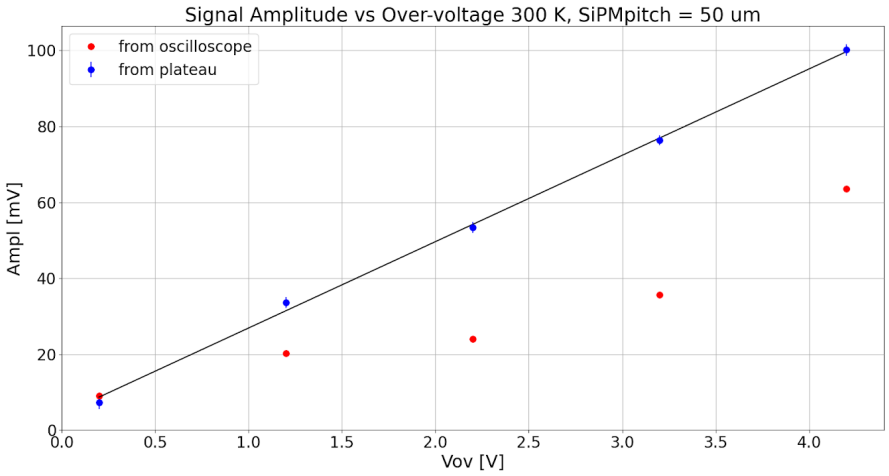
SiPM: extraction of Breakdown Voltage at 300K

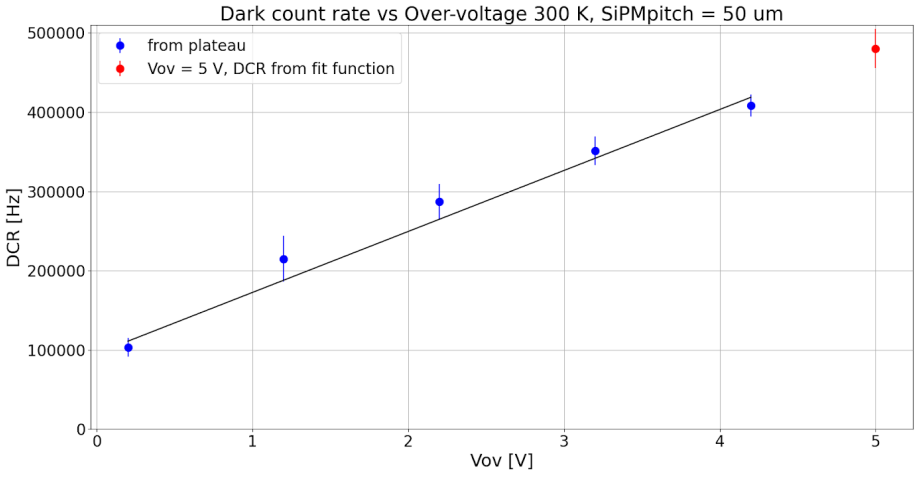


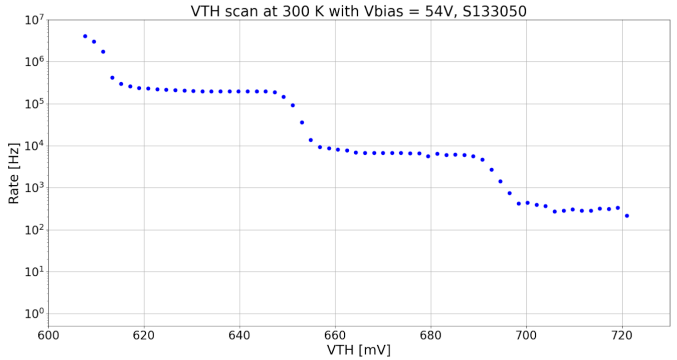


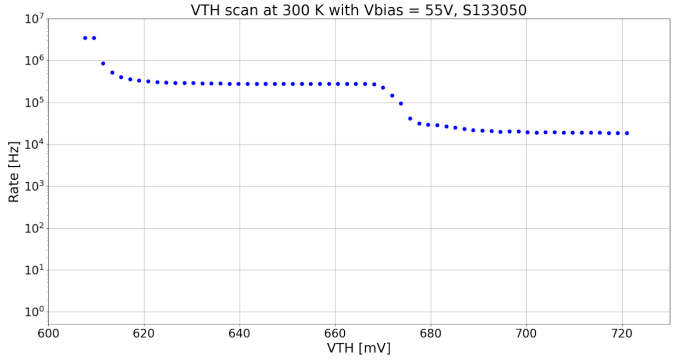
Laboratory Activities

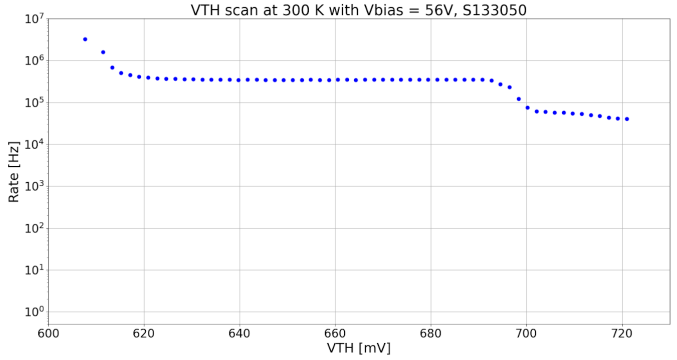
Dark Count Rate (DCR) and signal amplitude studies at 300K





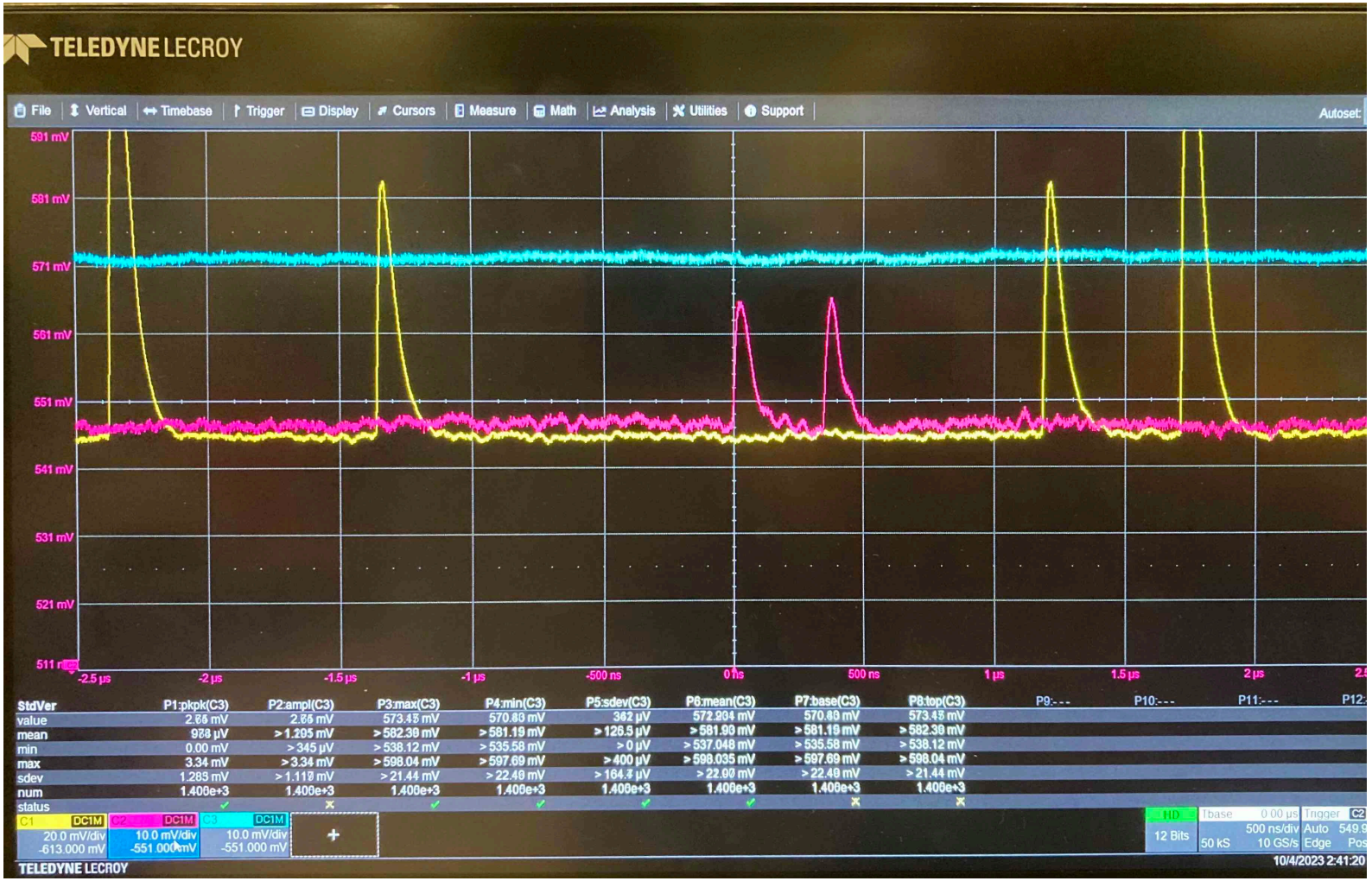






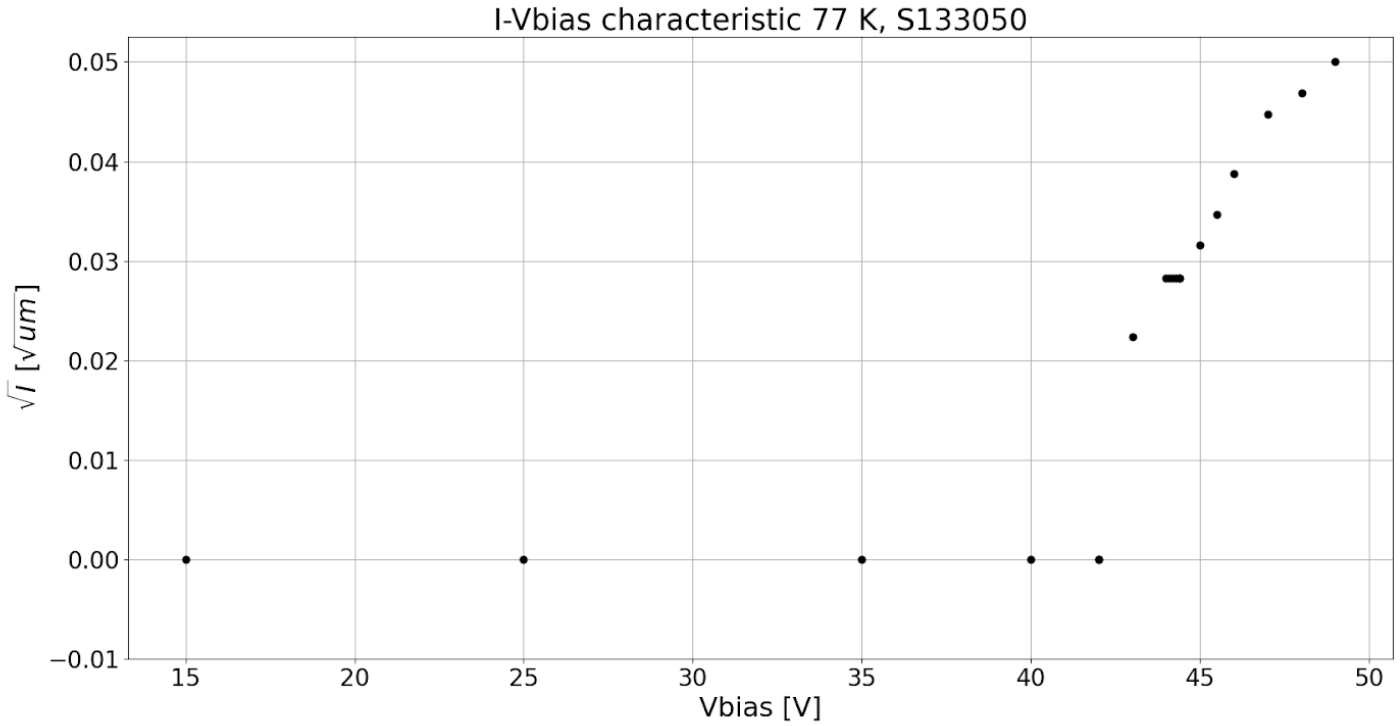
Laboratory Activities

Studies of signal amplitude and threshold scans during cool-down



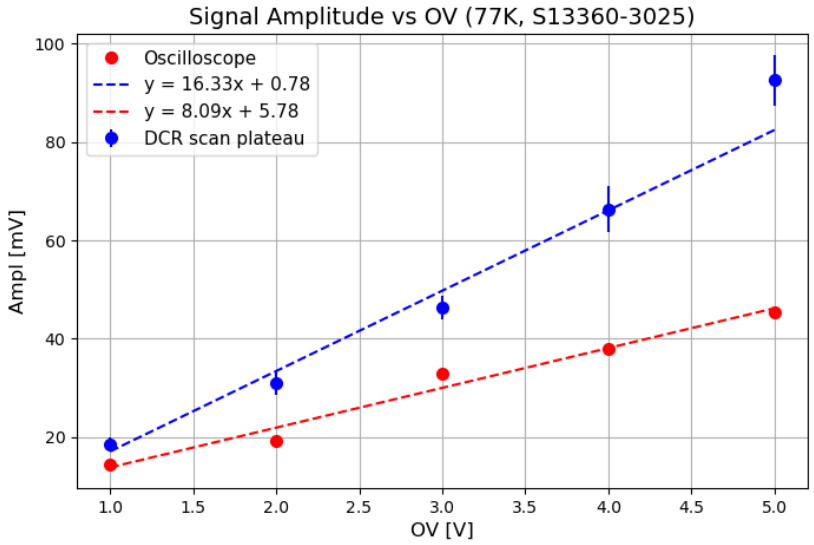
Laboratory Activities

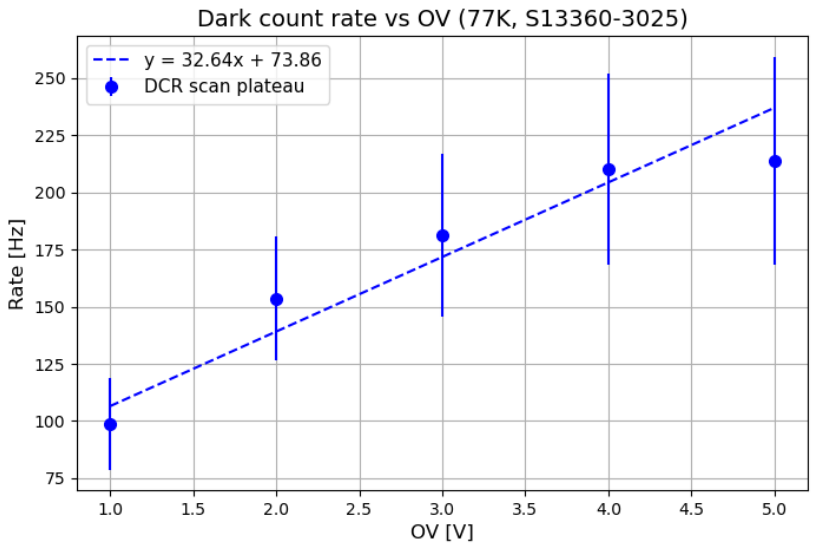
SiPM: extraction of Breakdown Voltage at 77K

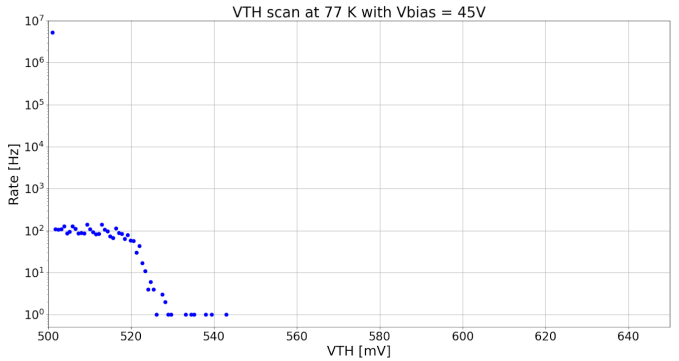


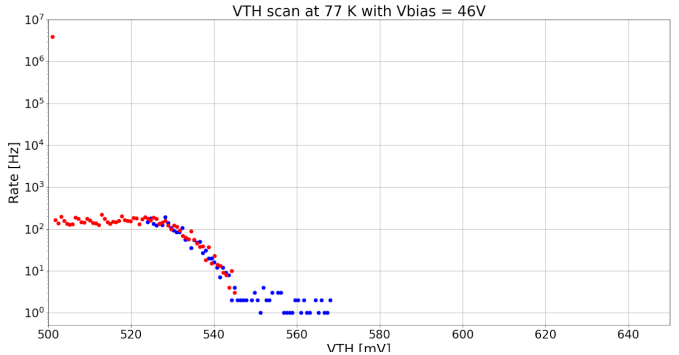
Laboratory Activities

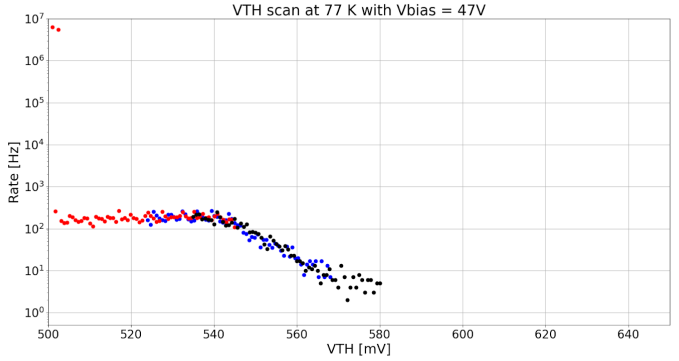
Dark Count Rate (DCR) and signal amplitude studies at 77K







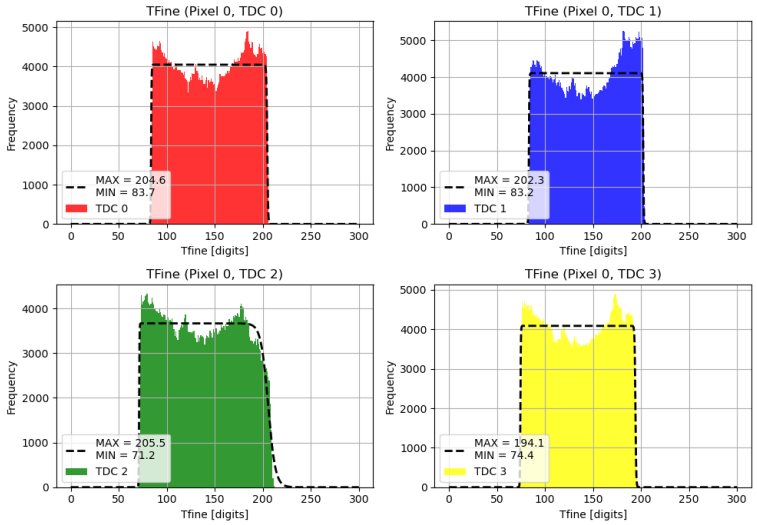


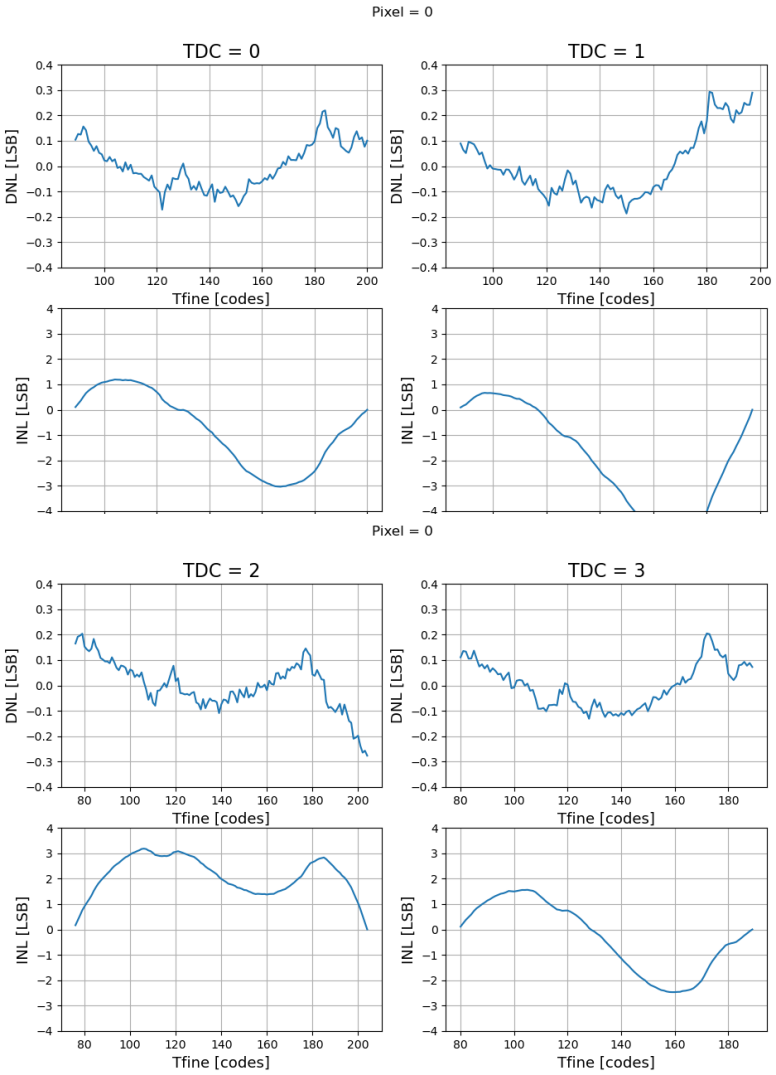


Laboratory Activities

Characterisation of Time-to-Digital Converters

- Code density and Linearity (RT vs. LN)
- Quantisation error (RT vs. LN)

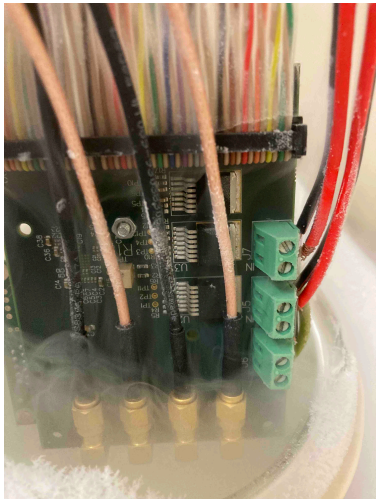




The Cold Test Setup

on the definition of “Hands-On Laboratory”…

- Test setup uses Liquid Nitrogen (77K)
- Handling of the electronics and cabling during test with LN (cool-down and warm-up) will be sorted out by the Laboratory Lecturer
- Keep a safe distance from the dewar during re-fill operations



Lab Support Material

what's inside

- ALCOR chip User Guide
- ALCOR Test Board Schematics
- SiPM Datasheets