Recent results and technical R&D developments for VELO Upgrade II

VERTEX 2023 - 32nd International Workshop on Vertex Detectors 19-Oct-23

Andrea Lampis
on behalf of the LHCb Collaboration

Upgrade II VELO

Framework TDR for the LHCb Upgrade II

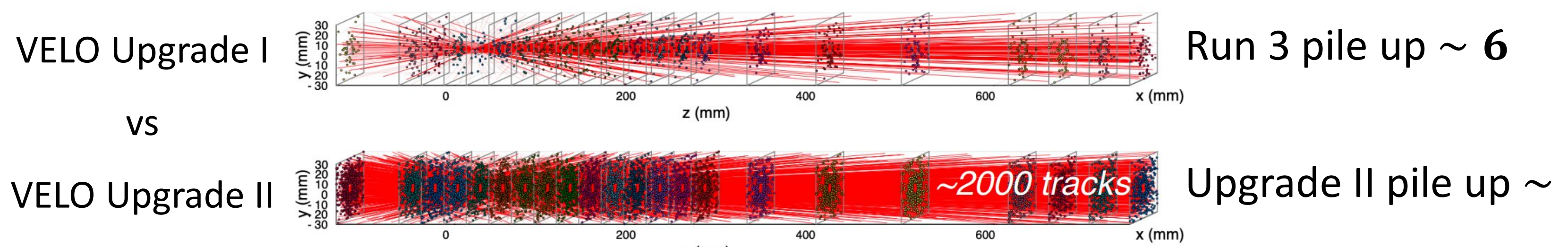
From 2032 instantaneous luminosity @ LHCb from $2 \cdot 10^{33}\ cm^{-2}s^{-1}$ to $1.5 \cdot 10^{34}\ cm^{-2}s^{-1}$

Higher luminosity -> **higher pile-up, radiation damage and data rate on detectors**

VELO Upgrade I

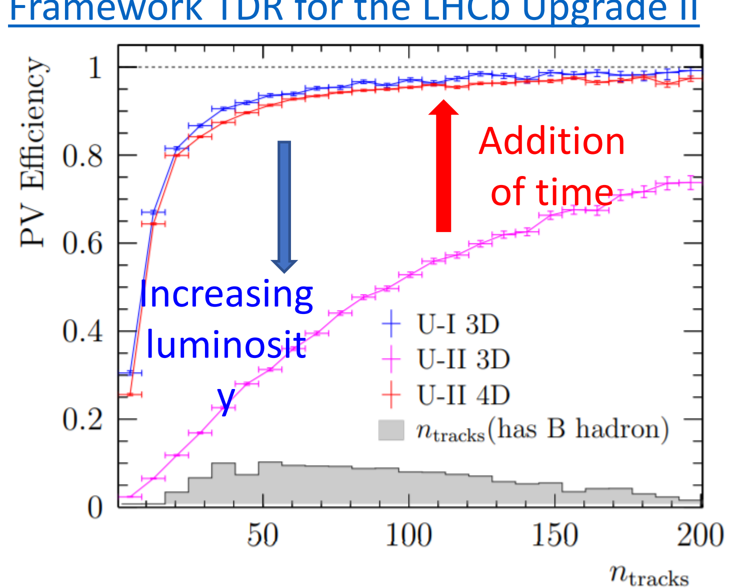
vs

VELO Upgrade II



Run 3 pile up $\sim$ **6**

Upgrade II pile up $\sim$ **40**



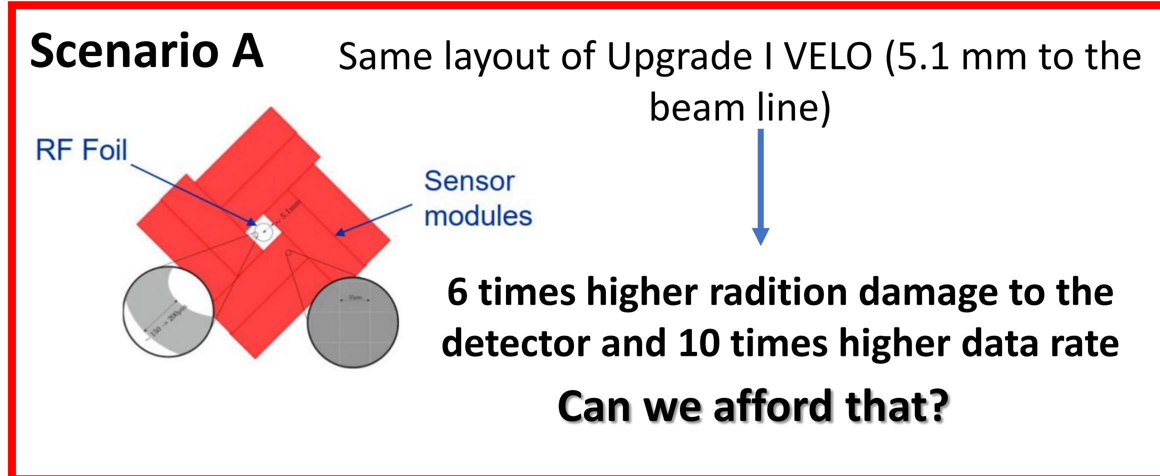
Tracking performances of the Upgrade I VELO in the high luminosity condition will significantly drop

A 4D VERTEX DETECTOR IS REQUIRED TO MAINTAIN PERFORMANCES

Two opposite scenarios to guide R&Ds

Scenario A

Same layout of Upgrade I VELO (5.1 mm to the beam line)

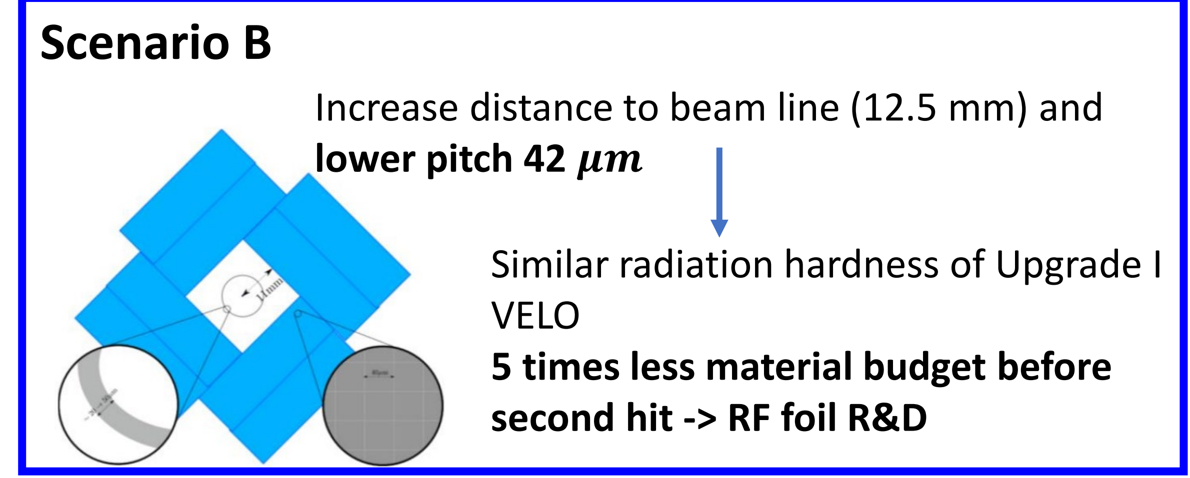


6 times higher radition damage to the detector and 10 times higher data rate

Can we afford that?

Scenario B

Increase distance to beam line (12.5 mm) and **lower pitch 42 μm**



Similar radiation hardness of Upgrade I VELO

5 times less material budget before second hit -> RF foil R&D

Sensors

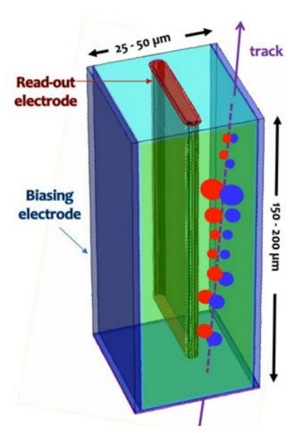
Framework TDR for the LHCb Upgrade II

Requirement	scenario S_A	scenario S_B
Pixel pitch [µm]	≤55	≤42
Lifetime fluence [1×10^{16} 1 MeV n_{eq}/cm^2]	> 6	> 1
TID lifetime [MGy]	> 28	> 5
Sensor Timestamp per hit [ps]	≤ 35	≤ 35
ASIC Timestamp per hit [ps]	≤ 35	≤ 35
Hit Efficiency [%]	≥ 99	≥ 99
Power per pixel [µW]	≤ 23	≤ 14
Pixel rate hottest pixel [kHz]	> 350	> 40
Max discharge time [ns]	< 29	< 250
Bandwidth per ASIC of 2 cm^2 [Gb/s]	> 250	> 94

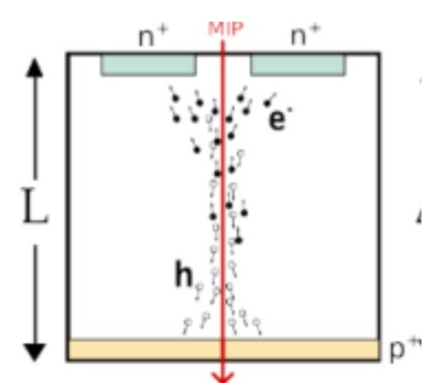
4 strong requirements to be accomplished at the same time

Several silicon sensors technologies under study to be used for the Upgrade II VELO

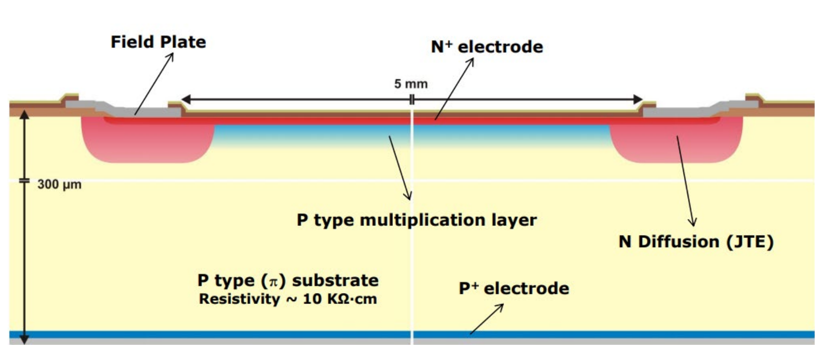
3D sensors



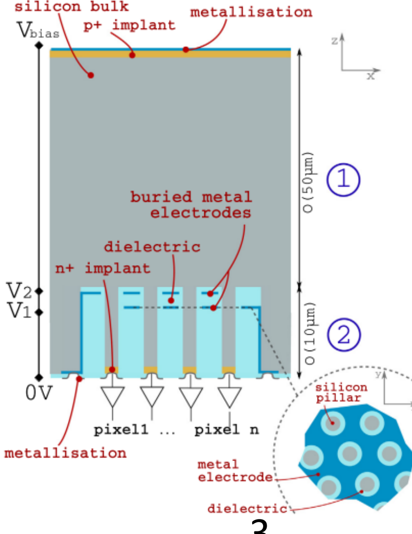
Thin planar sensors



LGADs



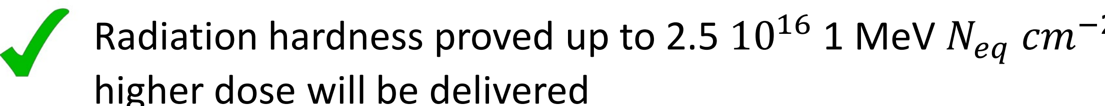
SiEM



3D sensors

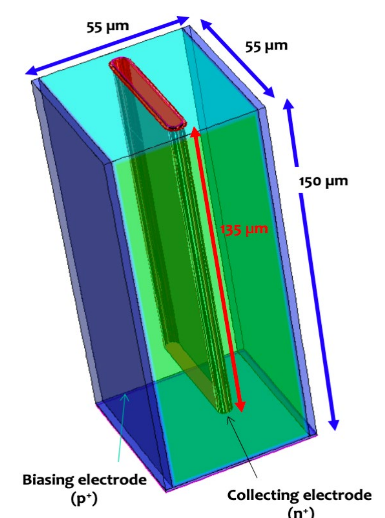
- 3D sensors optimized for best time resolution -> 3D trench

✓ Timing performances around 10 ps



✓ Radiation hardness proved up to 2.5 10^{16} 1 MeV $N_{eq}\ cm^{-2}$ higher dose will be delivered

✓ Fill factor around 80%, but if tilted recovers full efficiency



SPS 180 GeV/c π^+

time resolution σ_{eff}^{Si} [ps]

Not irradiated

1.0 10^{16} 1 MeV n_{eq} cm^{-2}

2.5 10^{16} 1 MeV n_{eq} cm^{-2}

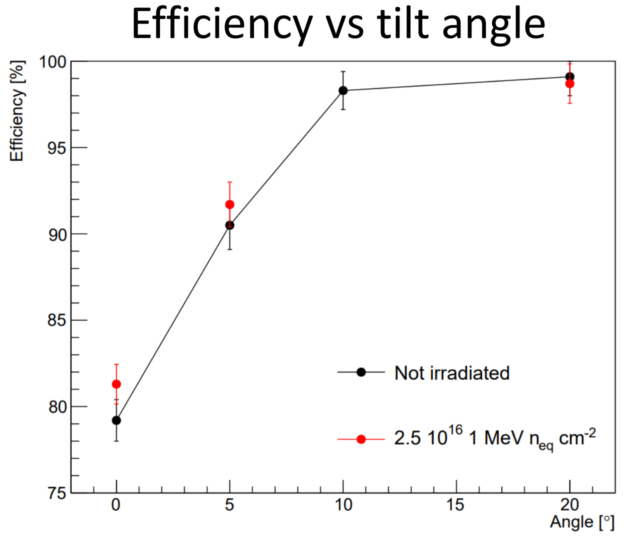
55um pitch

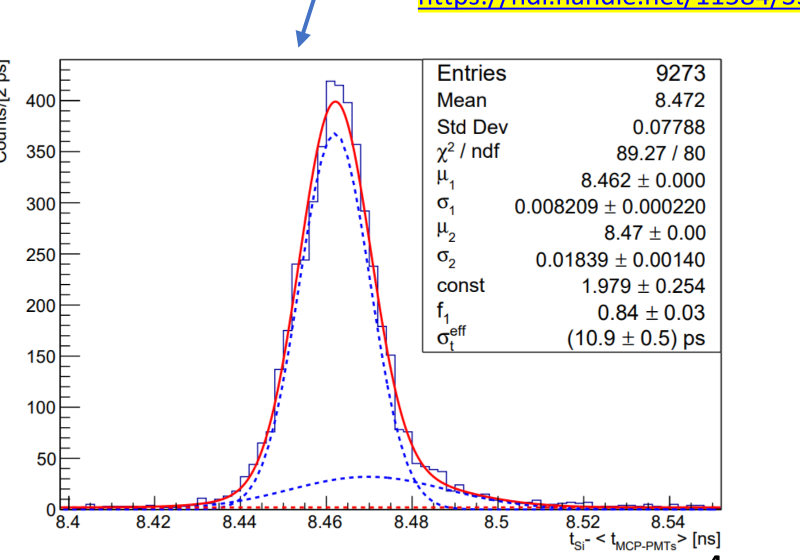
V_{bias} [V]

https://hdl.handle.net/11584/359379

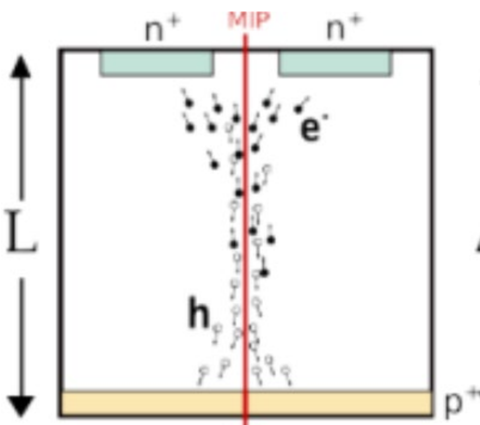
Higher capacitance with respect to other sensors O(100 fF)

New technology production yield still low, more runs needed to optimise production process





Thin planar sensors



In principle they could reach less than 30 ps time resolution

[W. Riegler and G. Rinella, Time resolution of silicon pixel sensors]

R&D aimed to study timing and radiation hardness of 50 μm to 300 μm thick sensors

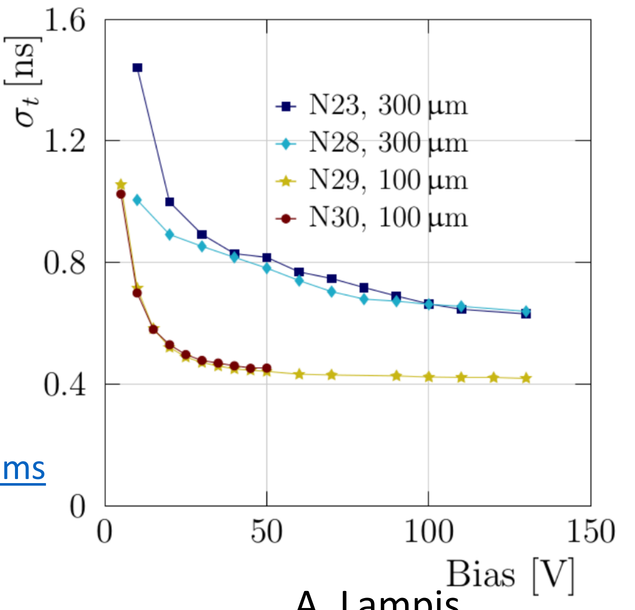
50 μm thick sensor irradiated up to $1 \cdot 10^{17}$ $1\ MeV\ n_{eq}\ cm^{-2}$

50 μm -20°C

[Link]

Timing performances

100 μm thick sensors connected to Timepix4, time resolution around 400 ps (dominated by ASIC)



Best time resolution of 100 μm thick planar sensors 108 ps, measured with high power consumption, discrete component readout (SiGe)

http://dx.doi.org/10.1088/1748-0221/11/03/P03011

[Kazu Akiba (Nikhef) @10th Beam Telescopes and Test Beams Workshop 2022]

Evaluation of timing performances of 50 μm thick sensors is ongoing

LGADs

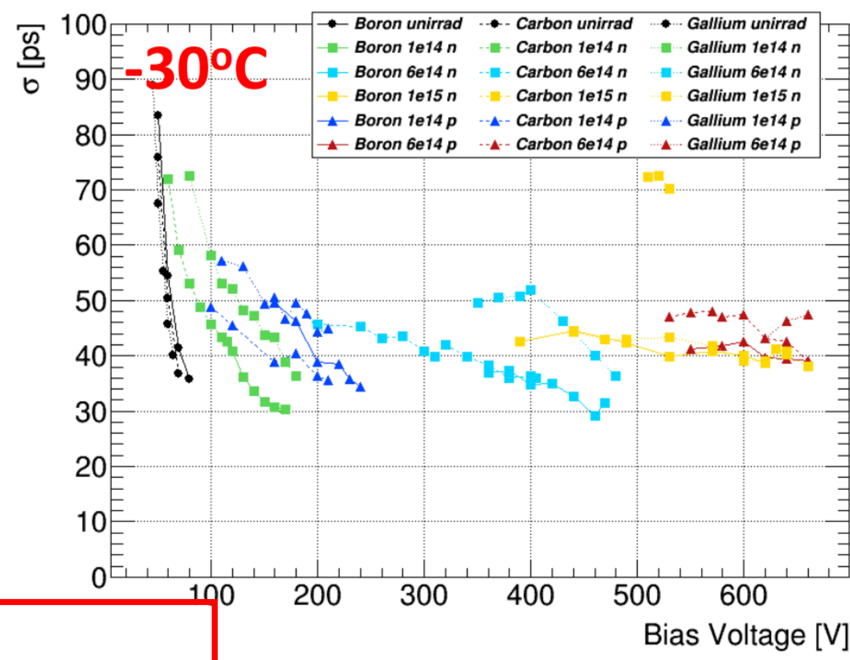
20÷40 ps time resolution, achieved through gain layer in thin sensors (35 μm to 50 μm)

Do not survive after $2.5 \cdot 10^{15}\ 1\ MeV\ n_{eq} cm^{-2}$

Strong dependance of gain variation to irradiation fluences

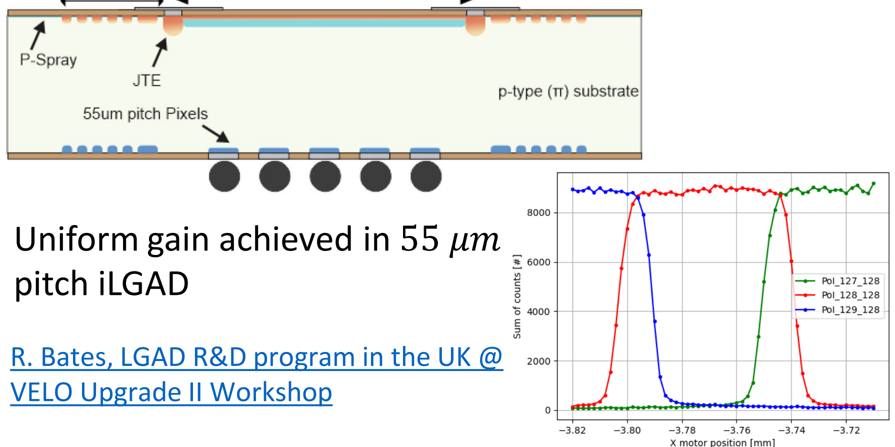
- Low fill factor with reduced pitch LGADs

R&Ds to reduce pitch and increase radiation hardness



Pitch reduction

iLGADs: readout on holes collection electrodes

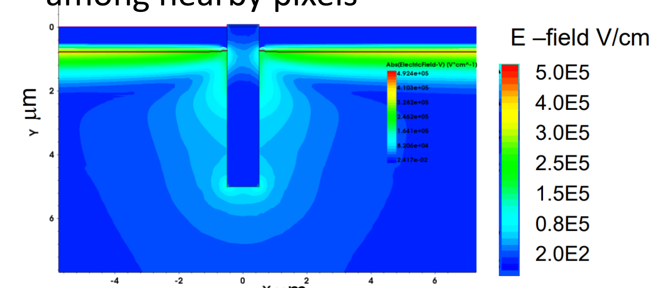


Uniform gain achieved in 55 μm pitch iLGAD

R. Bates, LGAD R&D program in the UK @ VELO Upgrade II Workshop

Trench isolated LGADs

Exploits physical trenches in the silicon substrate to provide electrical isolation among nearby pixels



Radiation hardness

- Ongoing studies to mitigate gain decreases with irradiation: several material implantation in gain layer (B, C, Li, In) to mitigate the effect

Radiation hardness must be increased by factor >2 to be considered for S_B

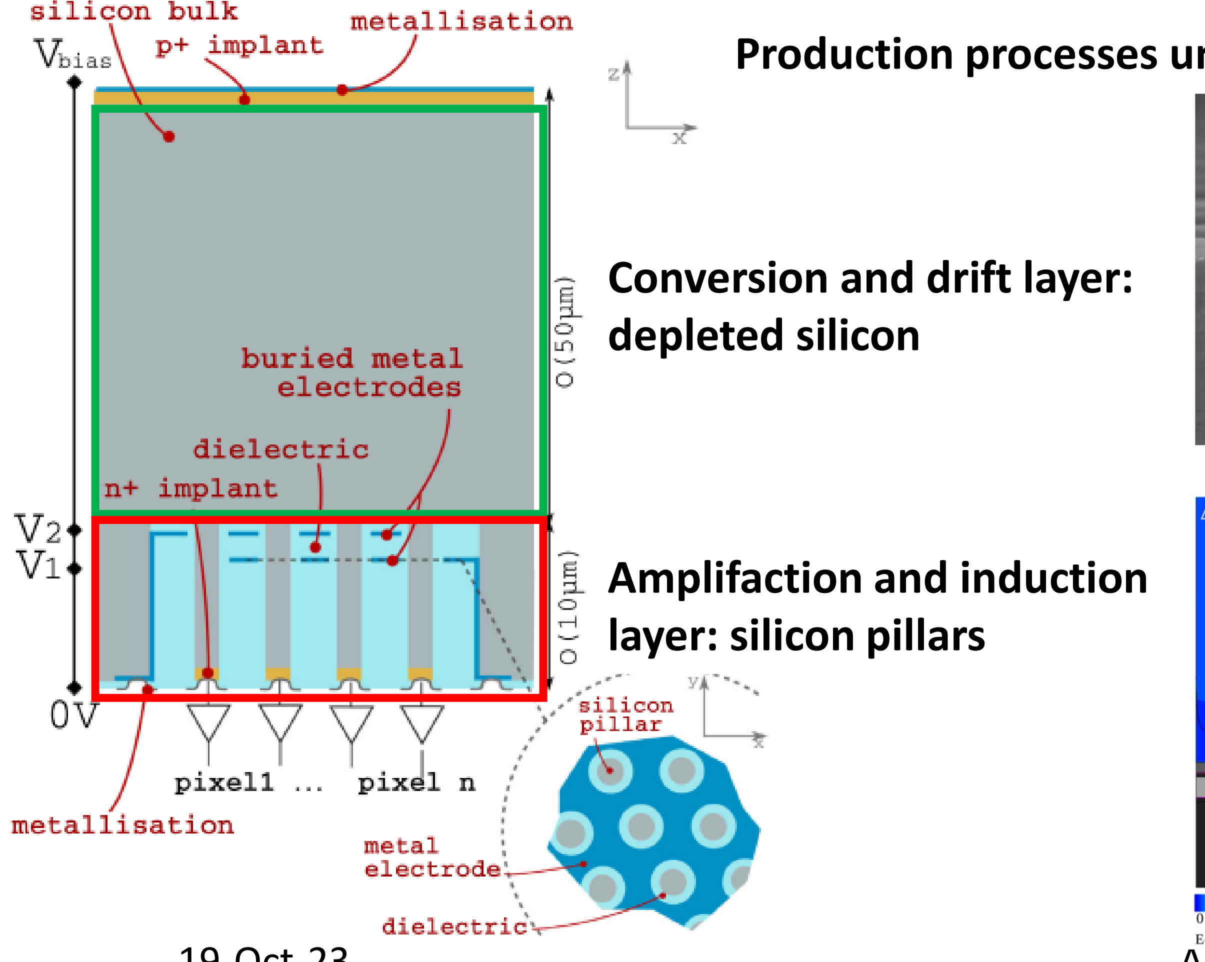
Silicon Electron Multiplier (SiEM)

New concept: **gain in silicon without doping**

The Silicon Electron Multiplier sensor, NIMA 2022

From simulations:

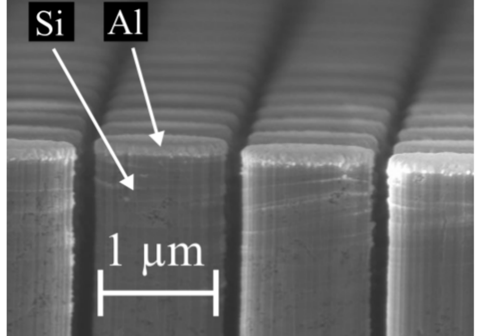
- Minimum pitch 10 μm
- Time resolution from 10 to 45 ps
- Radiation hardness up to $1 \cdot 10^{16}$ 1 MeV $n_{eq} cm^{-2}$

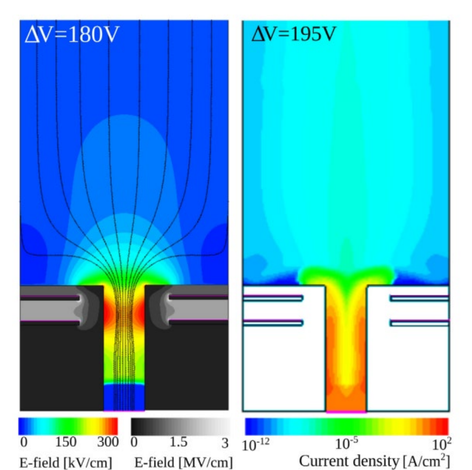


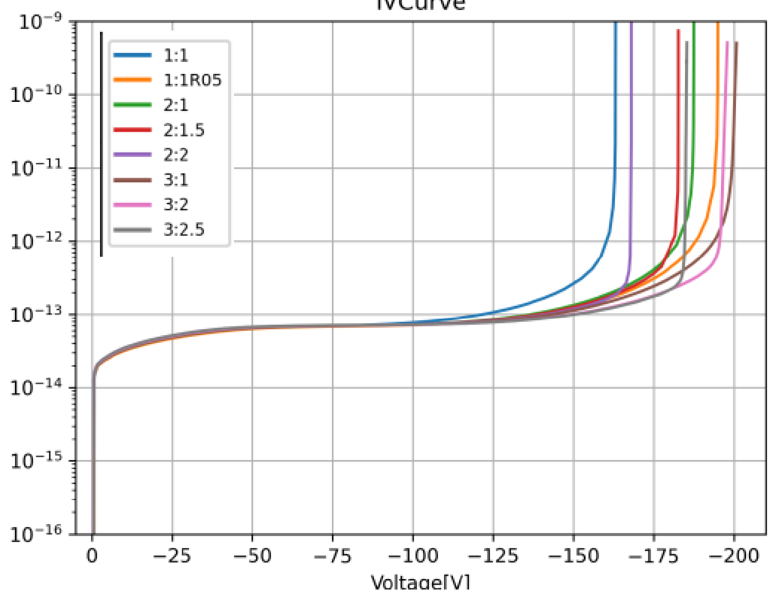
Production processes under study: DRIE (CNM), MacEtch (PSI, already produced)

Conversion and drift layer: depleted silicon

Amplifaction and induction layer: silicon pillars







Good electrical behaviour

Ongoing studies: laser and radioactive source characterizations

ASIC

Most challenging requirements toward a full 4D tracker

LHCb U2- From VELO support document for FTDR

Summary

Timing performances and **radiation hardness** with O(50 μm) **pitch**, **limited power budget** and **high data rate**

Requirement	scenario S_A	scenario S_B
Pixel pitch [µm]	≤55	≤42
Matrix size	256×256	335×335
Time resolution RMS [ps] **Mandatory**	≤ 30	≤ 30
Loss of hits [%]	≤ 1	≤ 1
TID lifetime [MGy]	> 24	> 3
ToT resolution/range [bits]	6	8
Max latency, BXID range [bits]	9	9
Power budget [W/cm^2]	1.5	1.5
Power per pixel [µW]	23	14
Threshold level [e$^-$]	≤ 500	≤ 500
Pixel rate hottest pixel [kHz]	> 350	> 40
Max discharge time [ns]	< 29	< 250
Bandwidth per ASIC of 2 cm^2 [Gb/s]	> 250	> 94

Mandatory to change the technology to overcome radiation hardness requirements: CMOS 28 nm

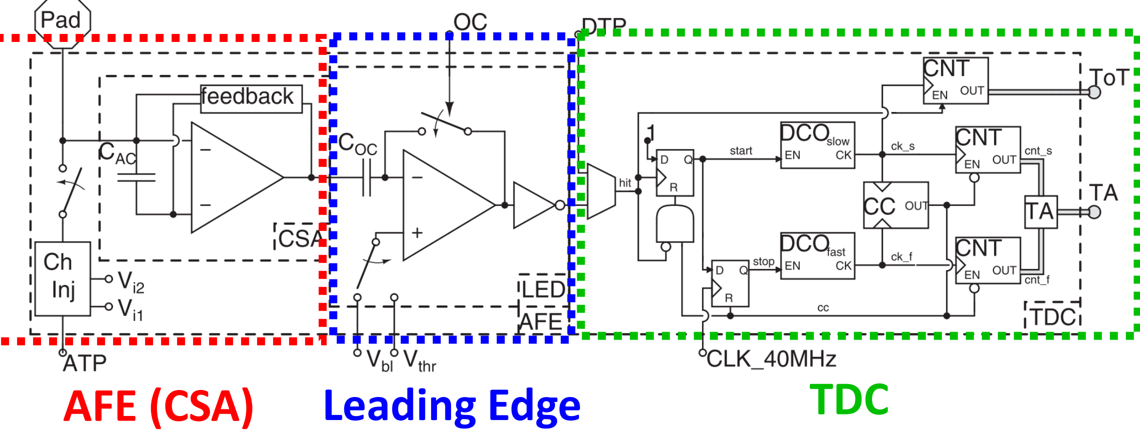
<u>**Two R&Ds focused on these technological aspects**</u>

PicoPix
(CERN, NIKHEF, IGFAE)

Timespot1 ASIC & Hybrid

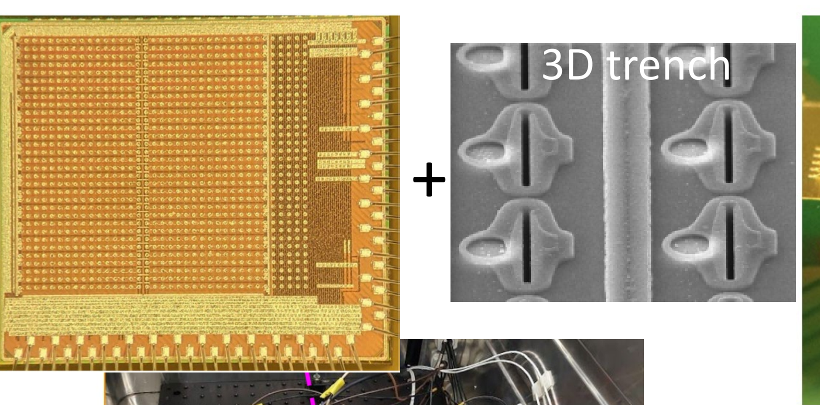
First development of an ASIC targetting LHCb VELO Upgrade II requirements

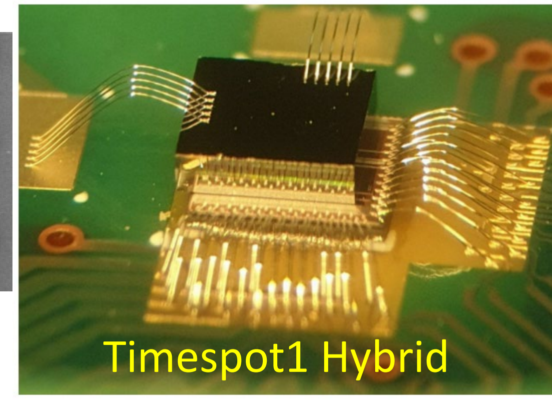
- 28 nm CMOS technology
- 32X32 channels, with a pitch of 55 μm
- Dimension: 66 mm^2



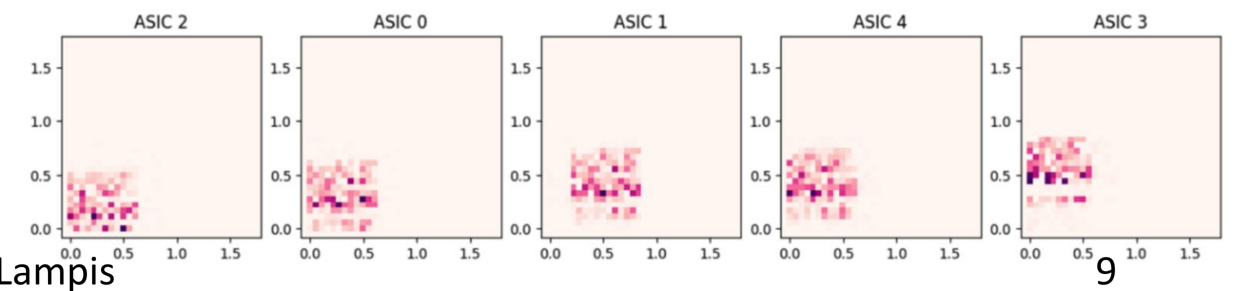
Charge injection tests showed **48 ps time resolution** high dispersion between pixels, (issue in the dynamic channel equalization method)

A. Lai (INFN) @ Pixel 2022





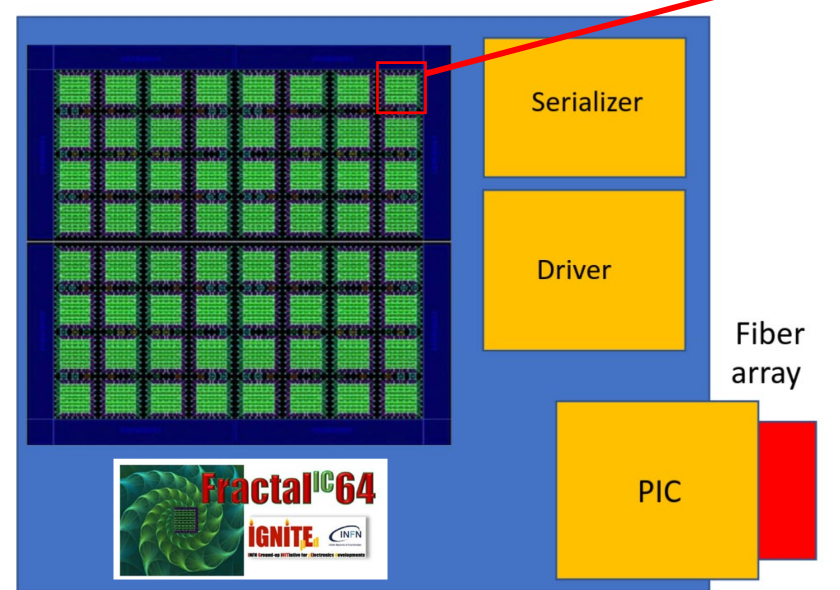
- Beam test @ SPS in 2023
- **First track ever reconstructed with 28 nm CMOS**
- Issue in biasing the sensor, max 1 V bias, time resolution around 200 ps dominated by sensor -> under investigation



INFN initiative involving 14 INFN institutes, 70 people (physicist and engineers), P.I. Adriano Lai (INFN Cagliari).

New project to develop a 4D tracking system by exploiting technologies oriented to the micro-integration at high-density in CMOS 28 nm to solve next experimental challenges of inner trackers in HEP (UII VELO first possible application)

First Matrix Prototype:
Fractalic64 will be submitted in 2024

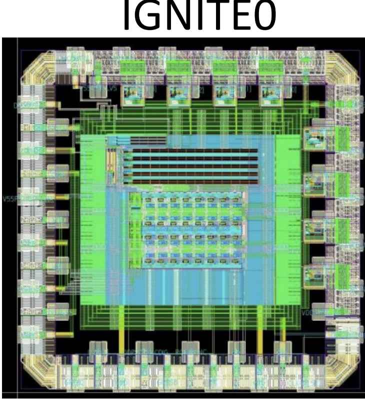


Single tile of 8x8 pixels

- 64x64 channels with a reduced pitch, (36 μm) **to be compatible with 45 μm or 55 μm pitch** by changing the top metal layer
- Individual 8×8 channels block is built as a repetition unit (spare area at the contour is used to place the service electronics)

Mini-asic to test components of Fractalic64 **submitted in July** (half version of the 8x8 matrix)

IGNITE0



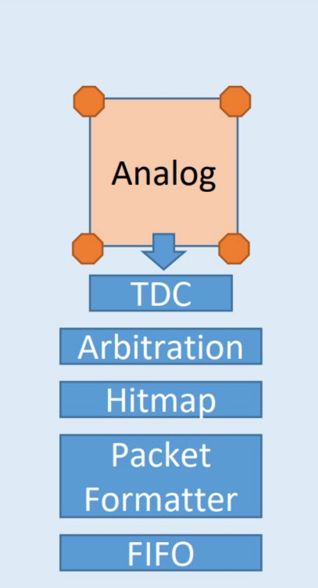
More information on Gian Matteo's talk

PicoPix (CERN, NIKHEF, IGFAE)

Exploration phase of the specs limitations for a large 30 ps ASIC, based on Timepix4 experience in TSMC 28 nm CMOS technology

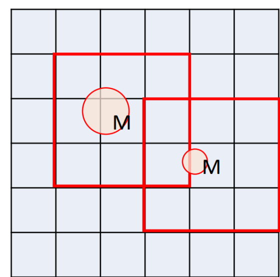
Two possible ASICs in line with the two VELO Upgrade II scenarios

SuperPixel



- Analog island containing 4 FE + 4 discriminator
- 1 TDC serving each analog island (input is the OR of 4 discriminator outputs)

Studies on solutions for on pixel event processing to reduce amount of data:



- Readout only the largest event in cluster (charge) and veto large clusters (>3x3)
- Best time (TOA) and energy (TOT) resolution and cluster hitmap

Study on solutions to mitigate performance non-uniformity in large area ASICSs due to power drop: studies of solutions with TSVs and on pixel power compensation

V. Sriskaran (CERN) @EP R&D Seminar

3.456 mm
Scenario A
Pixel Matrix
64x64 54µm
Periphery
3.456 mm
1 mm

2.88 mm
Scenario B
Pixel Matrix
64x64 45µm
Periphery
2.88 mm
1 mm

X. Llopart (CERN) @ VELO Upgrade II Workshop 2023

Submission expected on Q2/2024

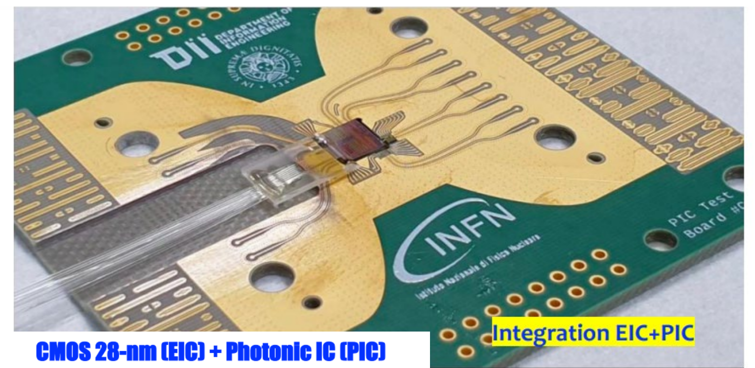
More information on Francesco's talk

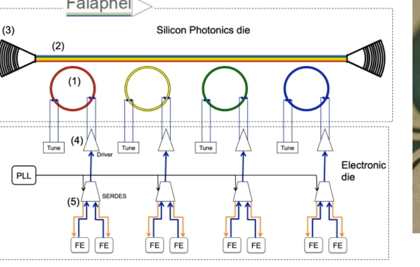
Data transmission

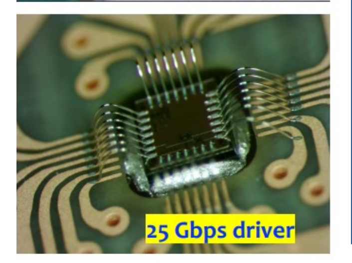
R&Ds in Silicon Photonics for High BW data transmission

- Chip FE (TSMC 28-nm)
- Serializer 12.5 Gbps (TSMC 28-nm)
- Driver 25 Gbps
- (TSMC 28-nm)
- Ring Modulator (Silicon Photonics)

Rad hard ring modulators 25 Gbps @ 1.25 GRad



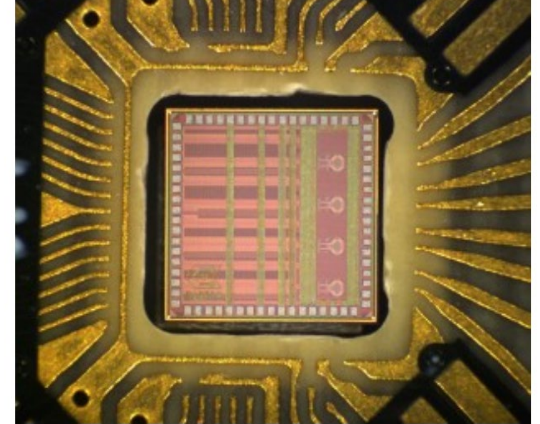




Requirement	scenario S_A	scenario S_B
Bandwidth per ASIC of 2 cm^2 [Gb/s]	> 250	> 94
	>10 times UI VELO	**5 times UI VELO**

DART28

Baszczyk @ TWEPP2023



- DART28 ASIC fully operational
- Able to operate @ 25.6 Gbps,
- Capable of driving 100 Ω transmission lines or optical ring modulators

Rad-hard measurements to be done

CERN PICs developments C. Scarcella @ TWEPP 2022

Dedicated R&D are needed also for **vacuum operation** (optical feedthrough)

RF foil

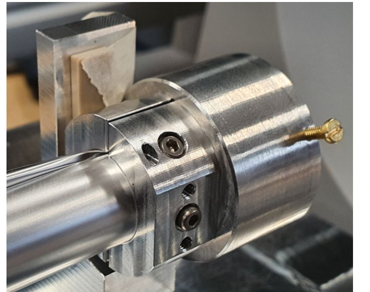
R&Ds results are fundamental also to fix the VELO Upgrade II design → RF foil in VELO Upgrade I (185μm Al Foil) accounts for 75% of the material. Scenario B requires lower material budget

In Upgrade I VELO fundamental for three main tasks:

- guarantee field continuity to LHC beams
- shield the detector electronics from RF pickup of the beams
- separate the high purity primary LHC vacuum from the secondary detector vacuum → Evaluation to combine CERN primary and VELO secondary vacuum volumes

Cylindrical Al thin foil

- 20 μm Al tensioned foil shield
- Tensions tests ongoing

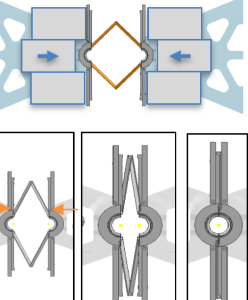


Wire mesh

- Proposed layout
- Feasibility studies are ongoing

Composite Shield
Ulta low Z material 120/60/30 um thick

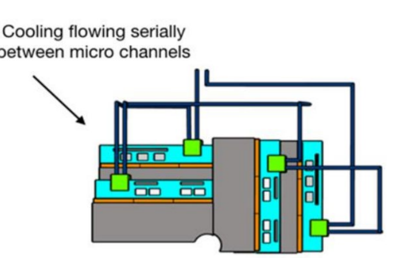
Mechanics for open and closed position



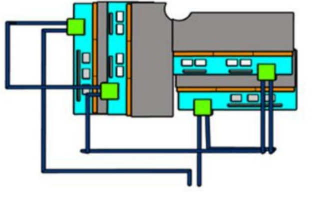
Cooling

- Fundamental to operate irradiated sensors
- Power budget of at least 1.5 W/cm^2 (in vacuum) mainly depends on cooling system, higher cooling capacity will benefits ASIC performances
- Limited material budget

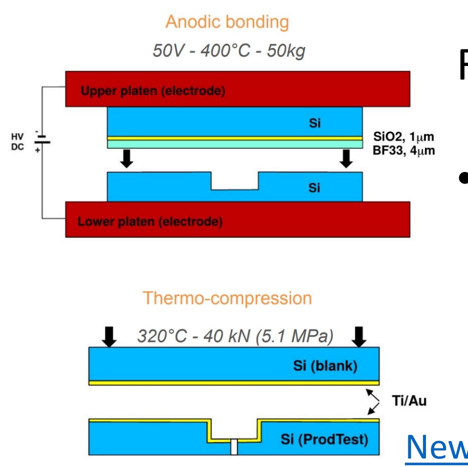
Several coolant under investigation: CO2, Krypton, Cryogenic



Two technologies under investigation



Microchannel substrate cooling



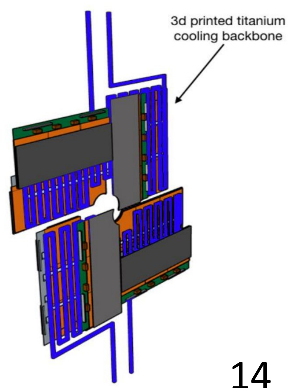
R&Ds ongoing:

- Microchannel laser etching, anodic or thermo-compression bonding to lower costs

[New Microchannels concepts @ VELO Upgrade II Workshop]

3D printing (Metal and Ceramics)

- Cheaper
- Easier to integrate
- More material



Conclusion

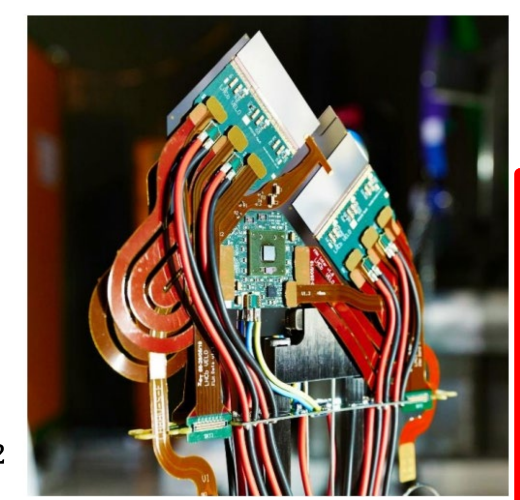
- Several R&Ds guided by two opposite detector scenarios toward the development of a 4D VELO detector
- Several sensor technologies are under investigation to be exploit in LHCb Upgrade II (3D, thin planar, LGAD and SiEM)
- Two projects are currently developing ASICs in CMOS 28 nm targeting Upgrade II VELO, both IGNITE and PicoPix will deliver first ASICs in 2024
- R&Ds to have thinner RF foils are ongoing
- Several coolant and cooling systems are under study

The development of the first full 4D vertex detector is an ambitious project, and it is also a huge opportunity to develop innovative technologies

BACKUP

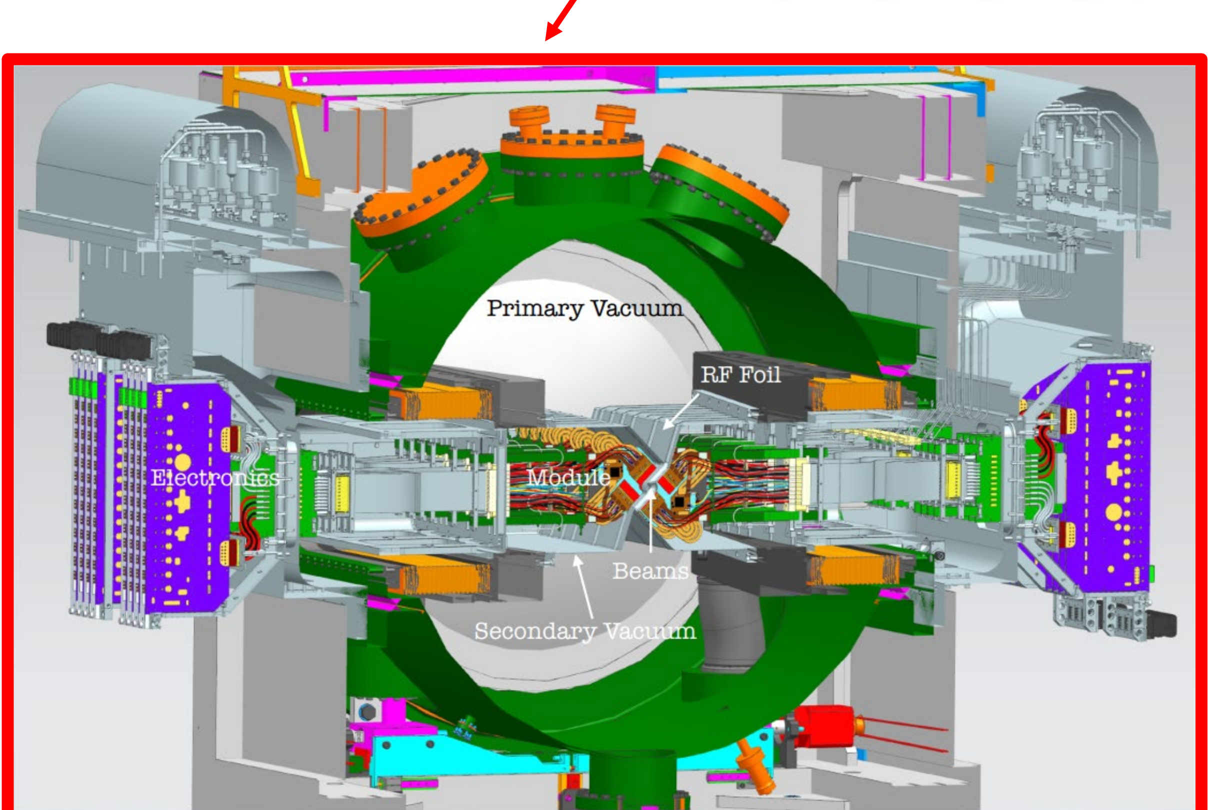
The LHCb VELO detector

VErtex LOcator (VELO) is a pixel detector for tracking particles close to the interaction region for the primary and secondary vertex reconstruction



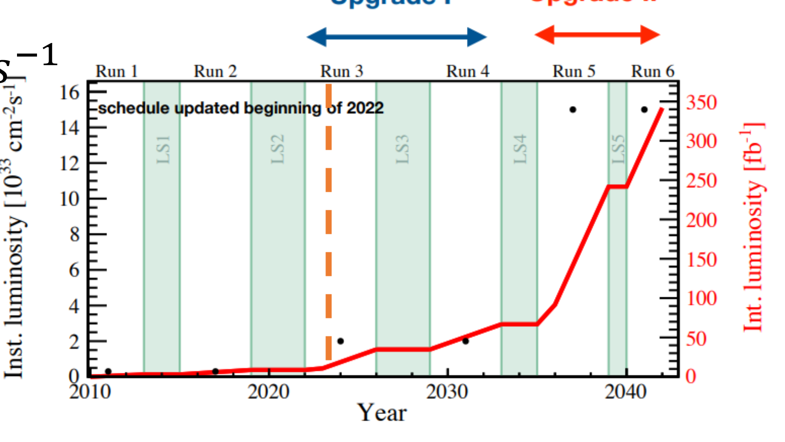
Upgrade I VELO

- Silicon pixel sensors
- 5.1 mm distance to LHC beams
- Radiation fluences up to $8 \cdot 10^{15}\ n_{eq} cm^{-2}$
- Operated in vacuum
- RF foil to isolate the detector from beam electromagnetic field
- Dedicated two-phase CO2 microchannel cooling to operate sensors at -20°C
- Movable detector to not interfere with LHC beam adjustments



Upgrade II VELO

From 2032 instantaneous luminosity @LHCb from $2 \cdot 10^{33}\ cm^{-2}s^{-1}$ to $1.5 \cdot 10^{34}\ cm^{-2}s^{-1}$

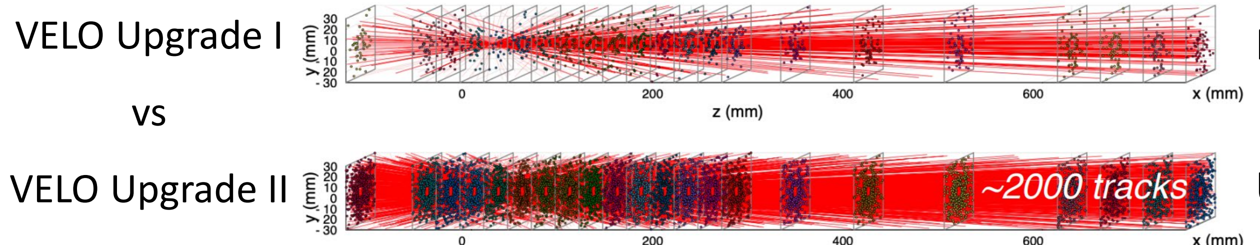


Higher luminosity -> higher pile-up, radiation damage and data rate on detectors

VELO Upgrade I

vs

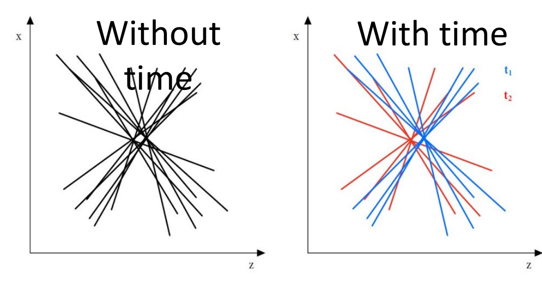
VELO Upgrade II



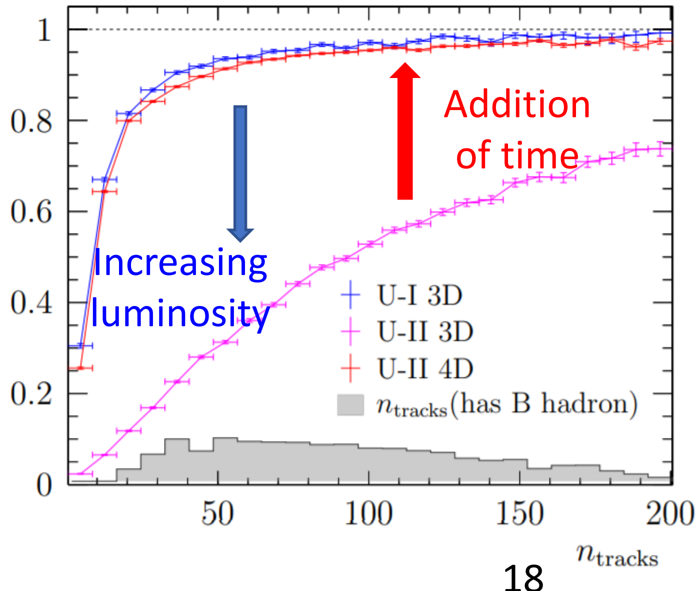
Run 3 pile up $\sim \mathbf{6}$

Tracking performances of the Upgrade I VELO in the high luminosity condition will significantly drop due to the higher number of particle to be detected simultaneously.

By measuring the **time of the tracks** with an accuracy of 50 ps per hit it is possible to recover the performances of current detector in high luminosity condition



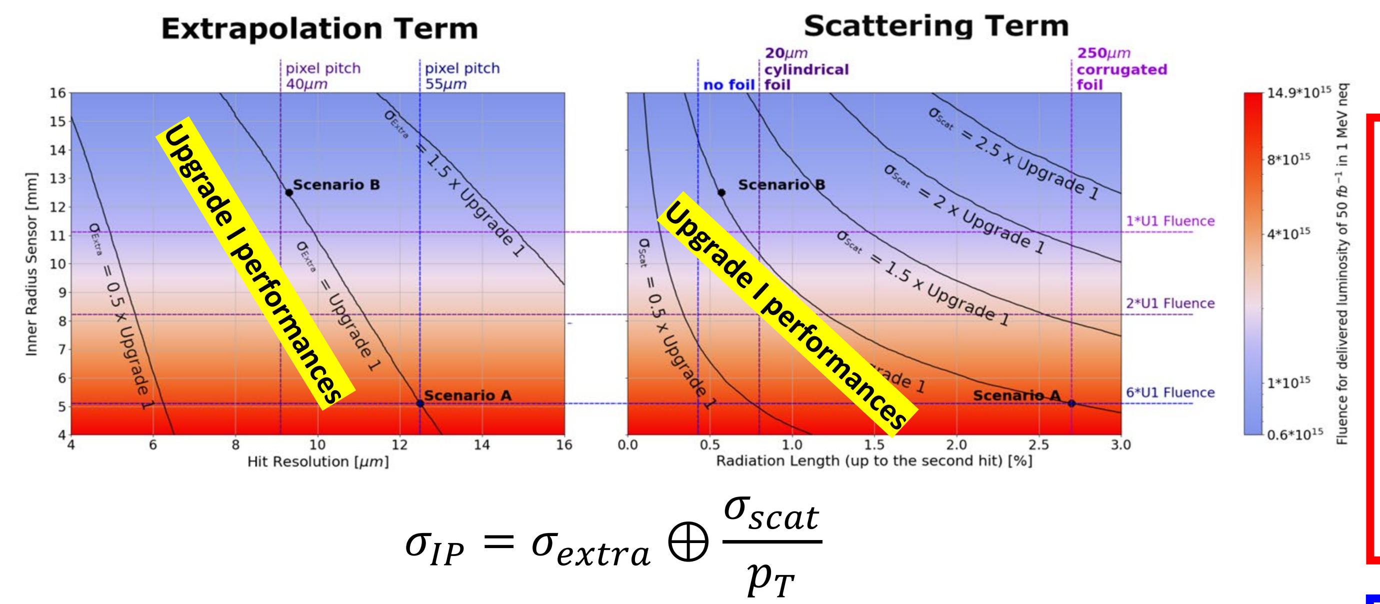
A 4D VERTEX DETECTOR IS REQUIRED TO MAINTAIN PERFORMANCES



Framework TDR for the LHCb Upgrade II

Detector layout

Distance from the beam has sever impact to technical requirements



$$\sigma_{IP} = \sigma_{extra} \oplus \frac{\sigma_{scat}}{p_T}$$

On this talk status update on R&Ds for:

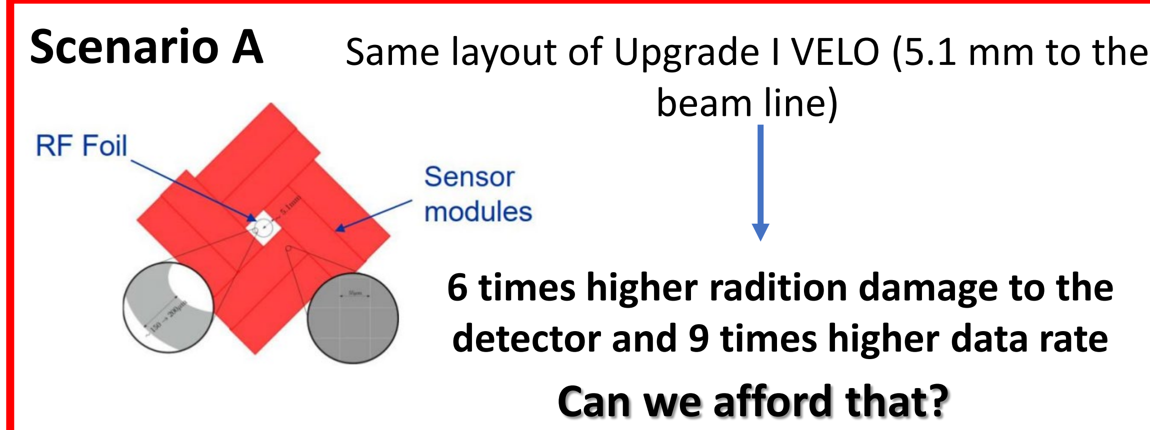
Sensors **ASICs** **RF foil** **Cooling**

<u>The real scenario will be defined according to R&D results</u>

Two opposite scenarios which both guarantee same performances of Upgrade I VELO to guide R&Ds

Scenario A

Same layout of Upgrade I VELO (5.1 mm to the beam line)

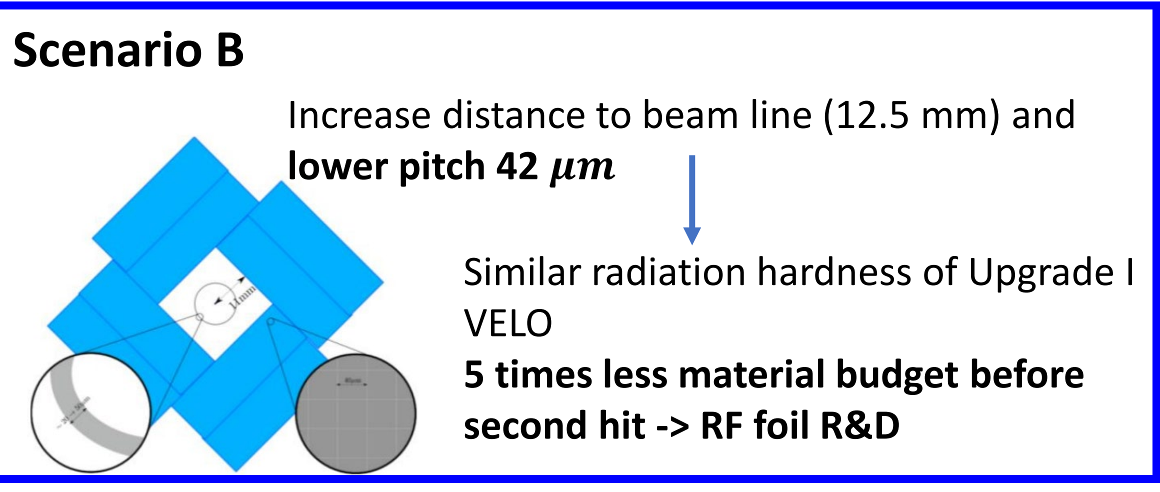


6 times higher radition damage to the detector and 9 times higher data rate

Can we afford that?

Scenario B

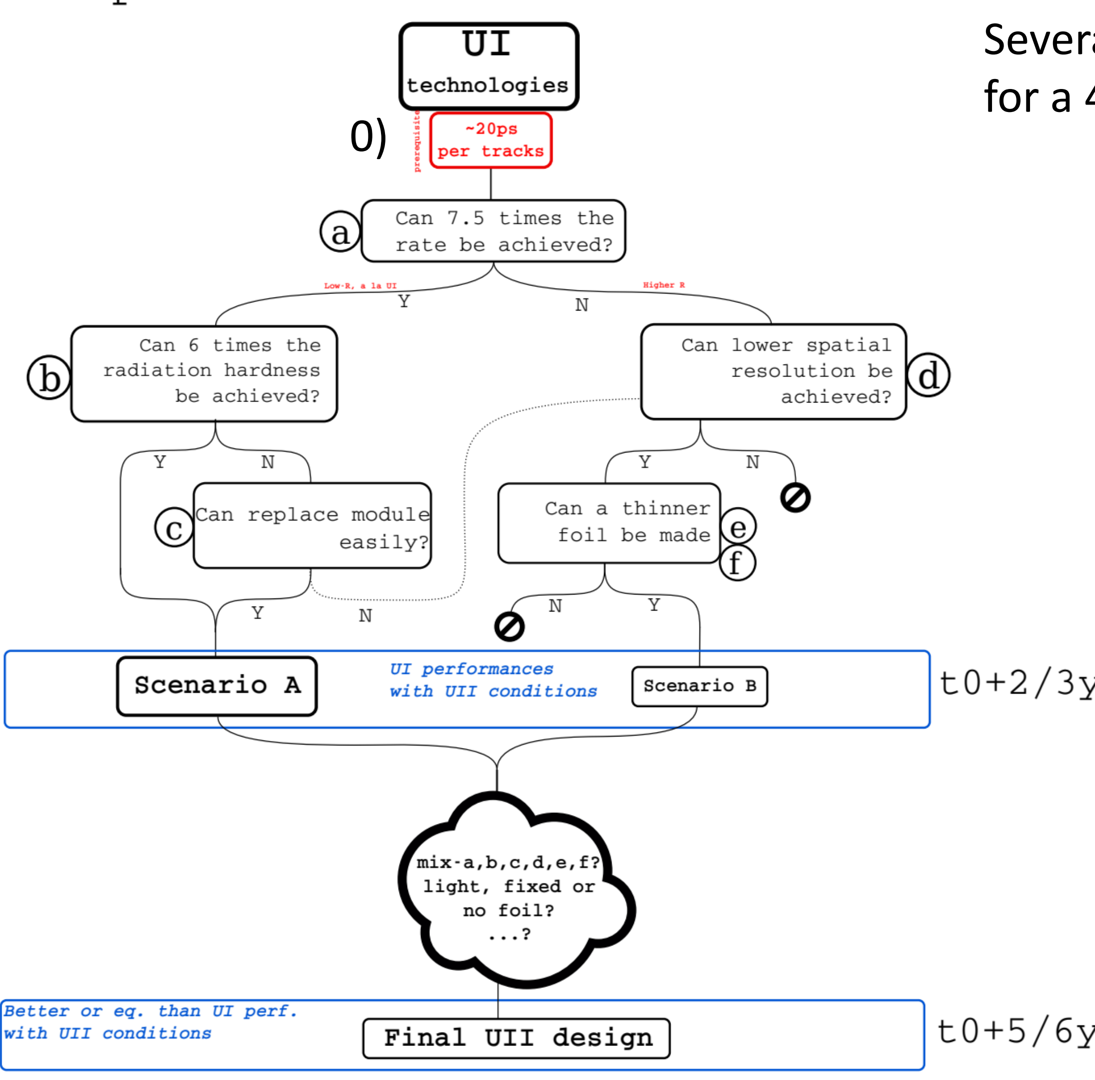
Increase distance to beam line (12.5 mm) and **lower pitch 42 μm**



Similar radiation hardness of Upgrade I VELO

5 times less material budget before second hit -> RF foil R&D

R&D path



Several R&Ds have been launched to cover all technological requirements for a 4D tracker able to deal with VELO Upgrade II specs

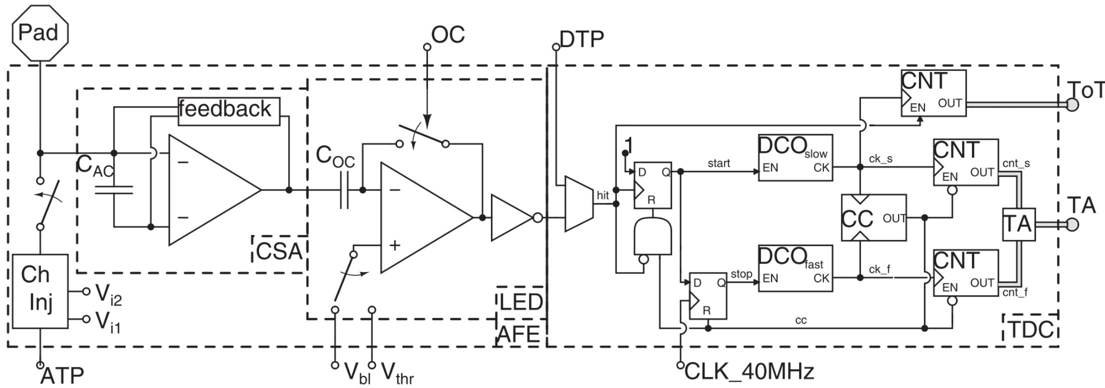
0) Time resolution of 20 ps (50 ps) per track (hit)

a) ASIC design allowing for high rate and high bandwidth + high speed link
b) ASIC and sensors able to survive Upgrade 2 particle fluences
c) Easy to make modules and mechanics allowing replacement
d) Lower spatial resolution (charge sharing or pixel pitch), IC and sensor
e,f) Ability to make a thin movable foil

TimeSPOT 1 ASIC

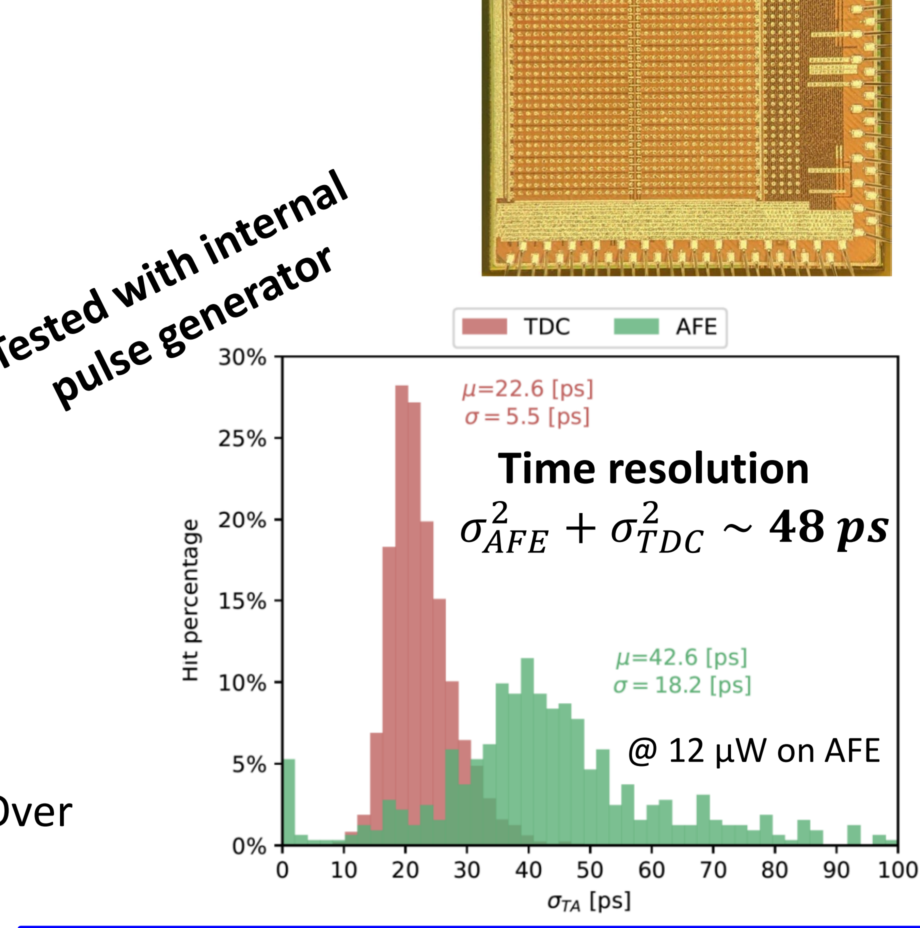
First development of an ASIC targetting LHCb VELO Upgrade II requirements

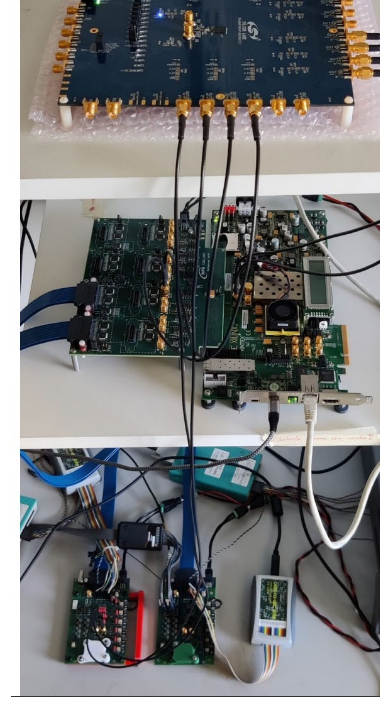
- Developed in a commercial 28 nm CMOS technology
- 32X32 channels, with a pitch of 55 μm
- Dimension: 66 mm^2



- For each channel AFE + Leading edge discriminator + TDC
- For each channel 23 bit world TA (Time of Arrival) + Time Over Threshold (TOT) trasmitted serially (LVDS) at 160 MHz

A. Lai (INFN) @ Pixel 2022





48 ps time resolution but too high dispersion between pixels, issue with the dynamic channel equalization method