Imperial College London

Track finder for the Phase-2 Upgrade of the CMS Level-1 Trigger

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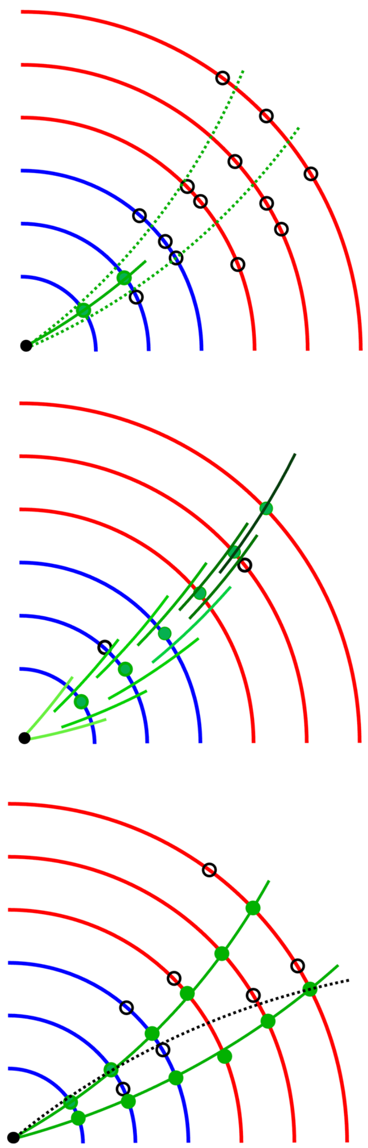
on behalf of the CMS Collaboration

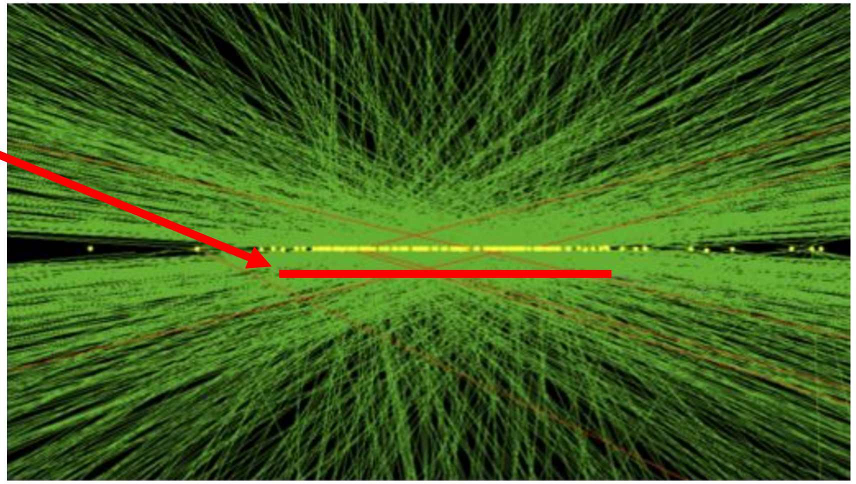
19^{th} October 2023

Introduction

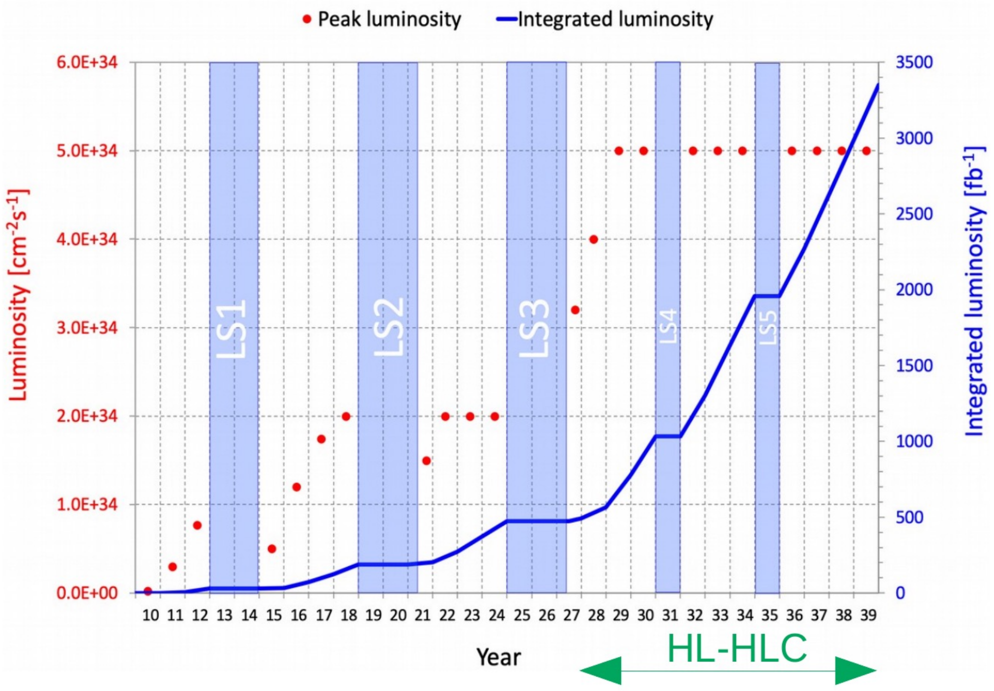
- HL-LHC
- CMS Phase-2 Upgrade
  - Trigger & Tracker
- Track Finding for the Level-1 Trigger
- Hybrid algorithm
  - Tracklet Pattern Recognition
  - Kalman Filter
  - Performance
  - Track Quality
- Firmware Implementation
- Hardware and Integration Testing



HL-LHC



- 3000-4000 fb^{-1} over the HL-LHC lifetime
- Good for rare BSM physics searches and SM precision measurements
- Simultaneous proton-proton interactions per bunch crossing (pileup) rising to 200 at 40 MHz
- Current era CMS cannot cope without loss in physics performance
- Radiation damage too high for current CMS tracker and endcaps
- CMS needs to be upgraded and the Level-1 trigger is a major part of these upgrades

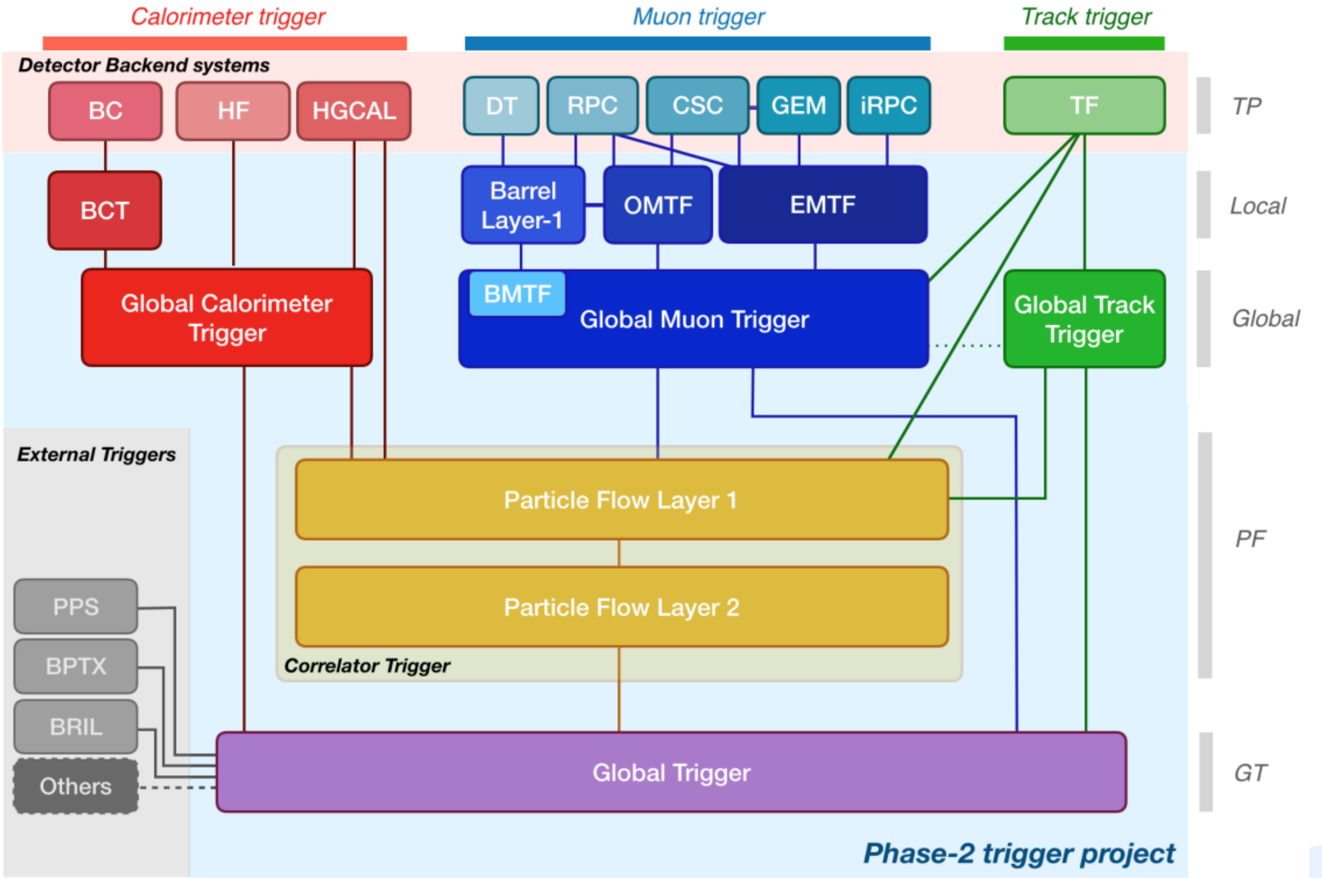


CMS Phase-2 Upgrade

- HGCal -> particle flow focused calorimeter
- Upgraded tracker, higher η coverage and Level-1 track finding
- Upgraded muon chambers, increased redundancy

Level–1 Trigger

- ~110 kHz → 750 kHz rate
- ~4 μs → 12.5 μs latency
- Big FPGAs → flexibility
- Upgraded HGCal and Calorimeter backend electronics, high granularity at L1
- Tracks from outer tracker at L1, full 40 MHz readout
- Can perform PF and vertex finding for particle per pileup identification



CMS Phase-2 Level-1 Trigger TDR

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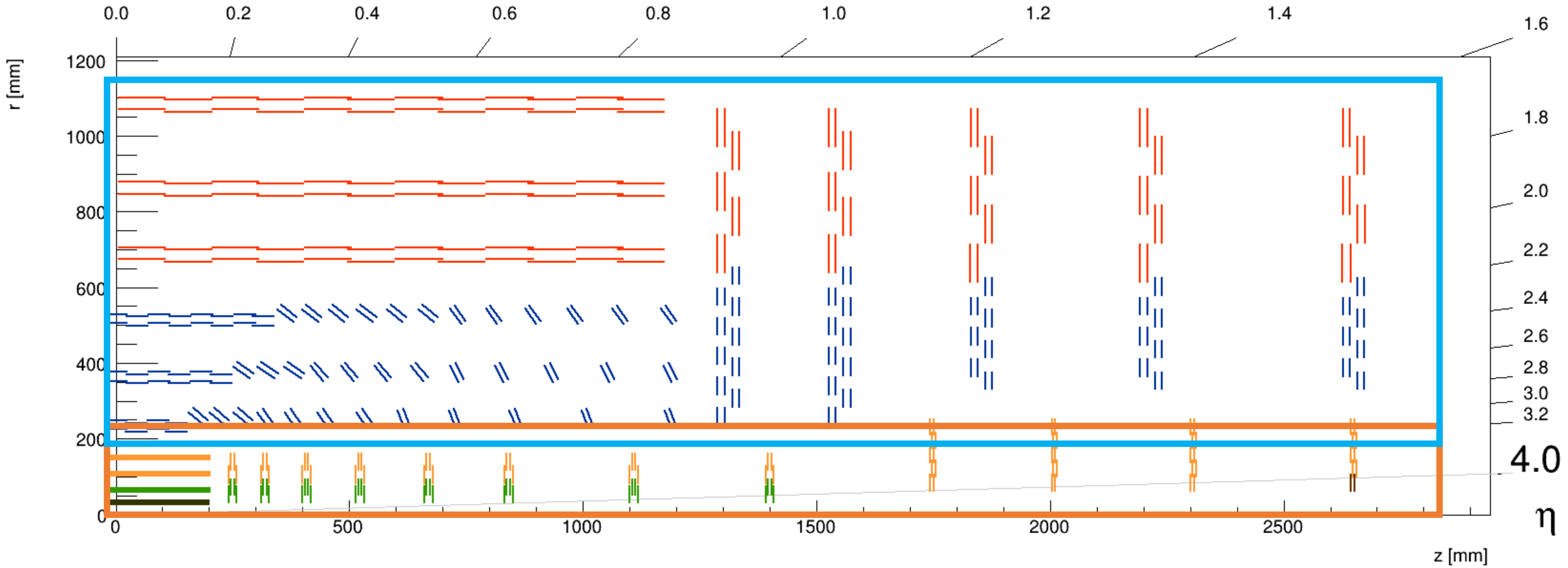
Tracker Upgrade



Inner tracker
- |η| up to 4
- Pixel sensors 25 x 100 μm² pixels
- Replaceable 3D pixel inner layer

Lea's Talk

Outer tracker
- Instrumented up to |η| = 2.8
- L1 track finder limited to |η| = 2.4

PS modules → pixel-strip modules

2S modules → two strip modules

Irene's Talk

CMS Phase-2 Tracker TDR

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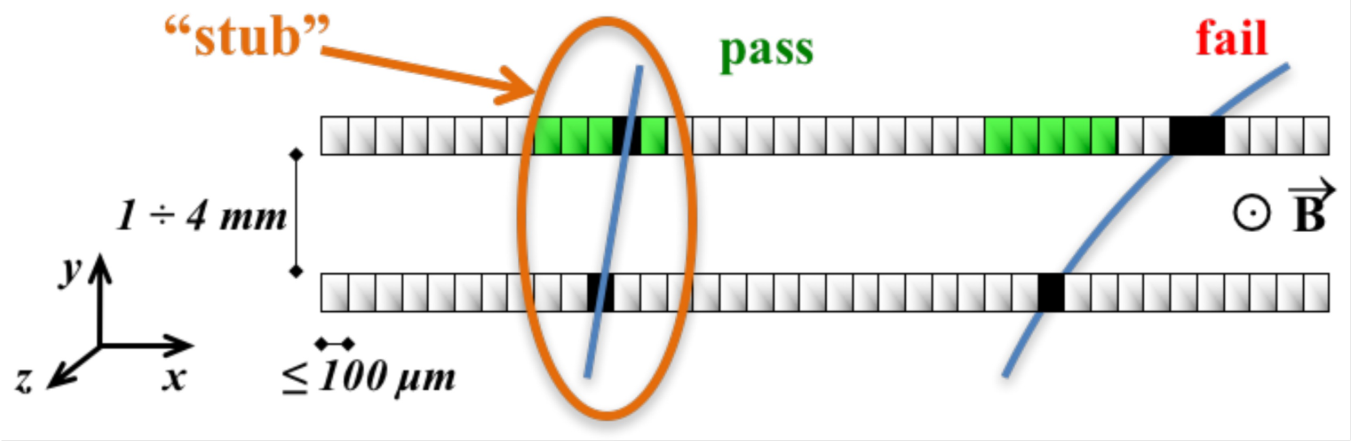
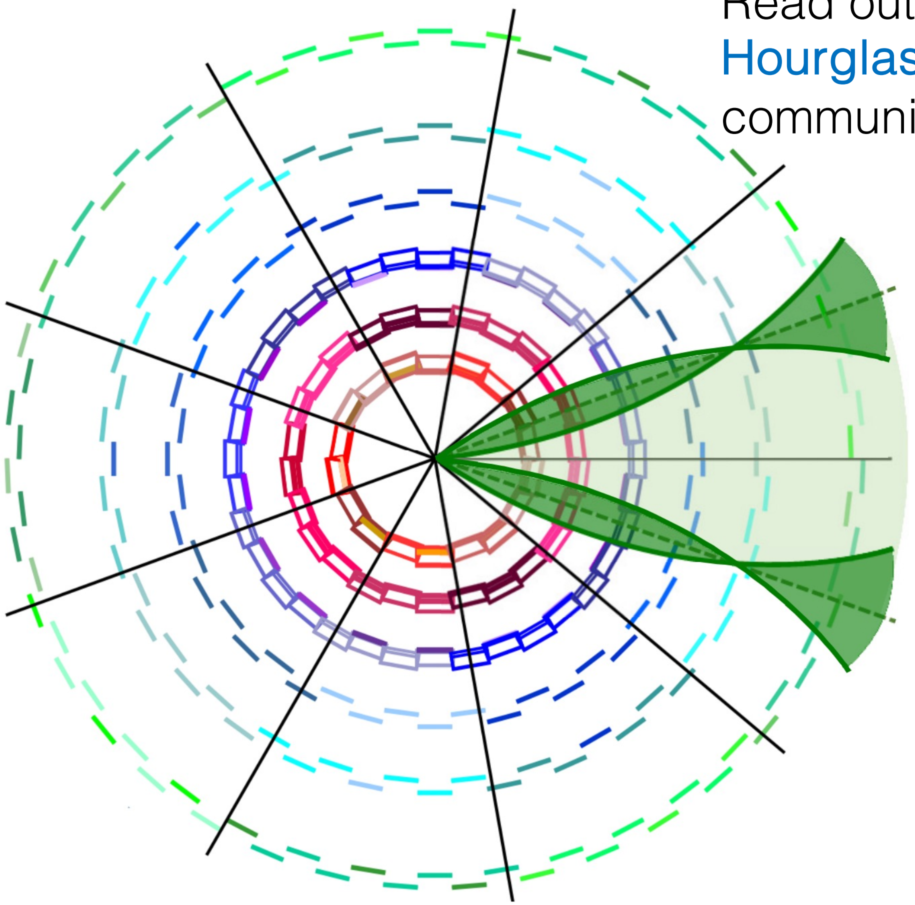
Tracker Upgrade

p_T modules

- 2 closely spaced layers of silicon
- Tuneable window give on module p_T cut
- Both types of outer tracker module contain p_T modules
- Can't have stereo strips → but need precise z_0 coordinates so use pixel-strip modules
- Reduces data rate enough for track finding at 40 MHz
- 1 mm z_0 resolution allows a vertex to be found in 200 pileup



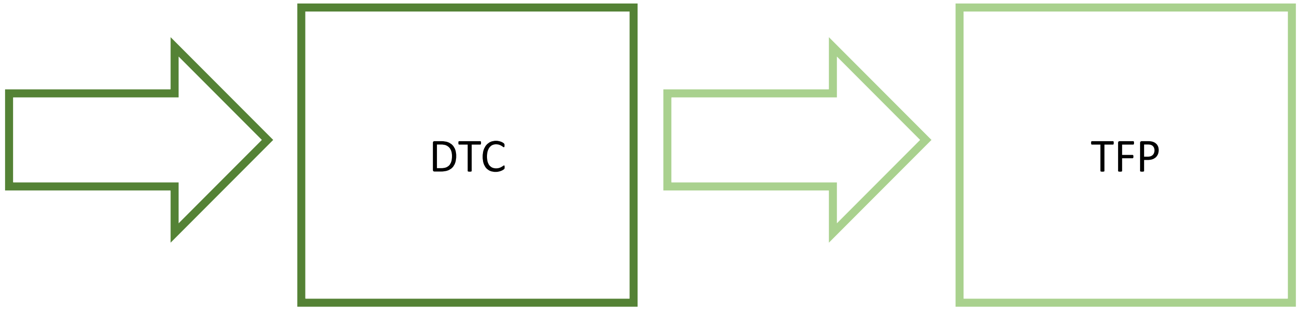
Tracks for Level-1 → System Overview



Read out tracker in nonants
Hourglass shape avoids inter-nonant communication

Track Finder Processor

- 18 boards per nonant
- New event every 450 ns
- 4 μs to process tracks



Data Trigger and Control

- 24 boards per nonant
- Stub pre-processing, distribute stubs to track finder
- Forwards rest of data on L1 accept

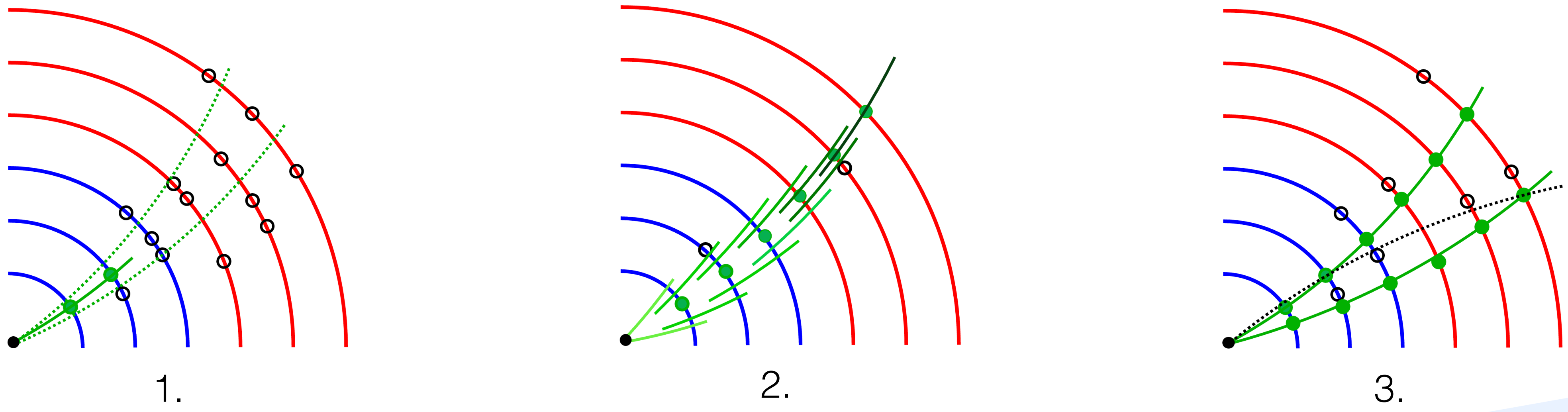
Hybrid Algorithm

Reconstruct all tracks $p_T > 2$ GeV, $|\eta| < 2.4$

4 μs to process over 10,000 stubs and form $\mathcal{O}$ (100) prompt tracks per event

Hybrid algorithm

1. Road search algorithm based on tracklet seeds
2. Kalman filter for identify best stub candidates and track parameters
3. Boosted decision tree to evaluate track quality



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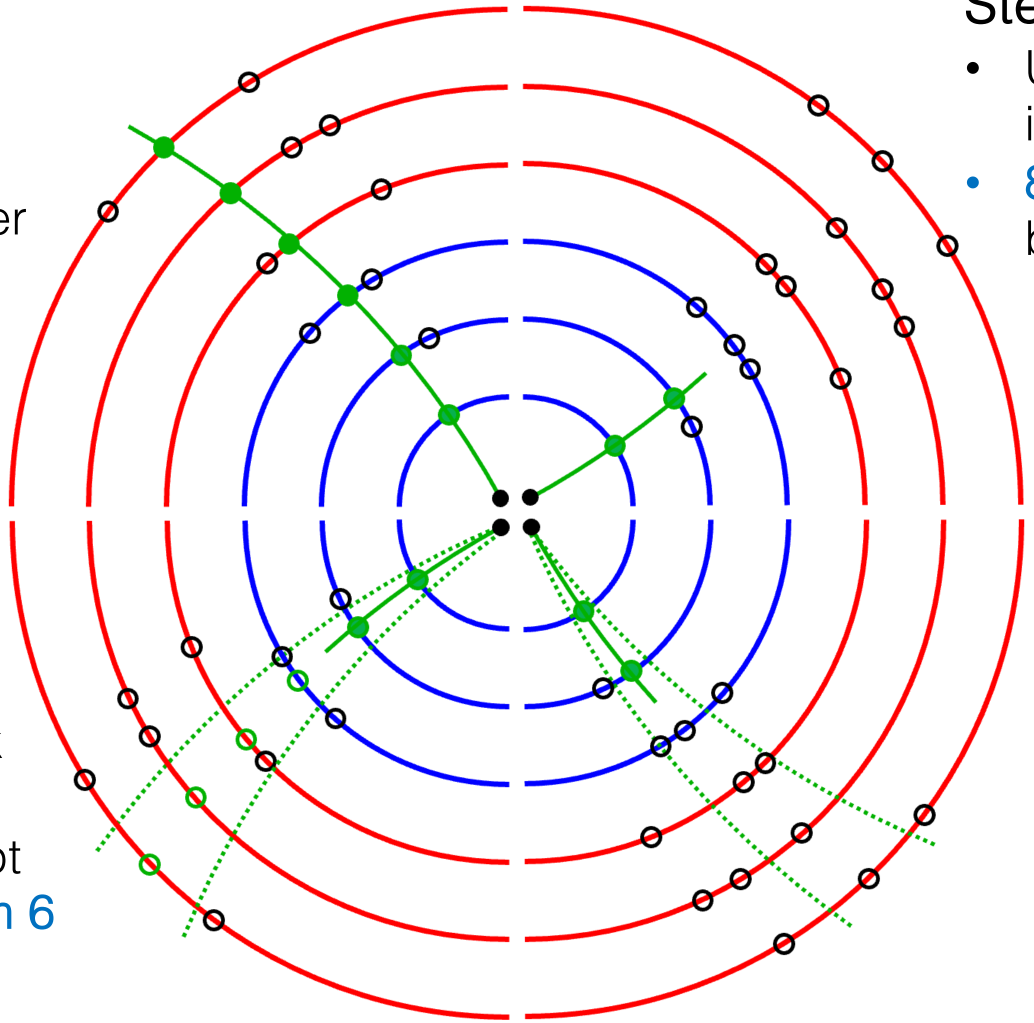
Hybrid Algorithm - Tracklet

Step 1
- Use two stub seeds to create initial tracklets
- 8 different combinations of barrel and endcap layers

Step 2
- Project track candidates outwards/inwards
- Based on a beamspot constraint
- Create a search window for more stubs

Step 3
- Add matching stubs to track candidate
- Smallest residual stub is kept
- Minimum 4 stubs, maximum 6 stubs for a track

Step 4
- Pass track candidates downstream to track merger and Kalman Filter



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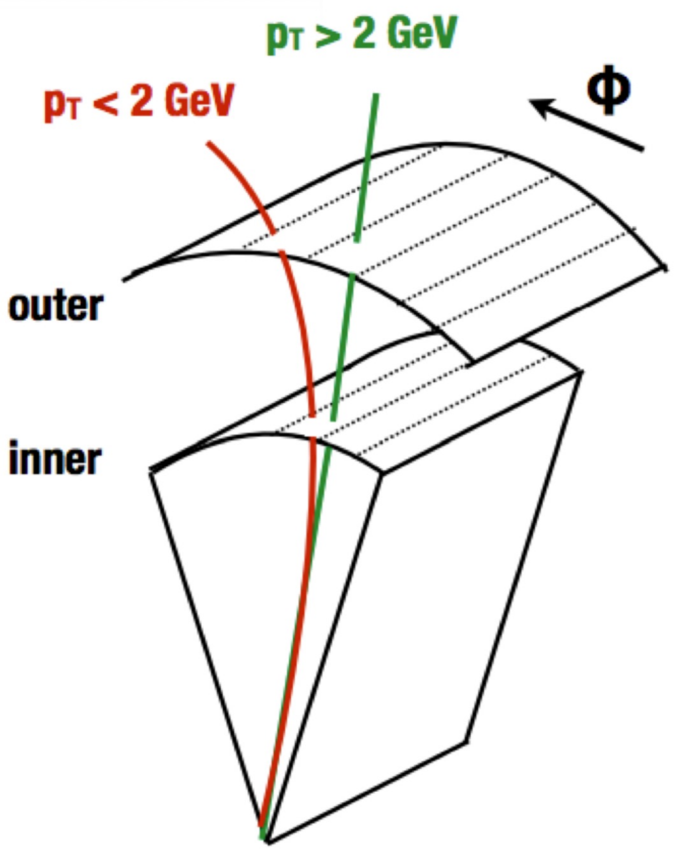
Hybrid Algorithm - Tracklet

- Use virtual modules binning stubs in fine ϕ regions so that only stub combinations $p_T > 2$ GeV are considered
  - Minimises combinatorics
  - Simplifies firmware

- Seeds are considered multiple times in parallel for efficiency

- Tracks with shared stubs are merged to reduce duplicates



FPGA-Based Tracking for the CMS Level-1 Trigger using the Tracklet Algorithm

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Hybrid Algorithm – Kalman Filter

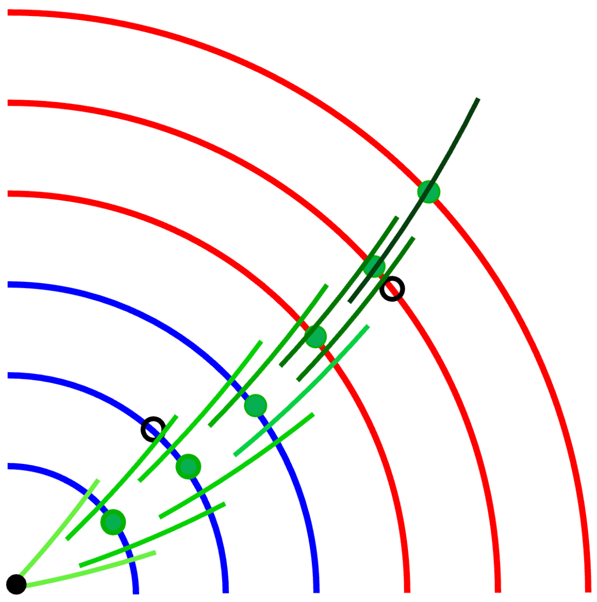
- Takes track candidates and track residuals to form Kalman filter state and covariance matrix respectively

- Stubs are iteratively added a layer at a time in a state propagation and state update

- State propagation estimates the track in the next layer

- State update uses the recorded stubs and their uncertainties to improve the track state, removing any tracks with incompatible stubs

- Track fit iteratively improves as stubs are added



[An FPGA Based Track Finder for the L1 Trigger of the CMS Experiment at the High Luminosity LHC]

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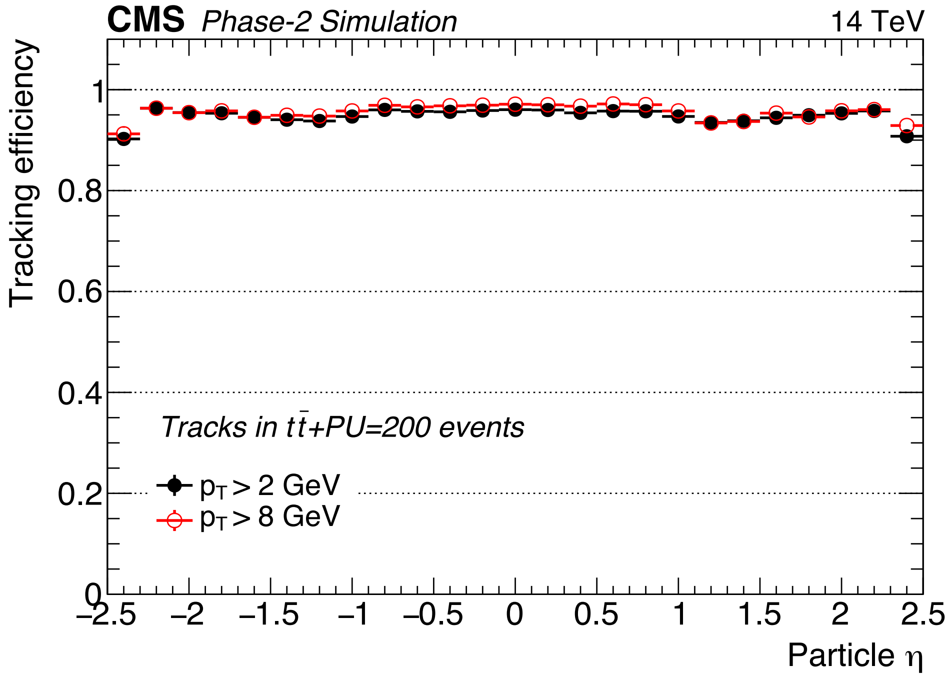
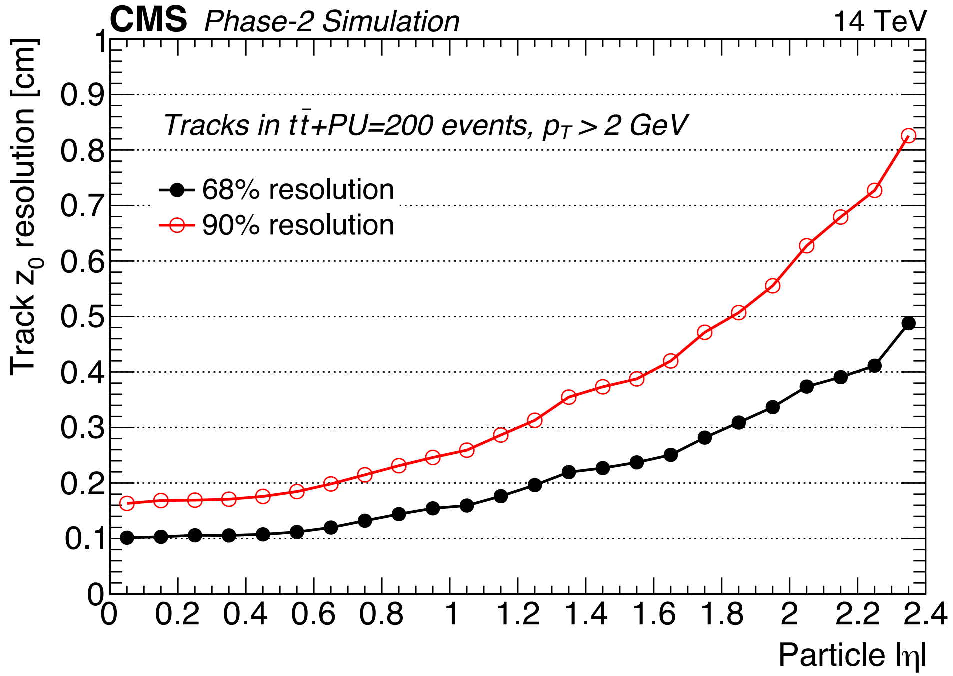
Hybrid Algorithm - Performance





High efficiency across η

Transition regions see fewer layers crossed so slight dip in efficiency at η = 1

1 mm z_0 resolution for tracks → good enough for vertex association in 200 PU

Worse resolution in η because of barrel geometry

[CMS Phase-2 Level-1 Trigger TDR](#)

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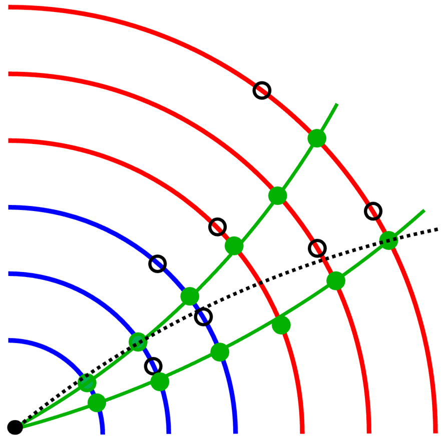
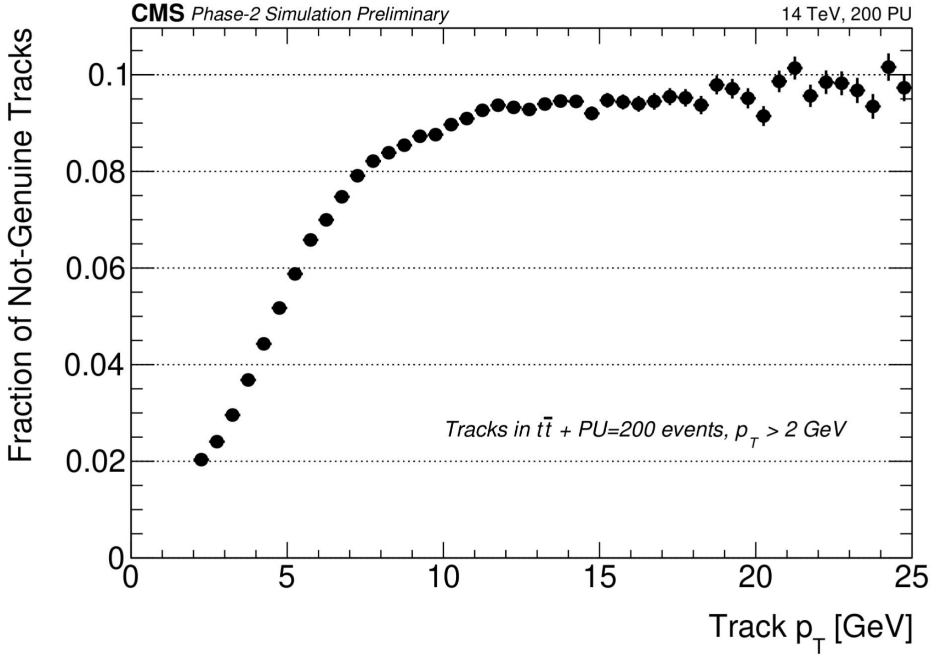
Hybrid Algorithm – Track Quality

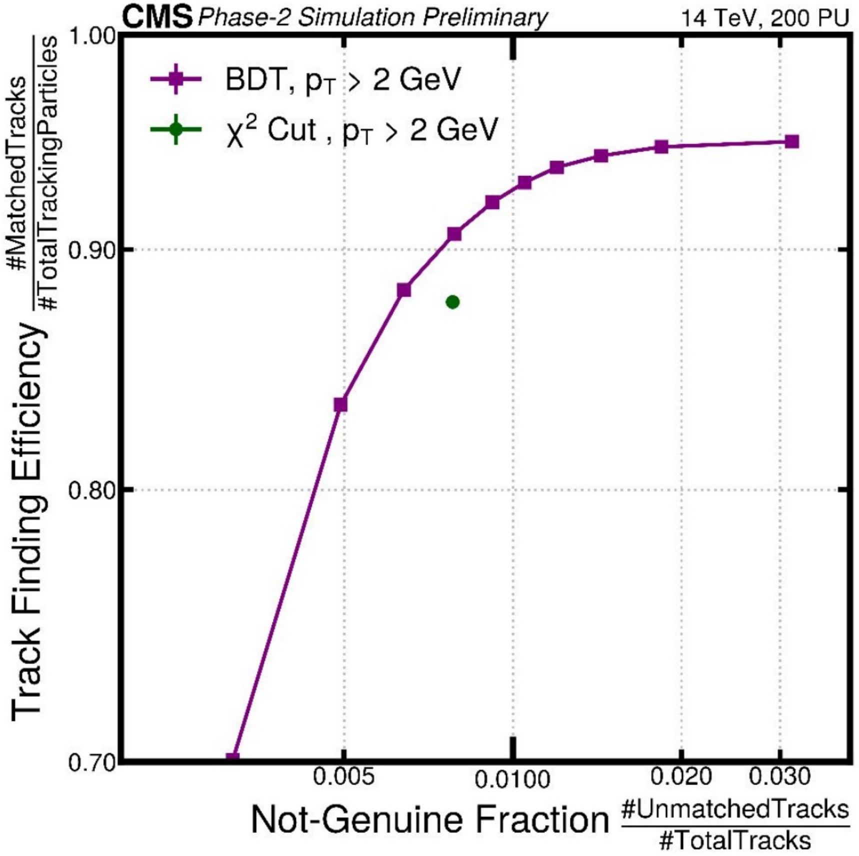


- High fake rate → tracks not coming from genuine charged particles
- Issue for algorithms such as E_T^{miss} where single high p_T tracks can reduce efficiency
- Kalman Filter calculated χ^2 fit parameters
- Can use these to reduce fake tracks → handle for downstream algorithms



Hybrid Algorithm – Track Quality

- Complex dependence of χ^2 in different η and z_0 regions
- Single cut on χ^2 cannot account for these interdependencies
- Simple boosted decision tree (60 trees, 3 deep) can improve identification
- Can be retrained and tuned as track finding evolves
- Single value for downstream users



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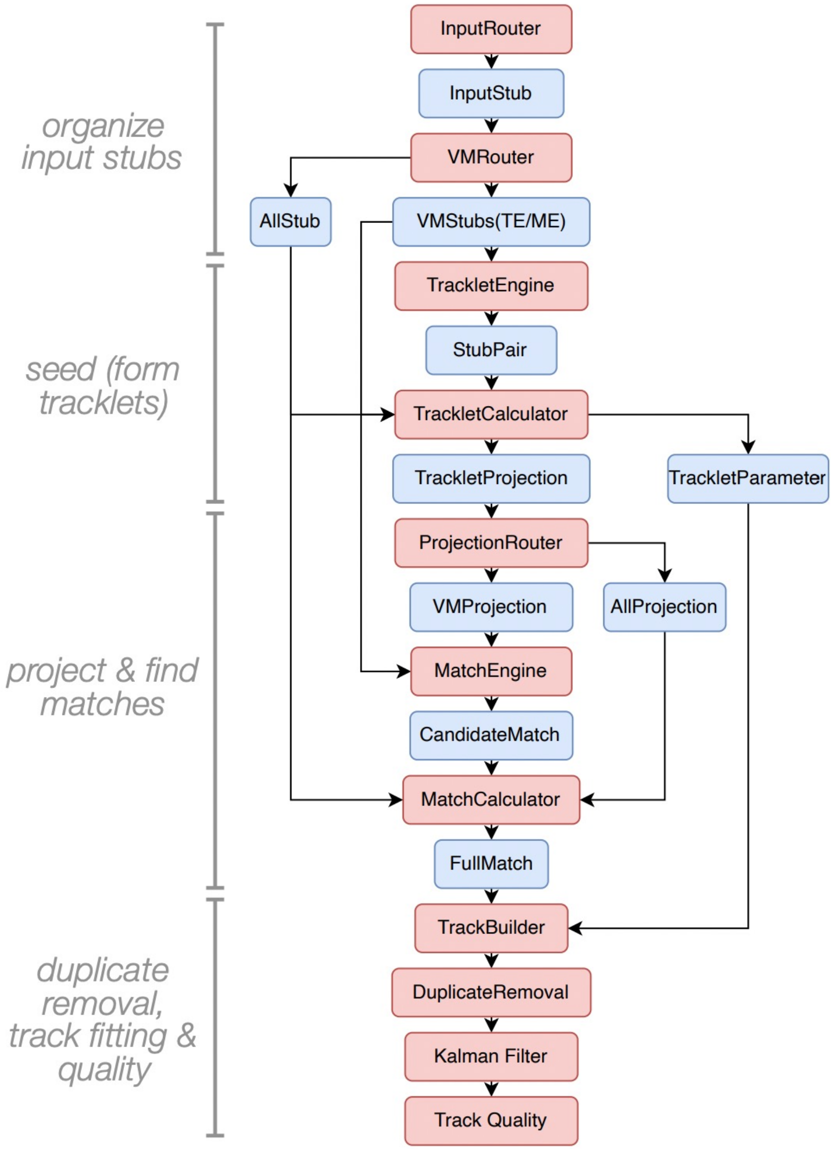
Firmware Implementation

- Pattern recognition firmware implemented in Vivado HLS
- Processing modules and memory modules interspersed
- Multiple copies in parallel
- Wiring map to control wiring between processing and memories
- Kalman filter in VHDL
- Track quality BDT implemented in VHDL
- Targetting 240 MHz clock
- All modules completed



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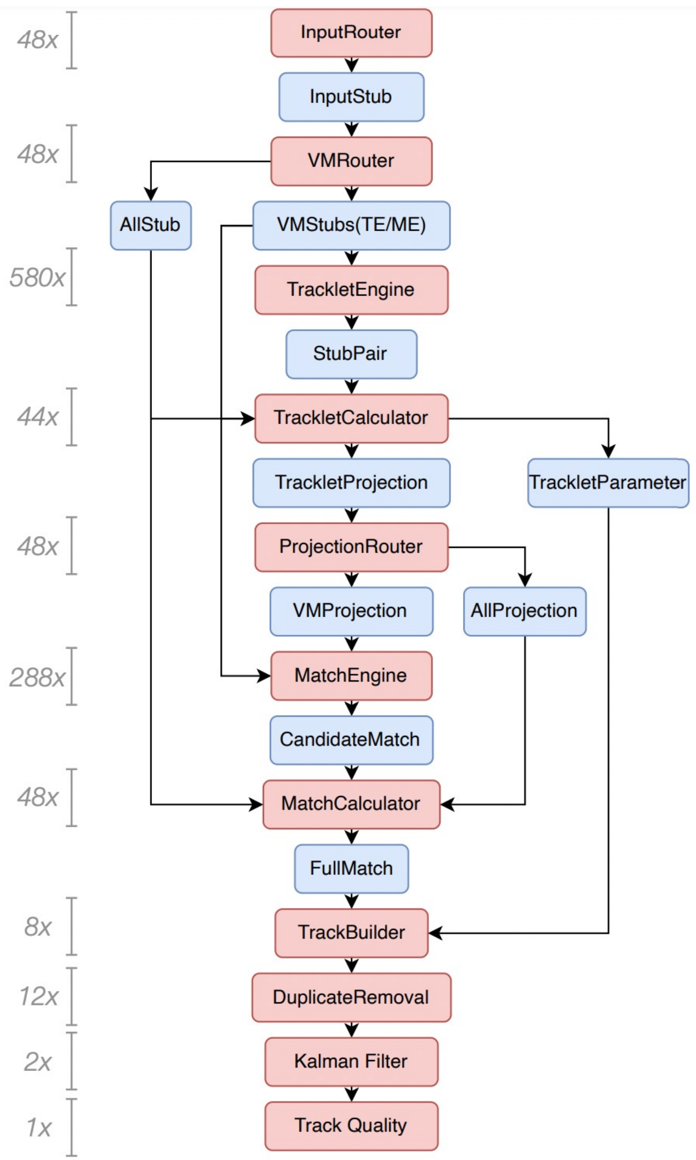

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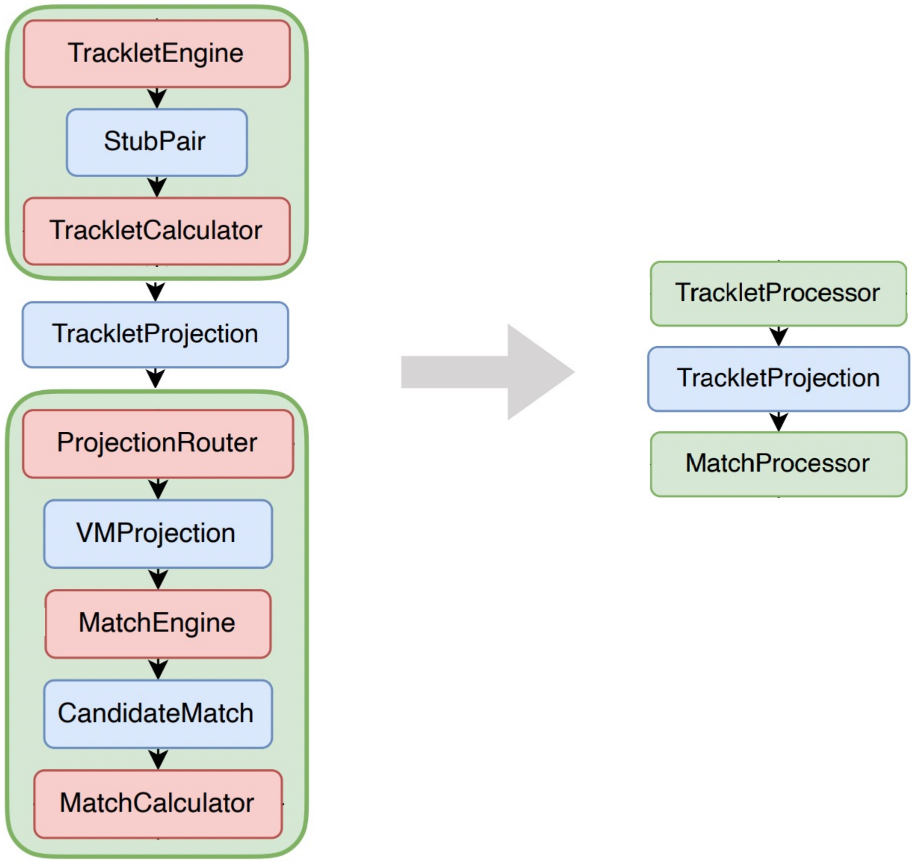
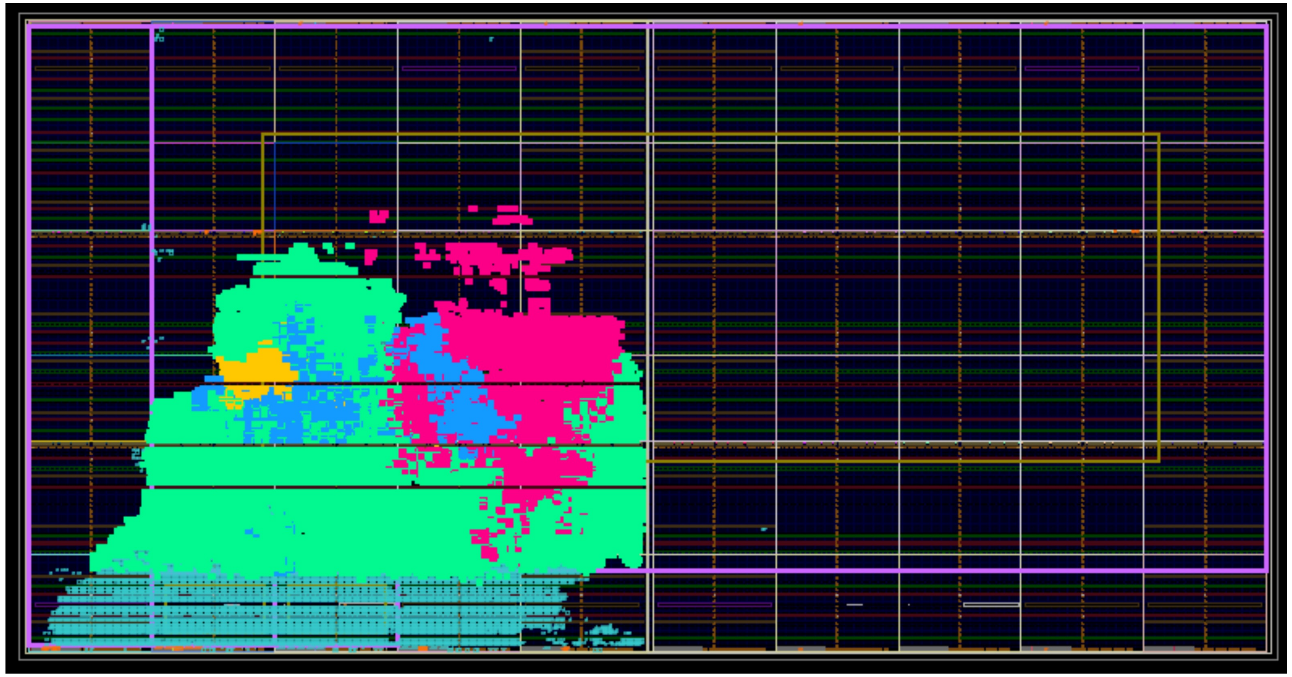
Firmware Implementation

- Use combined modules to reduce latency
- Reduce latency by 3 x 450 ns
- Reduce number of processing → memory steps
- Rewriting modules in HLS with some combined modules successfully implemented in a reduced chain



Firmware Implementation – Slice test

- Reduced configuration chain successfully implemented
- Narrow ϕ slice, single seed
- Implemented on a VU7P with KF and track quality added
- > 99% firmware-emulation agreement

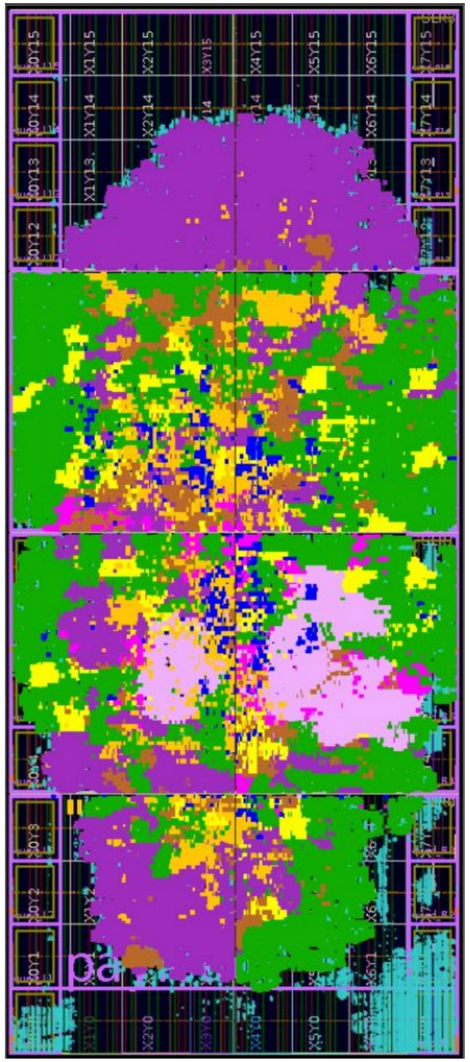


- Tracklet
- Kalman Filter
- Kalman Filter Output
- Track Quality BDT
- EMP Framework

Framework used for control, I/O, clock distribution and data buffering for the algorithm payload, used across the Phase-2 L1 Trigger

Firmware Implementation - Full Barrel

- Full barrel project
- Single VU13P
- 2/3 of entire project → just the pattern recognition stage
- Meeting timing is difficult with this complexity of project
  - advanced floorplanning
  - combined modules
  - rewriting parts in VHDL
- Lots of progress has been made to meeting timing
- Final project will be split between two VU13P FPGAs, making timing closure easier



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Hardware Testing

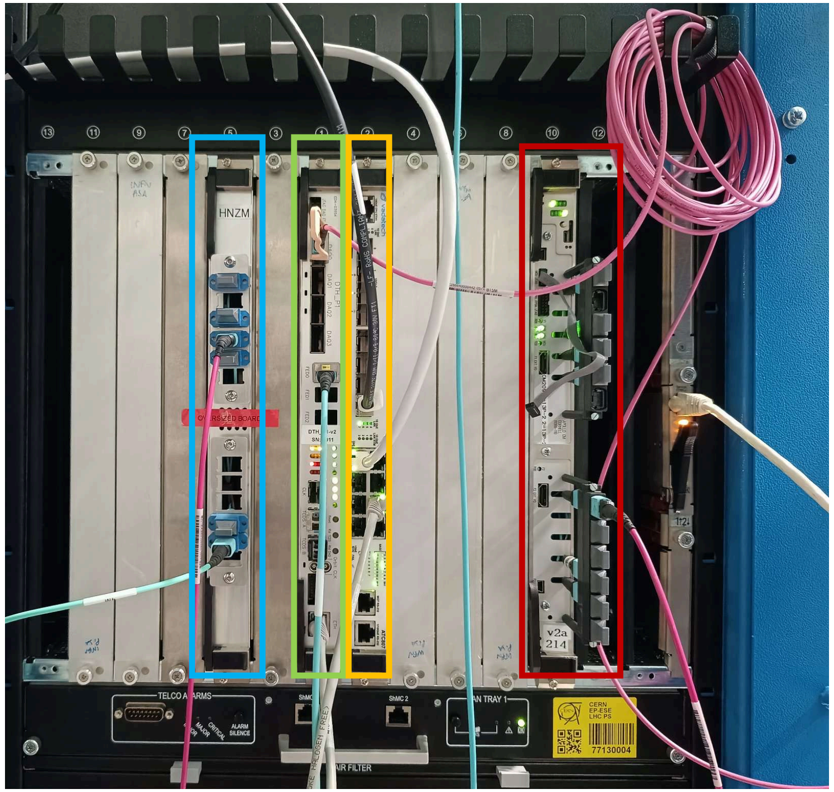
Using the Apollo board

- Rev-1 hosting a single VU7P (previous testing)
- Rev-2 hosting two VU13P FPGAs (current testing & final design in red in the picture)

Variety of optics under test, ultimately need 25 Gb/s (in pink in the picture)

- Tests involving wider trigger system
- Have successfully transferred tracks from the reduced configuration track finder processor to vertex finding system
- Tests underway using the Apollo Rev-2 board with more complete versions of the track finding firmware

Apollo Rev-2
DTH*
Ethernet Switch
Serenity



*For distributing a common clock between boards

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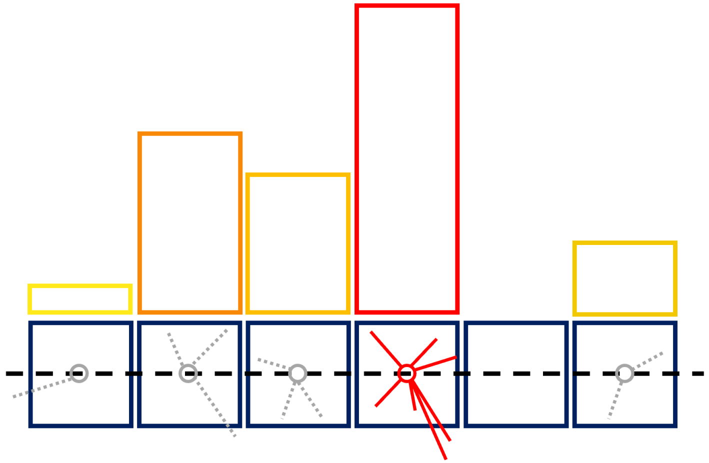
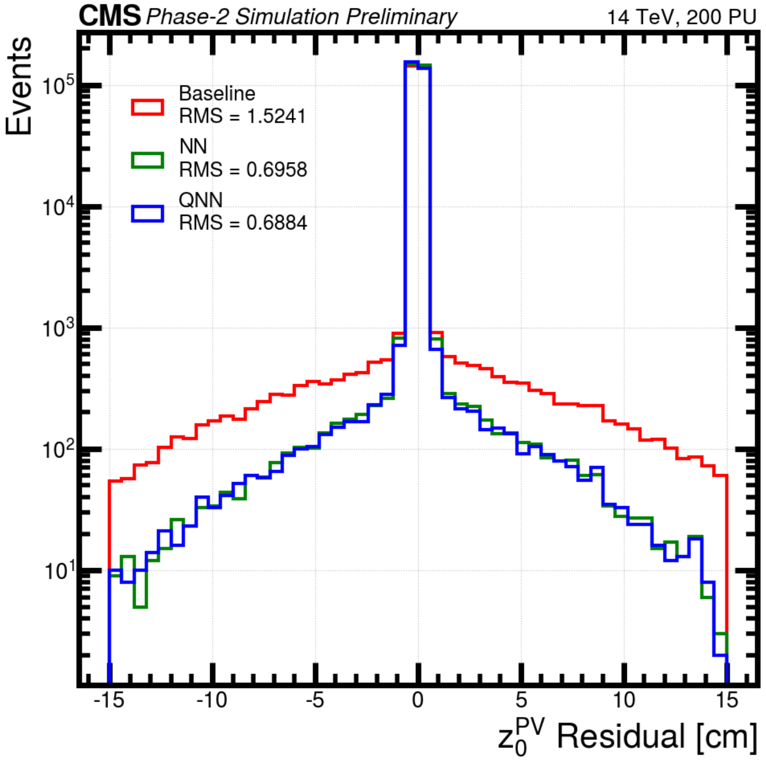
Example use of tracks in the L1 trigger



Vertex Finding

- Histogrammed approach to finding the highest p_T scatter in an event
- Developing a neural network-based approach taking advantage of track quality BDT to improve resolution



Particle Flow and Pileup per Particle Identification

- Major part of the CMS L1 trigger
- Reduce impact of far higher PU on trigger algorithms
- Main user of tracks and vertex downstream
- Higher efficiency across many key physics channels

Neural Network-Based Primary Vertex Reconstruction with FPGAs for the Upgrade of the CMS Level-1 Trigger System

Particle Flow Reconstruction for the CMS Phase-II Level-1 Trigger

Conclusion

- Track finding is essential for the CMS Level-1 trigger upgrade
  - Particle flow, vertex finding, pileup per particle identification all now possible in Level-1
- Track finding must reconstruct $\mathcal{O}$ (100) tracks, $p_T > 2$ GeV, $|\eta| < 2.4$ from 10,000 stubs all within 4 μs at 40 MHz
- Reduced configuration firmware testing successful, now expanding to (i) full barrel and (ii) full tracker projects
- Integration testing with the wider trigger system underway

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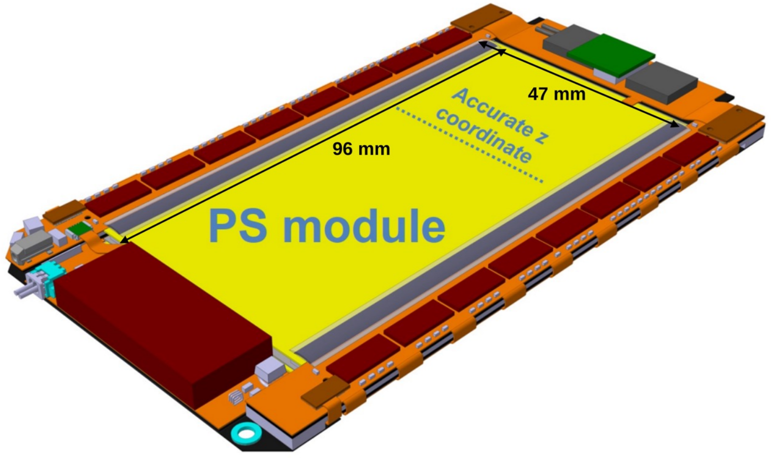
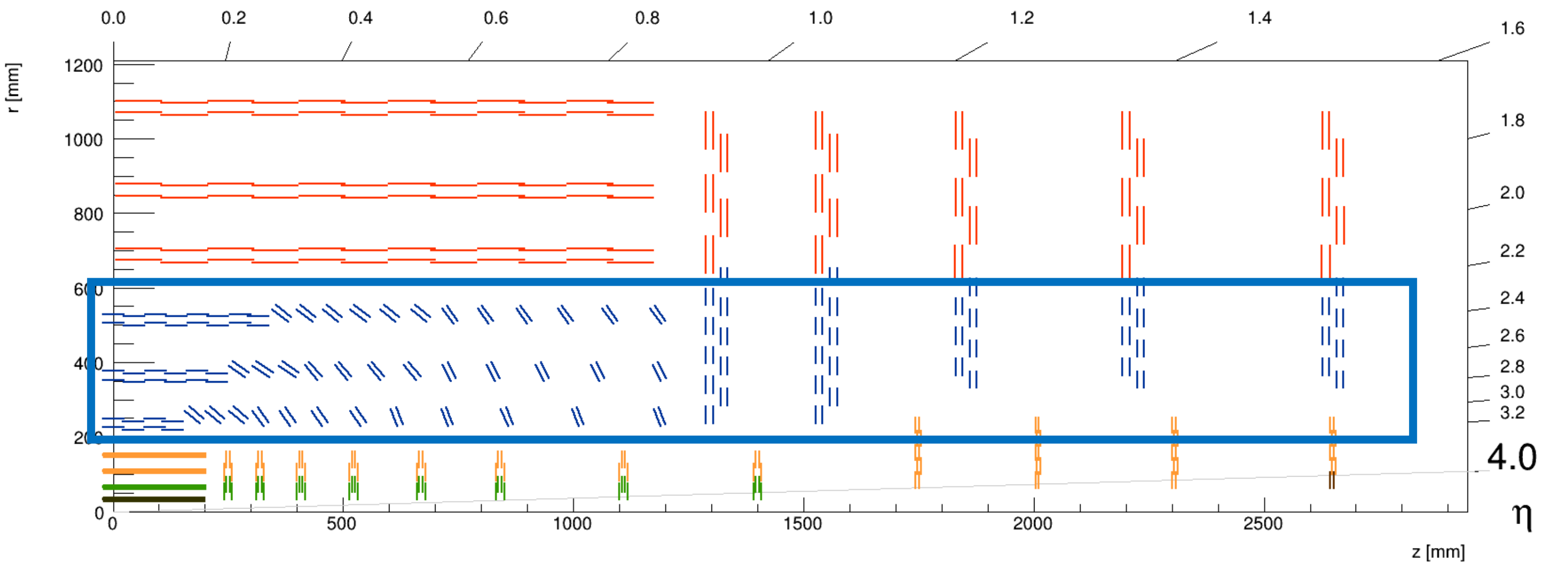
Backup

Tracker Upgrade

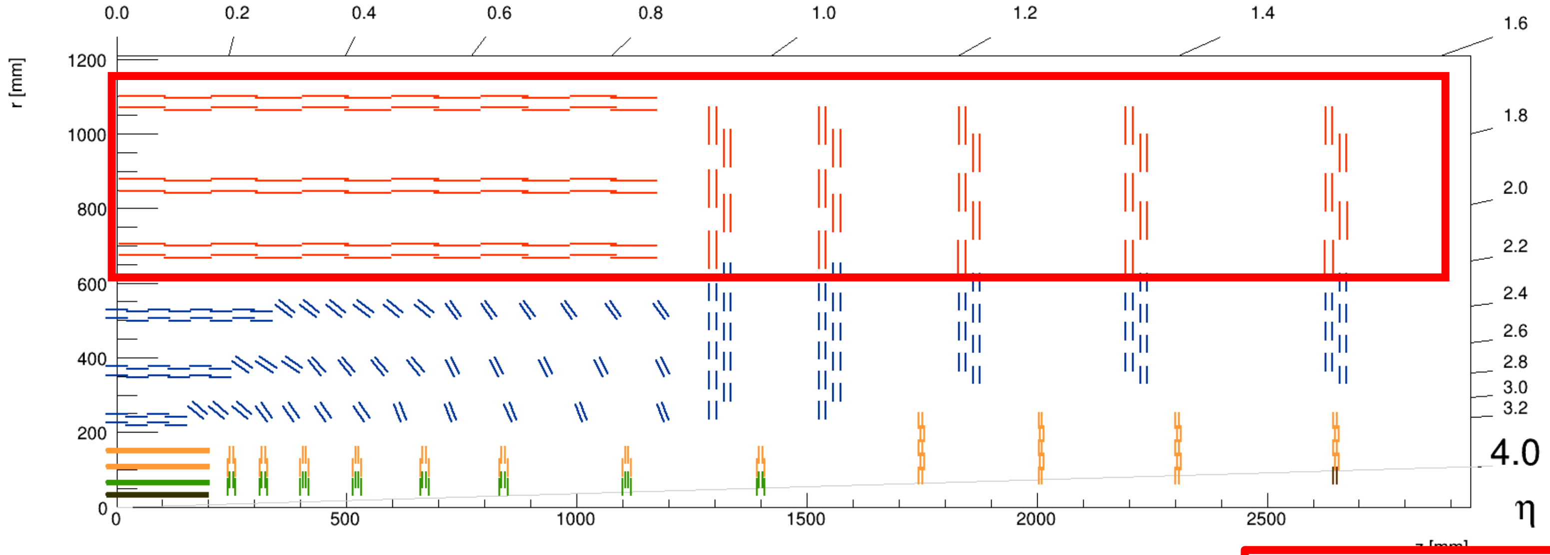


PS Modules

- One Pixel, one strip layer
- 1.47 mm long, 100 µm wide pixels give z_0 resolution for a track of 1 mm
- 100 µm pitch strip sensor
- Angled barrel region increases efficiency

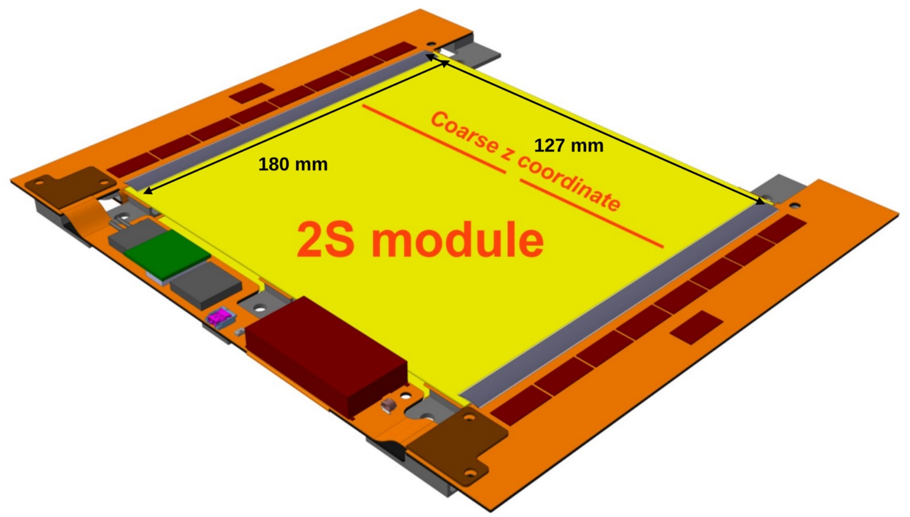


Tracker Upgrade



2S Modules

- Two strip sensor layers
- 90 µm pitch
- High resolution in ϕ, poor resolution in z (η) in the barrel (endcap)
- Lower occupancy and bandwidth motivates their use in the outer layers



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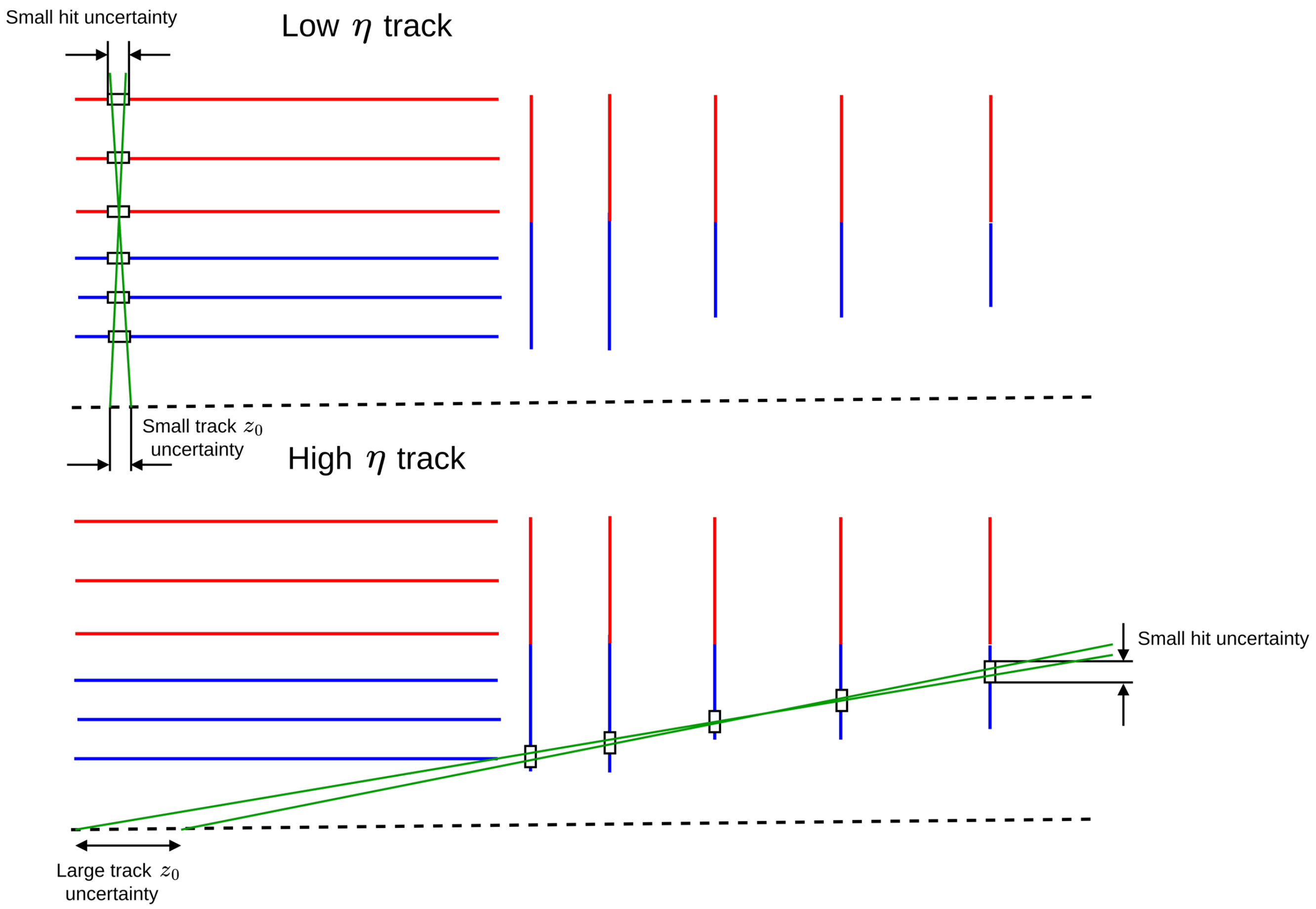
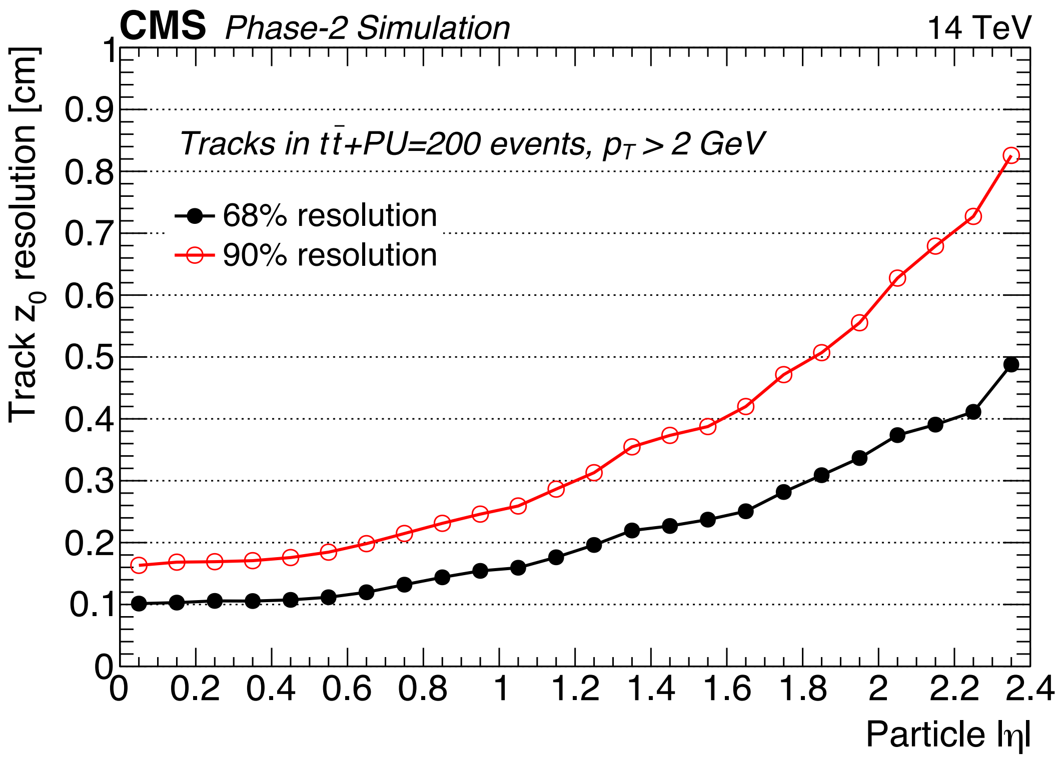
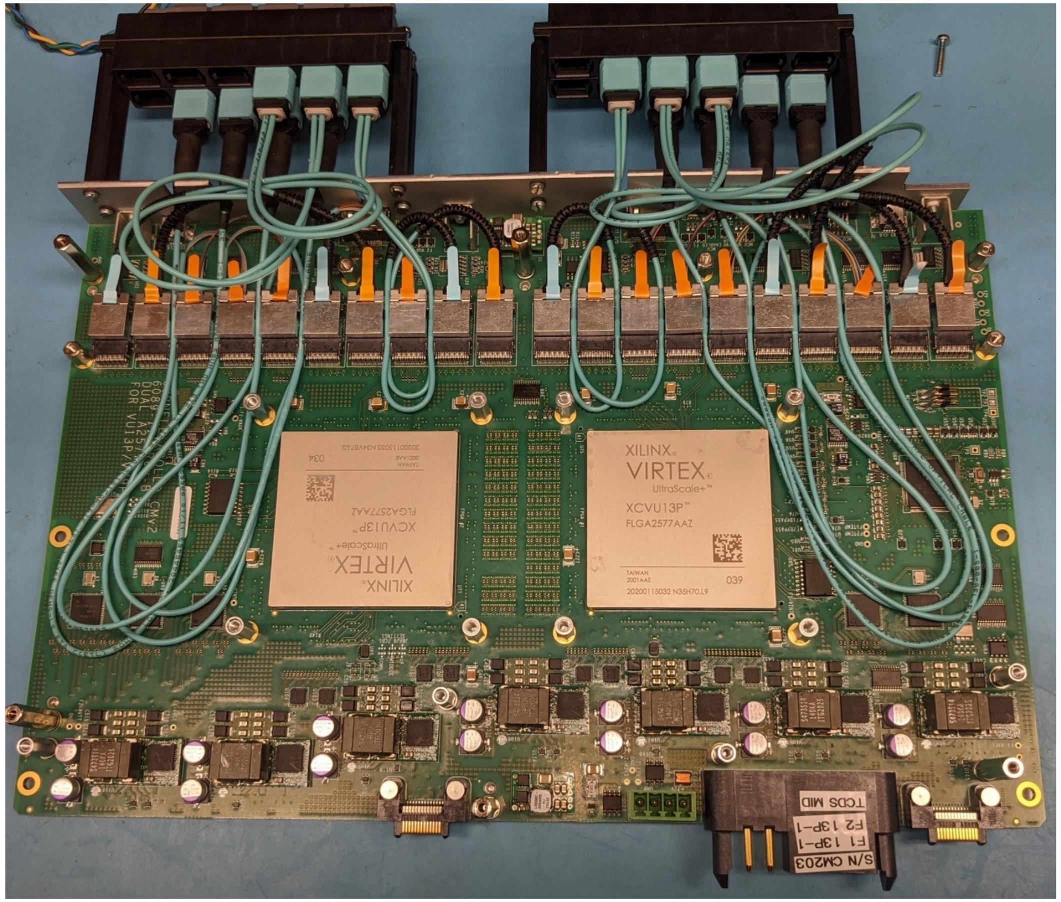
Hybrid Algorithm – z_0 resolution

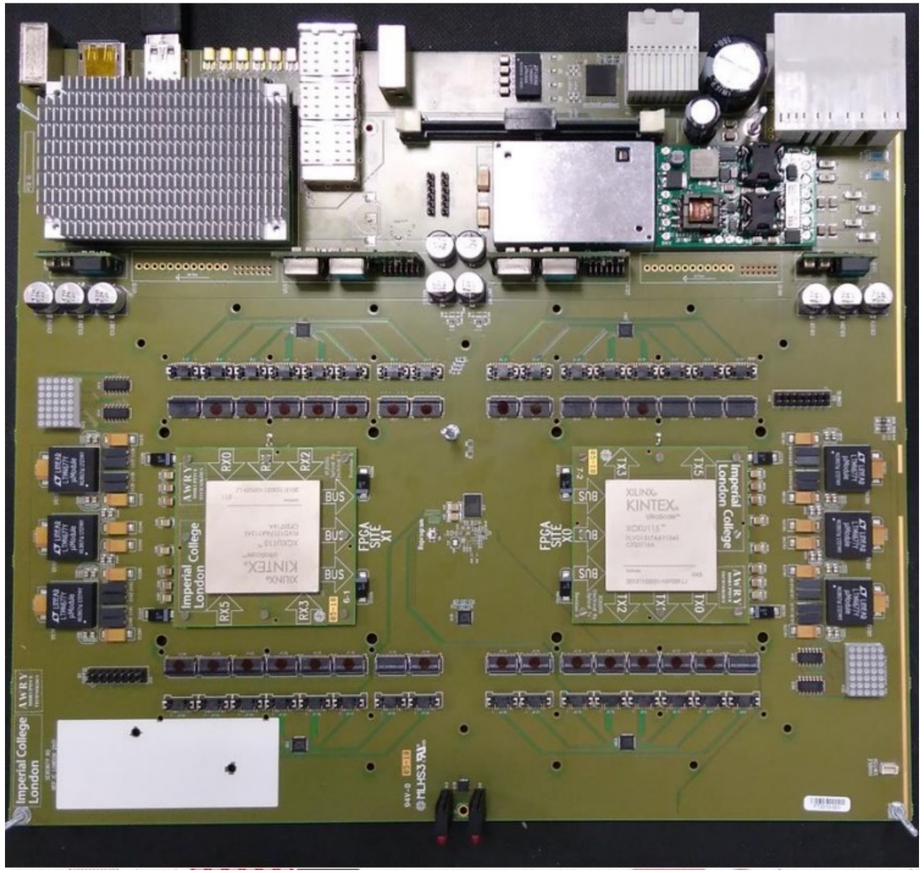




Hardware Testing - Boards



Apollo Rev-2, target board for the track finder FW, two VU13P FPGAs. Also used in inner tracker DTC and Lumi measuring



Serenity Board used for wider L1 trigger and used for integration testing with the track finder. Will be used for DTC