
# Recent results on micro-electronics developments for future trackers in Hi-Lumi upgrades

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*on behalf of the IGNITE collaboration*

# Challenges in next Hi-Lumi upgrades (and 4D tracking)

**Future colliders (LHCb Upgrade II, HIKE (NA62 upgrade), CMS-PPS, ATLAS AFP, FCC-hh) will have to cope with extremely high instantaneous luminosity:**

- REQUIREMENTS FOR SENSORS:
  - Radiation hardness against fluences from $10^{16}$ to $10^{17}$ $1MeV\,\frac{n_{eq}}{cm^2}$
  - Spatial resolution $\sigma_s \approx 10\,\mu m$
  - Time resolution $\sigma_t \leq 50\,ps$ per hit
  - Detection efficiency $\epsilon > 99\%$ per layer

- REQUIREMENTS FOR READ-OUT ELECTRONICS:
  - Pixel pitch $\approx 50\,\mu m$
  - Time resolution $\sigma_t \leq 50\,ps$ on the full chain $\rightarrow$ $\sigma_t^2 \sim \sigma_{sensor}^2 + \sigma_{AFE}^2 + \sigma_{TDC}^2$
  - Radiation hardness $TID > 1\,Grad$
  - Power budget per pixel $P \approx 25\,\mu W$ (referred to $55\,\mu m$ pitch, $1.5\,W/cm^2$)
  - DATA BANDWIDTH $\approx 100\,Gbps/ASIC$

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→ **CMOS 28-nm ELECTRONICS**

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→ **CMOS 28-nm ELECTRONICS**

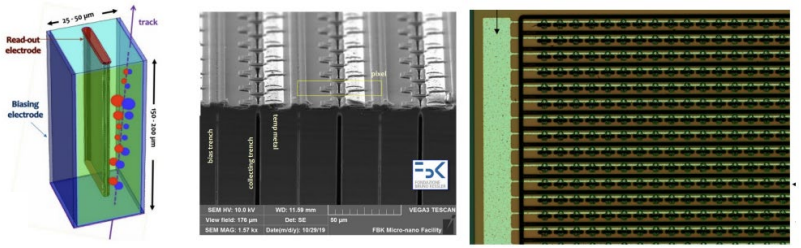
→ **SILICON PHOTONICS**

# R&D on 4D tracking

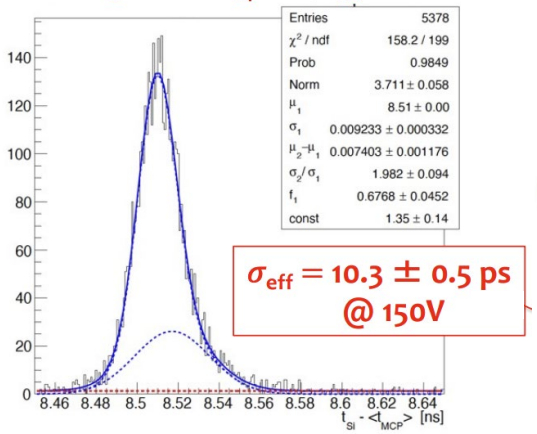
TimeSPOT
TIME and SPace real-time Operating Tracker

P. I. Adriano Lai

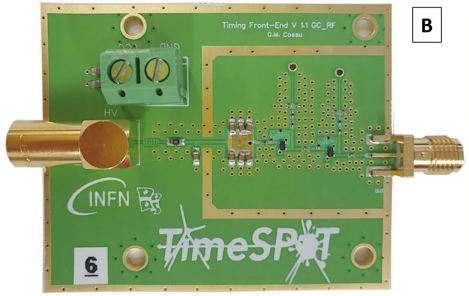
1. DESIGN AND FABRICATION OF 3D DETECTOR
(Silicon and Diamond)

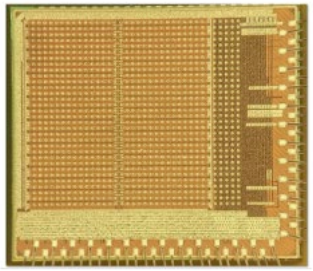



Irradiated @ 2.5 $10^{16}$ $n_{eq}/cm^2$ , $\alpha_{tilt} = 0°$




$\sigma_{eff} = 10.3 \pm 0.5$ ps @ 150V

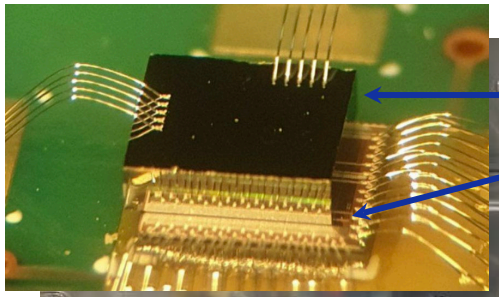


Timespot1 ASIC

10ps time resolution with 3D trench sensors and custom discrete electronics measured at test beam facility also on irradiated sensor up to fluence 2.5 $10^{16}$ 1 $MeV\ n_{eq}/cm^2$ see A. Lai presentation Vertex 2022
And Gian-Franco Dalla Betta's Talk Timing performance of 3D silicon sensor

See POSTER: ***Intrinsic timing properties of simulated ideal 3D-trench silicon sensor with fast front-end electronics*** *GM Cossu, D Brundu, A Lai*



Sensor matrix integrated electronics

Beam axis (180 GeV/c $\pi^+$)

Timespot 3D Silicon Hybrids

Timespot 3D Diamond Hybrids

Test beam with final demonstrator with 5 station with the TIMESPOT1 ASIC (May 2023)

# R&D on Silicon Photonics and High-speed Interconnect

Falaphel

P. I. Fabrizio Palla

## FAST LINK AND RAD-HARD FRONT-END WITH INTEGRATED PHOTONICS AND ELECTRONICS FOR PHYSICS

Compact Silicon Photonic Mach-Zehnder Modulators for High-Energy Physics

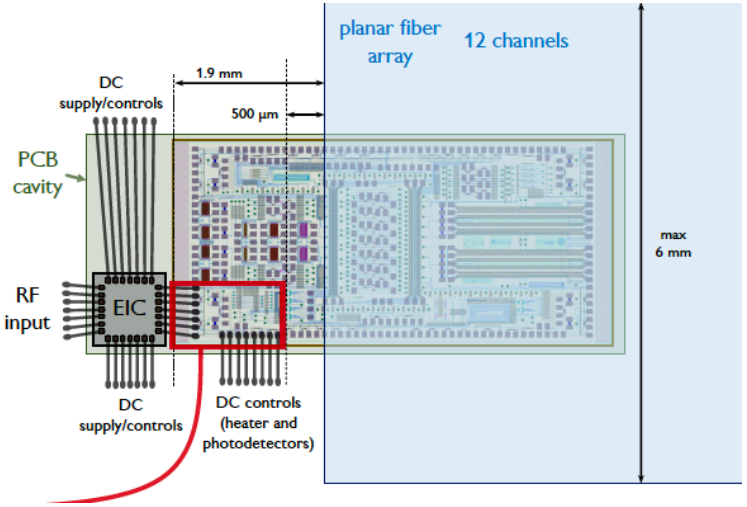
See Simone Cammarata's talk given at TWEEP 2023

25 Gb/s NRZ transmission validated using standard Folded Mach Zehnder Modulator (FMZM)and RAD HARD FMZM up to 1.25 Grad!

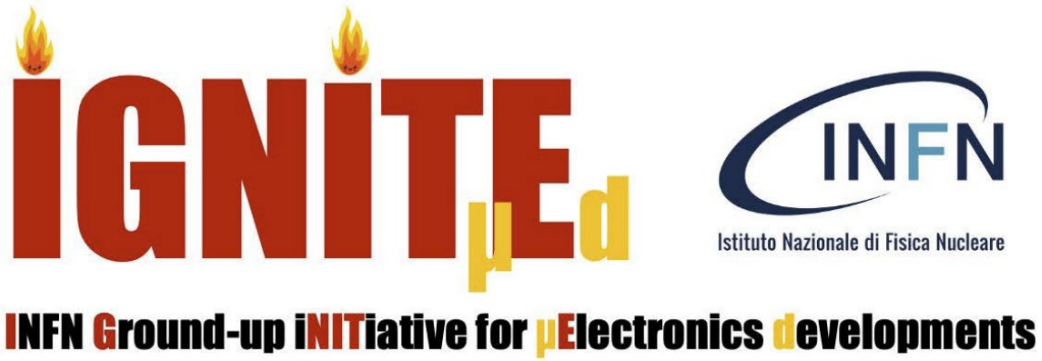
**Also developing:**

28-nm CMOS Serializer (target data rate 25 Gbps)

28-nm CMOS Driver/Receiver (target data rate 25 Gbps)



# The INFN - IGNITE initiative




National initiative fundend by **INFN**

- 14 INFN institutes
- 70 people involved (physicist and engineers)
- P.I. Adriano Lai (INFN Cagliari)

GOAL: DEVELOP A TRACKING SYSTEM SUITABLE FOR HIGH LUMINOSITY CONDITIONS

1) Integrated system composed by a hybrid 28nm CMOS ASIC and pixel Sensor MATRIX

2) Readout ASIC for HIGH-BANDWIDTH optical data transmission

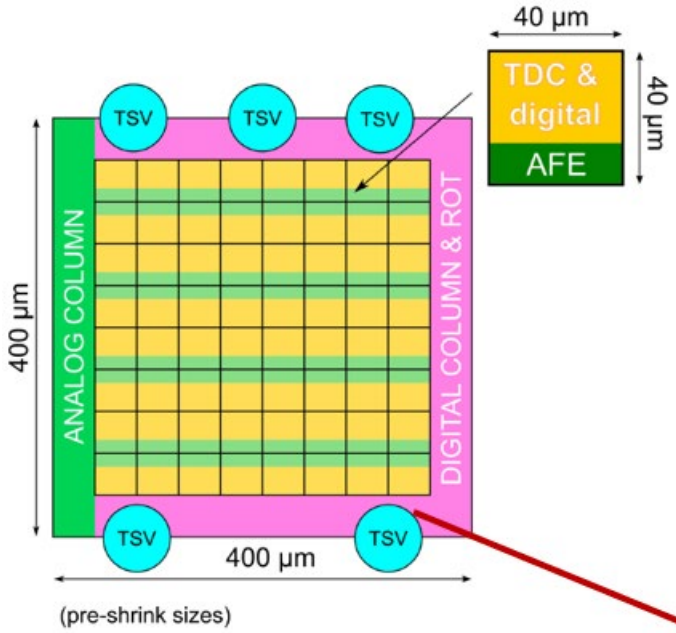
3) Take advantage of the experience obtained from the previous R&D projects (Timespot, Falaphel etc..)

considering all the challenges in realizing such a device

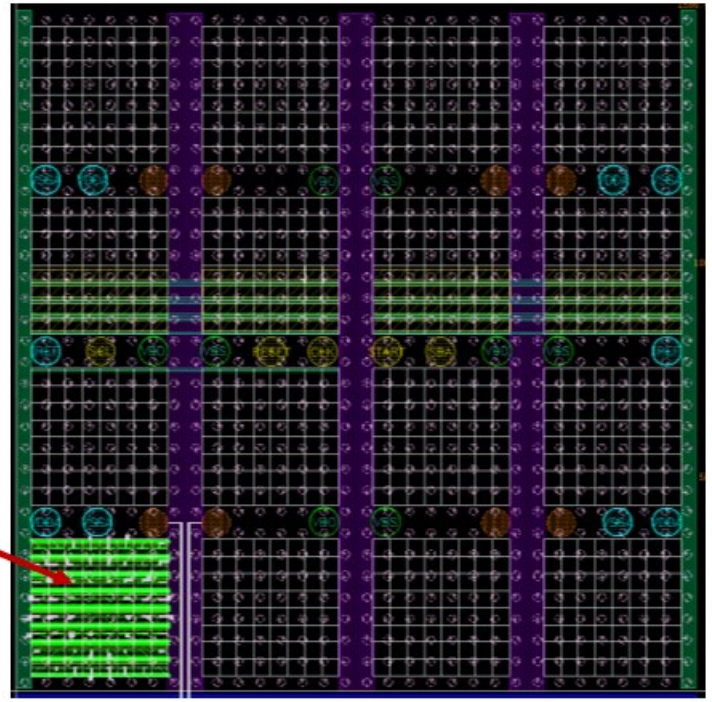
- Obtain uniform timing performance over a large area
- Minimize power consumption
- Distribute data to the read out
- Etc.

4) Explore innovative 3D technologies and vertical connections (TSVs, Face2Face or Face2Back bonding)

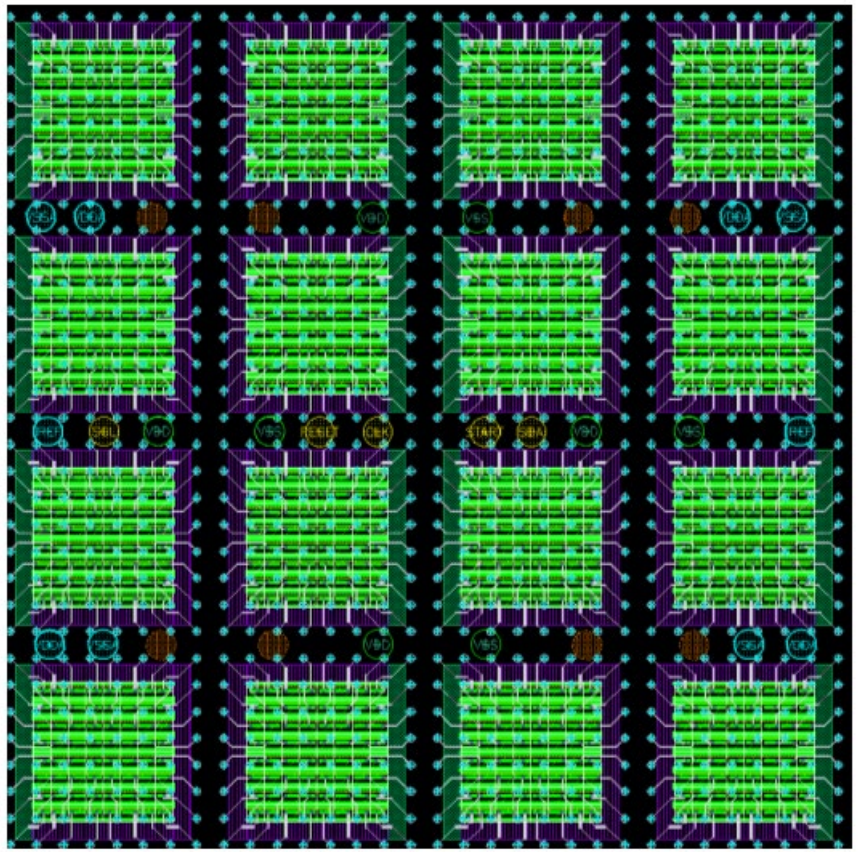
# The IGNITE ASIC concept




ELEMENTARY
REPETITION UNIT
**8X8 PIXEL**



**Example of 32x32 ASIC for 45 um pitch Sensor**



**Example of 32x32 ASIC for 55 um pitch Sensor**

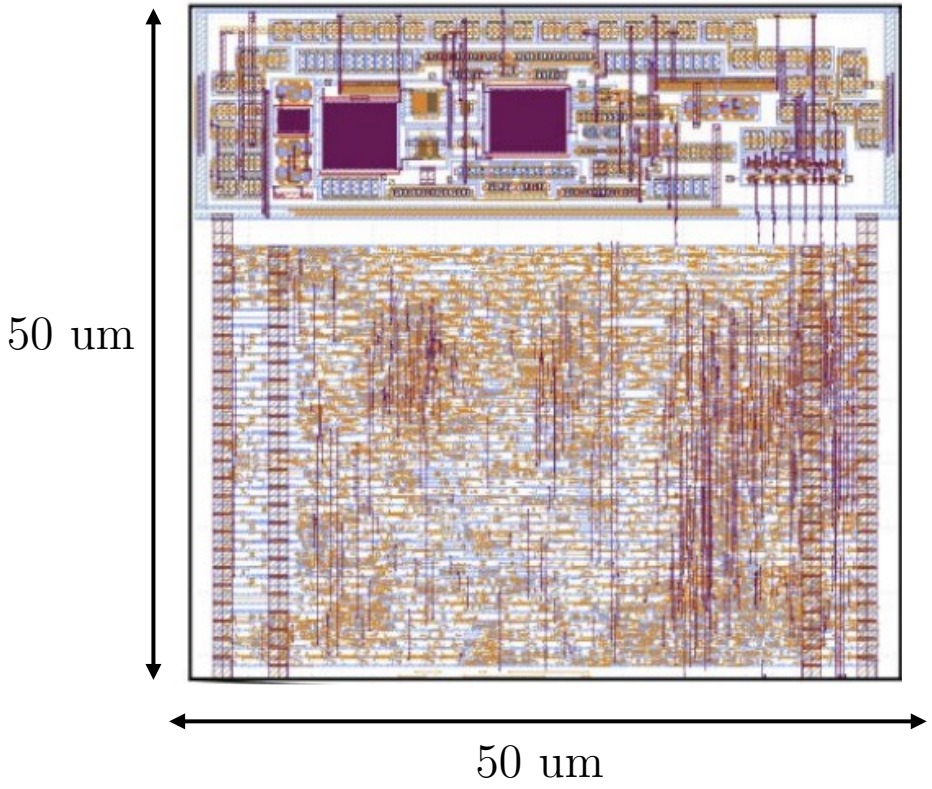
- Each pixel has 36um pitch and AFE + TDC
- Make space for the TSV
- Plls for clock distribution in the digital space between tiles

Same repetition unit with different redistribution layer

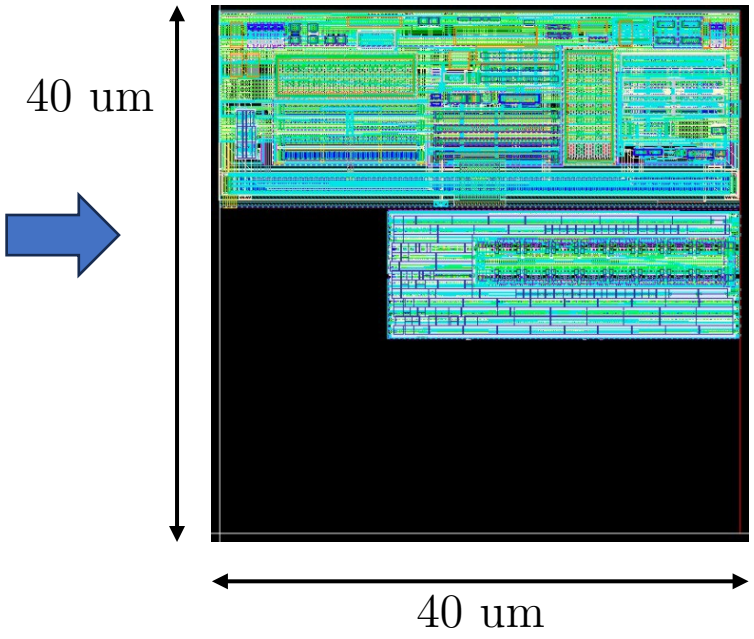
Higher pitch (110um, 165um etc.) can be obtained by channel masking

# RESULTS: IGNITE ASIC PIXEL

**TIMESPOT1 PIXEL**



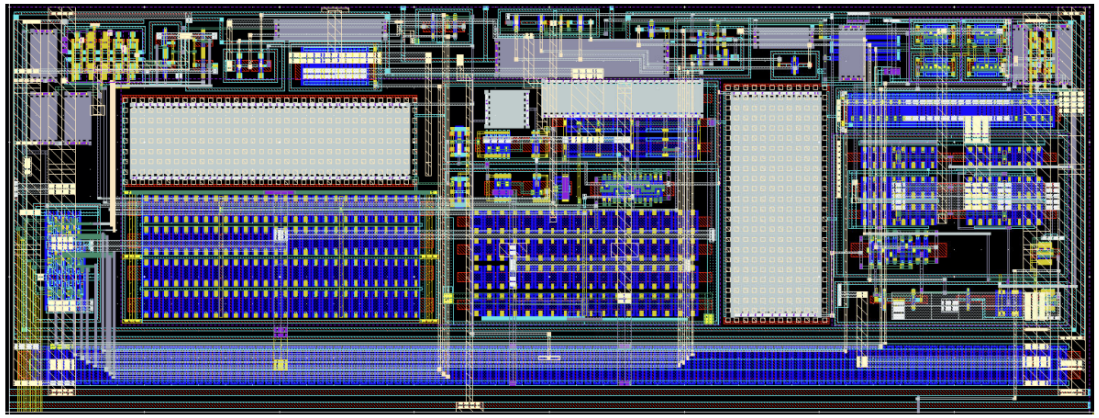

**IGNITE PIXEL**




- The pixel Fundament cells (AFE and TDC) have been completely redesigned using the new 28nm technology (HPC → HPC+)
- The experience gained with the TIMESPOT1 ASIC was fundamental to speedup the process
- Several improvements in area, power consumption and performance

* PRE-SHRINK SIZES

# RESULTS: PIXEL AFE



## TIMESPOT1 AFE

- CSA inverted based with double Krummenacher feedback + dual Stage Discriminator
- Discrete time DC Offset compensation (global threshold and baseline)
- Issue with the Offset compensation but average performance around 60ps for 2fC charge injection with 100fF Sensor Capacitance

## IGNITE Analog Front-Ends

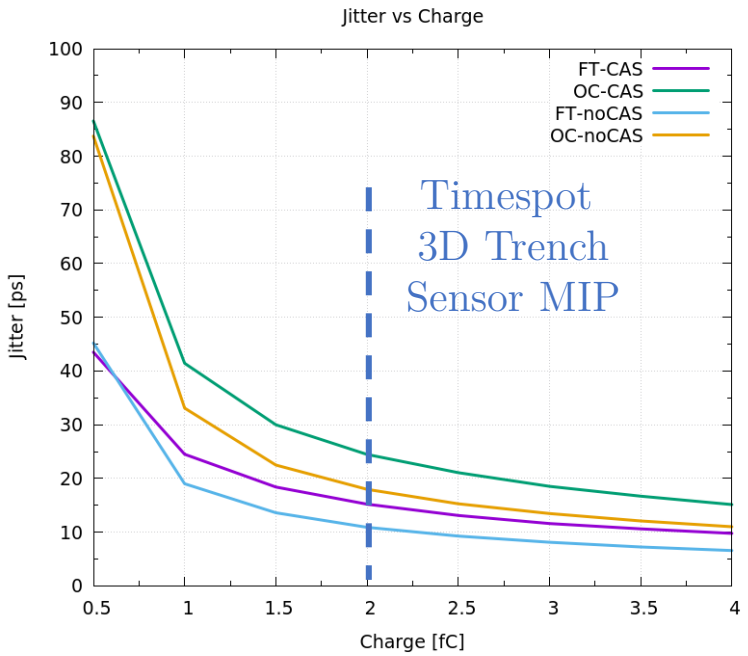
- Several topologies investigated ( CSA, Common Gate TIA, Cascode TIA..etc)
- 4 different flavors simulated and with finalized design (Layout + Post Layout Simulations)

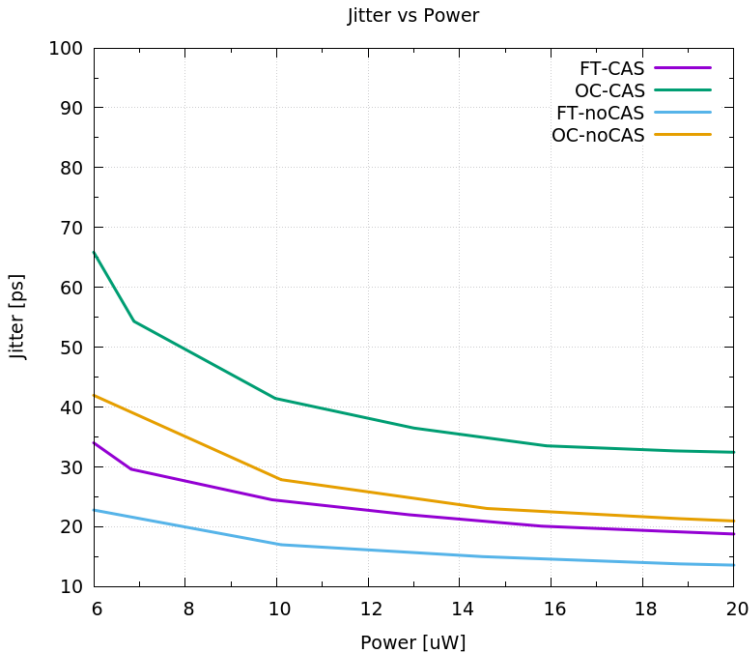
1. Cascoded Inverter with Fine DAC threshold tuning (**FT-CAS** )
2. Cascoded Inverter with enhanced Offset Compensation (**OC-CAS**)
3. No-Cascode Inverter with Fine DAC threshold tuning (**FT-noCAS** )
4. No-Cascode Inverter with enhanced Offset Compensation (**OC-noCAS**)

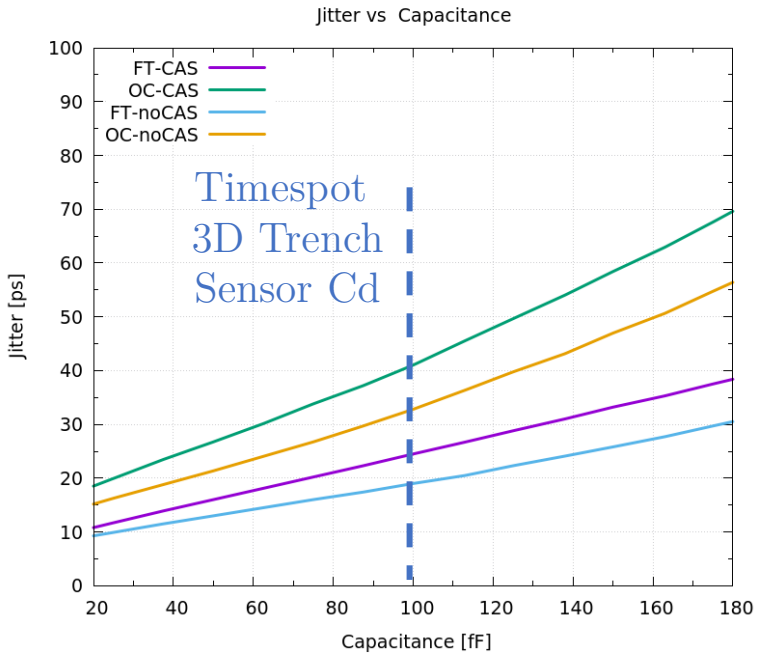
Specifics:

- LAYOUT AREA = 40um x 15um
- Local Charge injection circuit
- Programmable Power : 4uW → 21 uW
- Programmable TOT: e.g., 10ns → 160ns

# RESULTS: PIXEL AFE (post layout simulations)




Jitter Vs Charge
evaluated with:

Cd =100fF
Power = 10.8 uW
Discharge Current = 100nA
Vth ~ 30mV

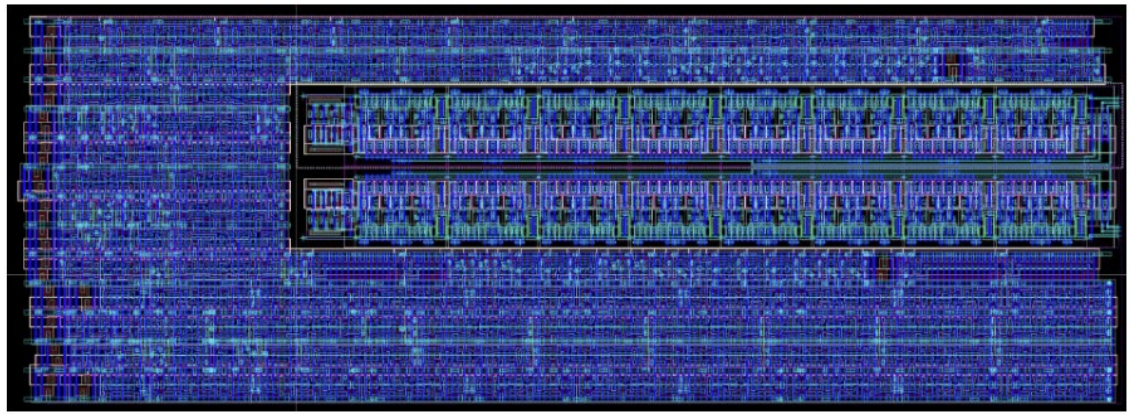
Jitter Vs Power
evaluated with:

Cd =100fF
Discharge Current = 100nA
Vth ~ 30mV
Qin = 1fC

Jitter Vs Capacitance
evaluated with:

Qin= 1fC
Power= 10.8uW
Discharge Current = 100nA
Vth ~ 30mV

# RESULTS: PIXEL TDC



## TIMESPOT1 TDC

- VERNIER ARCHITECTURE
- 2 DCO with frequency ~ 1GHz
- DCO switched off after measure
- Time resolution the depends on the difference in period of the 2 DCO
- TA (~ 20ps), TOT (~ 1ns)
- TIMESPOT1 RTL DESIGN

Timespot TDC Power Cons.

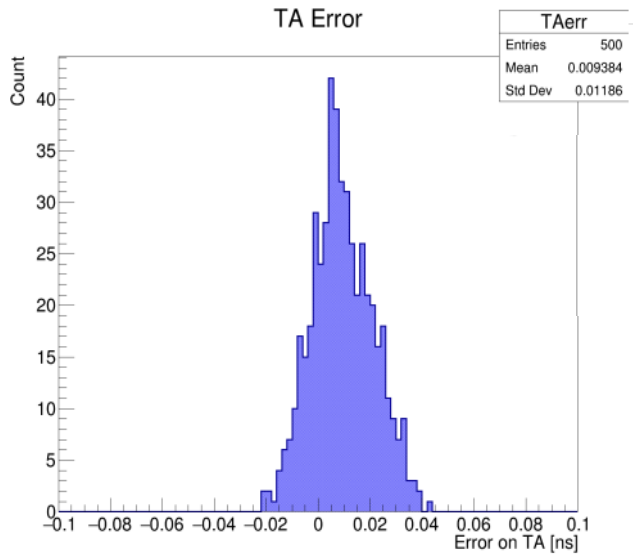
| TDC power | µW |
|---|---|
| IDLE | 20.7 |
| Calibration | 552 |
| DAQ 3 MHz | 175 |
| DAQ 1 MHz | 69.3 |
| DAQ 500 kHz | 45.5 |
| DAQ 100 kHz | 25.7 |

## IGNITE TDC

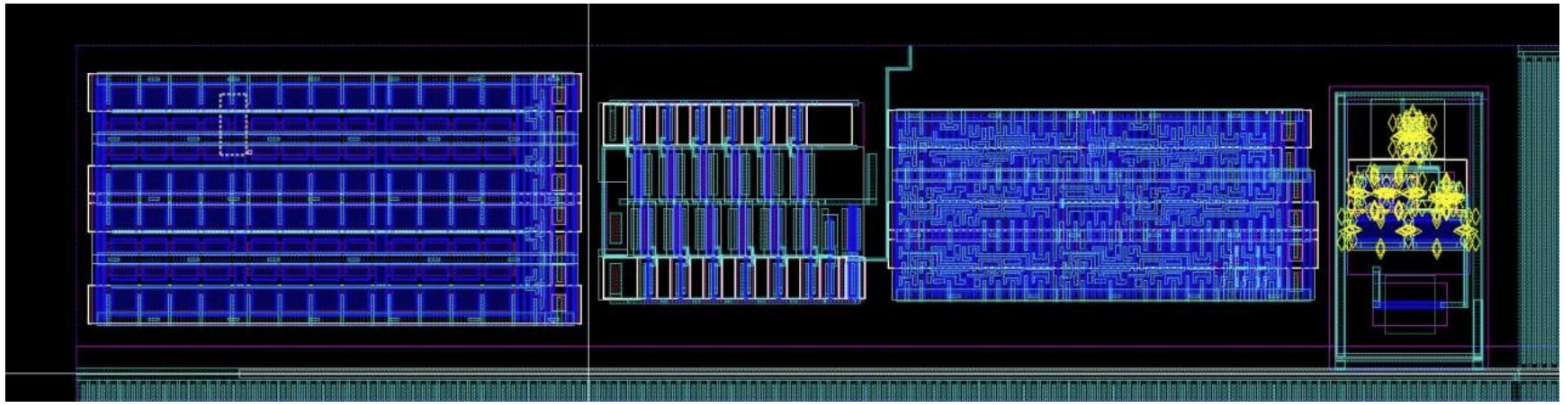
- SAME VERNIER ARCHITECTURE DESIGNED COMPLETELY FULL CUSTOM (Area 27um x 10um)
- DCO WITH 16 DELAY UNITS
  - Period range: 780ps → 900ps
  - Period tuning: Coarse (~50ps), Fine (3ps)
  - DCO jitter ~ 1ps
- MEASURE OF TA with resolution ~ **12ps rms (POST LAYOUT SIMULATION)**

IGNITE TDC Power Cons.

| TDC status | Current |
|---|---|
| OFF | 0.5 µA |
| IDLE | 1.3 µA |
| Calib. DCO {Istant. @1.12 GHz} | 98 µA |
| RUN (4.5 MHz) | 28.3 µA |
| RUN (1.0 MHz) | 7.5 µA |
| RUN (500 kHz) | 3.9 µA |
| RUN (333 kHz) | 3.0 µA |
| RUN (200 kHz) | 2.3 µA |



# RESULTS: IGNITE PLL



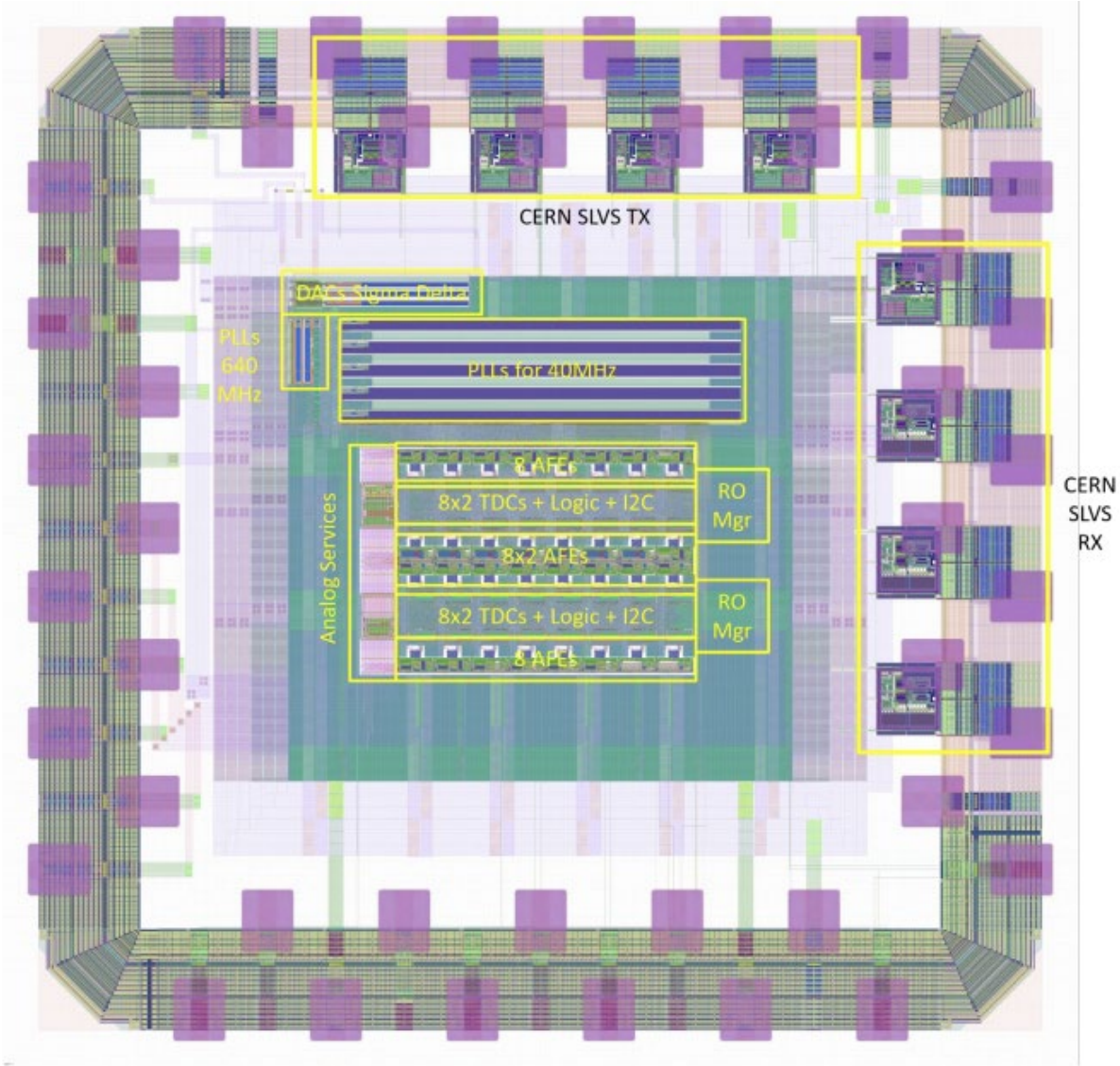
- PLL (Phased Locked Loop) designed in order to provide an internal reference clock with a static phase with respect to an external clock

- Based on a starved DCO with 3 different starving schemes (static, DAC and external)

- Core Area: 30um x 6um
- Area with Filter : 433um x 15.6 um
- Lock frequency : 40 MHz

- POST SIMULATION: power consumption 50uW, jitter filtering from 14ps (input) to 1.9ps (output)

# RESULTS: IGNITE0 TEST CHIP



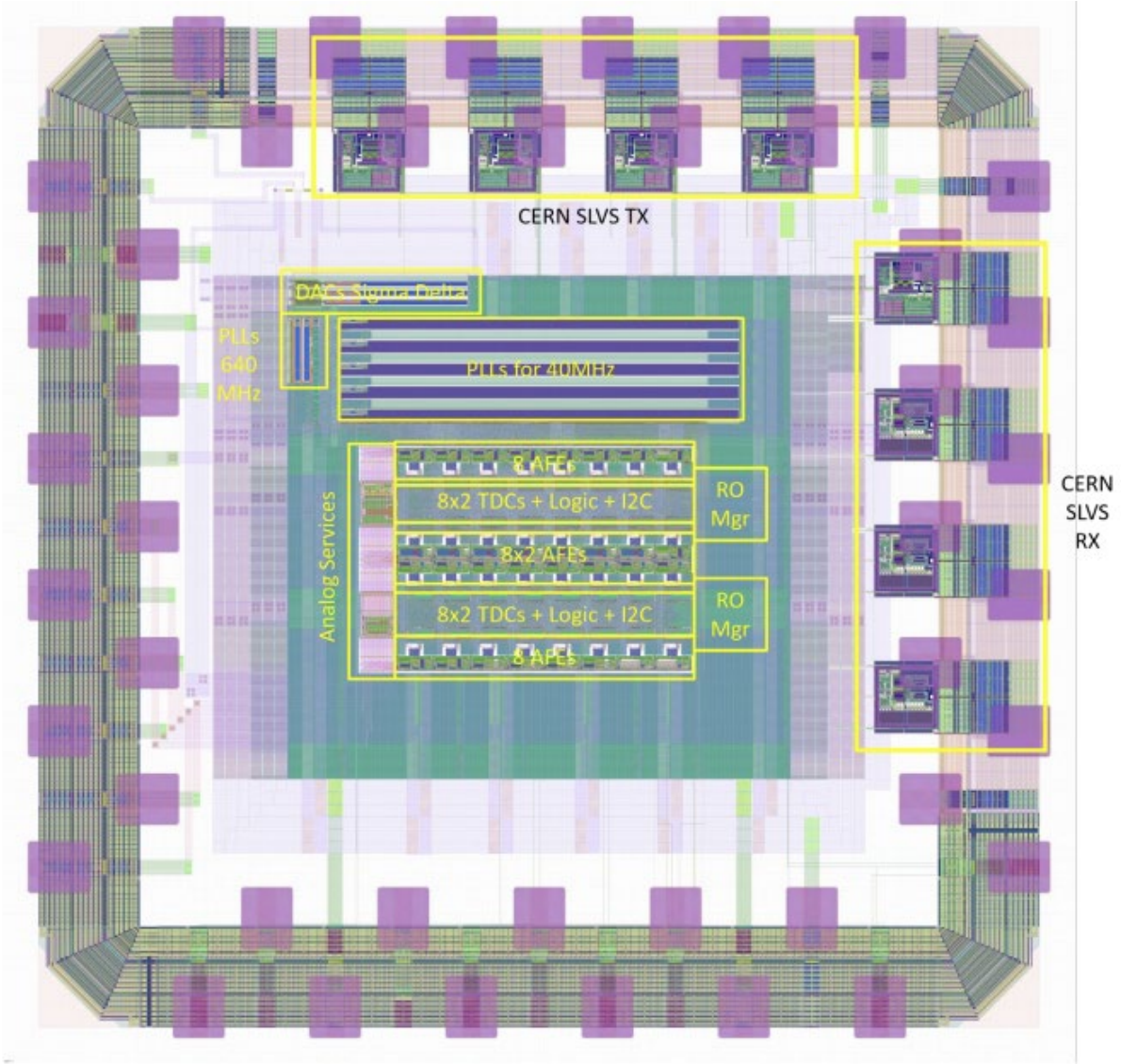

**IGNITE0 mini@SIC**

- Submitted in July ‘23
- Expected in November ‘23

Contains:

- Half Tile 8x4 ( Half repetition unit)
- 32 AFE channels (All different flavours)
- 32 TDCs
- PLLs for clock generation/filtering (40MHz and 640MHz)
- DACs
- Readout Managers
- I2C interfaces for controls and configuration

# RESULTS: IGNITE0 TEST CHIP



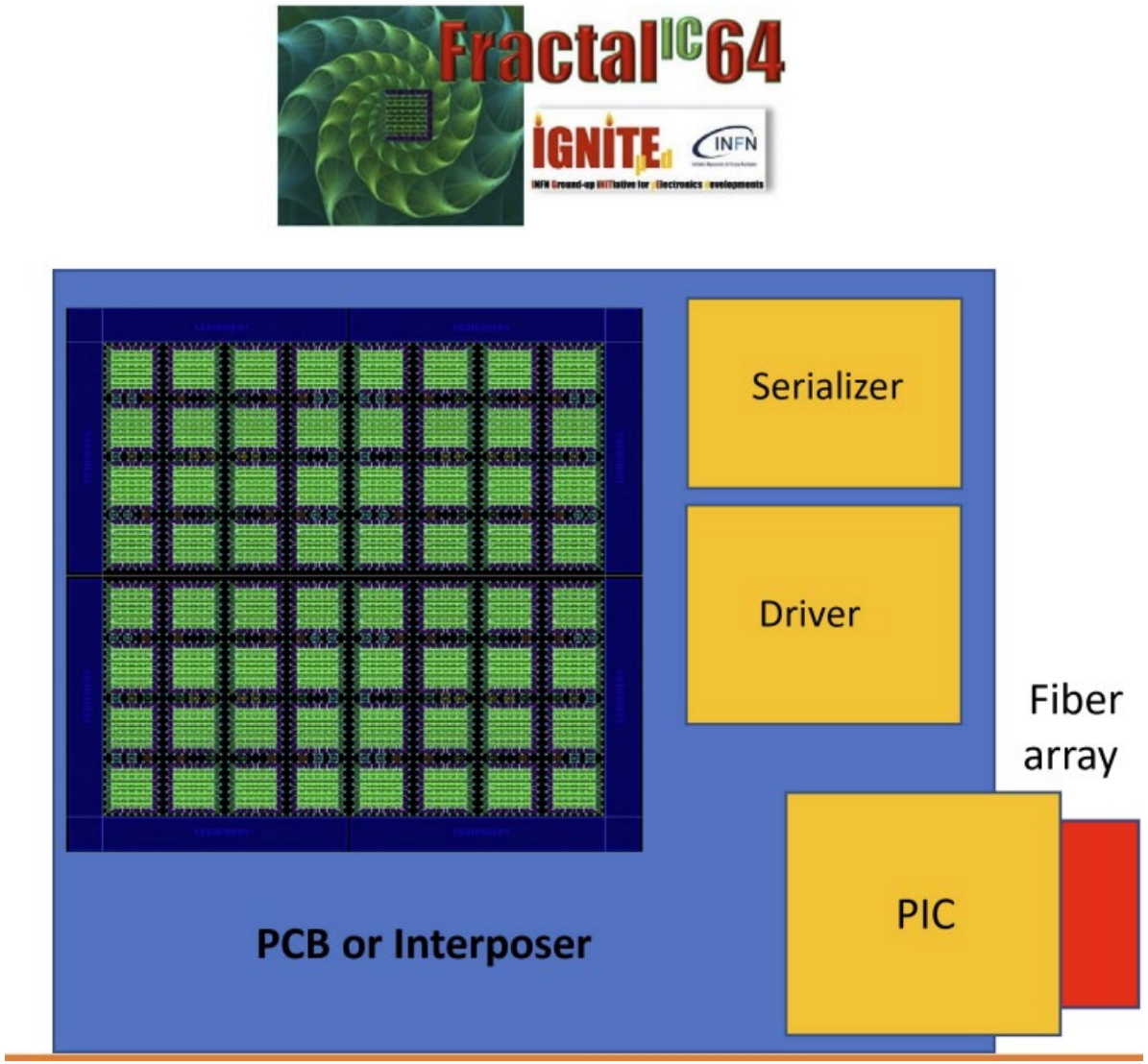

**IGNITE0 mini@SIC**

Some of the test we will be able to do:

- Each pixel AFE can be pulsed individually using the Charge injection cell (measure jitter vs Charge), (measure jitter vs power)
- Each AFE is connected to a "Sensor Cell" that allow to change the capacitance load (from 12.5fF to 187fF) at the input of the amplifier (measure jitter vs capacitance)
- TDCs can be pulsed through the AFE but also from outside using a FAST-IN LVDS input (TDC performance scanning the phase with high accuracy)
- Evaluate PLLs performance using loopback connection

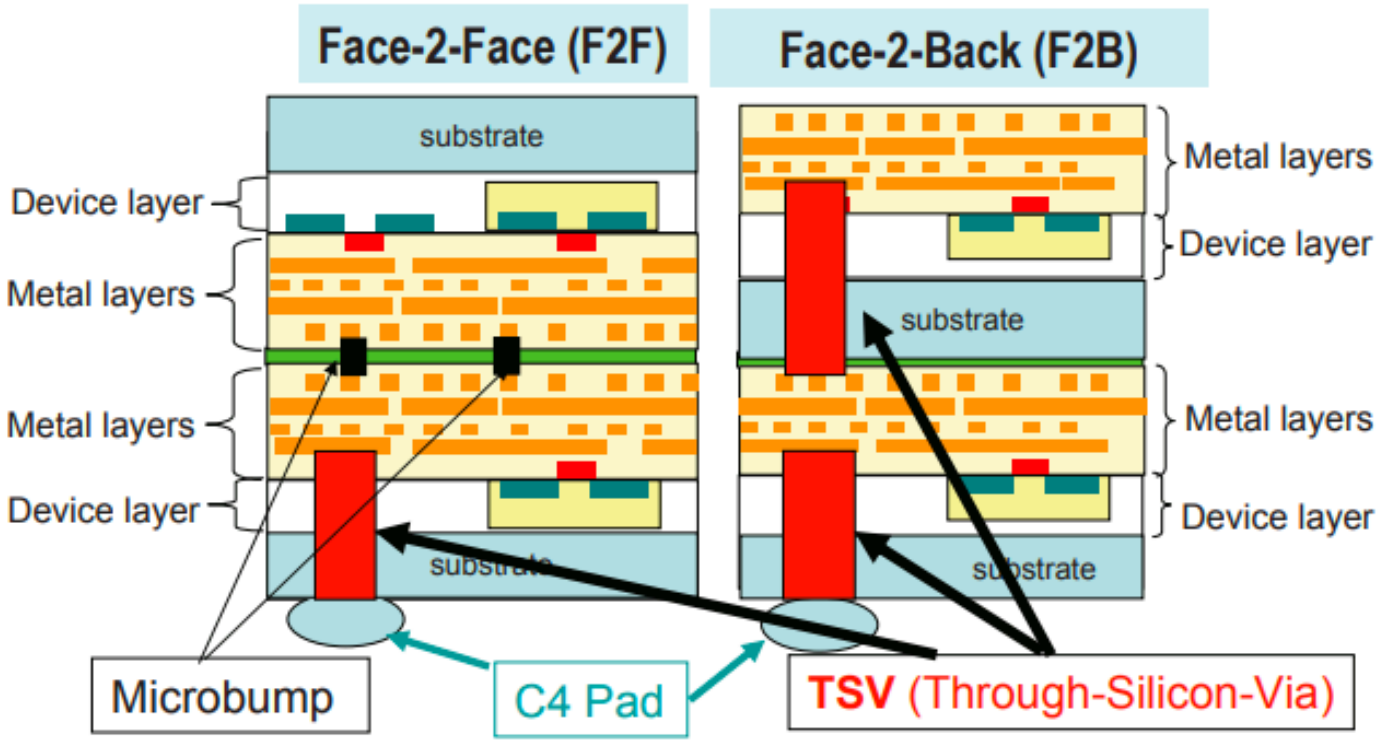
# IGNITE Conclusions and Perspectives:

- The IGNITE initiative is currently working for develop a tracking system for High luminosity environments
- We have submitted a first prototype (IGNITE0) that contains half of the repetition unit that we want to use as a building block for a larger chip
- We are currently working on the test PCB that will allow us to test IGNITE0
- **Next step development of ASIC "Fractal_IC_64"**
  - 64x64 pixels matrix
  - Periphery for test with conventional wire bonding integration



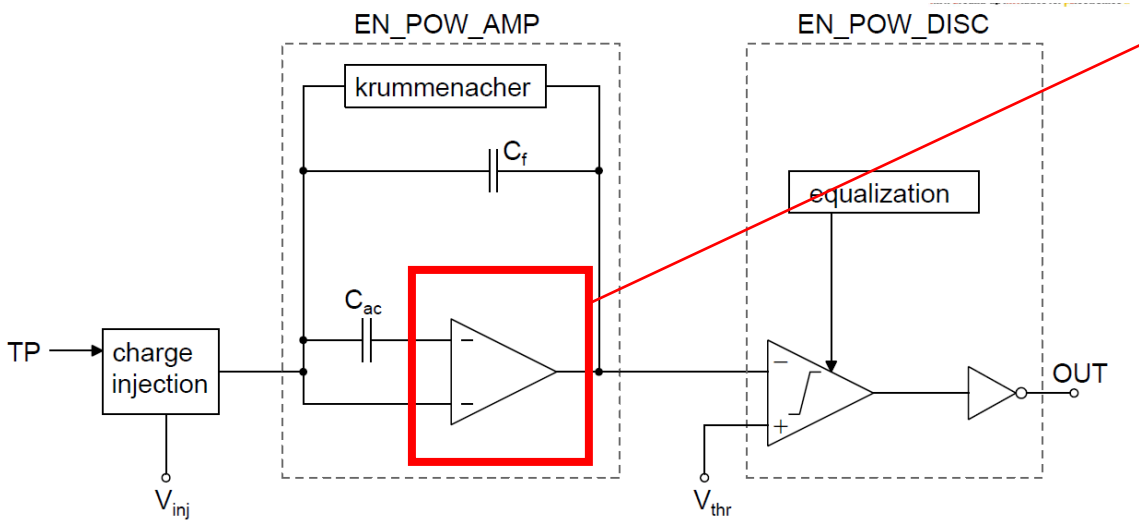
# THANK YOU

# IGNITE: 3D/Vertical integration techniques



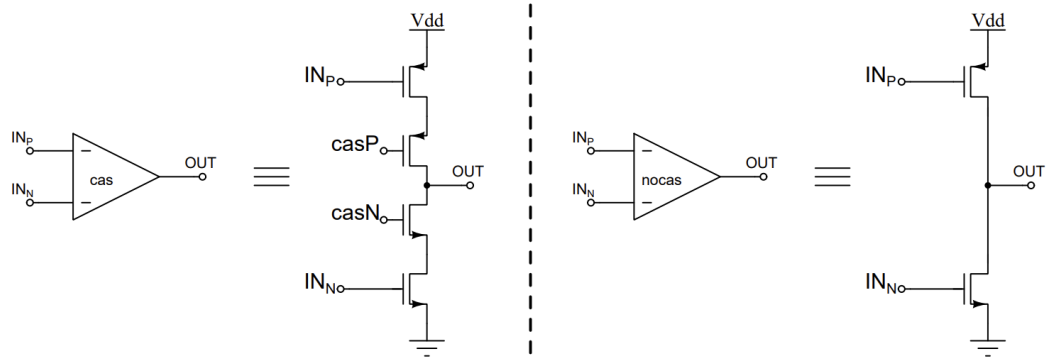

- 3D INTEGRATION: vertical interconnection of different active layers (different ASICs for example) using TSV (Through Silicon Vias)
- Possibility of eliminate the inactive areas due to wire-bondings and enable “abutting”
- Each layer can be assigned to a particular function, e.g. ( Front-end, Clock distribution, data merging)

# IGNITE AFE schematic:




Two Core Amplifier solution:

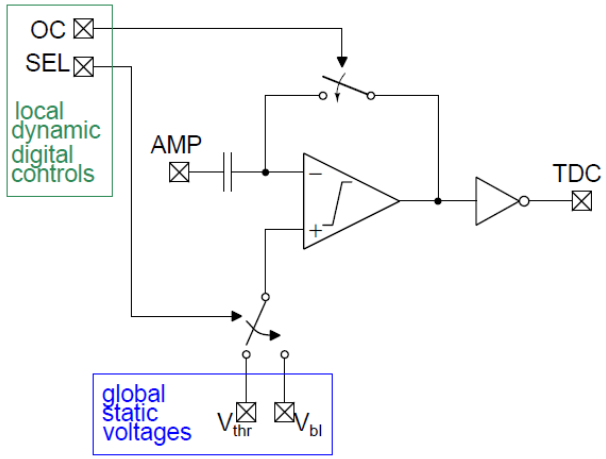
- Cascoded Inverter
- No-Cascode inverter

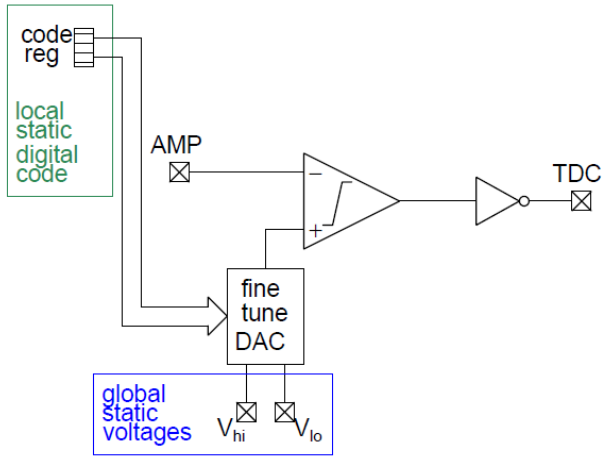



General architecture of the Analog Front-End

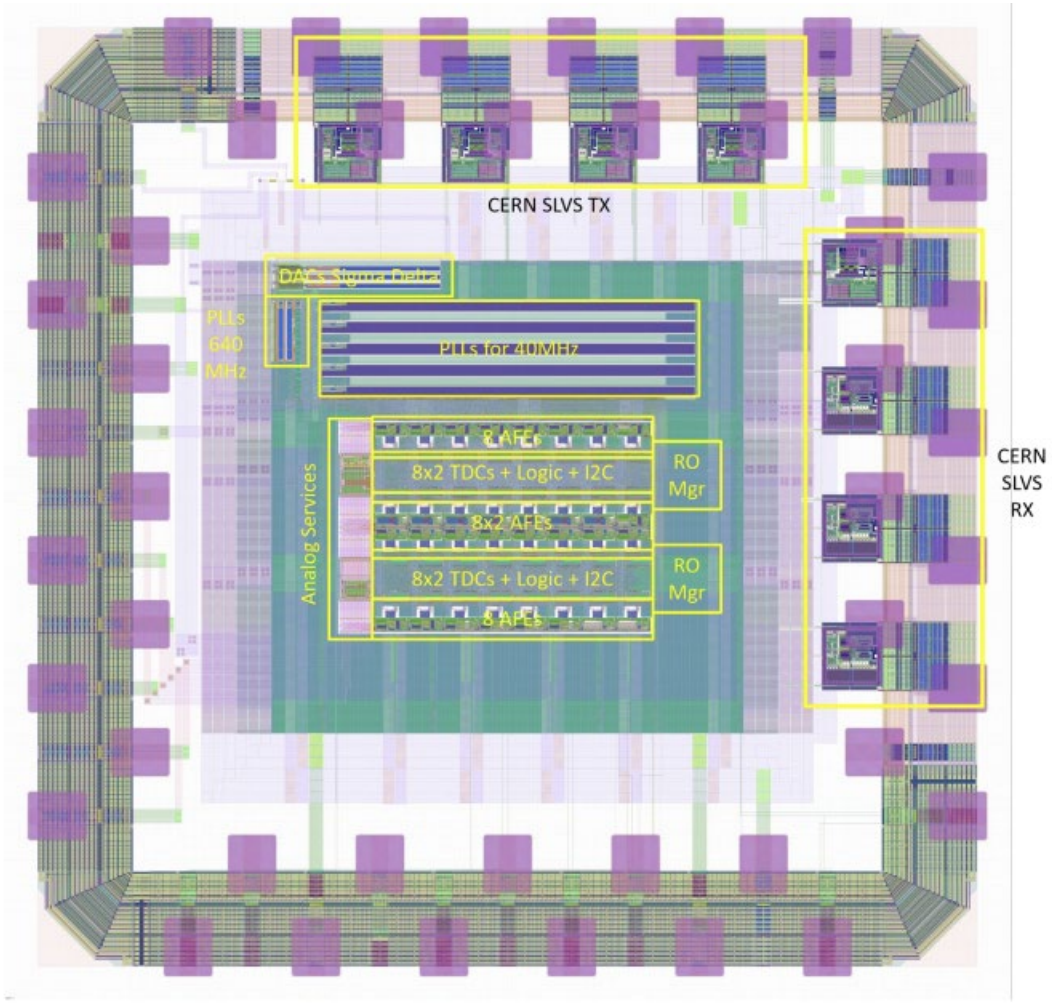
- Single Krummenacher Feedback
- AC coupling
- Dual Stage Discriminator

Two channel equalization solution: Offset Compensation, Finetune DAC



# RESULTS: IGNITE0 TEST CHIP

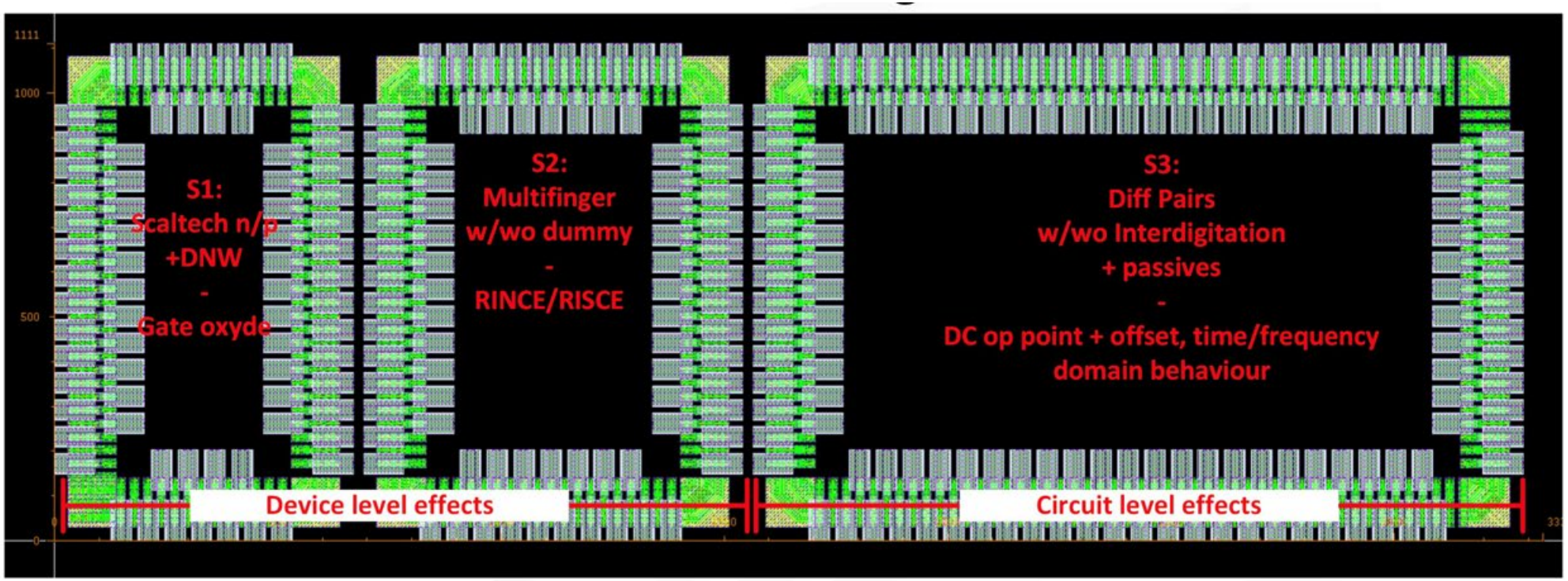



**IGNITE0 mini@SIC**

READOUT SYSTEM:

- One 16-word depth FIFO for each 8x2 block
- Each event is a 49-bit word that includes all the info (Vernier counters, TOT, Coarse Timestamp/Bxid, Event type, pixel Address, FIFO Status)
- Data not optimized for bandwidth (testing purposes)
- Data out on two differential lines @ 640 Mb/s
- Max event rate per output line/FIFO => ~ 12.5 MHz
- Max event rate per pixel ~ 780 KHz

# IGNITE radiation hardness of 28nm HPC+:




IGNITE RAD-CHIP

- Submitted in April, samples arriving
- PCB for testing under preparation
- Irradiation test scheduled in Padua