Status of the Picopix chip

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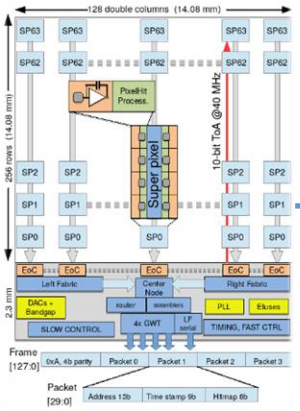
19th October 2023

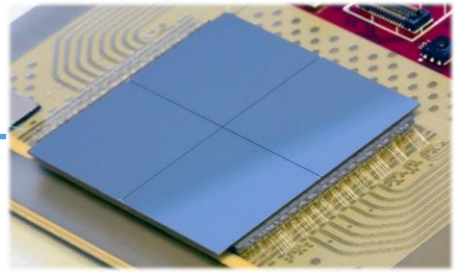
Index

1. Velopix2 and Picopix
2. Analog FE
3. Time Measurements
4. On-Pixel Clustering
5. Read-out Architecture
6. High-Speed Links

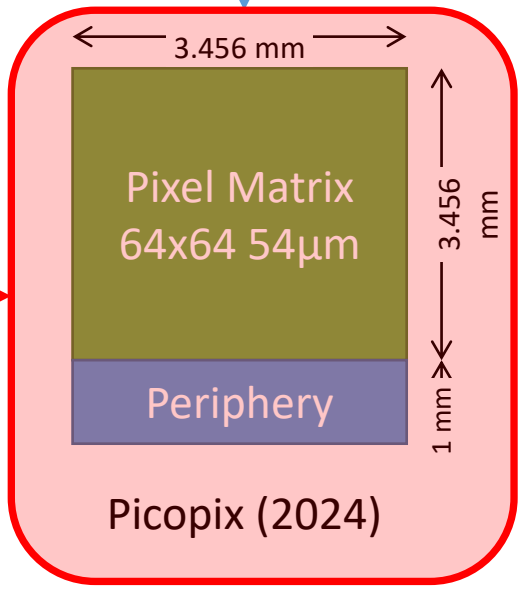
Velopix2 Roadmap



Velopix (2016)

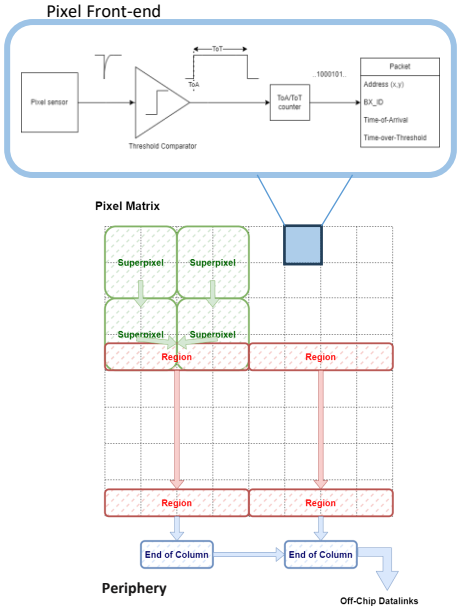


Timepix4 (2019)



Picopix (2024)

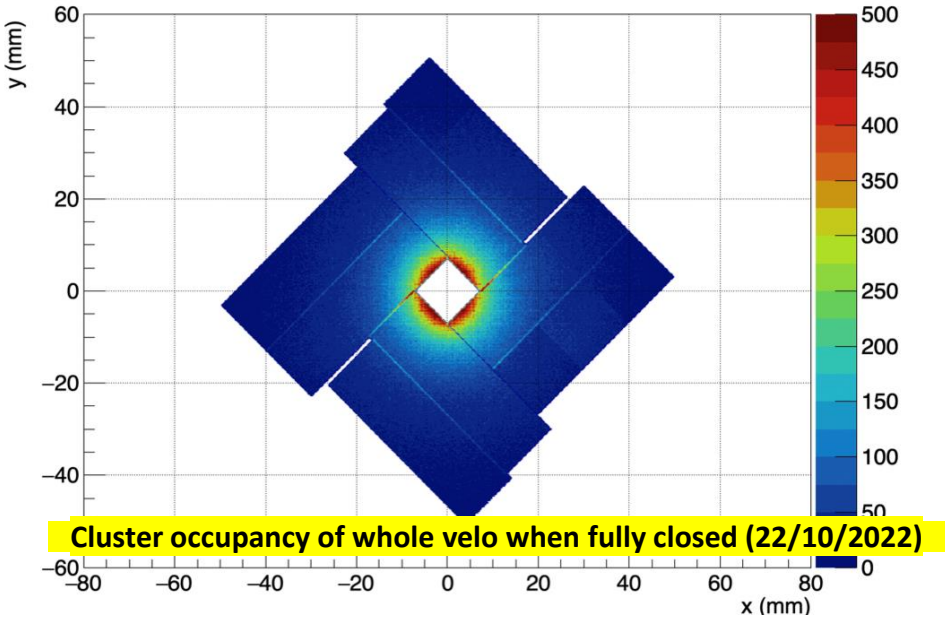
We are here



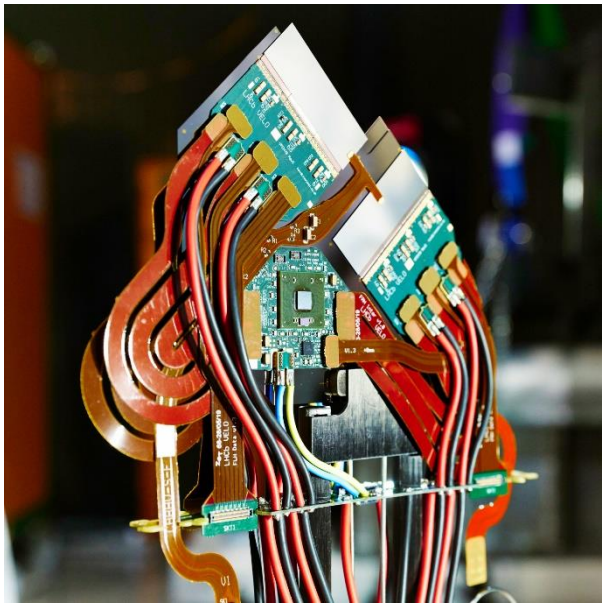
Velopix2 (HL-LHC)

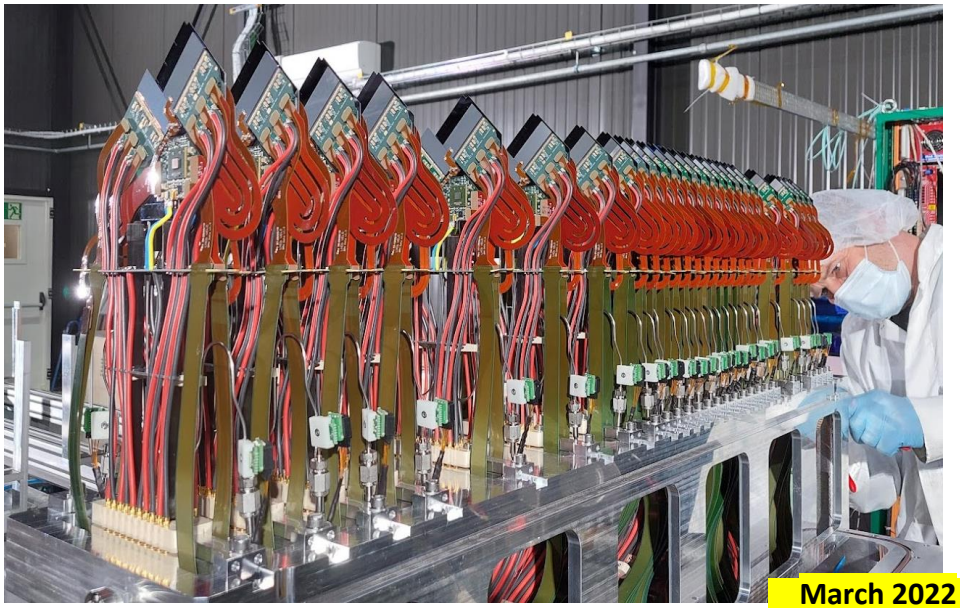
Velopix (2016)

Technology		TSMC 130nm – 8 metal
Pixel Size		55 x 55 µm
Pixel arrangement		256 x 256 (2x4 superpixels)
Sensitive area		1.98 cm^2
Data driven (Tracking)	Mode	Binary (hitmap) + TOA
	Event Packet	30-bit
	Max rate	**$5x10^6$ hits/mm^2/s**
	Max Pix rate	**~50 KHz/pixel**
TOT energy resolution		**< 1Kev**
Time resolution		**25ns**
Readout bandwidth		4x @5.12 Gbps
Minimum threshold		<500 e^-



Cluster occupancy of whole velo when fully closed (22/10/2022)

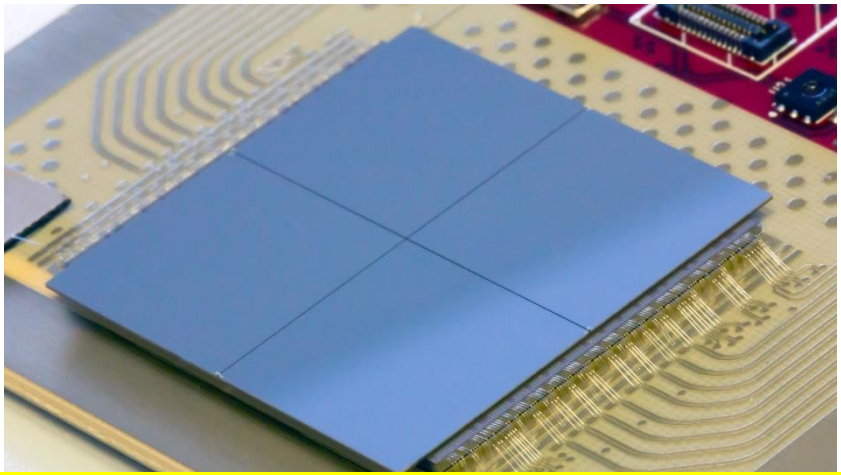




March 2022

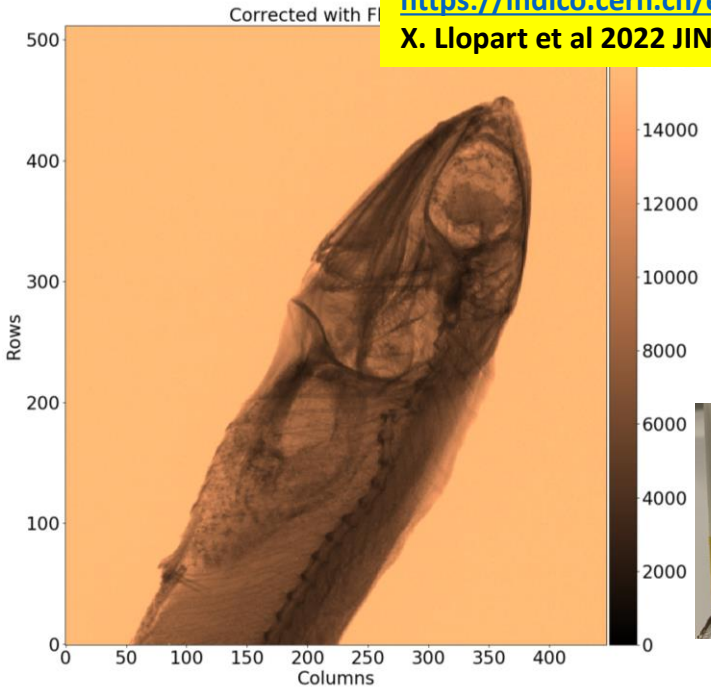
Timepix4 (2019)

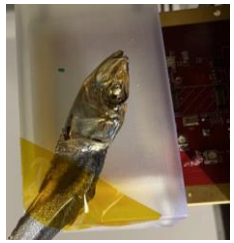
Technology			65nm – 10 metal
Pixel Size			55 x 55 µm
Pixel arrangement			4-side buttable 512 x 448
Sensitive area			6.94 cm^2
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA
		Event Packet	64-bit
		Max rate	**3.58x10^6 hits/mm^2/s**
		Max Pix rate	**10.8 KHz/pixel**
	Frame based (Imaging)	Mode	CRW: PC (8 or 16-bit)
		Frame	Not-zero-suppressed
		Max count rate	~5 x 10^9 hits/mm^2/s
TOT energy resolution			**< 1Kev**
Time resolution			**195ps bin → ~60ps$_{rms}$**
Readout bandwidth			16x @10.24 Gbps
Minimum threshold			<500 e^-



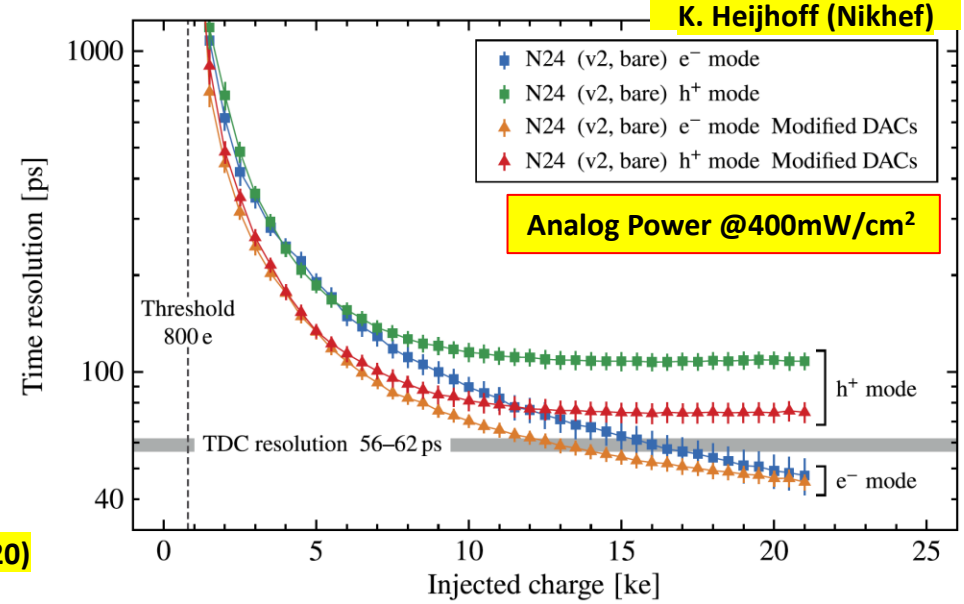
Timepix4v0 with 4x300 µm (256x256) edgeless Si sensor (August 2020)

https://indico.cern.ch/event/1121147
X. Llopart et al 2022 JINST 17 C01044

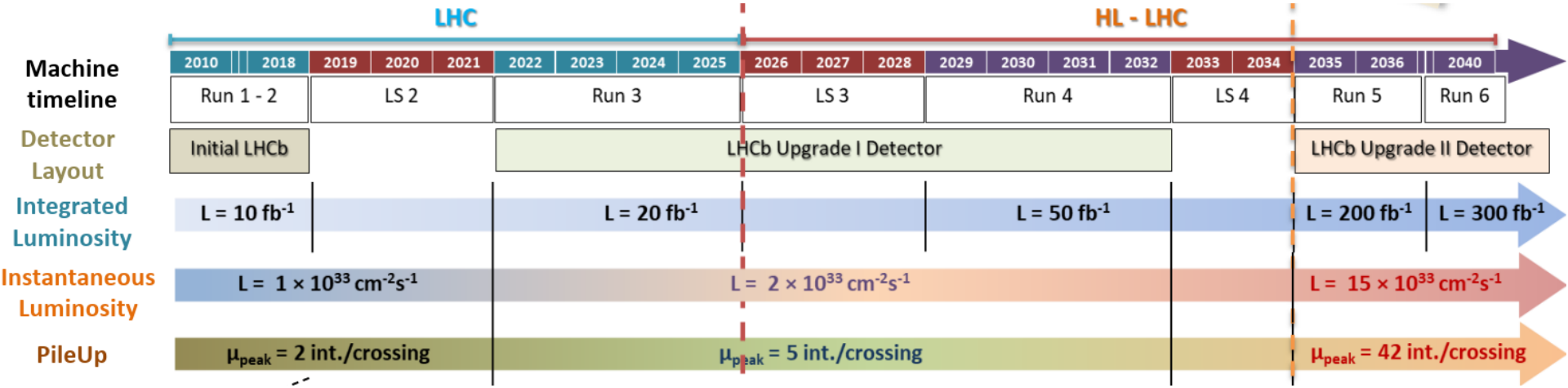


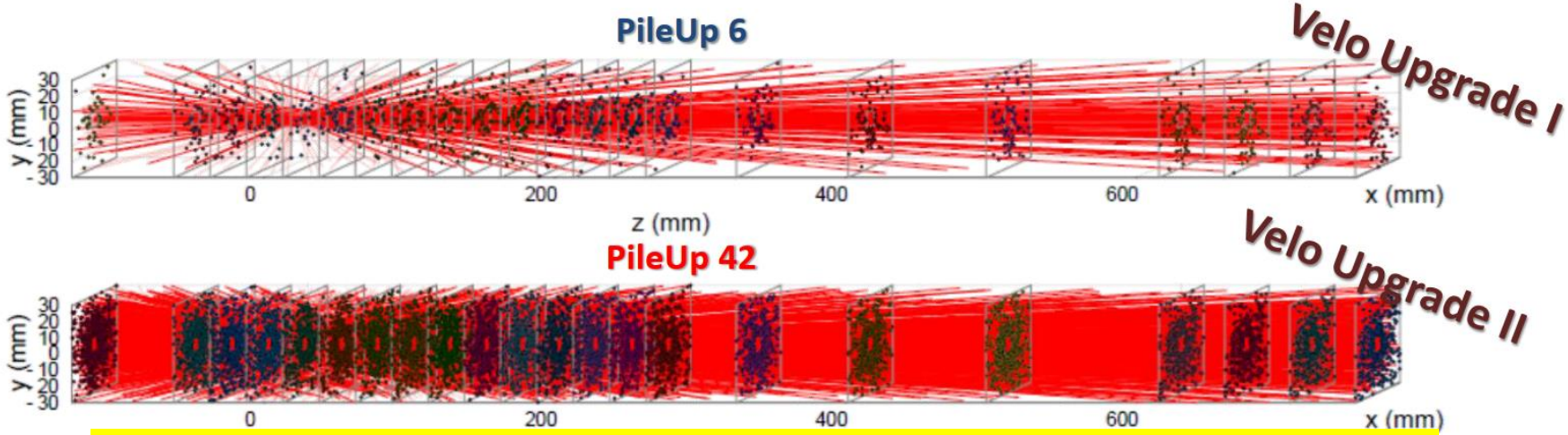


K. Heijhoff (Nikhef)



Towards HL-LHC in LHCb





If track time information <**20ps$_{rms}$** Primary Vertices can be reconstructed !!

https://indico.cern.ch/event/1140707/contributions/5067786/attachments/2536255/4365084/Gkougkousis_VERTEX22.pdf

Initial LHCb requirements for Velopix2

Requirement	scenario S_A	scenario S_B
Pixel pitch [µm]	≤55	≤42
Matrix size	256×256	335×335
Time resolution RMS [ps]	≤ 30	≤ 30
Loss of hits [%]	≤ 1	≤ 1
TID lifetime [MGy]	> 24	> 3
ToT resolution/range [bits]	6	8
Max latency, BXID range [bits]	9	9
Power budget [W/cm^2]	1.5	1.5
Power per pixel [µW]	23	14
Threshold level [e$^-$]	≤ 500	≤ 500
Pixel rate hottest pixel [kHz]	> 350	> 40
Max discharge time [ns]	< 29	< 250
Bandwidth per ASIC of 2 cm^2 [Gb/s]	> 250	> 94

Priority

Challenging!

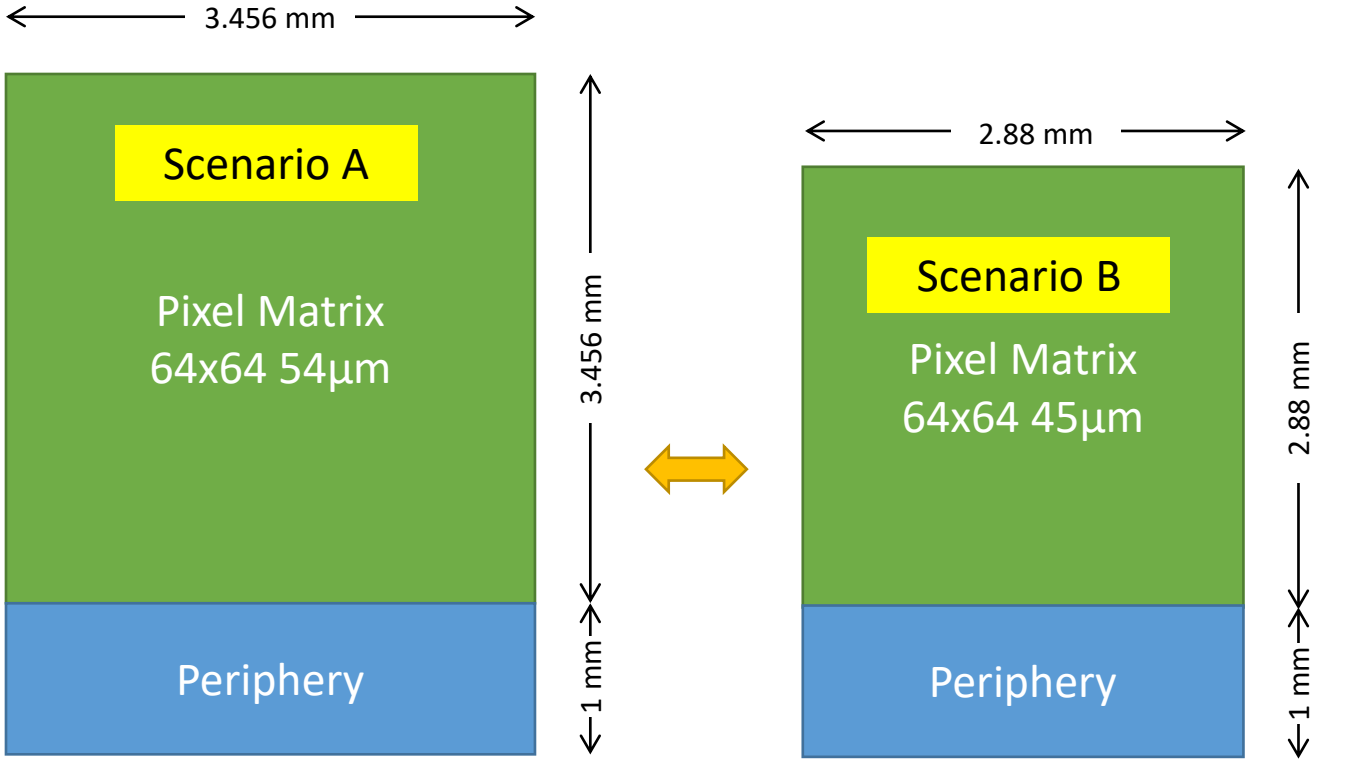
doable

Velopix2 demo chip → PicoPix

- TSMC HPC+ 28nm → Provides great level of integration at the Pixel level
  - Large choice of standard cell libraries included characterized at 0.8V, 0.9V and 1V
  - Radiation tolerance is better than in 65nm and 130nm
  - Make use of different Macro blocks being developed in the section (Serializer, DACs, ADC, IO Pads, DC-DC,…)
  - TSMC 28nm is a 90% linear shrinkage process from 32nm technology

- Designed as a "real" small scale prototype of the large Velopix2 to avoid to get false expectations on final design:
  - Analog FE
  - TDC (local DCO)
  - Pixel data clustering
  - Pixel readout
  - SEE robust architecture (TMR)
  - Clock distribution using dDLL approach (as in Timepix4)
  - High-speed links (DART28)
  - On-chip Bandgap and biasing DACs
  - UVM Functional verification

PicoPix ASIC



~120 K$

~75 K$

Pixel Size	
Drawn	Si
50	45
51	45.9
52	46.8
53	47.7
54	48.6
55	49.5
56	50.4
57	51.3
58	52.2
59	53.1
60	54
61.111…	55

- Price for 100 chips and all options
- Design time comparable to a full-scale design if targeting a “real” Velopix2 prototype
  - Might be spaced limited in the periphery…
- Bump-bonding with diced ASICs

Time resolution in tracking detectors: VELO2 case

- **Target resolution of <20ps$_{rms}$** track time is required to distinguish PV
- Single plane resolution of <50ps$_{rms}$ → σ^2_{sensor} (40ps$_{rms}$) + σ^2_{ASIC}
- σ^2_{ASIC} (30ps$_{rms}$) → $\sigma^2_{analogFE}$ + $\sigma^2_{conversion}$ + σ^2_{clock}

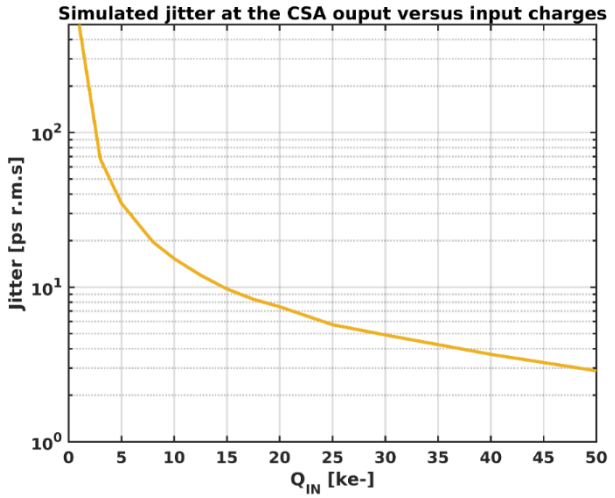
- $\sigma^2_{conversion}$ → $\frac{TDC_{bin}}{\sqrt{12}}$ → TDC$_{bin}$ = 40ps → 11.5 ps$_{rms}$
- σ^2_{clock} → Reference clock at pixel level < 10 ps$_{rms}$
- $\sigma^2_{analogFE}$ → <25ps$_{rms}$

Analog FE

Limits to time resolution in analog FE

$$Jitter_{FE} \propto \frac{C_{DET}^{3/2}\sqrt{C_{OUT}}}{g_m\sqrt{C_{FB}}} * \frac{\frac{Q_{IN}}{C_{FB}}}{\frac{Q_{IN}}{C_{FB}} - V_{THR}}$$

- C_{DET}, C_{FB}, and C_{OUT} are the front-end input, feedback, and output capacitances, respectively.
- g_m is the input transconductance
- V_{THR} is the threshold of the comparator



→ Minimize the front-end output capacitance.

→ Maximize the input charge and decrease the threshold.

→ Increase the analog pixel power consumption, but a large power drop over the ASIC worsens the timing performances!

→ The front-end input capacitance must be minimized, which depends on the choice of the sensor, pixel pitch…

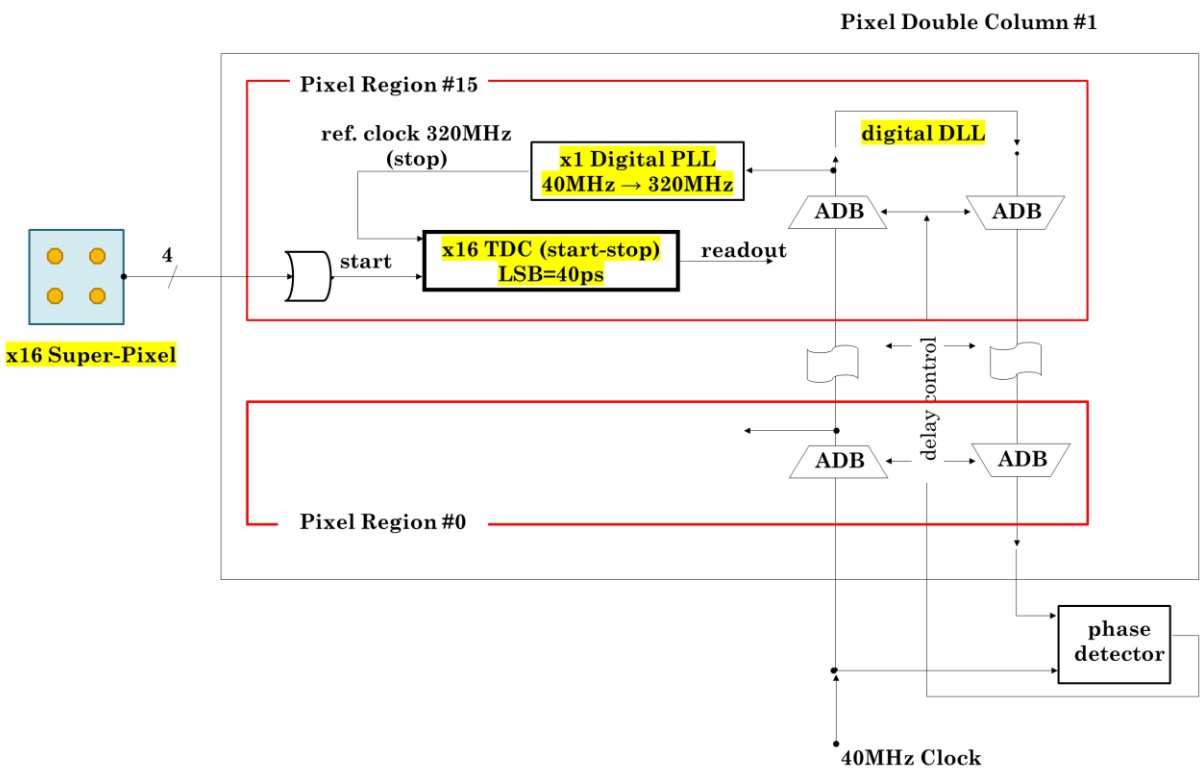
R.Ballabriga, The Timepix4 analog front-end design: Lessons learnt on fundamental limits to noise and time resolution in highly segmented hybrid pixel detectors https://doi.org/10.1016/j.nima.2022.167489

On-time measurements <30ps$_{rms}$

1) TOA Blocks
2) TOA & TOT Measurement

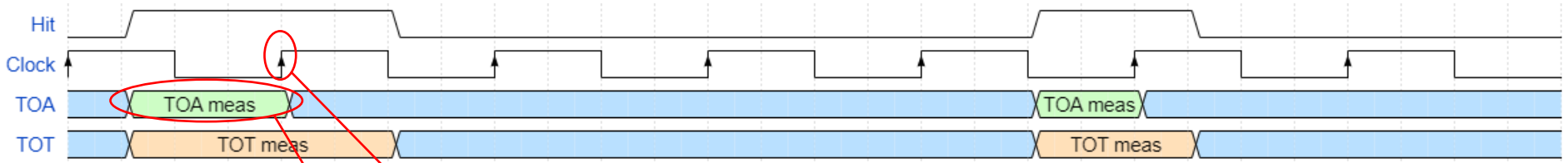
TOA Acquisition

- Digital Front-End jitter → $\sigma_{digitalFE}$ <17ps_{rms} :
  - $\sigma_{conversion}$ → $\frac{TDC_{bin}}{\sqrt{12}}$ = 11.5 ps_{rms} with TDC_{bin} = 40ps → 11.5 ps_{rms}
  - σ_{clock} < 10 ps_{rms} → from dPLL clock @320MHz



Time and Energy Measurement

- Time of arrival (TOA):
  - Coarse TOA → sample a BxID transmitted across the matrix (40MHz)
  - Fine TOA → measure Hit from first rising edge @320MHz to next rising edge @40MHz
  - Ultra-Fine TOA → measure from TDC with 40ps bins
- Time over threshold (TOT):
  - Measure the discriminator ON duration (320MHz) → Equivalent energy measurement



Reference clock distribution is critical:
- Pixel to pixel skew (static) can be corrected (calibrated)
- Clock jitter (dynamic) cannot be corrected

On-Pixel Time-to-Digital Converter (TDC):
- 40ps bin → 25GHz clock bin (needs calibration)
- Low area, low power TDC

On-Pixel Clustering

1) Master Pixels
2) Large Cluster Removal

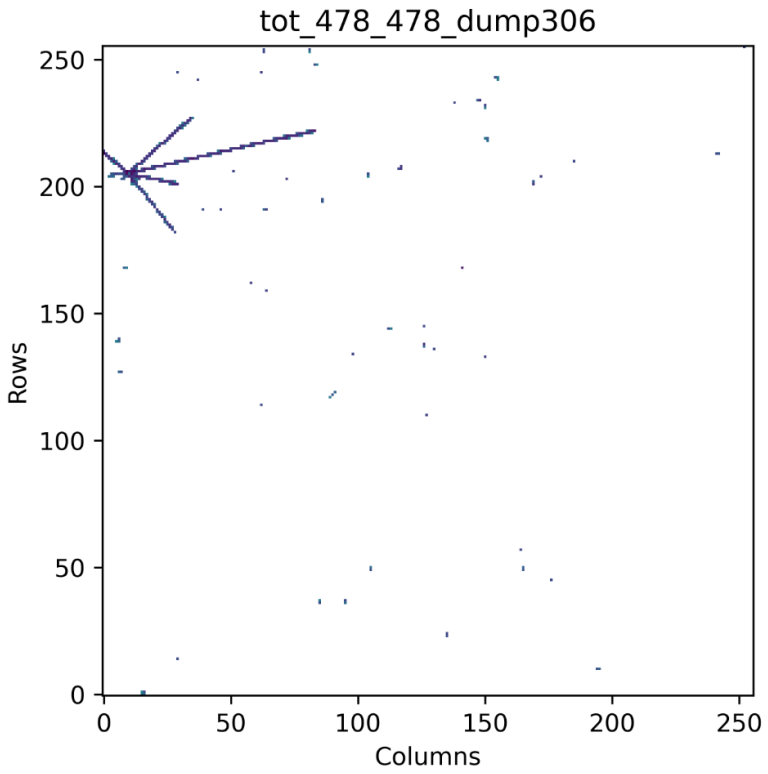
Cluster analysis

- PP simulation data analysis over 560 ASICs shows clusters sizes:

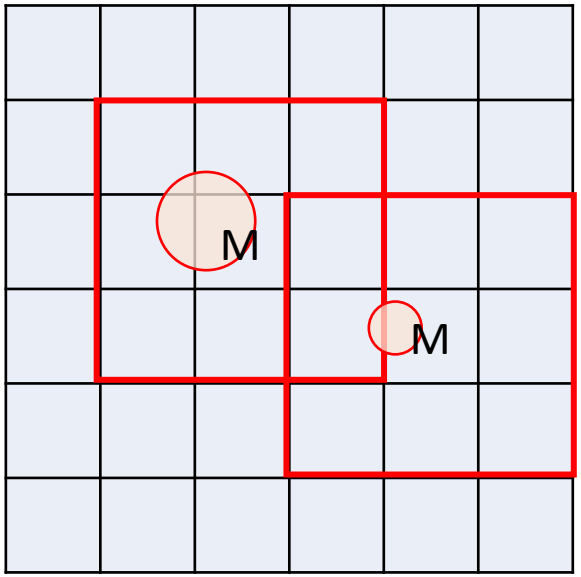
Cluster Size	1	2	3	4	Other	
Num Clusters	4666212	4510943	1286141	548639	480585	1149252
	40.6%	39.3%	11.2%	4.8%	4.2%	100.0%

- >99.5% of small clusters (3x3 pixel hits) have $\theta < 0.5$mrad:
  - **Readout only small clusters**

- Some clusters have large numbers of pixel hits (>300):
  - 19.7% of pixels hit are from large clusters
  - Big spread depending on ASIC position
  - **Early detection and filtering** have a big impact in power, bandwidth…



On pixel event processing → Data reduction

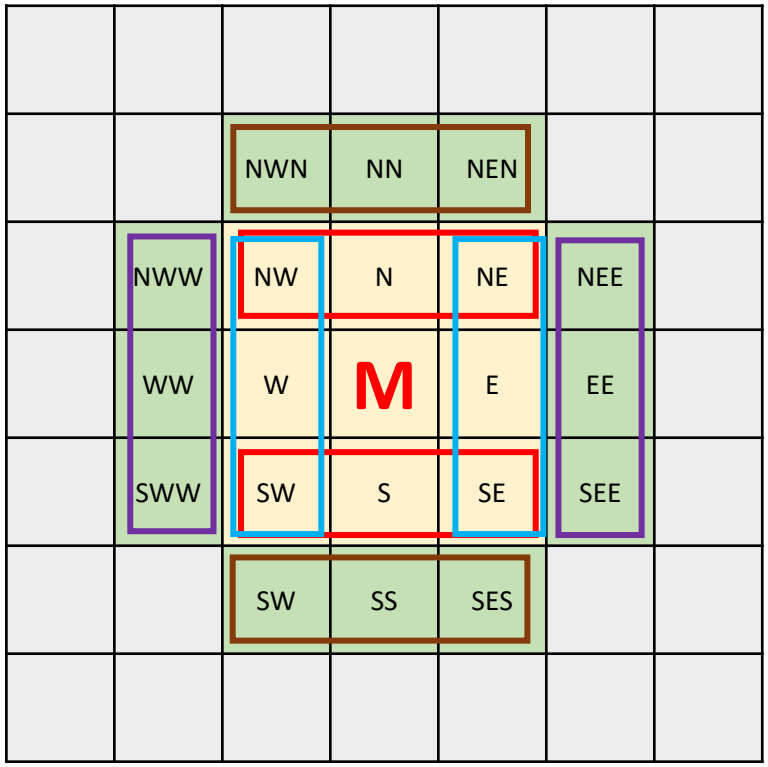


- Most events are clusters of 1-4 pixels
  - Readout only the largest event in a cluster → Best time (TOA) and energy (TOT) resolution
- Cluster events in X and Y in a single data output packets:
  - 1 data packet per cluster
  - Master (M) pixel found using arbitration circuitry as in Medipix4
  - TOA and TOT only on Master (M) pixel
  - Hitmap of pixels around Master (M)
- Advanced on-pixel data filtering possible:
  - Accept events only in certain TOT range
  - Accept events only in certain TOA range
  - Accept events only for certain hitmap range

Fundamental to filter undesired data at pixel level !!!

On-pixel VETO Large Clusters

- Based in TOT using arbitration + hitmap + veto logic:
  - Works asynchronously and across the whole matrix → No clock (low power)
  - Can be disabled



VetoN = (NW or N or NE) and (NWN or NN or NEN)
VetoE = (NE or E or SE) and (NEE or EE or SEE)
VetoS = (SW or S or SE) and (SW or SS or SES)
VetoW = (NW or W or SW) and (NWW or WW or SWW)

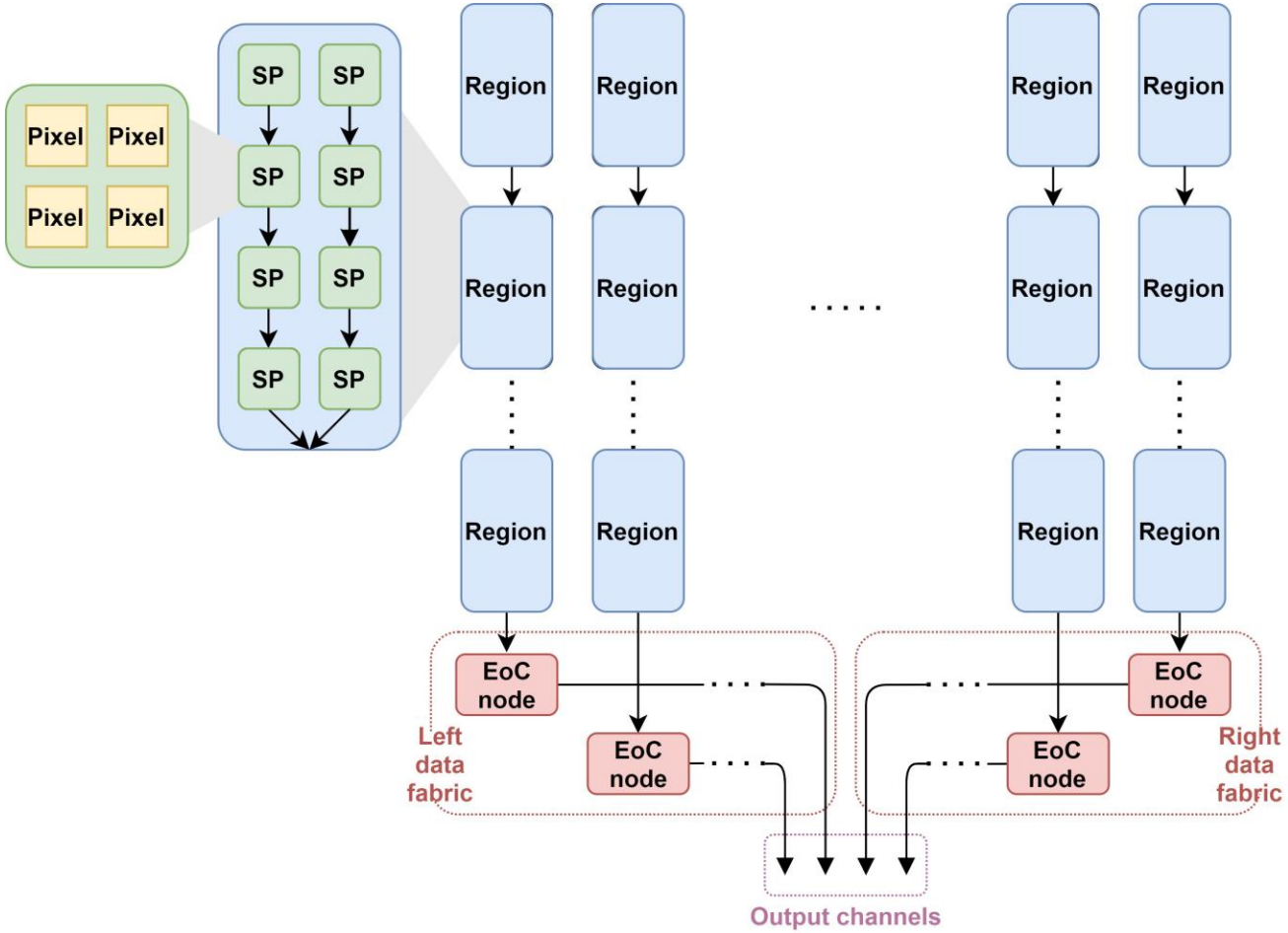
VETO_Large_hit = VetoN or VetoE or VetoS or VetoW

Pixel to output data readout

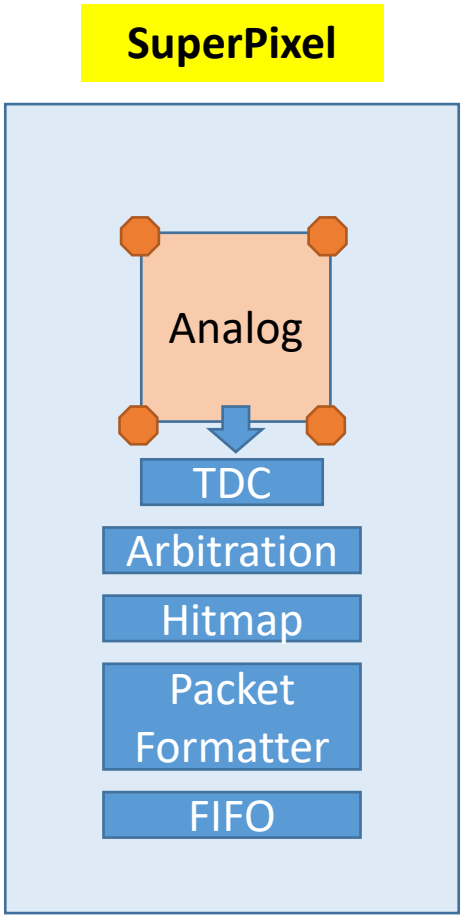
1) Superpixels
2) Regions
3) High-level Modeling
4) Reduction in the periphery

Read-out Architecture

- Triggerless, data-driven read-out
- Pixel → Superpixel → Region → End-of-Column

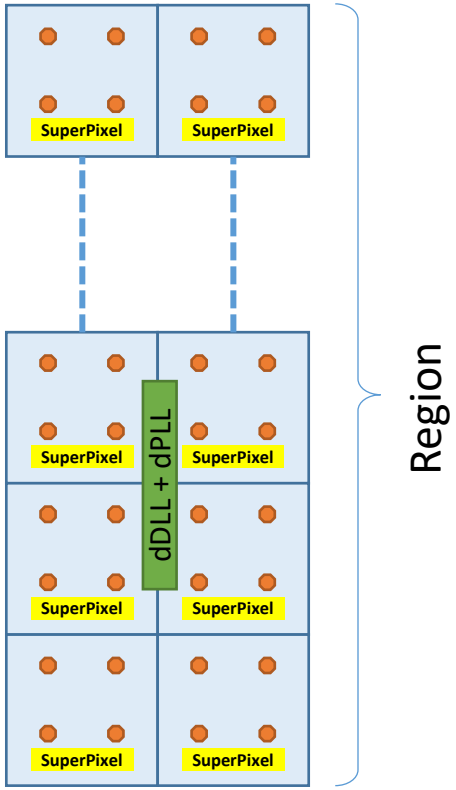


Pixel Matrix organization: PicoPix SuperPixel



- 1 Analog island:
  - 4 FE + 4 Disc
  - Threshold (5-bit) and TOT (3-bit) calibration
- 1 TDC:
  - Discriminator outputs are OR-ed → Only 1 TDC measurement per SuperPixel
  - In Timepix4 each pixel has an independent measurement → "Simpler" block for PicoPix
- Arbitration:
  - Finds the pixel with larger charge → Winner
  - From Medipix4
  - Works across SuperPixels in all directions
- Hitmap:
  - Finds pixel with a HIT around the Winner
  - Works across SuperPixels in all directions
- Packet Formatter:
  - Might add local filtering: TOT, size of hitmap,…
- FIFO:
  - Stores data temporarily

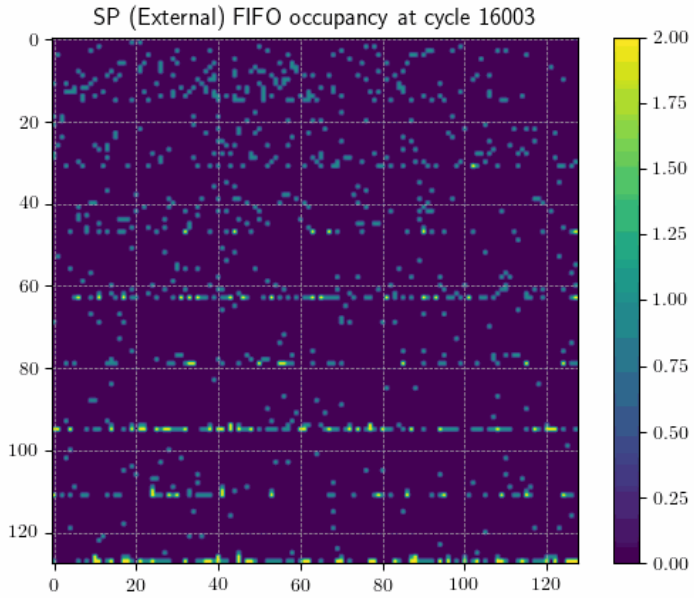
PixeMatrix organization: Region and Full Columns



- Contains 2xN SuperPixels:
  - N is a parameter in the RTL code
  - N=4 → 32 pixels
  - N=8 → 64 pixels
- 1 dDLL station node
- Should be the macro block for array formation

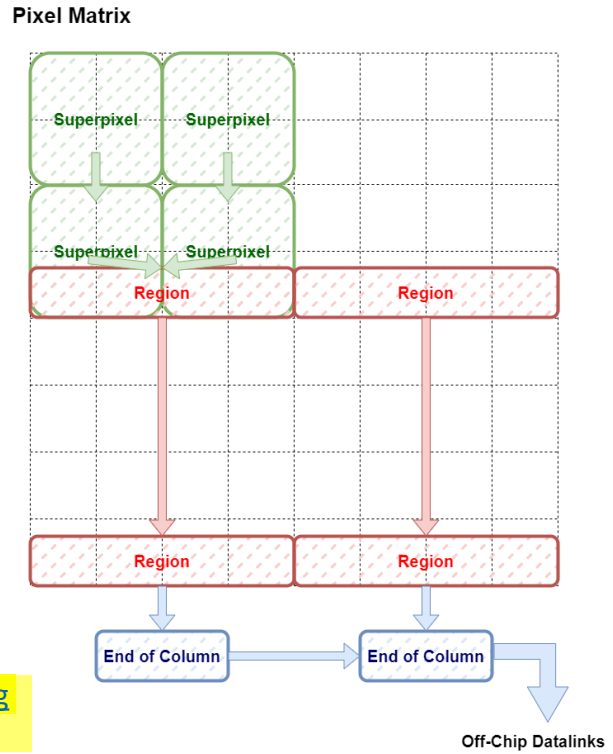
- M Regions form a full pixel column:
  - M is a parameter in the RTL code
  - M=16, N=4 → 512 pixels

PixelMatrix & Periphery



- High-level prototype (SystemC) for Velopix2
- Models data flow in pixel matrix and periphery, shows congestion and bottlenecks

	Velopix1	Velopix2
Pixel	256x256	256x256
SP	128x128	128x128
Regions	64x8	128x8
EoC	64 (8 ch.)	128 (16 ch.)

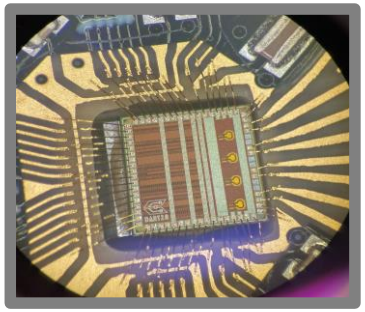


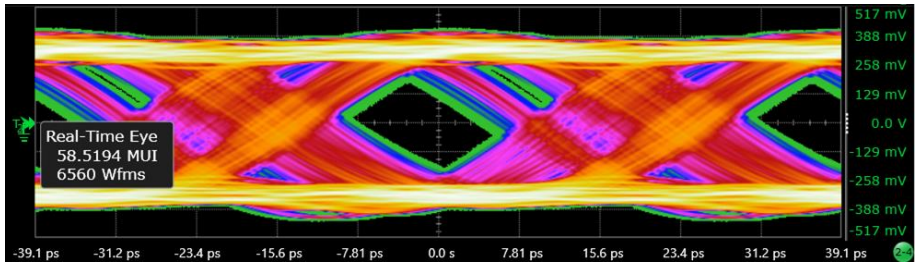
D. Ceresa, SystemC framework for architecture modelling of electronic systems in future particle detectors

High Speed Links

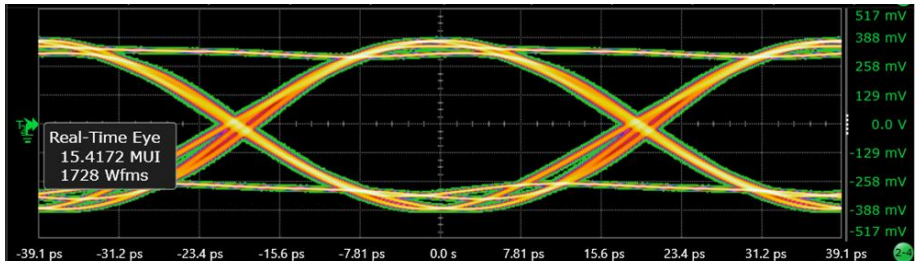
DART28 Testing Status

- DART28 has arrived, testing started
- All blocks operational, no functional issues:
  - Data generation, PLL, serializer, output driver
- PLL: Excellent jitter performance demonstrated
- 40MHz – 12.8 GHz: <300 fs rms
- Data transmission successfully demonstrated
- Performance degraded at 25.6 Gbps (data-dependent jitter):
  - Source: Supply bondwire inductance
  - Mitigation strategies being studied
- Sufficient performance at lower data rates (12.8 Gbps, 6.4 Gbps)

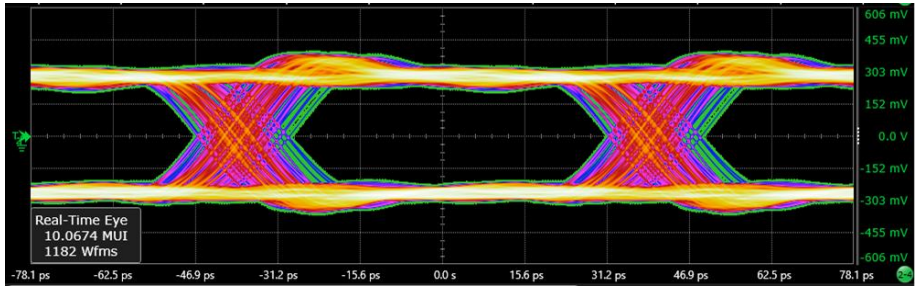




25.6 Gbps Line Driver (PRBS7)



25.6 Gbps Line Driver (Short Sequence)



12.8 Gbps Line Driver (PRBS7)

Summary and Project Status

- PicoPix is intended to be a “realistic” demonstrator chip for a possible future upgrade of the LHCb Velo project (LS4)
  - Main requirement is to target a time resolution < **$30ps_{rms}$**
  - Other very challenging requirements (pixel size, radiation hardness, power, bandwidth,…)

- Status → “exploration phase” of the specs limitations for a large $30ps_{rms}$ target ASIC:
  - Front-end limits and optimization
  - On-pixel TDC
  - dDLL reference clock distribution
  - On-pixel clock-cleaning PLL (Nikhef) + local LDO
  - 1st full column RTL exists
  - Readout architecture studies for Velopix2 → adapt to Picopix

- Project organization:
  - Bi-weekly design meetings have been organized
  - Design team: CERN, Nikhef and IGFAE

BACKUP

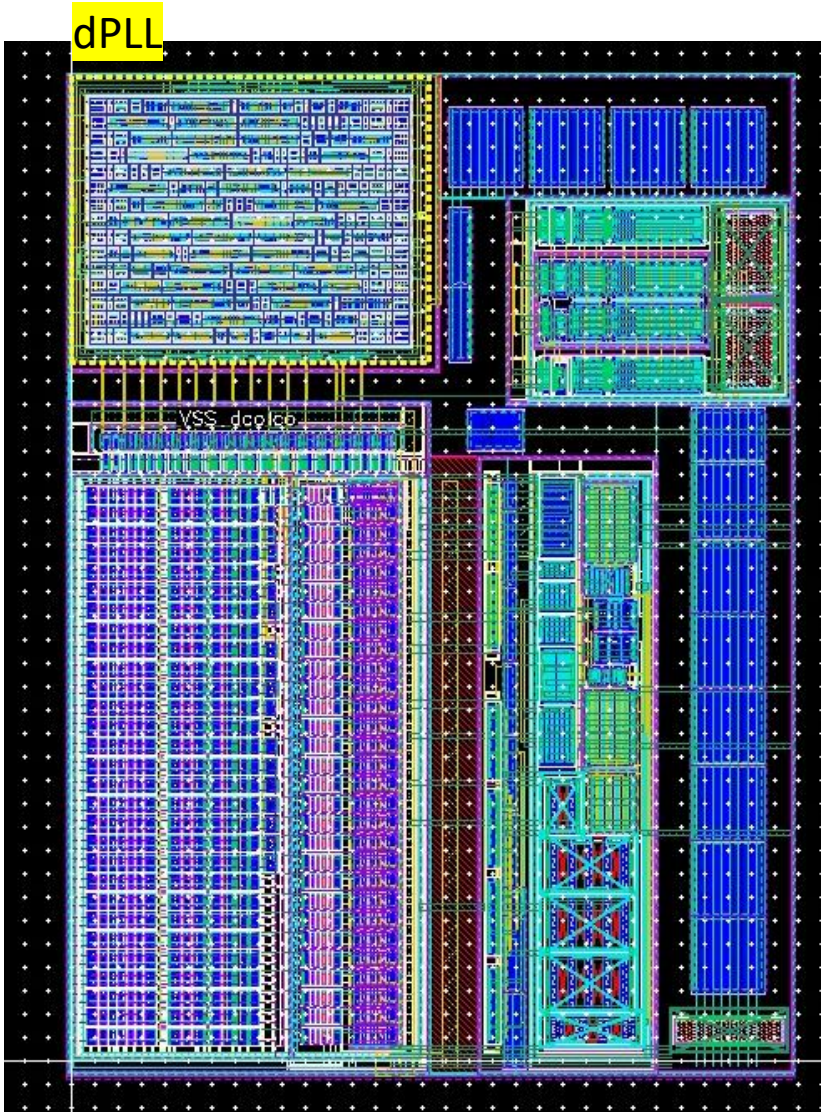
Project manpower

- Manpower:
  - CERN:
    - V. Sriskaran: Analog FE + analog periphery (100%)
    - S. Esposito: Functional verification and architecture debugging (50%)
    - A. Caratelli: digital designer (70%)
    - G. Bergamin: digital designer (30%)
    - X. Llopart: Project management & digital designer (50%)
  - NIKHEF:
    - V.Gromov: On-pixel PLL
    - C.Akgun: Sigma-delta DAC
  - IGFAE:
    - A. Fernandez: DAQ studies
  - More CERN manpower expected to join the team in 2024
    - Delayed due to CHIPS support to other projects
- Indirect manpower:
  - Many IP blocks in TSMC 28nm being designed in the CERN R&D (Serializer, SLVS drivers/receivers, PADs…)
  - CERN EP R&D WP5: Intelligence on detector

- Current submission plans Q2-Q4/2024

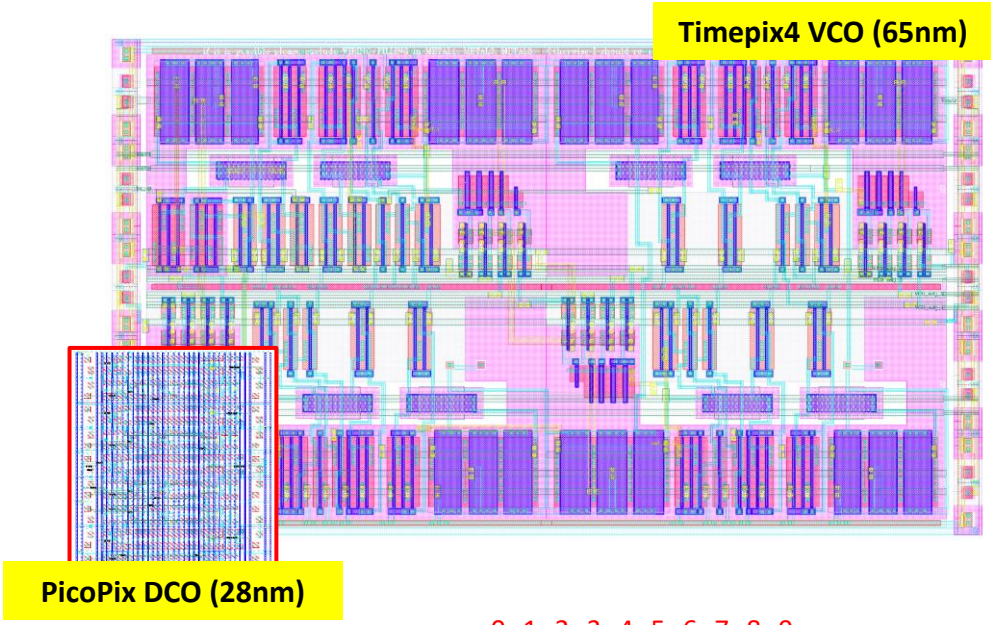
TOA Building blocks

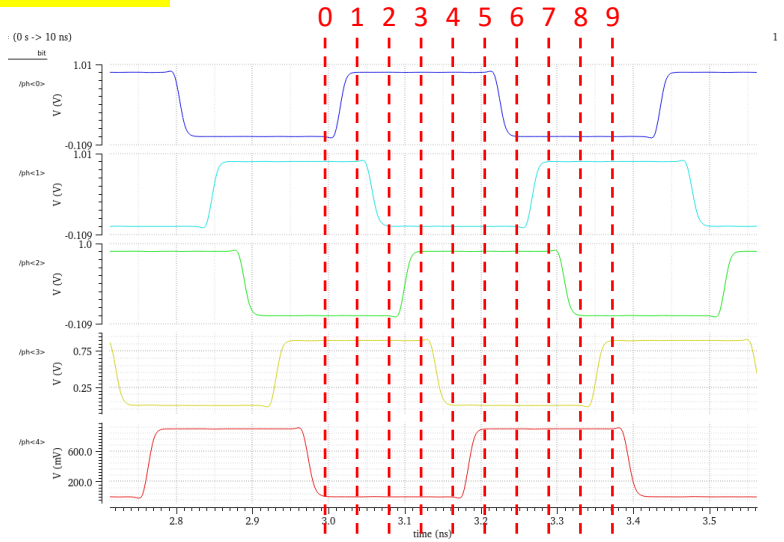
- dPLL (Nikhef) submitted in an MPW in September
  - Core is 25x40um
  - Generates 320MHz clock used for TDC while “cleans” jitter from column clock
- dDLL blocks are derived from Timepix4
  - Macro custom blocks are completed
- TDC is currently being implemented with a digital on top methodology
  - 2 DCO (5 phase and 7 phase) macros designed with 40ps LSB target



Free running On-pixel DCO

- Explored the idea of the on-pixel **free-running DCO with event-by-event calibration**:
  - With 3 bits oscillation control
  - Using 7T cells with extracted parasitic
- **Advantages**:
  - No control voltage distributed along the column
  - Systematic effects can be suppressed
  - Faster oscillation times and lower dynamic power → better time resolution
- **Disadvantages**:
  - Requires DCO calibration measurement → data bandwitdth!

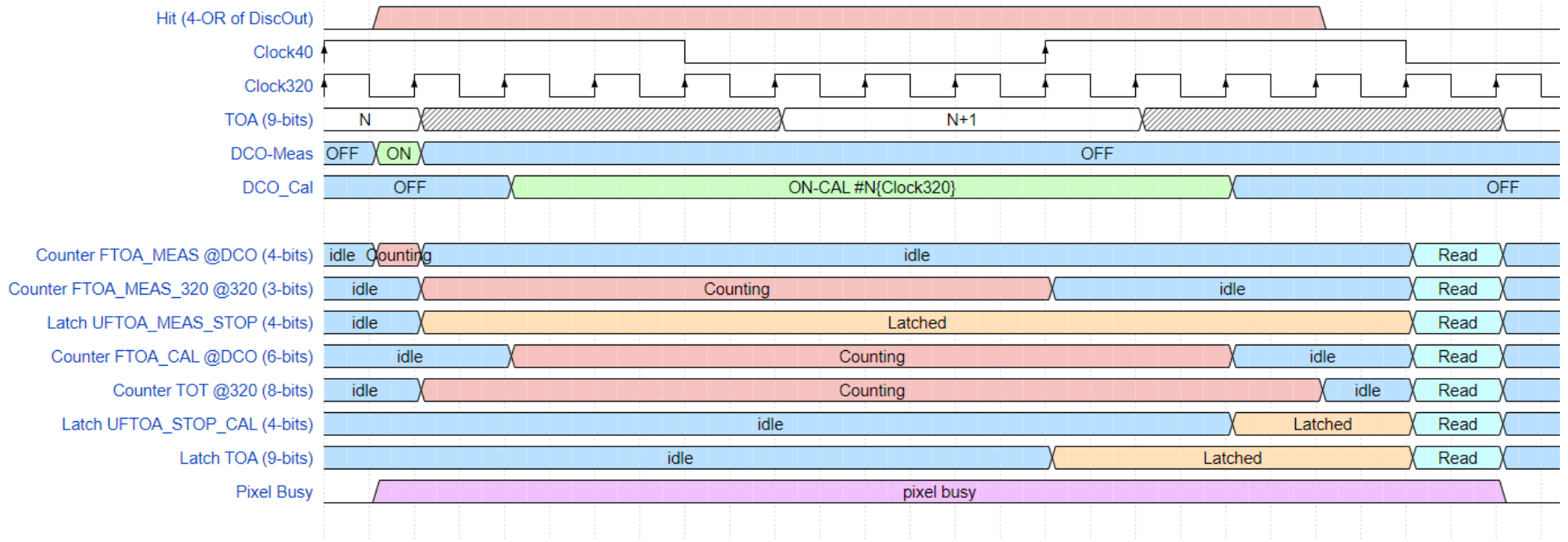




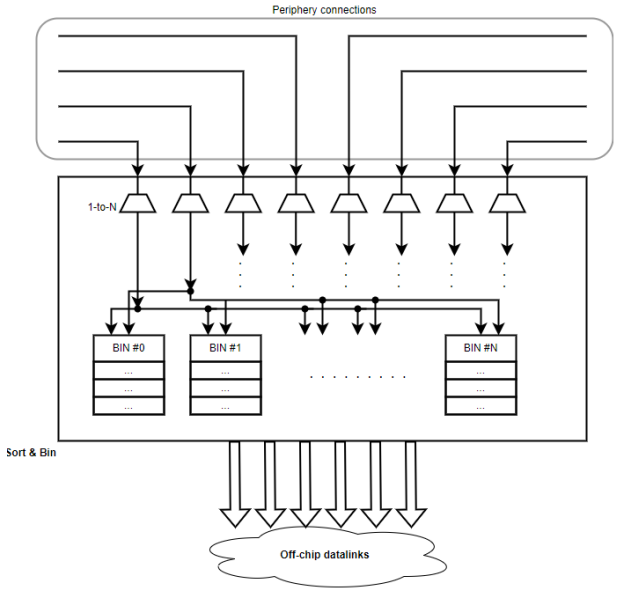
	freq	Phases	Phase mismatch [max-min]	LSB	Area	power
Timepix4 VCO	640 MHz	8	~25%	195ps	~350µm^2	~500µW
PicoPix DCO	2-3 GHz	10	< 5%	50-33ps	~38µm^2	~150µW

TDC Operation

- TOA → BxID (9-bit)
- At Periphery extract fine time (10-bit) based on:
  - FTOA_MEAS + FTOA_MEAS_320 + UFTOA_MEAS_STOP (11-bits)
  - FTOA_CAL + UFTOA_STOP_CAL (10-bits)



Data Reduction

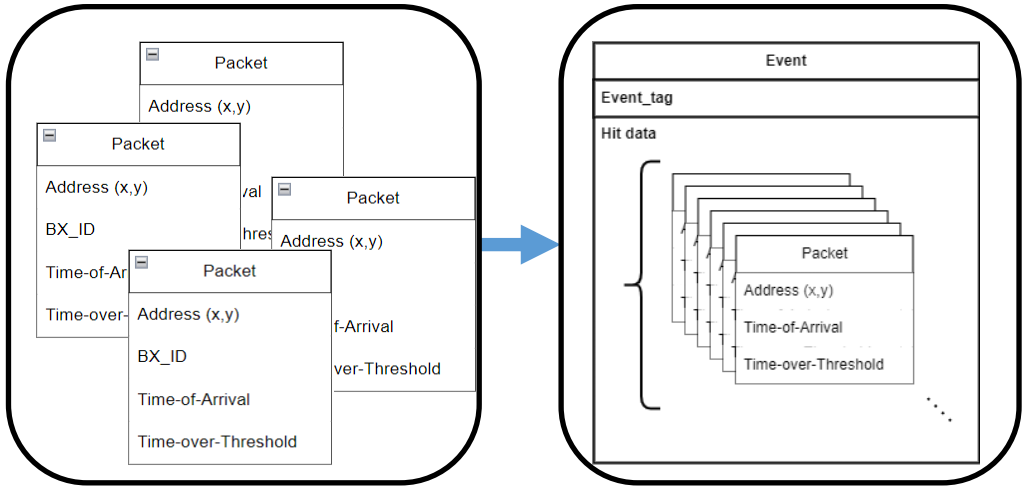


Sort&Bin module:

- **ASIC** module, placed between the EoC and off-chip data links of **Velopix2**
- **Accumulates** hit packets over time and **groups** them in bins based on event tag (BX)

Goals:

- Data reduction (~20 %)
- Fixed latency
- Power savings



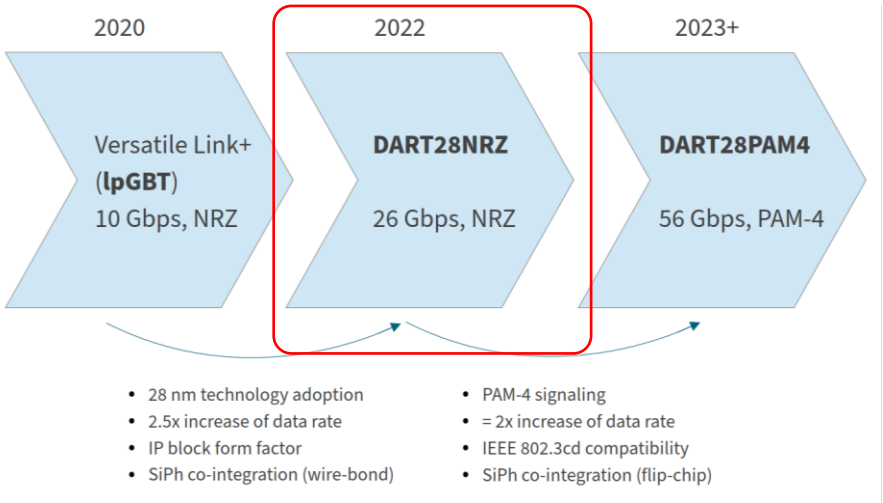
Out-of-order hit packets

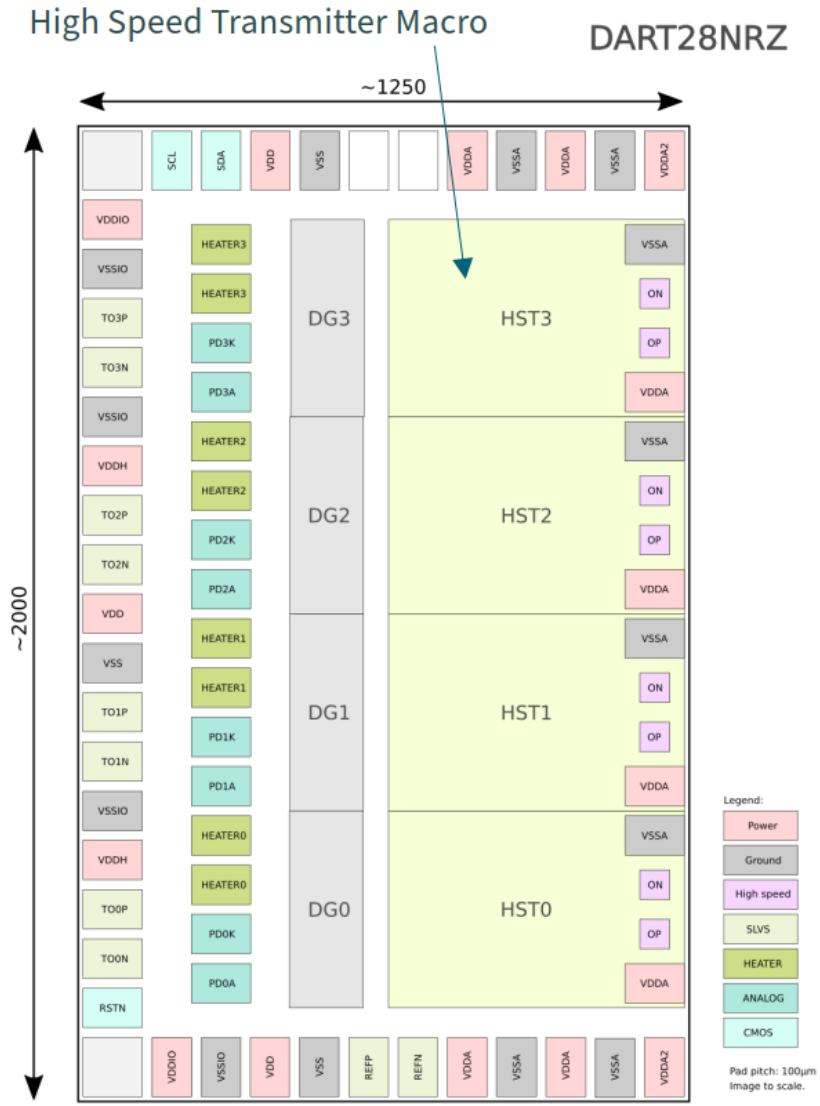
Event frame of hit packets

High Speed Links in 28nm

S.Bieregel (CERN-ESE-ME)
https://indico.cern.ch/event/1138500/

- WP6 ASIC Roadmap
- Planned submission in Q1/2023
- Demonstrate:
  - **Electrical**: correct operation of high-speed transmitter
  - **Optical**: SiPh integration, end-to-end optical link
  - **Dual Channel WDM***:2 NRZ links on one fiber

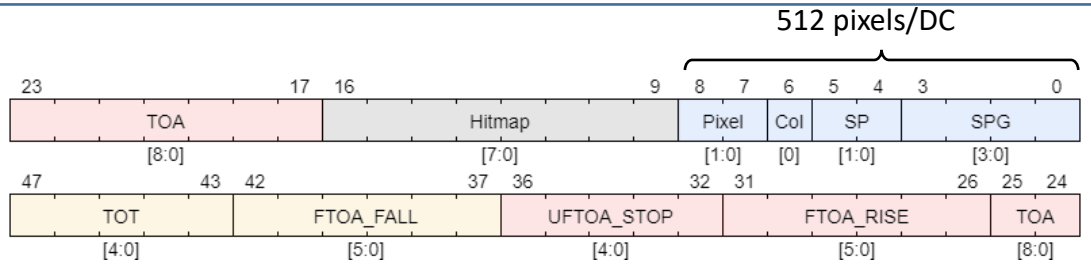




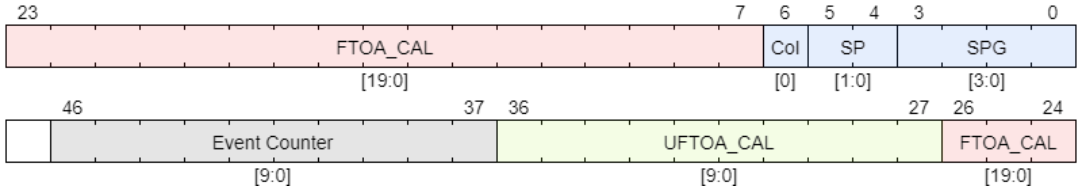
*Wavelength Division Multiplexing

Types of pixel packets

Event packet:
- 1 packet/event
- Address+hitmap+TOA+TOT



DCO Calibration packet:
- Cumulative calibration data → improved DCO measured frequency
- To be sent every N events or by DAQ request



Event counter packet:
- Used for threshold equalization, counting…