28nm technology and ASIC design in HEP experiments

VERTEX 2023

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Sestri Levante

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CERN

Introduction

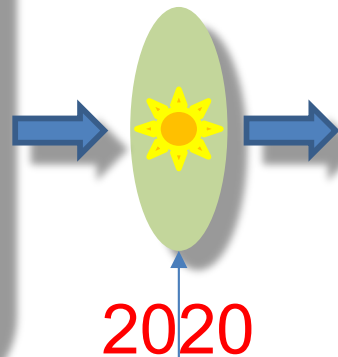- Why the 28nm node

- Technology Performance

- Common Design Platform

- Design Ecosystem

WP5.1 CMOS technologies

Survey of CMOS technologies

Selection Criteria
- Radiation Tolerance
- Accessibility
- Technical support
- Availability of IP blocks
- Long-term availability
- Cost

2020

Technology Selection

Design Platform
Mixed-Signal Design Kit,
Reference Workflows, Rad-Tol techniques

IP blocks
Rad-Tol IO pads, ESD structures, SRAMs
Rad-Tol Volt. Ref, ADC, DAC, PLL, DLL
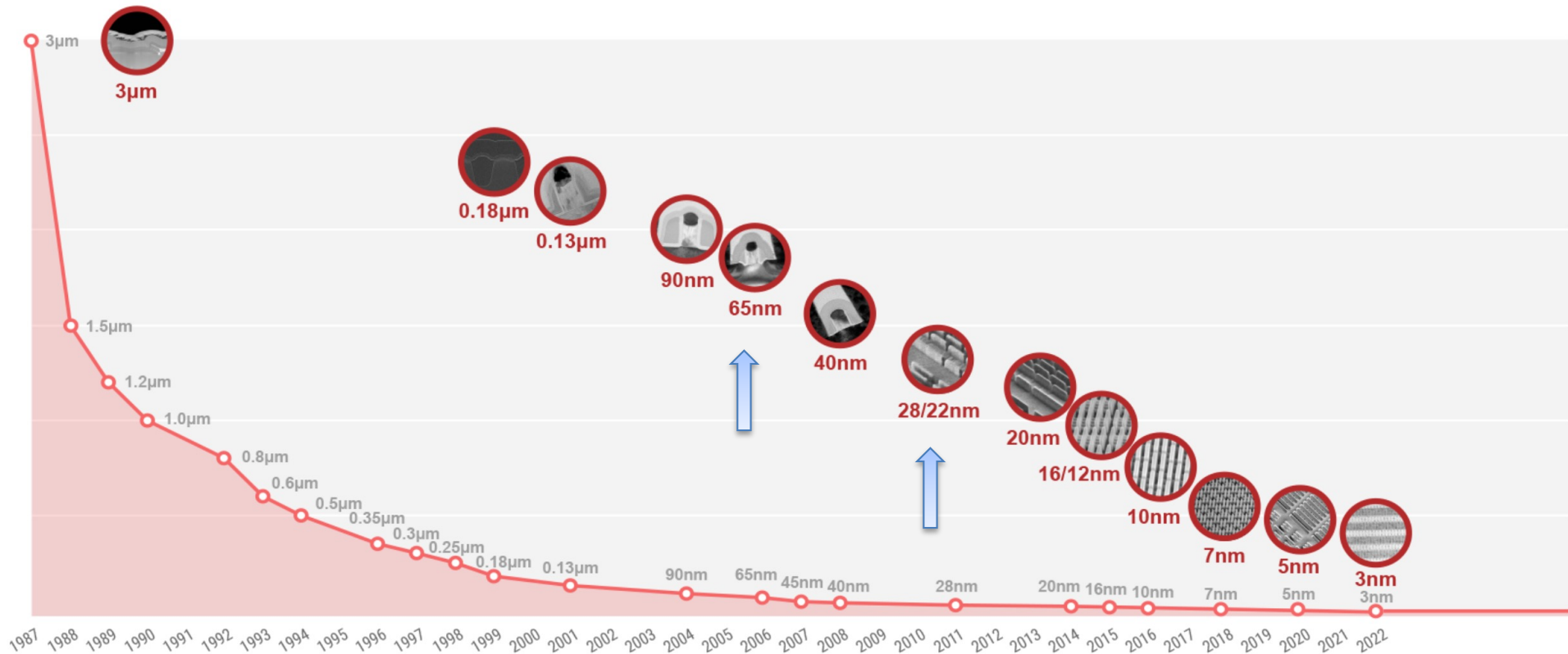
SOC Platform
System-On-Chip design Enablers

Collaborative Framework
NDAs, Commercial contract,
Support, Maintenance, Training

PERFORMANCE COMPARED TO 65 NM:
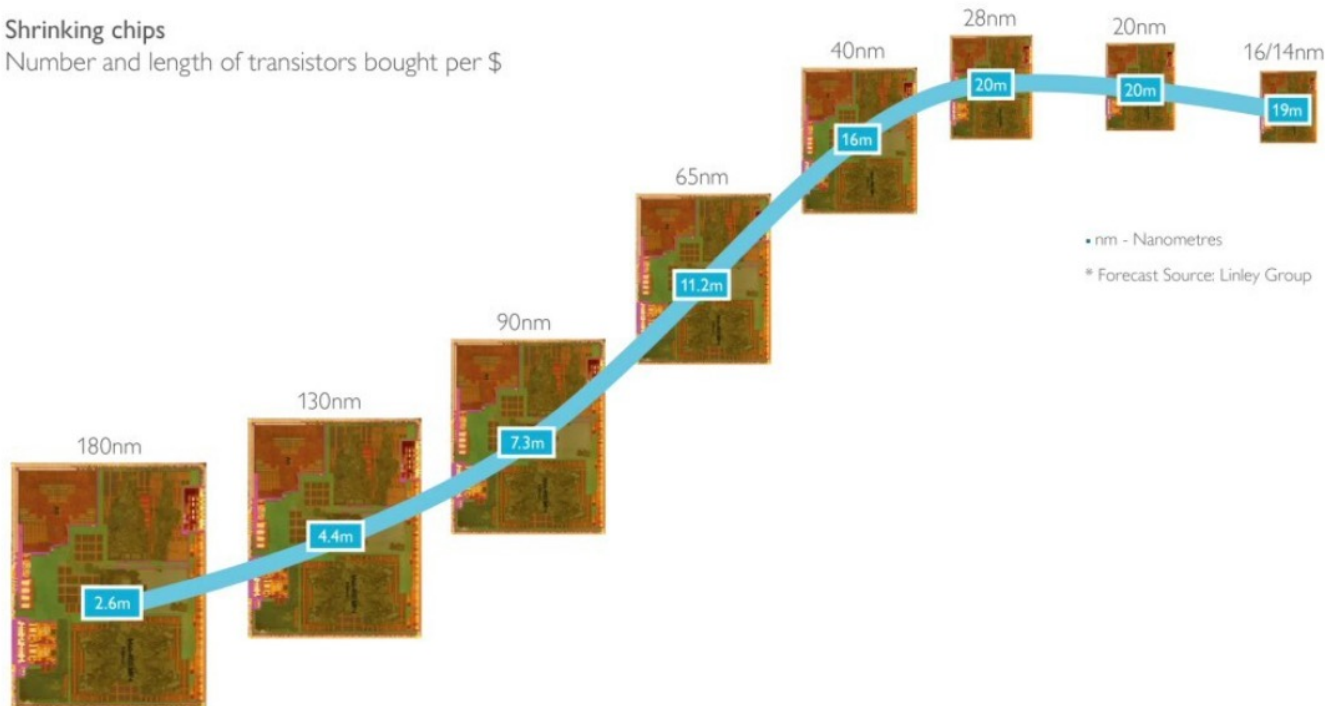
  x 4-5 GATE DENSITY INCREASE

  > x2 FASTER

  ➢ x50 LEAKAGE INCREASE – CAN BE REDUCED EXPLOITING MULTI-VT and MULTI-GL DESIGNS

Moore's Law has stopped at 28nm ?

28nm: Optimal Balance of Cost and Power for 2015 Devices

Shrinking chips
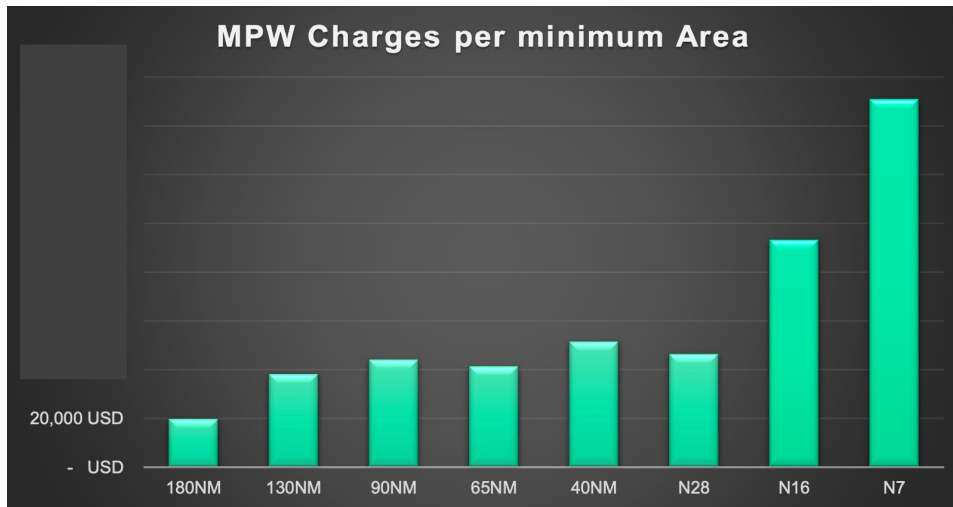Number and length of transistors bought per $

180nm — 2.6m
130nm — 4.4m
90nm — 7.3m
65nm — 11.2m
40nm — 16m
28nm — 20m
20nm — 20m
16/14nm — 19m

• nm - Nanometres
* Forecast Source: Linley Group

- 28nm offers the most transistors per $
- The last[1] planar bulk CMOS node

[1]almost; 22nm, 20nm "shrink" nodes

Cost comparison
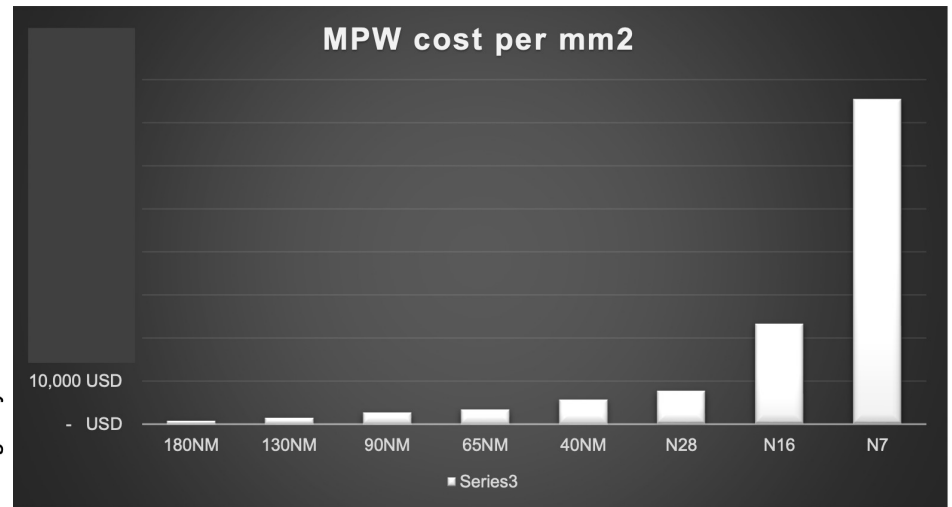
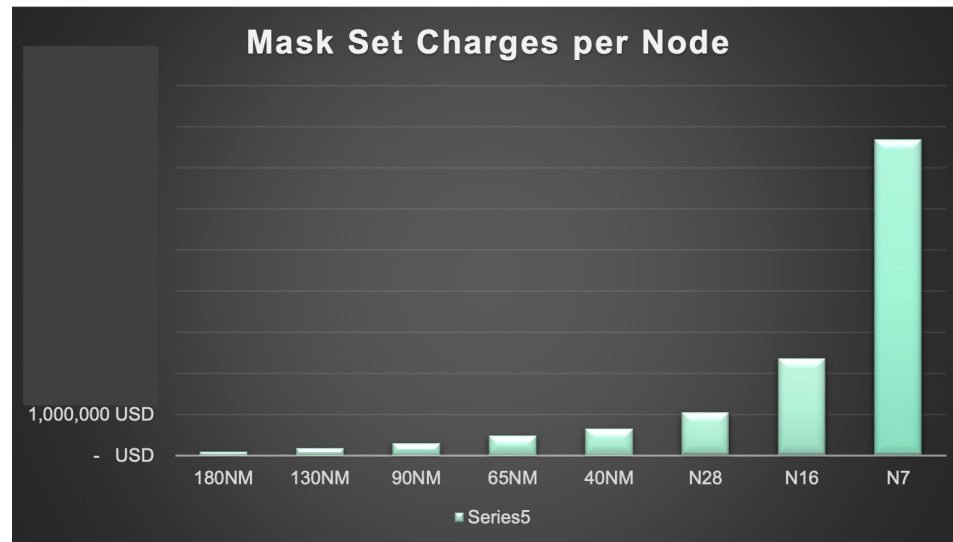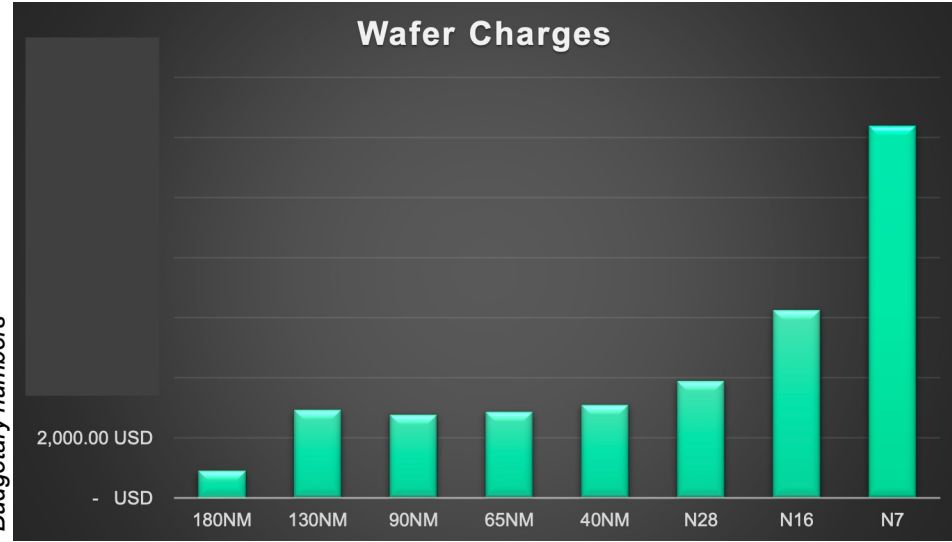

Source: Europractice presentation at MUG session TWEPP2023

28 HPC+ technology options

- Multiple metal schemes and technology options available

- **Narrow down options in the common design platform to facilitate**
  - IP block exchange
  - Work on common projects
  - Organize MPWs for sharing prototyping costs

28nm Common Design Platform

PDK: mmWave HPC+

Vt options: lvt, svt, hvt, uhvt, ehvt/SRAM_LL

Metal scheme: 1P9M_5X1Z1U + UTRDL

Europractice support

CERN ASIC support Team
Alessandro Caratelli
Marco Andorno
Kostas Kloukinas

28nm CMOS HPC+ Logic, RF

TSMC 28NM CMOS RF HIGH PERFORMANCE COMPACT MOBILE COMPUTING PLUS 0.9/1.8V

Technology characteristics	
	Shrink technology: YES
	Core voltage: 0.9V
	I/O voltage: 1.8V
	Shallow Trench Isolation (STI)
	Wells: Retrograde twin well for low well sheet resistance and better latch-up behavior.
	Triple well, Deep N-Well in option
	Dual Gate Oxide
	Vt options: ulvt, lvt, svt, hvt, uhvt, ehvt
	5V HVMOS
	HighRes resistors
	Temperature range: -40C to 125C
	# of metals: 5 to 10 Cu + ALRDL
	Interconnect dielectric: ELK
	Top metal: 1.9KA, 8.5KA, 11.5KA, 35KA
	CMP on STI, contact, via and passivation
	MoM capacitor
	Passivation: dual layers
Options that need special attention	SRAM Cell
	Vt's: maximum of 4 VT types in one design.

Metals Schemes

28 HPC	8M	/	1p8m_5x1z1u_ut-alrdl
28 HPC+ (use MMWAVE PDK)	7M	1p7m_4x1y1z_alrdl	/
	8M	1p8m_5x2r_alrdl	1p8m_5x1z1u_ut-alrdl
		1p8m_5x2r_ut-alrdl	
	9M	/	1p9m_5x1y1z1u_ut-alrdl

https://europractice-ic.com/mpw-prototyping/asics/tsmc/

Digital std. cell Libraries

- **Digital std. cells**
  - Foundry libraries
  - 120 different sets
  - Optimized implementation for Performance and Power
  - Front-end & Back-end views (layouts & netlists) are made available

- **CERN study**
  - Select the best sets and/or exclude cells to optimize Radiation Tolerance, Performance and Power
  - Integrate libraries in the Common Design Platform

Digital Standard Cell Libraries

tcbn28hpcbwp35p140

30 nm
35 nm
40 nm

Faster ↑
Less Power ↓

Gate length

HPC+ 12T	Raw Gate Density Kgates/mm2	Speed GHz	Active Power nW/MHz	Static Power nW/MHz
30nm	2,971	1	1	1
35nm	2,971	0.9	0.992	0.446
40nm	2,971	0.806	1.003	0.232
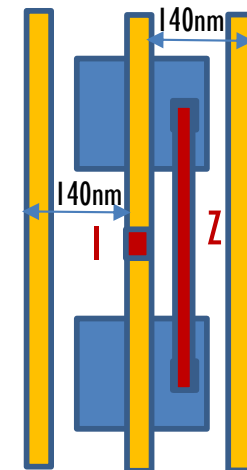
7, 9, 12

HPC+ only

Tracks

HPC+ 30P	Raw Gate Density Kgates/mm2	Speed GHz	Active Power nW/MHz	Static Power nW/MHz
7T	4,289	0.742	0.601	0.485
9T	3,961	0.886	0.781	0.714
12T	2,971	1	1	1

SVT, LVT, HVT, UHVT, ULVHT

Voltage threshold

HPC+ 12T 30P	Raw Gate Density Kgates/mm2	Speed GHz	Active Power nW/MHz	Static Power nW/MHz
LVT	2,971	1.351	1.235	5.305
SVT	2,971	1	1	1
HVT	2,971	0.654	0.911	0.127
EHVT	2,971	0.229	0.903	0.019

Poly pitch

140nm

140nm

I   Z

Common Design Platform

- 28nm Common Design Platform:
    - Support collaborative work of distributed design teams
    - Minimize efforts to integrate a "design environment"
    - Avoid incompatibilities

- Incorporates:
    - **Mixed-Signal Design kit**
    - **Scripted Design Flows** that are standardized and validated using <u>selected EDA software tools</u>
    - **Maintenance**
    - **Technical Support**
    - **Training**

    Europractice versions

- Developed by
    - **CERN ASIC Support Team** in collaboration with Cadence VCAD Design Services
        - https://asicsupport.web.cern.ch

Foundry PDK → Mixed signal kit ← Foundry Digital Libraries

Workflows → Common Design Platform ← Mixed signal kit
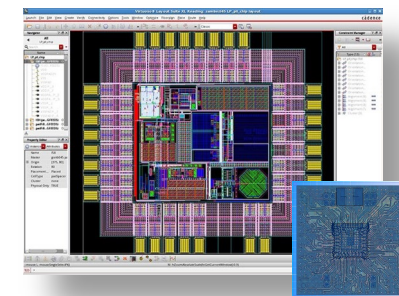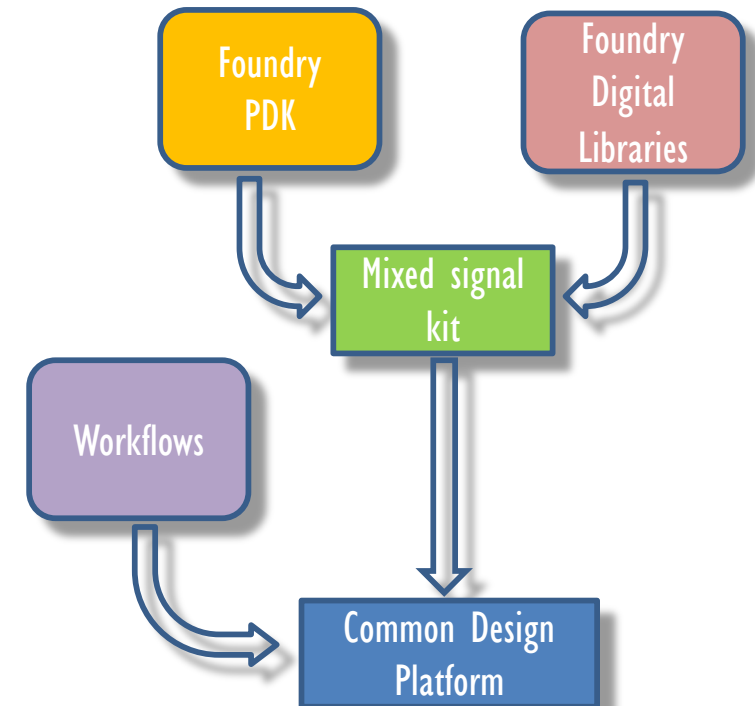
Radiation Evaluation test chips

TID CHIP LAYOUT
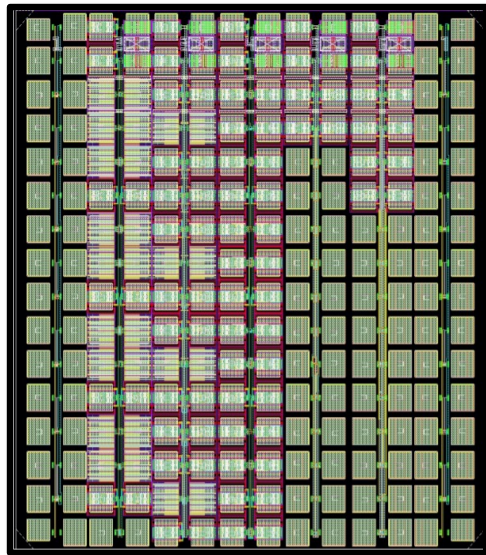
SINGLE TRANSISTORS ARRAY
7x probing arrays
Different transistor flavors
Variability arrays
Design submitted in June 2021

EXP28 CHIP SUITE
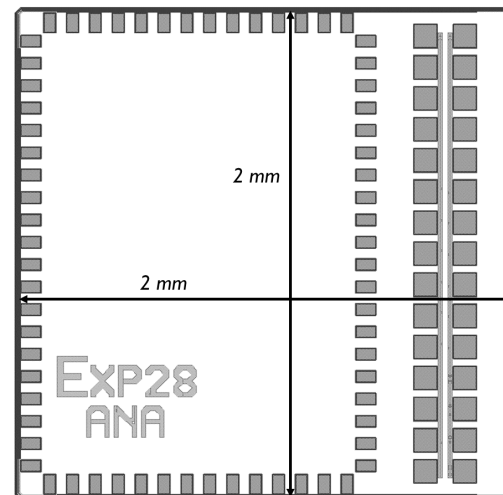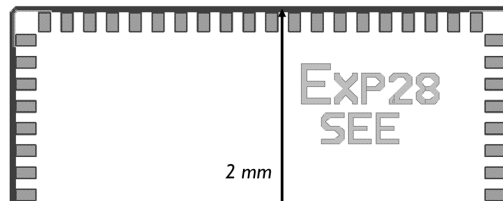
TOTAL IONIZING DOSE (TID) STUDIES:
- Ring Oscillator for standard cells
- Built-In-Self-Test for SRAM memories

SINGLE EVENT EFFECT (SEE) STUDIES:
- Vernier Delay line for SET studies
- Flip-Flop matrixes for SEU studies
- Functional SRAM test for SEE on memories

IP BLOCKS CHARACHTERIZATION
- Bandgap and Temperature sensor
- Digital-to- Analog Converted (DAC)
- Probe array for HV devices and resistors

slide by Giulio Borghello

Radiation Hardness of Modern CMOS Technologies to Ultra-High TID

28nm has a very interesting response at ultra-high TID!!

I_{ON}: maximum drain current

Kostas.Kloukinas@cern.ch   12

28nm TID performance

library standard cells
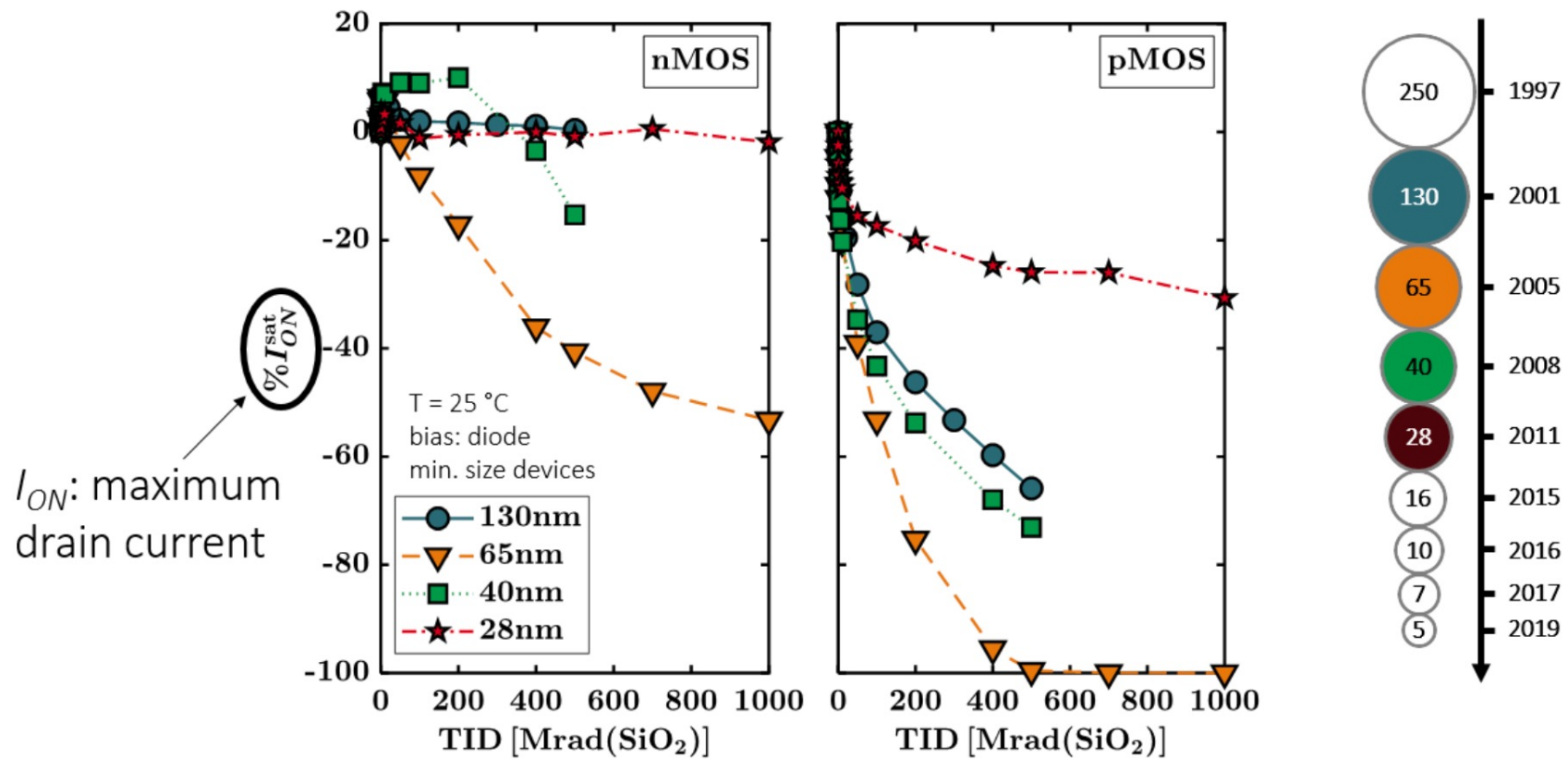
Power consumption vs TID for different std. cell libraries in Ring Oscillators
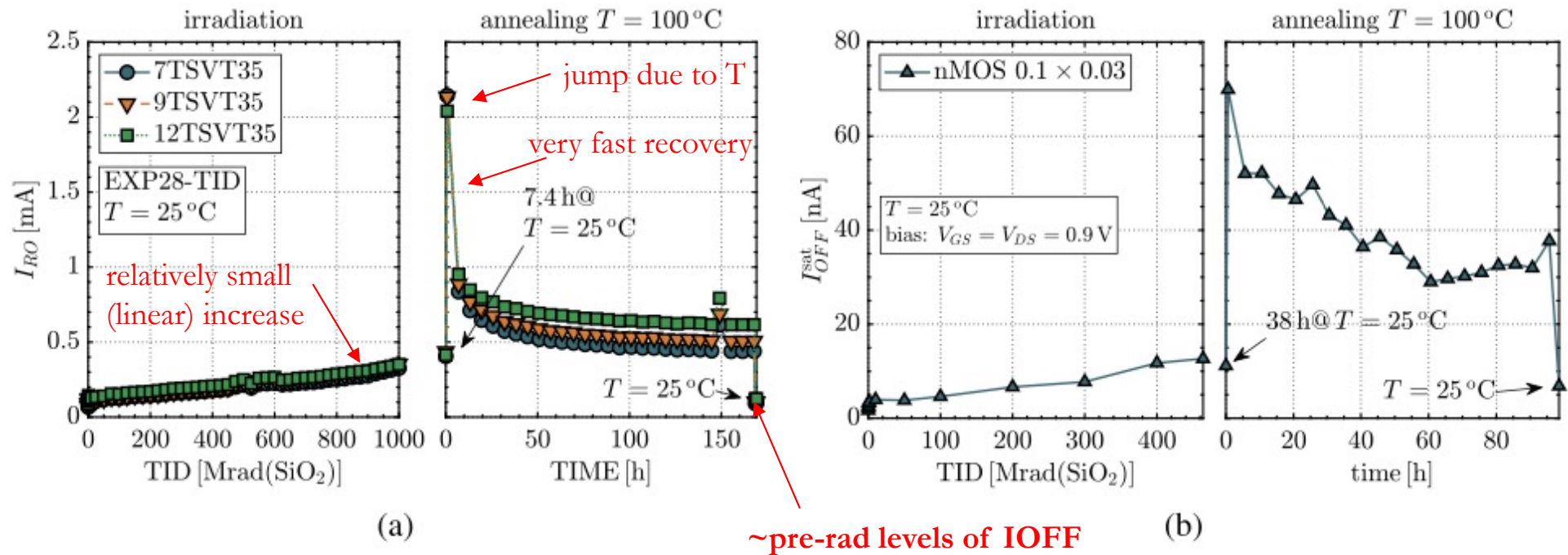
Figure 3. Current consumption during irradiation and HTA for ROs (a) and single nMOS (b).

https://iopscience.iop.org/article/10.1088/1748-0221/18/02/C02003/pdf

Kostas.Kloukinas@cern.ch

TID: 28nm vs 65nm

library standard cells

Ring Oscilators

16 cells x23 libraries = **368** ROs

28nm

28nm shows lower degradation than 65nm technology

65nm

DRAD chip, 65nm tech.
https://cds.cern.ch/record/2725573/files/DRAD%20report.pdf
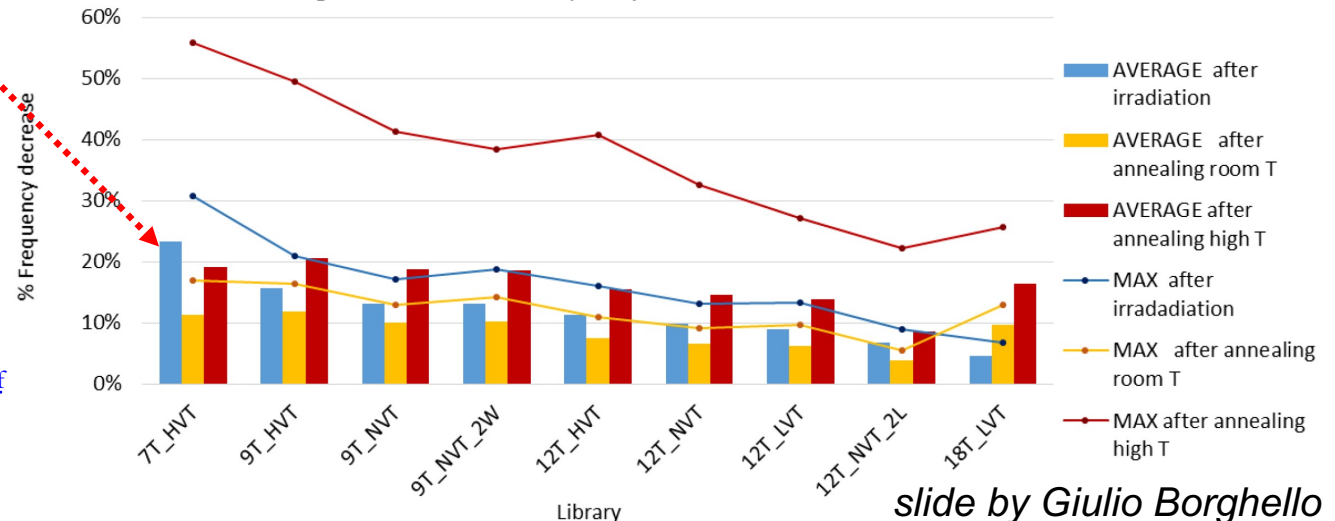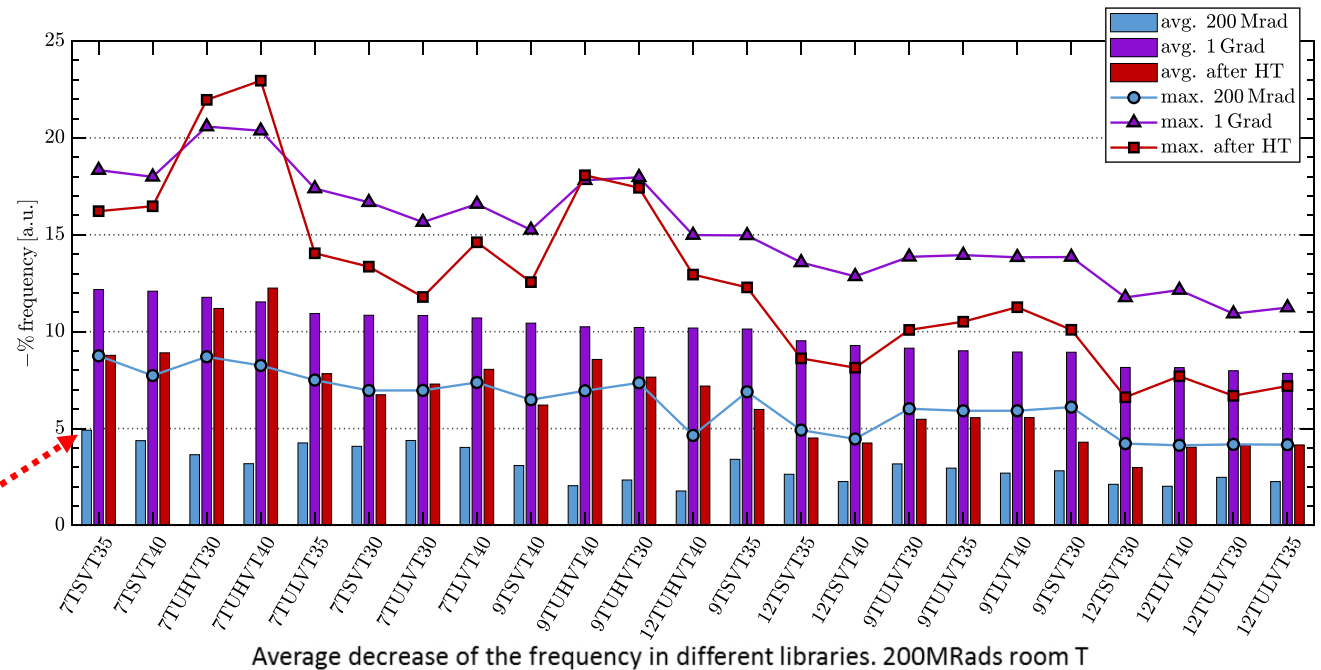
Borghello, G., et al. "Total ionizing dose effects on ring-oscillators and SRAMs in a commercial 28 nm CMOS technology." *Journal of Instrumentation* 18.02 (2023)

Average decrease of the frequency in different libraries. 200MRads room T

slide by Giulio Borghello

TID tests on foundry SRAMs

Testing procedure: BIST logic kept fixed at 0.9V, frequency and voltage scan for SRAMs.
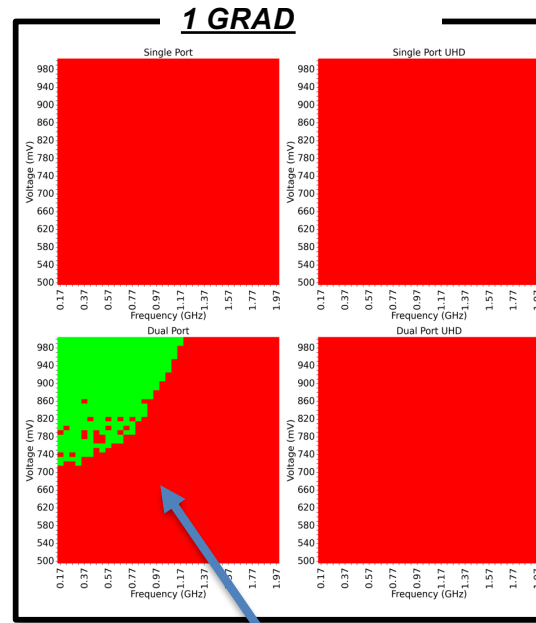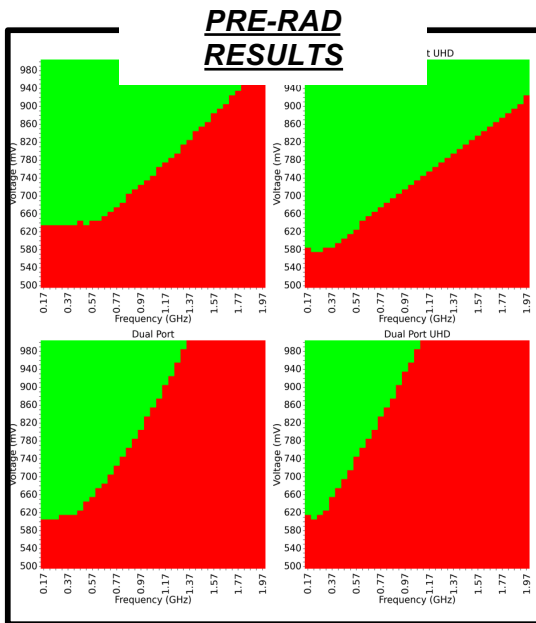
Dual-Port foundry SRAM survived (almost) up to 1Grad
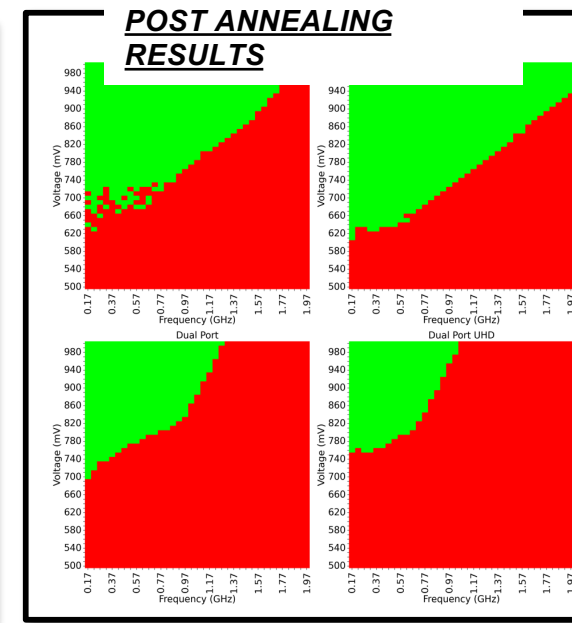
All SRAMs fully recover after annealing

Heavy Ion test run in UCL Louvain
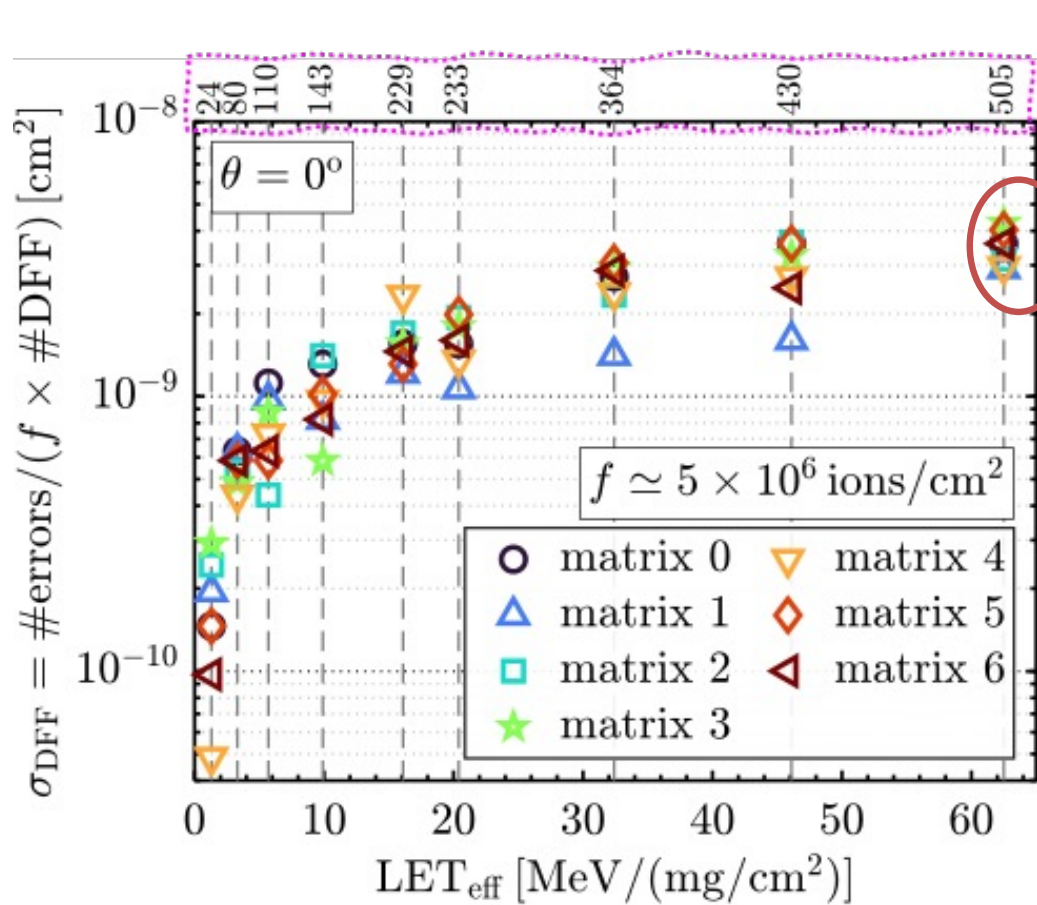
total number of errors

Similar SEE sensitivity for all D-FF types

cross-section σ_{DFF} [cm^2] = (#errors/#DFF in matrix)/fluence

$\theta = 0°$

$f \simeq 5 \times 10^6$ ions/cm^2

○	matrix 0	▽	matrix 4
△	matrix 1	◇	matrix 5
□	matrix 2	◁	matrix 6
★	matrix 3		

7 different matrixes with D-FF

0	$D_{FF}D1$	(D Flip-Flop with Sync Clear)
1	$D_{FF}D1+C_{KB}D1$	(D Flip-Flop with Sync Clear + buffer in the D-Q path)
2	$D_{FF}D4$	(D Flip-Flop with D4 driving strength)
3	$D_{FF}D1LVT$	(Low-Vt)
4	$D_{FF}D1UHVT$.	(High-Vt)
5	$D_{FF}D1ULVT$	(UltraLow-Vt)
6	$D_{FF}D1$	(~5.5 µm spacing between DFF)

slide by Giulio Borghello

16

much larger statistics than DFF
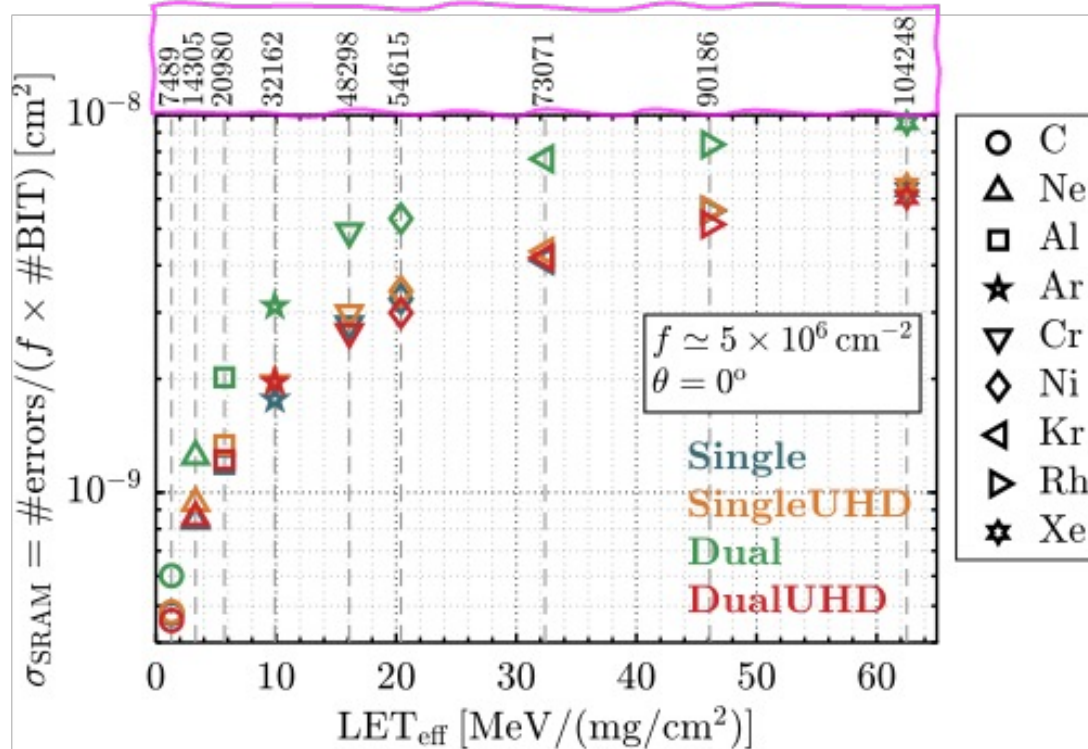
Dual SRAM has a slightly higher cross-section

larger cells in dual SRAM -> larger sensitive area

BITCELL transistor dimensions

SINGLE PORT (L,W,M) 6T	nchpd_sr	nchpg_sr	pchpu_sr
S1BHVTSWBASO100W10_BCELL_SD	35 95 1	35 65 1	35 40 1
S1BHVTSWBASO100W10_TKBL_BCELL_SD	35 95 1	35 65 1	35 40 1
S1BHVTSWBASO100W10_TKBL_EDGE_SD	35 95 1	35 65 1	35 40 1
DUAL PORT (L,W,M) 8T	pchpu_dpsr (2)	nchpd_dpsr[4]	nchpg_dpsr (4)
SDMWBASO100W10_MCB	35 50 1	35 195 1	35 140 1
SDMWBASO100W10_TKBL	35 50 1	35 195 1	35 140 1
SDMWBASO100W10_TKNOR	35 50 1	35 195 1	35 140 1
ULTRA HIGH DENSITY SINGLE PORT (L,W,M) 6T	nchpd_sr	nchpg_sr	pchpu_sr
S1BUHDHVTSWBSO100W10_TKBL_BCELL	35 95 1	35 65 1	35 40 1
S1BUHDHVTSWBSO100W10_MCB	35 95 1	35 65 1	35 40 1
S1BUHDHVTSWBSO100W10_TKBL_EDGE	35 95 1	35 65 1	35 40 1
ULTRA HIGH DENSITY DUAL PORT (L,W,M) 6T	nchpd_sr	nchpg_sr	pchpu_sr
SD8MWA100W10_TKBL_EDGE	35 95 1	35 65 1	35 40 1
SD8MWA100W10_TKBL_BCELL	35 95 1	35 65 1	35 40 1
SD8MWA100W10_MCB_TKWL_ISO	35 95 1	35 65 1	35 40 1
SD8MWA100W10_MCB_TKWL	35 95 1	35 65 1	35 40 1
SD8MWA100W10_MCB	35 95 1	35 65 1	35 40 1

slide by Giulio Borghello

7 matrices with D-flip/flops

2.38 μm

0.9 μm — DFF

5.432 μm

DFF ←—— 5.32 μm ——→ DFF
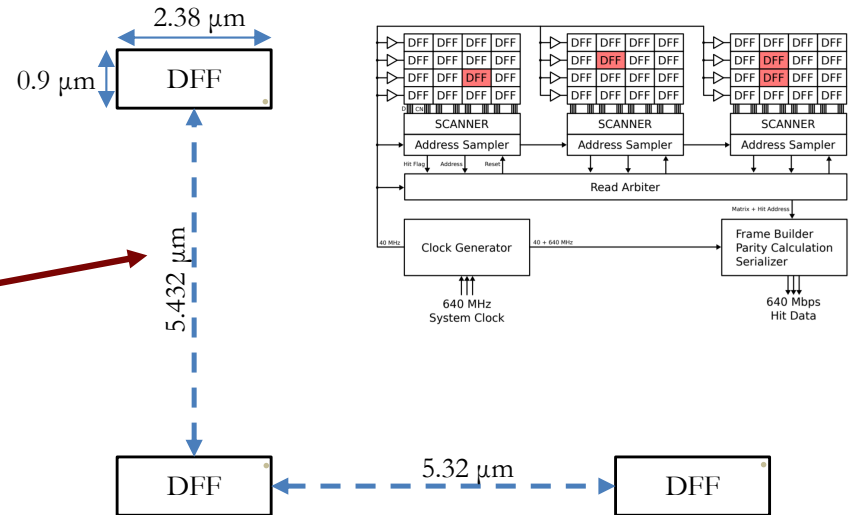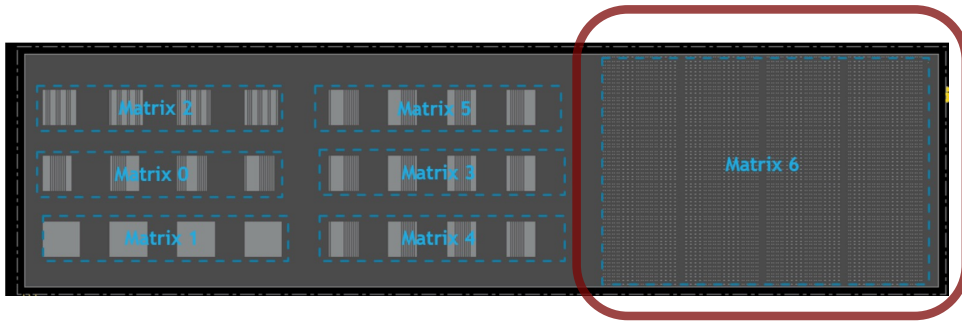
heavy ions

protons
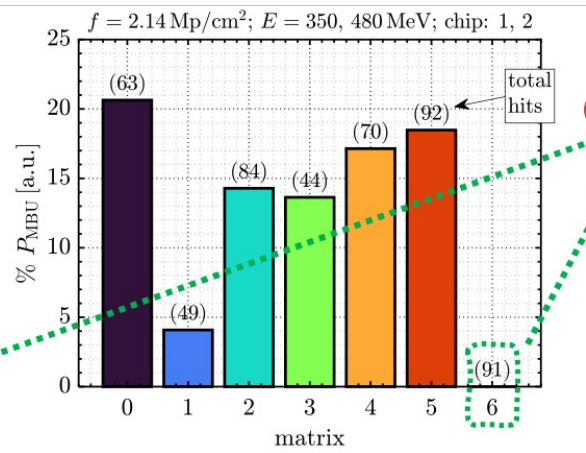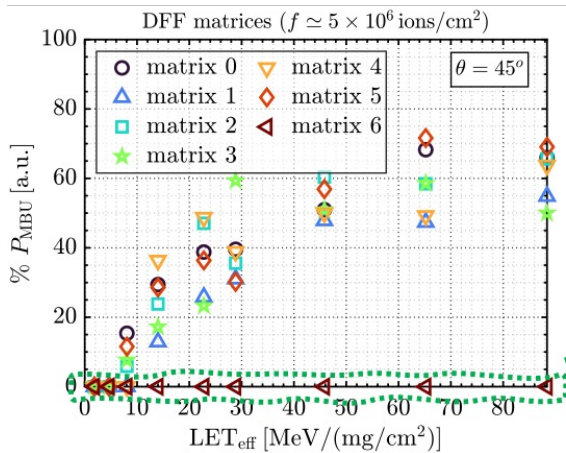
no MBU in matrix 6!

~6 μm spacing between DFFs drastically reduces probability of MBU!

- key information for triplication strategy!

- ~2.5 times less than the 15 μm typically used in 65nm technology!
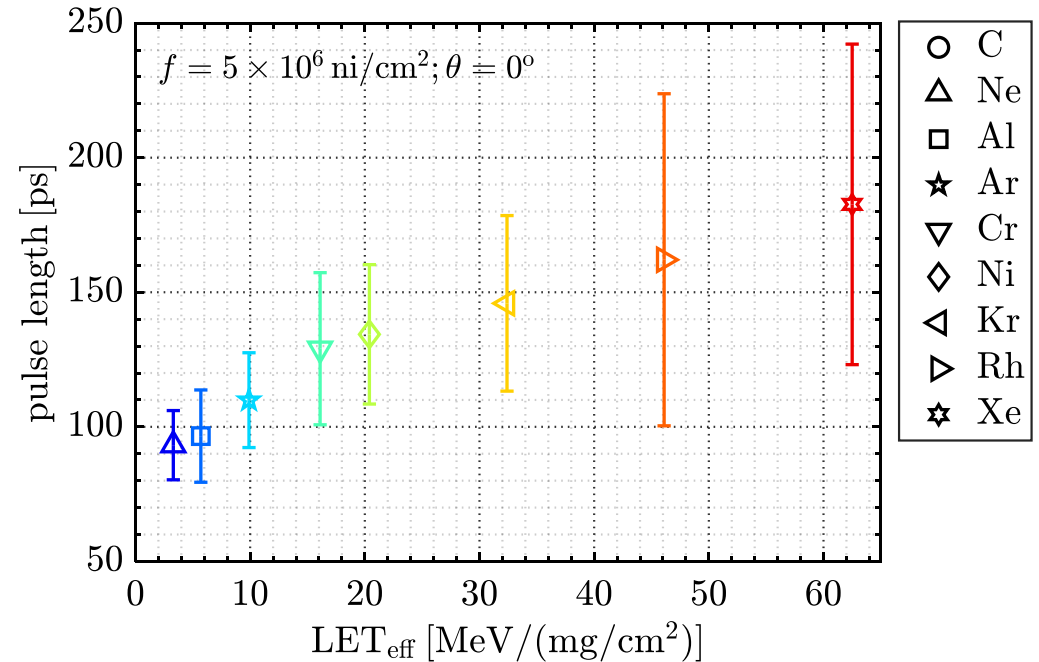
slide by Giulio Borghello

SET pulse length deduction

Important parameter for implementing Temporal Redundancy fault tolerant schemes
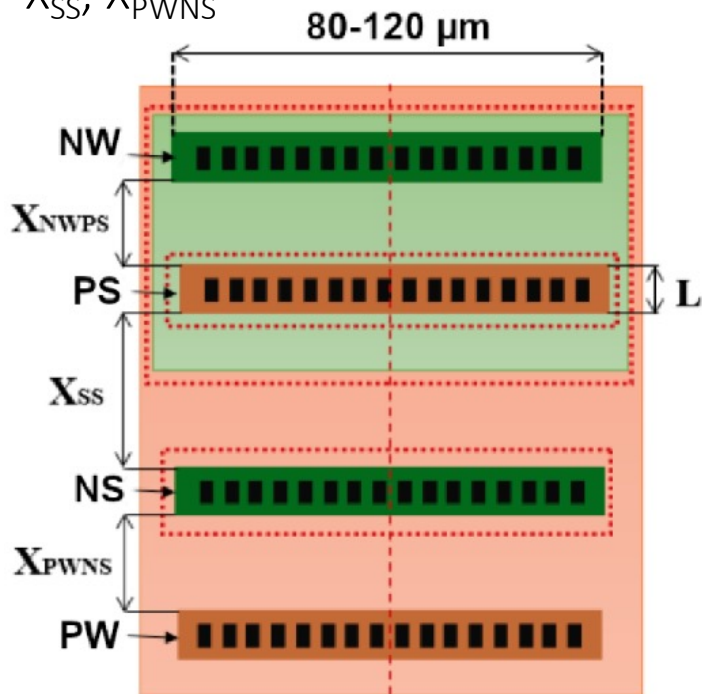

heavy ions
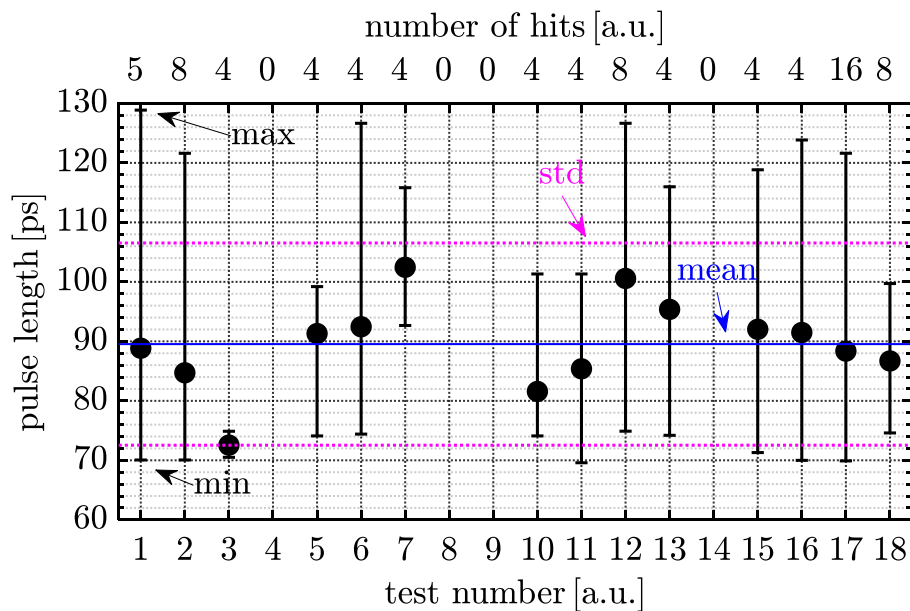
protons

Latch-up immunity tests

Latch-up sensitivity depends on doping levels(which cannot be changed) and distance between wells

40 structures with different X_{NWPS}, X_{SS}, X_{PWNS}

ion	angle [°]	LET [MeV/(mg/cm²)]	fluence [10^6 ni/cm²]	voltage
Ni	0	20.4	23.3	VDD (0.9 V)
Ni	45	28.85	16.2	VDD
Kr	45	45.82	11.4	VDD
Xe	0	62.5	51.6	VDD
Rh	45	65.2	11.4	VDD
Xe	45	88.39	6.2	VDD
Xe	45	88.39	45.0	1.15*VDD
Xe	75	241.48	1.72	1.15*VDD

high LET, high voltage

No SEL
in any of the structures
for any for the tests!!!

Giulio Borghello

Rad-Tol IP Block library

RADIATION TOLERANT ESD PROTECTIONS

- 👤 outsourced to SOFICS by the CERN ASIC Support
- 📅 Design completed. Submitted in Jan 2022 for radiation characterization.
- 🔗 https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

RADIATION TOLERANT CMOS IO PAD

- 👤 outsourced to SOFICS by the CERN ASIC Support
- 📅 In progress. Radiation characterization will follow.
- 🔗 https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

SRAM MEMORIES

- 👤 Compilers purchased from the Foundry by the CERN ASIC Support
- 🔗 We can distribute precompiled memory upon request
- 📅 Submitted in Jan 2022. Radiation characterization completed.
- 🔗 https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

EFUSES

- 👤 IP block purchased from the Foundry by the CERN ASIC Support
- 📅 Radiation characterization will follow.
- 🔗 https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

Rad-Tol IP Block library

BANDGAP VOLTAGE REFERENCE & TEMP MONITOR

- 👤 **G. Traversi** (Bergamo/Pavia) / INFN Falaphel project
- 📅 Design completed. Submitted in Jan 2022
- 🔗 https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

DIGITAL TO ANALOG CONVERTER (8-BIT)

- 👤 **Markus Piller** (DOCT, CERN EP-R&D WP5)
- 📅 Design completed. Submitted in Jan 2022
- 🔗 datasheet https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

DIFFERENTIAL LINE DRIVERS AND RECEIVERS

- 👤 **Franco Bandi** (CERN EP-R&D WP5)
- 📅 Design completed. Submitted in Jan 2022
- 🔗 https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

ANALOG PLL

- 👤 **Tobias Hofmann** (CERN EP-R&D WP5)
- 📅 In progress
- 🔗 https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

DCDC CONVERTER

- 👤 **Stefano Michelis** and **Giacomo. Ripamonti** (CERN EP-ESE)
- 📅 In progress
- 🔗 https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

RAIL TO RAIL OPERATIONAL AMPLIFIER

- 👤 **Jan Kaplon** (CERN EP-ESE)
- 📅 Design completed. To be submitted in Dec. 2022.
- 🔗 https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

ADC FOR MONITORING (12-BIT)

- 👤 **Tobias Hofmann** (CERN EP-R&D WP5)
- 📅 In progress
- 🔗 https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

RAIL TO RAIL OPERATIONAL AMPLIFIER

- 👤 **Markus Piller** (CERN, DOCT)
- 📅 In progress
- 🔗 https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

DIGITAL PLL

- 👤 **Markus Piller** (DOCT, CERN EP-R&D WP5)
- 📅 In progress
- 🔗 https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

LDO

- 👤 **Stefano Michelis** and **Giacomo Ripamonti** (CERN EP-ESE)
- 📅 In progress
- 🔗 https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

AMTest28 chip for common IPs

Test chip Submitted in August 2023

GOAL: Silicon-prove the IP blocks designed in 28nm, by functional and radiation testing

- Marco Andorno (ASIC Support) prepared a test chip that integrates several IP-blocks from CERN or form other institutes providing a single MPW run to test multiple blocks, and uniform testing requirements

- The analog and mixed-signal blocks were assembled Digital-on-Top, along with a control and configuration interface (triplicated):

IP-Block	Designer
SLVS Transmitter and Receiver	Franco Bandi (CERN)
Digital PLL	Vladimir Gromov (Nikhef)
Rail-to-rail analog buffer	Jan Kaplon (CERN)
Analog frontend	Markus Piller (TU Gratz)
Bandgap reference (4 different versions)	Grzegorz Wegrzyn, Stefano Michelis (CERN)
TIMO28 (TID response variation IP block)	Giulio Borghello (CERN)
8-bit DAC	Markus Piller (TU Gratz), Viros Sriskaran
12-bit Sigma-Delta DAC	Can Akgun (Nikhef)
Test structures (4 types)	SOFICS
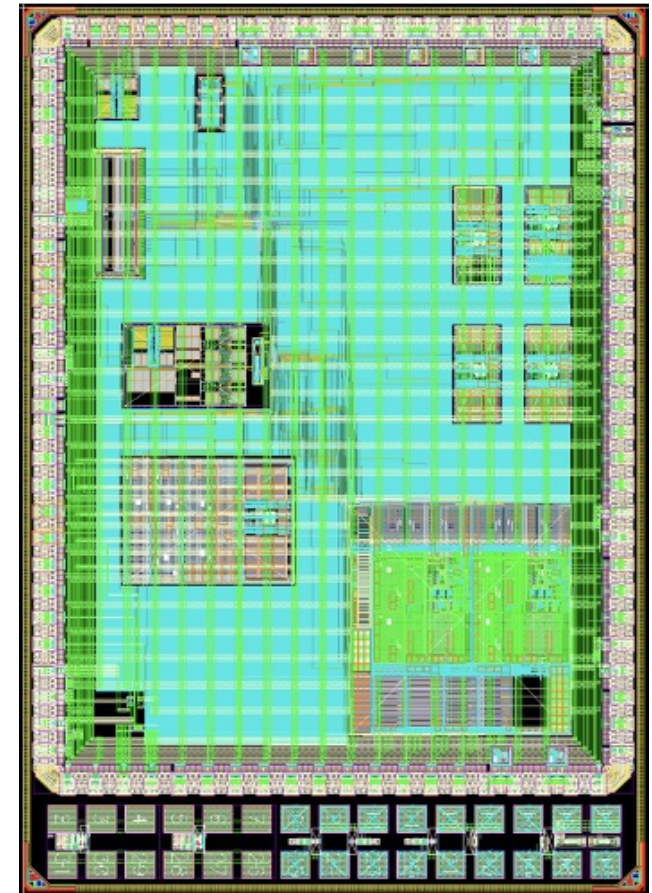
IP block Library

CERN ASIC Support is taking care of:

- Packaging in a uniform way the IP blocks

- Maintenance of the shared repositories (Cliosoft) and institutes access and provide access upon request

The ownership of the IP block remains with the designer. The platform allow to advertise and share the IP blocks with the community.

List of available IP blocks and datasheets:

F2 28:	https://asic-support-28.web.cern.ch/ip-blocks/
F2 65:	https://asic-support-65.web.cern.ch/docs2/
F2 130:	https://asic-support-130.web.cern.ch/docs2/
F1 130:	https://espace.cern.ch/asics-support/gf130/

All institutes that wish to contribute are invited to participate to common repositories with analog and digital IP blocks, shared within the community! Get in touch!

System-on-Chip design approach

Future detector upgrades will require more complex ASICs

They require advanced technology nodes, that come with high development costs in terms of design time, verification and costs
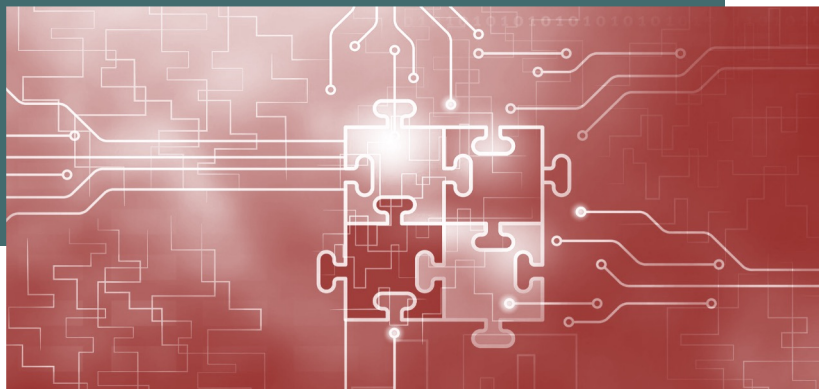
An abstract design methodology, focused on programmability and reusability will allow to:

- Develop reusable IP blocks

- Standardize interconnects for IP blocks

- Replace state machines with a control processor (RISC-V based)

- Programmable, flexible logic blocks (SoC Ecosystem, cores, eFPGA, NoCs)

- Enhance Hierarchical Digital Implementation and Verifications

- Use of Open Source scripts and tools
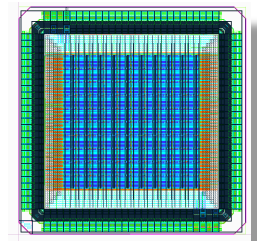
250nm RT-FPGA

(past successful project: [Development of SEU-robust, radiation tolerant and industry compatible programmable logic components](#)

SoC Generator Tool in development

 Hardware generation   Software generation

SoCMake

DOC: https://socmake.docs.cern.ch

GIT: https://gitlab.cern.ch/socmake
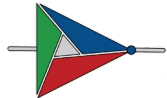
- Open-source SoC generator tool

- From a single SystemRDL description file, automatize the generation of:
  - Hardware design
  - Software toolchain
  - Verification platform
  - Documentation

- Generate custom SoCs

- Rapid SoC prototyping
  - Quickly build different architectures with different IP blocks, hardware accelerators and different CPUs

- Design team: R. Pejasinovic, M. Andorno, A. Caratelli, A. Nookala, K. Kloukinas

Diagram

Inputs:
- *.sv
- *.cpp
- *.rdl

RDL toolchain outputs:
- IP blocks and hardware accelerators (*.sv)
- Software application
- Top level HDL (*.v)
- Register file and Interconnections (*.v)
- Hardware abstraction layer (*.cpp)
- Linker scripts generation
- UVM testbench (SystemC) and SEE injection utilities
- Config files for synthesis and impl (* .yaml)
- Documentation - website (*.html *.pdf *.md)

Stages:
- SIMULATE
  - Verilator
  - Xcelium
  - VCS
- IMPLEMENT
  - Cadence
  - ...
- FPGA EMULATE
  - Vivado
- Software application
  - GCC

Work in progress

SoC platform in development

SoC platform components

CPU Core	Memory Subsystem	Digital and analog IPs	Hardware accelerators	Interconnect bus

RISC-V
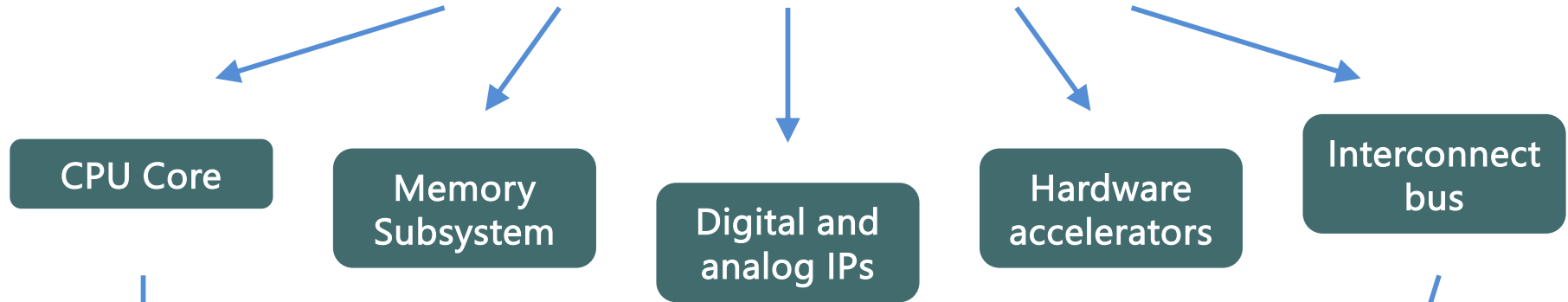
For the moment 4 popular cores supported:

- LowRISC Ibex
- ChipsAlliance (WD) EL2
- Syntacore SCR1
- Picorv32

Support for multiple interconnect busses

- APB4 → APB-RT
- AXI4-Full → **AXI-RT**
- Axi4-Lite → **AXI-Lite-RT**
- NMI, OBI

Radiation tolerant version:
Triplicated control signals
Encoded data and address lines

Work in progress

Collaborative Framework

- ## NDAs
  - Special 3-way NDA (institute-IMEC-Foundry) that permit collaborative work
    - <u>Permit the exchange of designs and technical data among collaborators</u>
    - CERN and 45 institutes have signed the 3-way NDA

- ## Commercial frame contract
  - CERN has a frame contract that allows small-scale prototyping (MPWs)
  - It will be extended to cover full-maskset engineering and production works
  - The <u>frame contract is accessible by HEP Institutes and Universities, via CERN</u>

ASIC Support website

https://asicsupport.web.cern.ch

Alessandro Caratelli, Marco Andorno, Kostas Kloukinas

Hitchhicker's guide to 28nm

- **28nm Designer's Guide**
  - Technology Overview
  - Design Guidelines
  - Reliabilty
  - Tutorials

- **Available at**
  - https://asic-support-28.web.cern.ch/tech-docs/designers_guide/

TSMC28nm Designer's Guide and Technology Overview

Markus Piller
Franco Nahuel Bandi
Alessandro Caratelli
Marco Andorno
Stefano Michelis
Davide Ceresa
Rafael Ballabriga
Stefan Biereigel

Summary This document gives the minimum requirements for ASIC designs in TSMC 28nm technology and gives a technology overview. The specified requirements are a guide to building a common basis for IP blocks within the new technology. Additional requirements or adaptions may be defined within the project's proposal specification document.

Contents

1

Training courses

INFO AND SUBSCRIPTION: https://asicsupport.web.cern.ch/training_courses/workshop28nm

A total of **145** Designers from HEP institutes have attended these training workshops in the last 3 years

Digital-on-top hierarchical Implementation in workshop	System Verilog Advanced Verification Environment using UVM workshop	Workshop on Mixed-Signal design in 28nm process
DoT Workshop	**Verification / UVM**	**Designing in 28nm**

DoT Workshop

- Learn the main concepts for designing in 65nm for the High energy Physics environment

- Learn the main concepts of the digital implementation from the synthesis, physical implementation and signoff (RTL to GDS)

- Perform synthesis, physical implementation and signoff steps

- Exercise bottom-up and top-down hierarchical design approaches

- Co-developed between CERN EP-ESE ASIC Support service and Cadence VCAD

2020 TO 2022: **6 TRAINING SESSIONS**

Verification / UVM

- Learn the main concepts of functional verification for the High energy Physics

- Learn the main concepts of digital design verification

- Learn about the Universal Verification Methodology (UVM)

- In the lab sessions you will learn how to build your own UVC and verification environment

- A Cadence Training Course adapted for the High Energy Physics community requirements

SINCE 2020: **3 TRAINING SESSIONS**

NEXT SESSION TO BE SCHEDULED

Designing in 28nm

- Learn the main concepts for designing in 28nm for the High energy Physics environment

- Learn the main concepts of the analog and Mixed-Signal design in 28nm, and analog IP characterization

- Learn main concepts about TIDs and SEUs tolerance design

- Learn the main concepts of the digital implementation from the synthesis, physical implementation and signoff (RTL to GDS)

SINCE JAN 2023: **3 TRAINING SESSIONS**
NEXT SESSION END OF 2023

The "28nm Forum"

- ## Purpose of the 28nm Forum
  - CERN to communicate the EP R&D WP5 activities
  - Institutes to present their R&D activities and plans
  - Identify synergies
  - Establish collaborations

28nm Technology Forum Sessions

1st session (Nov. 12, 2020) https://indico.cern.ch/event/970389/
2nd session (Mar. 10, 2021) https://indico.cern.ch/event/1009040/
3rd session (July 28, 2021) https://indico.cern.ch/event/1042567/
4th session (Mar 23, 2022) https://indico.cern.ch/event/1132318/
5th session (Nov 3, 2022) https://indico.cern.ch/event/1207114/
6th session (Nov .., 2023) **focus on IP blocks**

- Restricted access; requires registration
- Self-inscribed CERN e-group:
  28nm-Forum@cern.ch

Summary

- A 28nm bulk CMOS technology has been fully characterized for operation up to 1GRad TID

- A Common Design Platform and a Collaborative Framework are implemented to facilitate design work in the HEP community
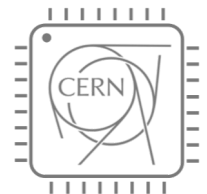
45
INSTITUTES HAVE SIGNED
THE 3-WAY NDA

14
PROTOTYPES on MPW runs
in 2022-23

- CERN EP R&D WP5 "IC Technologies" enabled the development ASIC support & Foundry Service facilitates long term access and support

Institutes wishing to join should contact CERN ASIC Support Service asic.support@cern.ch

Thank You

SOC Radiation Tolerant Ecosystem

Conceptual Diagram

Analog functions

ADC

DAC

Slow Control Interfaces

JTAG

GPIO

SPI

I²C

Interconnect

FE channel

FE analog blocks

eFPGA fabric

Programmable Logic

micro-code

SRAM

RISC-V

SRAM

data

e-Link

any-Link

High Speed Interfaces
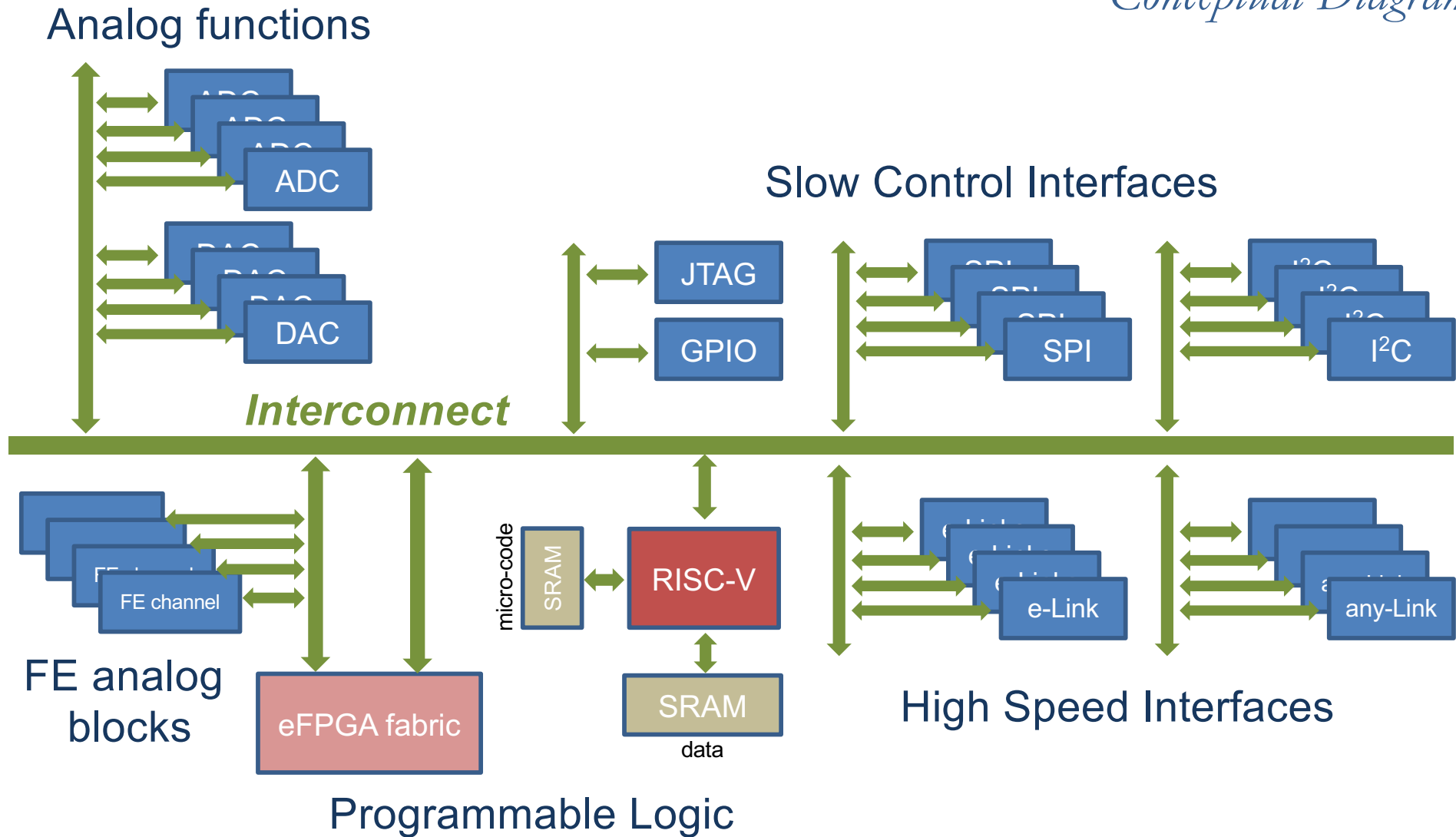
ASIC development costs
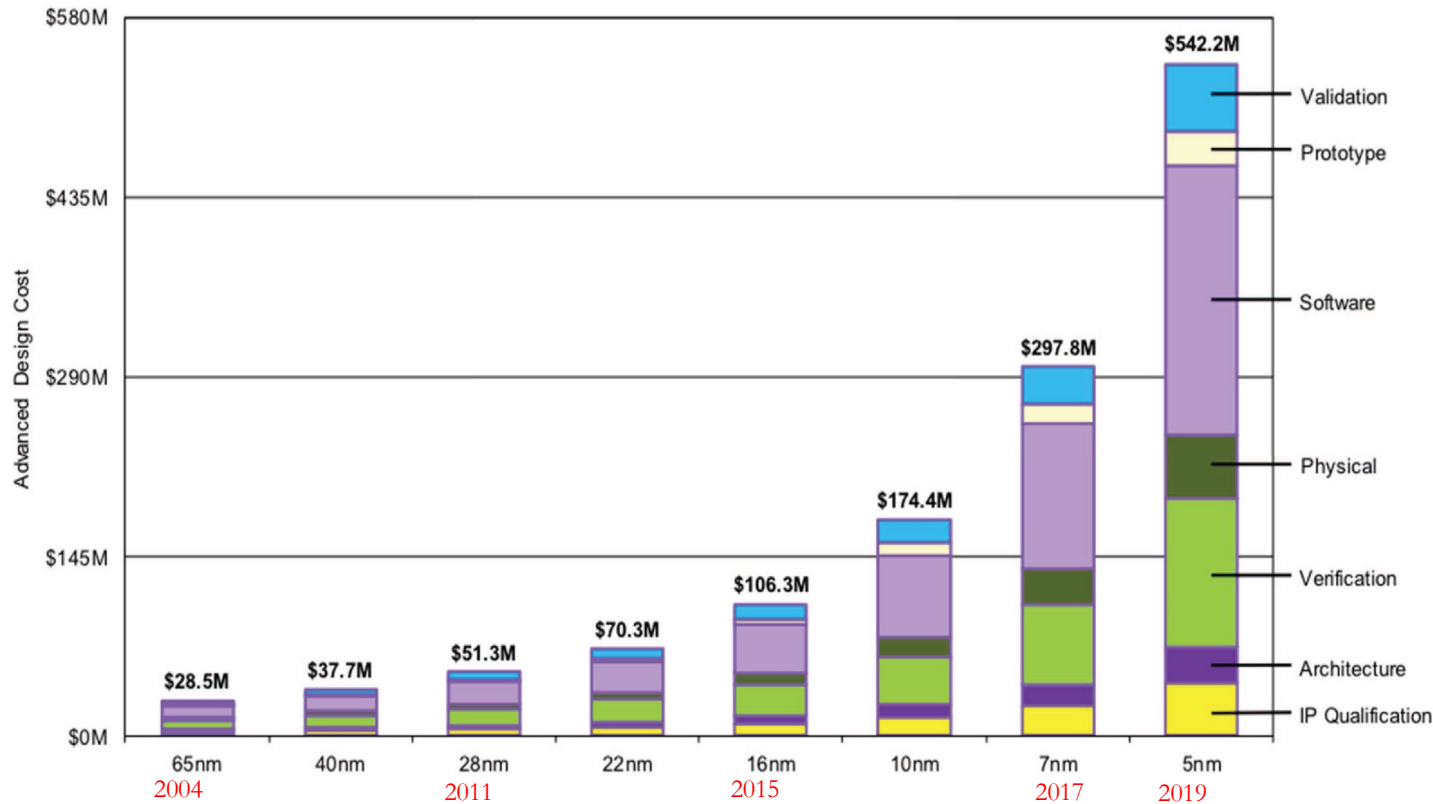
Chip Design and Manufacturing Cost under Different Process Nodes: Data Source from IBS*

- Escalating development costs when going Ultra Deep Submicron & Nanometer scale
- **At present the 28nm node is the optimum techno-economic choice (or limit ?)**

WP5.1 IC Technology Survey

- **<u>Three technologies were evaluated for TID radiation tolerance</u>**
    - 28nm bulk CMOS processes
        - Foundry A (one variant: Low Power)
        - Foundry B (two variants: High Performance, Low Power)
    - 22nm CMOS FD-SOI process
        - Foundry A

Prototyped & irradiated test chips
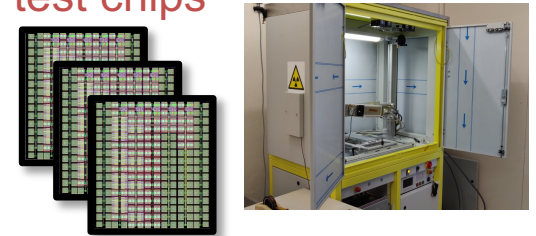
- Selected a <u>28nm bulk CMOS</u> technology as the next mainstream node for future Rad-Tol designs
    - Radiation Tolerance
    - Accessibility
    - Technical support   Europractice
    - Foundry IP blocks   Regular MPWs and mini@sics
    - Long Term availability   Mainstream Foundry
    - Cost