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# 28nm technology and ASIC design in HEP experiments

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**VERTEX 2023**

October 16-20 , 2023

Sestri Levante

*Kostas Kloukinas*

*CERN*



# Introduction

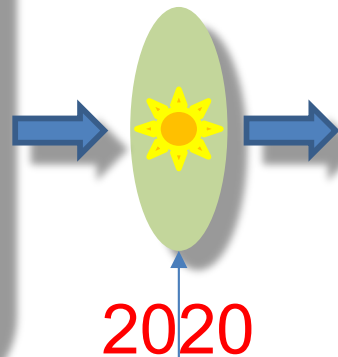
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- Why the 28nm node
- Technology Performance
- Common Design Platform
- Design Ecosystem

## Survey of CMOS technologies

### Selection Criteria

- Radiation Tolerance
- Accessibility
- Technical support
- Availability of IP blocks
- Long-term availability
- Cost



Technology  
Selection

### Design Platform

Mixed-Signal Design Kit,  
Reference Workflows, Rad-Tol techniques

### IP blocks

Rad-Tol IO pads, ESD structures, SRAMs  
Rad-Tol Volt. Ref, ADC, DAC, PLL, DLL

### SOC Platform

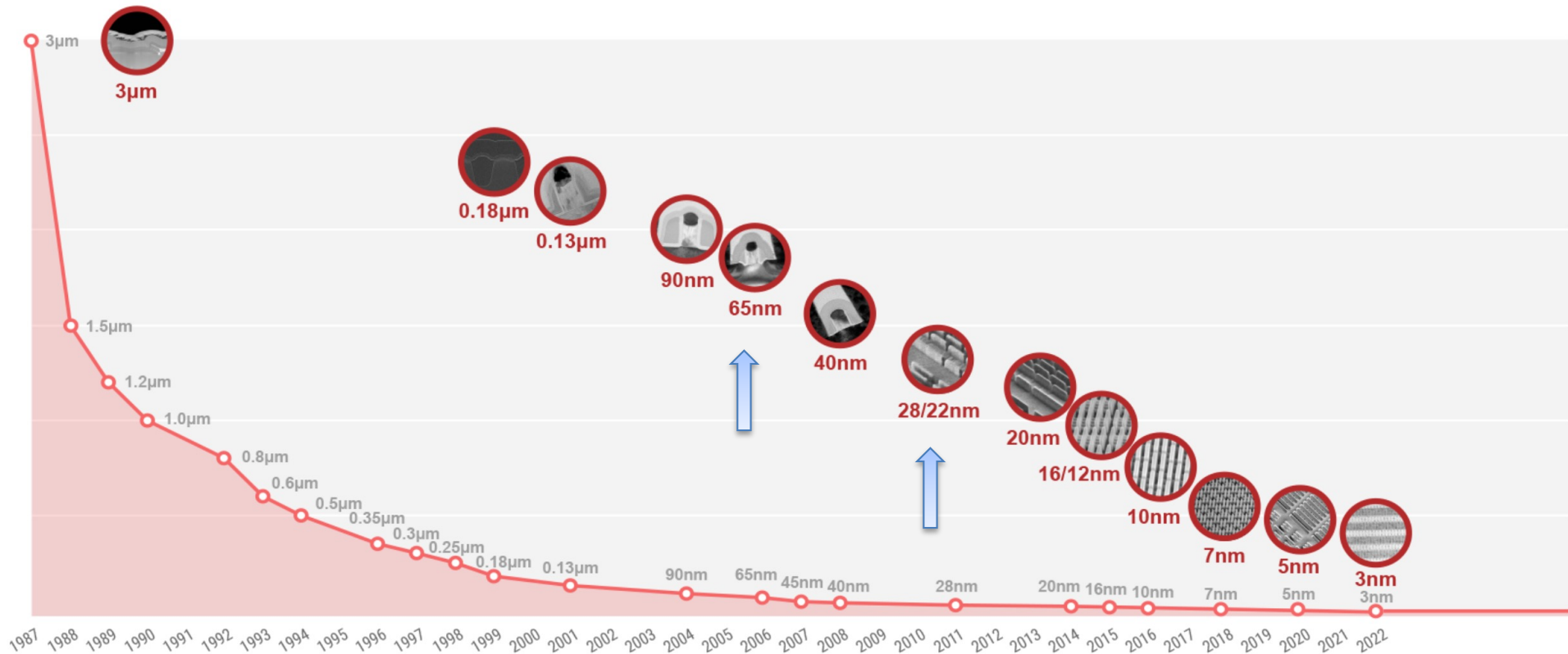
System-On-Chip design Enablers

### Collaborative Framework

NDA, Commercial contract,  
Support, Maintenance, Training



# The “position” of the 28nm node



## PERFORMANCE COMPARED TO 65 NM:

x 4-5 GATE DENSITY INCREASE

> x2 FASTER

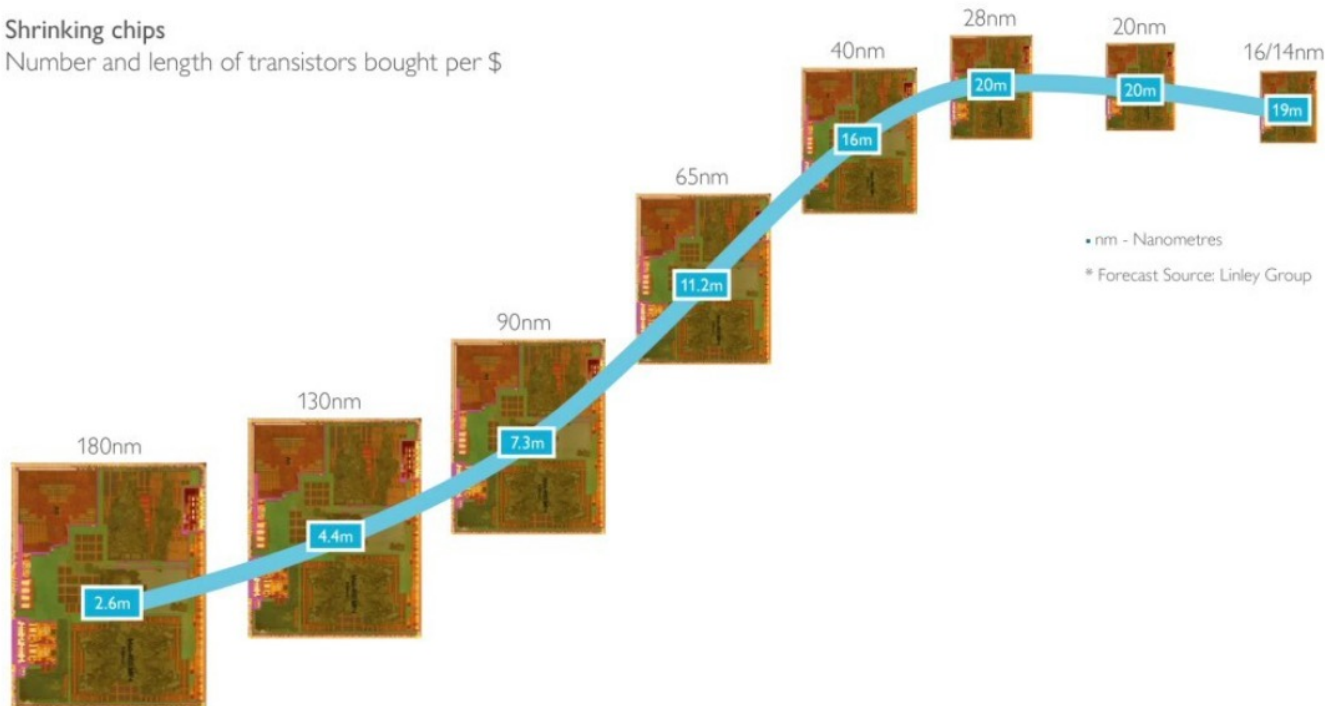
➤ x50 LEAKAGE INCREASE – CAN BE REDUCED EXPLOITING MULTI-VT and MULTI-GL DESIGNS

# Moore's Law has stopped at 28nm ?

## 28nm: Optimal Balance of Cost and Power for 2015 Devices

Shrinking chips

Number and length of transistors bought per \$

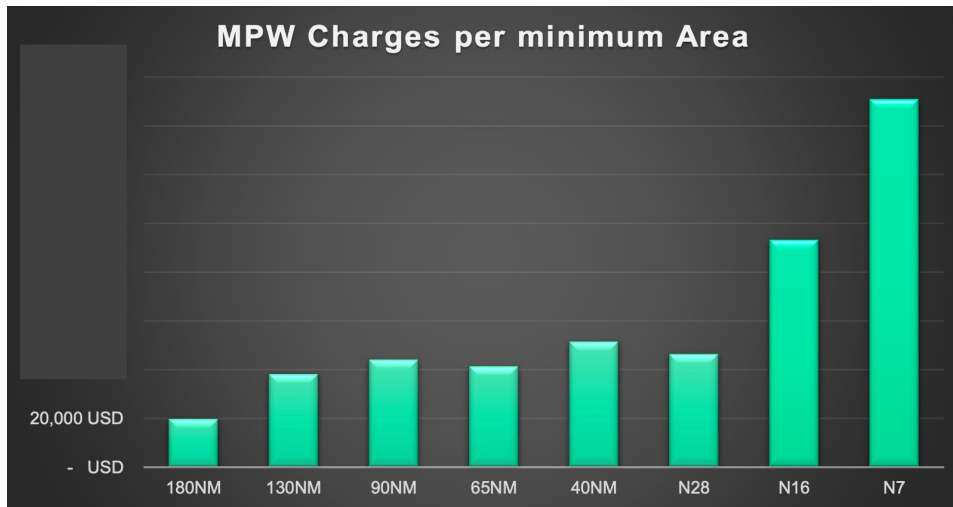


- 28nm offers the most transistors per \$
- The last<sup>1</sup> planar bulk CMOS node

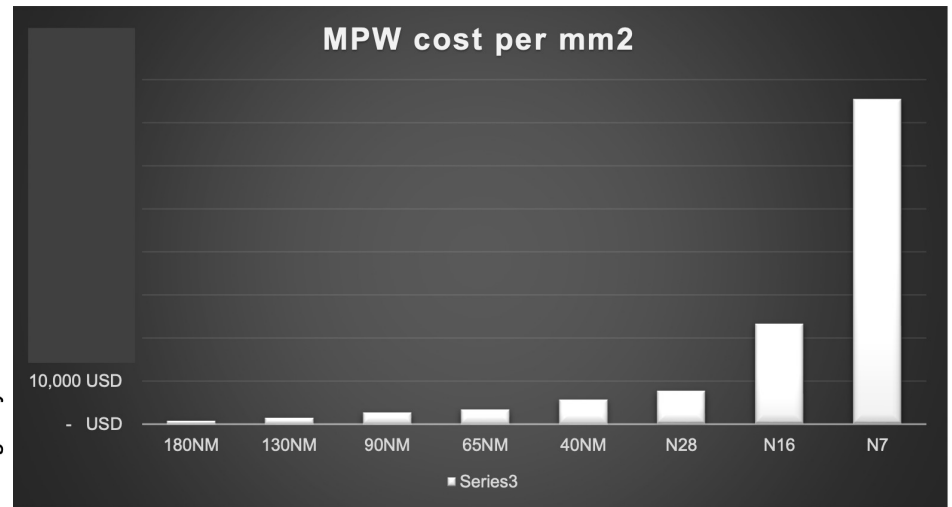
<sup>1</sup>almost; 22nm, 20nm "shrink" nodes



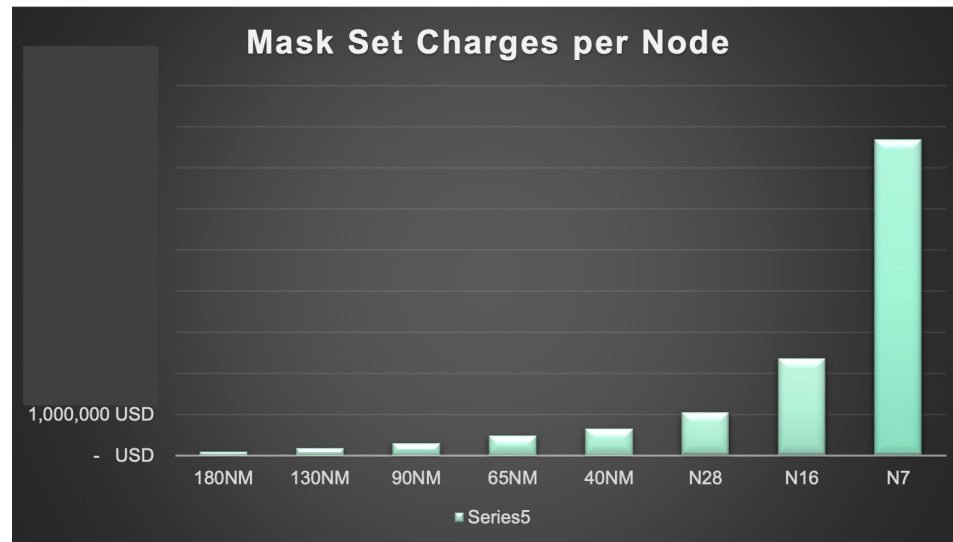
# Cost comparison



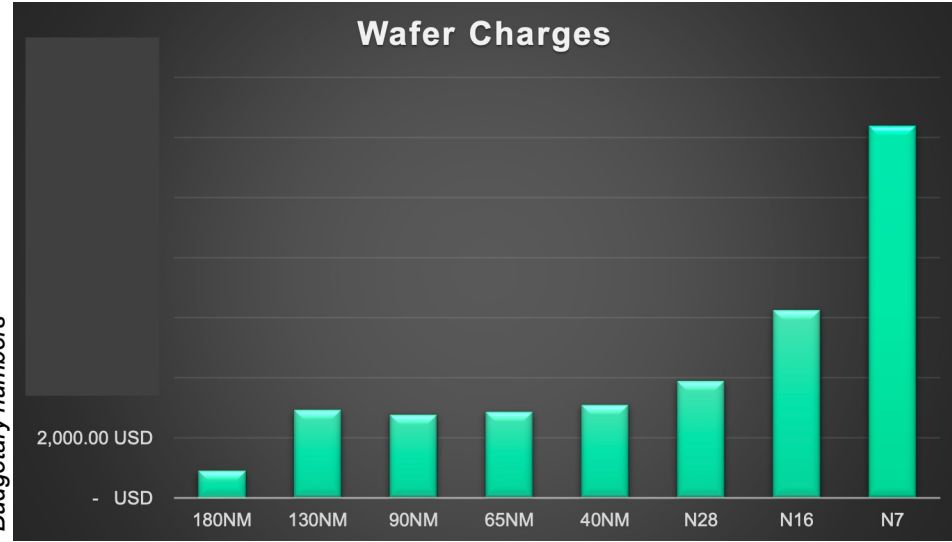
Budgetary numbers



Budgetary numbers



Budgetary numbers



Budgetary numbers

Source: Europractice presentation at MUG session TWEPP2023



# 28 HPC+ technology options

- Multiple metal schemes and technology options available
- **Narrow down options in the common design platform to facilitate**
  - IP block exchange
  - Work on common projects
  - Organize MPWs for sharing prototyping costs

## 28nm Common Design Platform

PDK: mmWave HPC+

Vt options: lvt, svt, hvt, uhvt, ehvt/SRAM\_LL

Metal scheme: IP9M\_5X1Z1U + UTRDL

## Europractice support

### CERN ASIC support Team

Alessandro Caratelli

Marco Andorno

Kostas Kloukinas

### 28nm CMOS HPC+ Logic, RF

TSMC 28NM CMOS RF HIGH PERFORMANCE COMPACT MOBILE COMPUTING PLUS 0.9/1.8V

#### Technology characteristics

Shrink technology: YES  
 Core voltage: 0.9V  
 I/O voltage: 1.8V  
 Shallow Trench Isolation (STI)  
 Wells: Retrograde twin well for low well sheet resistance and better latch-up behavior.  
 Triple well, Deep N-Well in option  
 Dual Gate Oxide  
Vt options: ulvt, lvt, svt, hvt, uhvt, ehvt  
 5V HVMOS  
 HighRes resistors  
 Temperature range: -40C to 125C  
 # of metals: 5 to 10 Cu + ALRDL  
 Interconnect dielectric: ELK  
 Top metal: 1.9KA, 8.5KA, 11.5KA, 35KA  
 CMP on STI, contact, via and passivation  
 MoM capacitor  
 Passivation: dual layers

#### Options that need special attention

SRAM Cell  
Vt's: maximum of 4 VT types in one design.

### Metals Schemes

28 HPC	8M	/	lp8m_5x1z1u_ut-aldl
<b>28 HPC+ (use MMWAVE PDK)</b>	7M	lp7m_4x1y1z_aldl	/
	8M	lp8m_5x2r_aldl	lp8m_5x1z1u_ut-aldl
		lp8m_5x2r_ut-aldl	
	9M	/	<b>lp9m_5x1y1z1u_ut-aldl</b>

<https://europractice-ic.com/mpw-prototyping/asics/tsmc/>







# Digital Standard Cell Libraries

tcbn28hpcbw35p140

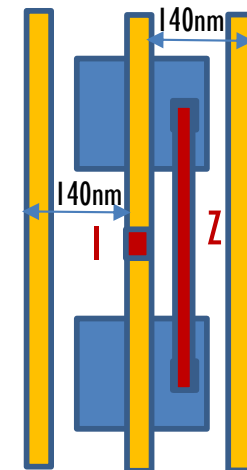
30 nm  
35 nm  
40 nm

Faster ↑  
Less Power ↓

## Gate length

HPC+ 12T	Raw Gate Density Kgates/mm2	Speed GHz	Active Power nW/MHz	Static Power nW/MHz
30nm	2,971	1	1	1
35nm	2,971	0.9	0.992	0.446
40nm	2,971	0.806	1.003	0.232

## Poly pitch



7, 9, 12  
HPC+ only

## Tracks

HPC+ 30P	Raw Gate Density Kgates/mm2	Speed GHz	Active Power nW/MHz	Static Power nW/MHz
7T	4,289	0.742	0.601	0.485
9T	3,961	0.886	0.781	0.714
12T	2,971	1	1	1

SVT, LVT, HVT,  
UHVT, ULVHT

## Voltage threshold

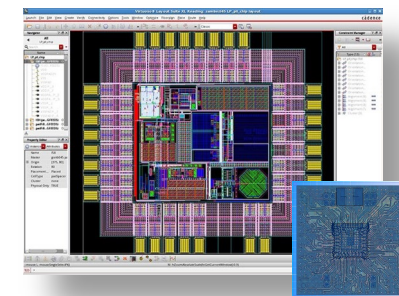
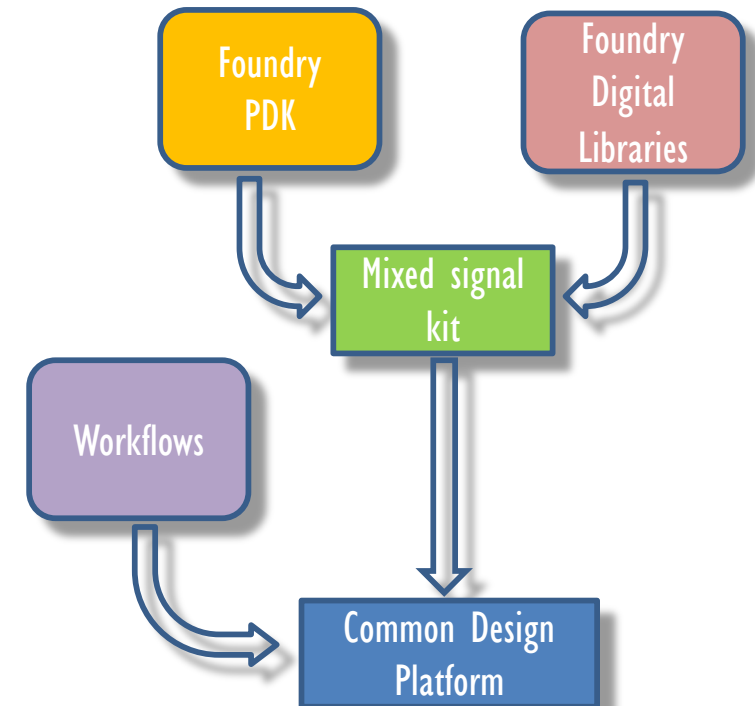
HPC+ 12T 30P	Raw Gate Density Kgates/mm2	Speed GHz	Active Power nW/MHz	Static Power nW/MHz
LVT	2,971	1.351	1.235	5.305
SVT	2,971	1	1	1
HVT	2,971	0.654	0.911	0.127
EHVT	2,971	0.229	0.903	0.019



# Common Design Platform

- 28nm Common Design Platform:
  - Support collaborative work of distributed design teams
  - Minimize efforts to integrate a “design environment”
  - Avoid incompatibilities
- Incorporates:
  - **Mixed-Signal Design kit**
  - **Scripted Design Flows** that are standardized and validated using selected EDA software tools
  - **Maintenance**
  - **Technical Support**
  - **Training**
- Developed by
  - **CERN ASIC Support Team**  
in collaboration with Cadence VCAD Design Services
    - <https://asicsupport.web.cern.ch>

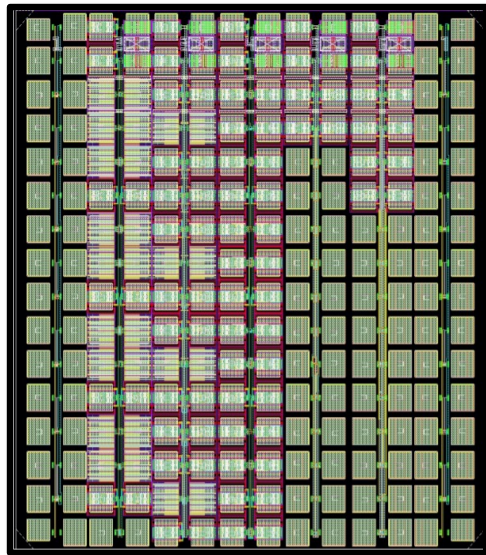
*Europractice versions*





# Radiation Evaluation test chips

## TID CHIP LAYOUT



### SINGLE TRANSISTORS ARRAY

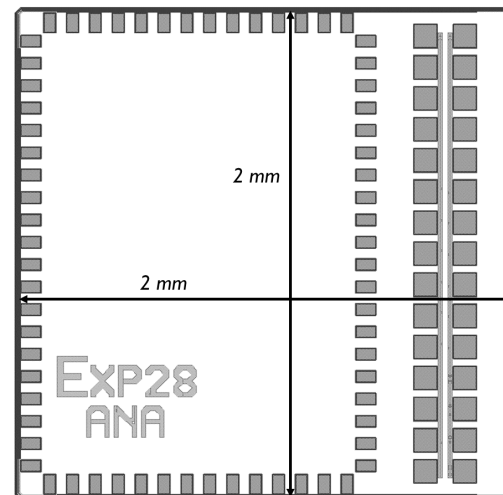
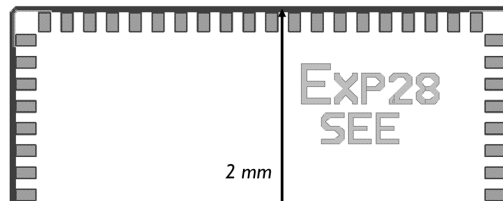
7x probing arrays

Different transistor flavors

Variability arrays

Design submitted in June 2021

## EXP28 CHIP SUITE



### TOTAL IONIZING DOSE (TID) STUDIES:

- Ring Oscillator for standard cells
- Built-In-Self-Test for SRAM memories

### SINGLE EVENT EFFECT (SEE) STUDIES:

- Vernier Delay line for SET studies
- Flip-Flop matrixes for SEU studies
- Functional SRAM test for SEE on memories

### IP BLOCKS CHARACTERIZATION

- Bandgap and Temperature sensor
- Digital-to-Analog Converter (DAC)
- Probe array for HV devices and resistors

*slide by Giulio Borghello*

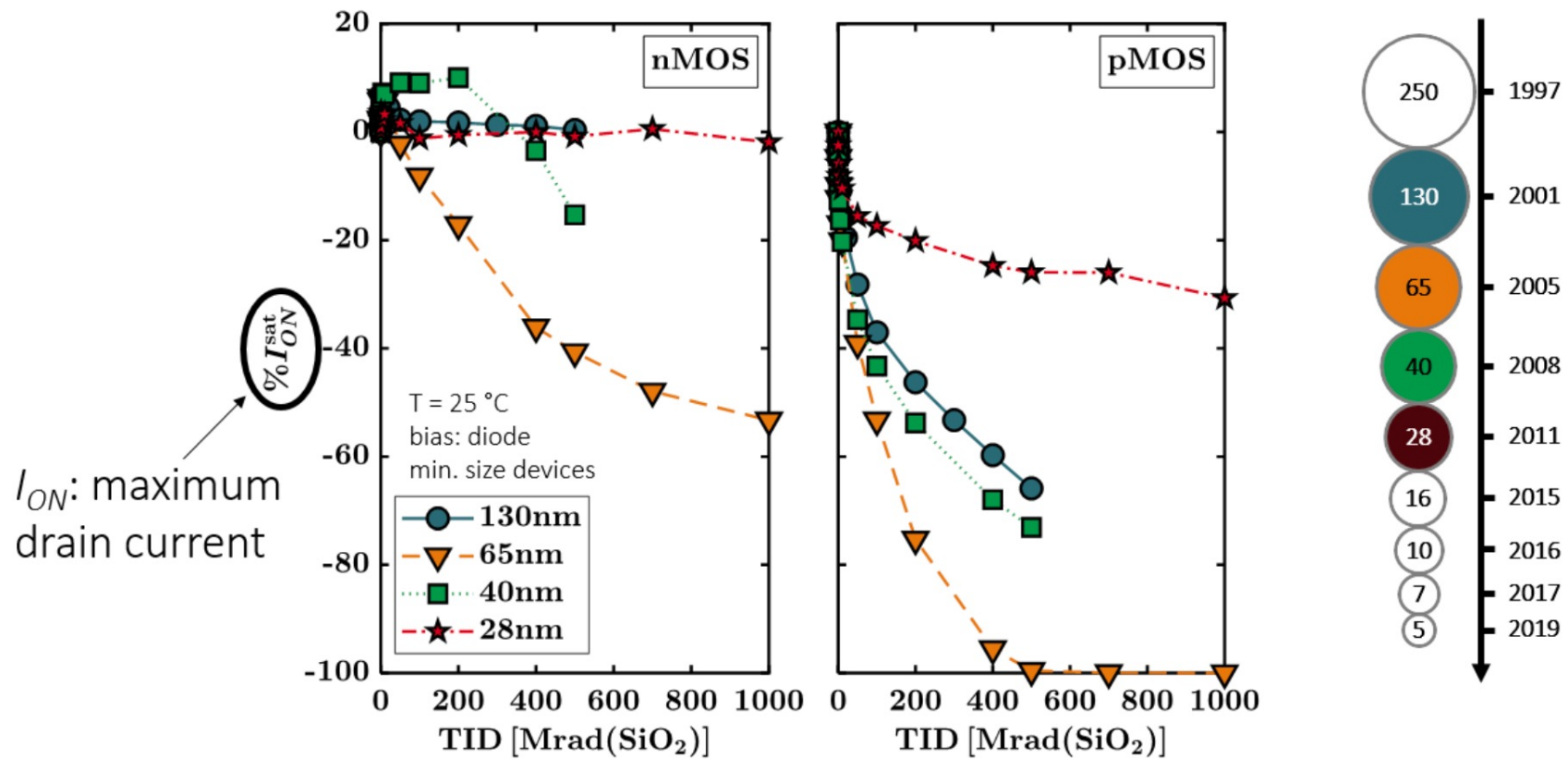


# 28nm TID performance

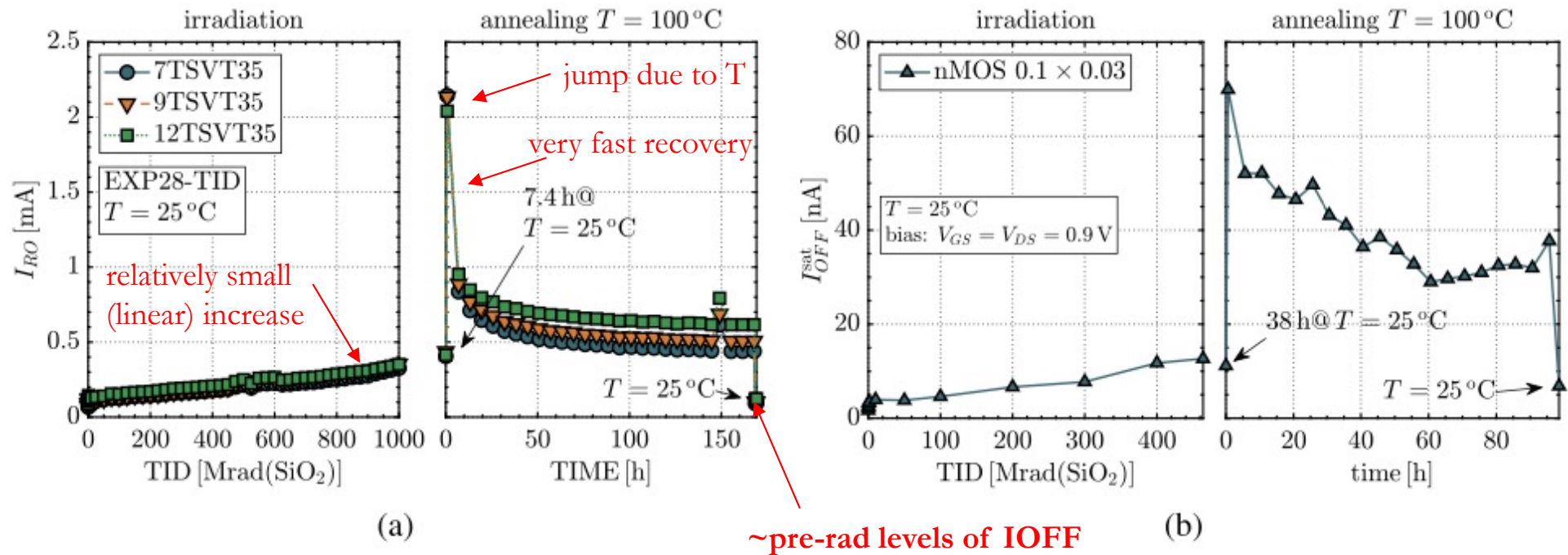
Single transistors

Radiation Hardness of Modern CMOS Technologies to Ultra-High TID

28nm has a very interesting response at ultra-high TID!!



## Power consumption vs TID for different std. cell libraries in Ring Oscillators



**Figure 3.** Current consumption during irradiation and HTA for ROs (a) and single nMOS (b).



# TID: 28nm vs 65nm

library standard cells

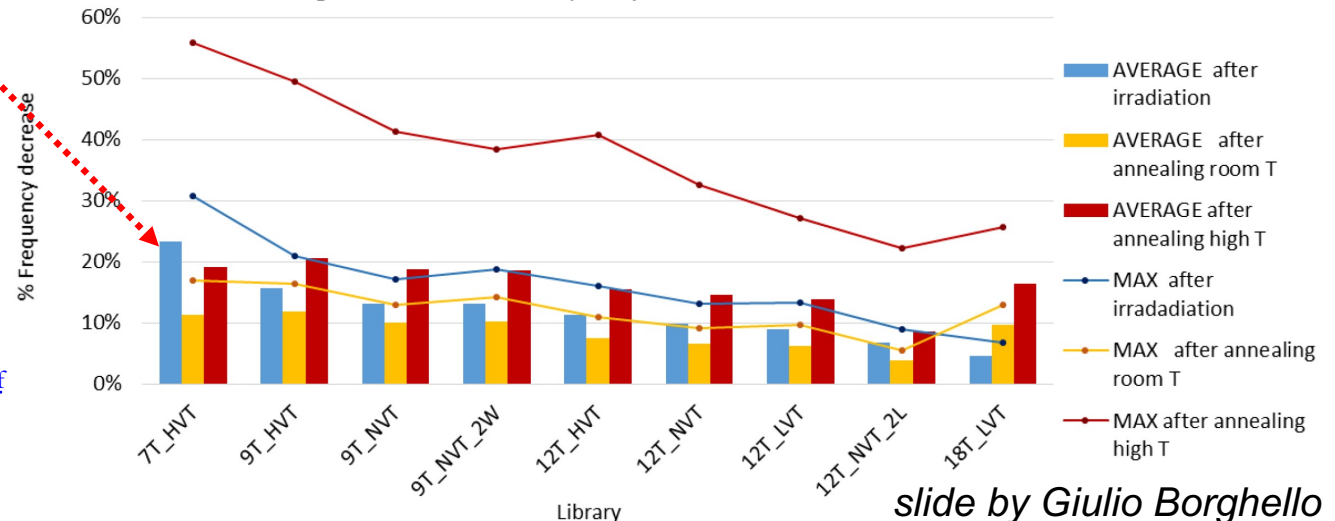
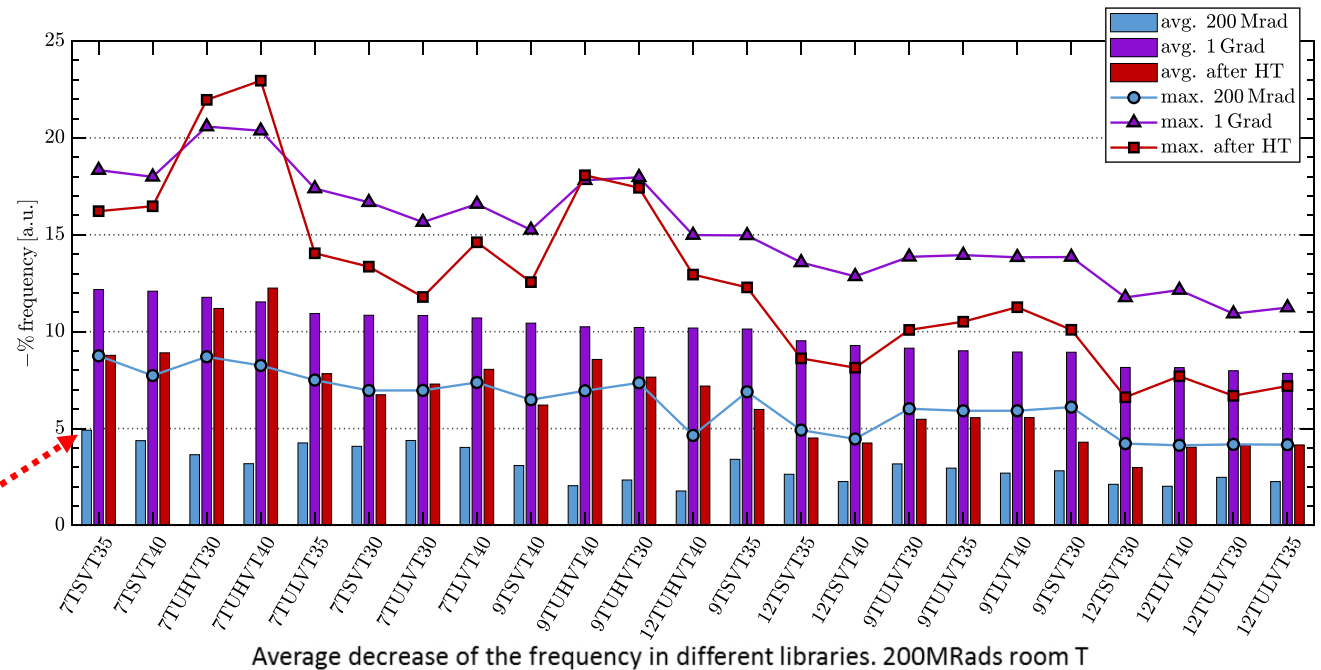
## Ring Oscillators

16 cells x 23 libraries = **368** ROs

28nm

65nm

28nm shows lower degradation than 65nm technology



DRAD chip, 65nm tech.

<https://cds.cern.ch/record/2725573/files/DRAD%20report.pdf>

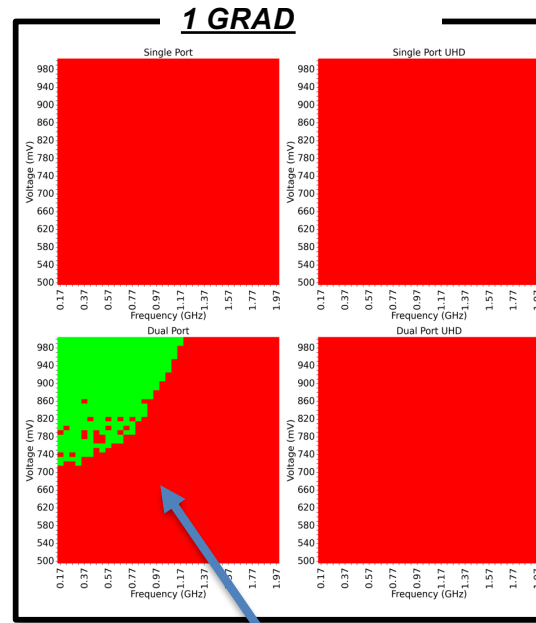
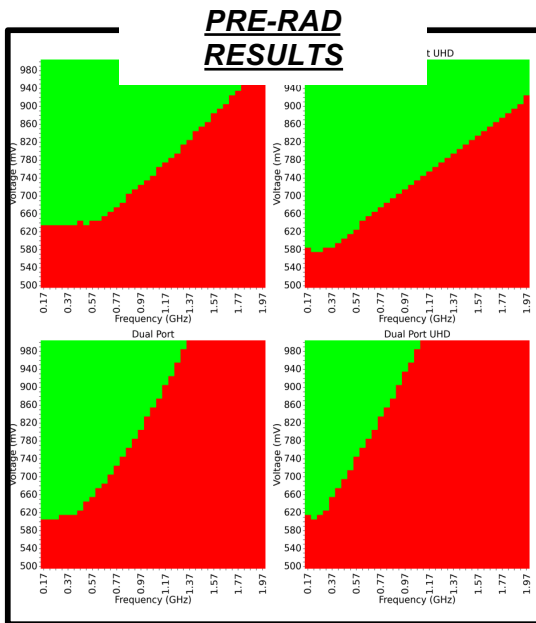
Borghello, G., et al. "Total ionizing dose effects on ring-oscillators and SRAMs in a commercial 28 nm CMOS technology." *Journal of Instrumentation* 18.02 (2023)

slide by Giulio Borghello

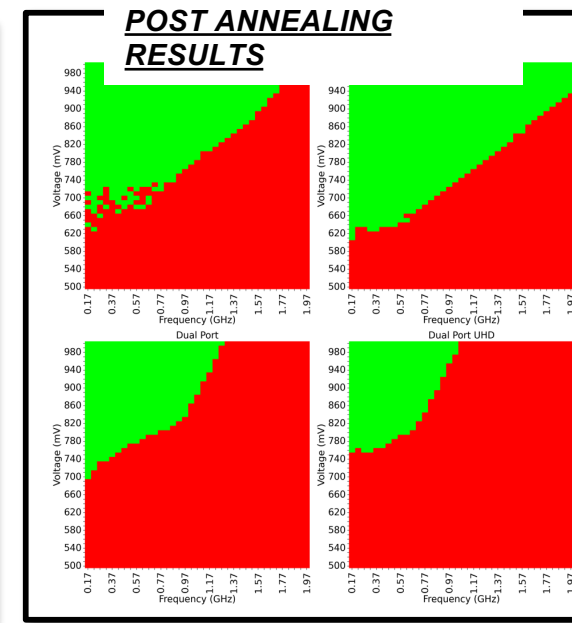
Presented by G. Bergamin at TWEPP 2022:

<https://indico.cern.ch/event/1127562/contributions/4904915/>

**Testing procedure:** BIST logic kept fixed at 0.9V, frequency and voltage scan for SRAMs.



Dual-Port foundry SRAM survived (almost) up to 1Grad

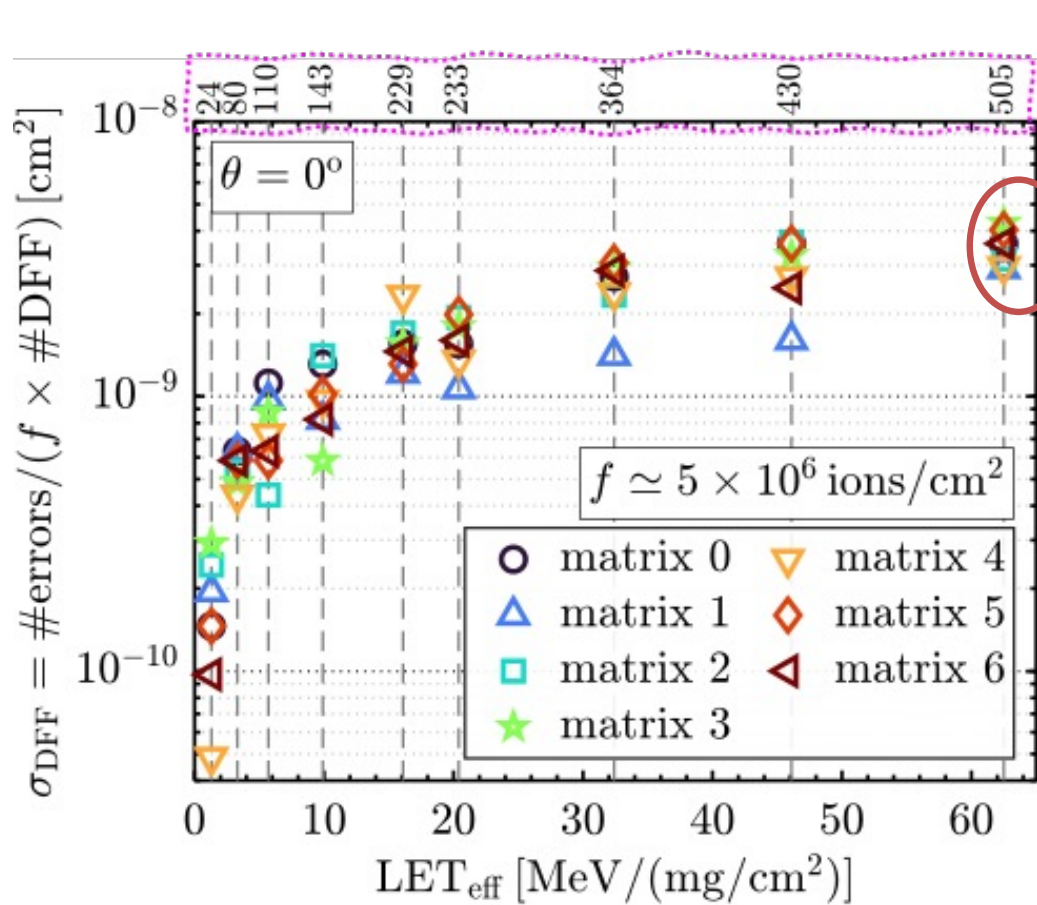


All SRAMs fully recover after annealing

Heavy Ion test run in UCL Louvain



# SEE: Library D-FF



total number of errors

Similar SEE sensitivity for all D-FF types

cross-section  $\sigma_{DFF}$  [cm<sup>2</sup>] = (#errors/#DFF in matrix)/fluence

7 different matrixes with D-FF

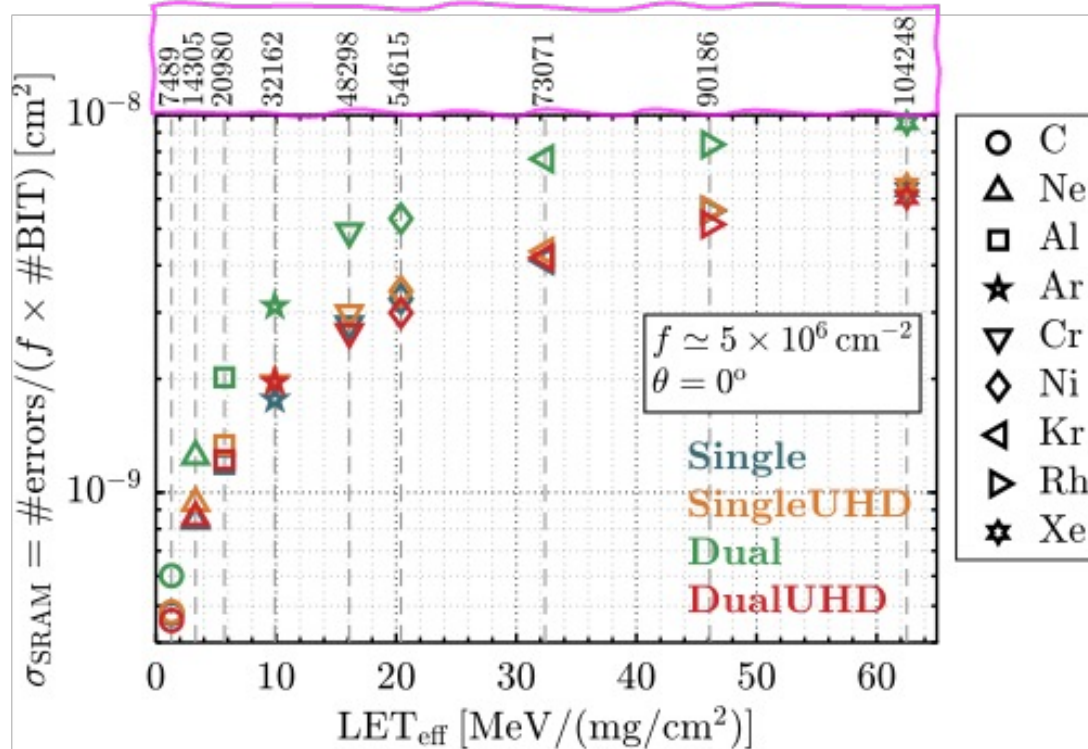
0	<b>D<sub>FF</sub>D1</b>	(D Flip-Flop with Sync Clear)
1	<b>D<sub>FF</sub>D1+C<sub>KB</sub>D1</b>	(D Flip-Flop with Sync Clear + buffer in the D-Q path)
2	<b>D<sub>FF</sub>D4</b>	(D Flip-Flop with D4 driving strength)
3	<b>D<sub>FF</sub>D1LVT</b>	(Low-Vt)
4	<b>D<sub>FF</sub>D1UHVT</b>	(High-Vt)
5	<b>D<sub>FF</sub>D1ULVT</b>	(UltraLow-Vt)
6	<b>D<sub>FF</sub>D1</b>	(~5.5 μm spacing between DFF)

slide by Giulio Borghello



# SEE: SRAM blocks

much larger statistics than DFF



Dual SRAM has a slightly higher cross-section

larger cells in dual SRAM  
-> larger sensitive area

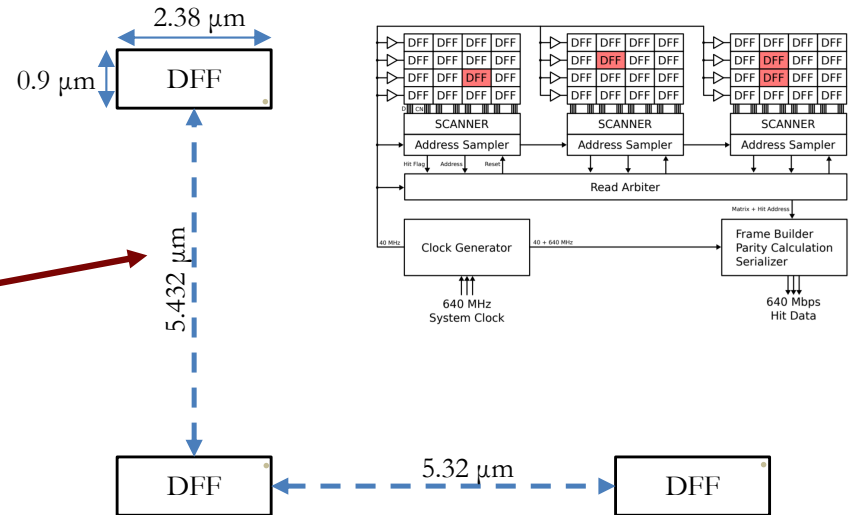
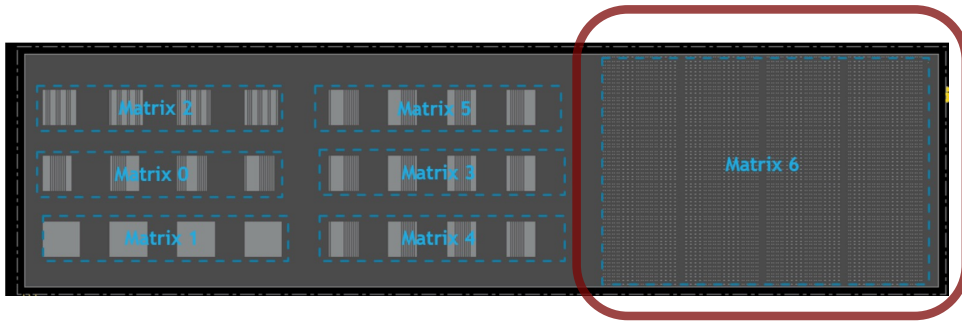
BITCELL transistor dimensions

SINGLE PORT (L,W,M) 6T	nchpd_sr	nchpg_sr	rchpu_sr
S1BHVT5WBASO100W10_BCELL_SD	35 95 1	35 65 1	35 40 1
S1BHVT5WBASO100W10_TKBL_BCELL_SD	35 95 1	35 65 1	35 40 1
S1BHVT5WBASO100W10_TKBL_EDGE_SD	35 95 1	35 65 1	35 40 1
DUAL PORT (L,W,M) 8T	pchpu_dpsr [2]	nchpd_dpsr [4]	nchpg_dpsr [4]
S0MWBASO100W10_MCB	35 50 1	35 195 1	35 140 1
S0MWBASO100W10_TKBL	35 50 1	35 195 1	35 140 1
S0MWBASO100W10_TKNOR	35 50 1	35 195 1	35 140 1
ULTRA HIGH DENSITY SINGLE PORT (L,W,M) 6T	nchpd_sr	nchpg_sr	rchpu_sr
S1BUHDHVT5WBASO100W10_TKBL_BCELL	35 95 1	35 65 1	35 40 1
S1BUHDHVT5WBASO100W10_MCB	35 95 1	35 65 1	35 40 1
S1BUHDHVT5WBASO100W10_TKBL_EDGE	35 95 1	35 65 1	35 40 1
ULTRA HIGH DENSITY DUAL PORT (L,W,M) 6T	nchpd_sr	nchpg_sr	rchpu_sr
S0BMWA100W10_TKBL_EDGE	35 95 1	35 65 1	35 40 1
S0BMWA100W10_TKBL_BCELL	35 95 1	35 65 1	35 40 1
S0BMWA100W10_MCB_TKWL_ISO	35 95 1	35 65 1	35 40 1
S0BMWA100W10_MCB_TKWL	35 95 1	35 65 1	35 40 1
S0BMWA100W10_MCB	35 95 1	35 65 1	35 40 1

slide by Giulio Borghello

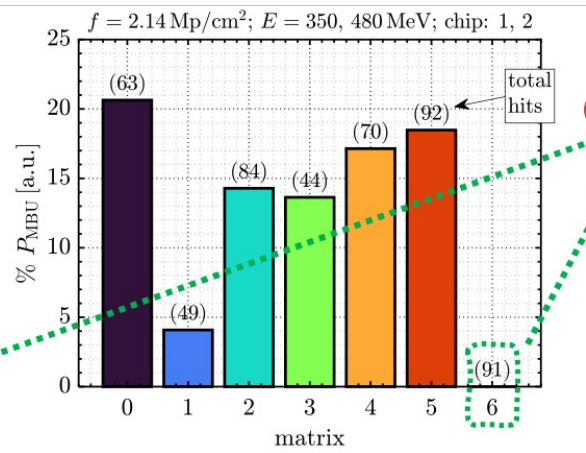
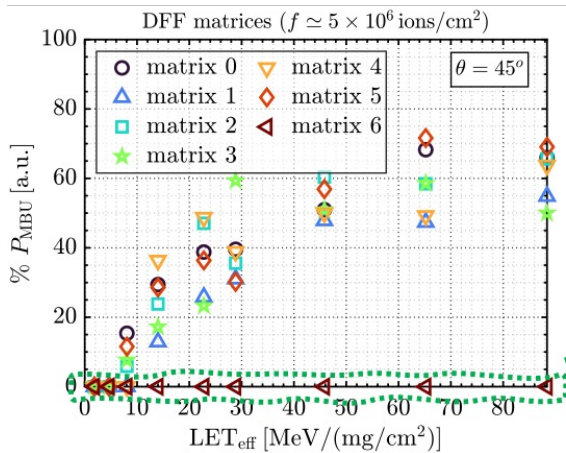
# SEE: min distance for MBUs

7 matrices with D-flip/flops



heavy ions

protons



no MBU in matrix 6!

~6 μm spacing between DFFs drastically reduces probability of MBU!

- key information for triplication strategy!
- ~2.5 times less than the 15 μm typically used in 65nm technology!

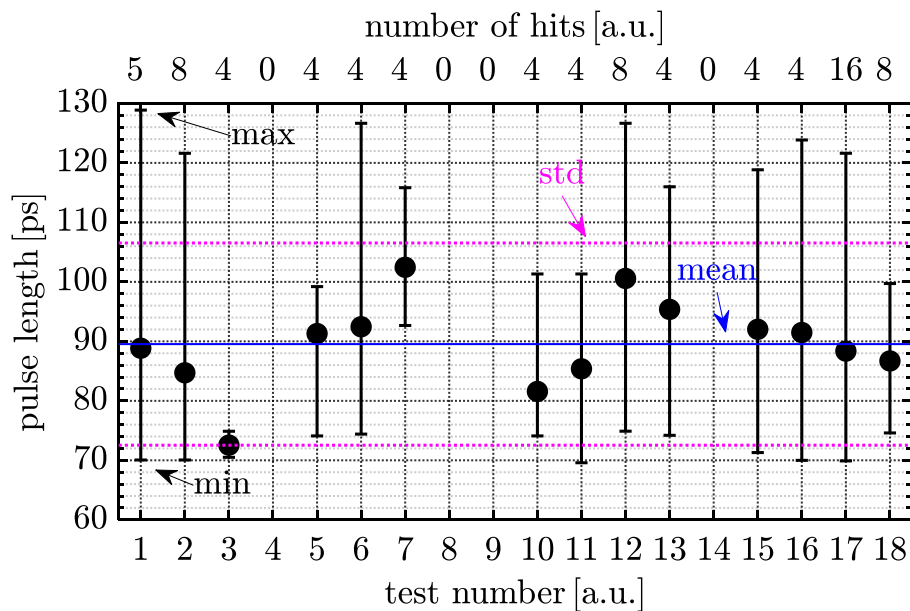
slide by Giulio Borghello



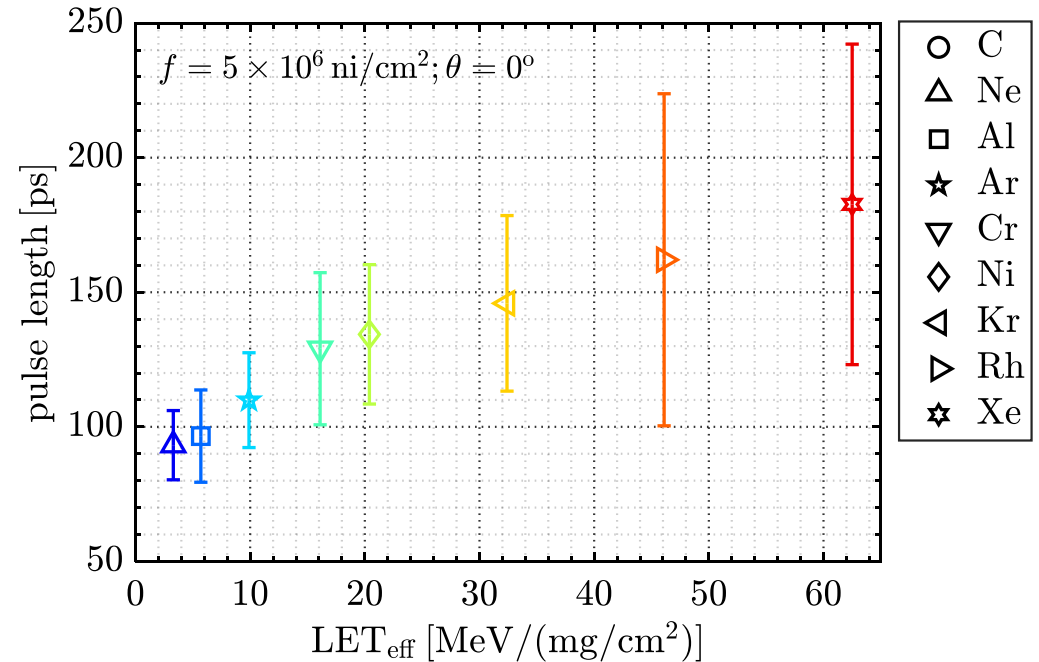
# SET pulse length deduction

Important parameter for implementing Temporal Redundancy fault tolerant schemes

heavy ions →



← protons

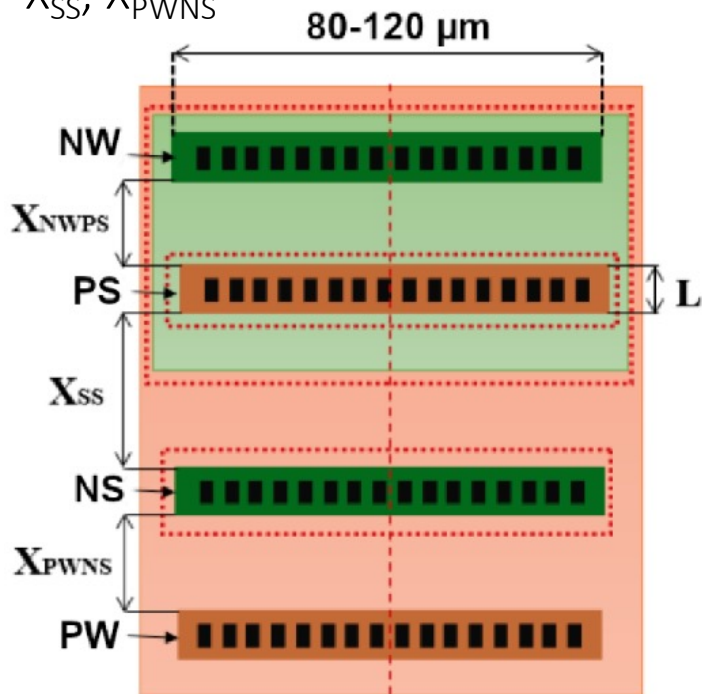


slide by Giulio Borghello

# Latch-up immunity tests

Latch-up sensitivity depends on doping levels (which cannot be changed) and distance between wells

40 structures with different  $X_{NWPS}$ ,  $X_{SS}$ ,  $X_{PWNS}$



ion	angle [°]	LET [MeV/(mg/cm <sup>2</sup> )]	fluence [10 <sup>6</sup> ni/cm <sup>2</sup> ]	voltage
Ni	0	20.4	23.3	VDD (0.9 V)
Ni	45	28.85	16.2	VDD
Kr	45	45.82	11.4	VDD
Xe	0	62.5	51.6	VDD
Rh	45	65.2	11.4	VDD
Xe	45	88.39	6.2	VDD
Xe	45	88.39	45.0	1.15*VDD
Xe	75	241.48	1.72	1.15*VDD

high LET, high voltage

No SEL  
in any of the structures  
for any for the tests!!!






# Rad-Tol IP Block library

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## RADIATION TOLERANT ESD PROTECTIONS

-  outsourced to SOFICS by the CERN ASIC Support
-  Design completed. Submitted in Jan 2022 for radiation characterization.
-  [https://asic-support-28.web.cern.ch/docs2/slvs\\_tx\\_rx](https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx)





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## RADIATION TOLERANT CMOS IO PAD

-  outsourced to SOFICS by the CERN ASIC Support
-  In progress. Radiation characterization will follow.
-  [https://asic-support-28.web.cern.ch/docs2/slvs\\_tx\\_rx](https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx)

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## SRAM MEMORIES

-  Compilers purchased from the Foundry by the CERN ASIC Support
-  We can distribute precompiled memory upon request
-  Submitted in Jan 2022. Radiation characterization completed.
-  [https://asic-support-28.web.cern.ch/docs2/slvs\\_tx\\_rx](https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx)

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## EFUSES

-  IP block purchased from the Foundry by the CERN ASIC Support
-  Radiation characterization will follow.
-  [https://asic-support-28.web.cern.ch/docs2/slvs\\_tx\\_rx](https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx)



# Rad-Tol IP Block library

## BANDGAP VOLTAGE REFERENCE & TEMP MONITOR

- G. Traversi** (Bergamo/Pavia) / INFN Falaphel project
- Design completed. Submitted in Jan 2022
- [https://asic-support-28.web.cern.ch/docs2/slvs\\_tx\\_rx](https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx)

## RAIL TO RAIL OPERATIONAL AMPLIFIER

- Jan Kaplon** (CERN EP-ESE)
- Design completed. To be submitted in Dec. 2022.
- [https://asic-support-28.web.cern.ch/docs2/slvs\\_tx\\_rx](https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx)

## DIGITAL TO ANALOG CONVERTER (8-BIT)

- Markus Piller** (DOCT, CERN EP-R&D WP5)
- Design completed. Submitted in Jan 2022
- datasheet [https://asic-support-28.web.cern.ch/docs2/slvs\\_tx\\_rx](https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx)

## ADC FOR MONITORING (12-BIT)

- Tobias Hofmann** (CERN EP-R&D WP5)
- In progress
- [https://asic-support-28.web.cern.ch/docs2/slvs\\_tx\\_rx](https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx)

## DIFFERENTIAL LINE DRIVERS AND RECEIVERS

- Franco Bandi** (CERN EP-R&D WP5)
- Design completed. Submitted in Jan 2022
- [https://asic-support-28.web.cern.ch/docs2/slvs\\_tx\\_rx](https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx)

## RAIL TO RAIL OPERATIONAL AMPLIFIER

- Markus Piller** (CERN, DOCT)
- In progress
- [https://asic-support-28.web.cern.ch/docs2/slvs\\_tx\\_rx](https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx)

## ANALOG PLL

- Tobias Hofmann** (CERN EP-R&D WP5)
- In progress
- [https://asic-support-28.web.cern.ch/docs2/slvs\\_tx\\_rx](https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx)

## DIGITAL PLL

- Markus Piller** (DOCT, CERN EP-R&D WP5)
- In progress
- [https://asic-support-28.web.cern.ch/docs2/slvs\\_tx\\_rx](https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx)

## DCDC CONVERTER

- Stefano Michelis** and **Giacomo Ripamonti** (CERN EP-ESE)
- In progress
- [https://asic-support-28.web.cern.ch/docs2/slvs\\_tx\\_rx](https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx)

## LDO

- Stefano Michelis** and **Giacomo Ripamonti** (CERN EP-ESE)
- In progress
- [https://asic-support-28.web.cern.ch/docs2/slvs\\_tx\\_rx](https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx)



# AMTest28 chip for common IPs

## Test chip Submitted in August 2023

**GOAL:** Silicon-prove the IP blocks designed in 28nm, by functional and radiation testing

- Marco Andorno (ASIC Support) prepared a test chip that integrates several IP-blocks from CERN or from other institutes providing a single MPW run to test multiple blocks, and uniform testing requirements
- The analog and mixed-signal blocks were assembled Digital-on-Top, along with a control and configuration interface (triplicated):

### IP-Block

### Designer

SLVS Transmitter and Receiver

Franco Bandi (CERN)

Digital PLL

Vladimir Gromov (Nikhef)

Rail-to-rail analog buffer

Jan Kaplon (CERN)

Analog frontend

Markus Piller (TU Gratz)

Bandgap reference (4 different versions)

Grzegorz Wegrzyn, Stefano Michelis (CERN)

TIMO28 (TID response variation IP block)

Giulio Borghello (CERN)

8-bit DAC

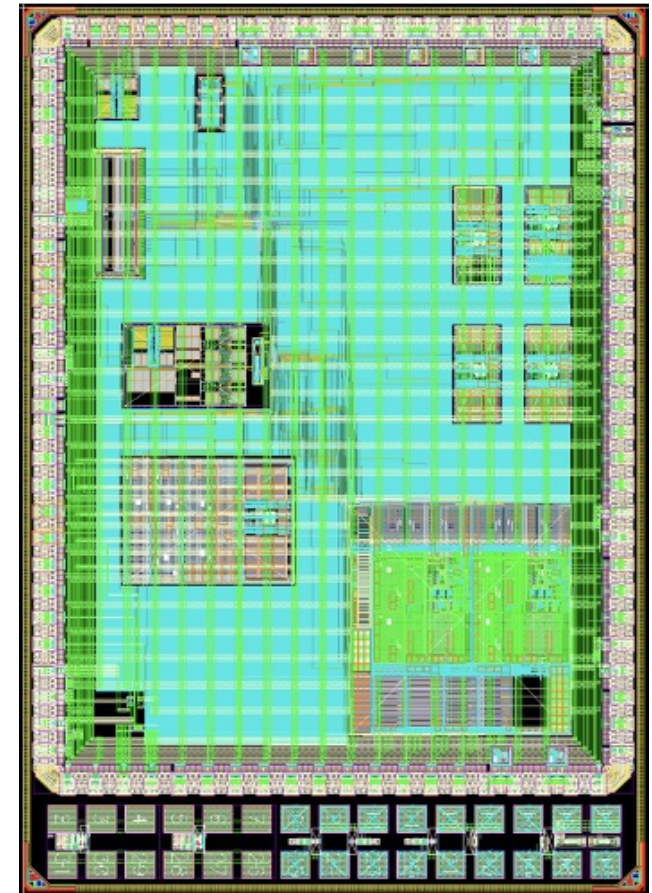
Markus Piller (TU Gratz), Viros Sriskaran

12-bit Sigma-Delta DAC

Can Akgun (Nikhef)

Test structures (4 types)

SOFICS





# IP block Library

## CERN ASIC Support is taking care of:

- Packaging in a uniform way the IP blocks
- Maintenance of the shared repositories (Cliosoft) and institutes access and provide access upon request

The ownership of the IP block remains with the designer. The platform allow to advertise and share the IP blocks with the community.

## List of available IP blocks and datasheets:

- F2 28:** <https://asic-support-28.web.cern.ch/ip-blocks/>  
**F2 65:** <https://asic-support-65.web.cern.ch/docs2/>  
**F2 130:** <https://asic-support-130.web.cern.ch/docs2/>  
**F1 130:** <https://espace.cern.ch/asics-support/gf130/>

All institutes that wish to contribute are invited to participate to common repositories with analog and digital IP blocks, shared within the community! Get in touch!

The screenshot displays the 'IPs And Macro Blocks' page on the CERN ASIC Support website. The page features a navigation menu at the top with options like HOME, DESIGN PLATFORMS, and TECHNICAL DOCUMENTS. The main content area is titled 'IPs And Macro Blocks' and includes a sub-header: 'The TSMC 28nm based common design platform for the high Energy Physics community'. Below this, there is a call to action: 'All institutes that wish to, are invited to contribute with analog and digital IP blocks shared within the community. Get in touch!'. The page lists several IP blocks and datasheets, each with a 'CONTINUE READING' button. The listed items include: RADTOL ESD PROTECTION LIBRARY, SLVS TRANSMITTER AND RECEIVER, TSMC DUAL-PORT SRAM, and TSMC ELECTRICAL FUSE. A right-hand sidebar contains 'Categories' (Designer's Guide, Foundry documents, IPs and macro blocks) and 'Tags' (Application Notes, Foundry, Guide, IPs, Macroblocks, Manuals, PDK, Tutorial).



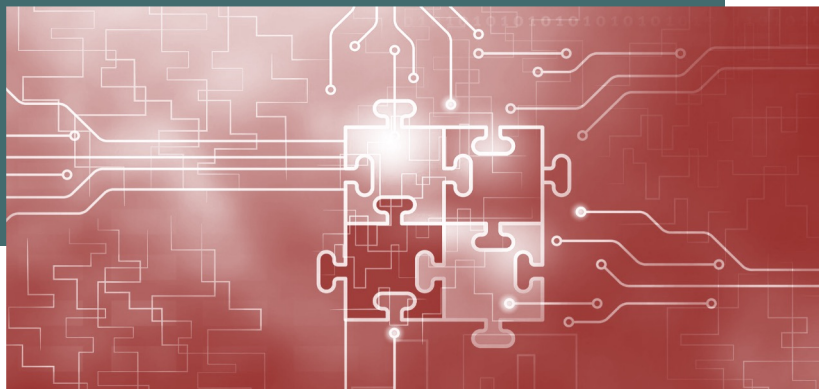


# System-on-Chip design approach

Future detector upgrades will require more complex ASICs

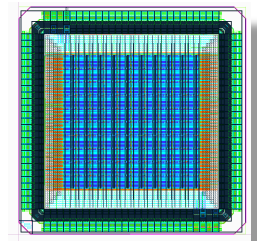


They require advanced technology nodes, that come with high development costs in terms of design time, verification and costs



An abstract design methodology, focused on programmability and reusability will allow to:

- Develop reusable IP blocks
- Standardize interconnects for IP blocks
- Replace state machines with a control processor (RISC-V based)
- Programmable, flexible logic blocks (SoC Ecosystem, cores, eFPGA, NoCs)
- Enhance Hierarchical Digital Implementation and Verifications
- Use of Open Source scripts and tools



250nm RT-FPGA

(past successful project: [Development of SEU-robust, radiation tolerant and industry compatible programmable logic components](#))



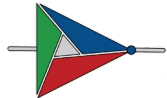
# SoC Generator Tool in development



Hardware generation



Software generation

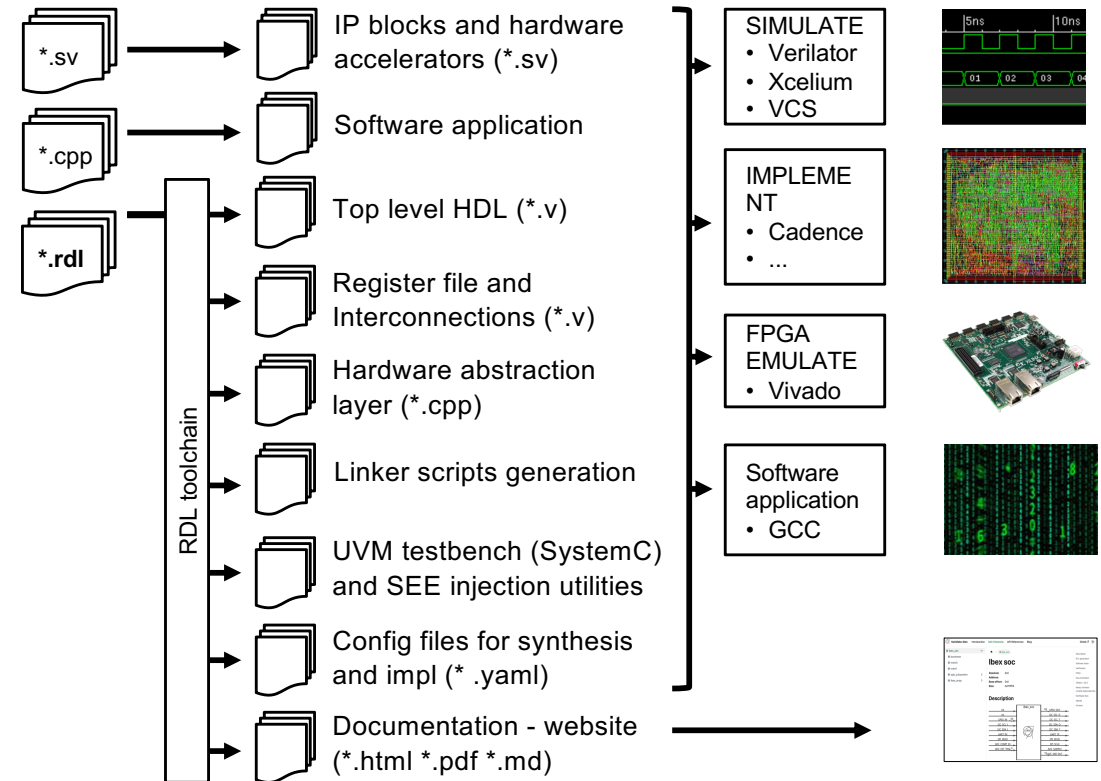


## SoCMake

DOC: <https://socmake.docs.cern.ch>

GIT: <https://gitlab.cern.ch/socmake>

- Open-source SoC generator tool
- From a single SystemRDL description file, automatize the generation of:
  - Hardware design
  - Software toolchain
  - Verification platform
  - Documentation
- Generate custom SoCs
- Rapid SoC prototyping
  - Quickly build different architectures with different IP blocks, hardware accelerators and different CPUs
- Design team: [R. Pejasinovic](#), M. Andorno, A. Caratelli, A. Nookala, K. Kloukinas

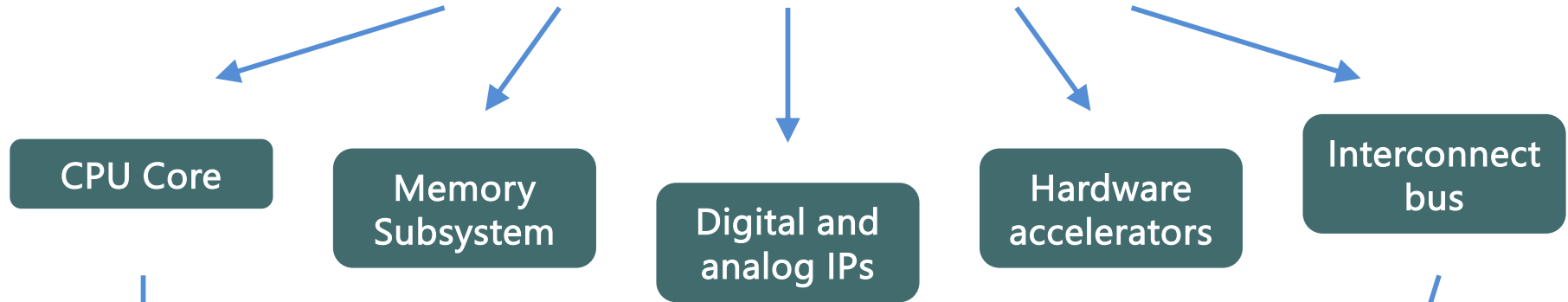


## Work in progress



# SoC platform in development

## SoC platform components



For the moment  
4 popular  
cores supported:

- LowRISC Ibex
- ChipsAlliance (WD) EL2
- Syntacore SCR1
- Picorv32

Support for multiple interconnect busses

- APB4 → APB-RT
- AXI4-Full → AXI-RT
- Axi4-Lite → AXI-Lite-RT
- NMI, OBI

Radiation tolerant version:  
Tripllicated control signals  
Encoded data and address lines

Work in progress



# Collaborative Framework

---

- NDAs
  - Special 3-way NDA (institute-IMEC-Foundry) that permit collaborative work
    - Permit the exchange of designs and technical data among collaborators
    - CERN and 45 institutes have signed the 3-way NDA
  
- Commercial frame contract
  - CERN has a frame contract that allows small-scale prototyping (MPWs)
  - It will be extended to cover full-maskset engineering and production works
  - The frame contract is accessible by HEP Institutes and Universities, via CERN



# ASIC Support website



<https://asicsupport.web.cern.ch>

Alessandro Caratelli, Marco Andorno, Kostas Kloukinas

HOME DESIGN PLATFORMS FOUNDRY SERVICES IP BLOCKS TECHNICAL DOCUMENTS DESIGN FLOWS TRAINING FORUM CONTACTS English

## CERN ASICs TECHNOLOGIES & FOUNDRY SERVICES

The CERN EP-ESE group is offering a set of services to all the collaborating institutes and universities for the exploitation of state of the art microelectronic technologies for the implementation of application specific integrated circuits in the High Energy Physics experiments.

- COMMON DESIGN PLATFORMS**: Development and maintenance of the common Design Platforms
- TECHNICAL SUPPORT**: Provide technology and EDA tool support to designers in the HEP community
- IP BLOCKS ACCESS**: Distribution and maintenance of HEP specific radiation tolerant macro blocks and IPs
- DESIGN FLOWS**: Prepare and distribute Digital and Mixed-signal design flows of general use
- TRAINING**: Organize and provide courses and workshop about 3 times per year
- CONTRACTS**: Establish Commercial Contracts with silicon vendors
- NDAS**: Establish NDAs that allow for collaborative work
- SILICON FABRICATION**: Organize & coordinate silicon fabrication

CONTACTS

Design Platforms Foundry Services Design Flows Training Discourse Forum Contacts 469

CERN - EP-ESE - ASICs Technology Support and Foundry Services

TECHNICAL DOCUMENTS ▾

- GF 130nm docs
- TSMC 130nm docs
- TSMC 65nm docs
- TSMC 28nm docs**
- Radiation tolerance reports

## Design Manuals And Guidelines

CERN-EP Common Design Platform for the TSMC 65nm technology

March 2, 2022 Posted by CERN-EP-ESE ASICs Technology Support Service Manuals, Foundry, Application Notes

In this section you can access the design manuals and PDK documentation

**DISCLAIMER:** The material contained herein is protected by a non-disclosure agreement and CERN. To the best of authors' knowledge, all readers have signed an equivalent. Authors do not take any responsibility of eventual infringements or abuses related to the use of this information. Usage of this information is subject to the conditions that the information is provided for a specific purpose only. CERN and the authors of this document are not responsible for the interpretation of the data and disclaims any and all types of warranties, express or implied, of merchantability or fitness for a particular purpose.

**Design Manual v2.0**

**Tapeout guidelines document**

**RC Extraction Guidelines**

**N28HPC+ Sign-off Recommendation.pdf**

**Standard Cell Library Application Note**

**PDK usage introduction guide**

## 28nm Reliability Rules

CERN-EP Common Design Platform for the TSMC 65nm technology

February 5, 2022 Posted by CERN-EP-ESE ASICs Technology Support Service Manuals, Foundry, Application Notes

Gate Oxide Lifetime prediction - Hot Carrier Injection Effect - Bias Temperature Instability (NBTI / PBTI)

**1. Gate Oxide Lifetime prediction**

click here to visit the related discourse topic for more info and discussions

**1.1 Failure mechanism**

When an electron current is passed through gate oxide, defects such as electron traps, interface states, positively charged donor-like traps, and so on, gradually build up in the gate oxide until a conduction path is formed, followed by thermal run away. According to the anode hole injection model, injected electrons generate holes at the anode that can tunnel back into the oxide. Intrinsic breakdown occurs when a critical hole density is reached.

**1.2 Core devices gate oxide lifetime prediction**

**Outline**

- 1.1 Failure mechanism
- 1.2 Core devices gate oxide lifetime prediction
- 1.3 IC devices gate oxide lifetime prediction
- 1.4 Measurements conditions
- 1.4.1 Stress condition
- 1.4.2 Failure Criteria
- 2.1 Failure mechanism
- 2.2 DC Lifetime due to Hot Carrier Injection Effect
- 2.3 Measurements conditions
- 2.4.1 Stress condition
- 2.4.1 Failure Criteria
- 3.1 Failure mechanism
- 3.2 DC Lifetime due to Negative / Positive Bias Temperature Instability (NBTI)
- 3.2.1 NBTI DC Lifetime due to Positive Bias Temperature Instability (PBTI)
- 3.2.2 NBTI DC Lifetime due to Positive Bias Temperature Instability (PBTI)
- 3.3 Measurements conditions
- 3.3.1 Stress condition
- 3.3.2 Failure Criteria



# Hitchhiker's guide to 28nm



## ■ 28nm Designer's Guide

- Technology Overview
- Design Guidelines
- Reliability
- Tutorials

## ■ Available at

- [https://asic-support-28.web.cern.ch/tech-docs/designers\\_guide/](https://asic-support-28.web.cern.ch/tech-docs/designers_guide/)



v0.3  
 April 18, 2023  
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### TSMC28nm Designer's Guide and Technology Overview

Markus Piller  
 Franco Nahuel Bandi  
 Alessandro Caratelli  
 Marco Andorno  
 Stefano Michelis  
 Davide Ceresa  
 Rafael Ballabriga  
 Stefan Biereigel

Keywords: CMOS, 28nm, TSMC, Designers guide, Front-End, Back-End, FEOL, BEOL, transistor, capacitor, resistor, current density, electromigration

**Summary** This document gives the minimum requirements for ASIC designs in TSMC 28nm technology and gives a technology overview. The specified requirements are a guide to building a common basis for IP blocks within the new technology. Additional requirements or adaptations may be defined within the project's proposal specification document.

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# Training courses



INFO AND SUBSCRIPTION: [https://asicsupport.web.cern.ch/training\\_courses/workshop28nm](https://asicsupport.web.cern.ch/training_courses/workshop28nm)

A total of **145** Designers from HEP institutes have attended these training workshops in the last 3 years

Digital-on-top hierarchical  
Implementation in workshop

## DoT Workshop

- Learn the main concepts for designing in 65nm for the High energy Physics environment
- Learn the main concepts of the digital implementation from the synthesis, physical implementation and signoff (RTL to GDS)
- Perform synthesis, physical implementation and signoff steps
- Exercise bottom-up and top-down hierarchical design approaches
- Co-developed between CERN EP-ESE ASIC Support service and Cadence VCAD

2020 TO 2022: 6 TRAINING SESSIONS

System Verilog Advanced Verification  
Environment using UVM workshop

## Verification / UVM

- Learn the main concepts of functional verification for the High energy Physics
- Learn the main concepts of digital design verification
- Learn about the Universal Verification Methodology (UVM)
- In the lab sessions you will learn how to build your own UVC and verification environment
- A Cadence Training Course adapted for the High Energy Physics community requirements

SINCE 2020: **3 TRAINING SESSIONS**  
NEXT SESSION TO BE SCHEDULED

Workshop on Mixed-Signal  
design in 28nm process

## Designing in 28nm

- Learn the main concepts for designing in 28nm for the High energy Physics environment
- Learn the main concepts of the analog and Mixed-Signal design in 28nm, and analog IP characterization
- Learn main concepts about TIDs and SEUs tolerance design
- Learn the main concepts of the digital implementation from the synthesis, physical implementation and signoff (RTL to GDS)

SINCE JAN 2023: **3 TRAINING SESSIONS**  
NEXT SESSION END OF 2023



# The “28nm Forum”



- Purpose of the 28nm Forum
  - ❑ CERN to communicate the EP R&D WP5 activities
  - ❑ Institutes to present their R&D activities and plans
  - ❑ Identify synergies
  - ❑ Establish collaborations

## 28nm Technology Forum Sessions

- 1<sup>st</sup> session (Nov. 12, 2020) <https://indico.cern.ch/event/970389/>
- 2<sup>nd</sup> session (Mar. 10, 2021) <https://indico.cern.ch/event/1009040/>
- 3<sup>rd</sup> session (July 28, 2021) <https://indico.cern.ch/event/1042567/>
- 4<sup>th</sup> session (Mar 23, 2022) <https://indico.cern.ch/event/1132318/>
- 5<sup>th</sup> session (Nov 3, 2022) <https://indico.cern.ch/event/1207114/>
- 6<sup>th</sup> session (Nov .., 2023) **focus on IP blocks**

- Restricted access; requires registration
- Self-inscribed CERN e-group: [28nm-Forum@cern.ch](mailto:28nm-Forum@cern.ch)

Forum on 28nm CMOS  
Thursday 12 Nov 2020, 09:00 → 12:30 Europe/Zurich

Forum on 28nm CMOS  
Wednesday 10 Mar 2021, 14:00 → 17:15 Europe/Zurich

Forum on 28nm CMOS  
Monday 28 Jun 2021, 14:00 → 17:35 Europe/Zurich

Forum on 28nm CMOS  
Wednesday 23 Mar 2022, 14:00 → 18:30 Europe/Zurich  
Kostas Kloukinas (CERN)

Videoconference  
Forum on 28nm CMOS

14:00 → 14:10 **Welcome and Introduction**  
Speaker: Kostas Kloukinas (CERN) 10m

14:10 → 14:35 **28nm CMOS Technology & IP blocks for HEP experiments**  
Speaker: Alessandro Caratelli (CERN, EPFL) 25m

14:35 → 14:50 **28nm Documentation and First IP Blocks for the HEP Community**  
Speaker: Franco Nahuel Bandi (CERN) 15m

14:50 → 15:10 **28nm CMOS Technology Evaluation & Radiation Tolerance**  
Speaker: Giulio Borghello (CERN) 20m

15:10 → 15:25 **Fully integrated Point of Load regulator in 28nm technology**  
Speaker: Stefano Michelis (CERN) 15m

15:25 → 15:45 **News from INFN FALAPHEL project**  
Speaker: Guido Magazzu (Universita & INFN Pisa (IT)) 20m

15:45 → 16:05 **News from INFN TIMESPOT project**  
Speaker: Adriano Lal (Universita & INFN Cagliari (IT)) 20m

16:05 → 16:20 **Coffee Break** 15m

16:20 → 16:35 **News & Plans from IN2P3**  
Speaker: Mohsine Menouni (Asi/Marseille Univ, CNRS/IN2P3, CPPM, Marseille, France) 15m

16:35 → 16:55 **Low frequency noise: MOSFET characterization setup and testchip development for RTN studies**  
Speaker: Alicja Michalowska-Forsyth 20m

16:55 → 17:15 **Status update on TSMC 28 nm design at Fermilab - Case study for CMS Pixel chip in 28 nm**  
Speaker: Ceesar Boudin (Dowling) 20m





# Summary

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- A 28nm bulk CMOS technology has been fully characterized for operation up to 1GRad TID
- A Common Design Platform and a Collaborative Framework are implemented to facilitate design work in the HEP community

45

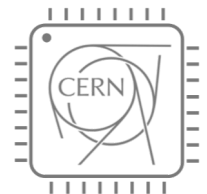
INSTITUTES HAVE SIGNED  
THE 3-WAY NDA

14

PROTOTYPES on MPW runs  
in 2022-23

- CERN EP R&D WP5 “IC Technologies” enabled the development ASIC support & Foundry Service facilitates long term access and support

Institutes wishing to join should contact CERN ASIC Support Service [asic.support@cern.ch](mailto:asic.support@cern.ch)



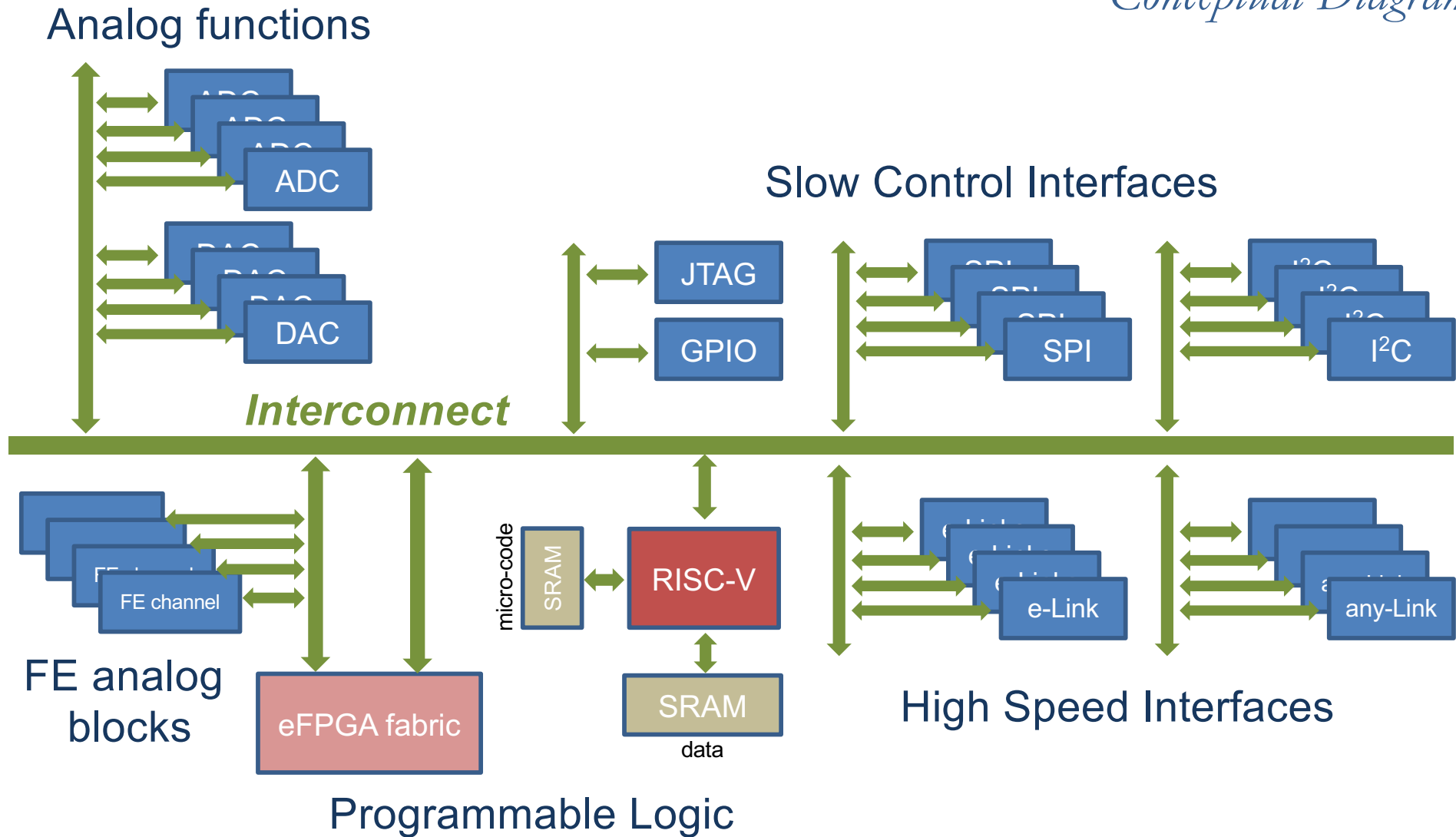


*Thank You*



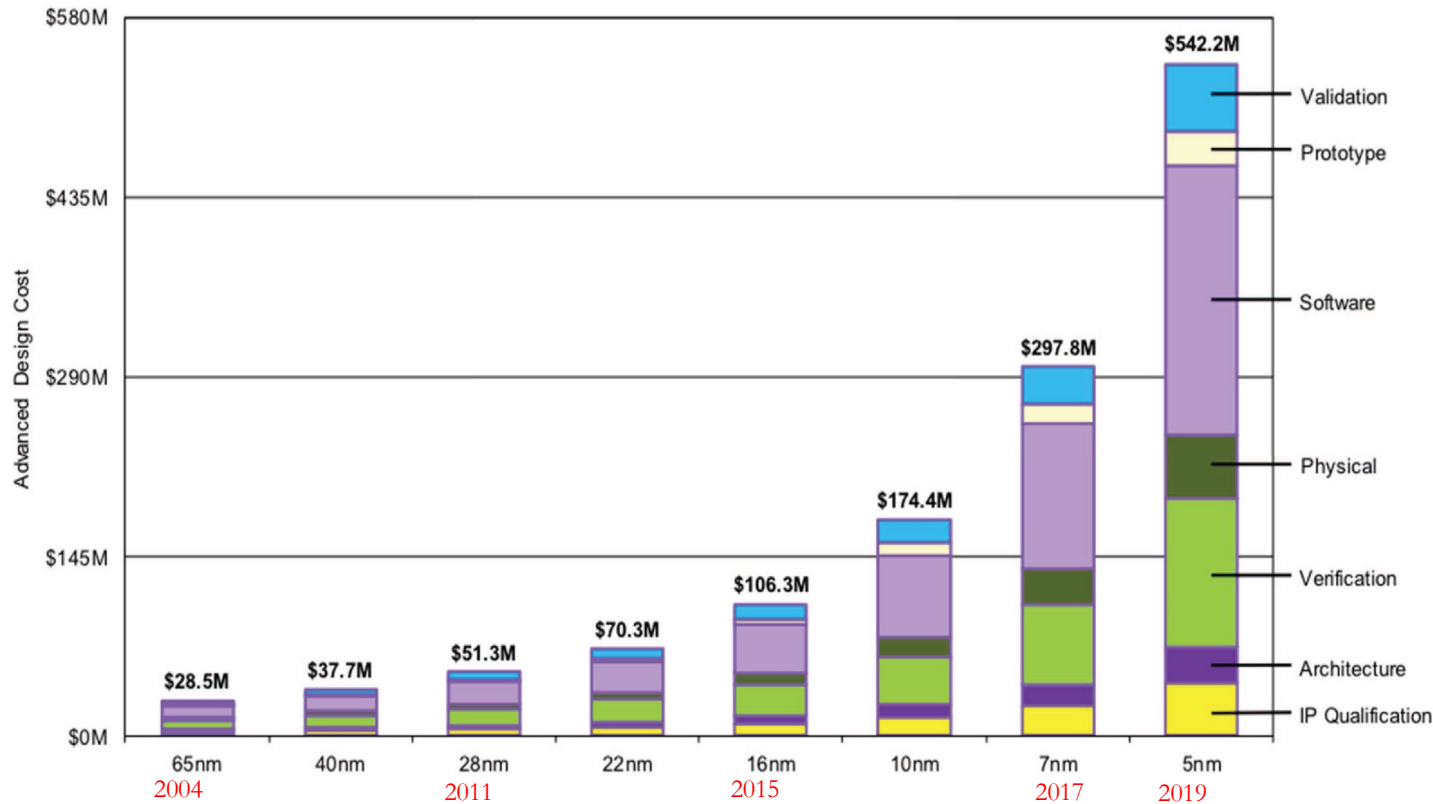
# SOC Radiation Tolerant Ecosystem

*Conceptual Diagram*





# ASIC development costs



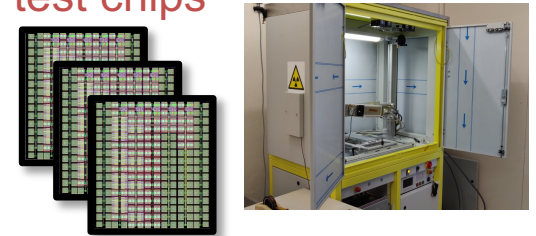
Chip Design and Manufacturing Cost under Different Process Nodes: Data Source from IBS\*

- Escalating development costs when going Ultra Deep Submicron & Nanometer scale
- **At present the 28nm node is the optimum techno-economic choice (or limit ?)**

- Three technologies were evaluated for TID radiation tolerance

- 28nm bulk CMOS processes
  - Foundry A (one variant: Low Power)
  - Foundry B (two variants: High Performance, Low Power)
- 22nm CMOS FD-SOI process
  - Foundry A

Prototyped & irradiated test chips



- Selected a 28nm bulk CMOS technology as the next mainstream node for future Rad-Tol designs

- Radiation Tolerance
  - Accessibility
  - Technical support
  - Foundry IP blocks
  - Long Term availability
  - Cost
- } Europractice  
 Regular MPWs and mini@sics  
  
 Mainstream Foundry