Timepix4 performance

Riccardo Bolzonella, INFN and University of Ferrara
On behalf of Medipix4 collaboration

VERTEX23 workshop - Sestri Levante, 16th - 20th October 2023

Overview

- Medipix4 collaboration and Timepix4 overview
- Timepix4 architecture and operating principle
  - pixels arrangement
  - Through-Silicon-Vias and Wire Bonds
  - acquisition modes
  - Time-of-Arrival (ToA) and Time-over-Threshold (ToT) measurements
- Measured performance
- Conclusions

Medipix4 collaboration

- **Medipix4 Collaboration is set to provide the next generation of Medipix family chips (Medipix4 and Timepix4):**
  - Agreement signed on May 2016
  - 19 collaboration members
- **Timepix4 (2019)**
  - 65nm technology
  - Pixel matrix of **512 x 448 pixels** (55 x 55 μm^2)
  - Particle identification and tracking (Data-driven and zero suppressed)
  - Sub-ns time binning
  - X-ray Imaging (full frame based with CRW sequential readout)
  - Improved energy resolution
- **Medipix4 (2022)**
  - 130nm technology
  - Pixel matrix of 320 x 320 (75 x 75 μm^2) or 160 x 160 (150 x 150 μm^2)
  - Charge Summing architecture
- **Both chips have a 4-side buttable architecture:**
  - Periphery integrated inside the pixel matrix
  - **Prepare for readout using TSV (Through-Silicon-Vias)**
  - **Larger ASICs**

- **CEA, Paris, France**
- **CERN, Geneva, Switzerland**
- **DESY, Hamburg, Germany**
- **Diamond Light Source, England, UK**
- **IEAP, Czech Technical University, Prague, Czech R.**
- **IFAE, Barcelona, Spain**
- **JINR, Dubna, Russian Federation**
- **NIKHEF, Amsterdam, The Netherlands**
- **University of California, Berkeley, USA**
- **University of Canterbury, Christchurch, New Zealand**
- **University of Geneva, Switzerland**
- **University of Glasgow, Scotland, UK**
- **University of Houston, USA**
- **University of Maastricht, The Netherlands**
- **University of Oxford, England, UK**
- **INFN, Italy**
- **LNLS, Brazil**
- **CSNS, China**
- **PNRI, Philippines**

Expected global parameters

			Timepix3 (2013)	Timepix4 (2019)
Technology			130nm – 8 metal	65nm – 10 metal
Pixel Size			55 x 55 µm	55 x 55 µm
Pixel arrangement			3-side buttable 256 x 256	4-side buttable 512 x 448
Sensitive area			1.98 cm^2	6.94 cm^2
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA	
		Event Packet	48-bit	64-bit
		Max rate	0.43×10^6 hits/mm²/s	**3.58×10^6 hits/mm²/s**
		Max Pix rate	1.3 KHz/pixel	**10.8 KHz/pixel**
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)
		Max count rate	~0.82 x 10^9 hits/mm²/s	~5 x 10^9 hits/mm²/s
TOT energy resolution			< 2KeV	**< 1Kev**
TOA binning resolution			1.56ns	**195ps**
TOA dynamic range			409.6 µs (14-bits @ 40MHz)	**1.6384 ms** (16-bits @ 40MHz)
Readout bandwidth			≤5.12Gb (8x SLVS@640 Mbps)	**≤163.84 Gbps (16x @10.24 Gbps)**
Target global minimum threshold			<500 e^-	<500 e^-

Timepix4 submissions

Q4 2019

Timepix4v0

Full mask engineering run

6 wafers received

Chip is operational

1) Excess noise coupling from peripheries to FE
2) 640 MHz clock in edge peripheries
3) VCO not oscillating at nominal frequency

Q3 2020

Timepix4v1

4 BEOL masks changed

Small test VCO chip

6 wafers received

1) Improved RDL shielding in peripheries
2) 640MHz in peripheries recovered

1) VCO not oscillating at nominal frequency

Q2 2021

Timepix4v2

4 FEOL + 4 BEOL masks changed

19 wafers received

1) TDC and High speed links working as expected
2) Further improvement in RDL shielding in peripheries

Chip at its final version

Q3 2022

Timepix4v3

2 BEOL masks changed

25 wafers received

1) Larger IO Pads

Chip at its final version

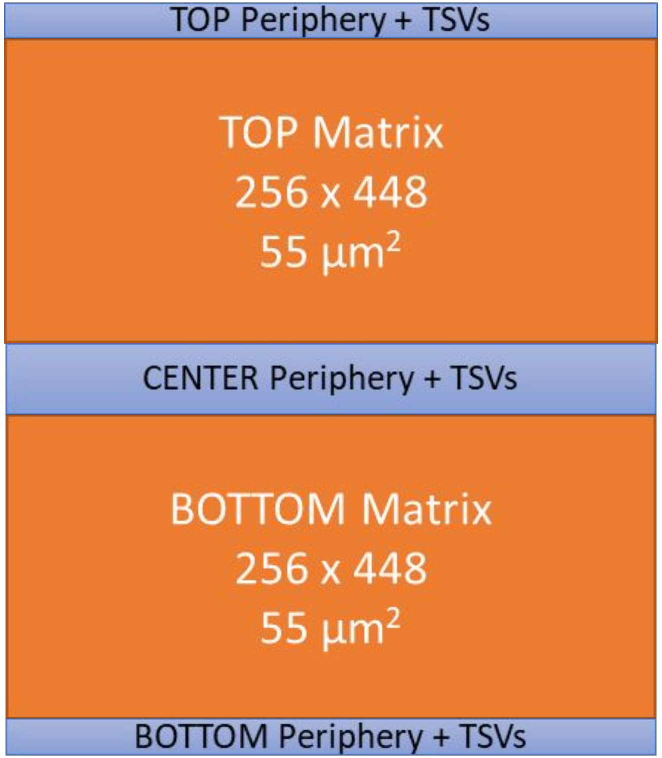
Potential applications of Timepix4 ASIC

- **Particle tracking:**
    - very high rate pixel telescope
    - sensor studies with < 100 ps timing resolution and ~10 μm spatial resolution
    - Time-of-flight mass spectroscopy
    - Radiation monitors
    - Compton camera
    - Gamma and neutron imaging
    - X-ray imaging
- **Frame-based imaging:**
    - X-ray imaging in synchrotrons with very high rates (> 10^9 particles/mm^2/s)

Timepix4 arrangement: TSV, Wire bonds

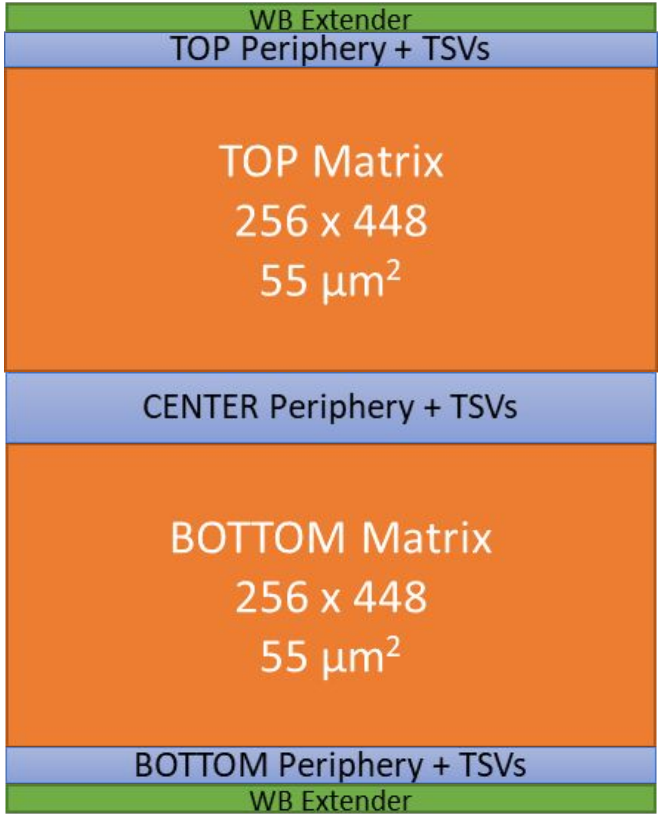
- 2 matrices: TOP and BOTTOM
  - 256 x 448 pixels each

Timepix4 arrangement: TSV, Wire bonds



- 2 matrices: TOP and BOTTOM
  - 256 x 448 pixels each
- 3 peripheries:
  - TOP and BOTTOM: data readout (16 x 10.24 Gbps serializers)
  - CENTER: analog blocks (global DACs and ADCs, …)

Timepix4 arrangement: TSV, Wire bonds



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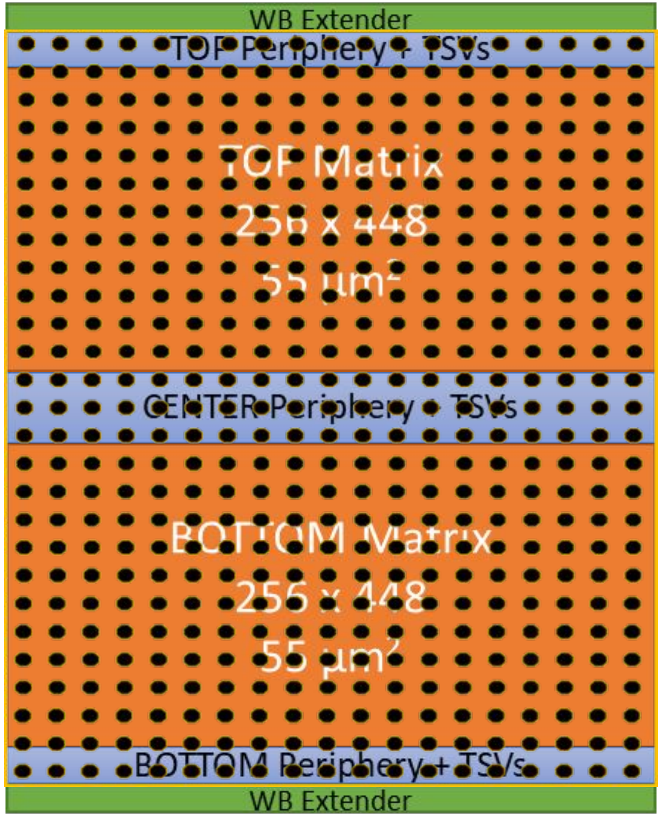

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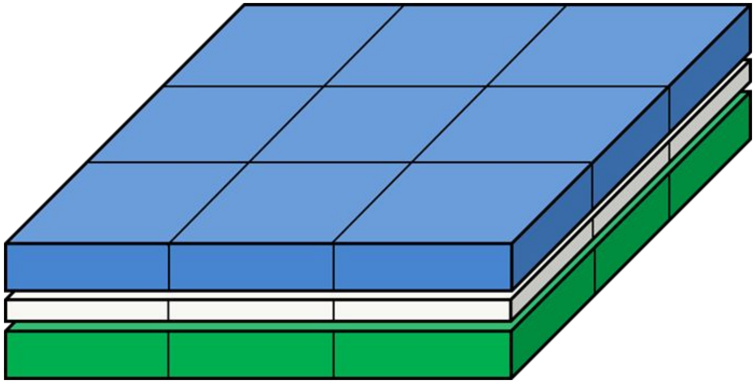
- 2 wire bond extenders on edge peripheries
- Through-Silicon-Via compatible
  - 4-side buttable
  - possibility to place several chips adjacent to cover larger detectors
- Dicing options:
  - with wire bonds: ∼93.7 % active area
  - with TSV: ∼99.5 % active area

Timepix4 arrangement: TSV, Wire bonds



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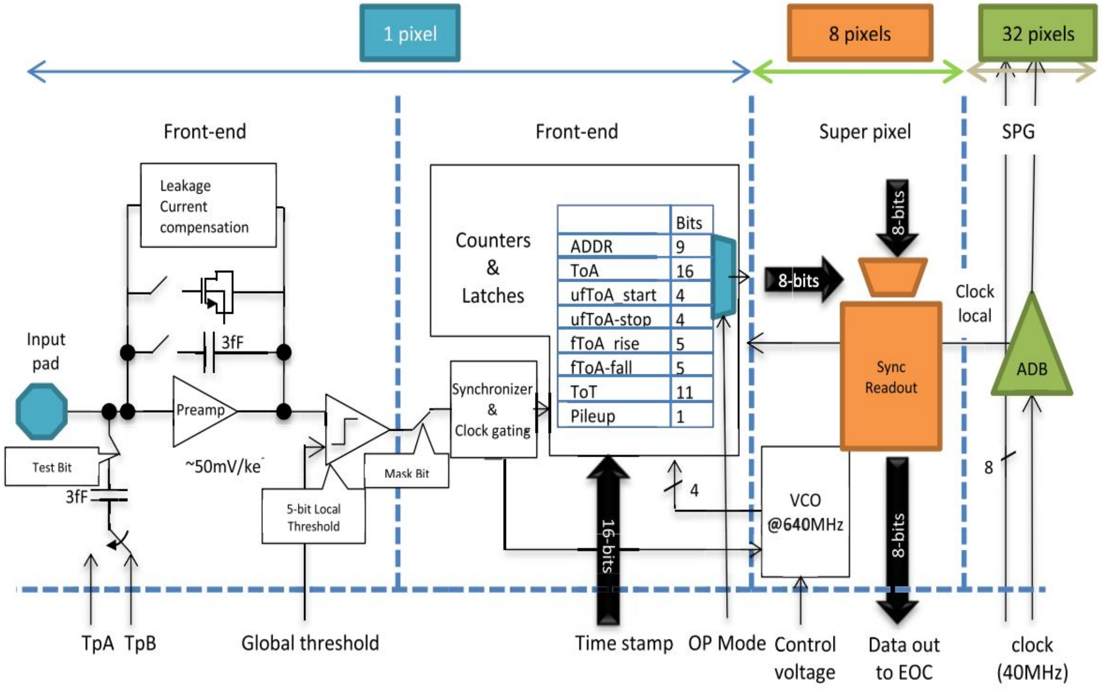
Analog and digital front-end

- Pixel level:
  - analog front-end:
    - pixel enable
    - input pad
    - charge integration circuit
    - local threshold
    - local test pulse
  - digital front-end:
    - pixel mask
    - TDC and time stamp
- SP level:
  - VCO
  - pixels readout
- SPG level:
  - Adjustable Delay Buffer, to correctly distribute the reference clock to the pixels across the double column



[X. Llopart *et al* 2022 *JINST* **17** C01044]

Readout modes: data driven

- Event-based readout
- Zero-suppressed
- 2 acquisition modes:
    - 24-bit photon counting:
        - pixel coordinates
        - photon counting per pixel

Address: 18 bits →

Photon counting: 24 bits →

PC24bit mode packets specification		
Name	**Width**	**Bits used**
Top	1	[63:63]
EoC	6	[62:55]
SPGroup	4	[54:51]
Spixel	2	[50:49]
Pixel	3	[48:46]
UNUSED	22	[45:24]
Event Count	24	[23:0]

Readout modes: data driven

- Event-based readout
- Zero-suppressed
- 2 acquisition modes:
  - 24-bit photon counting:
    - pixel coordinates
    - photon counting per pixel
  - ToA-ToT mode:
    - pixel coordinates
    - timestamp
    - charge

ToA/ToT mode packets specification		
Name	**Width**	**Bits used**
Top	1	[63:63]
EoC	6	[62:55]
SPGroup	4	[54:51]
Spixel	2	[50:49]
Pixel	3	[48:46]
ToA	16	[45:30]
ufToA_start	4	[29:26]
ufToA_stop	4	[25:22]
fToA_rise	5	[21:17]
fToA_fall	5	[16:12]
ToT	11	[11:1]
Pileup	1	[0:0]

Time: 29 bits

Charge: 21 bits

Readout modes: data driven

- Event-based readout
- Zero-suppressed
- 2 acquisition modes:
  - 24-bit photon counting:
    - pixel coordinates
    - photon counting per pixel
  - ToA-ToT mode:
    - pixel coordinates
    - timestamp
    - charge
- 64-bit packets for each event, encoded with Aurora 64b/66b standard encoding communication protocol
- Output via:
  - slow control: 40 Mb/s (2.6 Hz/pixel)
  - high speed links: from 40 Mb/s to 160 Gb/s (10.8 kHz/pixel)

ToA/ToT mode packets specification		
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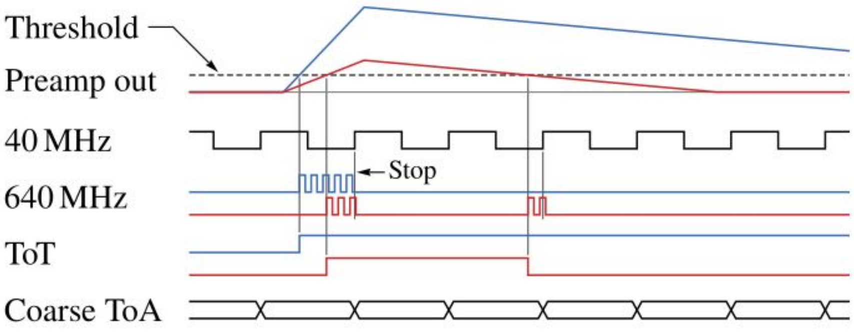
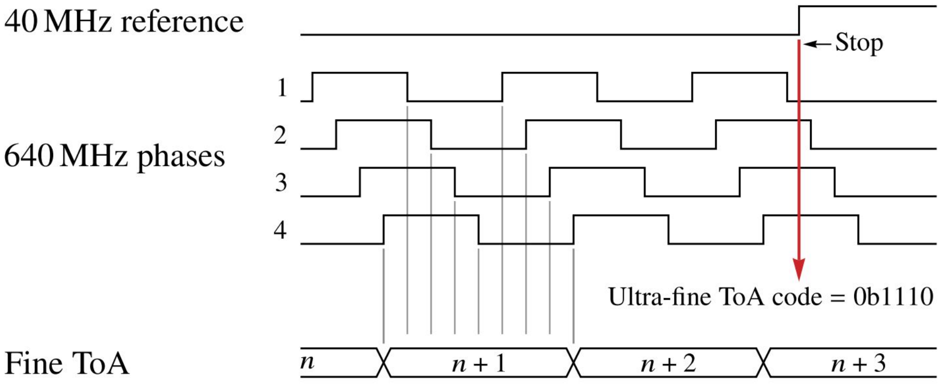
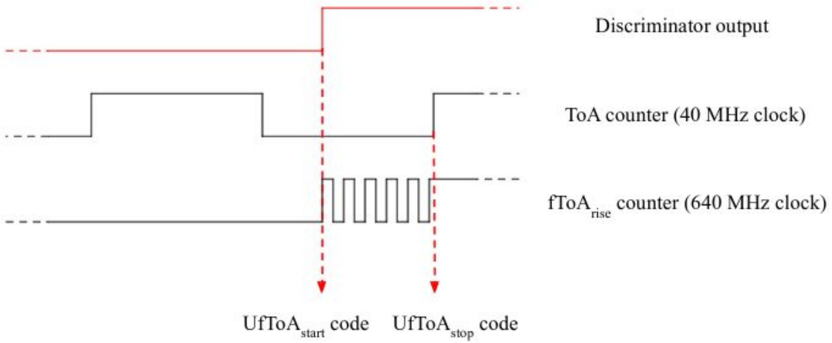
ToT	11	[11:1]
Pileup	1	[0:0]

ToA and ToT measurements

- ToA measurement:
  - coarse Time-of-Arrival (ToA), **40 MHz clock** (25 ns bins width)
  - fine-ToA bins, **640 MHz clock**, generated by the VCO (**1.56 ns bins width**)
  - Ultrafine-ToA, by 4 copies of 640 MHz clock (**195 ps bins width**)
- ToT measurements: only coarse and fine



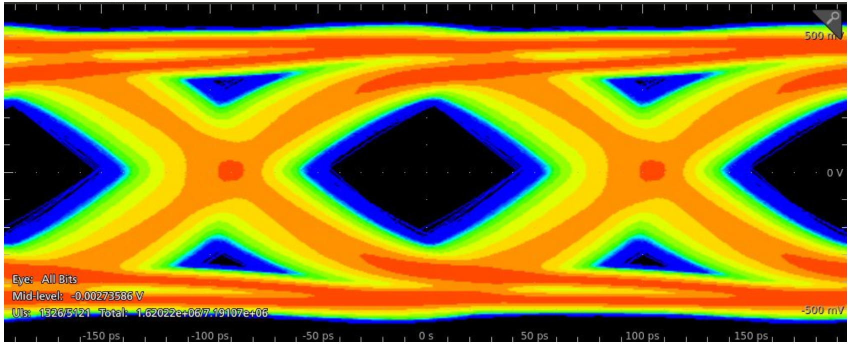


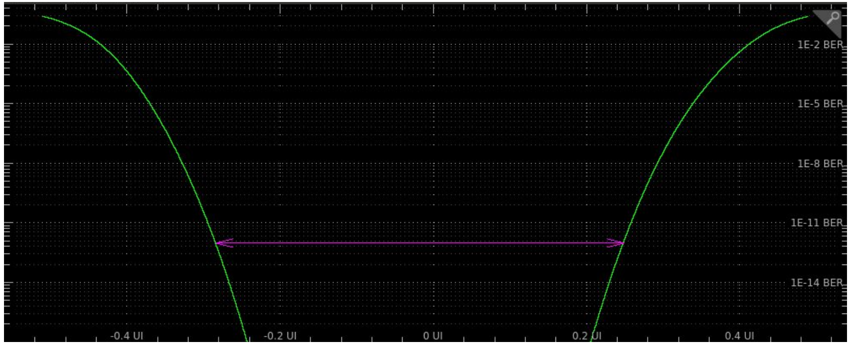


[K. Heijhoff *et al* 2022 *JINST* 17 P07006]

High-speed readout

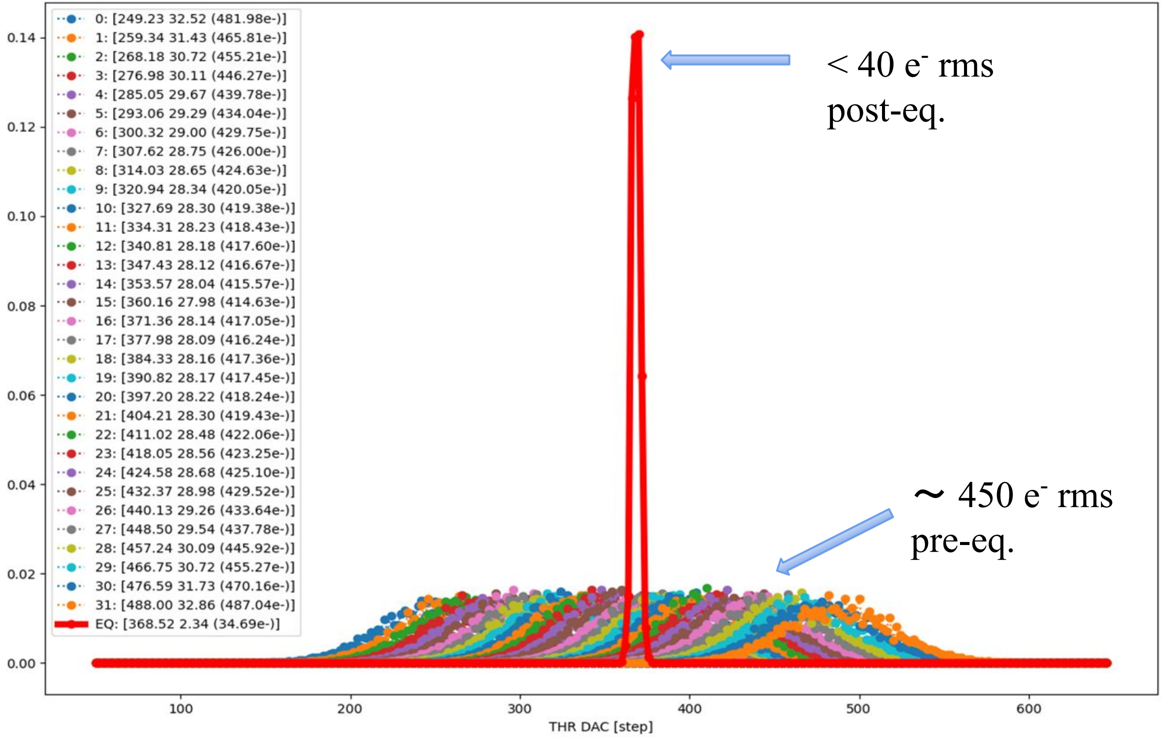
- Gigabit Wireline Transmitter with a Clock Cleaner (GWT-CC):
  - serializes data stream
  - transmits data to an off-chip receiver
- High configurability:
  - each link can be configured to operate at different speed, from 40 Mb/s to 10.24 Gb/s
  - possible to use from 1 to 8 links per half-matrix
- Max bandwidth of 160 Gb/s
- PRBS generator for links tests
- Tested up to 5.12 Gb/s, both with WB and TSV connection
- Timepix4 and control board links alignment and physics measurement performed only @ 2.56 Gb/s





Timepix4 threshold equalization and noise

- ➢ Threshold equalization:
  - ○ 24-bit photon counting mode
  - ○ global threshold shifted using 5-bit local DAC
  - ○ just few pixel masked
  - ○ threshold distribution from ∼450 e^- r.m.s. pre-equalization to < 40 e^- r.m.s. post-equalization



X. Llopart (CERN)

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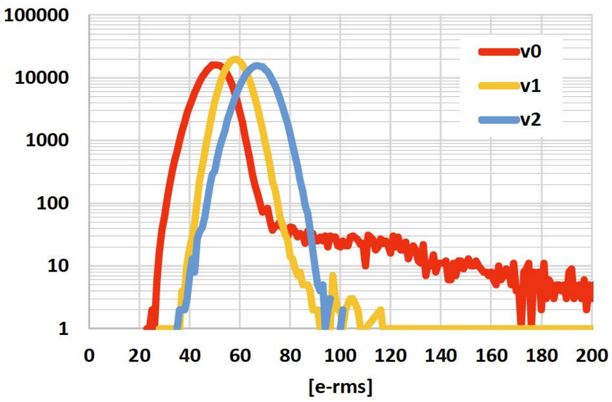
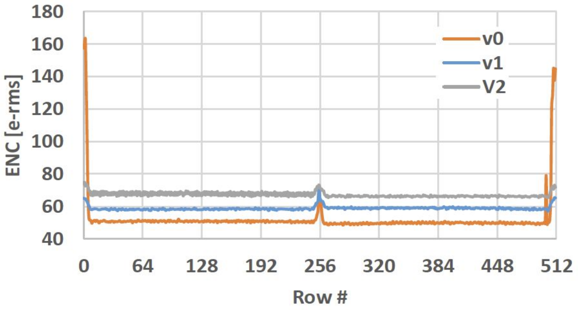
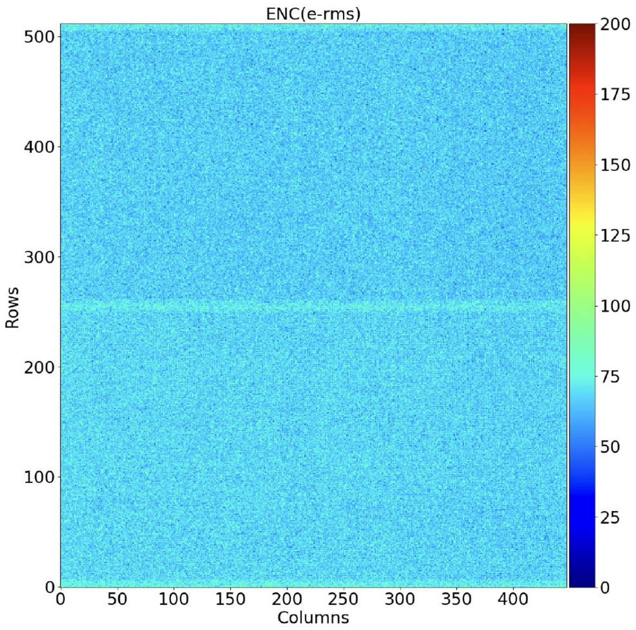
- ➢ Threshold equalization:
  - ○ 24-bit photon counting mode
  - ○ global threshold shifted using 5-bit local DAC
  - ○ just few pixel masked
  - ○ threshold distribution from ∼450 e⁻ r.m.s. pre-equalization to < 40 e⁻ r.m.s. post-equalization
- ➢ Noise after equalization:
  - ○ ENC average of ∼70 e⁻ r.m.s.



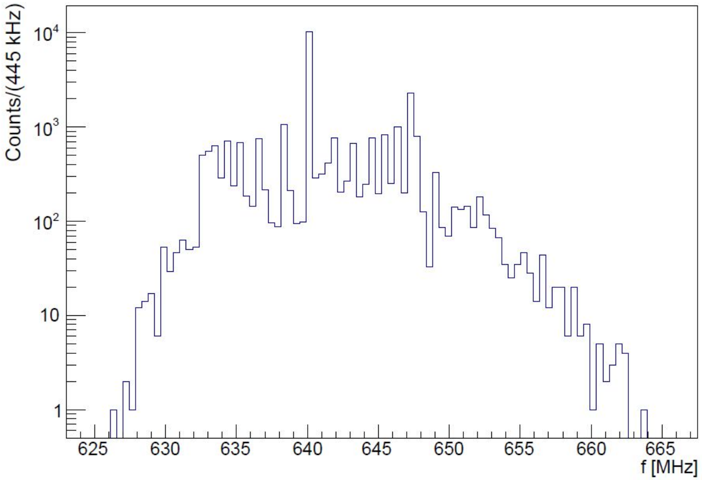


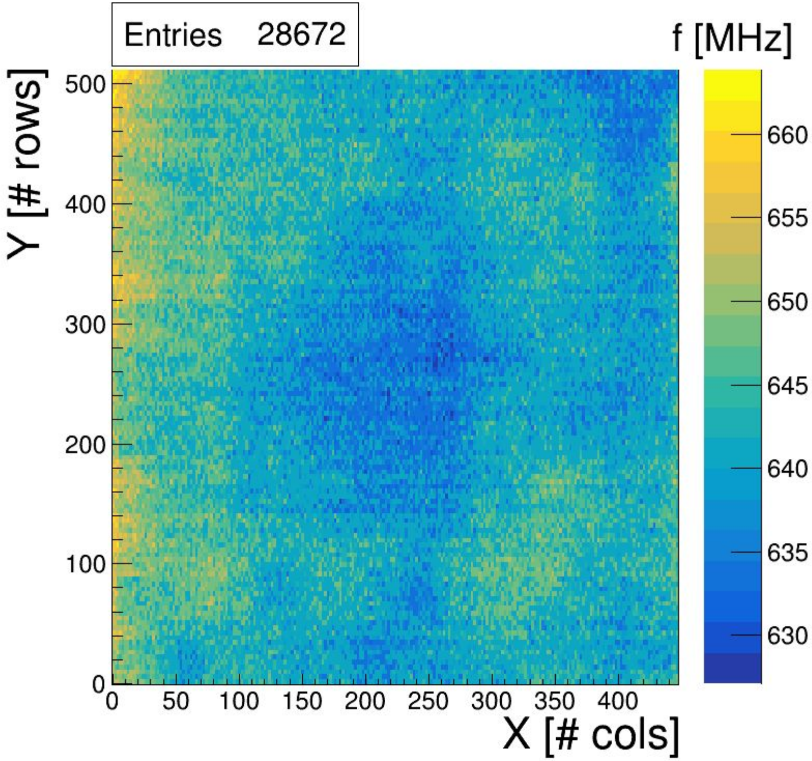


X. Llopart (CERN)

Timepix4 characterization measurements - VCO calibration

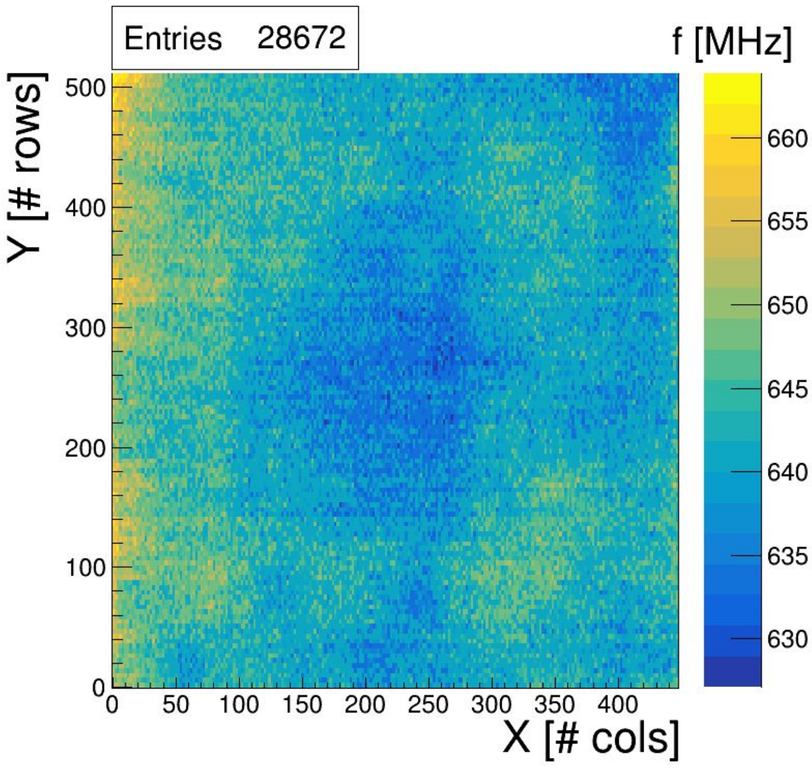
- On pixel VCO oscillation frequency controlled by a PLL at the center of the chip (@ 640 MHz nominal)
- It has been measured that on pixel VCO oscillate around 640 MHz with a spread of around 40 MHz





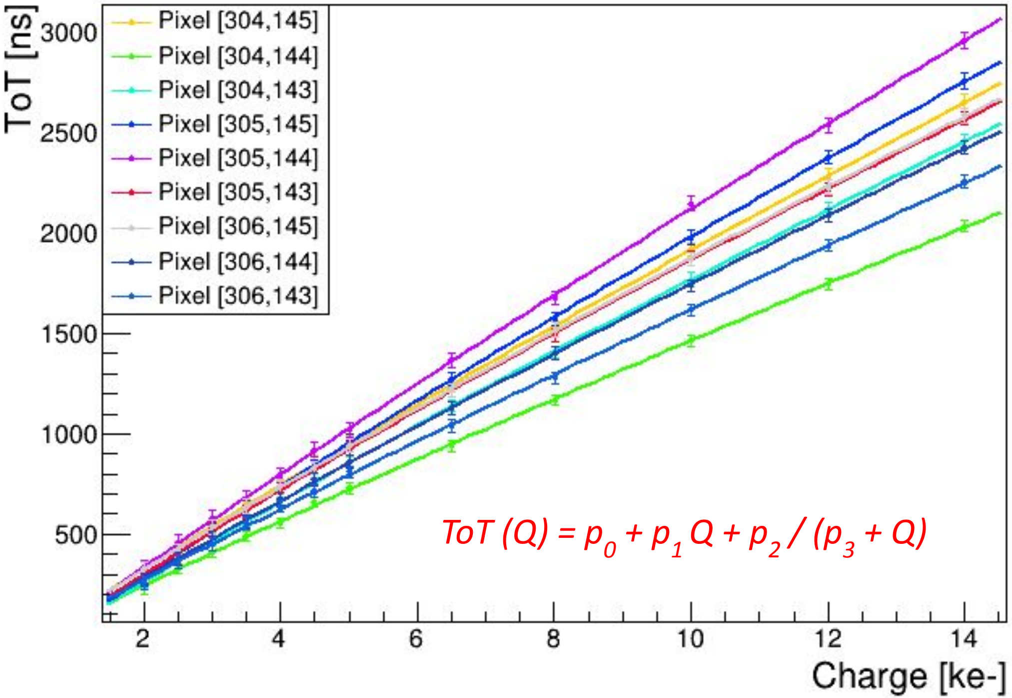
Timepix4 characterization measurements - VCO calibration

- On pixel VCO oscillation frequency controlled by a PLL at the center of the chip (@ 640 MHz nominal)
- It has been measured that on pixel VCO oscillate around 640 MHz with a spread of around 40 MHz
- Spread caused by power supply dispersion due to large size and wire bonds: large improvements expected with TSV
- Finer ToA bins generated with different width
- Timing performances heavily affected by this effect
- Internal test pulse tool exploited to **calibrate VCO frequencies for the whole matrix (28672 VCO)**



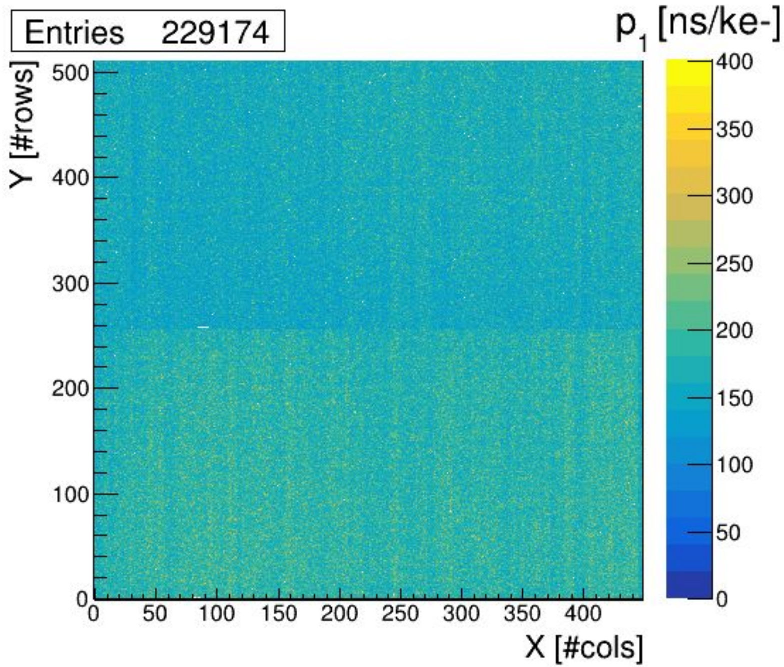
ToT vs Q calibration

- Analog testpulse
- **Non linear** calibration
- Threshold set to 1 ke^-
- Per-pixel calibration done over the whole matrix



ToT vs Q calibration

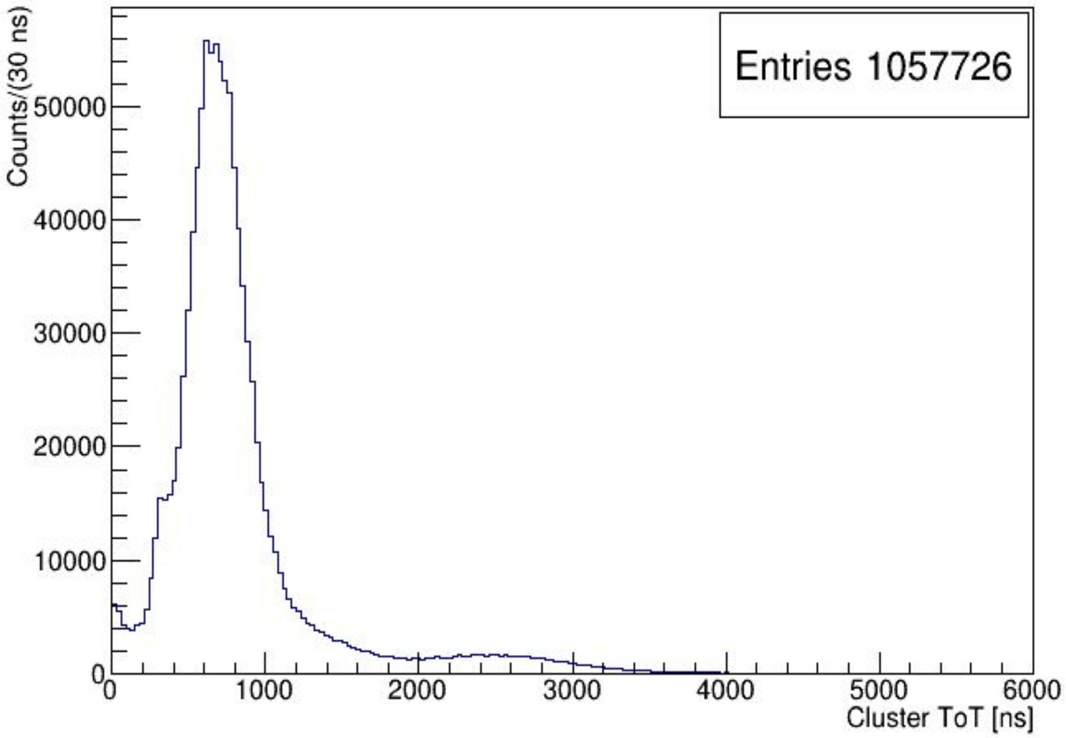
- Analog testpulse
- **Non linear** calibration
- Threshold set to 1 ke$^-$
- Per-pixel calibration done over the whole matrix
- Automatic algorithm exploiting fast read-out
- Calibration fit parameters distribution



$$ToT\,(Q) = p_0 + p_1 Q + p_2 / (p_3 + Q)$$

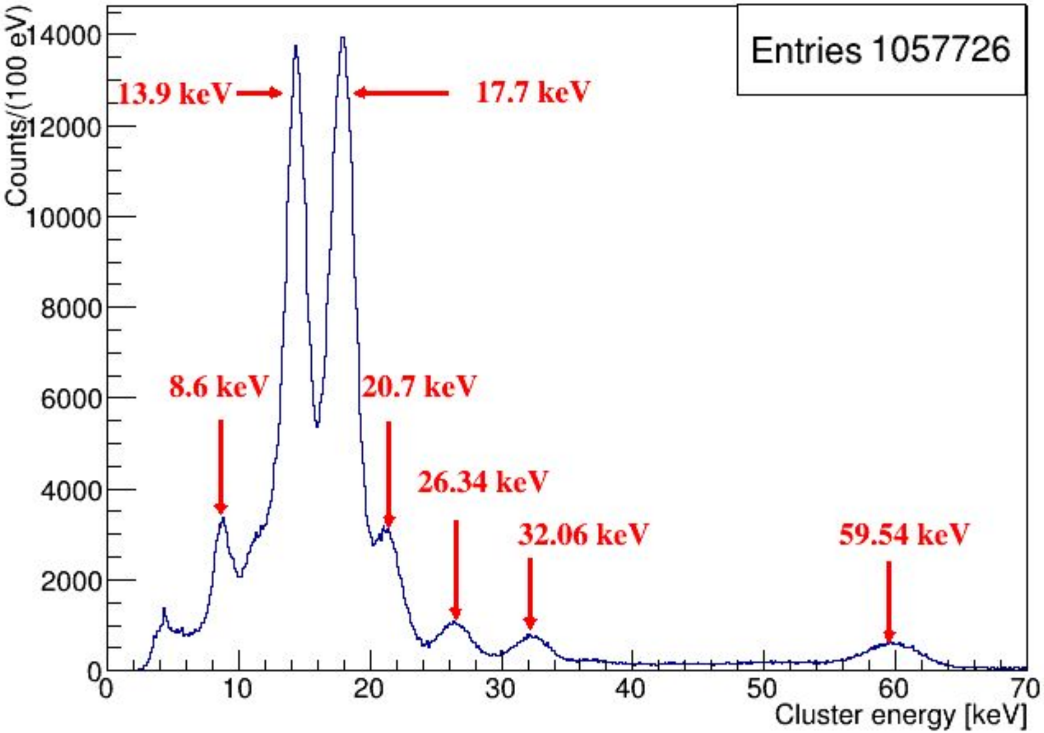
ToT vs Q calibration

- Validation with radioactive sources(^{137}Cs and ^{241}Am superimposed spectra)



ToT vs Q calibration

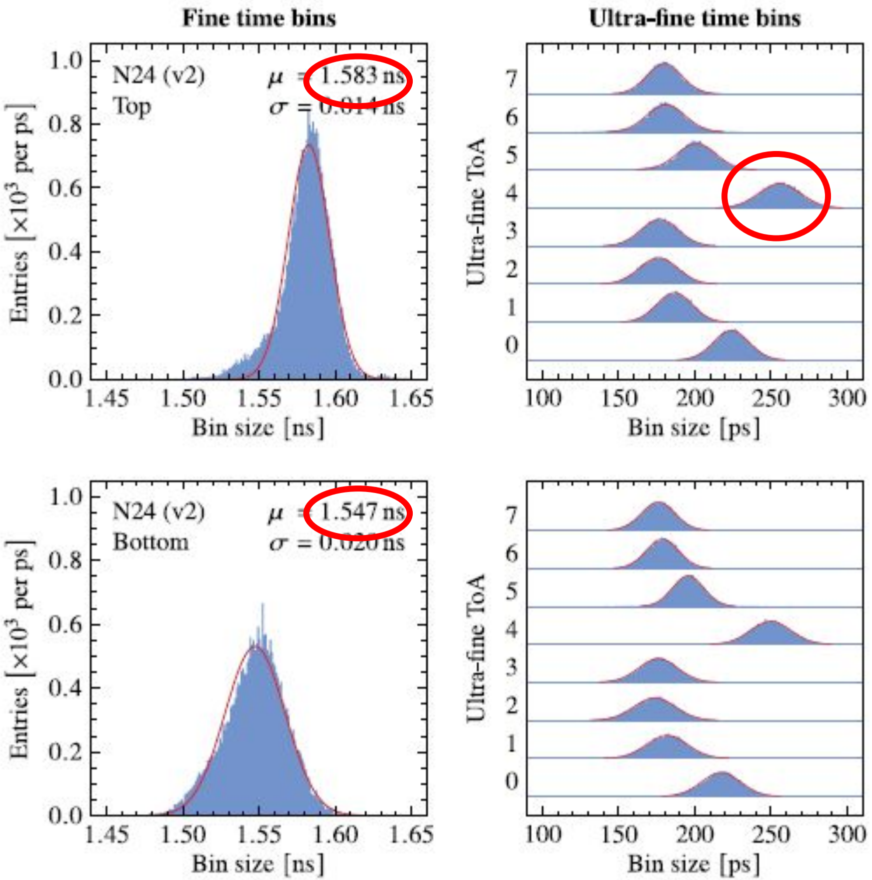
- **Validation with radioactive sources(^{137}Cs and ^{241}Am superimposed spectra)**



- Up to 1.3 keV FHWM (@ 8 keV)
- Resolution up to 8% (@60 keV)
- ASIC bonded to 100 µm n-on-p Si detector

Timing resolution measurements - Time bins sizes measurements

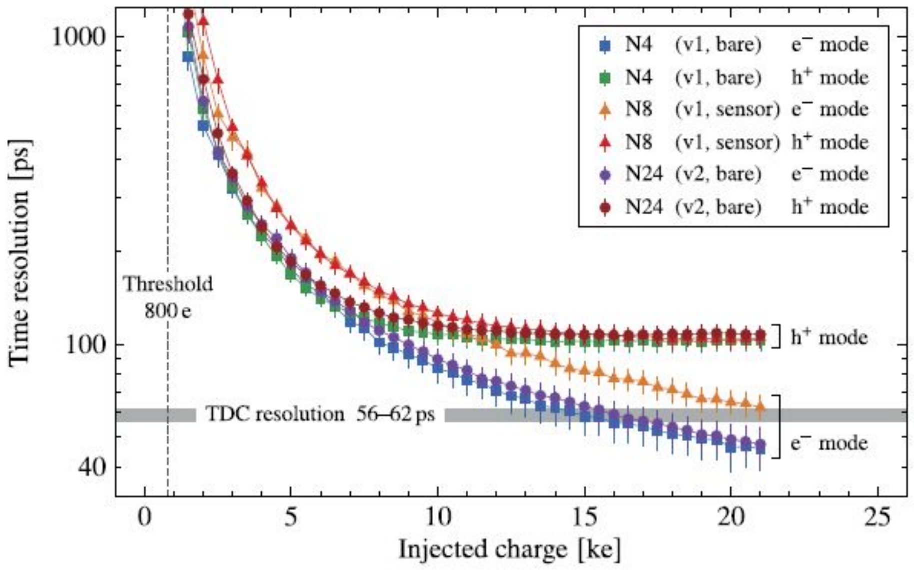
- External testpulse used to measure fToA and UfToA bins width:
  - delay settable up to ps precision
  - signals sent directly to the Timepix4 through digital pixels
- Correct VCO on Timepix4_v2:
  - average fToA bin size: 1.56 ns
  - average UfToA bin size: ~ 195 ps
- Some UfToA bins with much higher size



[K. Heijhoff *et al* 2022 *JINST* 17 P07006]

Timing resolution measurements - Test pulse

- ➢ Analog internal test pulse used to measure the analog front-end jitter
- ➢ Hole-collecting mode:
  - jitter asymptotic to ~100 ps r.m.s.
  - bare Timepix4 and Timepix4 bonded to Si sensor show similar trends
  - at low charge, worst resolution with sensor bonded
- ➢ Electron-collecting mode:
  - no asymptotic trend
  - resolution lower than 50 ps r.m.s. both with bare and bonded chips

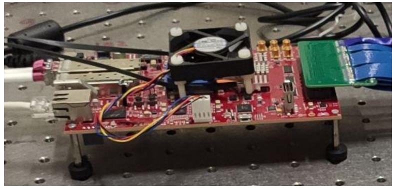


[K. Heijhoff *et al* 2022 *JINST* 17 P07006]

Timing resolution measurements - Laser measurements

- **Spidr4** control board
- **Timepix4v2**:
  - bonded to a 100 µm n-on-p Si detector biased at -150 V
  - metalization with holes pattern
  - Courtesy of CERN and NIKHEF Medipix4/VELO groups
- **Waveform generator**
  - input signal to digital pixels
  - laser trigger
- **Laser**:
  - 1060 nm
  - variable attenuator

Spidr4 control board



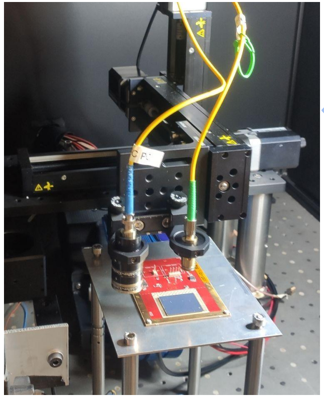
Pulse generator Active Technologies PG-1072 (interchannel jitter ~7 ps r.m.s.)

To digital pixels

Period: 5 ms
Width: 1 µs
Amplitude: 1.9 V

6dB attenuation

Period: 5 ms
Amplitude: 1.2 V



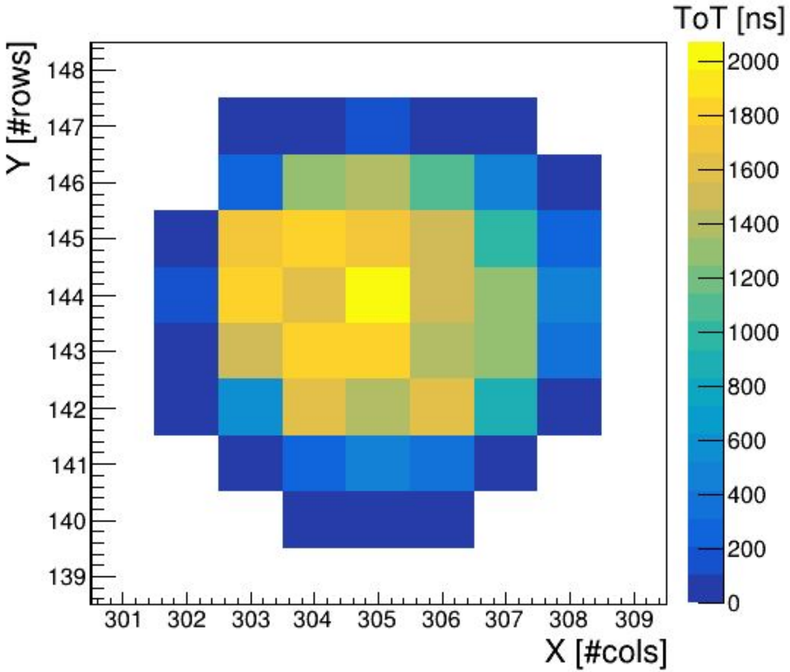
Laser variable Attenuator

Pulsed Diode Laser PDL 800-B

This project has received funding from the European Research Council (ERC) under the European Union’s Horizon 2020 research and innovation programme (4DPHOTON project, grant agreement No. 819627)

Single pixel timing resolution

- **Laser focused using micro-collimator**:
    - σ = 1.4 pixel = 77 µm
- Laser spot in **fixed position** for all presented measurements



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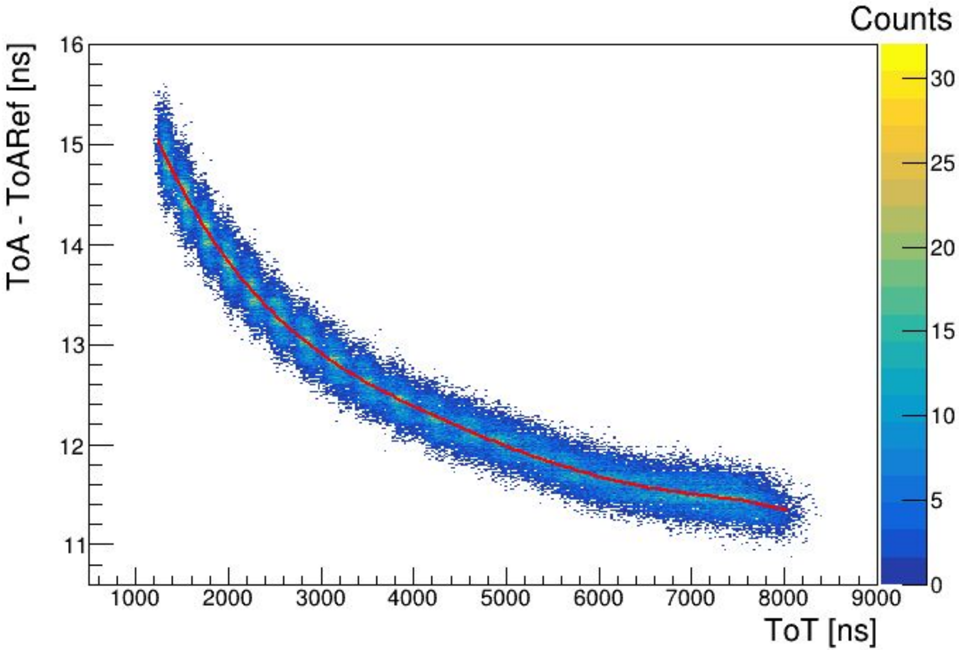
- Measurements using **variable laser attenuation**, populating a wide ToT range on each pixel
- **Different time walk trends** on different pixels
- Time walk corrected separately on each pixel



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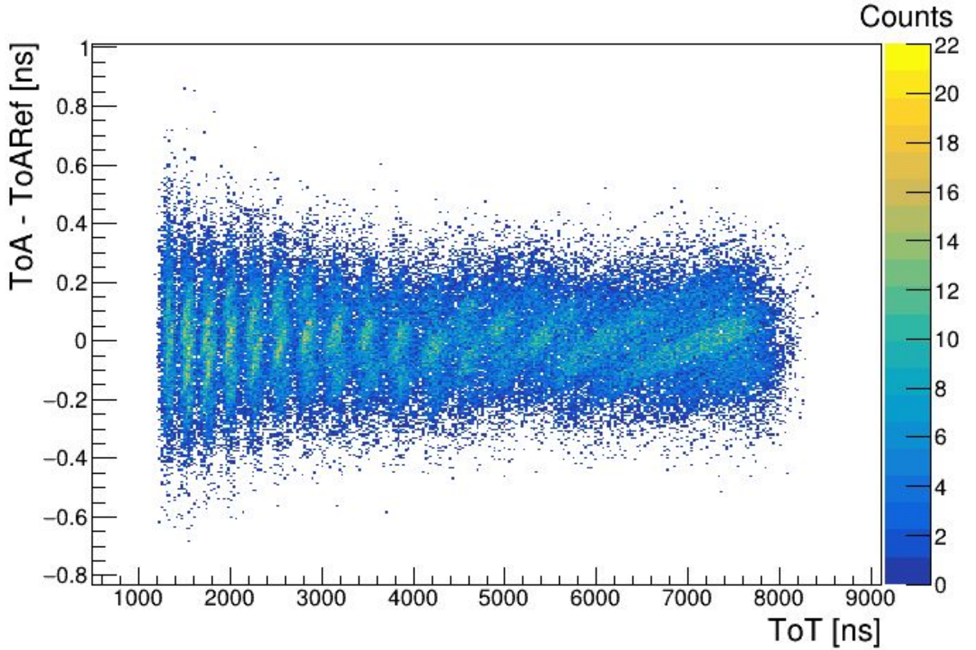
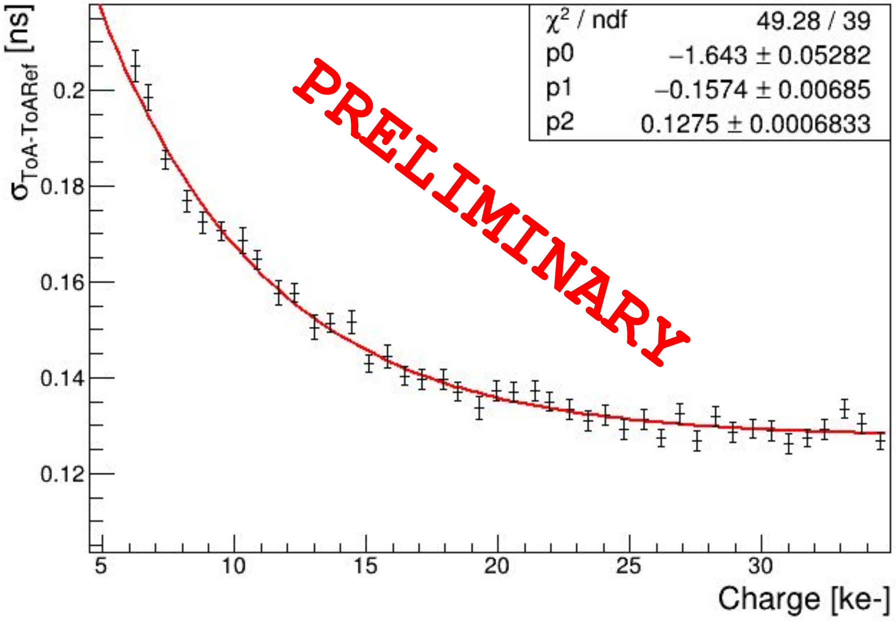


Single pixel timing resolution

$\sigma_{ToA-ToARef}(ToT) = Exp(p_0 + p_1 \cdot ToT) + p_2$



- ➢ ToT vs charge calibration applied to each pixel
- ➢ Distribution of timing resolution as a function of injected charge
- ➢ For the pixel [305,144], where the laser is focused, the standard deviation saturates at 128±1 ps rms
- ➢ Subtracting the contribution of the reference TDC (60 ps), a resolution of 111±1 ps rms is obtained

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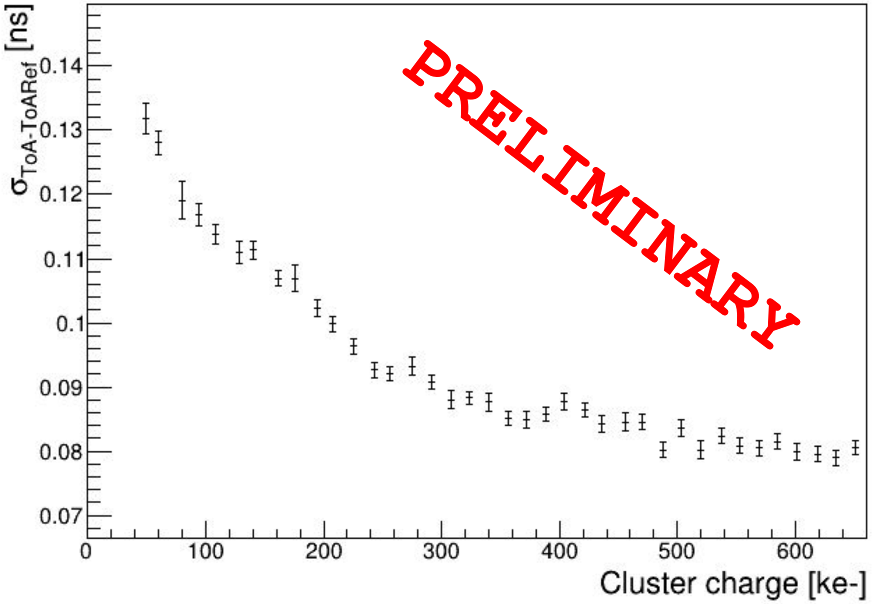
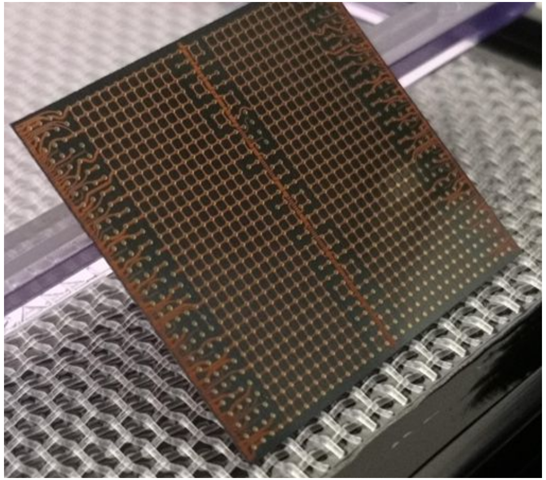
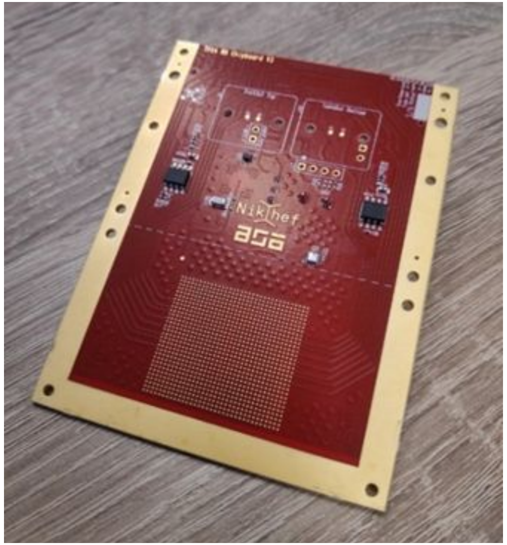
Cluster timing resolution

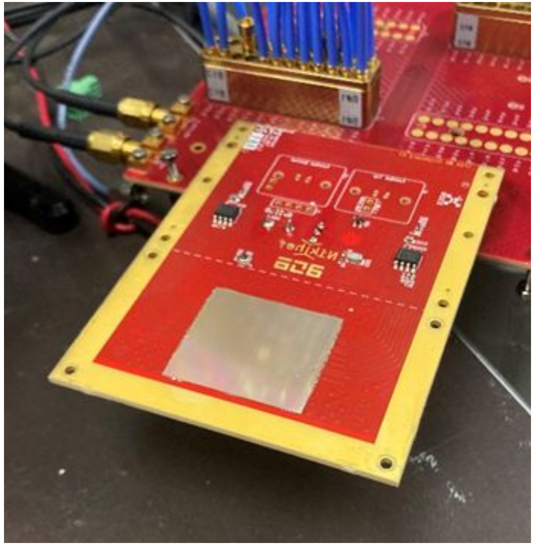
- For each cluster:
  - **weighted average** of ToA using charge as weights
  - cluster charge computed
- Timing resolution dependency on cluster charge:
  - best result: $\sigma_{ToADiffAvg}$=79 ± 1 ps rms
    - timing resolution subtracting reference TDC contribution: σ_{ToAAvg}=49 ± 1 ps rms



Through-Silicon Via first tests with Timepix4v0 in IZM (Germany)

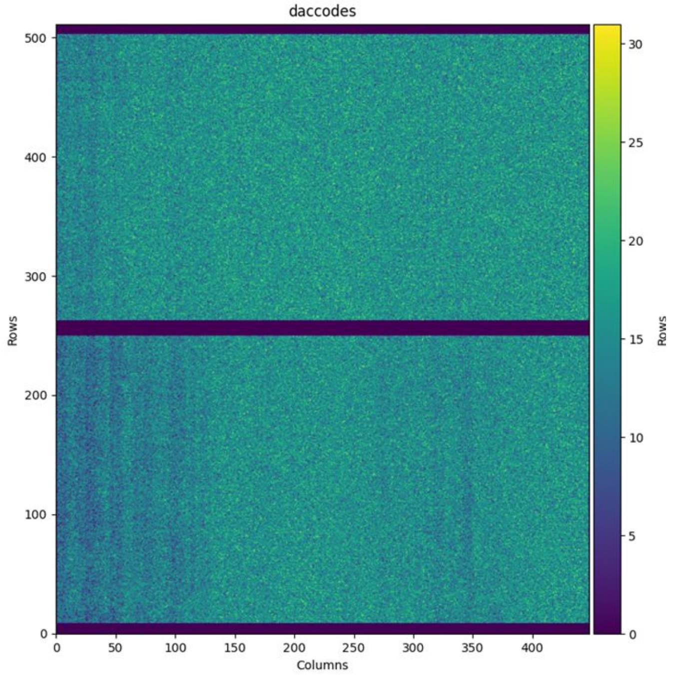
- ➢ First Timepix4v0 samples received on June 2023 (43 TSV ASICs received)
- ➢ IZM to finish remaining 2 Timepix4v1 wafers and 3 Timepix4v2
- ➢ First devices mounted on Nikhef TSV chipboard (with 2 different bonding methods)

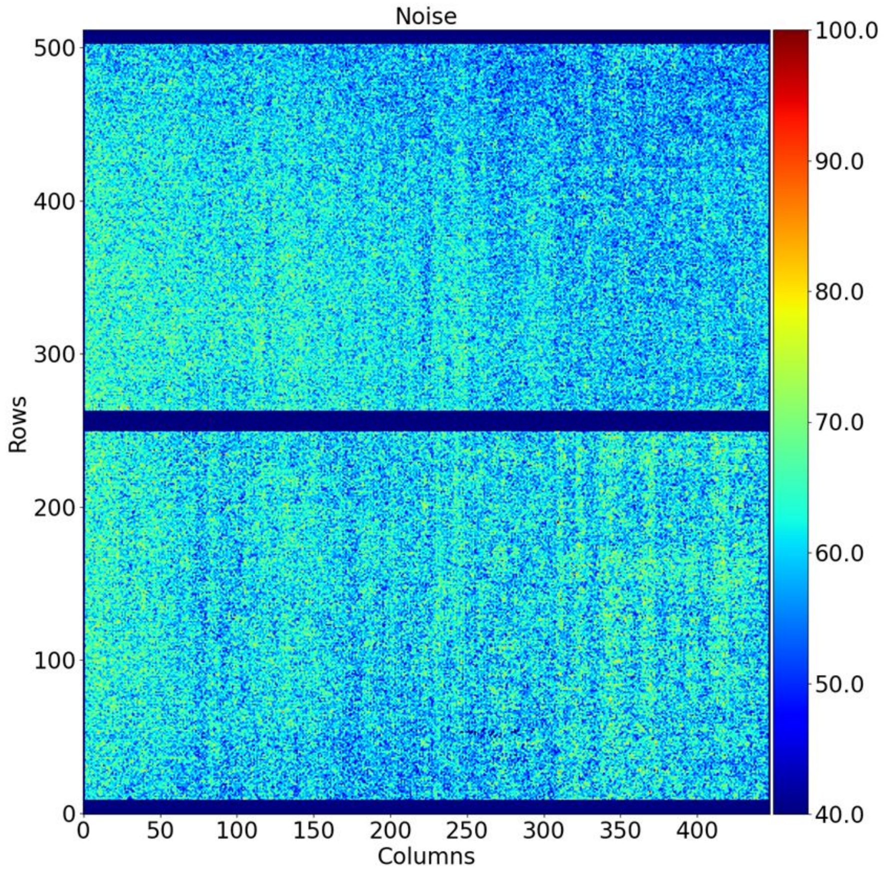





Through-Silicon Via first tests with Timepix4v0 in IZM (Germany)

- First tests very promising, with both the bonding techniques:
  - chip equalized
  - average ENC of ∼60 e^- r.m.s.
  - fast links locking at 5.12 Gb/s





Conclusions

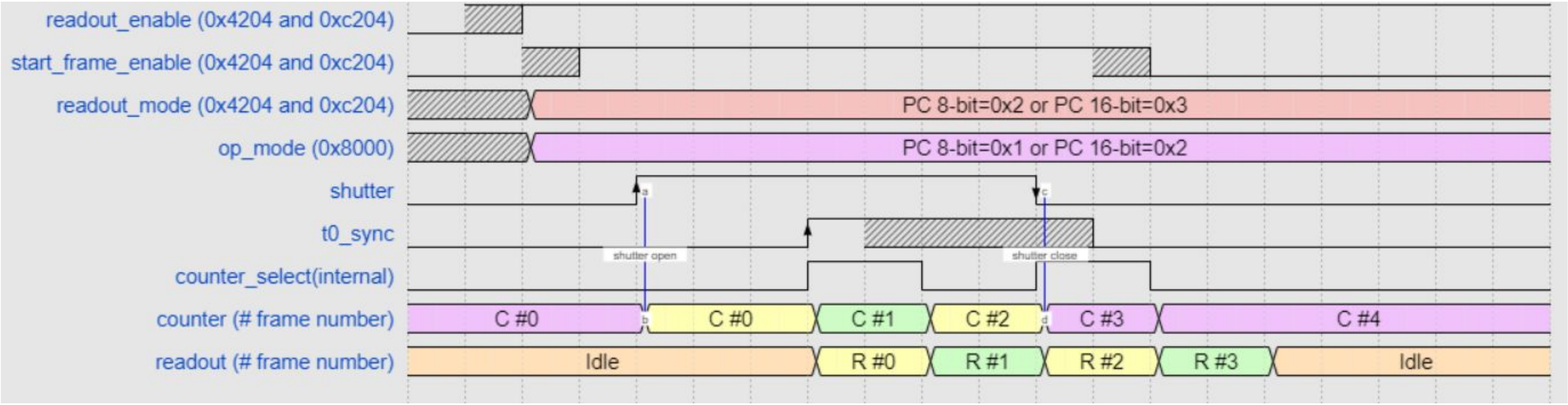
- Timepix4:
  - new hybrid pixel detector for tracking and imaging developed by the Medipix4 collaboration
- Characteristics:
  - large active area: 6.94 cm^2
  - 4-side buttable architecture
  - ToA: 1.6 ms dynamic range; 195 ps bin size
  - ToT: 1.56 ns bin size (~200 e^- rms charge resolution)
  - Frame-based PC: 8-bit or 16-bit, up to $5x10^9$ hits/mm^2/s
  - Readout: up to 160 Gb/s, encoded 64b/66b
- Performance:
  - energy calibration with Timepix4v2 bonded to 100 µm n-on-p Si detector, with resolution up to 8% (@ 60 keV) and FWHM up to 1.3 keV (@ 8.6 keV)
  - timing resolution measured with internal analog testpulse ~40 ps on single pixel
  - timing resolution measured with laser with Timepix4 bonded to 100 µm n-on-p Si detector biased at -150 V: ~110 ps on single pixels and ~50 ps on clusters
- Next steps:
  - characterization with TSV processed wafers and TSV compatible chipboard (NIKHEF)
  - several DAQs being designed by members of the collaboration


THANK YOU
FOR YOUR ATTENTION
0
100
200
300
400
500
0
50
100
150
200
250
300
350
400

Backup

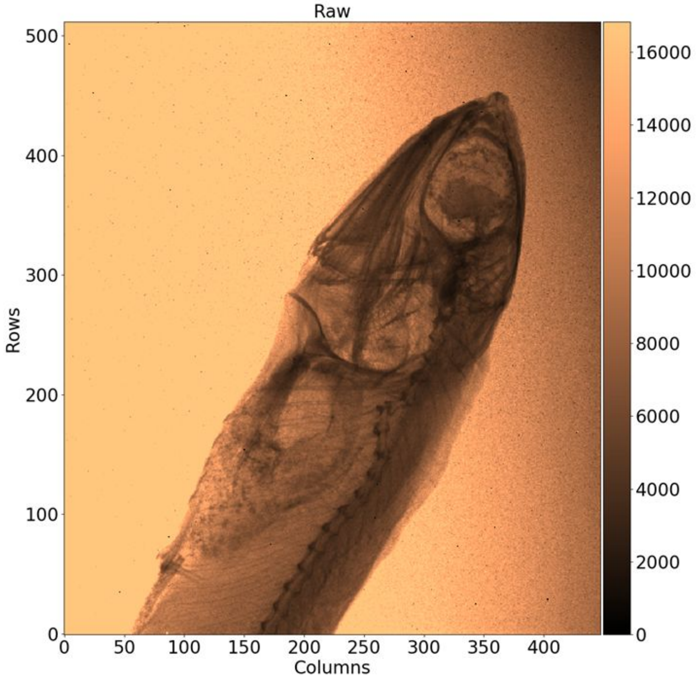
Readout modes: frame based

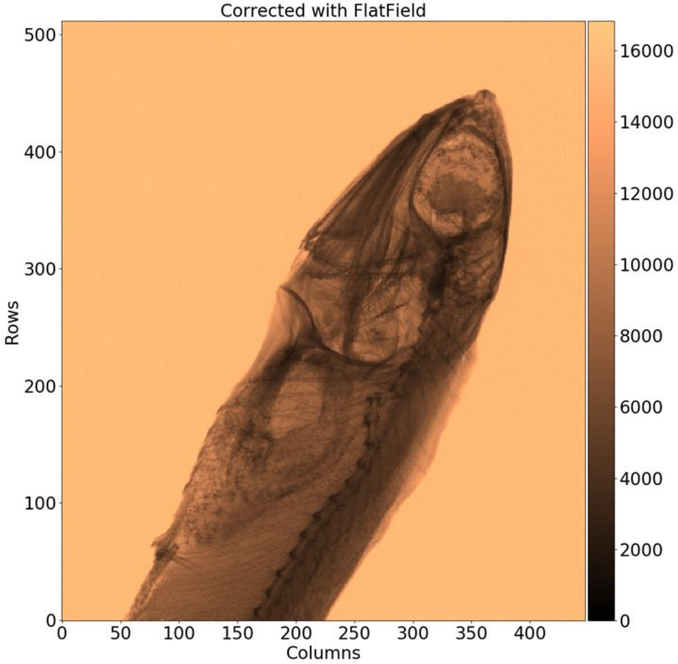
- Photon counting information
- 2 counter depths modes:
  - 8-bit
  - 16-bit
- Full frame readout
- Max count rate (with 16 high speed links enabled): ~5 x 10^9 hits/mm/s^2



Readout modes: frame based

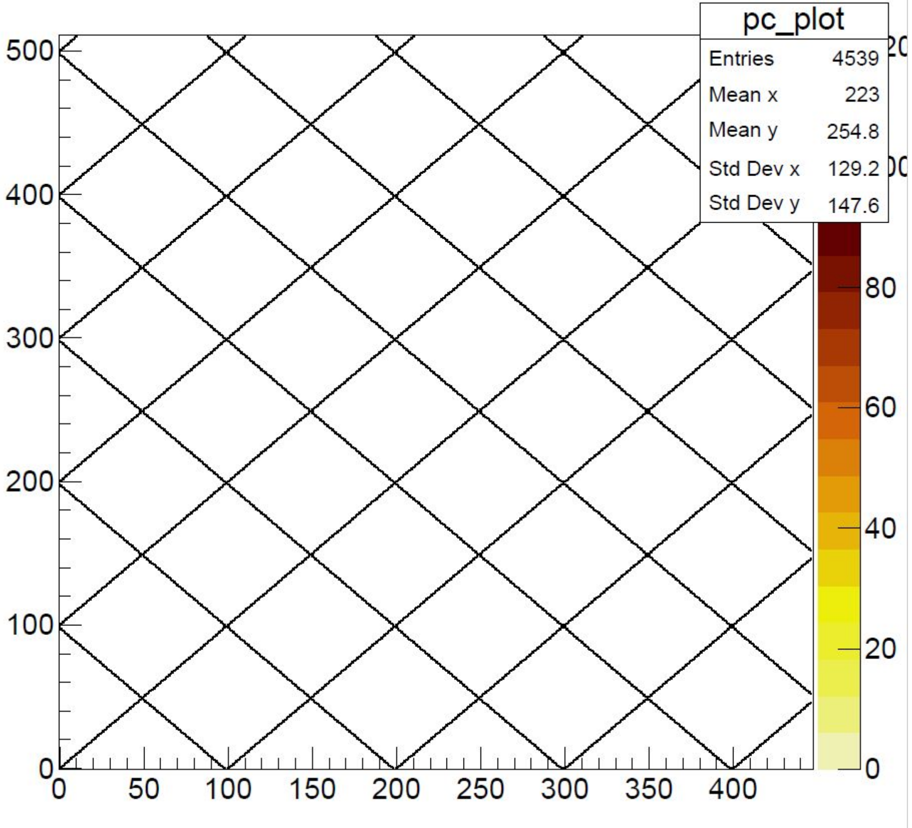
- Timepix4v1 with 300 μm Si sensor
- CRW 16 bit frame based
- X-ray source (s2 acquisition)





Readout modes: frame based

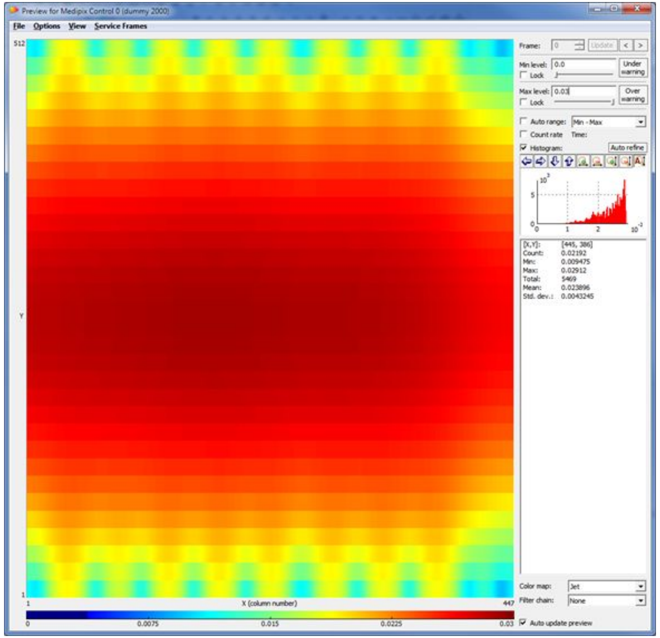
- ➢ Frame based through high-speed links implemented
- ➢ Up to now tested only with internal testpulse
- ➢ Both 8-bit and 16-bit modes tested

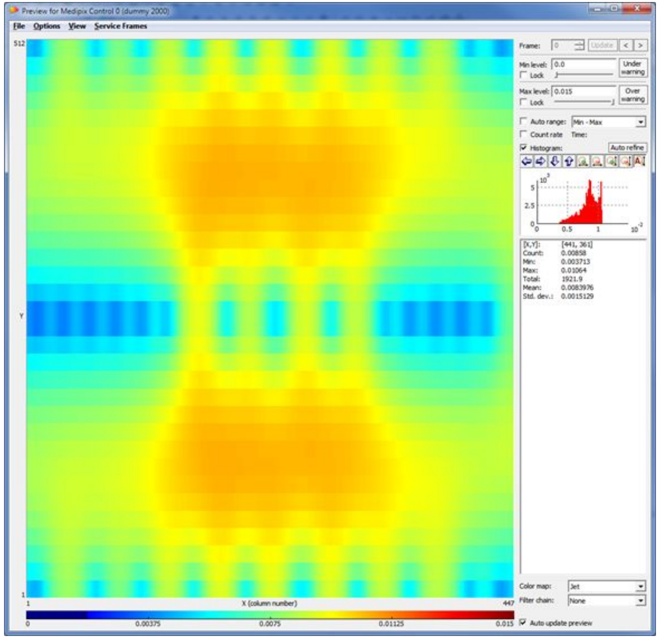


Analog power supply distribution

	Total I (chip)		2 WB	3 TSV
Nominal Analog Power [10 µA/pixel]	~2300 mA	V_{drop} [VDDA-GNDA]	19.6 mV	6.9 mV
		Imax pad	60 mA	57 mA
Low Analog Power [1 µA/pixel]	~230 mA	V_{drop} [VDDA-GNDA]	1.96mV	0.69mV
		Imax pad	6 mA	5.7 mA

2 Wire bonds



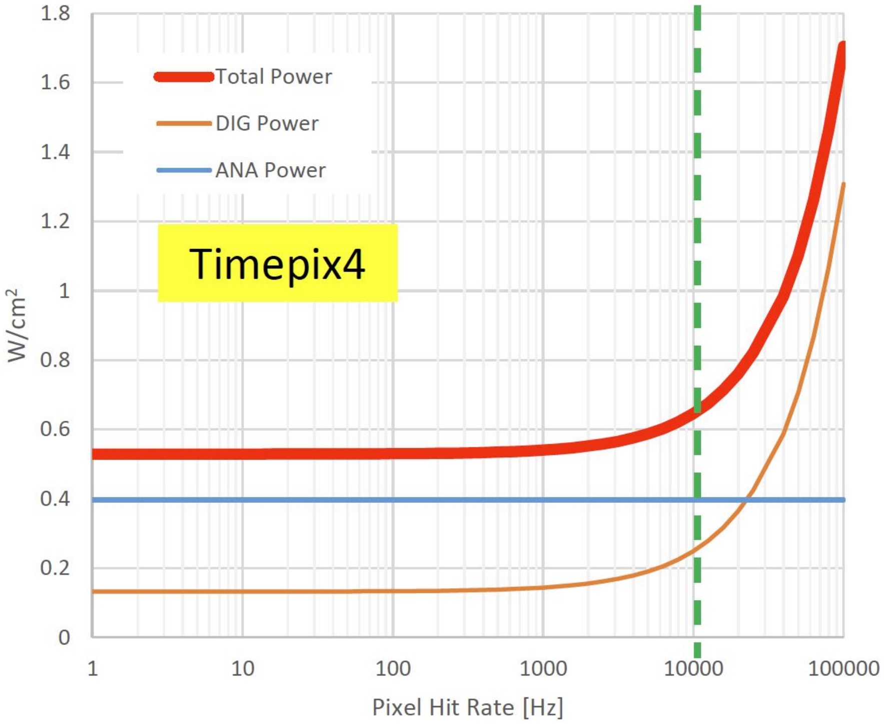


3 TSV

X. Llopart (CERN)

Digital power consumption and cooling

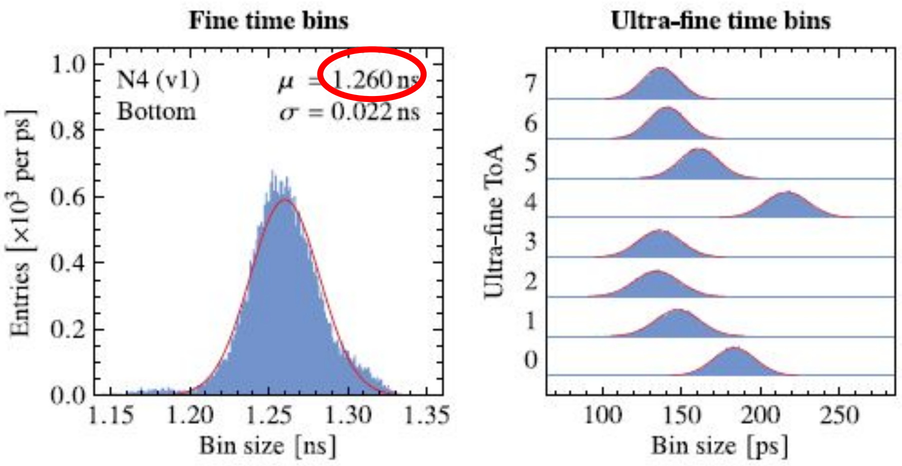
- ➢ Timepix4 power consumption～ 5 W
- ➢ Goal: stable operation with 20°C inside the vacuum tube
  - ○ Cold finger attached to the ceramic carrier



X. Llopart (CERN)

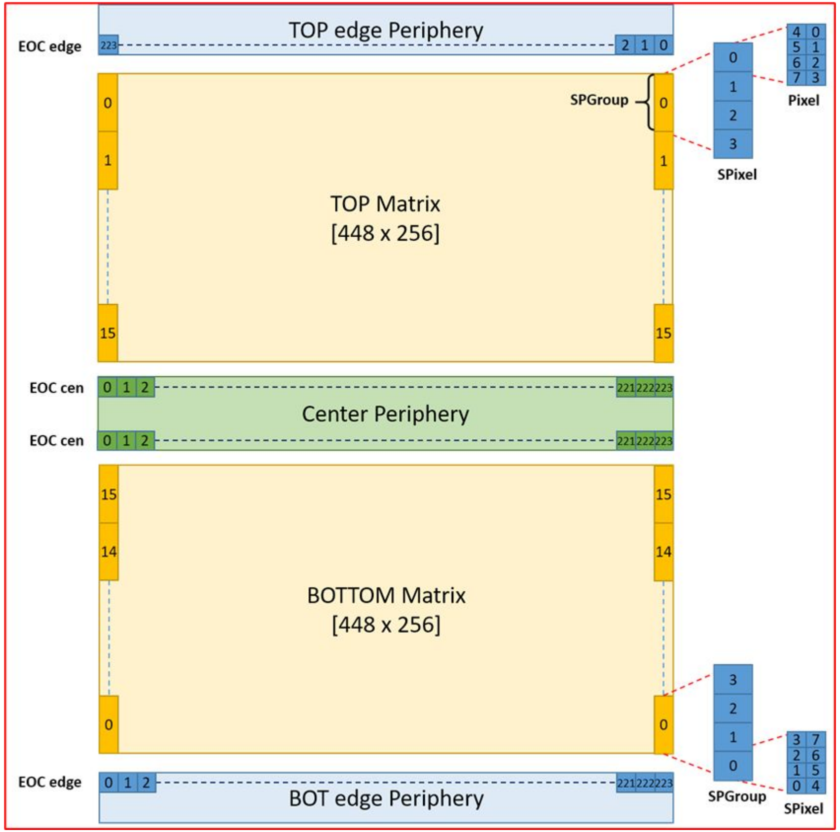
Timing resolution measurements - Time bins sizes measurements

- ➢ External testpulse used to measure fToA and UfToA bins:
  - ○ delay settable up to ps precision
  - ○ signals sent directly to the Timepix4 through digital pixels
  - ○ error function fit of even and odd fToA and UfToA to estimate bins width
- ➢ VCO too fast on Timepix4_v1:
  - ○ average fToA bin size: 1.26 ns
  - ○ average UfToA bin size: ~ 150 ps



Pixel structure

- ➢ Active area: ~ 7 cm^2
- ➢ Super Pixel (SP): 2 adjacent columns of 4 pixel
- ➢ Super Pixel Group (SPG): column of 4 SP
- ➢ 16 SPG in a column form a Double column



[X. Llopart *et al* 2022 *JINST* **17** C01044]

Timepix generations

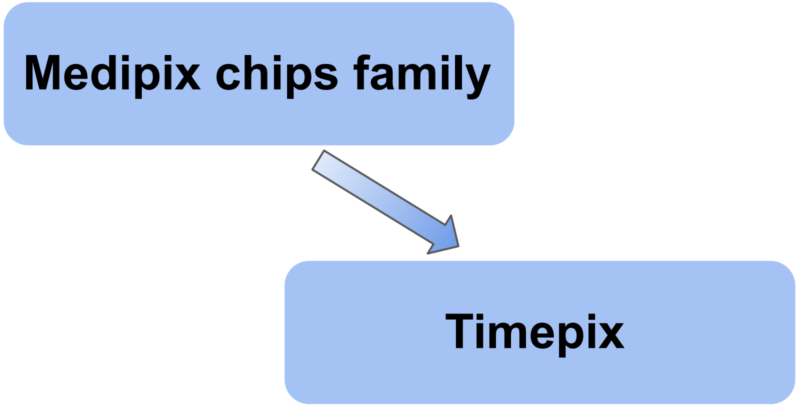
			Timepix	Timepix2	Timepix3	Timepix4
Tech. node (nm)			IBM 250	TSMC 130	IBM 130	TSMC 65
Year			2005	2018	2013	2019
Pixel size (mm)			55	55	55	55
# pixels (x x y)			256 x 256	256 x 256	256 x 256	448 x 512
Sensitive area			1.98 cm^2	1.98 cm^2	1.98 cm^2	6.94 cm^2
Number of sides for tiling using WB			3 (87.1% active area)	3 (85.6% active area)	3 (86.7% active area)	2 (93.7% active area)
Number of sides for tiling using TSV			No TSV ready	3 (85.6% active area)	3 (91.6% active area)	4 (99.3% active area)
Front-end	positive (h+)		Gain (16mV/kh^+) (Volcano >0.8MeV/pixel)	High Gain (25mV/kh^+) Logarithmic Gain (19mV/kh^+)	High Gain (45mV/kh^+) (Volcano >0.3MeV/pixel)	High Gain (35mV/kh^+) Low Gain (20mV/kh^+) Logarithmic Gain
	negative (e-)		Gain (16mV/ke^-)	High Gain (25mV/ke^-)	High Gain (45mV/ke^-)	High Gain (35mV/ke^-) Low Gain (20mV/ke^-)
Minimum detectable charge			~750 e^-	~600 e^-	~500 e^-	~500 e^-
Operation Modes	Tracking (Event arrival time and/or energy)	Readout	Full Frame-based (Sequential R/W)	Full Frame-based (Sequential or Continuous R/W)	Data-driven (48-bit packet per pixel hit)	Data-driven (64-bit packet per pixel hit)
		Event Data	TOT or TOA	TOT and TOA; TOT or TOA	TOT & TOA	TOT & TOA
		TOT energy resolution	<3keV (FWHM Si)	~0.75keV (FWHM Si)	~2KeV (FWHM Si)	~1KeV (FWHM Si)
		TOA bin size	10ns (@100MHz)	10ns (@100MHz)	1.56ns (On-pixel TDC @40MHz)	195ps (On-pixel TDC @40MHz)
		TOA dynamic range	118.1µs (@100MHz)	2.62ms (@100MHz)	409.6µs (@40MHz)	1.63ms (@40MHz)
		Max Rate	<1x10^6 hits/cm^2/s (with 300µs readout dead time)	<1x10^6 hits/cm^2/s (no readout dead time)	43x10^6 hits/cm^2/s (no readout dead time)	358x10^6 hits/cm^2/s (no readout dead time)
		Max Pix Rate	33 Hz/pixel	33 Hz/pixel	1.3 KHz/pixel	10.8 KHz/pixel
	Imaging (Event counting)	Readout	Full Frame-based (Sequential R/W)	Full Frame-based (Sequential or Continuous R/W)	Zero-suppressed (with pixel addr) (Sequential R/W)	Full Frame-based (Continuous R/W)
		Counter depth	14-bits	10-bit or 14-bit	Counting (10-bit) and integral TOT (14-bit)	8-bits or 16-bits
		Frame rate	100 fps @1x100Mbps 3.2 kfps @32x100Mbps	4.9 kfps @10-bit 32x100Mbps 3.5 kfps @14-bit 32x100Mbps	1.62 kfps @48-bit 8x640Mbps	89.2 kfps @8-bit 16x163Gbps 44.8 kfps @16-bit 16x163Gbps
		Max Count Rate	~35 x 10^9 hits/cm^2/s	~35 x 10^9 hits/cm^2/s	~82 x 10^9 hits/cm^2/s	~800 x 10^9 hits/cm^2/s
Maximum Readout bandwidth			3.2Gbps (32 x 100MHz)	3.2Gbps (32 x 100MHz)	≤5.12Gbps (8x SLVS@640 Mbps)	≤163.84Gbps (16x @10.24 Gbps)

Timepix generations

Medipix chips family

- Photon counting chips
- Frame based readout

Timepix generations



- Pixel arrangement:
  - 256 x 256 pixels
  - 55 µm pitch
- Frame based readout
- Operating modes:
  - arrival time mode
  - energy mode (ToT measurement)
  - event counting
- Timing resolution: 10 ns
- Dead time per pixel: 300 µs

Timepix generations

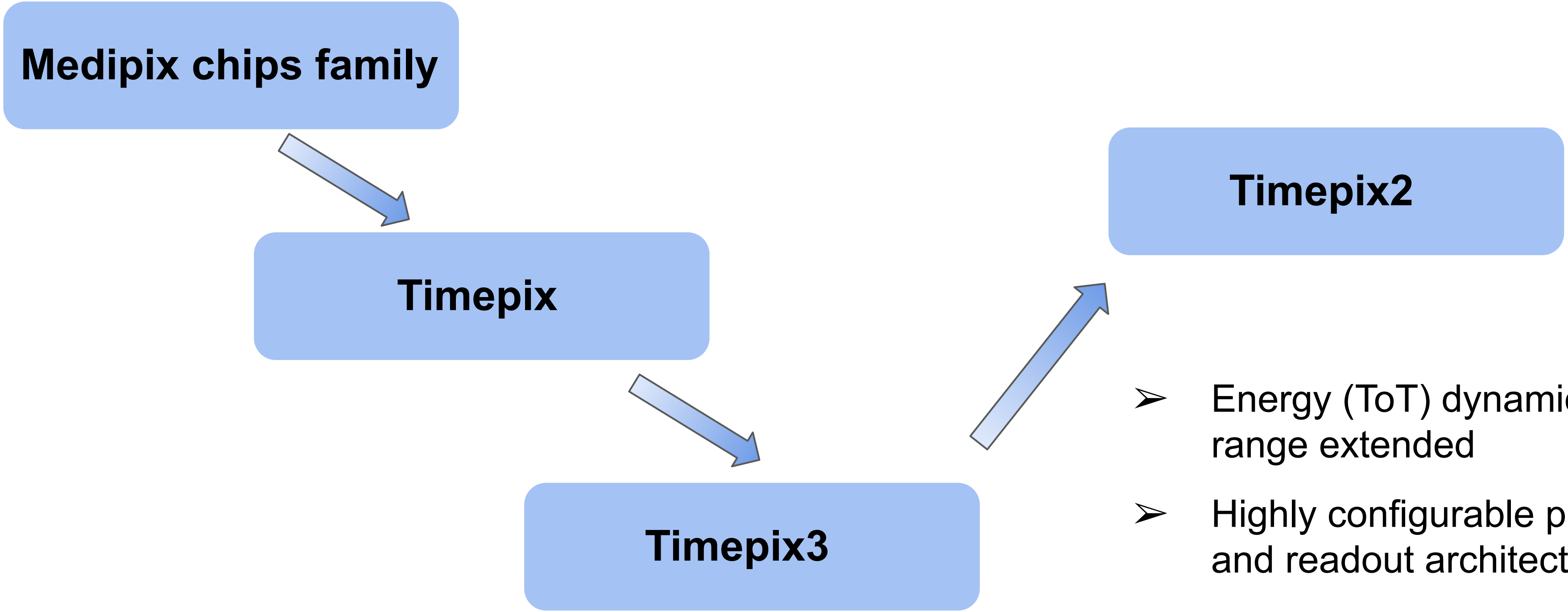
Medipix chips family

Timepix

Timepix3

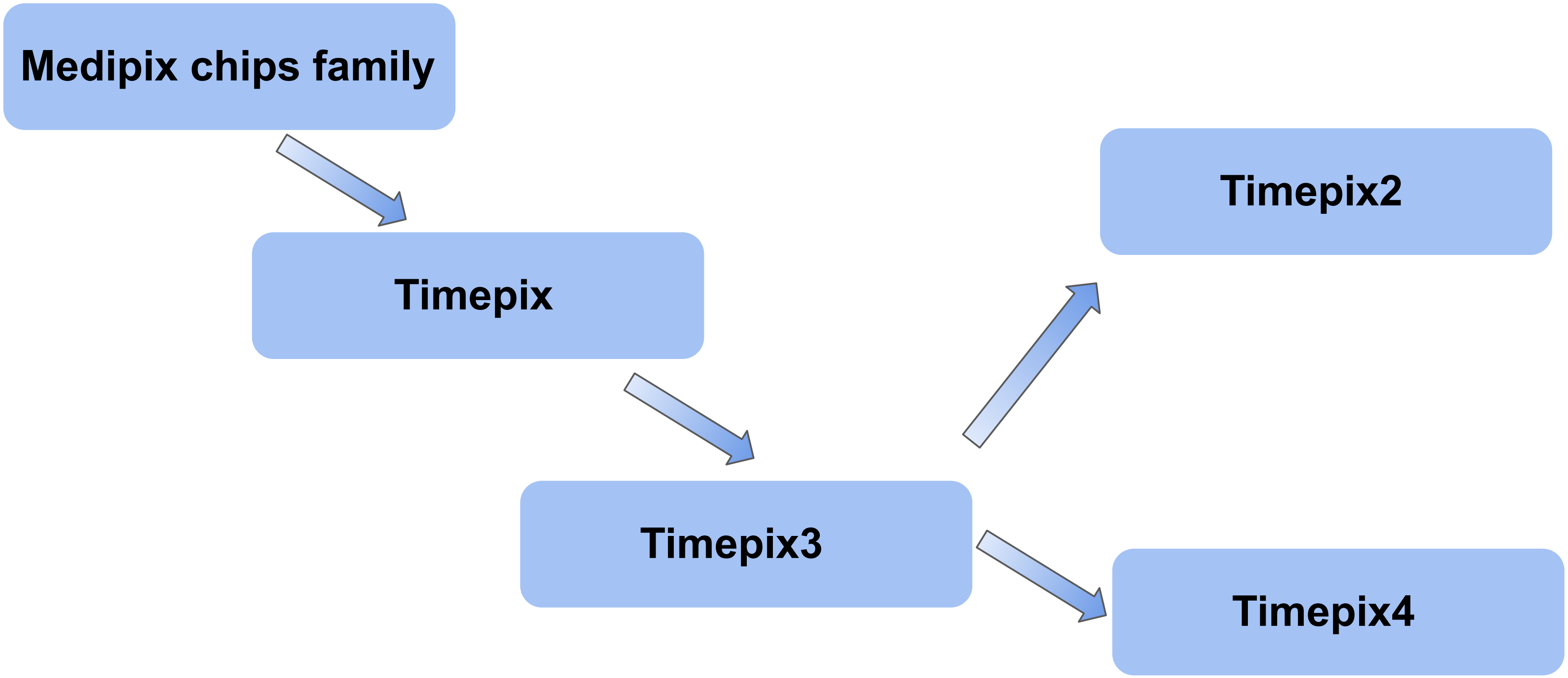
- Pixel arrangement:
  - 256 x 256 pixels
  - 55 µm pitch
- Particle with both polarities measurable
- Simultaneous ToA and ToT information per pixel
- Data-driven readout introduction (event-by-event readout and 0-suppressed): decreased dead time
- Improved time resolution: 1.56 ns

Timepix generations



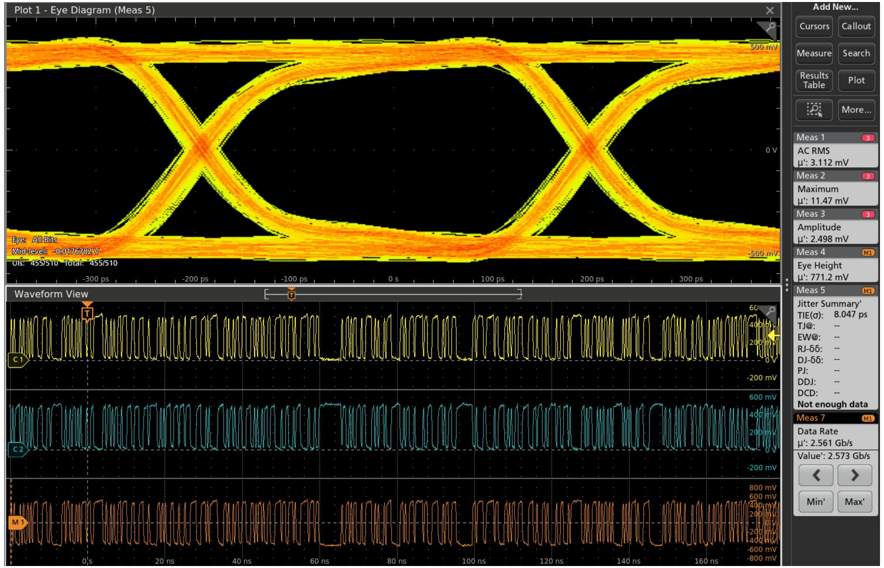
- Energy (ToT) dynamic range extended
- Highly configurable pixel and readout architecture

Timepix generations

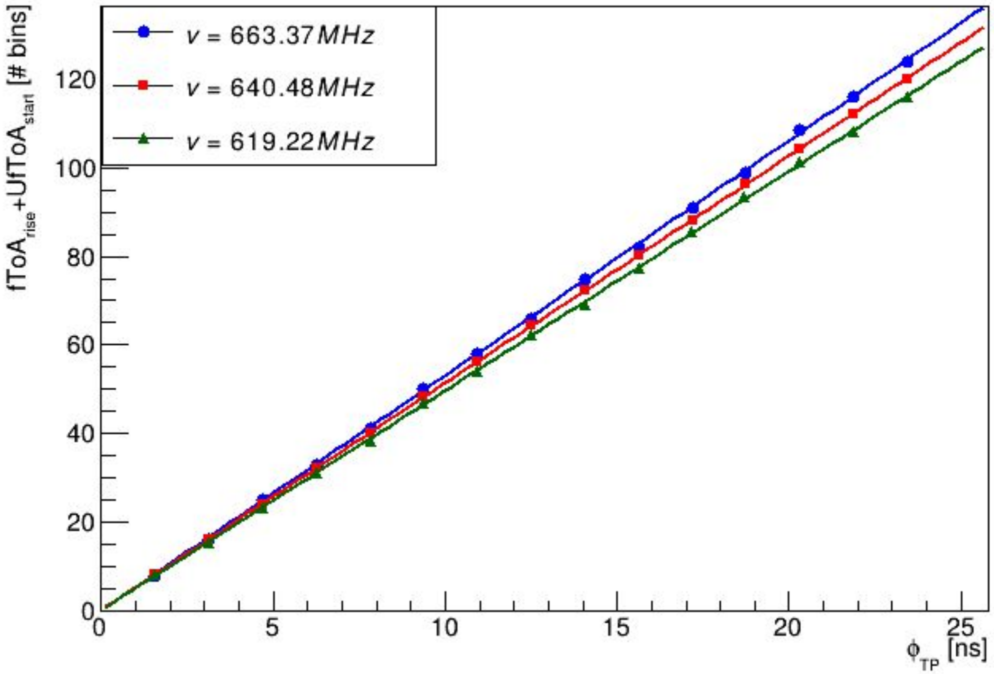


High-speed readout

- Gigabit Wireline Transmitter with a Clock Cleaner (GWT-CC):
  - serializes data stream
  - transmits data to an off-chip receiver
- Two operation mode:
  - high-speed: 80 Mb/s - 10.24 Gb/s per link
  - lower-speed: 40 Mb/s - 5.12 Gb/s per link
- Total of 16 links (8 per half-matrix): max bandwidth of 160 Gb/s
- PRBS generator for links tests
- Tests performed on each link at each possible frequency:
  - eye diagram well opened @ 2.56 Gb/s

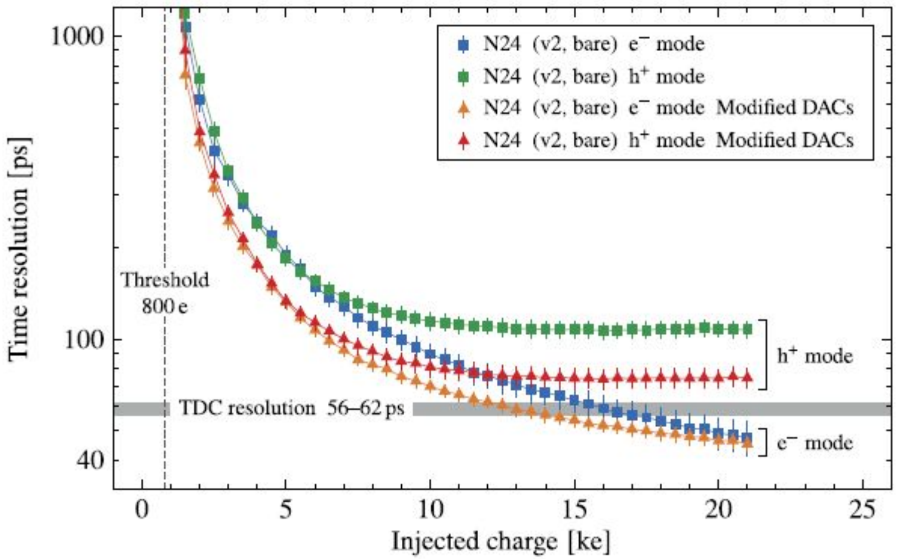


- VCO of different pixels oscillate with **different frequencies**
- Finer ToA bins generated with different width
- ToA and ToT measurements heavily affected by this effect



Timing resolution measurements - Test pulse

- ➢ Analog internal test pulse used to measure the analog front-end jitter
- ➢ Hole-collecting mode:
  - ○ jitter asymptotic to ~100 ps r.m.s.
  - ○ bare Timepix4 and Timepix4 bonded to Si sensor show similar trends
  - ○ at low charge, worst resolution with sensor bonded
- ➢ Electron-collecting mode:
  - ○ no asymptotic trend
  - ○ resolution lower than 50 ps r.m.s. both with bare and bonded chips
- ➢ Resolution improved changing discriminator bias



[K. Heijhoff *et al* 2022 *JINST* 17 P07006]

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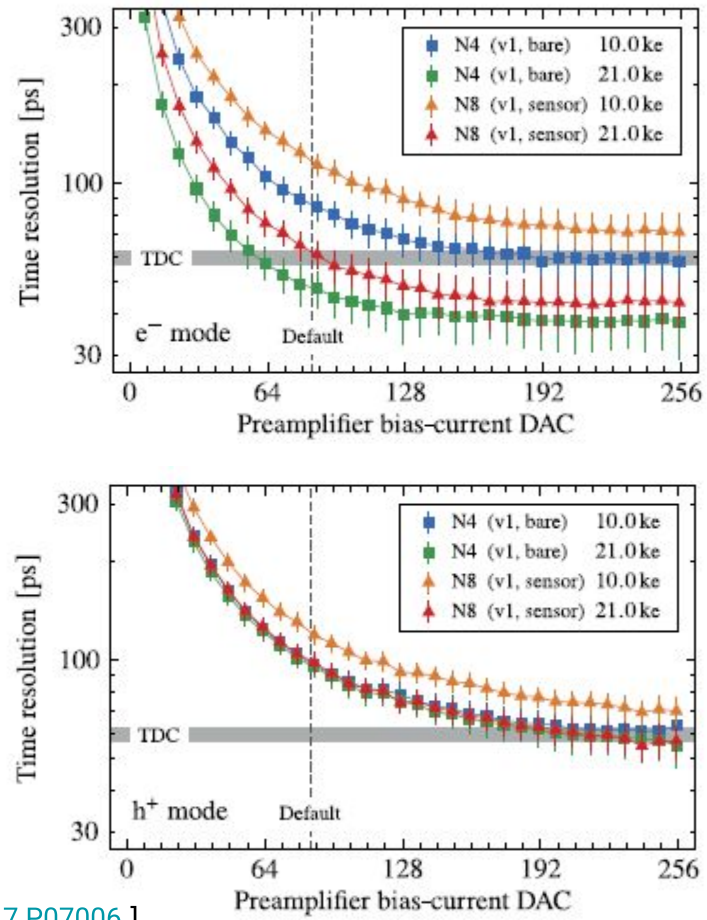
  - ○ resolution lower than 50 ps r.m.s. both with bare and bonded chips
- ➢ Resolution improved changing discriminator bias
- ➢ Resolution dependence on preamp current



[K. Heijhoff *et al* 2022 *JINST* 17 P07006]

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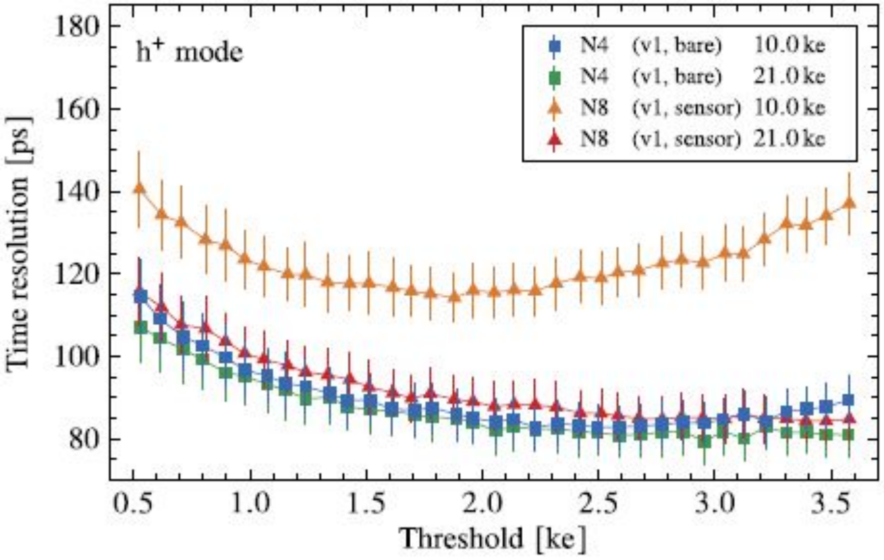
  - at low charge, worst resolution with sensor bonded
- Electron-collecting mode:
  - no asymptotic trend
  - resolution lower than 50 ps r.m.s. both with bare and bonded chips
- Resolution improved changing discriminator bias
- Resolution dependence on preamp current
- Dependence on threshold



[K. Heijhoff *et al* 2022 *JINST* 17 P07006]

Single pixel timing resolution

- ➢ ToT vs charge calibration applied to each pixel
- ➢ Distribution divided into “vertical” slices, each one selecting a narrow range of charge
- ➢ Timing resolution values extracted for each slice