# The future of electronics and its impact on vertex detectors

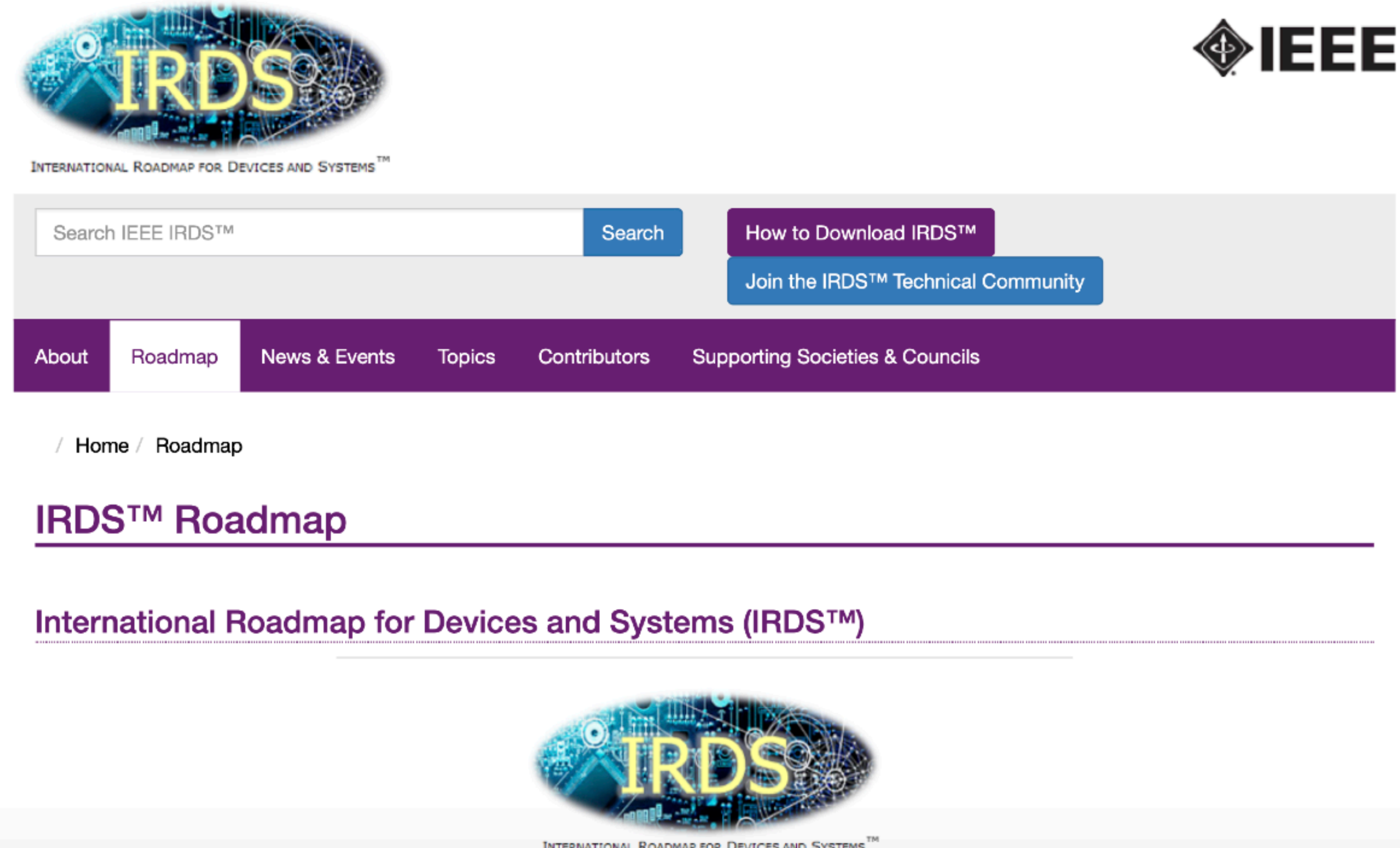
## an overview of the DRD7 research program

Angelo Rivetti
on behalf of the DRD7 steering committee

# Outline

- **Relevant trends in microelectronics**
- **Opportunities and challenges for HEP applications**
- **An overview of the DRD7 R&D program**

# Relevant trends in microelectronics: the IRDS 2022 roadmap




- NTRS ⇨ ITRS ⇨ IRDS

# The key IRDS 2022 chapters

- Application Benchmarking
- Systems and Architectures
- Outside System Connectivity
- More Moore
- Beyond CMOS
- Cryogenic Electronics and Quantum Information Processing
- Packaging Integration
- Factory Integration
- Lithography
- Yield Enhancement
- Metrology
- Environment, Safety, Health, and Sustainability
- More than Moore
- Autonomous Machine Computing
- Mass Data Storage and Nonvolatile Memory
- Medical Devices Market Drivers
- Automotive Market Drivers

Radiation hardness not in the menu

# Technology nodes

**Logic/Foundry Process Roadmaps (for Volume Production)**

2016 2017 2018 2019 2020 2021 2022

Intel: 14nm+ | 10nm (limited) 14nm++ | 10nm | 10nm+ | 10nm++ | 7nm EUV

Samsung: 10nm | 8nm | 7nm EUV | 6nm EUV | 18nm FDSOI | 5nm | 4nm | 3nm GAA

TSMC: 10nm | 7nm | 12nm | 7nm+ EUV | 5nm | 6nm | 5nm+ | 4nm | 3nm

GlobalFoundries: 22nm FDSOI | 12nm finFET | 12nm FDSOI | 22nm+ FDSOI | 12nm+ finFET

SMIC: 14nm finFET | 12nm finFET | 8-10nm finFET

UMC: 14nm finFET | 22nm planar

Note: What defines a process "generation" and the start of "volume" production varies from company to company, and may be influenced by marketing embelishments, so these points of transition should only be seen as very general guidelines.

Sources: Companies, conference reports and IC Insights

*Figure ES13 Scaling progressing unabated with EUV technology*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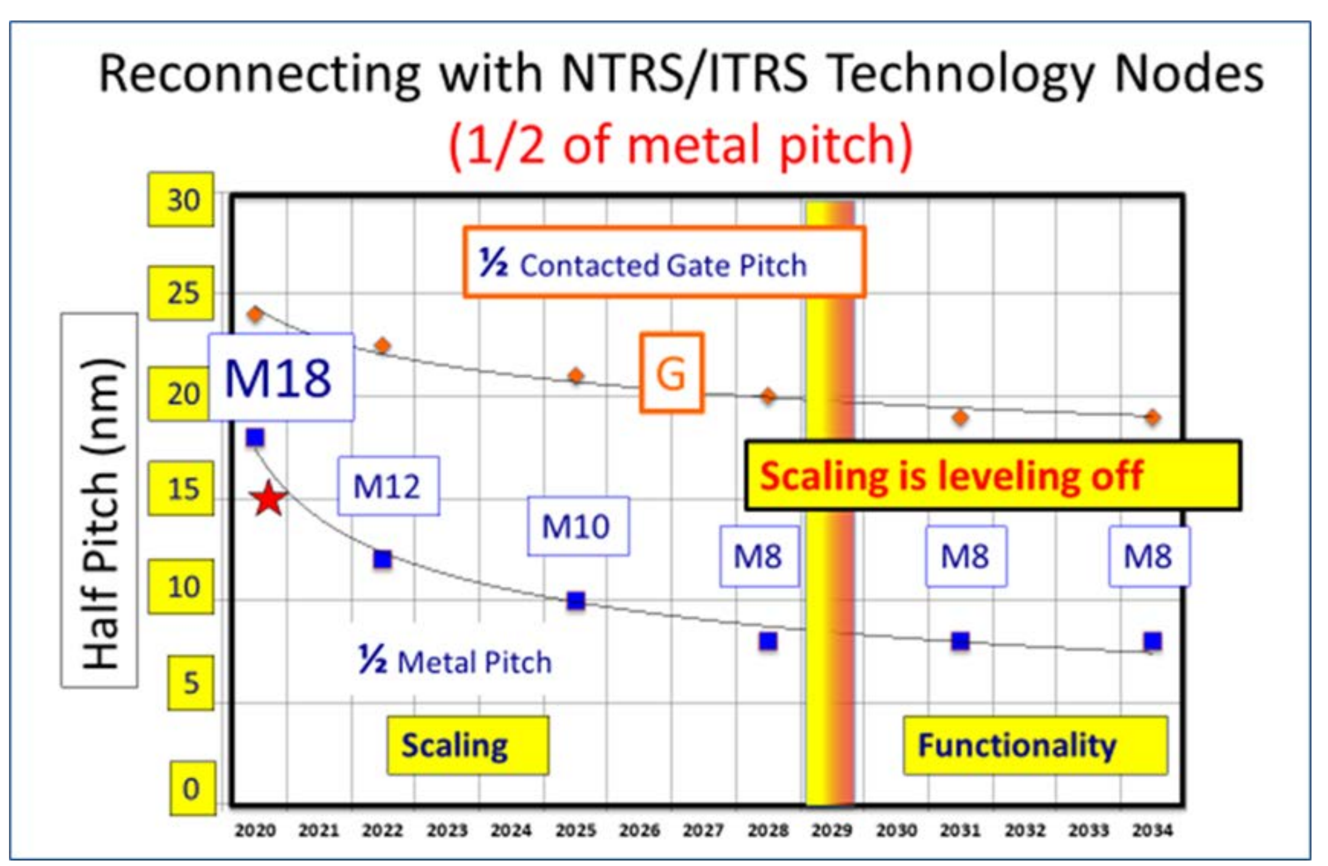
# The gate length is not the full story

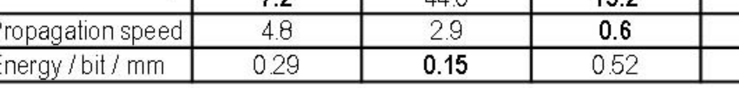



- **Source: IRDS ES, p. 28**

# More Moore and more than Moore

- More Moore
  - Keeping the pace with More’s law when 2D ICs hits the physics (or economics) barrier
  - In practice in the mid-near term: going 3D
  - Already common for high bandwidth memories, soon to become standard also for logic
  - 3D VLSI expected to extend Moore’s law up to 2040
- More than Moore
  - Heterogeneous integration
  - Use of silicon-based technology to integrate different functionalities (RF, power, sensor, actuators) into compact and high performance systems

| ...sity | 0.5 | 3.0 | 1.6 | Tb/s/mm² |
|---|---|---|---|---|
| ...ection | 0.9 | N/A | 0.8 | Tb/s/mm |
| ...iplets | 394 | 133 | 640 | GB/s |
| | 527 | | | |



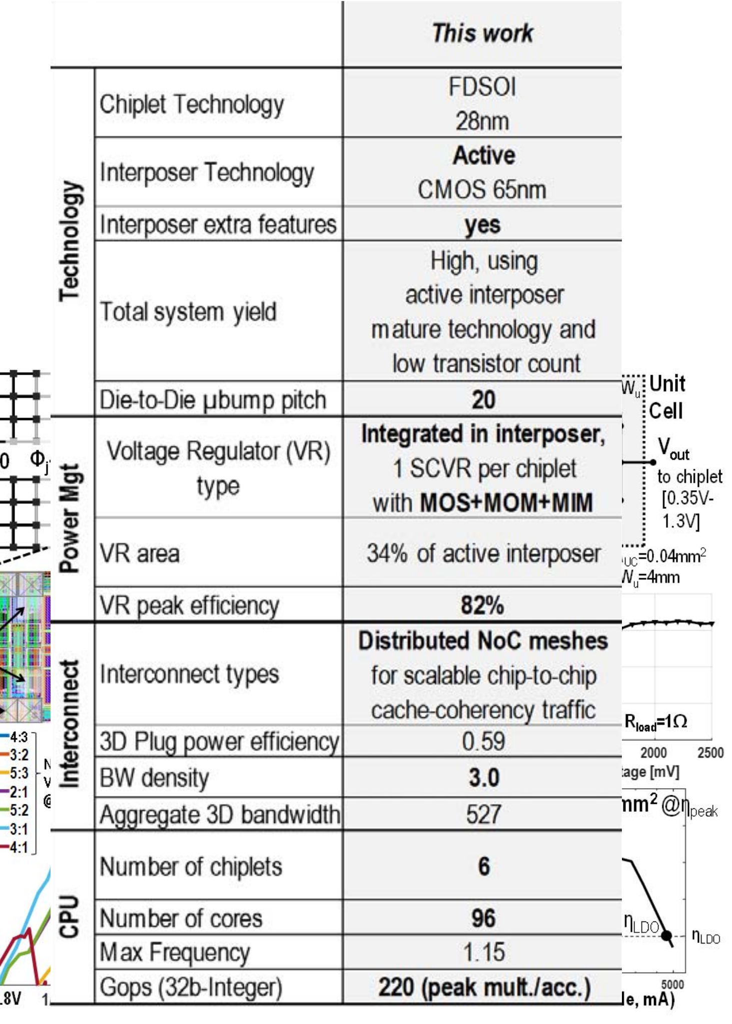
| | 7.2 | 44.0 | 13.2 |
|---|---|---|---|
| Propagation speed | 4.8 | 2.9 | **0.6** |
| Energy / bit / mm | 0.29 | **0.15** | 0.52 |

# More Moore

**2.3 A 220GOPS 96-Core Processor with 6 Chiplets**

## ISSCC 2020@IEEE

*Power consumption break-down (total and per-chiplet)*
*Chiplets @ 1V, 900 MHz*



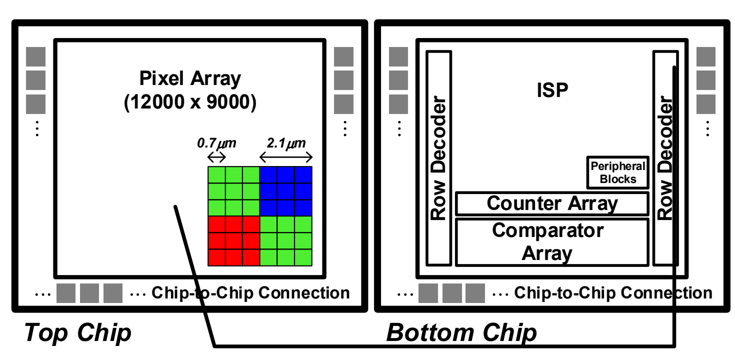
| | | *This work* |
|---|---|---|
| Technology | Chiplet Technology | FDSOI 28nm |
| | Interposer Technology | **Active** CMOS 65nm |
| | Interposer extra features | **yes** |
| | Total system yield | High, using active interposer mature technology and low transistor count |
| | Die-to-Die µbump pitch | **20** |
| Power Mgt | Voltage Regulator (VR) type | **Integrated in interposer,** 1 SCVR per chiplet with **MOS+MOM+MIM** |
| | VR area | 34% of active interposer |
| | VR peak efficiency | **82%** |
| Interconnect | Interconnect types | **Distributed NoC meshes** for scalable chip-to-chip cache-coherency traffic |
| | 3D Plug power efficiency | 0.59 |
| | BW density | **3.0** |
| | Aggregate 3D bandwidth | 527 |
| CPU | Number of chiplets | **6** |
| | Number of cores | **96** |
| | Max Frequency | 1.15 |
| | Gops (32b-Integer) | **220 (peak mult./acc.)** |

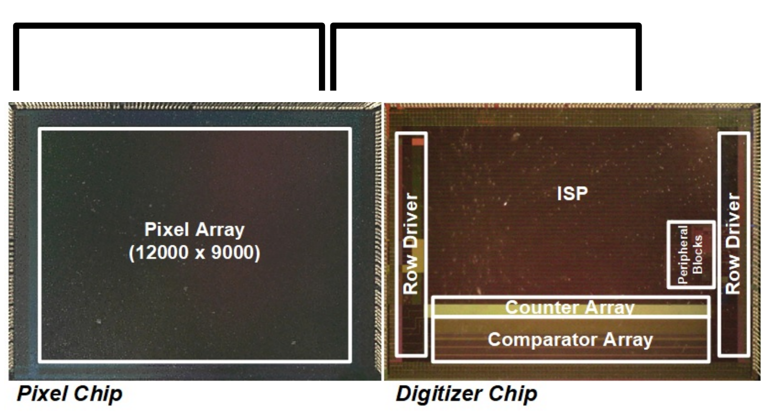
# More than Moore

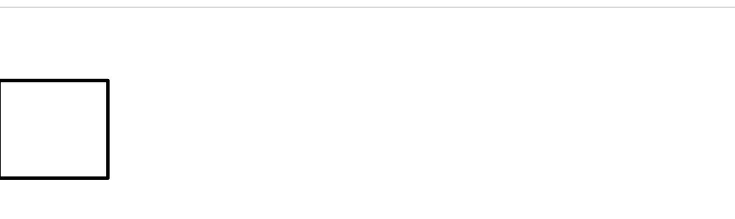
- **ISCAS 2022**

A 0.7 μm-Pitch 108 Mpixel Nonacell-Based CMOS Image Sensor with Decision-Feedback Technique

Jaehoon Jun, Haneol Seo, Hyukbin Kwon, Jongyeon Lee, Beomsoo Yoon, Youngwoo Lee,
Yongbin Kim, Woong Joo, Jesuk Lee, and Kyoungmin Koh
System LSI Division, Samsung Electronics
Hwaseong, South Korea
E-mail: jaehoon.jun@samsung.com



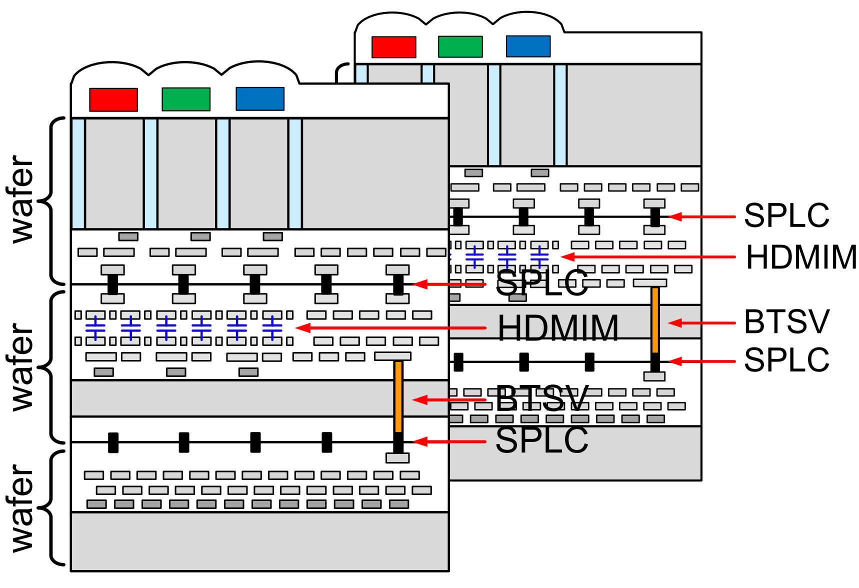
# More than Moore

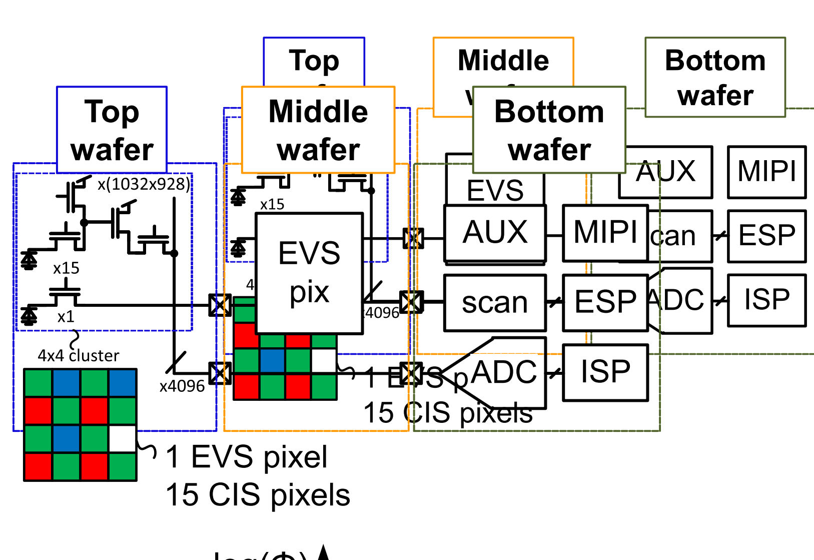
This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.



# A Three-Wafer-Stacked Hybrid 15-MPixel CIS + 1-MPixel EVS With 4.6-GEvent/s Readout, In-Pixel TDC, and On-Chip ISP and ESP Function

Menghan Guo, Shoushun Chen, *Senior Member, IEEE*, Zhe Gao, Wenlei Yang, Peter Bartkovjak, Qing Qin, Xiaoqin Hu, Dahai Zhou, Qiping Huang, Masayuki Uchiyama, Yoshiharu Kudo, Shimpei Fukuoka, Chengcheng Xu, Hiroaki Ebihara, Xueqing Wang, Peiwen Jiang, Bo Jiang, Bo Mu, Huan Chen, Jason Yang, T. J. Dai, and Andreas Suess, *Member, IEEE*



# Key IPs: ADCs

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 58, NO. 10, OCTOBER 2023 2709

## A 14b 500 MS/s Single-Channel Pipelined-SAR ADC With Reference Ripple Mitigation Techniques and Adaptively Biased Floating Inverter Amplifier

Wenning Jiang, *Member, IEEE*, Yan Zhu, *Senior Member, IEEE*, Chixiao Chen, *Member, IEEE*, Hao Xu, *Member, IEEE*, Qi Liu, *Member, IEEE*, Ming Liu, *Fellow, IEEE*, Rui P. Martins, *Fellow, IEEE*, and Chi-Hang Chan, *Senior Member, IEEE*

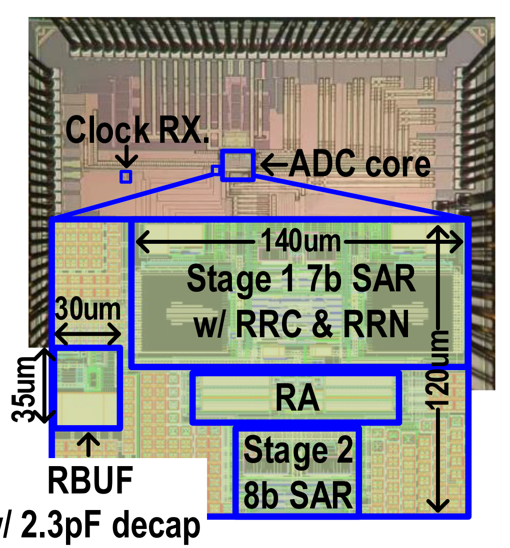



TABLE II

ADC PERFORMANCE SUMMARY AND COMPARISON

| | This work | JSSC'22 J. Lagos | ISSCC'17 H. Huang | JSSC'18 E. Martens | JSSC'22 X. Guo | JSSC'18 R. Sehga |
|---|---|---|---|---|---|---|
| Architecture | Pipe-SAR | Pipe-SAR | Pipe-SAR | Pipe-SAR | Pipe-SAR | Pipelined |
| Technology | 28nm | 16nm | 65nm | 16nm | 40nm | 28nm |
| Sample Rate[MS/s] | 500 | 500 | 330 | 300(2x TI) | 625 | 280 |
| Resolution [bit] | 14 | 11.5 | 12 | 13.5 | 13 | 12 |
| Supply [V] | 1/1.2 | 0.9 | 1.3 | 0.8 | 1.15 | 1 |
| Input Swing [V] | 1.6 | 1.8 | 2.4 | N/A | 2.2 | 1.2 |
| SFDR @Nyq.[dB] | 80.55 | 75.5 | 75.8 | 73.6 | 70 | 77 |
| SNDR @Nyq.[dB] | 64.2 | 62.3 | 63.5 | 64 | 62.4 | 64 |
| Power[mW] | 6.34 | 3.3 | 6.2 | 3.6 | 7.05 | 13 |
| $FoM_W$@Nyq.[fJ/c-s] | 9.6 | 6.2 | 15.4 | 9.2 | 10.5 | 35.8 |
| $FoM_S$@Nyq.[dB] | 170.2 | 171.1 | 167.8 | 170.2 | 168.9 | 164.3 |
| Reference Buffer | Yes | No | No | No | Yes | No |
| Decap on Ref.[pF] | 3 | 105 | N/A | 50 | N/A | N/A |
| Core Area[mm²] | 0.018* | 0.0404* | 0.08 | 0.11* | 0.022 | 0.22 |
| Ripple Mitigation | RRC/RRN | Regulation | No | Aux. DAC | No | No |

* Core area w/ reference decap

RRC ON, RRN ON: SNDR=67dB, SFDR=80dB

$F_S$=500MS/s, $F_{IN}$=~67MHz

Normalized Frequency

Max(|DNL|)=Max(DNL$_{RRN_OFF}$)-Max(DNL$_{RRN_ON}$)

RBUF Bias Current [mA]

RRC OFF, RRN ON: SNDR=39.3dB, SFDR=50.4dB

RRC ON, RRN OFF: SNDR=63.7dB, SFDR=80dB

# Key IPs: ADCs

624 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 58, NO. 3, MARCH 2023

## A 13b 600-675MS/s Tri-State Pipelined-SAR ADC With Inverter-Based Open-Loop Residue Amplifier

Xiaofeng Guo, *Member, IEEE*, Run Chen, *Senior Member, IEEE*, Zhenqi Chen, *Senior Member, IEEE*, and Bin Li, *Member, IEEE*

| C1 [nV²] | RA1 [nV²] | Dig.-S. [nV²] | CDAC2 [nV²] | Others [nV²] |
|---|---|---|---|---|
| 5 | 30.53 | 18.25 | 2.85 | 0.97 |
| % | 35.1% | 21.0% | 3.3% | 1.0% |

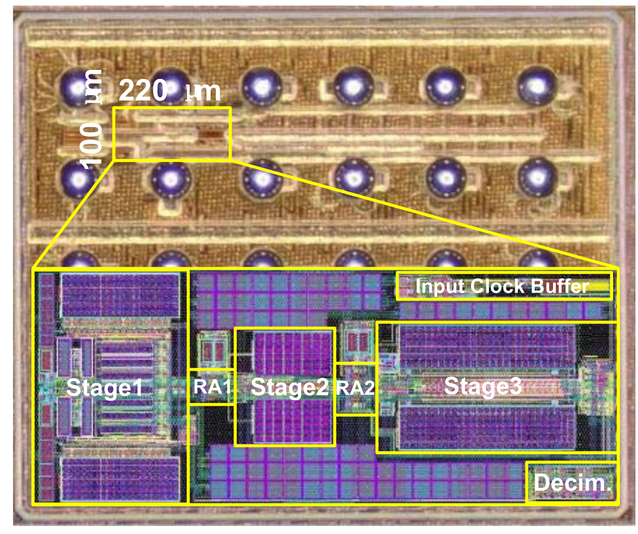



TABLE III
ADC PERFORMANCE SUMMARY AND COMPARISON

| | This Work | ISSCC 2021 [6] | JSSC 2017 [5] | JSSC 2020 [1] | VLSI 2021 [11] | ISSCC 2022 [10] |
|---|---|---|---|---|---|---|
| Architecture | **3-Stage Pipe-SAR** | 2-Stage Pipe-SAR&TI DSM | 2-Stage Pipe-SAR | 3-Stage Pipe-SAR | 2-Stage Pipe-SAR | 2-Stage Pipe-SAR |
| SAR Architecture | **Tri-State** | Binary | Binary | Binary | Binary | Binary |
| RA Architecture | **Open Loop Inverter-Based** | Open Loop Source-Follower | Open Loop Gm-C + V2T | Open Loop Gm-R | Closed Loop Ring-Amp | Closed Loop |
| Technology | **40nm** | 7nm | 65nm | 28nm | 16nm | 28nm |
| Measured Samples | **10** | 5 | 2 | 1 | 1 | 1 |
| Supply Voltage [V] | **1.1 ~ 1.2** | 0.77 ~ 0.9 | 1.25 ~ 1.35 | 1 | 0.8 ~ 1 | 1.1 |
| Measured Temperature [℃] | **-40 ~ 125** | -40 ~ 80 | -5 ~ 85 | 0 ~ 80 | - | - |
| Resolution [bits] | **13** | 12 | 12 | 12 | 11.5 | 14 |
| Fs [MS/s] | **625 (ups to 675)** | 600 | 330 | 1000 | 500 | 130 |
| Input Swing [Vpp] | **2.2** | 1 | 2.4 | 1.2 | 1.8 | - |
| DR [dB] | **67** | - | - | - | 63.6 | - |
| SNDR w/ PVT Variation [dB] | **59.8~62.8 (Mean)**<br>**< 1.7 (1-σ)** | > 54 | 0.8 degradation | - | - | - |
| SNDR [dB] LF | **63.8** | 56.6 | 67.7 | 61.36 | - | 72.9 |
| SNDR [dB] HF | **62.4** | 55.3 | 63.5 | 59 | 62.9 | 72.5 |
| Peak SFDR [dB] | **76** | 71.1 | 83.4 | 74.5 | 75.5 | 87.5 |
| Power [mW] | **7.05** | 13 | 6.23 | 7.6 | 2.8 | 0.82 |
| $FoM_W$@HF [fJ/c-s] | **10.5** | 45.6 | 15.4 | 9.28 | 4.9 | 1.8 |
| $FoM_S$@HF [dB] | **168.9** | 158.9 | 167.8 | 168.2 | 172.4 | 181.5 |
| Area [mm²] | **0.022** | 0.037 | 0.08 | 0.009 | 0.0084 | 0.013 |
| Cs [pF] | **0.29** | 0.69 | 1 | 0.54 | - | 1.6 |
| Bias-Free RA | **Yes** | No | No | No | No | No |

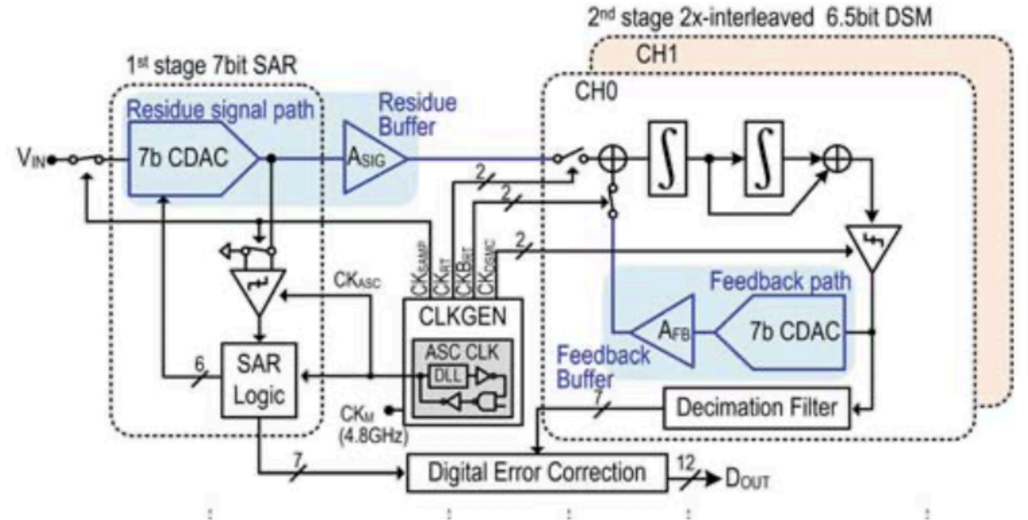
# Key IPS: ADCs

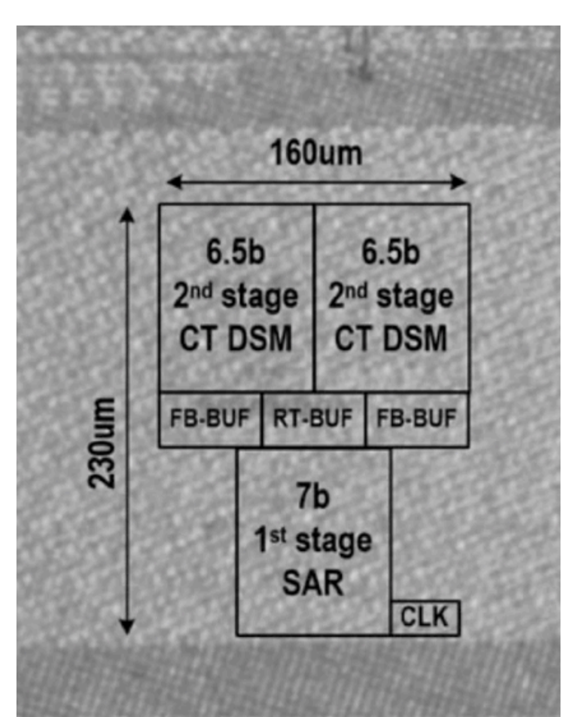
## ISSCC 2021

**10.5 A 12b 600MS/s Pipelined SAR and 2×-Interleaved Incremental Delta-Sigma ADC with Source-Follower-Based Residue-Transfer Scheme in 7nm FinFET**

Seungyeob Baek, Ilhoon Jang, Michael Choi, Hyungdong Roh, Woongtaek Lim, Youngjae Cho, Jongshin Shin

Samsung Electronics, Hwasung, Korea

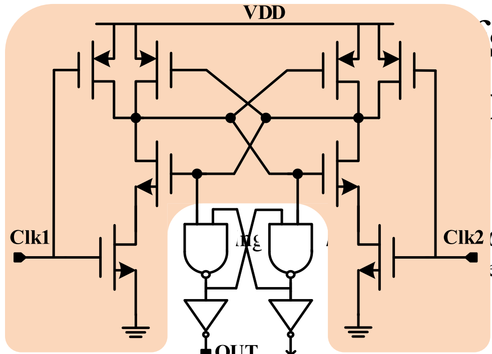



**Power: 13 mW**

# Key IPs: TDCs

IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, VOL. 72, 2023 2004911



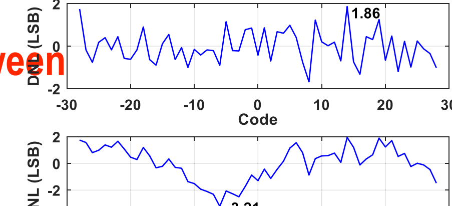

...s Time-Resolution 7.5-bit Stochastic
...-Digital Converter Based on
Two Arbiter Groups

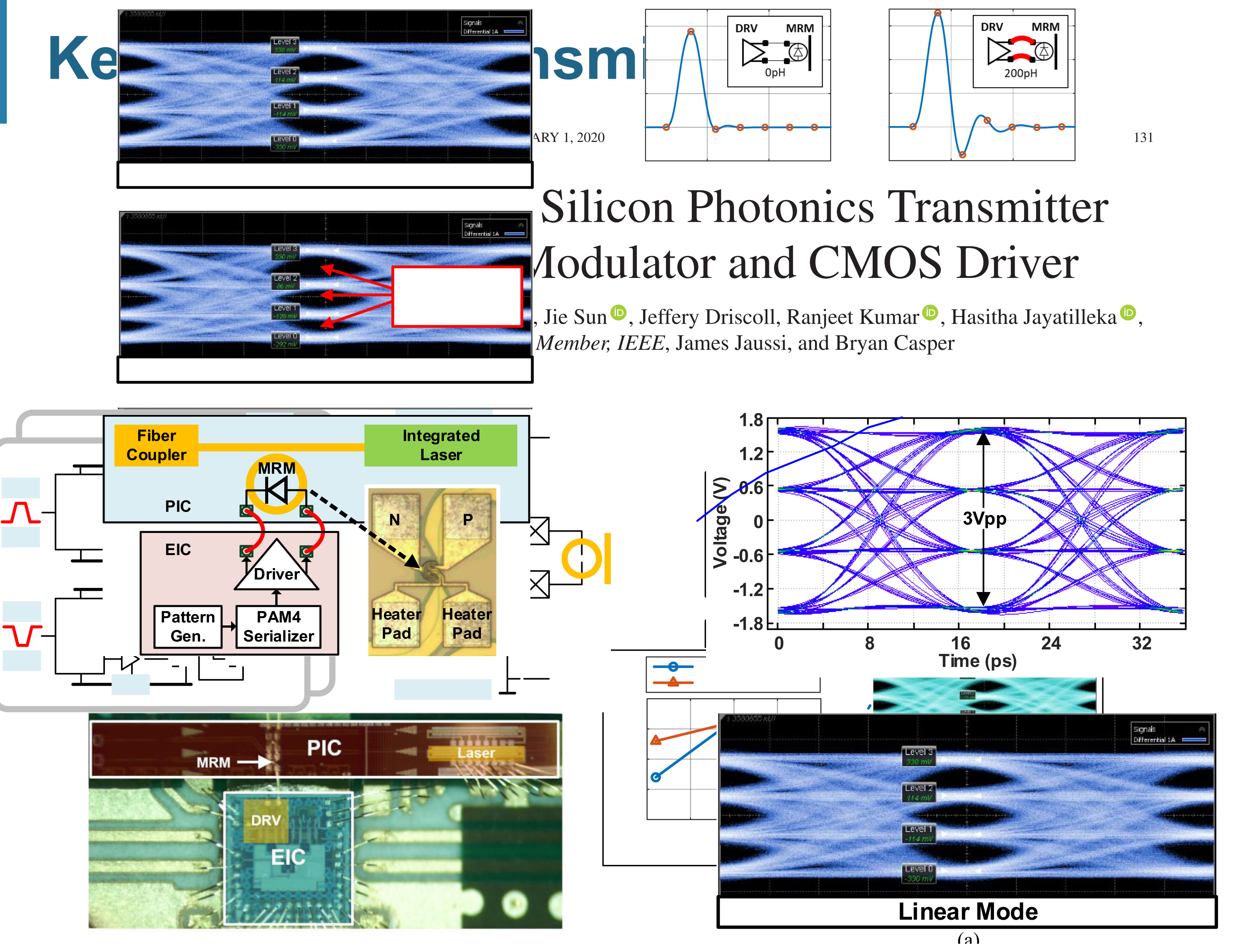
Graduate Student Member, IEEE, Xinquan Lai (来新泉), Member, IEEE,
...eng Wang (王宇恒), Graduate Student Member, IEEE

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

| | | [2] | [19] | [23] | [29] | [30] | [32] | **This work** |
|---|---|---|---|---|---|---|---|---|
| Architecture | | multi-level | multi-segment | pipeline | stochastic phase interpolation | stochastic phase interpolation | stochastic | **stochastic** |
| Technology [nm] | | 180 | 180 | 65 | 14 | 180 | 65 | **180** |
| Sampling rate [MHz] | | 333 | 0.82 | 250 | 100 | 60 | 100 | **50** |
| Time resolution [ps] | | 50 | 36 | 1.12 | 1.17 | 63 | 0.36 | **0.55** |
| Input range [ns] | | 13100 | 63.5 | 0.6 | 1.2 | 16.67 | 0.05 | **0.105** |
| NOB [bits] | | 18* | 10.8 | 9 | 10 | 8 | 7 | **7.5** |
| Linearity | INL [LSB] | 0.71 | 1.5 | 1.7 | 2.3 | 1.1 | 0.75 | **−1.81** |
| | DNL [LSB] | 0.47 | 0.65 | 0.6 | 0.8 | 0.8 | 0.77 | **1.87** |
| Effective time resolution [ps]** | | 85.5 | 90 | 3.01 | 3.86 | 132.3 | 0.63 | **1.55** |
| Power [mW] | | 87.6 | 0.44 | 15.4 | 0.78 | 25 | 6.2† | **19.8** |
| Area [$mm^2$] | | 2.25 | 0.11 | 0.14 | 0.036 | 1.13 | 0.068 | **0.893** |
| FoM [pJ.ps/conv.-step] | | 257.22*** | 27.09 | 0.36 | 0.029 | 215.33 | 0.305 | **3.38** |

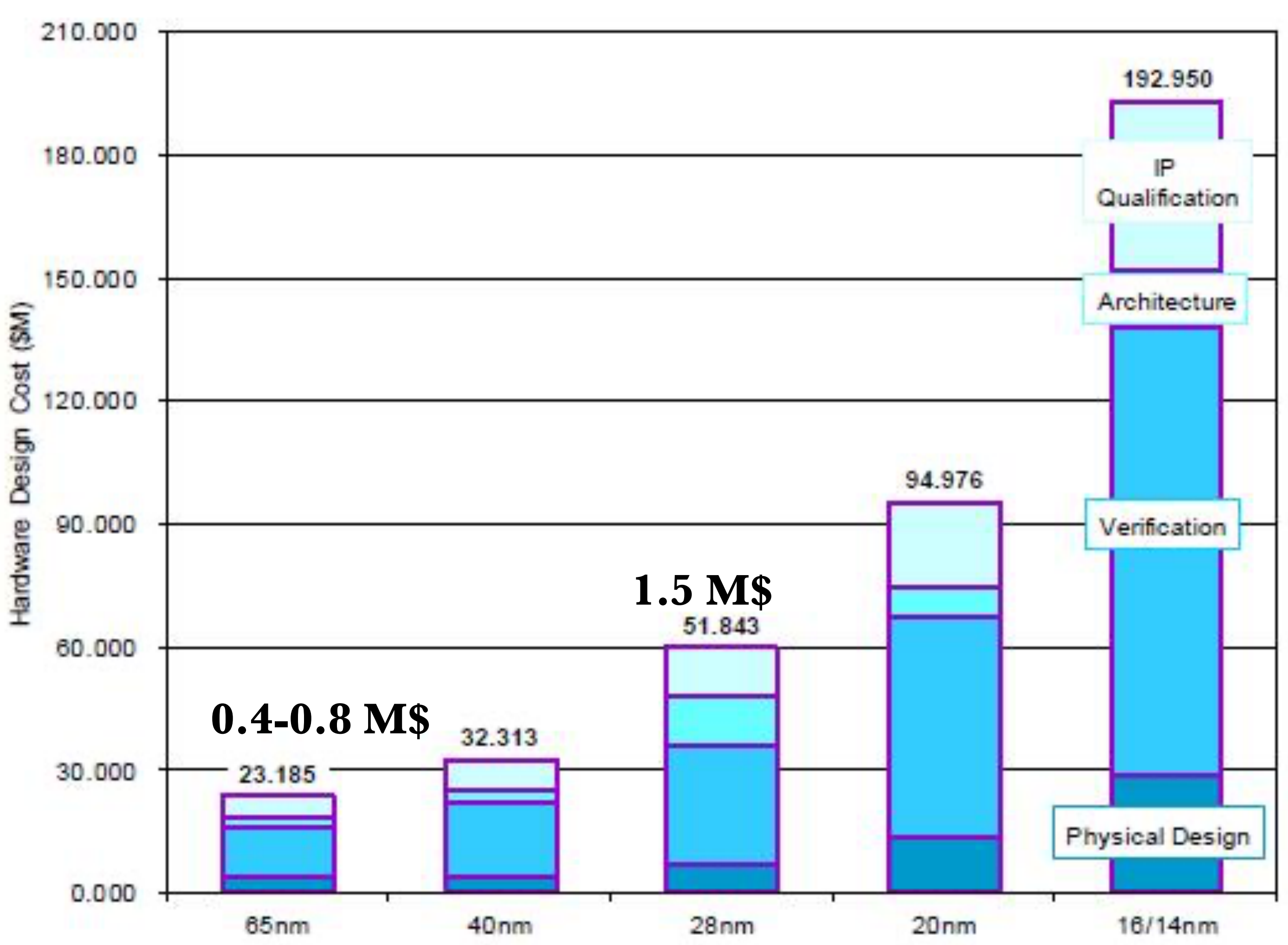
Timing resolution defined at the interplay between the very front-end





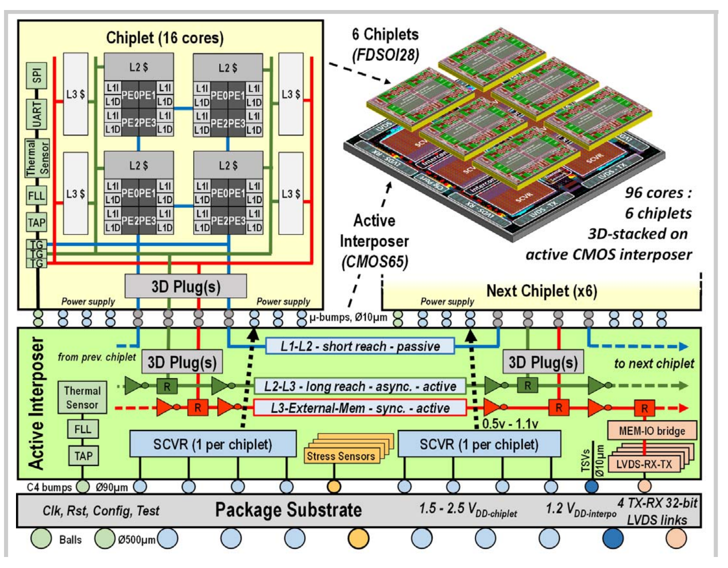

28 nm + Silicon Photonics

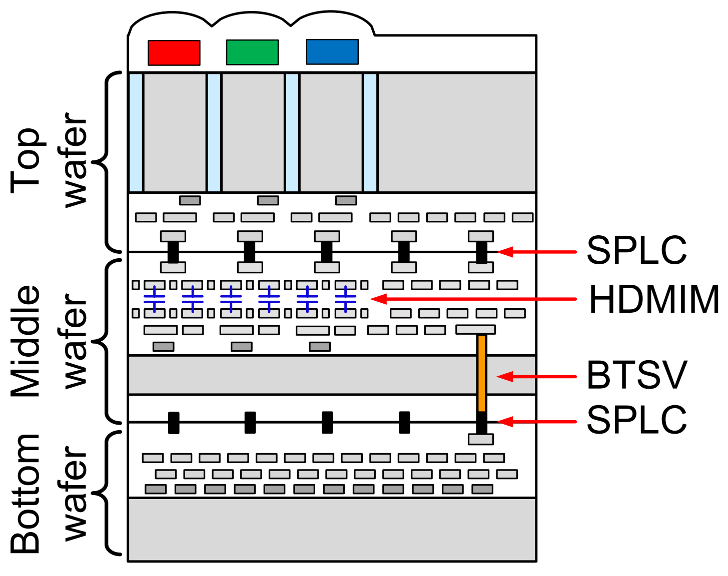
# IC economics




- 1.5 billions cell phones/year
- 250 millions wafers/year

# Chiplets, again




**How a future vertex detectors could look like:**

- **An active support (stitched sensing layers ( with internal gain) and bare minimum electronics**
- **Efficient digital processing layer (28 nm or beyond)**

**Key aspects:**

- **Efficient data and power management, smart and flexible digital readout, fast data transfer, access to critical technologies, radiation hardness…**

# Opportunities and challenges

- IC technologies deploy fantastic capabilities
- Moore law expected to continue in the foreseeable future within an evolutionary paradigm with 3D stacking becoming more and more prominent
- We do not fully exploit in electronics for HEP what technology can offer even today
  - Small design teams
  - Low production volumes
  - Long development cycles
  - Lack of shared, reusable IPs
  - Lack of appropriate simulation/verification environments
  - Difficulties in securing experienced people
  - Budgets
  - ….
- Can we address some of these issue?

# DRD7 collaboration

- **DRD7 in a nutshell: a collaborative effort to push electronics for particle detectors beyond our state of the art through a set of well harmonised multinational projects**
- **A dynamic environment: projects can be proposed at regular times**
- **A structured environment: projects are framed along prioritised lines of interest (the working groups) and are expected to be transformative for the field, multinational and with reasonable resources to make the project feasible**
- **It's an R&D: a project could also yield a null result!**

# DRD7 working groups and projects

- WG7.1: Data density and power efficiency
  - Silicon photonics transceivers
  - Powering next generation systems
  - Wireless for data & power
- WG7.2: Intelligence on detector
  - Programmable logic array IP
  - Radiation tolerant RISC-V processor
  - Virtual electronics prototyping
- WG7.3: 4D and 5D techniques
  - High performance ADCs and TDCs
  - Calibration strategies for timing systems
  - Timing distribution systems
- WG7.4: Extreme environments
  - Cryogenic CMOS PDKs
  - Radiation tolerance of advanced nodes
  - Proximity cooling
- WG7.5: Back-end systems and COTS
  - COTS architectures, tools and IPs
  - No back-end, full 100GbE from FE to DAQ
  - Generic back-end board
- WG7.6: Complex imaging ASICs and technologies
  - Common access to selected imaging technologies and IP blocks
  - Common access to 3D advanced integration

- WG7: Technologies and tools

# Interface with other DRDs

- R&D in electronics is cross-boundary
- DRD7 tasks
  - Develop and maintain common IPs and subsystems, encompassing hardware, firmware and software
  - Develop common, generic complete components or system when too complex to be designed in a single DRD
  - Provision access to vendors and tools
  - Review system specifications and designs as requested
- DRDx specific projects
  - Determination of system parameters and specifications
  - Planning and costing of prototype development and productions
  - Production, verification and integration of ASICs and other project-specific components
  - Testing and operation of large scale projects

# A DRD7 project example

- **WP71.b Power efficiency**
  - **Reduced power voltage ⇨ more bias current ⇨ heavier cables**
- **Project goals: improve power efficiency and reduce material budget in future detectors**
- **Characterisation of new HV technologies and IP developments**

**Parallel Powering (DCDC)**

Contribution from:

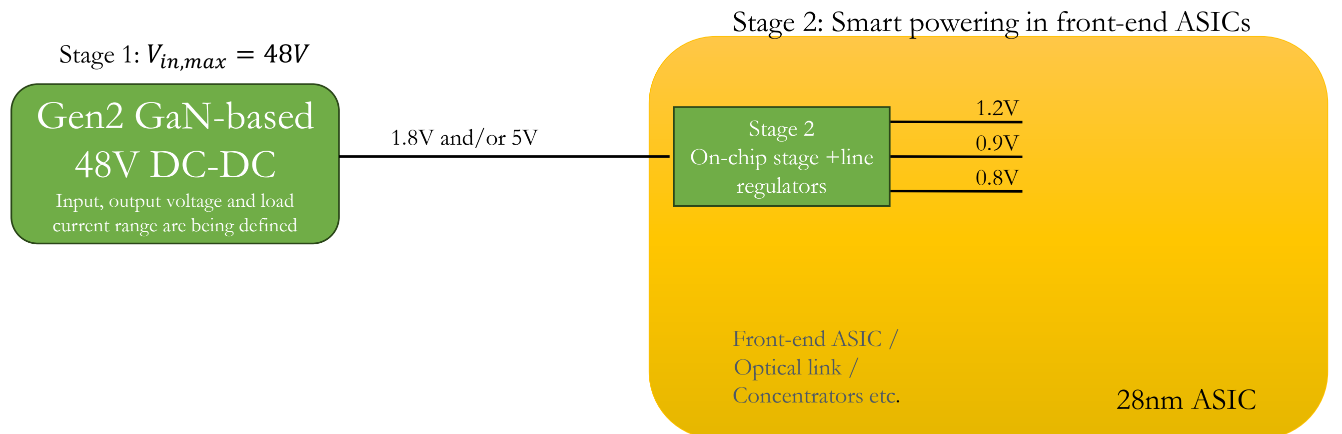
- CERN
- FH Dortmund
- RWTH Aachen
- TU Graz
- UNIUD
- UNIMI+INFN

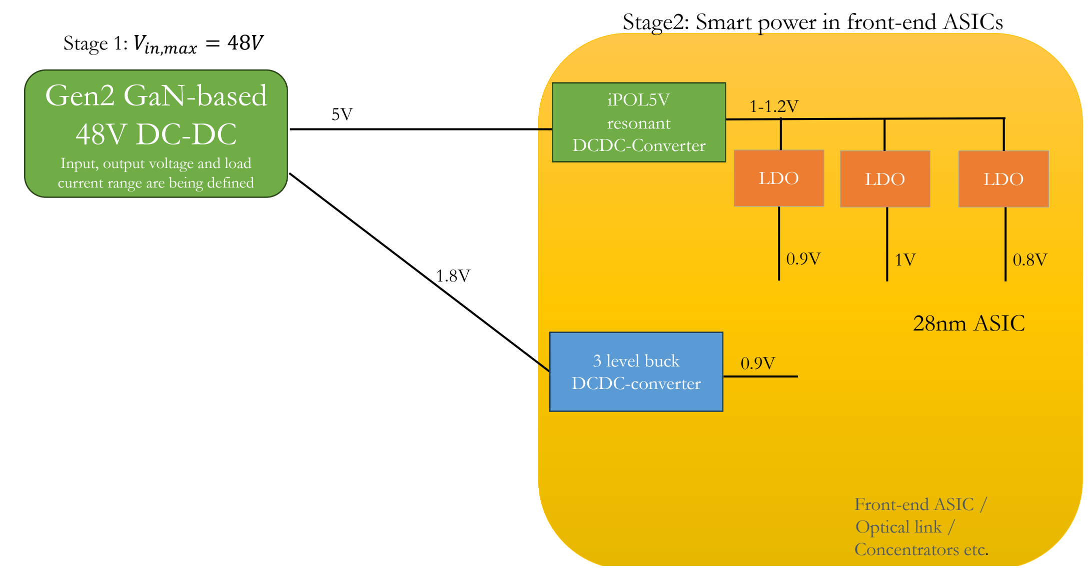
**Serial Powering**

Contribution from:

- FH Dortmund
- ITAINNOVA
- UNIMI+INFN

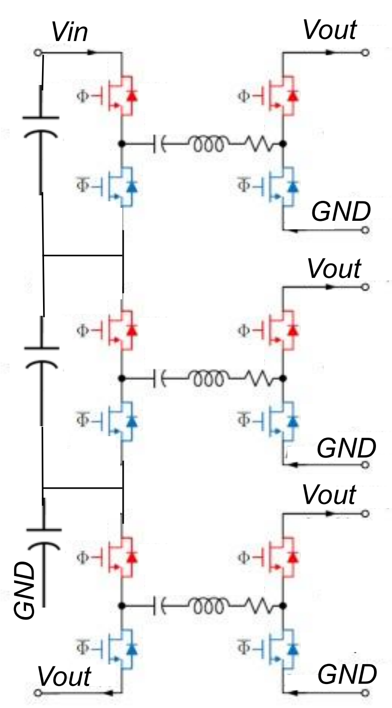
# Introducing on chip DC-DC converters

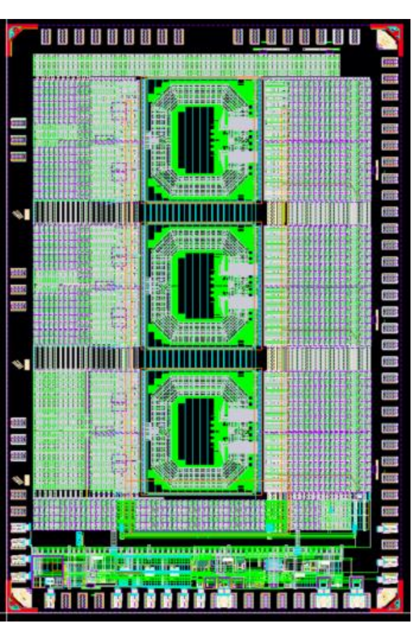


# On chip DC-DC IP example

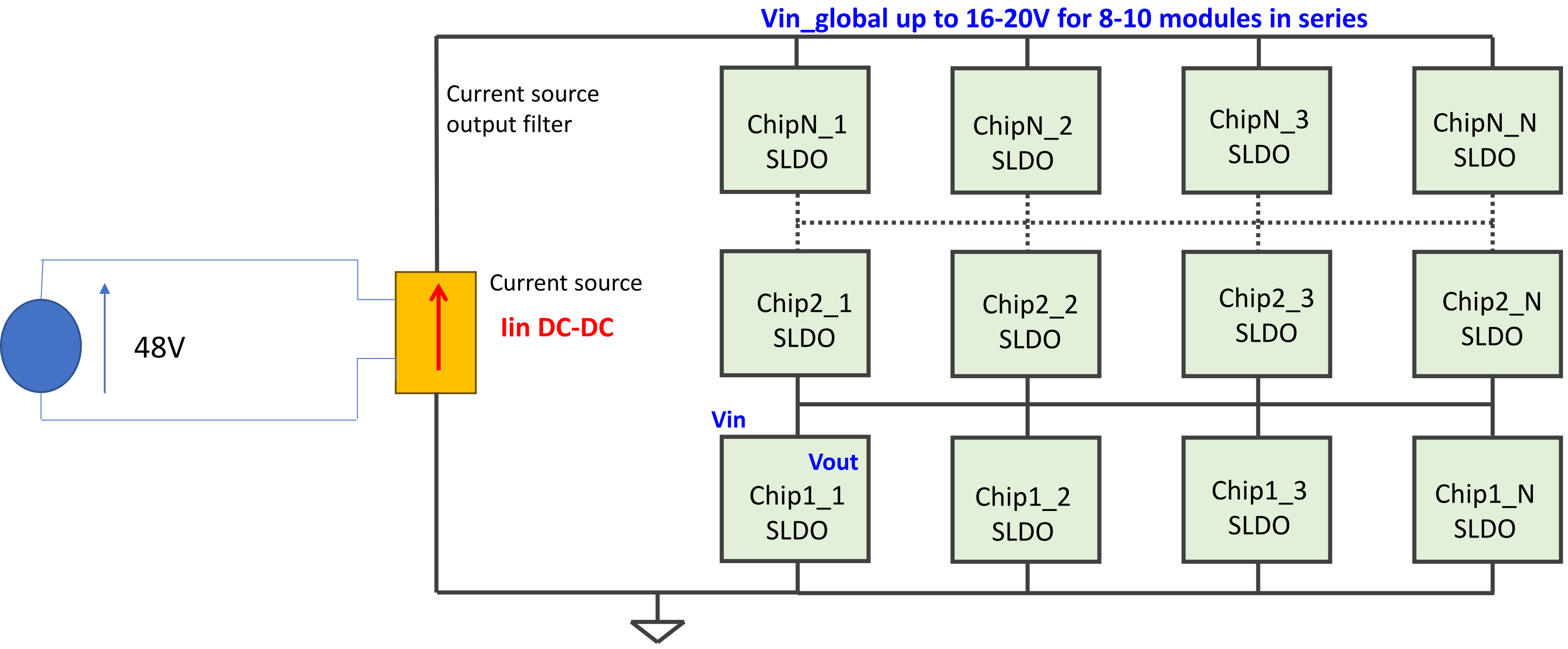
- iPOL5V
- 28 nm fully integrated DC-DC converter
- Input 5 V
- Output 0.9 V - 1 V @ 500 mA
- Radiation tolerante: 1 Grad



3.2 x 2.1 mm

# Serial powering




- **Deploying novel and more efficient shunt LDO**
- **Serial powering for CMOS sensors (encouraging results form ATLASPIX3**

# DRD7 status and plans

- Two workshop held (September and March 2023)
  - https://indico.cern.ch/event/1214423/ (March 2023)
  - https://indico.cern.ch/event/1318635/ (Sept 2023)
- Letter of intent issued on September 15th, 2023
  - https://indico.cern.ch/event/1318635/contributions/5551432/attachments/2720844/4726969/DRD7%20Letter%20of%20IntentV2.1.pdf
- Collaboration proposal being worked-out for end of the year