

Experimental Research

Design and testing of a new tracking system for the PRM measurement at AMBER experiment at CERN

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Apparatus for Meson and Baryon Experimental Research (AMBER, NA66)



AMBER program

	Beam	Target	Additional Hardware			
Proton radius measurement	100 GeV muons	high pressure Hydrogen	active target TPC, tracking stations (SciFi, Silicon)	1 /ed)		
Antiproton production cross section	50 GeV - 280 GeV protons	<i>LH</i> ₂, <mark>LHe</mark> 2023	Liquid He target	hase	approv	2023 -> 2029
Drell-Yan measurements with pions	190 GeV charged pions	Carbon, Tungsten	vertex detector	<u>с</u>	_	
Drell-Yan measurements with Kaons	~100 GeV charged Kaons	Carbon, Tungsten	vertex detectors, 'active absorber'	ation)		
Prompt photon measurements	> 100 GeV charged Kaon/pion beams	LH2, Nickel	hodoscopes	se 2 repar		2020 >
K-induced spectroscopy	50 GeV - 100 GeV charged Kaons	LH ₂	recoil ToF, forward PID	Pha (in p		2029->
Meson radii	50 GeV to 280 GeV charged pions and Kaons					

AMBER PRM



Proton-radius puzzle

Bernauer et al., A1 coll. [PRL 105 242001 (2010)] Pohl et al., CREMA coll. [Nature 466 213 (2010)] Zhan et al. [PLB 705 59 (2011)] • Mohr et al. [Rev. Mod. Phys. 84 1527 (2012)] Antognini et al., CREMA coll. [Science 339 417 (2013)] Mohr et al. [Rev. Mod. Phys. 88 035009 (2016)] Beyer et al. [Science 358 6359 (2017)] Fleurbaey et al. [PRL.120 183001 (2018)] Tiesinga et al. [Rev. Mod. Phys. 93 025010 (2021)] Mihovilovič et al. [arXiv:1905.11182 (2019)] Bezginov et al. [Science 365 1007 (2019)] Xiong et al. [Nature 575, 147-150 (2019)] Proposal AMBER [SPSC-P-360 (2019)]



Missing: muon-proton with E_{μ} of 10 - 100 GeV

- Test of lepton universality
- Different systematics compared to others

Proton Radius Measurement @ AMBER

- Aimed precision of charge-radius below 1%
- Aimed Q²-range: 0.001 GeV²/ c^2 to 0.040 GeV²/ c^2

□ Measurement of low-Q² elastic-scattering events 3.0 m 2.5 m 3.0 m Incident muor AMBER approach: Combined measurement of low energetic recoil-protons and scattered muons at small scattering-angles. Hydrogen filled Time-Projection-Chamber (TPC) as an ECAL2 HCAL2 active target to measure recoil protons Silicon trackers along long leaver-arm to measure small scattering-angles (<100 μ rad) ECAL1 SM₂ HCAL1 Scintillating fibers for timing (~1ns) and tracking New continuously-running DAQ required Muon Filter 2 SM1 Momentum measurement of scattered muon Target TPC Radiative background using electromagnetic calorimeter Muon Filter 1 RICH1

Muon identification with muon filter and hodoscope 18/10/2023 VERTEX 2023 Vertexing design for PRM@AMBER

spectrometer











UTS concept & status

- Silicon pixel detector (ALPIDE) and Scintillating-Fiber Hodoscope (SFH) combined in Unified Tracking Station (UTS)
- Three layers of pixel detectors in combination with four planes of scintillating fibres
- Reduced material budget in the active ~10x10 cm² area
- He atmosphere



SFH design

- Four planes of square scintillating fibers (500 μm edge length, Kuraray SCSF-78)
- 196 fibers per plane, active area of ~9x9 cm²
- Packages containing eight fibers each



- SiPM arrays: Hamamatsu S13361-3050 (8x8)
- CITIROC's discriminator, ifTDC readout





SFH detector first results



2022





Improved prototype with changes in SiPM coupling, clamping fiber and assembly procedure for two new detector planes



2023





2 3 Position along fiber [cm] 12

18/10/2023

Silicon (ALPIDE) detector design

- 15 mm (Y) × 30 mm (X) sensor, 512 x 1024 pixels
- 29.24 x 26.88 (X × Y) μm²
- Thickness 50 µm •
- 1.2 Gb/s Serial Data port •
- Flex PCB with 10um thick Al conductors ٠
- 240 um thermo-conductive carbon fibre plate
- Heat exchange through water cooling ٠
- Gas tight mechanics ٠







ALPIDE

Assembly order



Some moments of the assembly



First RO of the first FPC



Silicon (ALPIDE) detector status

Testing of the ALPIDE for the running conditions



Assembly of the FPC



Assembly on the carbon support





18/10/2023

DAQ concept

Combination of slow and fast detectors with a continuous readout and software trigger logic for data reduction.

Free-running Triggered readout readout Hardware Front-End Trigger Front-End Logic Layer 1 Data Multiplexer Hardware Data Filter Laver 2 Multiplexer Data Multiplexer Event Timeslice Builder Builder Storage Software PC FPGA High-level trigger Storage/CDR Permanent storage/CDR HLT Spill Slice 1 Slice 2 Slice 2^20 software Very slow Detectors Image 1 Image 2 Image 2 Image 1 Image 2 Image 1 (TPC, ...) ... Slow Detectors Image 1 Image 200 Image 1 Image 200 Image 1 Image 200 (DCs, W45, ...) Fast Detectors

Data stream sorted in time slices

- Detector data ordered in time images based on to resolution
- Hardware event builder stores data

• High-level trigger selects time slices + images

•

New DAQ hardware installed; tests are ongoing

VERTEX 2023 | Vertexing design for PRM@AMBER

(Hodoscopes, SciFis, ...)

DAQ status

2023 test running was mostly dedicated to the DAQ



iFTDCs were operational







Conclusions & plans

- Presently both the parts of the UTS are preparing full size prototypes that are to be tested parasitically
- Major effort is done to be able to test a fully equipped setup in the autumn of 2024 as part of the PRM test running
- We are targeting to demonstrate the full running capability of the UTS based vertexing to support the request for 2025 full year data tacking





SPARES



Proposal of a New Measurement

High-energy elastic muon-proton scattering

Measurement of the cross-section of elastic muon-proton scattering using the *CERN M2* beamline. (SPSC-P-360)

$$< r_p^2 > = -6\hbar^2 \cdot \frac{dG_E(Q^2)}{dQ^2} \bigg|_{Q^2 \to 0} \qquad \qquad \frac{\mathrm{d}\sigma^{\mu p \to \mu p}}{\mathrm{d}Q^2} = \frac{4\pi\alpha^2}{Q^4} R\left(\epsilon G_E^2 + \tau G_M^2\right)$$

- Measure as close as possible to $Q^2 \rightarrow 0$
- \rightarrow suppress influences from higher order form-factor terms
- \rightarrow high-energy $\mathcal{O}(10 100 \text{ GeV})$ Cross-section $\propto G_{E^2}$
- Disagreement on experimental data: PRad and MAMI
- Sufficient range to determine radius:
- \rightarrow Aimed precision of below 1 %
- \rightarrow Aimed Q²-range: 0.001 0.04 GeV²/c²
- Below Q² = 0.001 GeV²/c²:
- \rightarrow Deviation from point-like proton level of $\mathcal{O}(10^{-3})$
- \rightarrow Smaller than unavoidable systematic effects
- Above $Q^2 = 0.04 \text{ GeV}^2/c^2$:
- \rightarrow Non-linearity of the cross section
- \rightarrow Predominant source of uncertainty



layer	t item	А	Ζ	d	density	X_0	X/X_0	contrib.
			(u)	(cm)	$\left(g/cm^{3}\right)$	$\left(g/cm^{2}\right)$	(%)	(%)
1	solder mask (epoxy)			0.0030	1.250	34.99	0.011	4.64
2	aluminum layer (Al)	26.982	13	0.0014	2.699	24.01	0.016	6.82
3	Kapton			0.0010	1.420	40.58	0.003	1.516
4	aluminum layer (Al)	26.982	13	0.0014	2.699	24.01	0.016	6.82
5	solder mask (epoxy)			0.0030	1.250	34.99	0.011	4.64
6	glue flex (C)	12.011	6	0.0050	0.958	43.01	0.011	4.82
7	ALPIDE (Si)	28.085	14	0.0050	2.329	21.82	0.053	23.12
8	glue to plate (C)	12.011	6	0.0080	0.958	43.01	0.018	7.72
9	carbon fleece (C)	12.011	6	0.0020	0.400	43.01	0.002	0.81
10	cold plate (C)	12.011	6	0.0240	1.583	43.01	0.088	38.28
11	carbon fleece (C)	12.011	6	0.0020	0.400	43.01	0.002	0.81
	Total:			0.0558			0.231	100.00

Table 1.2: Material budget for the FDI-A-24 Flex-based stack with aluminum conductors. [43]

Picture 5

Power: Heat flux= 50mW/cm2 - 0,225W/chip - 1,350W/HIC TOTAL Power= 4,050 W

23

Temperature map on the carbon support





ALPIDE DAQ Boards

- Centred around a Kintex-7 FPGA: K160T-FFG676.
 - 8 GTX transceivers up to 12.5 Gbps.
 - Plenty of I/Os.
- 6 transceivers for **ALPIDE** data reception.
- 2 transceivers to SFP+.
- 1 **Ethernet** (10/100/1000) interface.
- On-board **clock generation** with Si5344/Si5394.
- Additional clock I/Os on optional **SMA or LEMO connectors**: 2 for transceivers, 2 for FPGA fabric.
- **3 versions** designed so far, the last two meant to overcome the chip supply issues:
 - Variations to power and clock generation.
- 19 boards have been produced.
- Next generation board based on Kintex UltraScale.



2023-07-25

Carlos García Argos (Uni. Freiburg

18/10/2023

25

3/11

DHmx/DHsw

- Backbone module of DAQ
 - FPGA: XC6LX130-2
 - 4GB DDR3 Memory, 3GB/s throughput
- Firmware versions
 - LV0 MUX for iFTDC with UCF links
 - Time Slice Builder (Switch), 5 GB/s throughput
 - Future: LV1 MUX



iFTDC

• Specification

- ARTIX7 FPGA XC7A-50-2
- 64 channels,
- Programmable signal edge or both edges
- Bin size : 0.8 ns, 0.4 ns, 0.2 ns (32 channels)
- Time resolution : 300ps, 170 ps, 100 ps
- Differential nonlinearity : 10%, 20%, 40%
- Trigger less capable data flow

Applications

- MWPC
- Drift Chambers
- SciFi



