Development of the radiation-hard MALTA CMOS sensor for tracking applications

Giuliano Gustavino

Phil Allport, Ignacio Asensi Tortajada, Prafulla Behera, Dumitru Vlad Berlea, Daniela Bortoletto, Craig Buttar, Florian Dachs, Valerio Dao, Ganapati Dash, Dominik Dobrijević, Lucian Fasselt, Leyre Flores Sanz de Acedo, Andrea Gabrielli, Martin Gaži, Vicente González, Giuliano Gustavino, Pranati Jana, Heinz Pernegger, Francesco Piro, Petra Riedler, Milou van Rijnbach, Heidi Sandaker, Carlos Solans Sánchez, Walter Snoeys, Tomislav Suligoj, Marcos Vázquez Núñez, Anusree Vijay, Julian Weick, Steven Worm, Abdelhak M. Zoubir

CERN

VERTEX 2023

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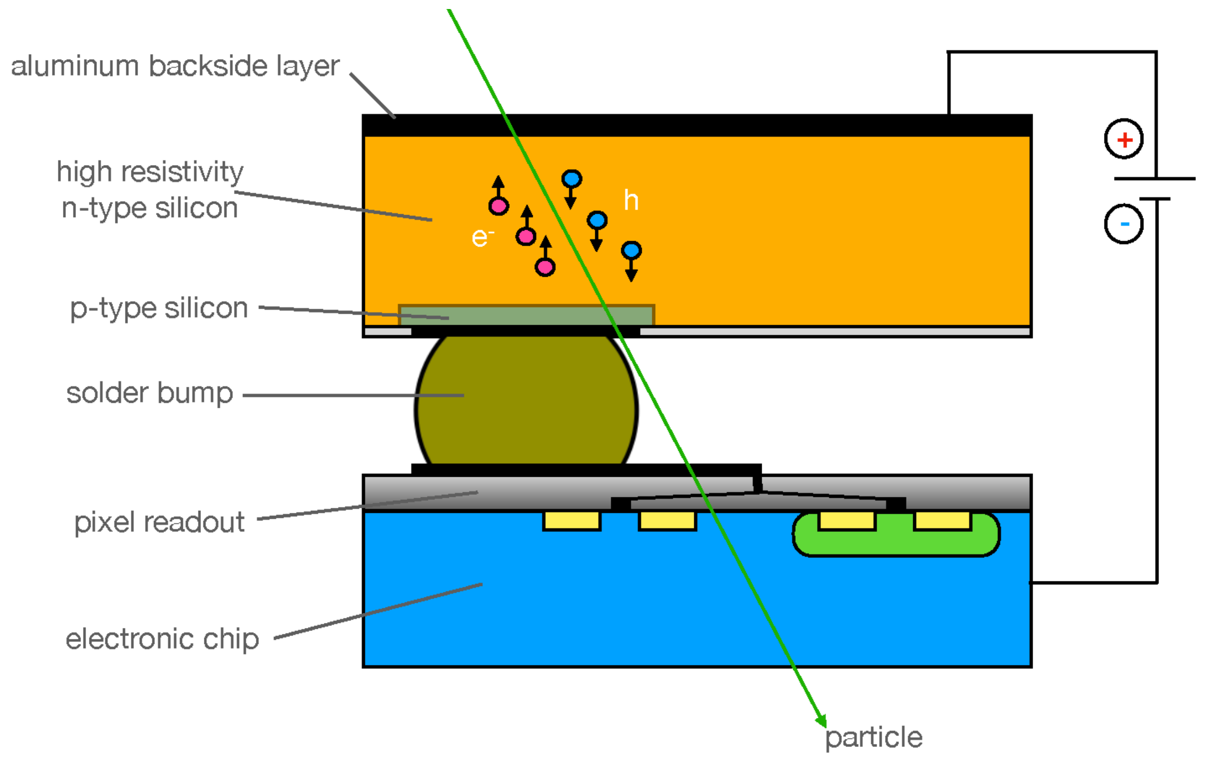
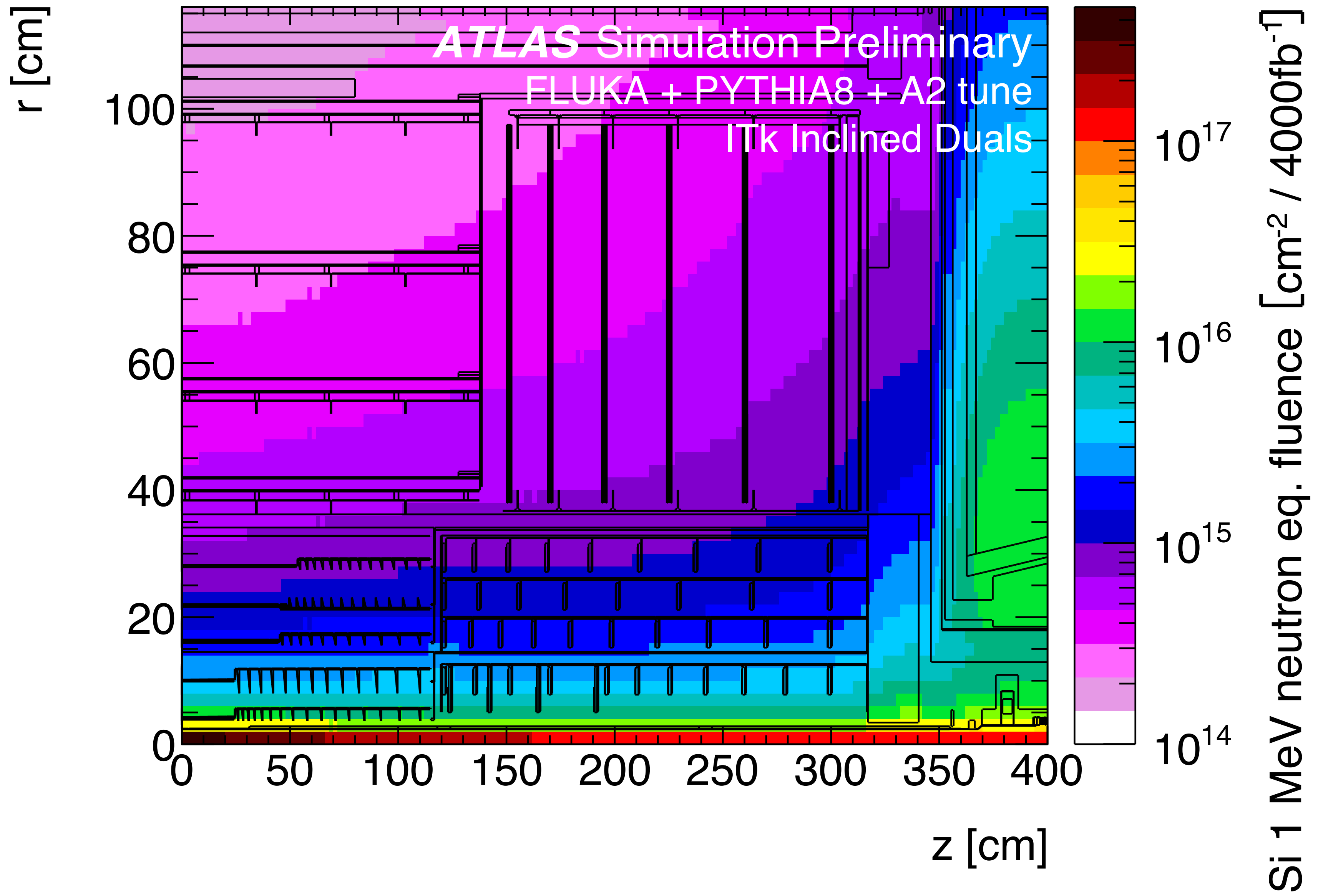
Motivation for Monolithic Pixel Sensors

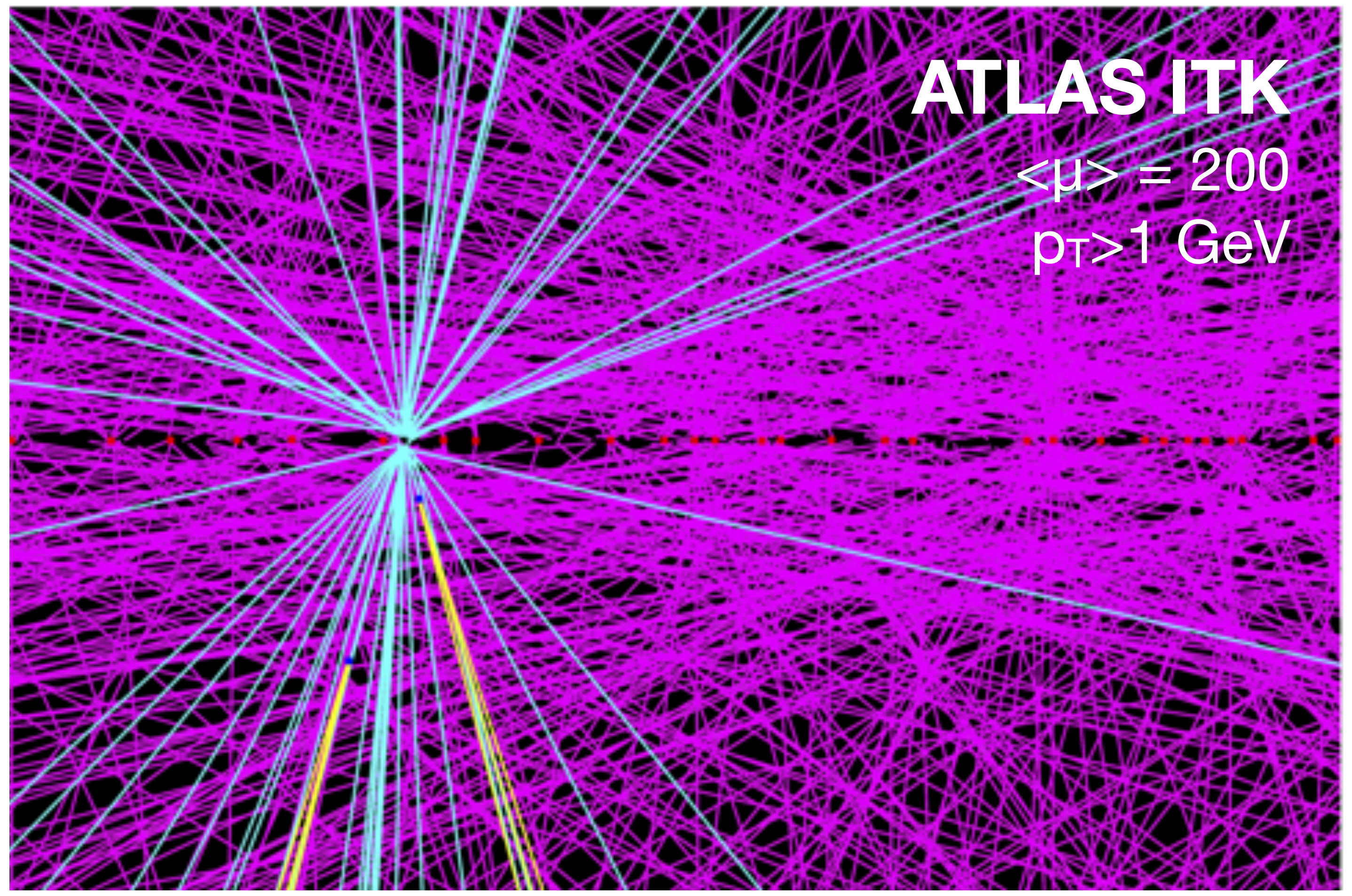


Hybrid detectors (ASIC bump-bonded to sensor) are the most adopted and field-tested solution

Challenging requirements for future collider experiments:

- Extreme radiation tolerance
- Large hit rate
- High granularity
- Fast response time
- Large surface
- Very thin



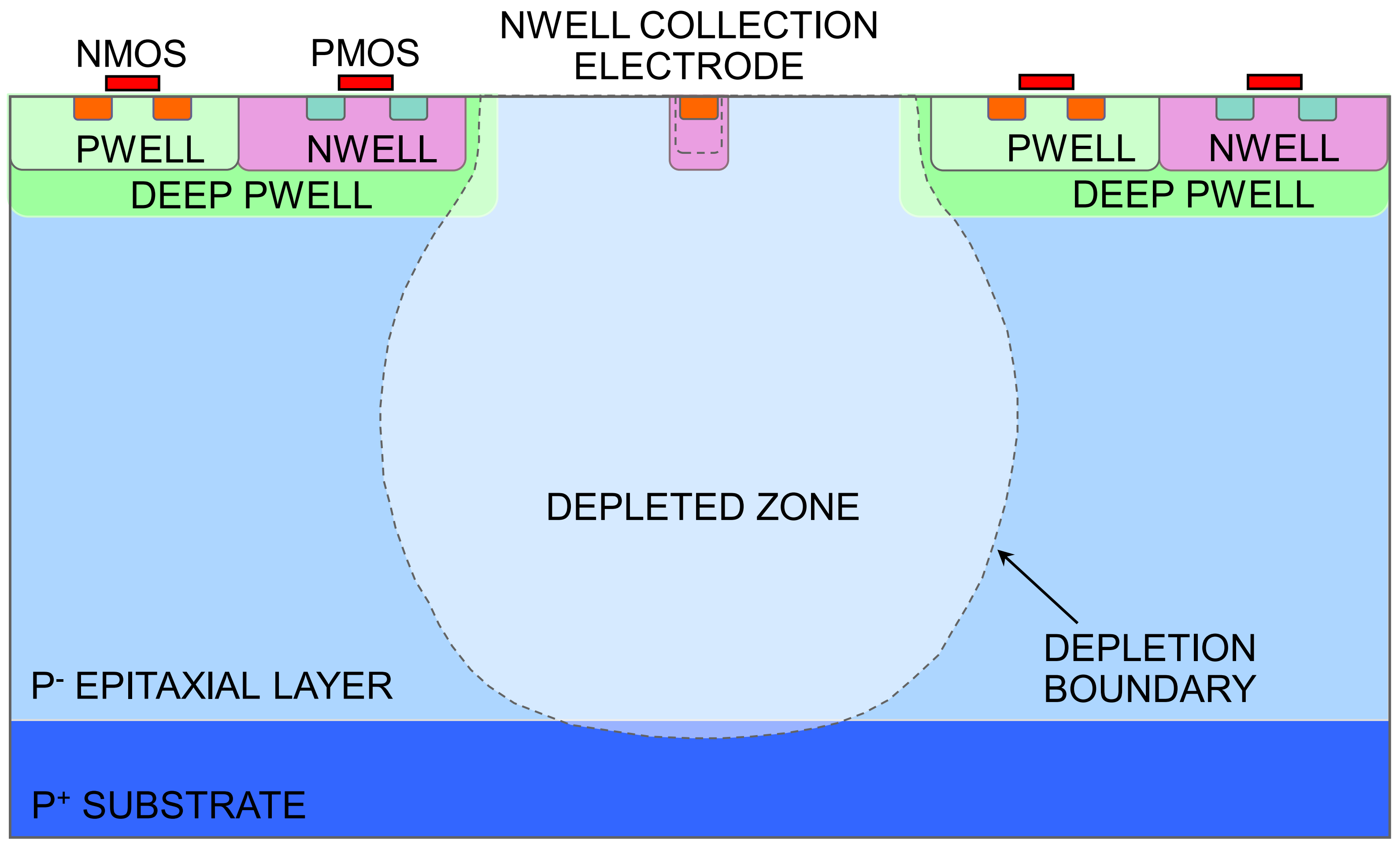


MAPS (Monolithic Active Pixel Sensors)

- ASICs and sensor on the same substrate
  - avoid custom bump bonding
  - reduced production effort
- industrial-like CMOS production process
  - reduced costs
  - large area detectors
- low mass / high granularity detectors
  - reduced material
- small capacitance
  - large signal/noise ratio
- still in R&D phase for HEP
  - in particular for what concerns radiation hardness

A MALTA ancestor:

ALPIDE - ALICE ITS



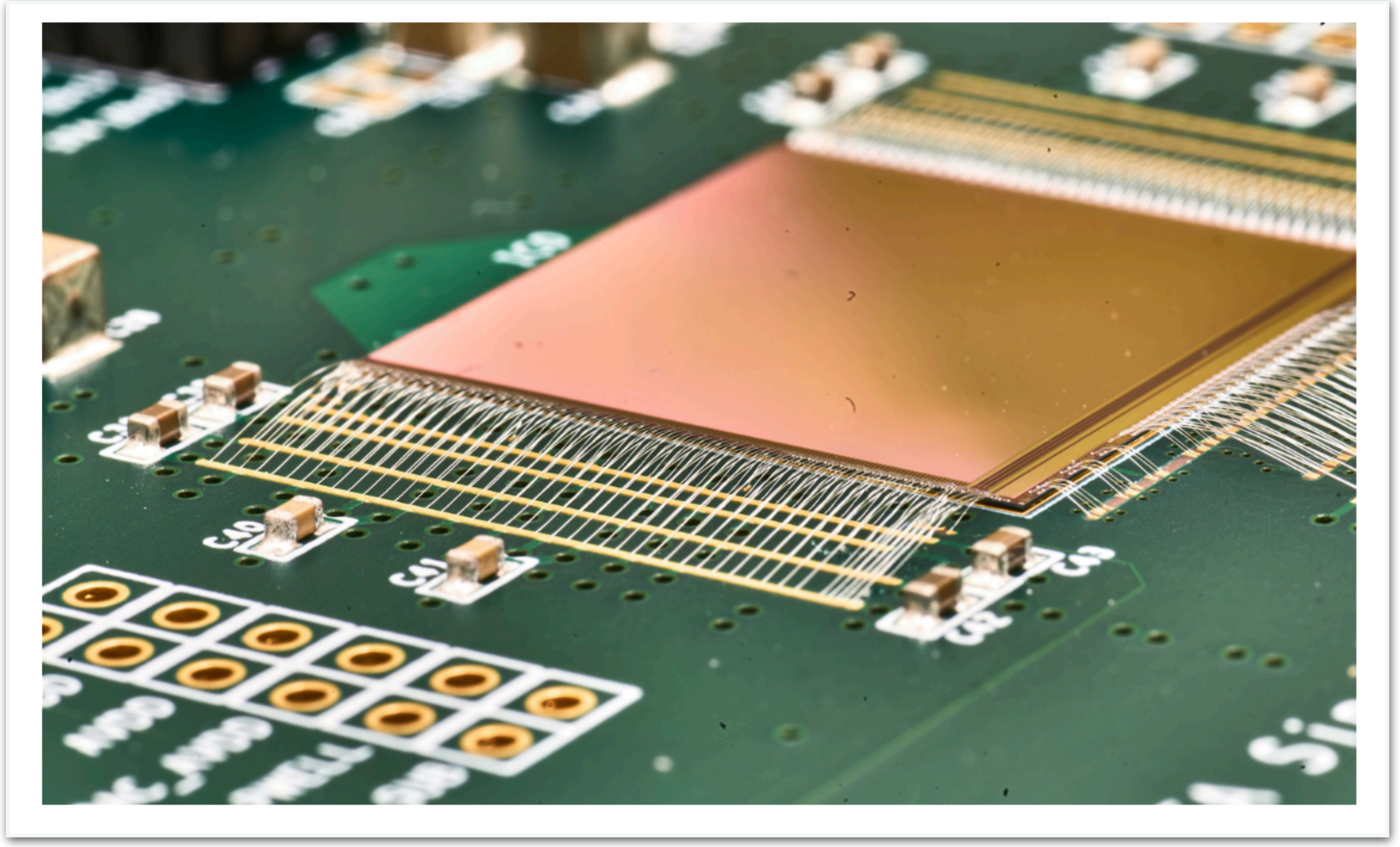
Charge collection time ~100 ns via diffusion

A MALTA cousin:

TJ-MonoPix

see L. Schall' slides for details

MALTA chip



- Full scale demonstrator*
  - 180 nm Tower CMOS imaging technology
  - 2x2 cm^2
  - 512 x 512 pixels

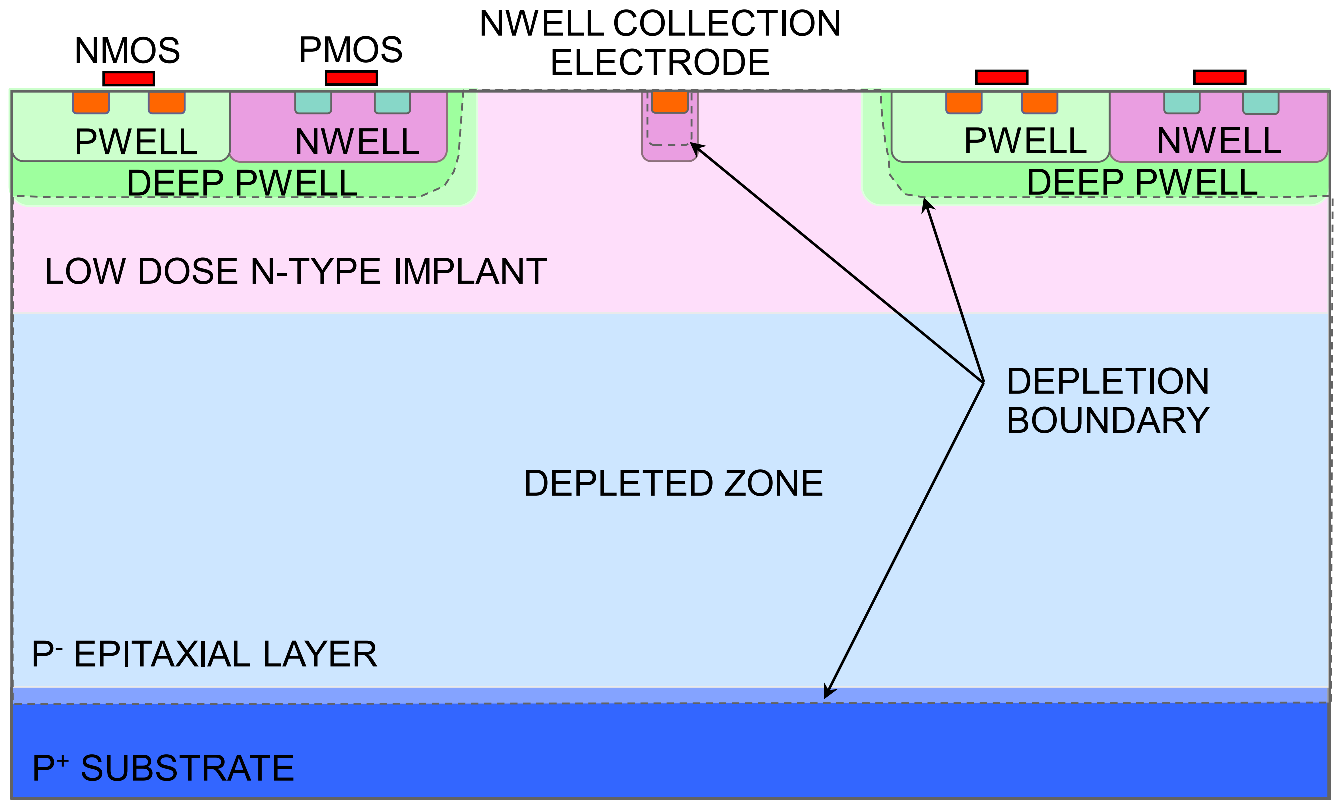
- Originally conceived for ATLAS pixel detector upgrade for HL-LHC:
  - radiation hard up to **1.5 x 10^{15} n_{eq}/cm^2** → ALPIDE: < 10^{14} n_{eq}/cm^2
  - timing response: **within 25 ns** → ALPIDE: several μsec

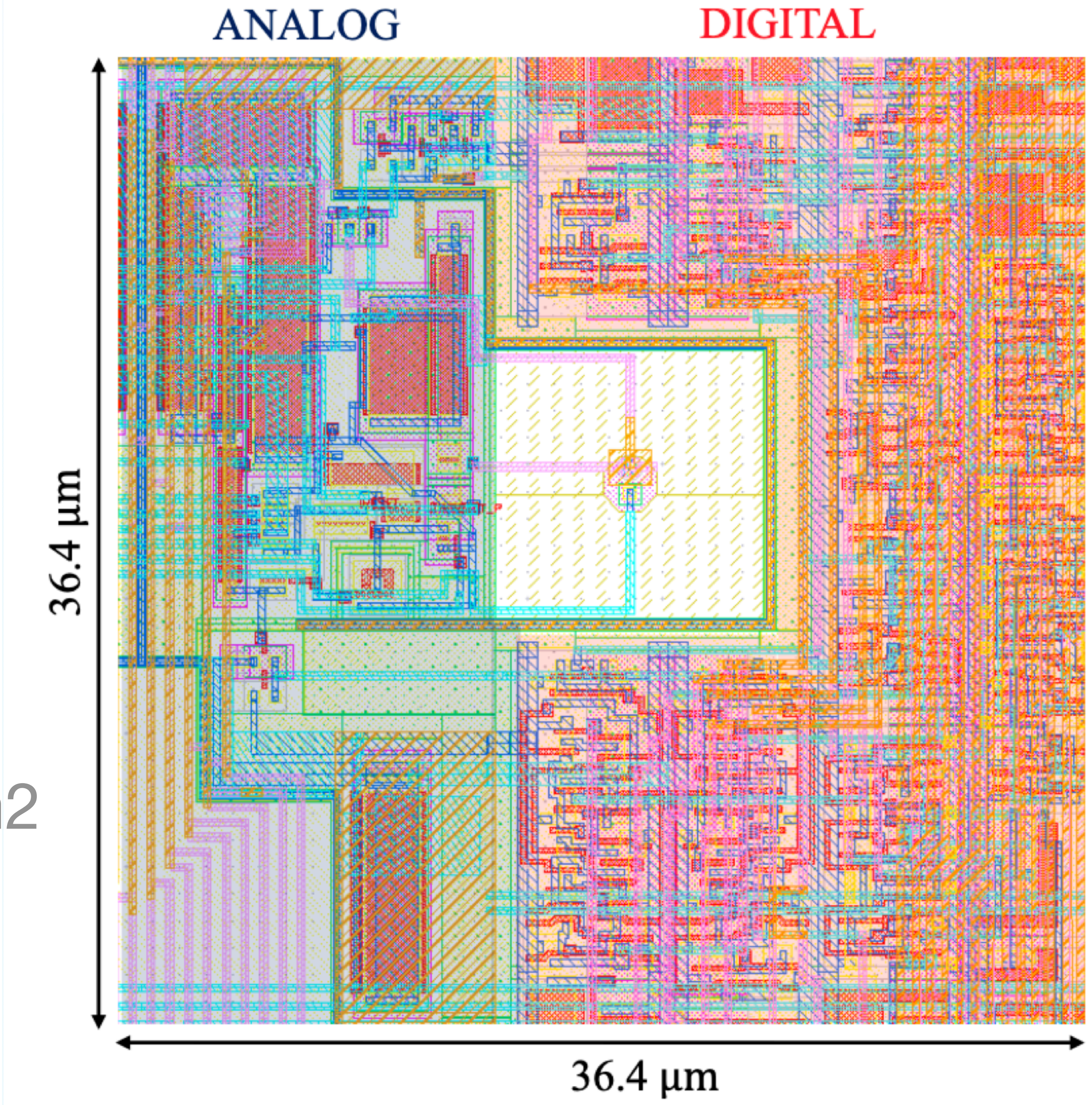
- **Asynchronous readout architecture**
  - no time-over-threshold information
  - hit info directly transmitted from chip to periphery
  - reduce power consumption and maintain hit-time information
    - high data rate (>100 MHz/cm^2)

*

MALTA Pixel

- pixel size 36.4 x 36.4 μm^2 → ATLAS ITkPIX: 50x50 μm^2
- thickness down to 50 μm → ATLAS ITkPIX: ~100 ÷ 150 μm
  - available also with 100 and 300 μm
- 3x3 μm^2 collection electrode
  - minimal capacitance (< 5 fF)
    - ENC < 15 e$^-$
- low voltage (6 ÷ 55 V) → ATLAS ITkPIX: 80 ÷ 500 V
- low power
  - 1 μW/pixel
  - 70 mW/cm2 analog power
  - 10 mW/cm2 digital power → ATLAS ITkPIX (RD53) <1W/cm2





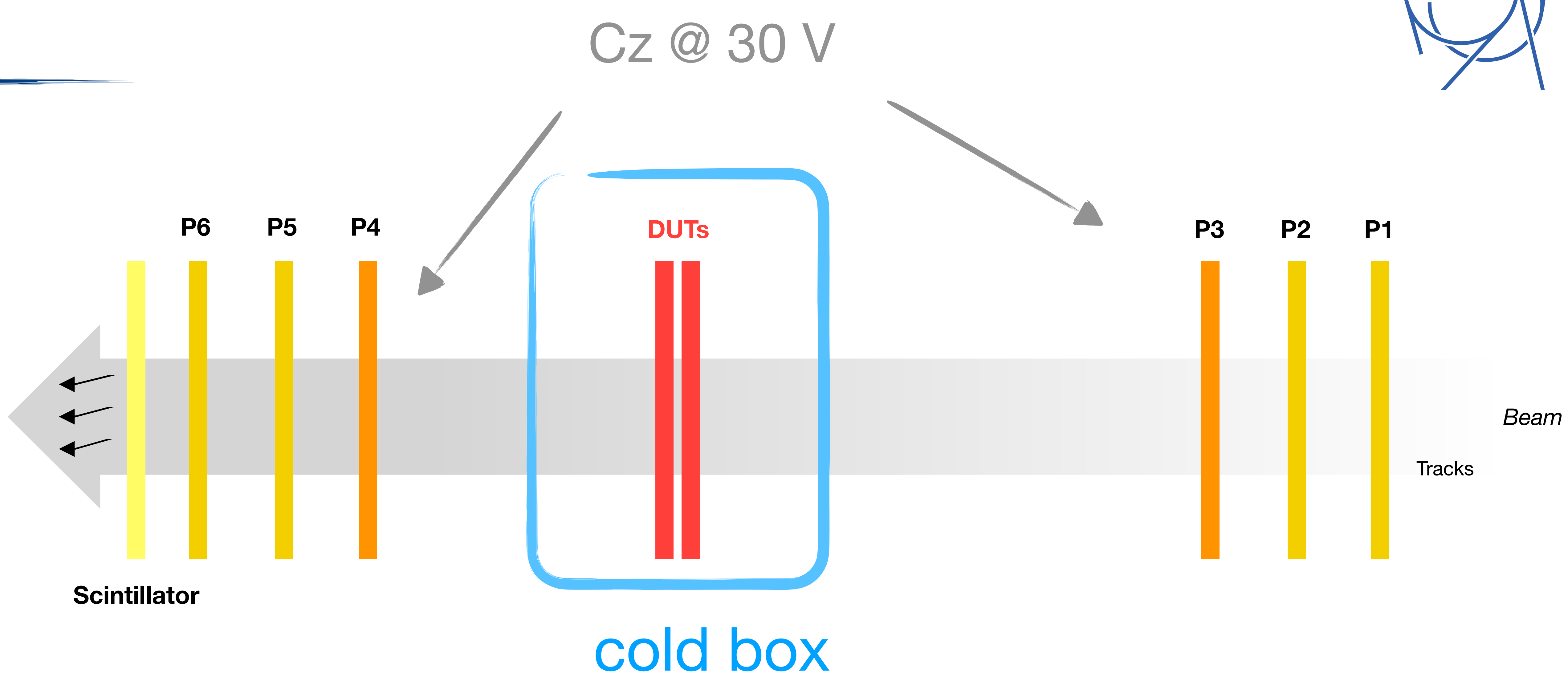
MALTA Telescope @ SPS

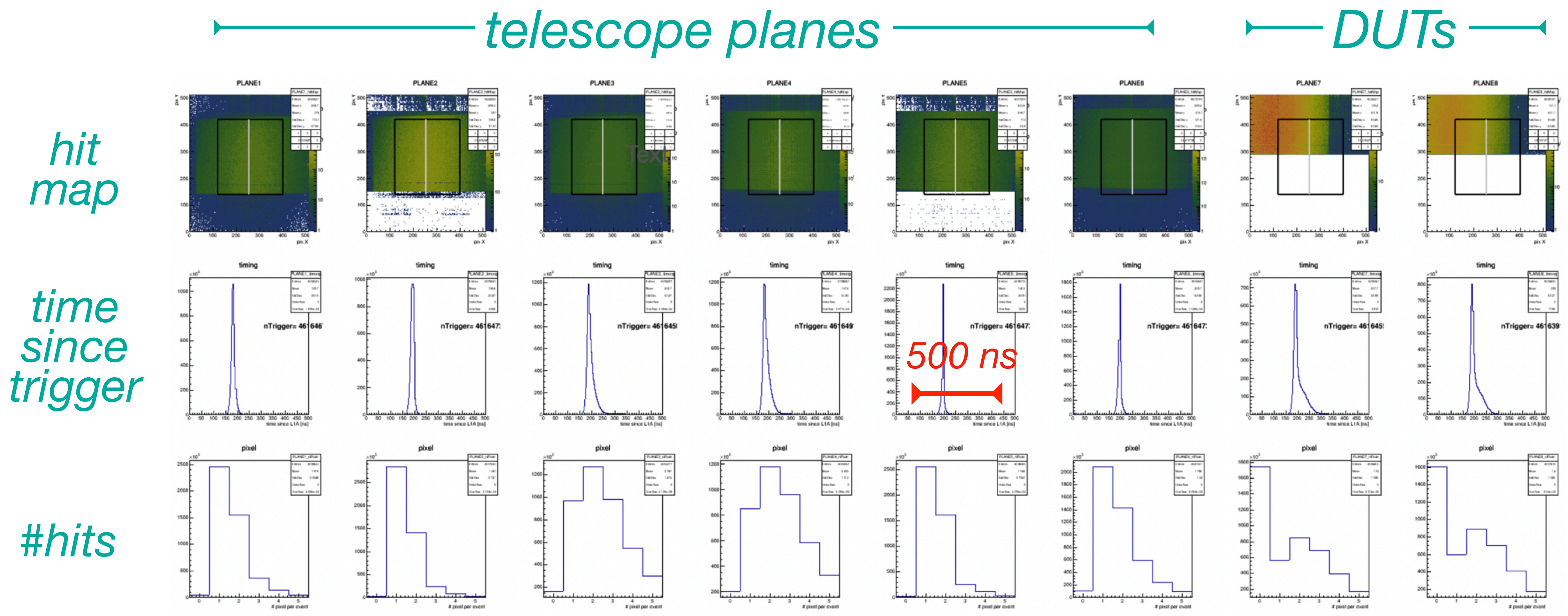
EPJC 83 (2023) 7, 581

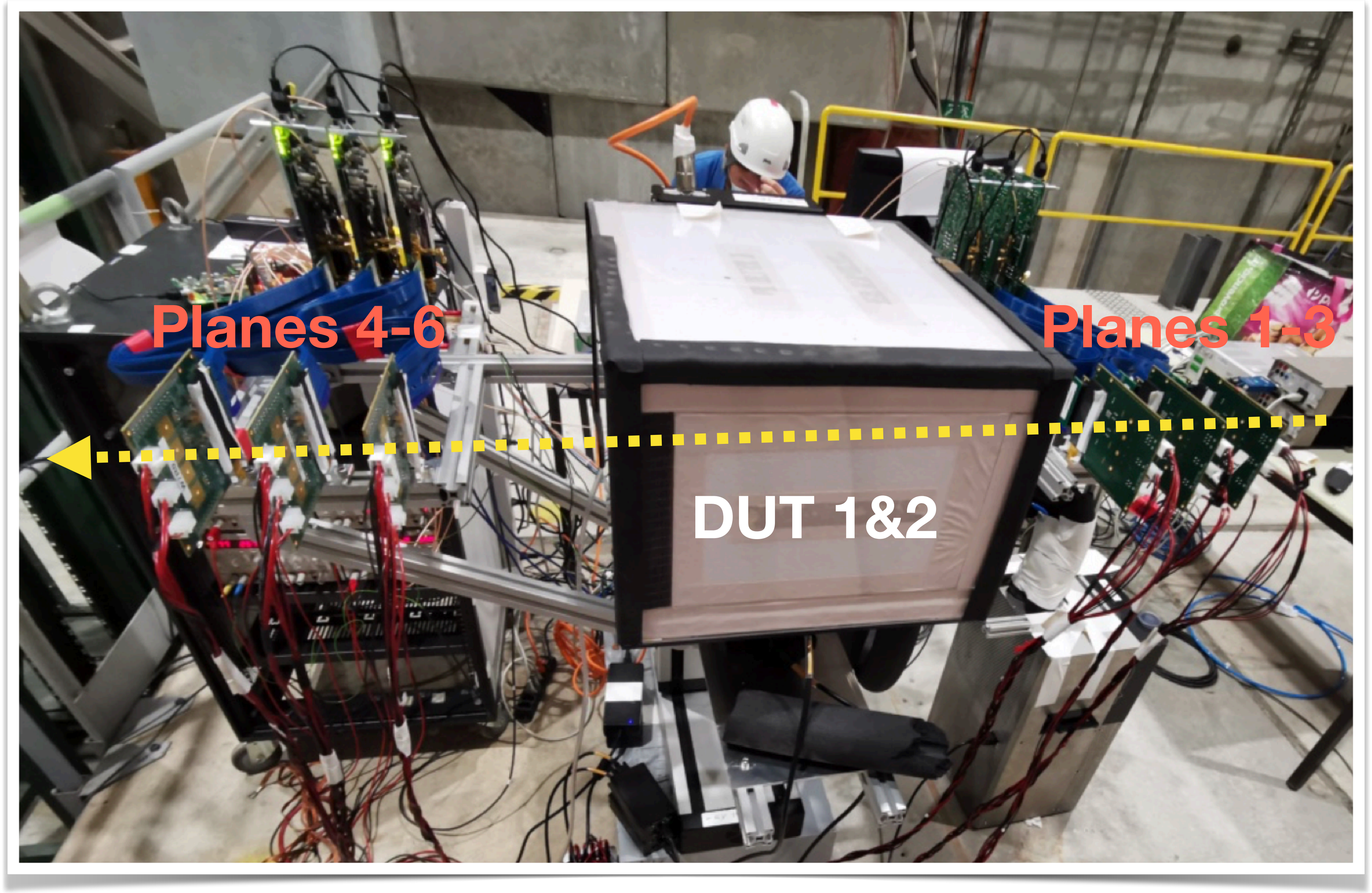
Dedicated beam telescope

with 1st generation MALTA chips:

- 6 tracking planes
  - internal Cz samples @ 30 V ⇨ *cl size ~ 2*
- scintillator for precise timing reference
- flexible TLU configurations & online monitoring
- can host different DUT sizes
- permanently installed at SPS



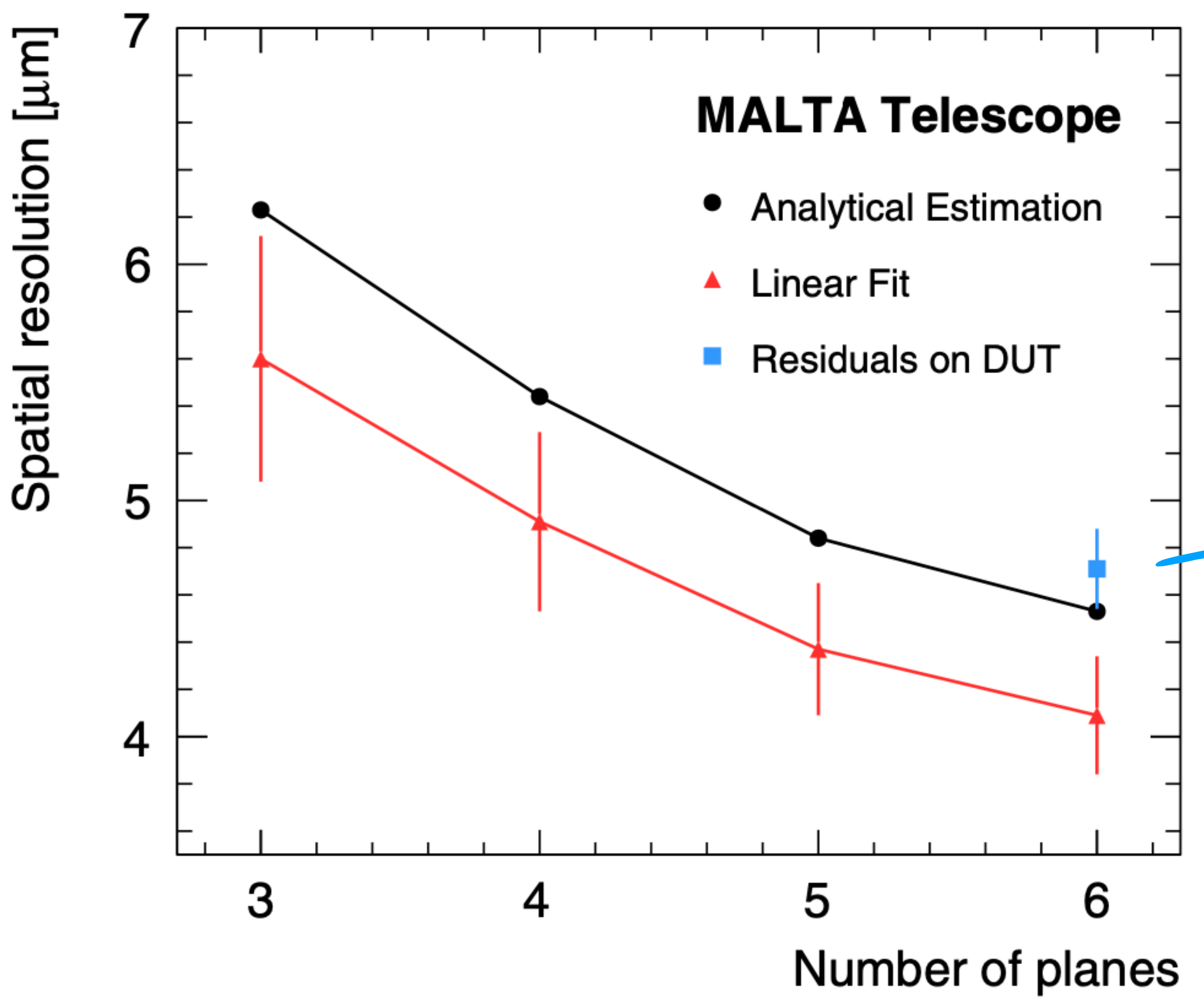


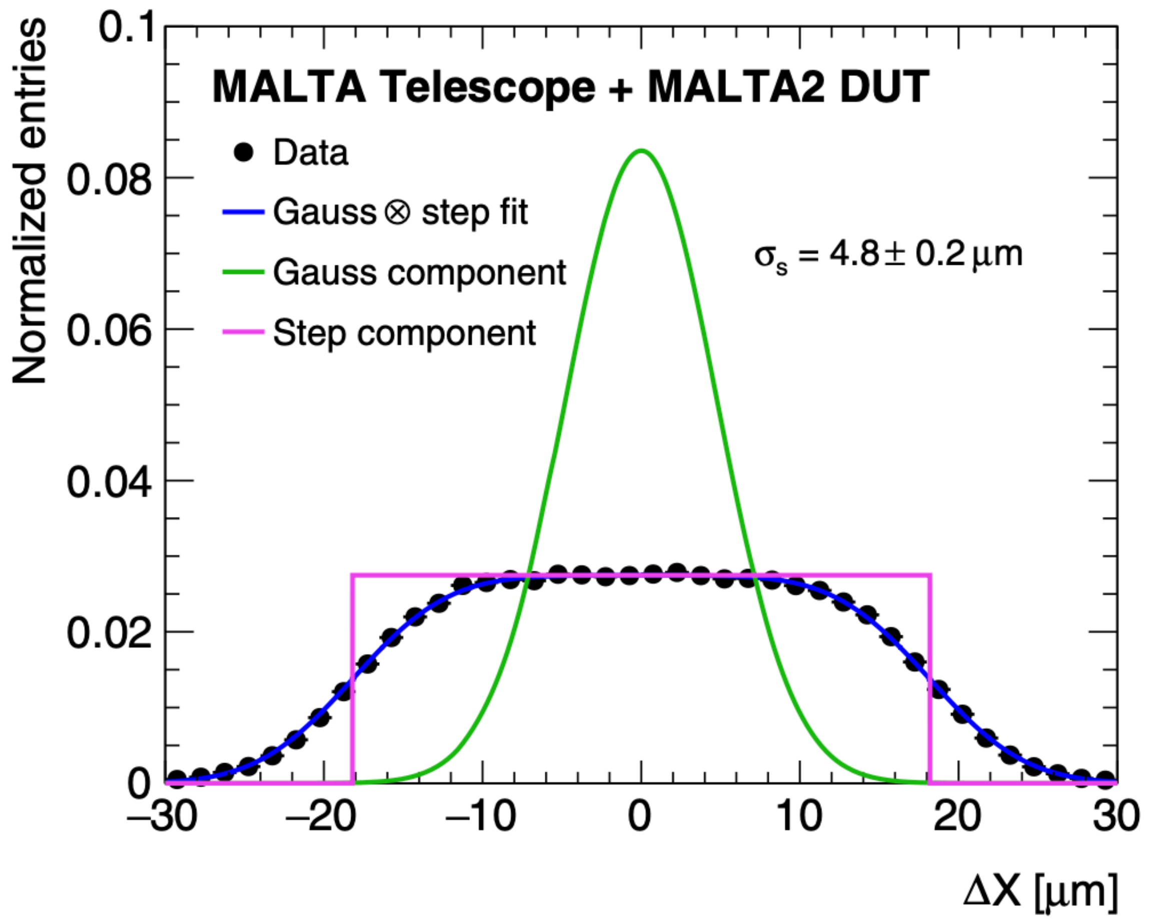


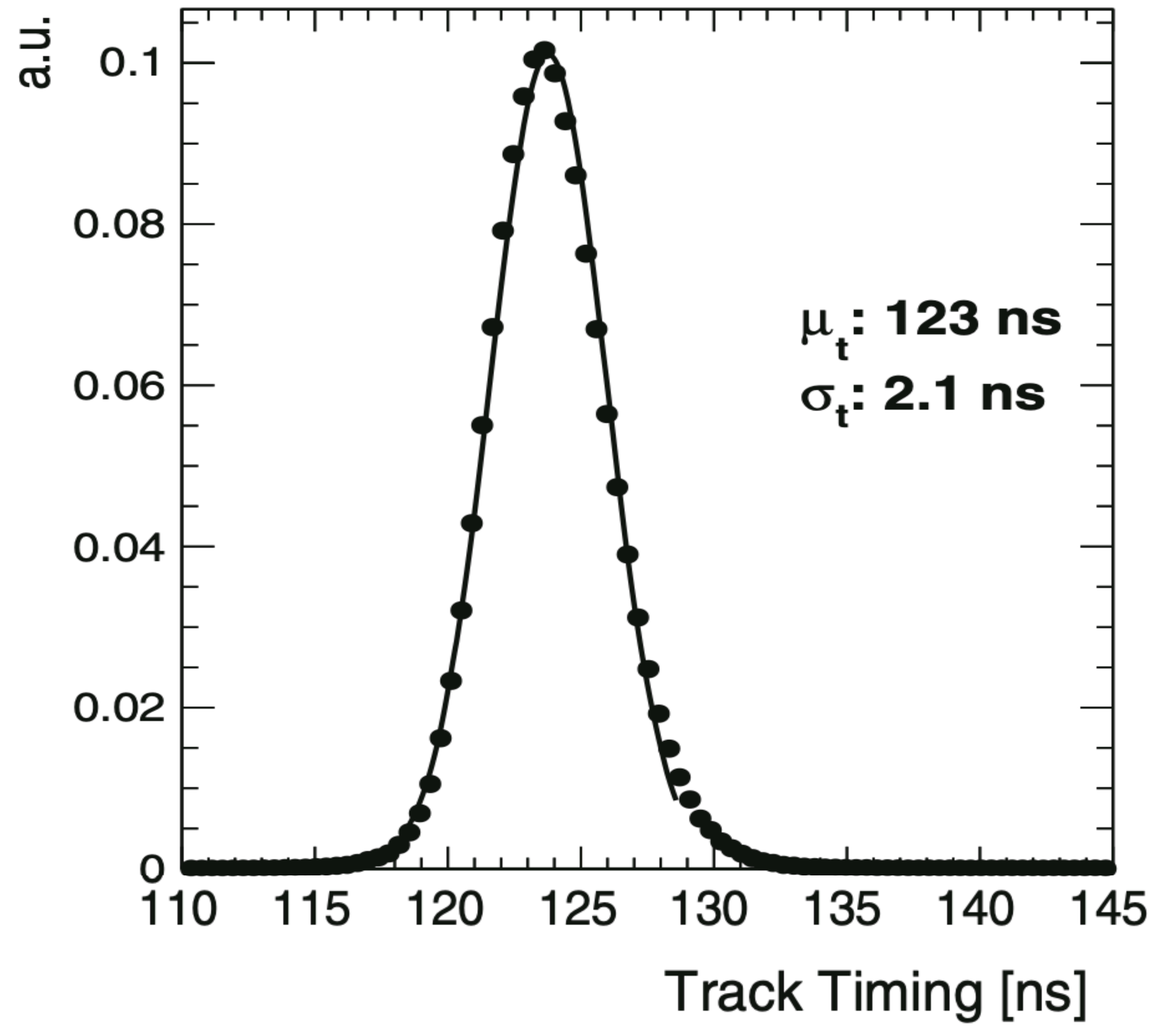
MALTA Telescope performance

EPJC 83 (2023) 7, 581

- Spatial resolution: σ_s = 4.1 μm
  - larger cluster size improves the analytical estimation
  - fit of gaus ⊗ step σ_s = 4.7 μm
    includes effects of inhomogeneity and time resolution at the edges of the DUT that are not taken into account







- average time resolution: σ_t = 2.1 ns
  - allows it to operate at high rates
    > 4×10^6 particles per spill

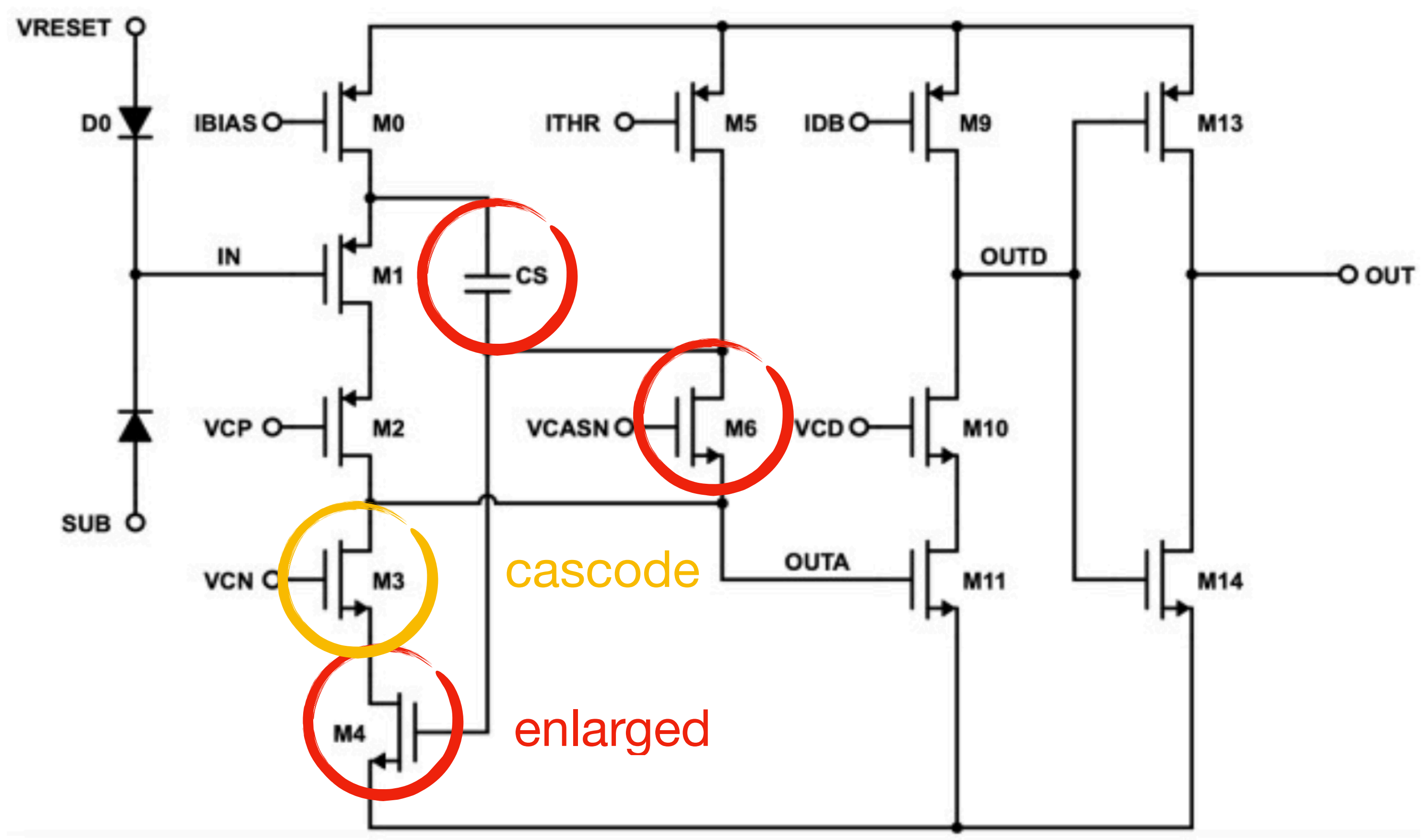
It is currently used to characterise MALTA chips, BCM', ITk pixels, HGDT's LGAD

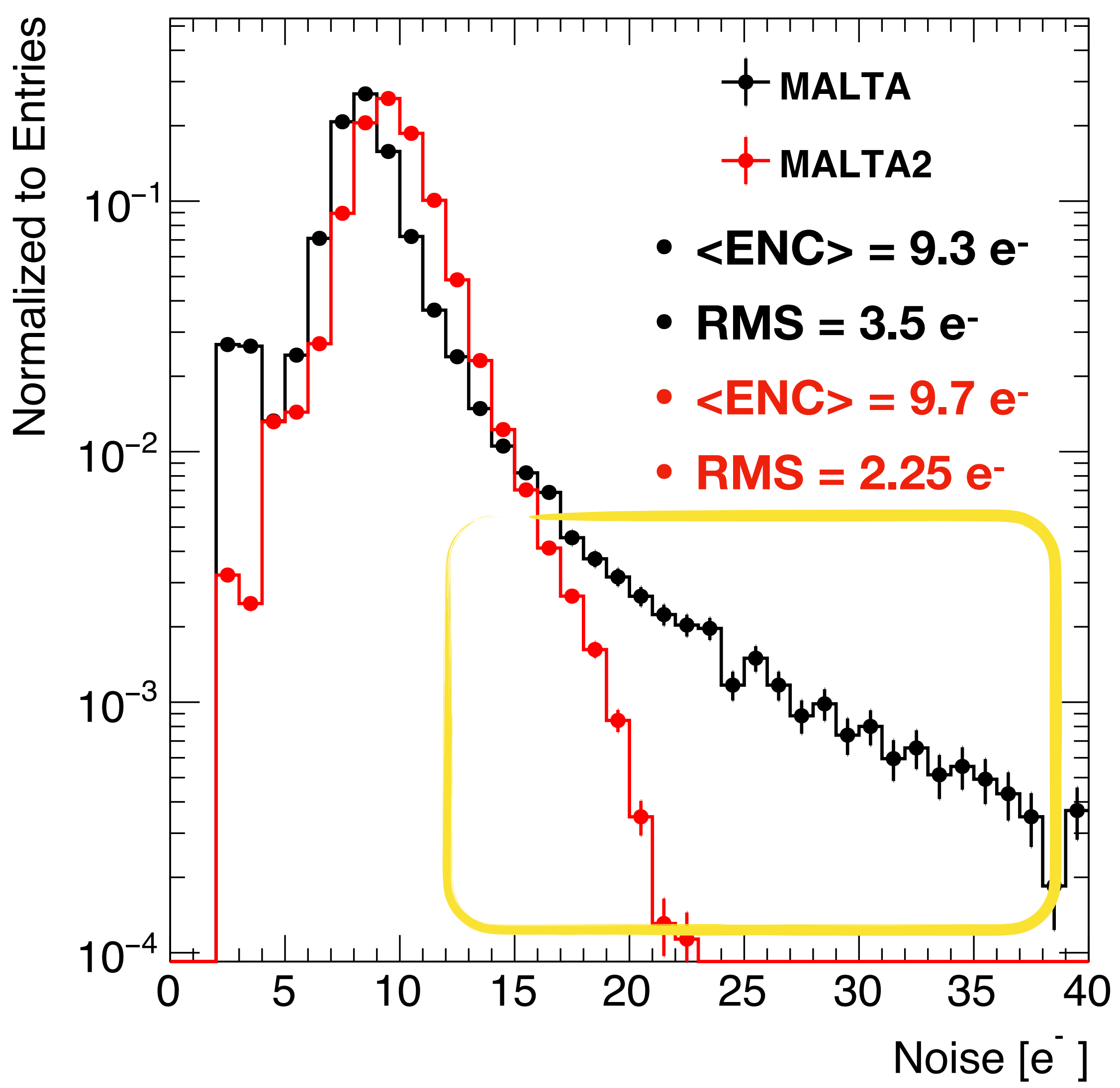
MALTA2 processing

[Malta2 public plots](#)

Improved the FE in MALTA2

- enlarged transistors & cascode stage
  - lower noise & higher gain

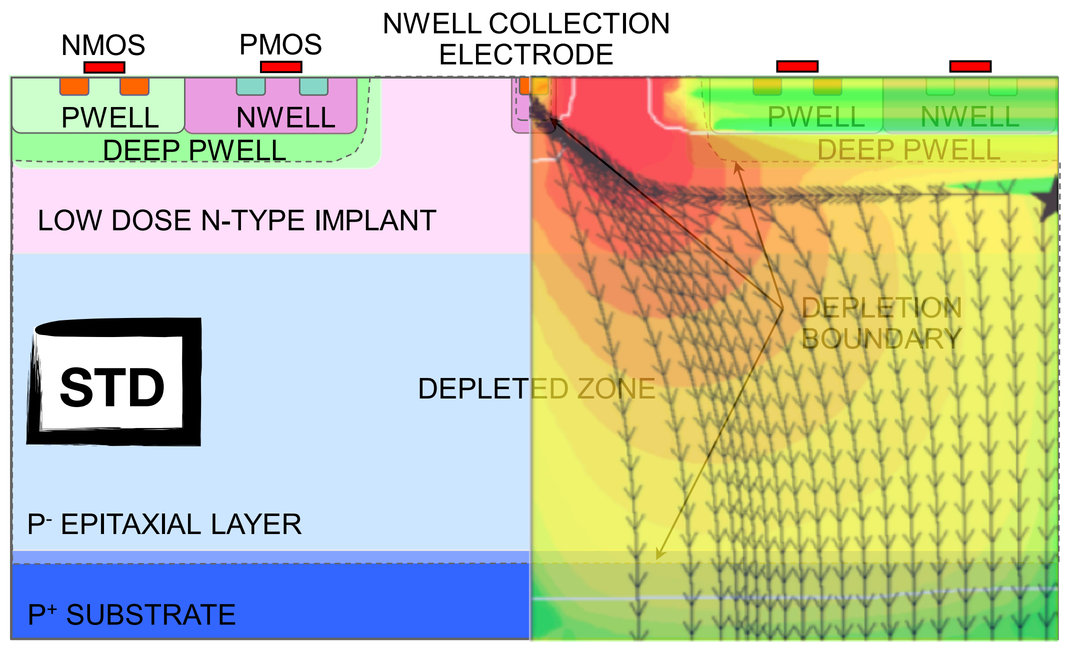


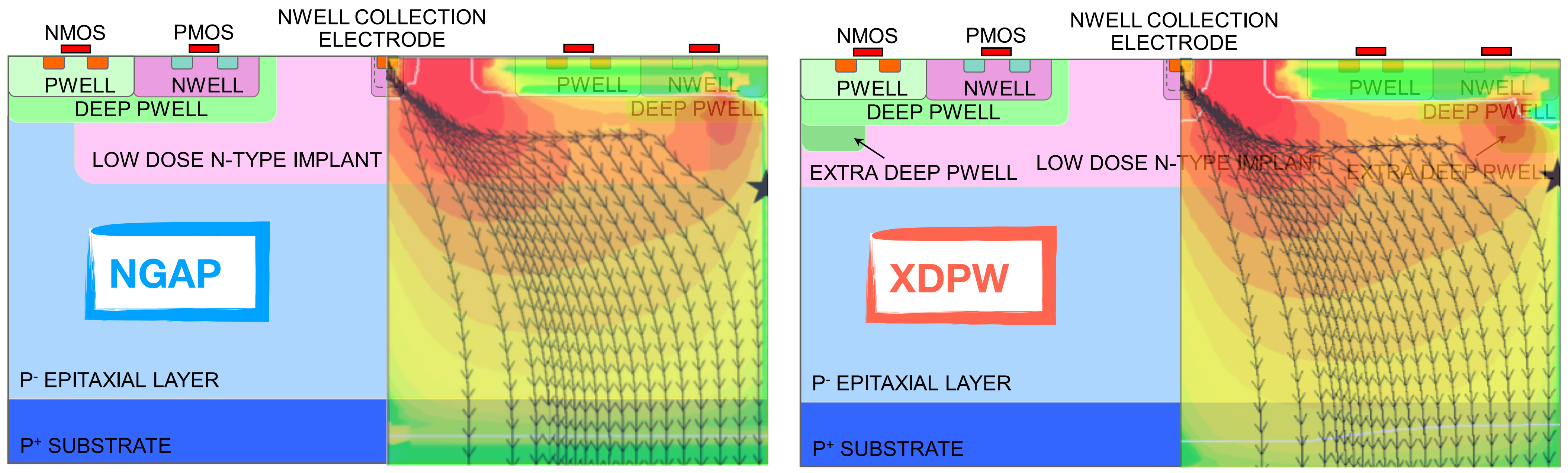


Process modifications

to increase lateral E-field in pixel corners

* *faster charge collection*
* *No visible differences btw NGAP and XDPW*





Gap in the low dose N-type implant

Extra Deep P-Well

High resistivity (3-4 kΩcm) Czochralski substrate

* larger depleted region with increasing substrate voltage
* larger cluster size
* larger radiation resistance

Backside metallisation

guarantees a good propagation of the bias voltage across the whole chip

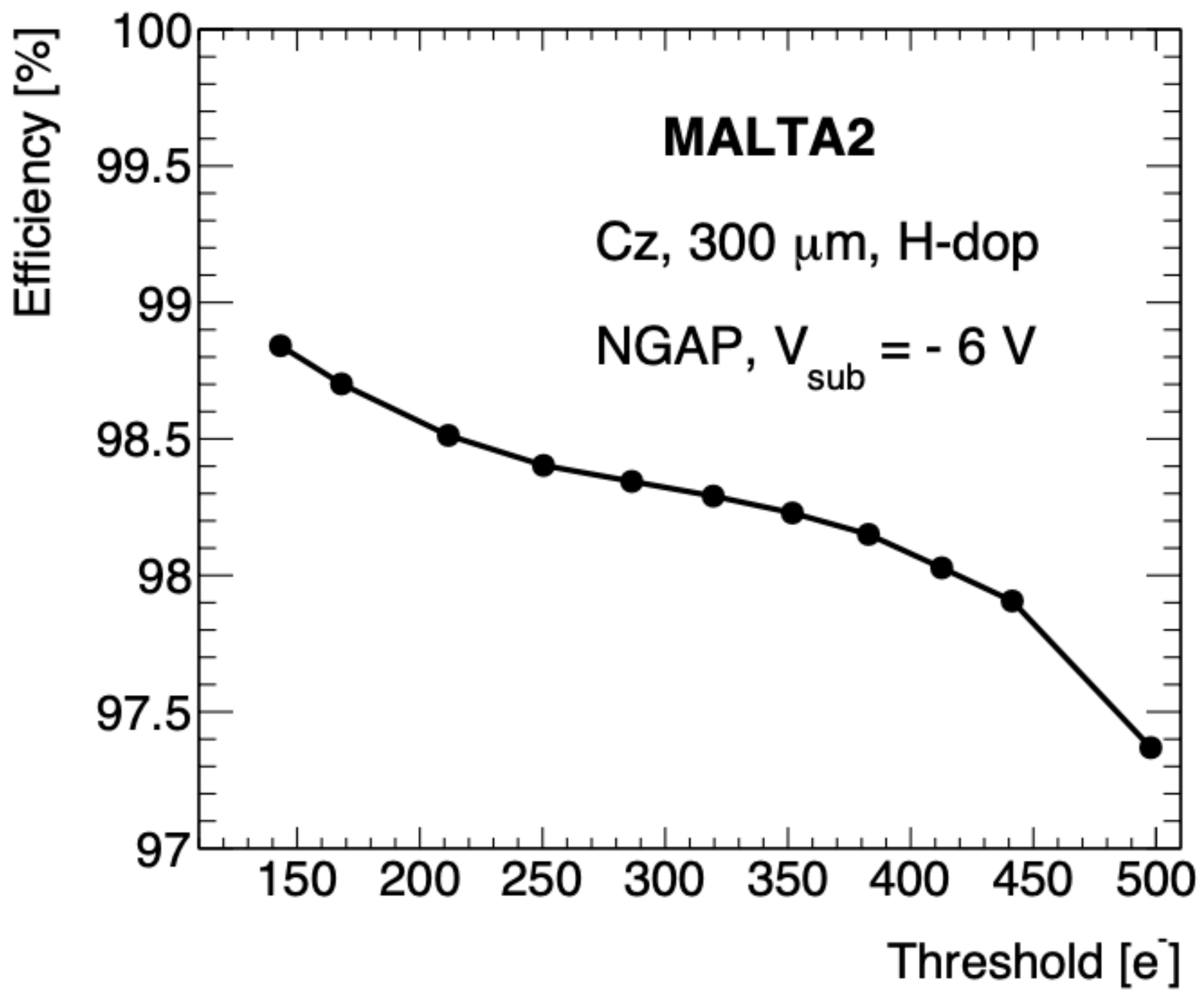
* better performing than conductive glue

Efficiency

arXiv:2308.13231

BEFORE irradiation

Full efficiency (~99%) at 150 e^- thresholds at substrate voltage V_{SUB} = -6 V



Efficiency

arXiv:2308.13231

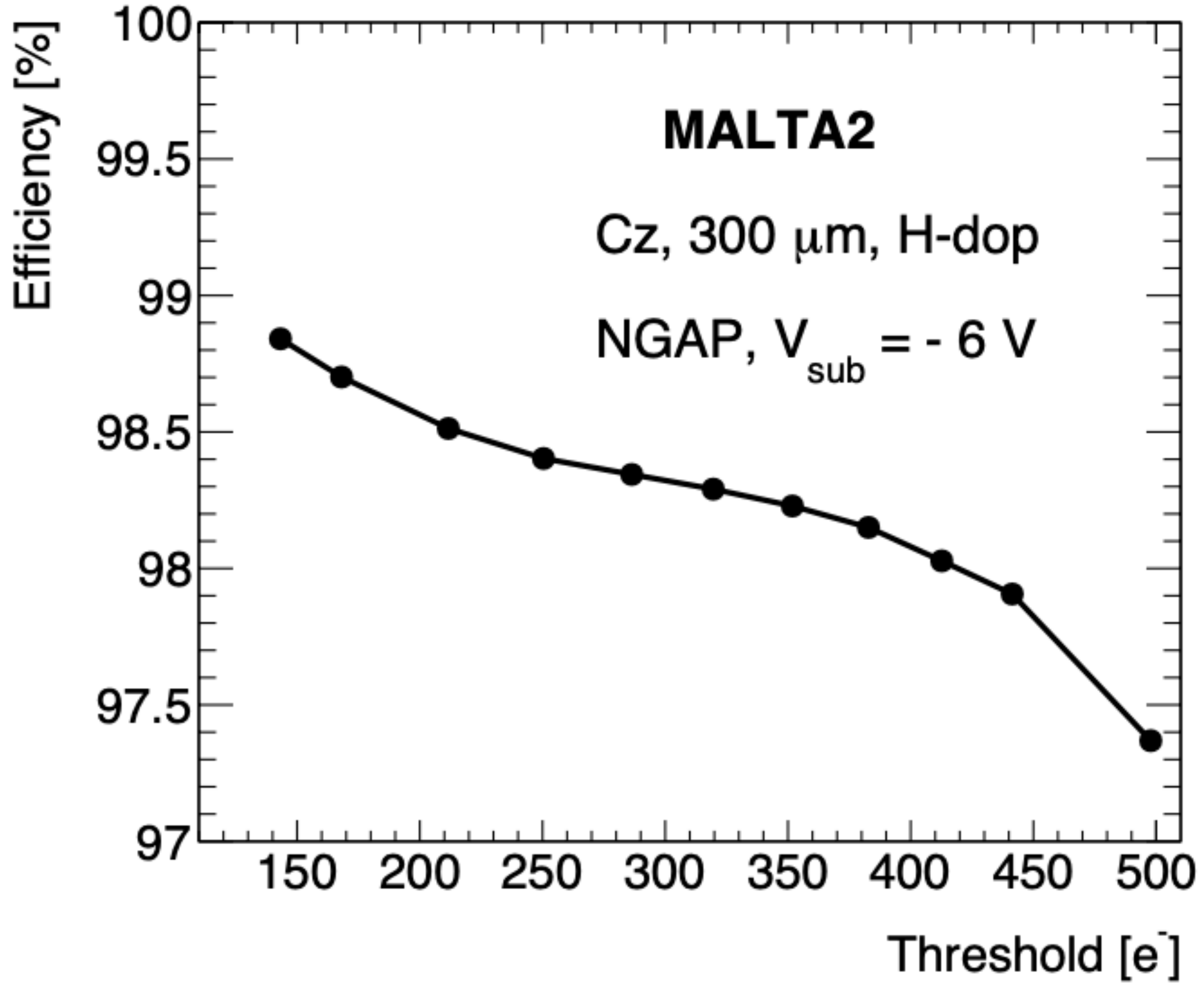
BEFORE irradiation

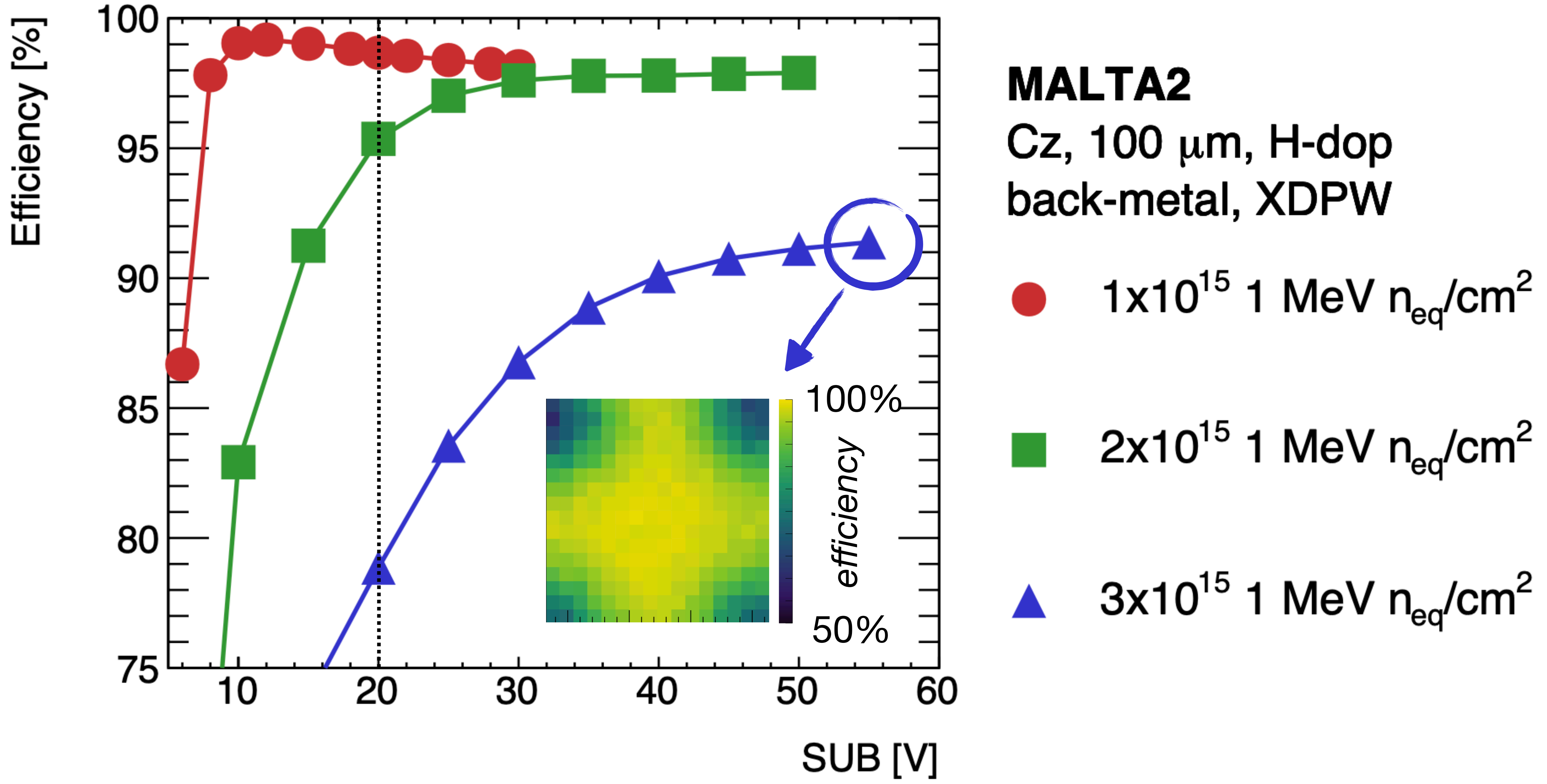
Full efficiency (~99%) at 150 e^- thresholds at substrate voltage V_{SUB} = -6 V

AFTER irradiation

> 95% efficiencies up to **2x10^{15}** n_{eq}/cm^2

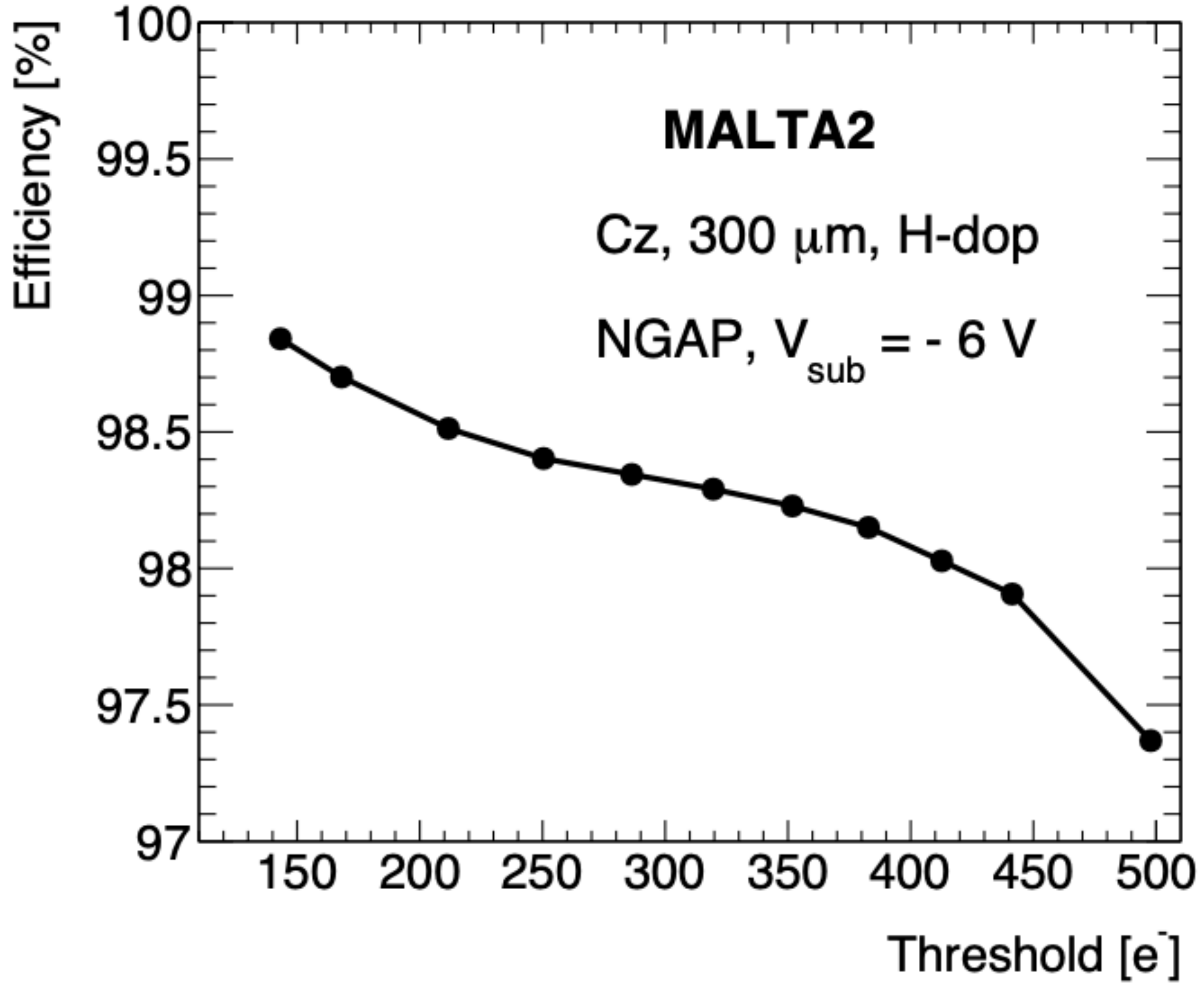
* at substrate voltage ~20 V





Efficiency

arXiv:2308.13231



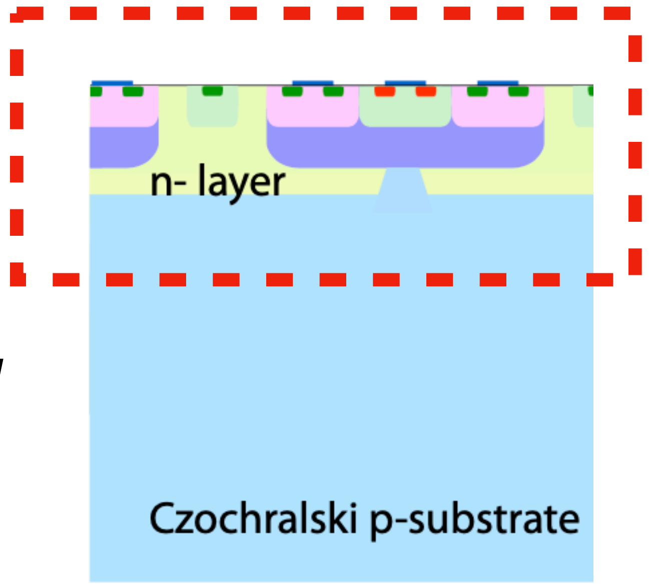
BEFORE irradiation

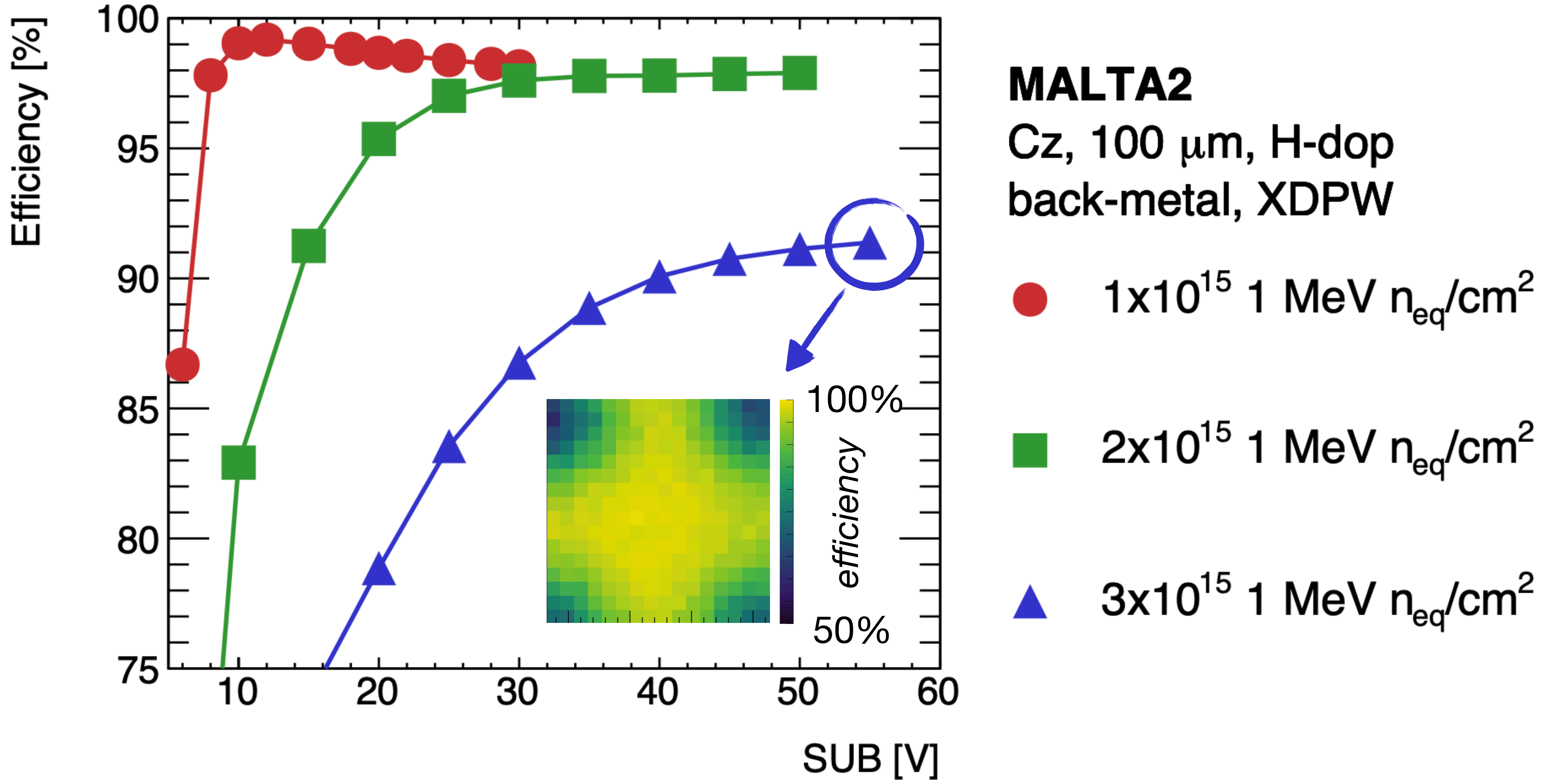
Full efficiency (~99%) at 150 e^- thresholds
at substrate voltage V_{SUB} = -6 V

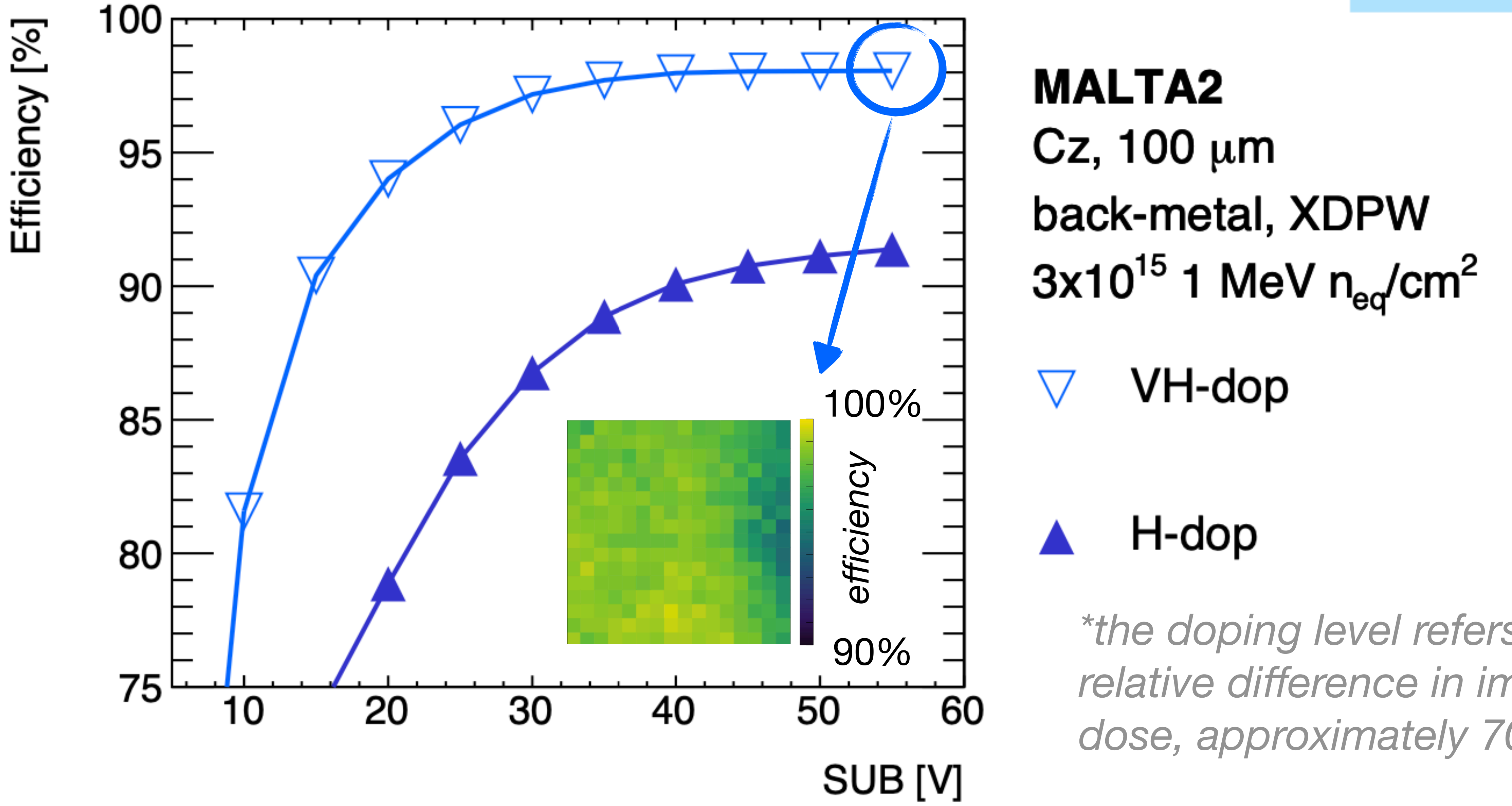
AFTER irradiation

> 95% efficiencies up to ~~2x10¹⁵~~ 3x10¹⁵ n_{eq}/cm^2

- at substrate voltage ~20 V
- with higher doping on continuous n-layer* → *help recovering efficiency on the pixel corners!*



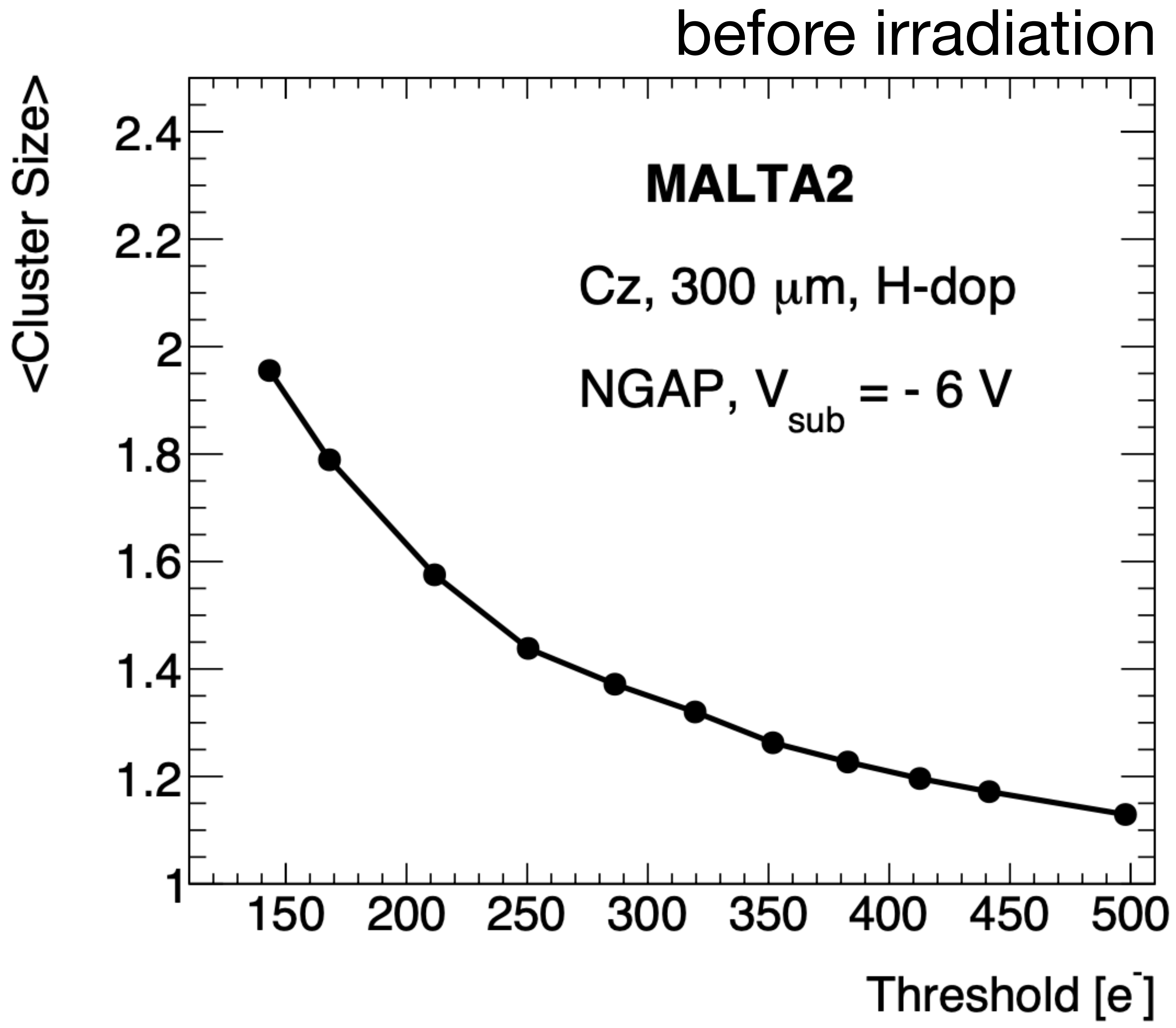


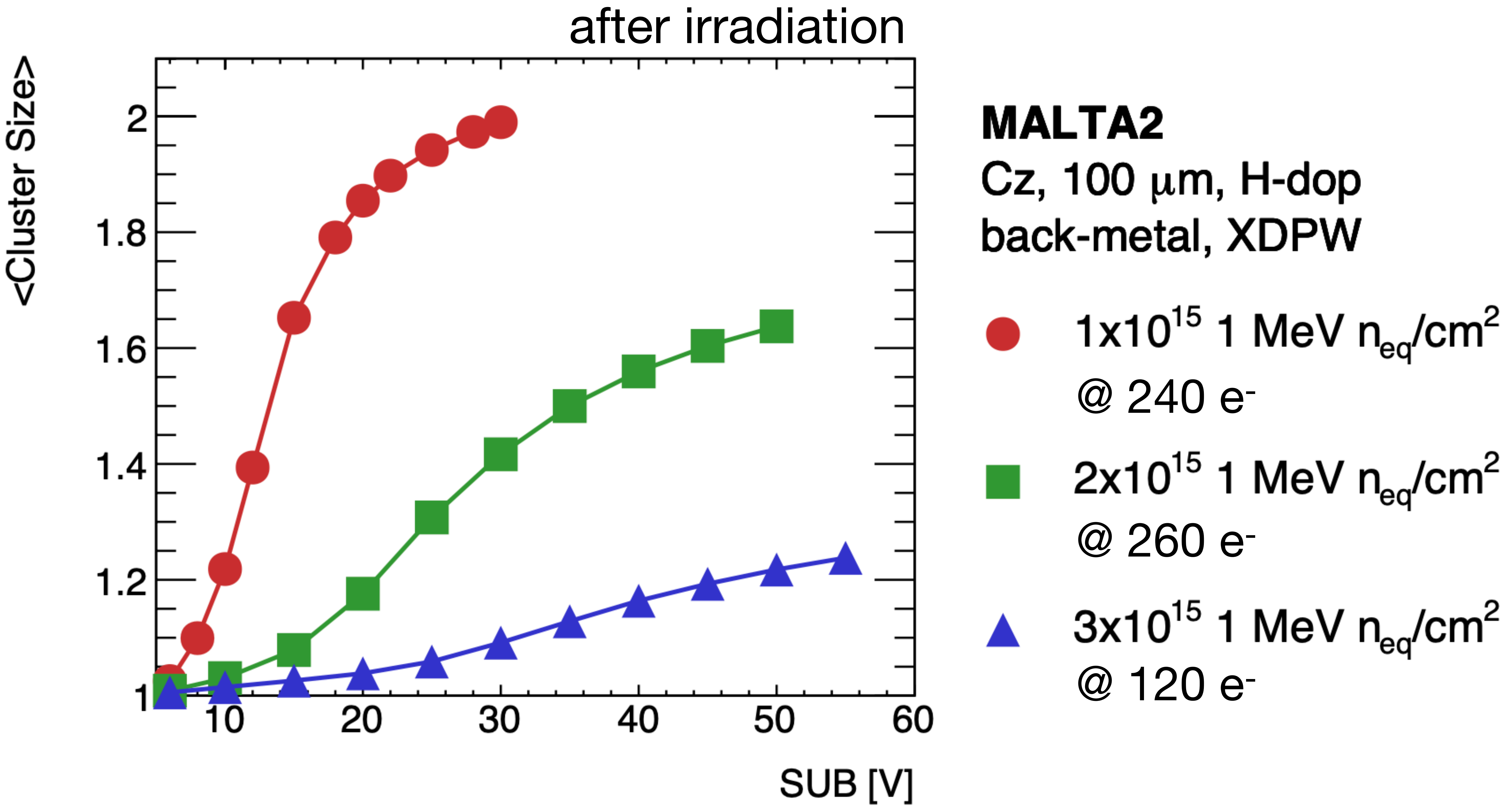


the doping level refers to the relative difference in implantation dose, approximately 70%.

Cluster size

arXiv:2308.13231





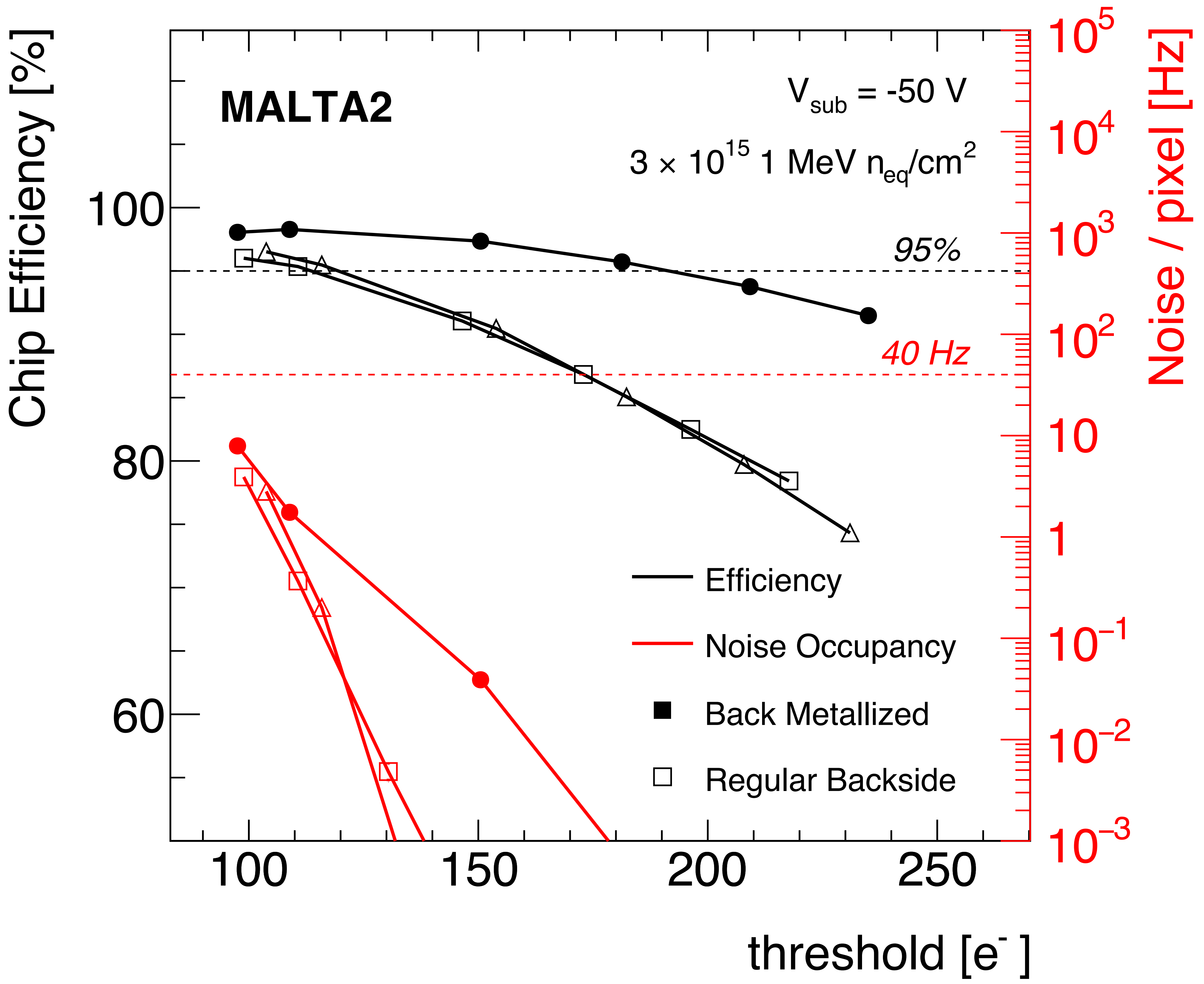
The cluster size increases for **lower thresholds** and **higher substrate voltages**

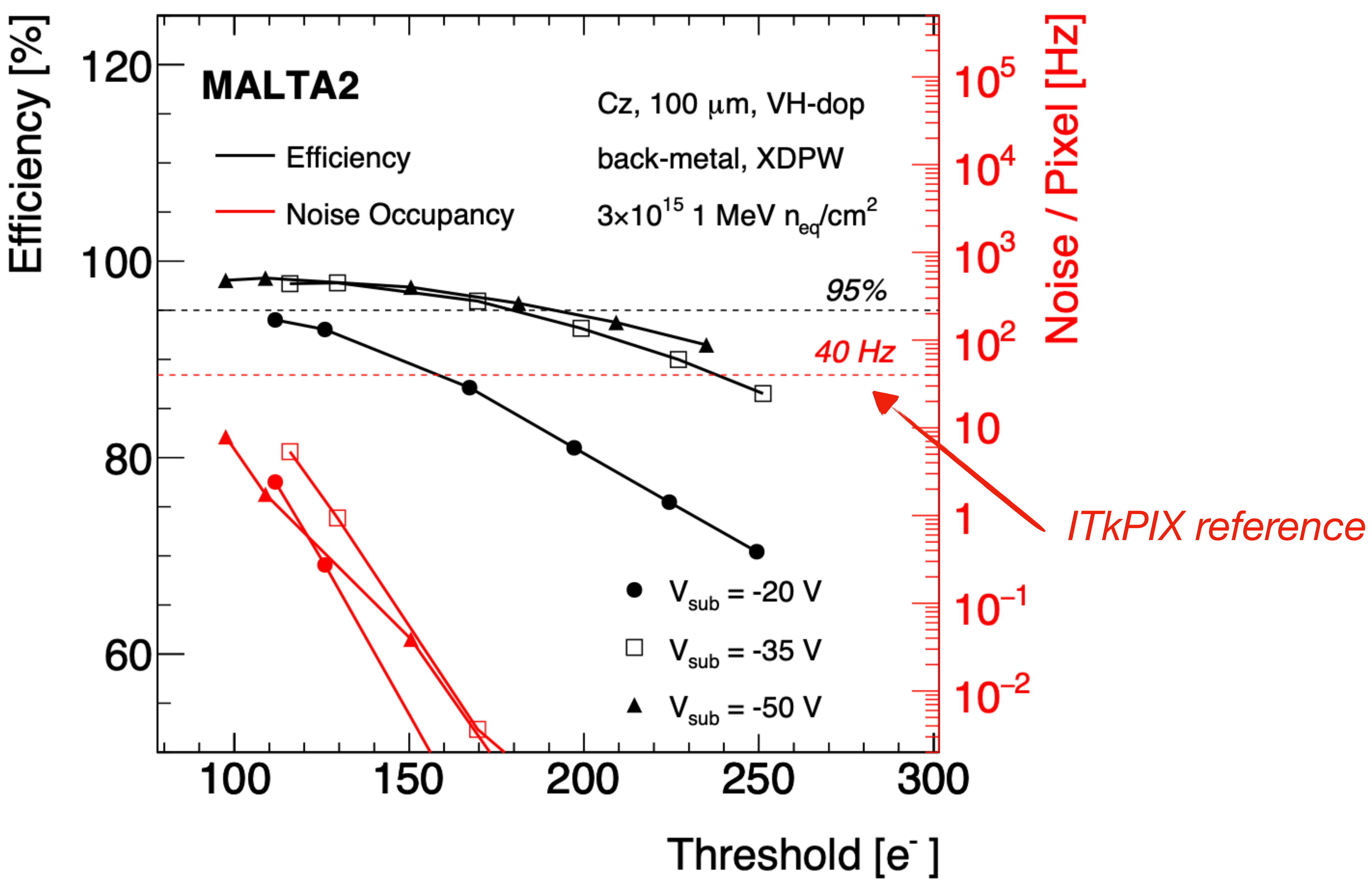
- enhanced charge-sharing effect btw pixels for larger active depths

Operational Window

arXiv:2308.13231
Malta2 public plots

Full efficiency after 3e15 n_{eq}/cm^2 with backside metallisation at ~-30 V substrate bias on VH-doped sensors
with a small noise occupancy





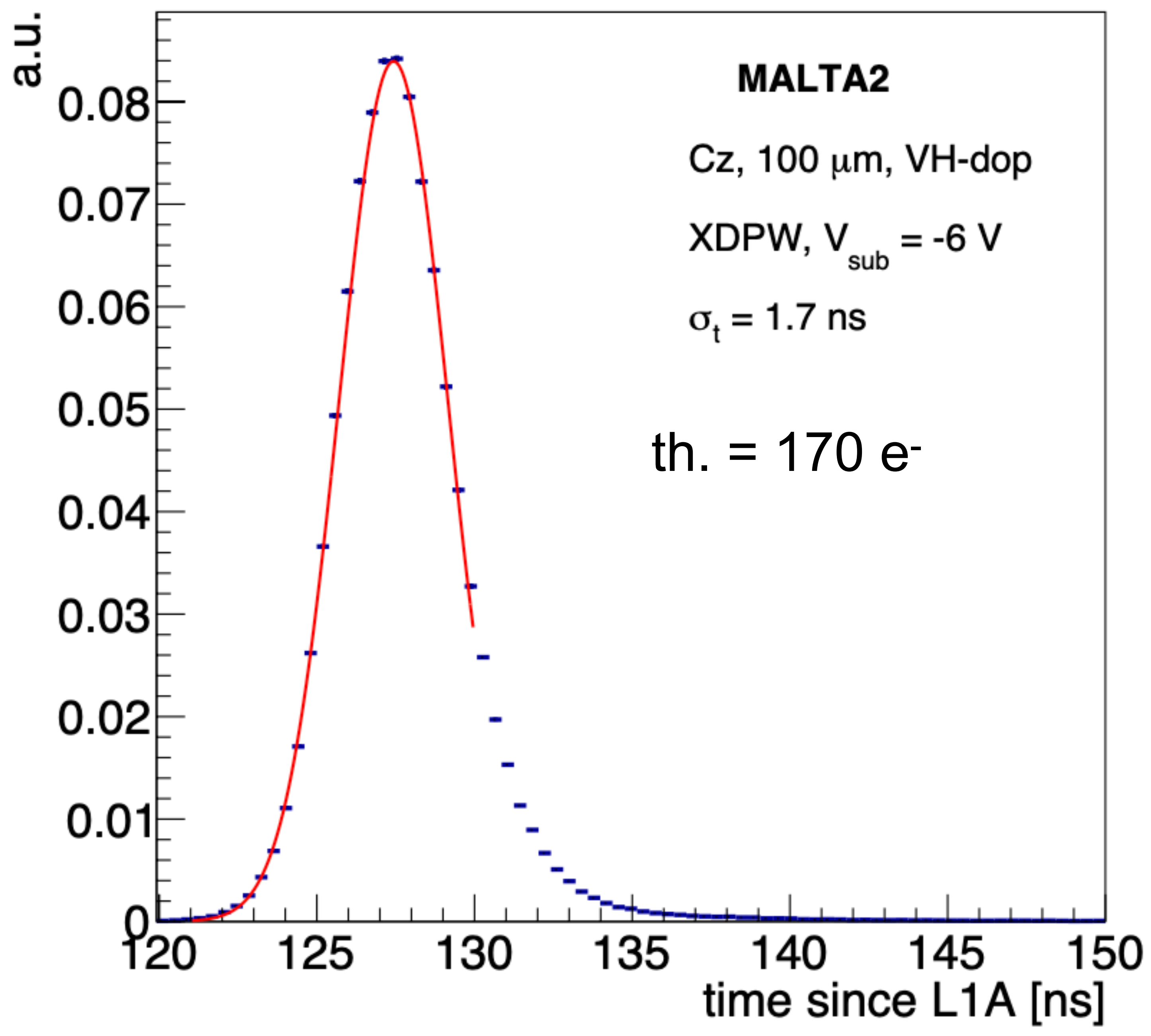
Backside metallisation allows propagating the bias voltage over the entire chip* and improves the performance

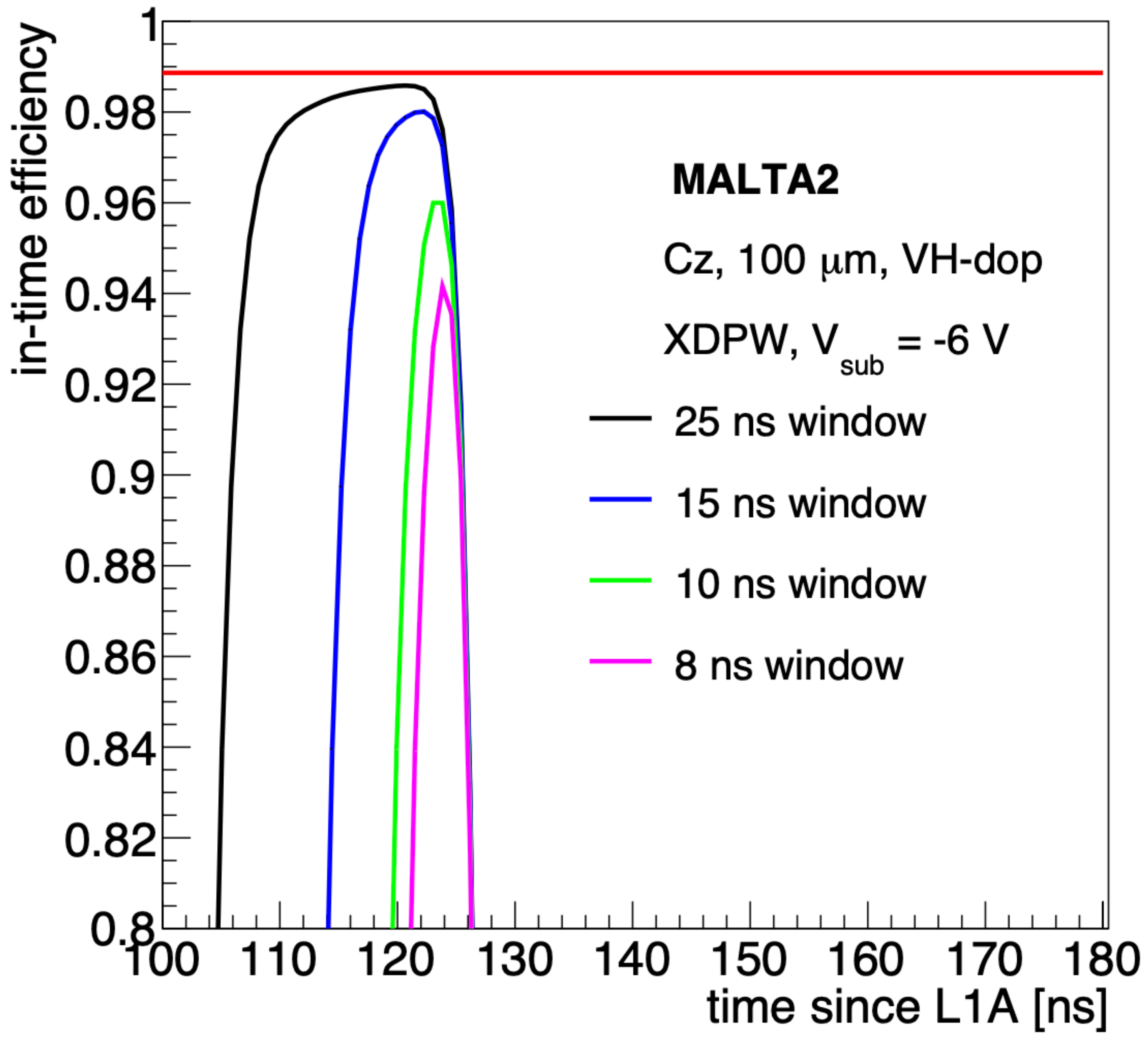
*A fiducial region (5% of the matrix) for regular backside sample is shown

Timing - before irradiation

arXiv:2308.13231

Time of arrival of leading hit in the cluster wrt the scintillator reference





After signal propagation correction

☑ time resolution is σ_t ~ 1.7 ns

Convolution of:

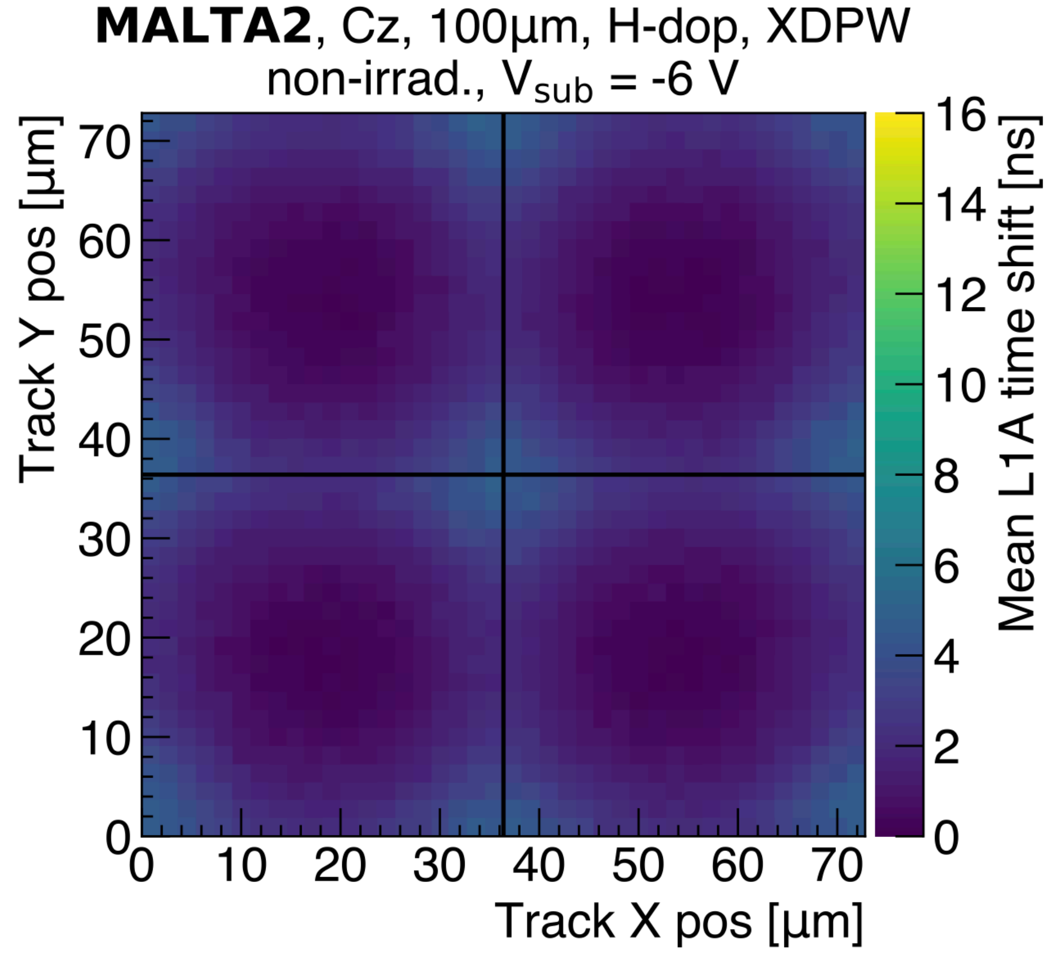
- Electronics jitter
- Time-walk
- Charge collection effects
- Scintillator jitter (~0.5 ns)
- FPGA readout jitter (~0.9 ns)

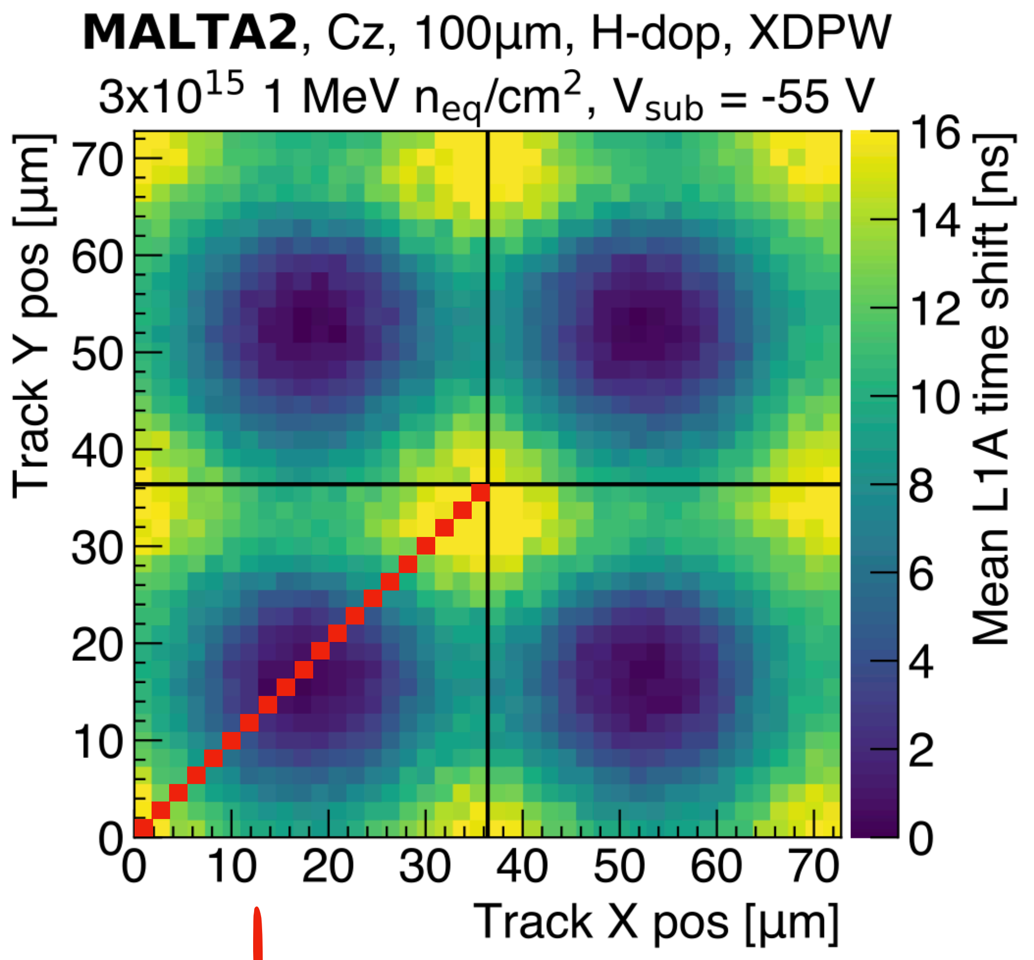
* ***98% of hits collected within 25 ns***
* ***90% of hits collected within 8 ns***

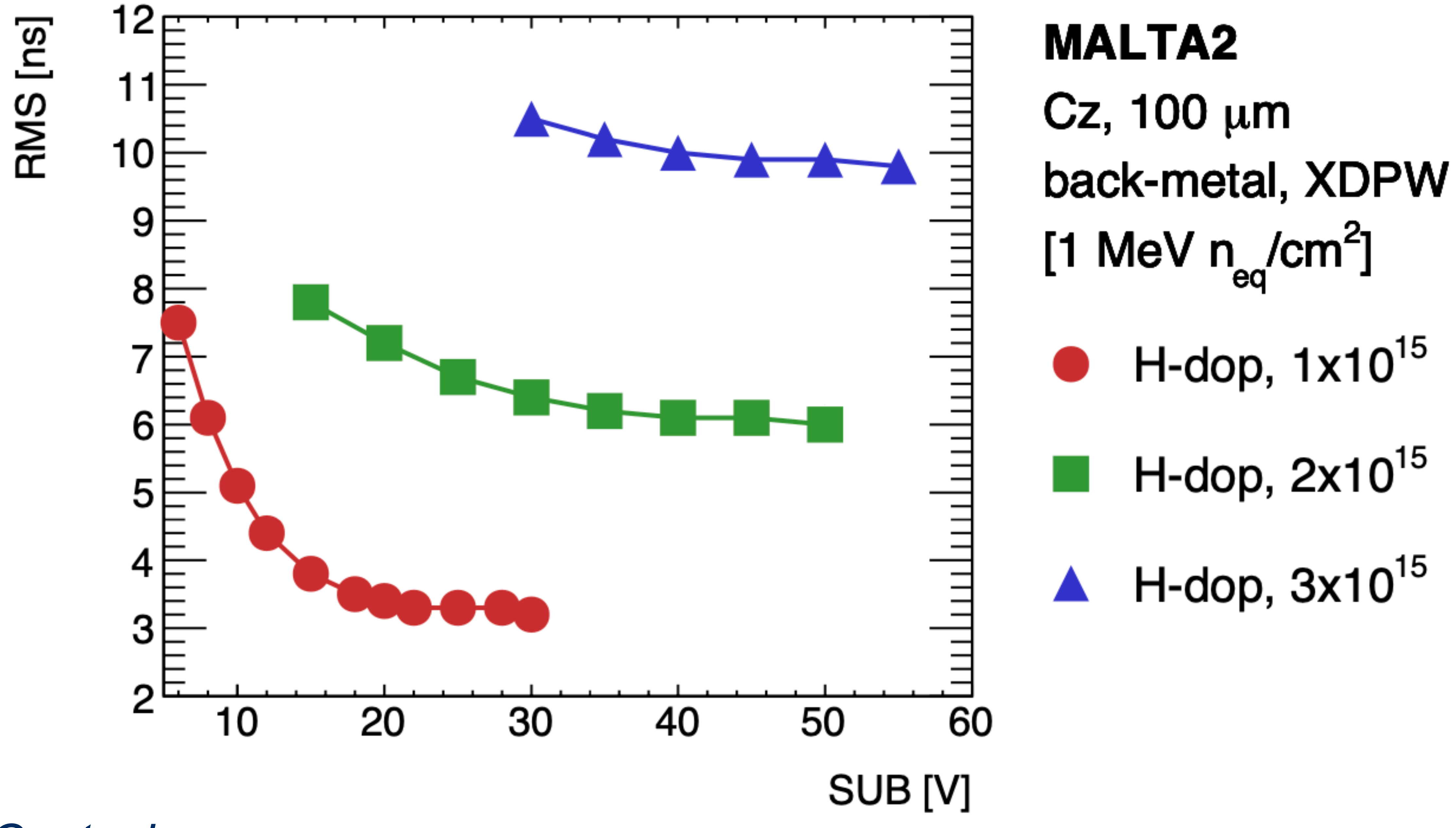
Timing - after irradiation

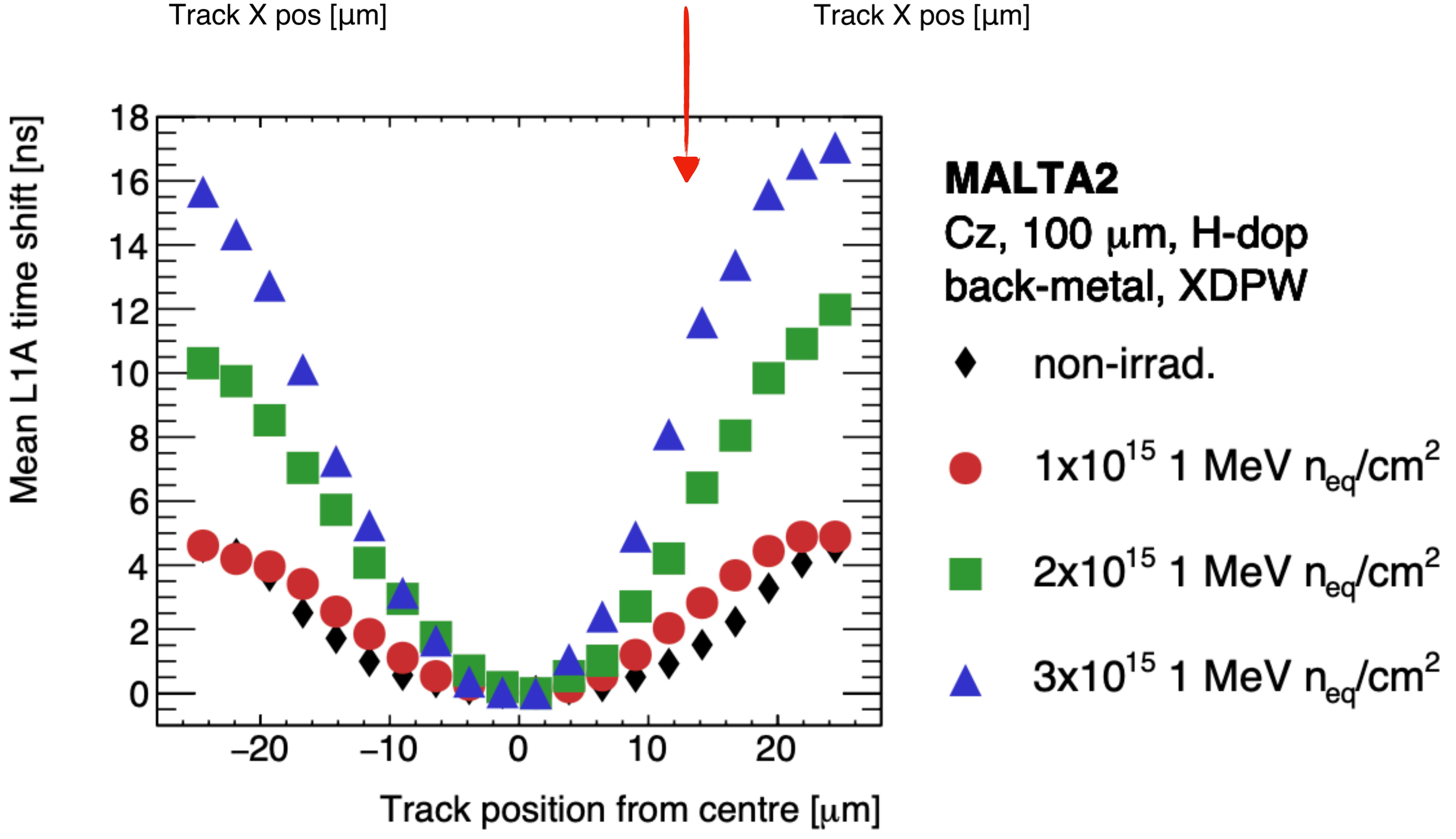
arXiv:2308.13231

- Charge trapping and changing mobility of charge carriers
- Uniformity deteriorates as the radiation dose increases
- *Increasing the substrate voltage helps!*







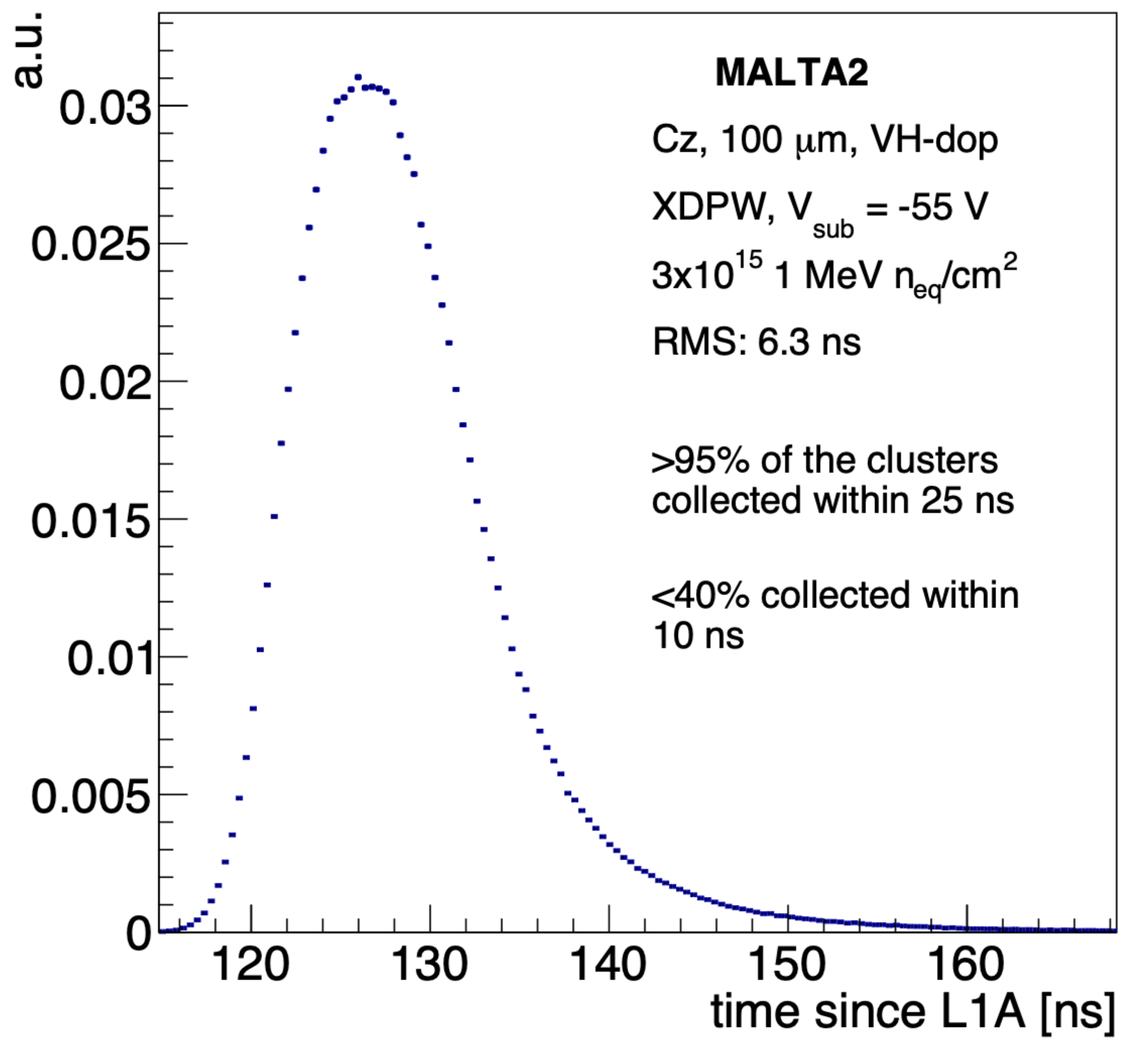


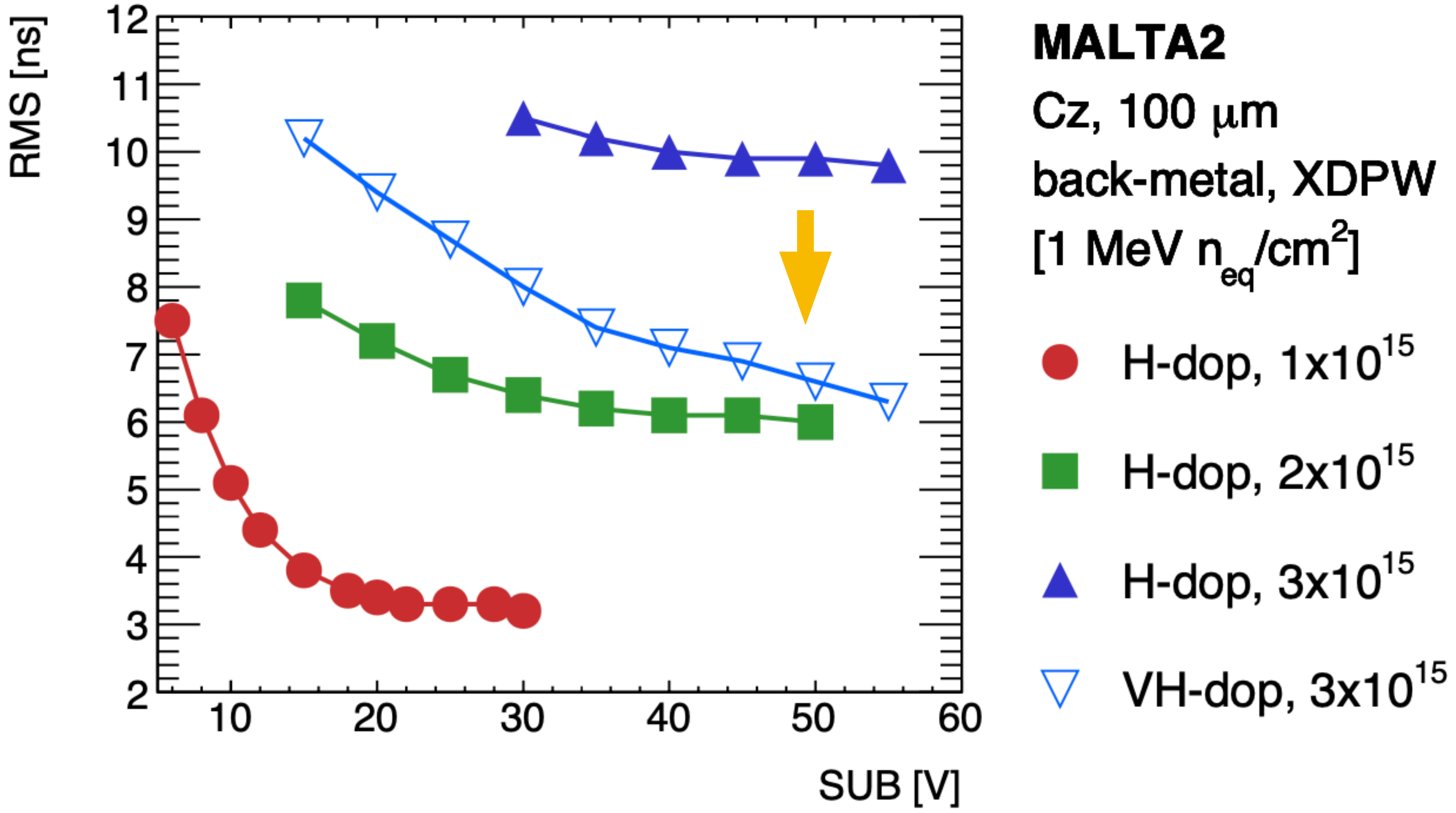
Timing - after irradiation *w/ VH doping*

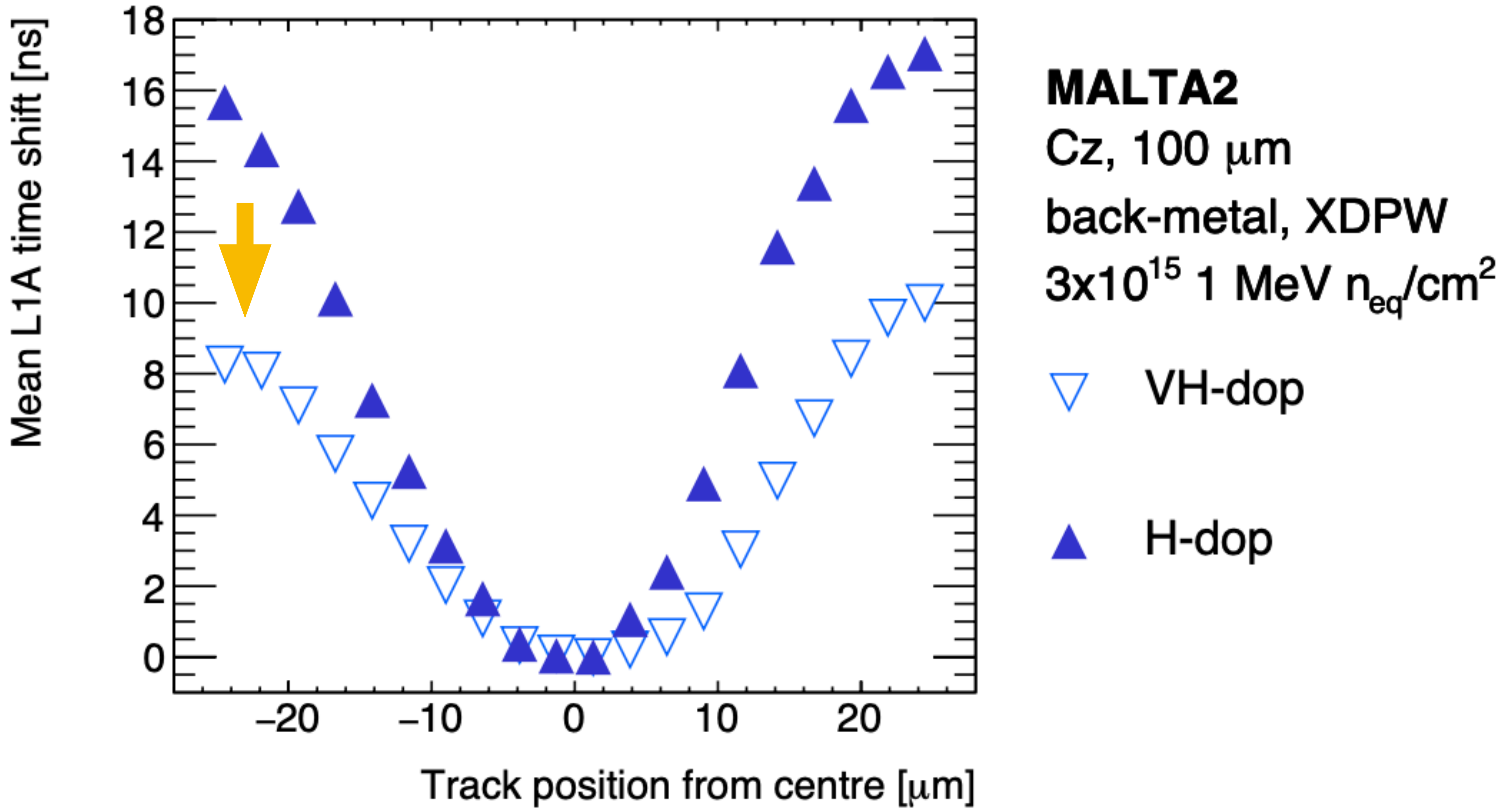
arXiv:2308.13231

- **Higher doping** further improves the performance
  - ***95% of hits collected within 25 ns***
  - ***40% of hits collected within 8 ns***

@ 3 x 10^{15} n_{eq}/cm^2







Conclusions

First **successful application** of MALTA chips as telescope planes with $\sigma_s = 4.1 \mu m$ & $\sigma_t = 2.1\ ns$*

The large R&D campaign of MALTA2 brought a combination of modifications including

- pixel design
- high-resistivity Cz substrates
- backside metallisation
- high doping of the n-layer

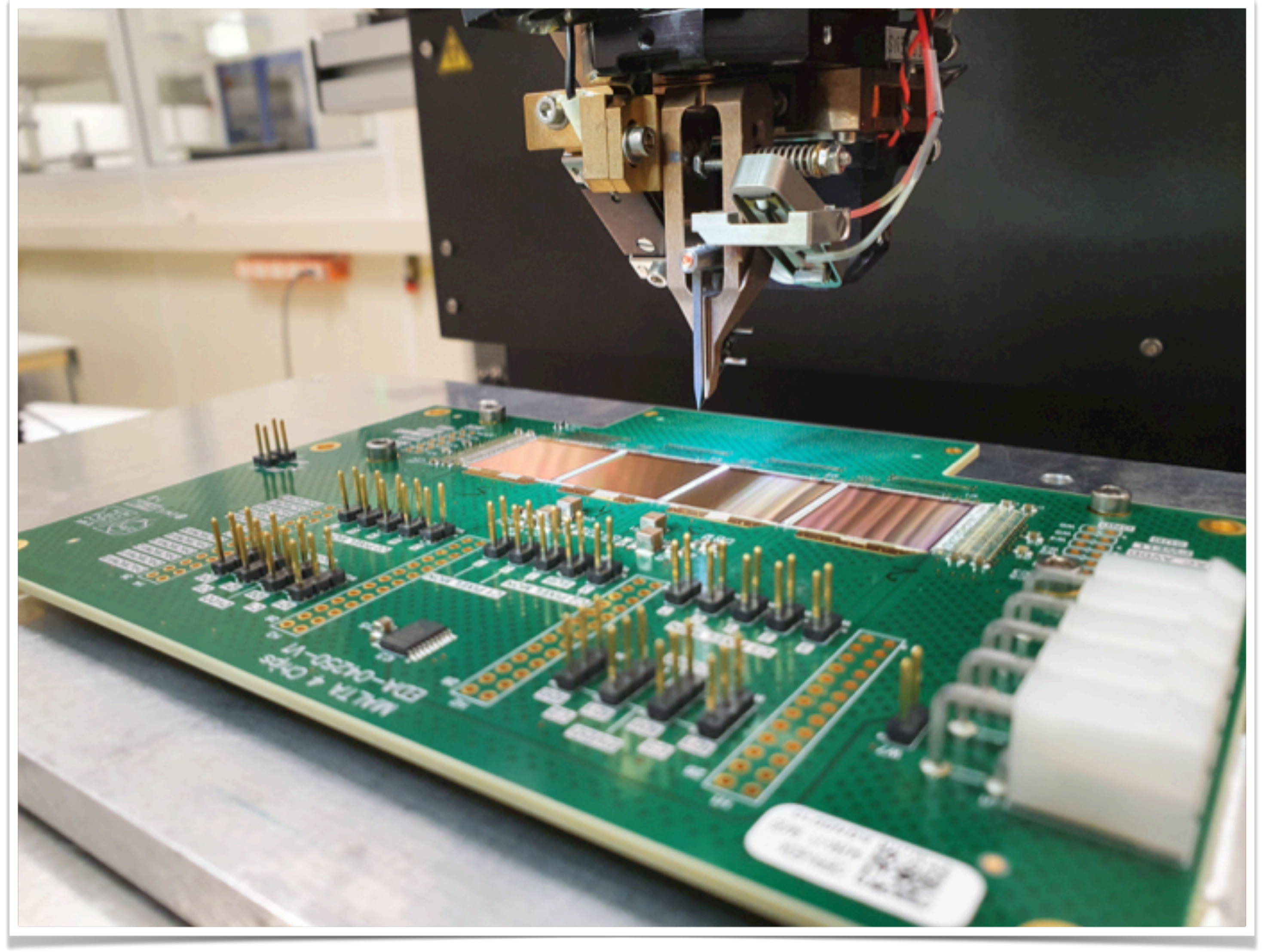
Excellent performance up to **$3 \times 10^{15}\ n_{eq}/cm^2$**

- *99% efficiency*
- *< 40 Hz/pixel noise occupancy*
- *> 95% of the clusters collected within the LHC bunch crossing window*

Ongoing measurements to estimate the depletion depth.

Four-chip board and flex

- 4-chip MALTA board functionality recently demonstrated
- tested successfully in 2023 at SPS



MALTA3 chip demonstrator under production:

- improved in-pixel digital electronics:
  - faster signal generation
- <1 ns time-stamping in periphery, >1 Gb/s serial output communication

**see also the PS telescope application in Brian's poster for the material measurement of an ATLAS Pixel Module*

BACKUP

Bibliography

Radiation Hardness of MALTA2 Monolithic CMOS Sensors on Czochralski Substrates

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Milou van Rijnbach, Giuliano Gustavino et al.

e-Print: 2304.01104 [hep-ex]

DOI: 10.1140/epjc/s10052-023-11760-z

Published in: Eur.Phys.J.C 83 (2023) 7, 581

MALTA-Cz: a radiation hard full-size monolithic CMOS sensor with small electrodes on high-resistivity Czochralski substrate

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DOI: 10.1088/1748-0221/18/09/P09018 (publication)

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Published in: JINST 15 (2020) 02, P02005

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Magdalena Munker(CERN) et al.

e-Print: 1903.10190 [physics.ins-det]

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Published in: JINST 14 (2019) 05, C05013

A 1μW Radiation-Hard Front-End in a 0.18-μm CMOS Process for the MALTA2 Monolithic Sensor

F. Piro et al.

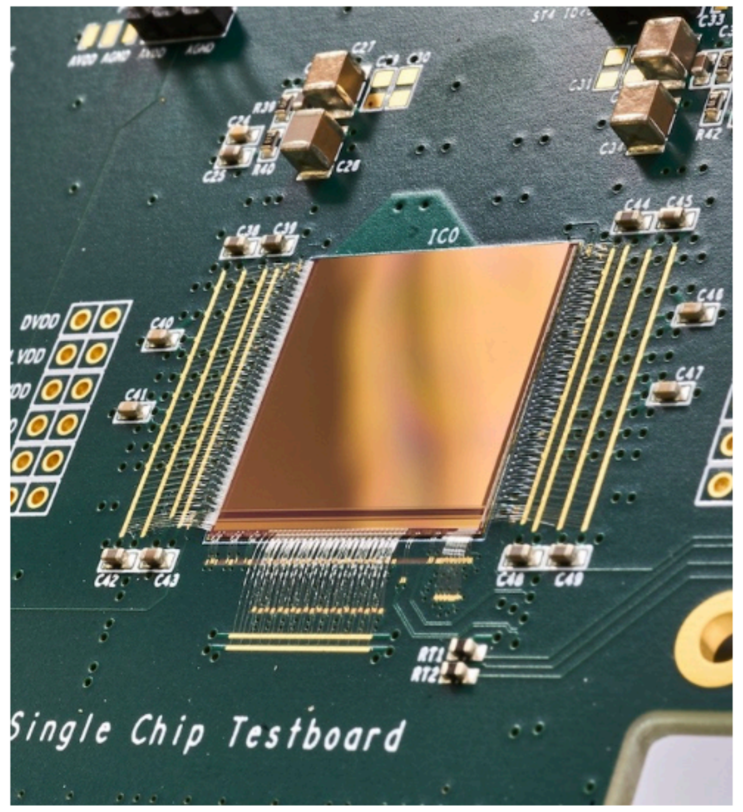
DOI: 10.1109/TNS.2022.3170729 , 10.36227/techrxiv.19222311.v1

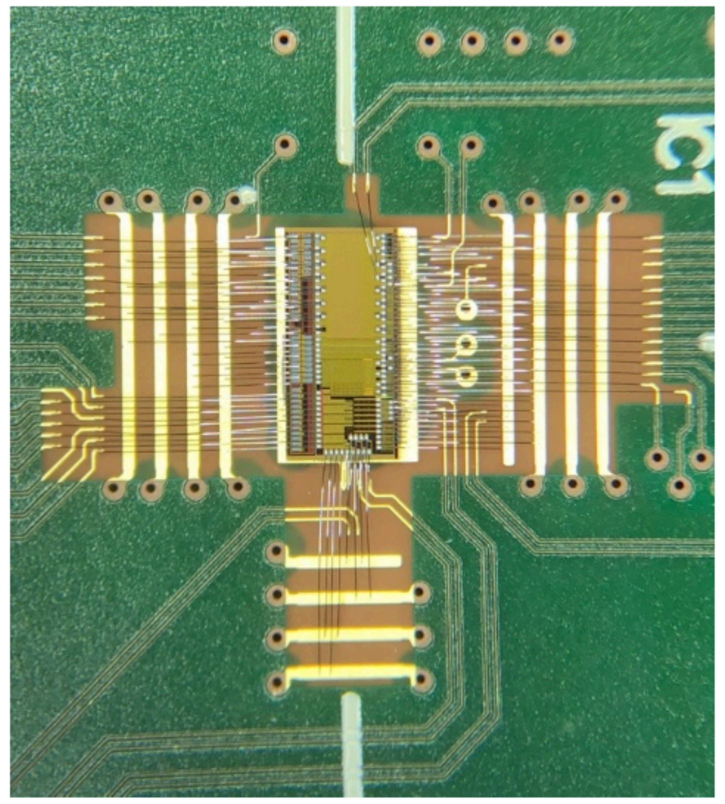
Published in: IEEE Trans.Nucl.Sci. 69 (2022) 6, 1299-1309

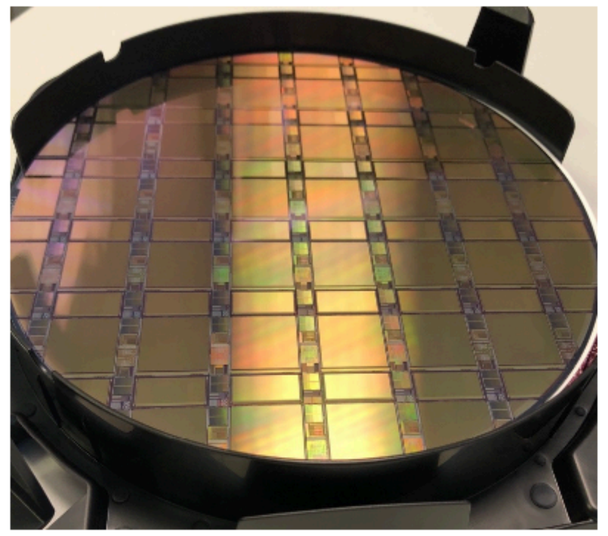
MALTA history

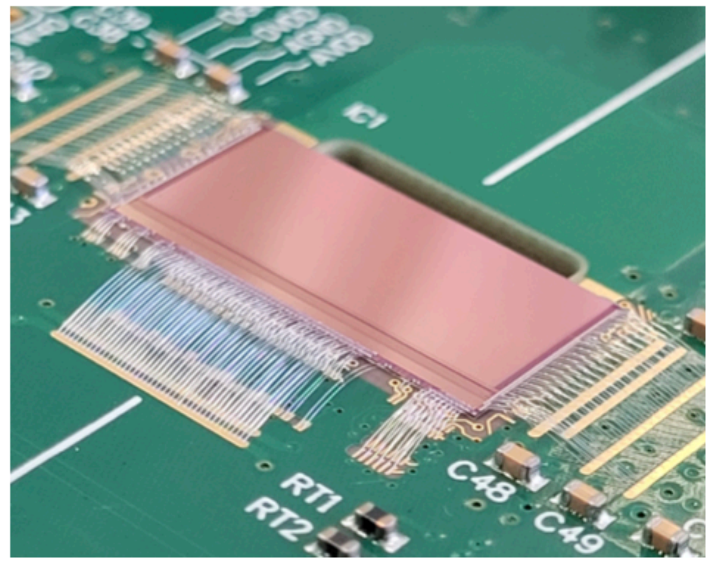
STREAM

AIDA Innova WP5 and CERN EP R&D WP 1.2







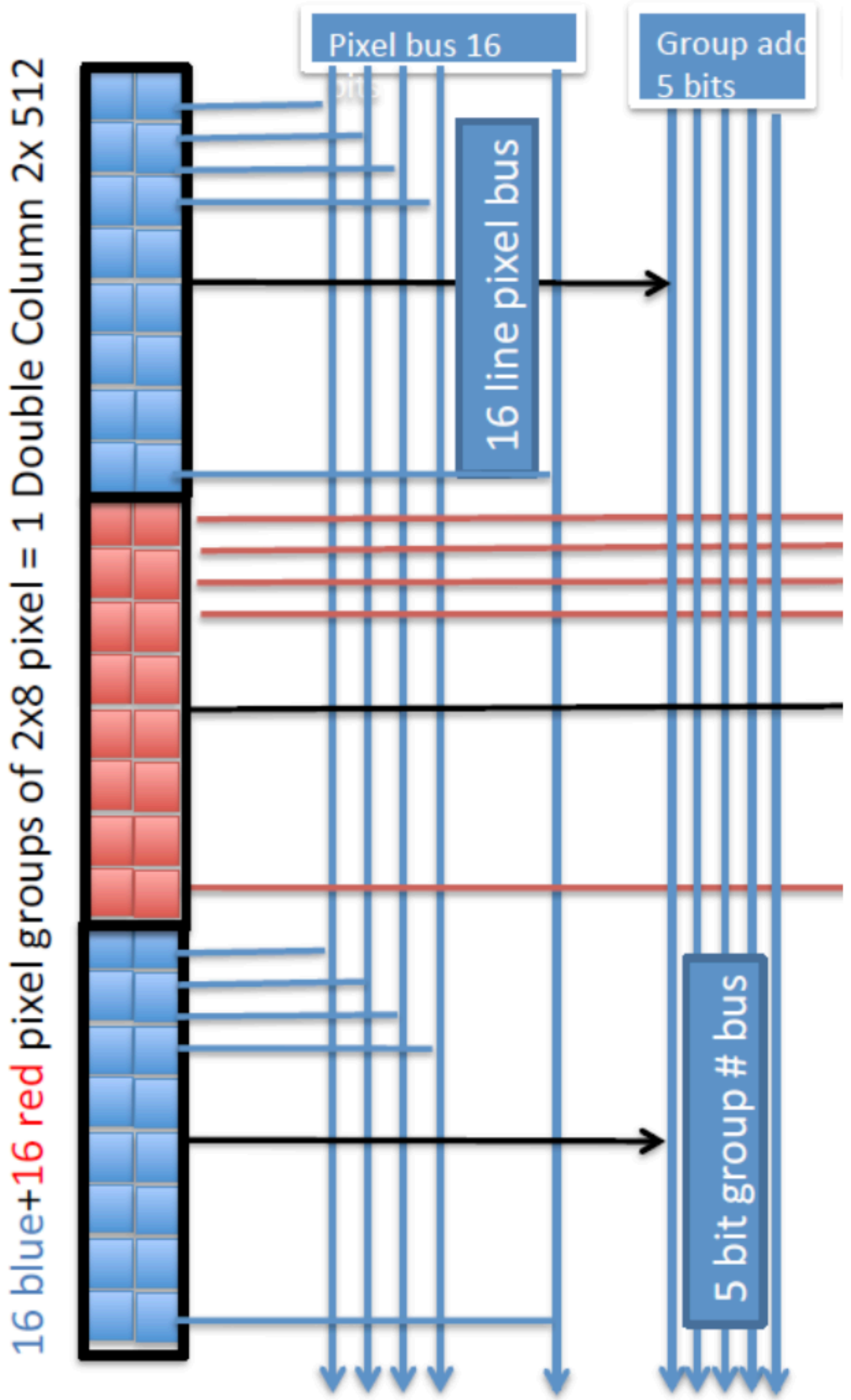


MALTA3
#digital-flow-design

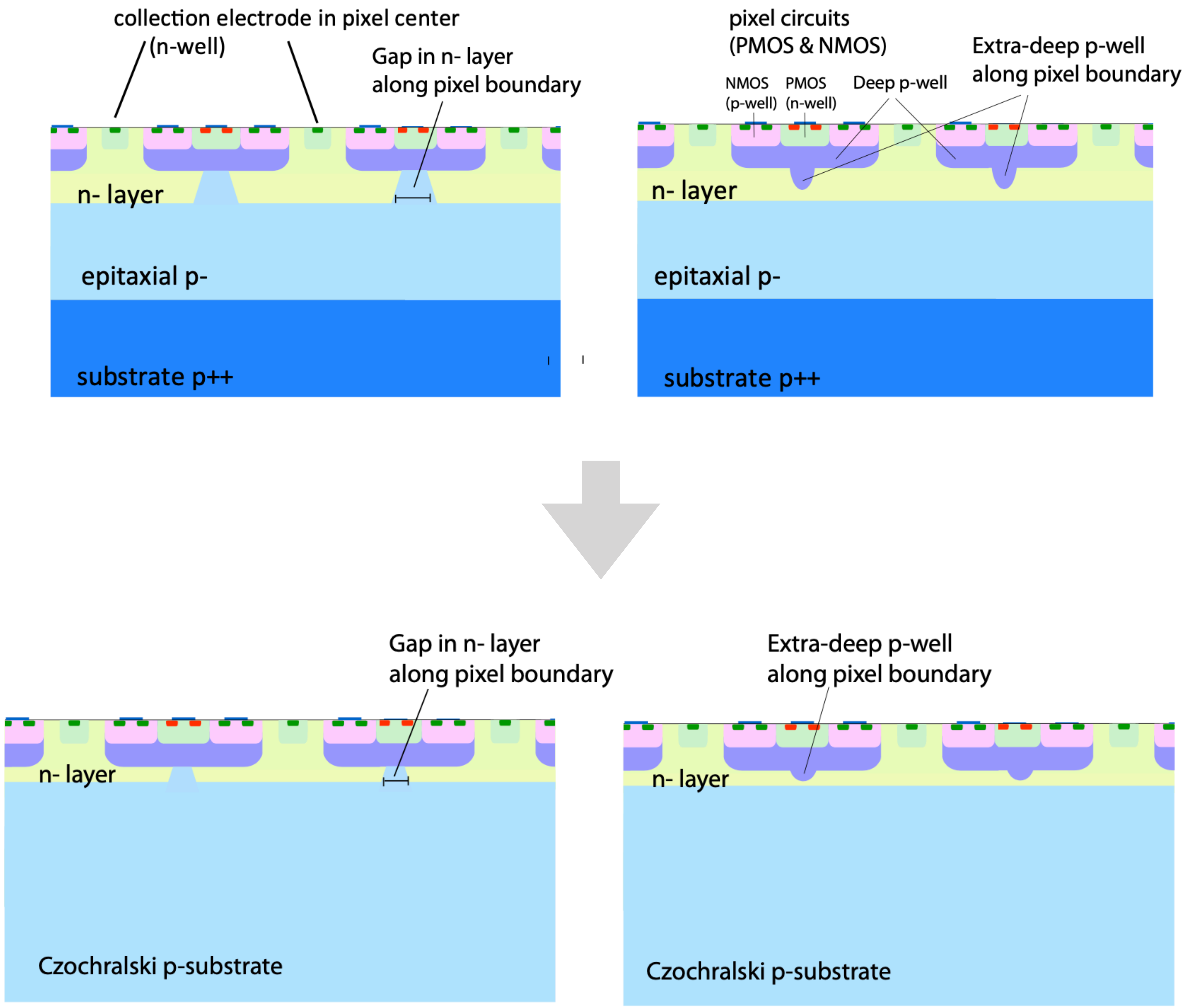
MALTA1 & MLVL	Mini-MALTA	MALTA C	MALTA 2	MALTA 3
Jan 2018	**Jan 2019**	**Aug 2019**	**Jan 2021**	**2023**
Large demonstrator Asynchronous readout Electrode size and reset mechanism evaluation	Small demonstrator Process and mask modification	Slow control improvements on EPI and Czochralski substrates	New front-end Additional process modification	Large matrix Time tagging
Poor lateral field after irradiation	Full efficiency after 1e15 n/cm^2	Enlarged cluster size and improved time resolution on Czochralski	Improved time resolution and on chip synchronization	

MALTA read-out architecture

- Novel asynchronous readout architecture for ***high hit rate capability***:
  - data transmitted *asynchronously* (no clock) over to end of column
  - latency: ***~ few ns***
  - output rate: ***>>100 MHz***
  - ***hit coordinates transmitted through 37 parallel output signals***



Czochralski geometry



MALTA Telescope - specifications

MALTA Telescope Planes

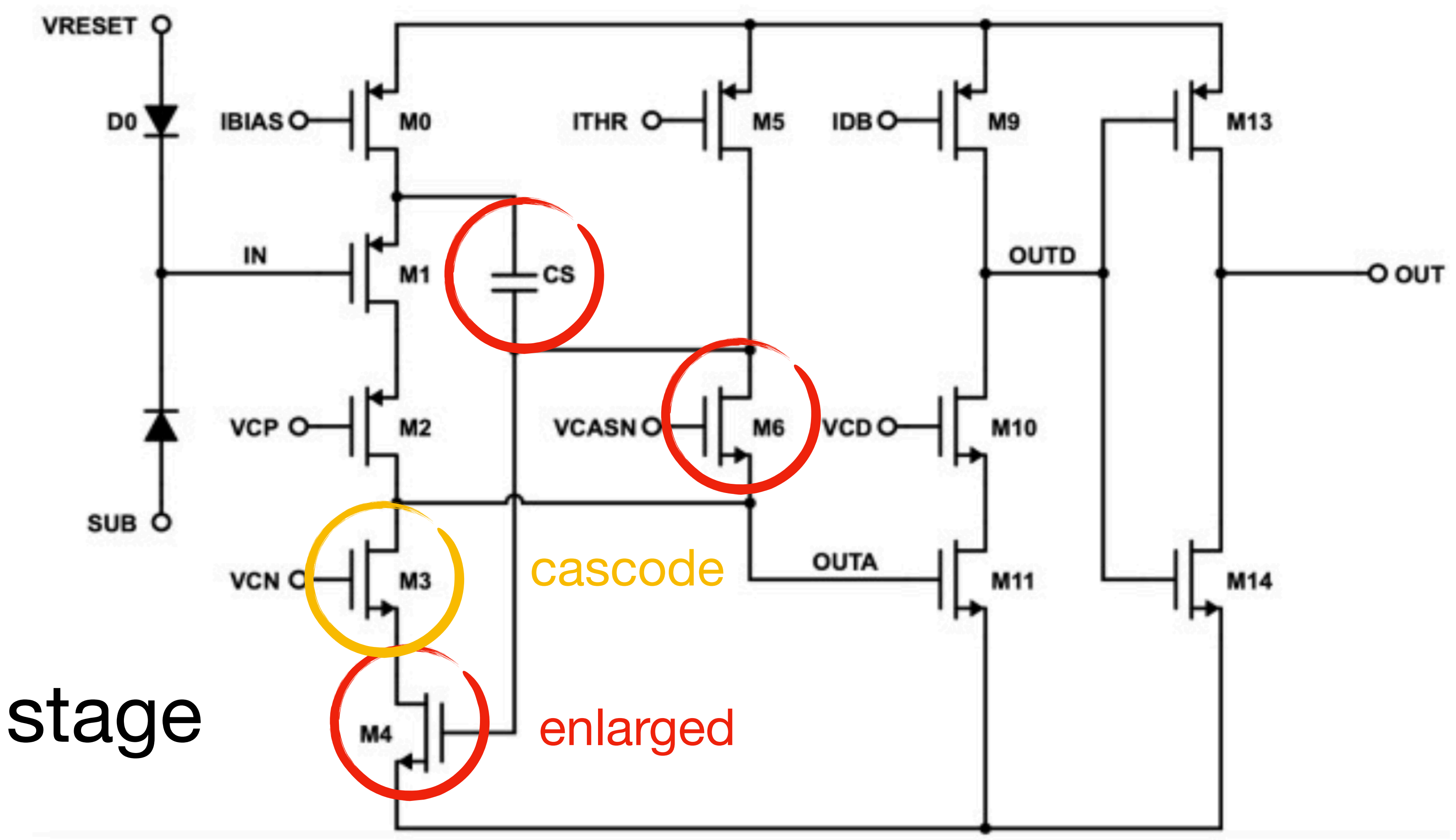
Plane	1	2	3	4	5	6
Specifications						
Substrate Type	Epi	Cz	Cz	Cz	Cz	Epi
Sensor Flavour	STD	NGAP	STD	STD	NGAP	STD
Total Thickness [μm]	100	100	300	300	100	300
Operation Voltage [V]	-6	-6	-30	-30	-6	-6
Distance [cm]	0	8	16	94	102	110

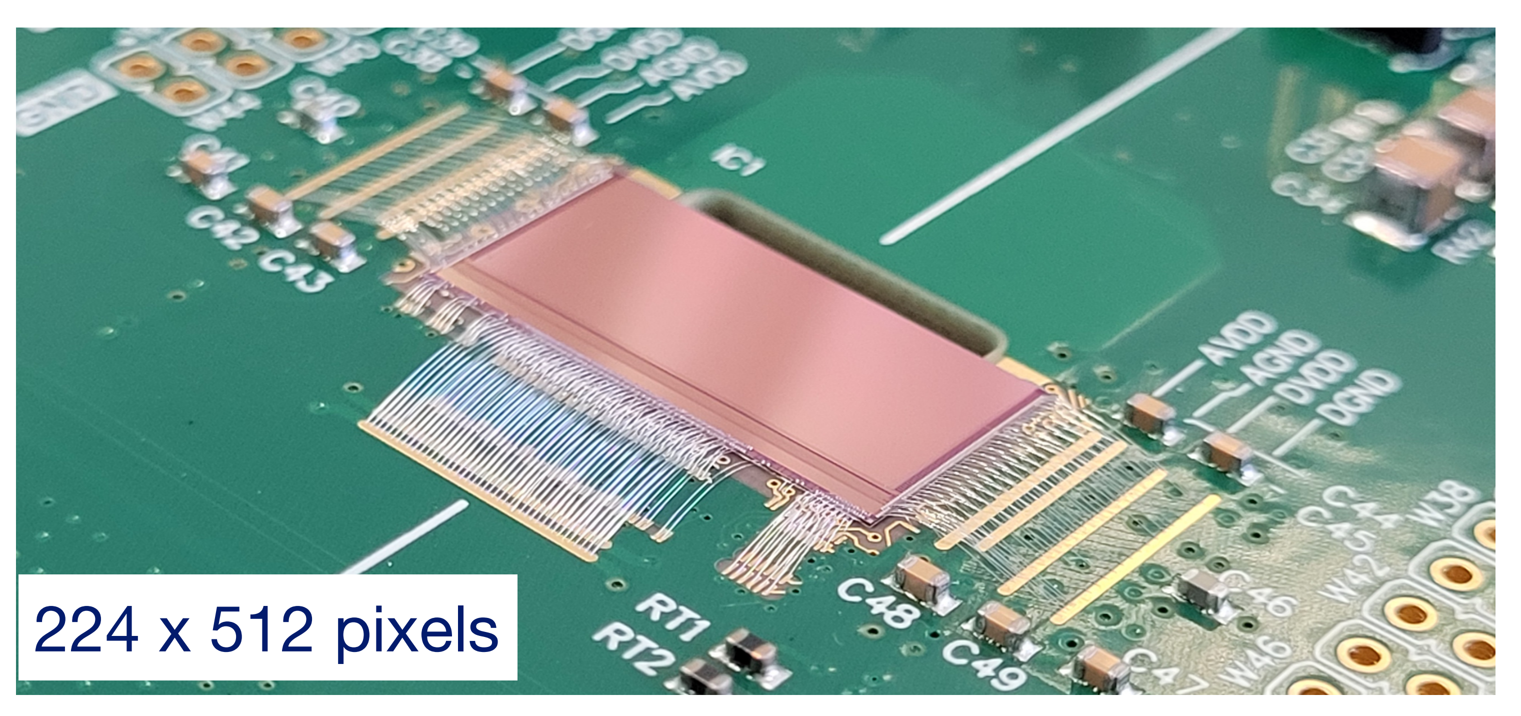
Characterisation of Telescope Planes

Plane	1	2	3	4	5	6
Average Efficiency [%]	97.4 $\pm$0.1	96.9 $\pm$0.1	99.2 $\pm$0.1	99.0 $\pm$0.1	95.0 $\pm$0.1	94.0 $\pm$0.1
Average number of hits per event	1.7 $\pm$0.9	1.8 $\pm$1.0	2.2 $\pm$1.1	2.5 $\pm$1.2	1.7 $\pm$0.9	1.6 $\pm$0.9
Average Cluster Size [pixels]	1.1 $\pm$0.3	1.1 $\pm$0.4	1.7 $\pm$0.8	1.9 $\pm$0.9	1.1 $\pm$0.3	1.1 $\pm$0.4

MALTA2

IEEE Trans. Nucl. Sci. , vol. 69, no. 6, pp. 1299-1309, June 2022





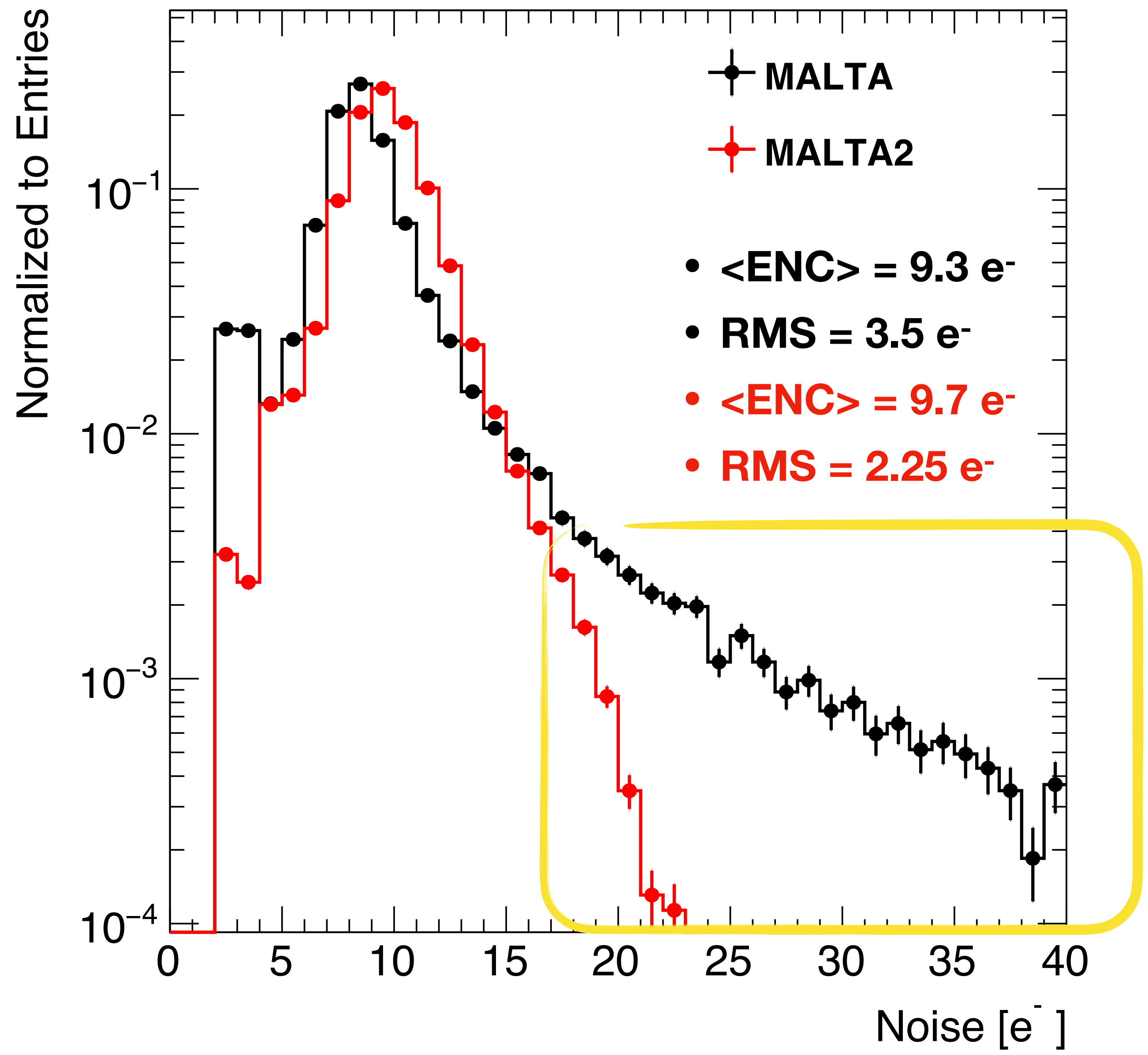
2nd prototype of MALTA family

- Improved FE:
  - enlarged transistors & cascode stage
    - lower noise & higher gain
- ☑ enables operating the chip at lower threshold (down to O(100) e^-)
- ☑ increases sensitivity to small signal
  - higher radiation tolerance
    - with same configuration (Ref. *JINST 15 (2020) 02*)

      std. transistors: thr = 340 el. , enlarged transistors = 200 el.

      eff @ 1×10^{15} n_{eq}/cm^2: std transistors=87%, enlarged transistors =98%
- ☑ improve speed of analog FE

Malta2 public plots



Comparison of MALTA & MALTA2 at compatible threshold (~340 e^-)

MALTA2 Timing: Front End

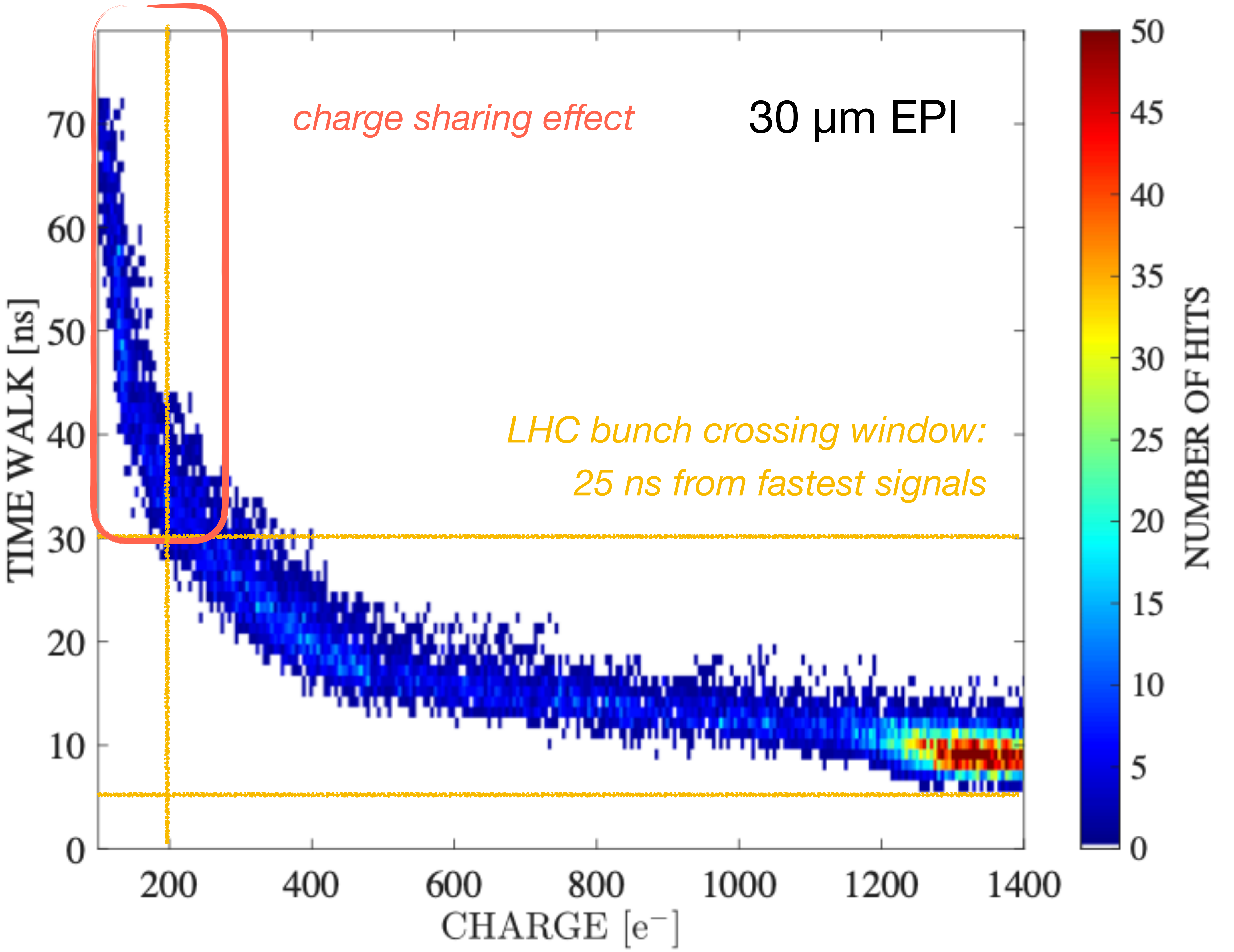
Time-walk of FE measured using special pixels with analog output monitoring.

- time for amplifier output to reach discriminator threshold, depends on charge deposition.

Sensor exposed to ^{90}Sr source

- MIP-like signals, avg. deposition ~1800 e^-

- **90% of hits arrive within 25 ns window**
  - **in-time threshold ➡ ~200 e–**
- largest deposited charges ➡ time-walk ~10 ns.
- small charge deposition attributed to charge-sharing effects
  - small signals from pixel corners arrives later



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MALTA2 Timing front end jitter

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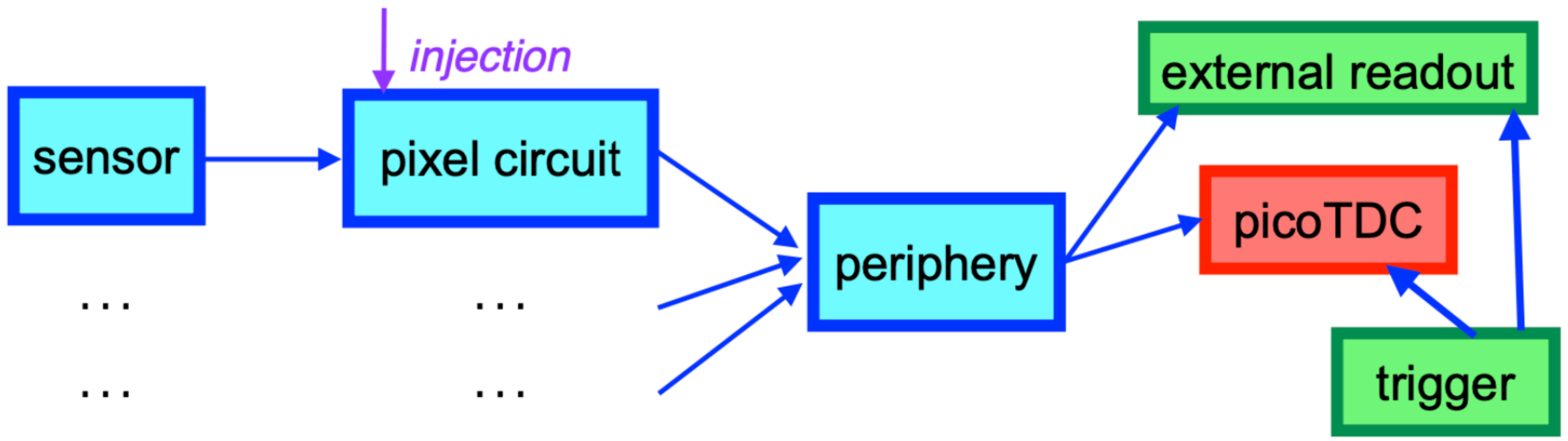
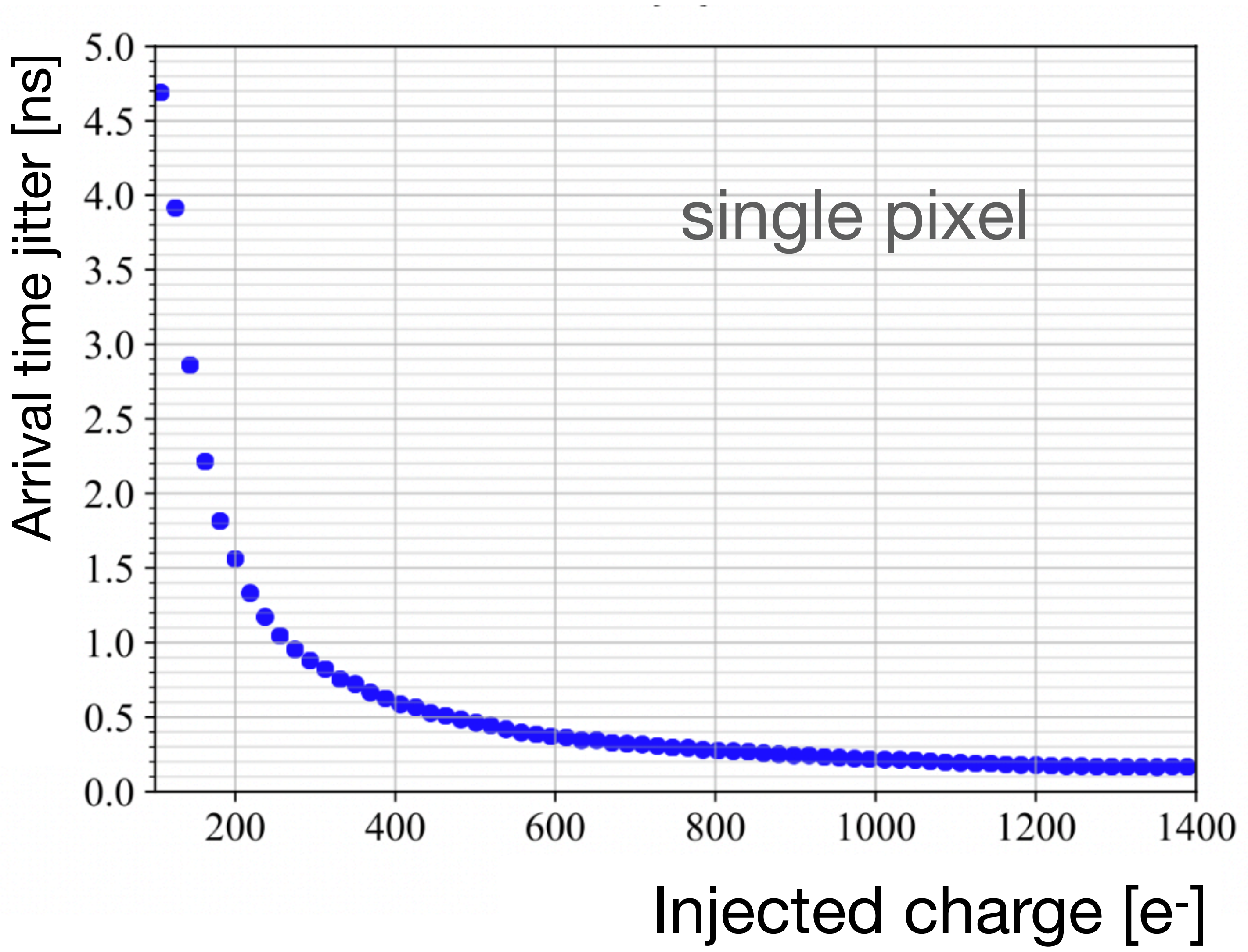
Set of measurements to isolate individual contributions:

- in-pixel charge injection
- chip interfaced with picoTDC (3 ps resolution)



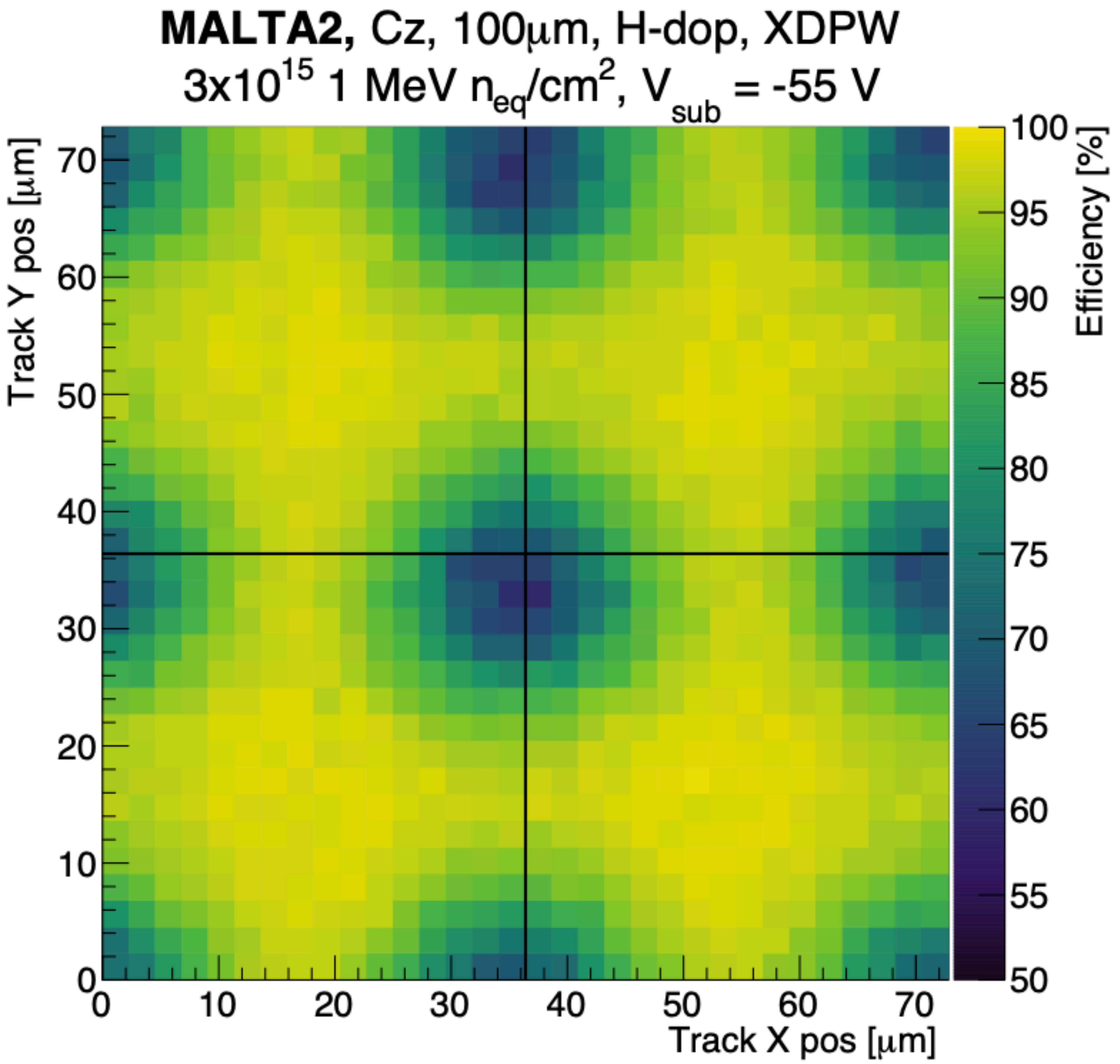
Measuring time jitter dominated by FE*

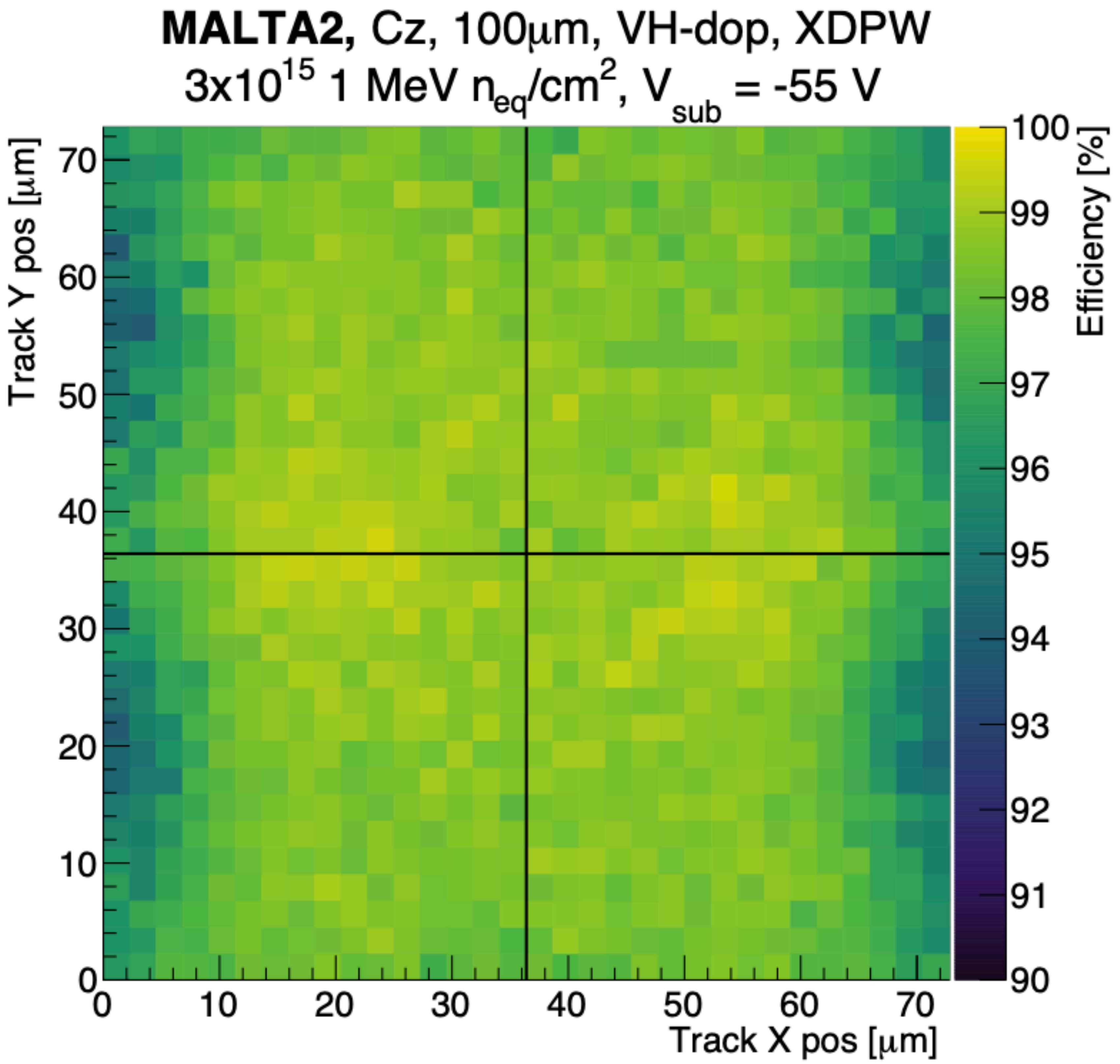
- varying between
  4.7 (100 e$^-$) to 0.16 ns (> 1200 e$^-$)
  as injected charge increases
  - 500 ps for 500 e$^-$
- uniform response across the entire chip



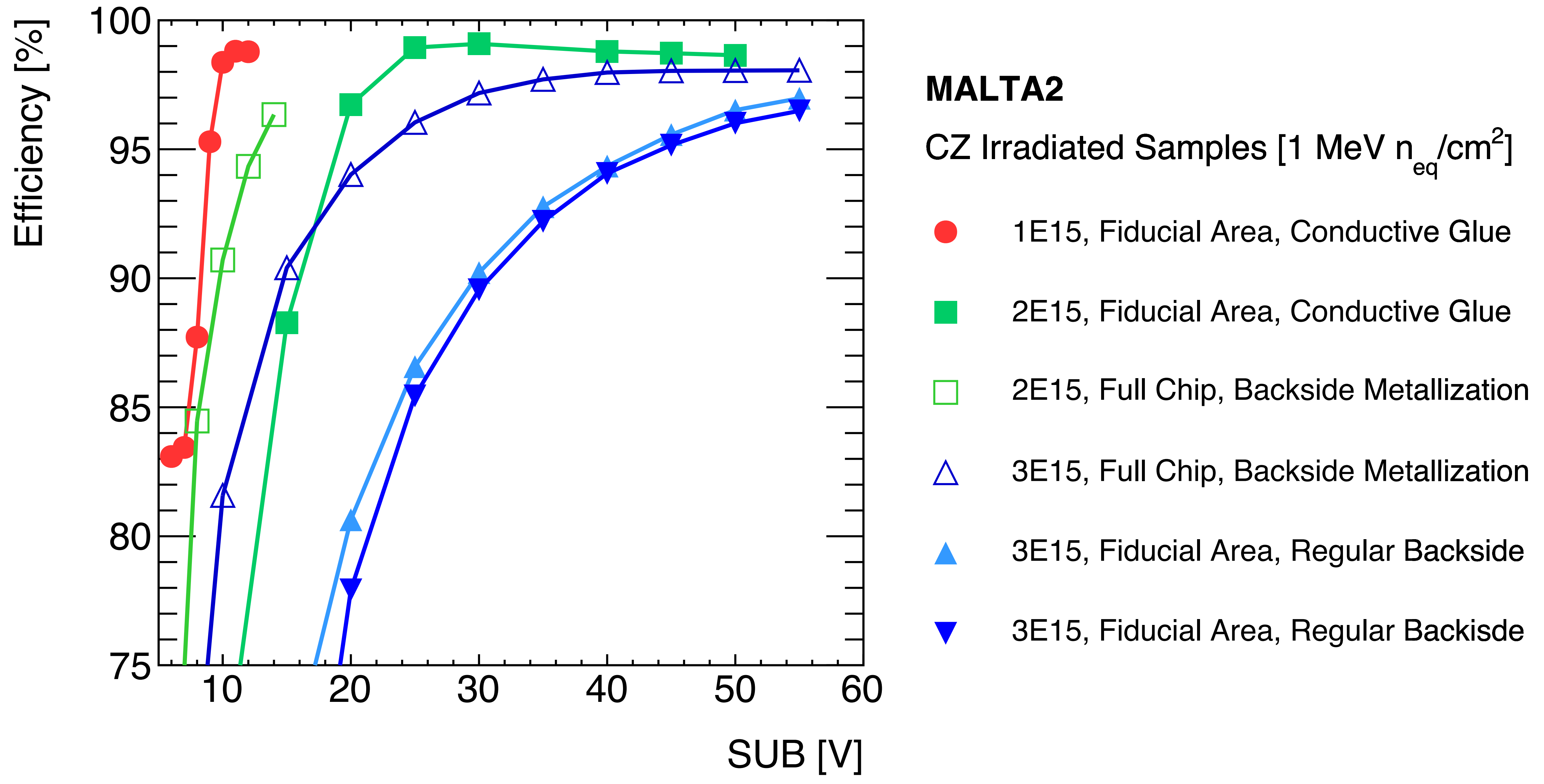
*time jitter of the reference pulse is < 100 ps

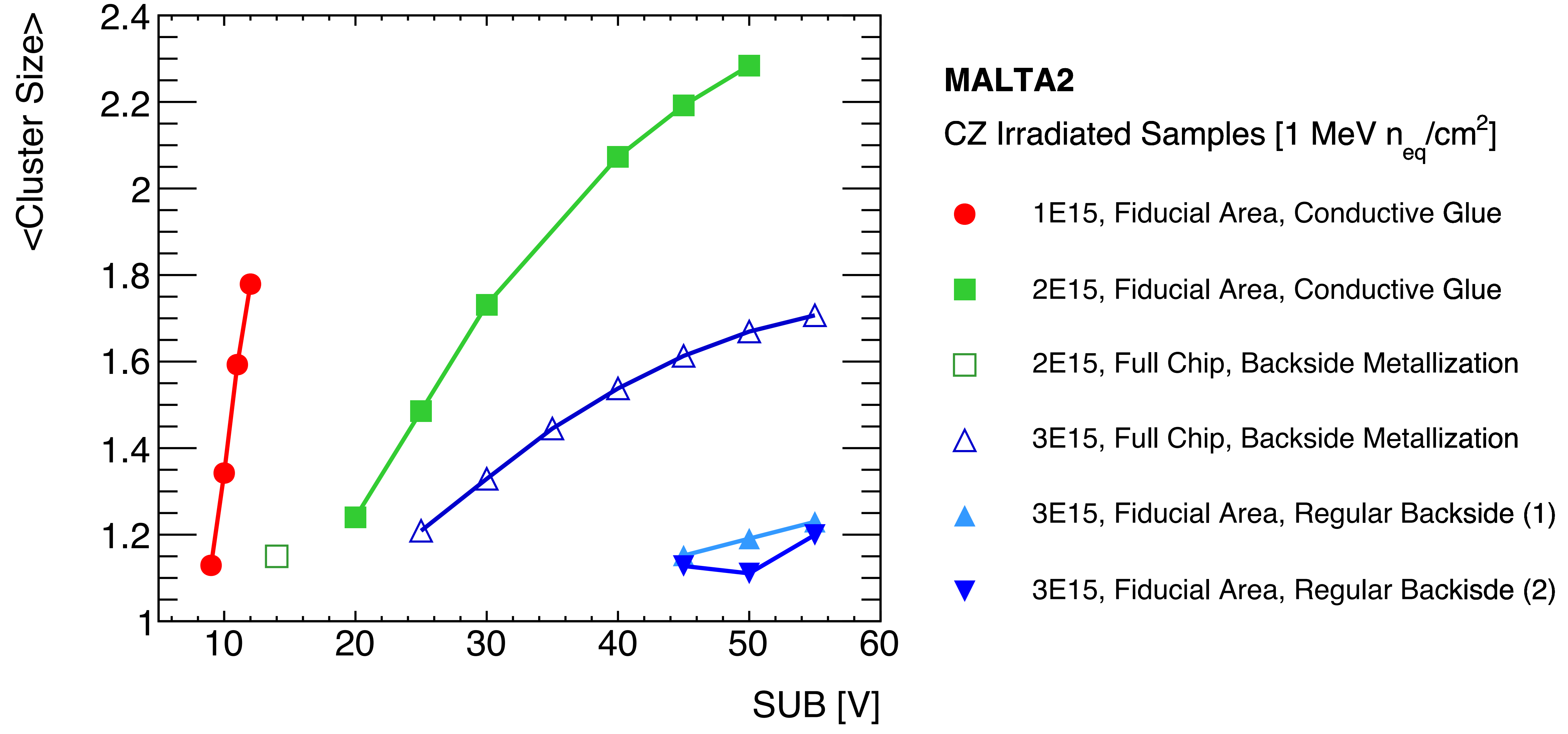
In-pixel efficiency

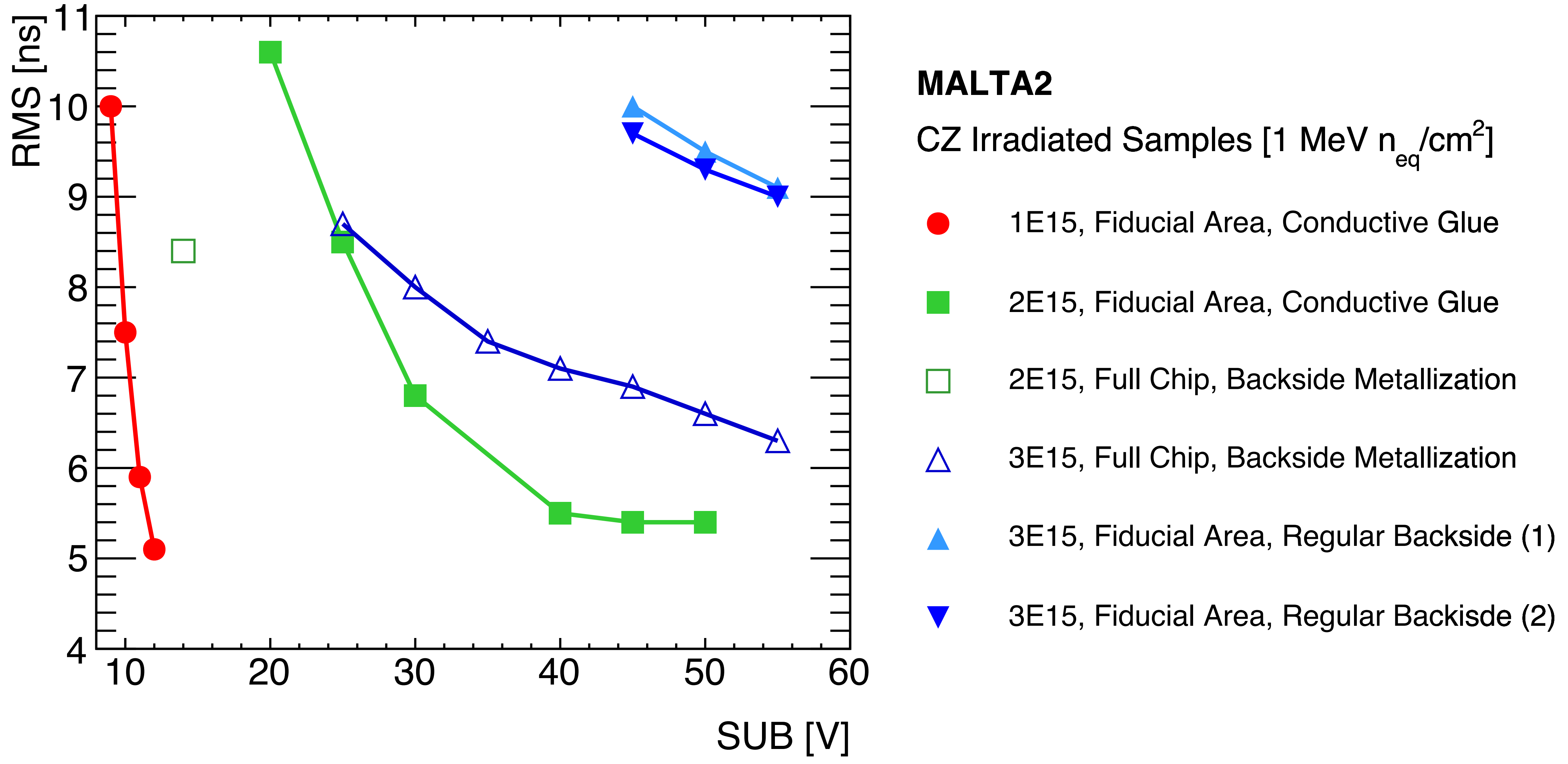




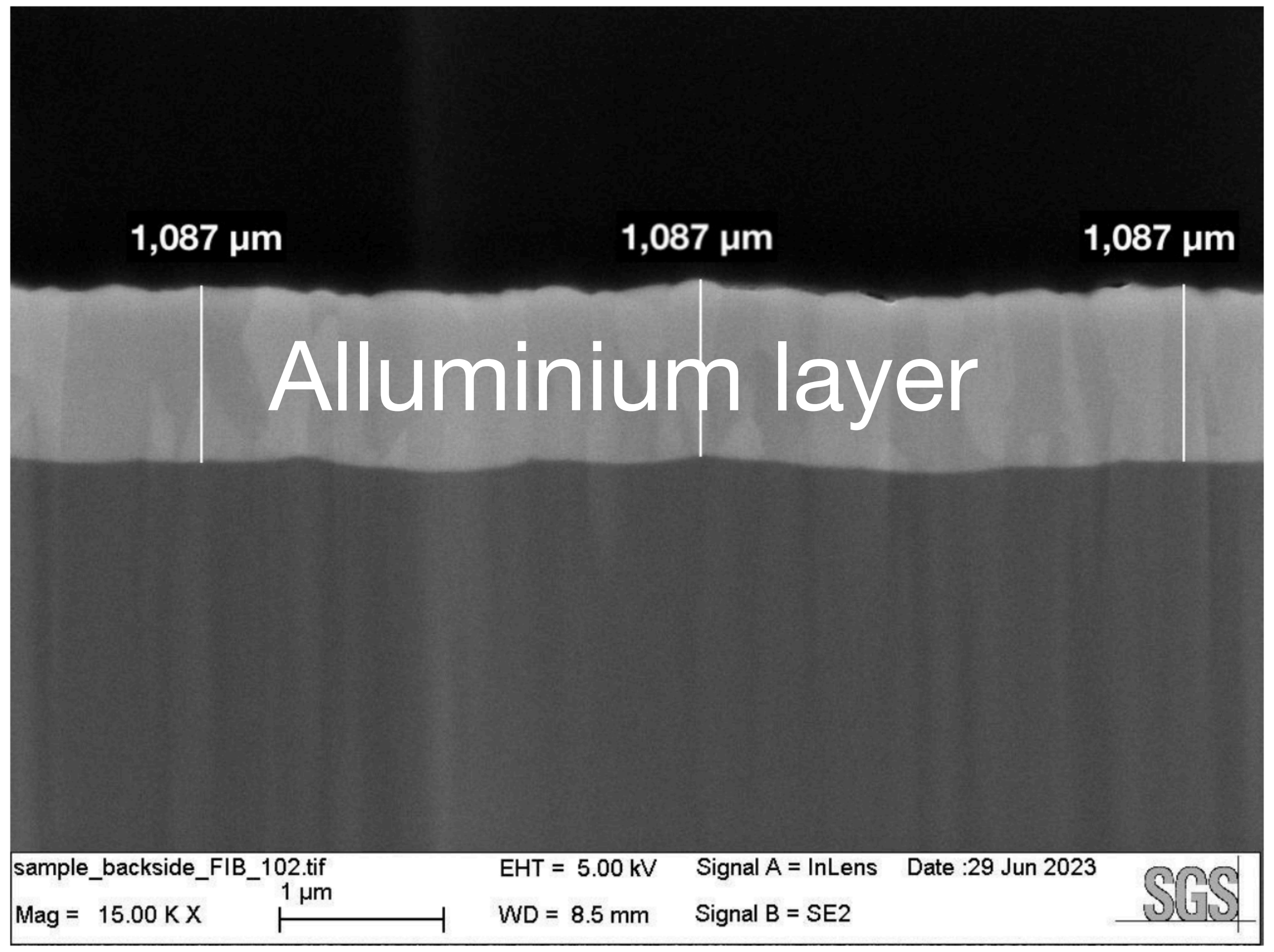
Summary plots



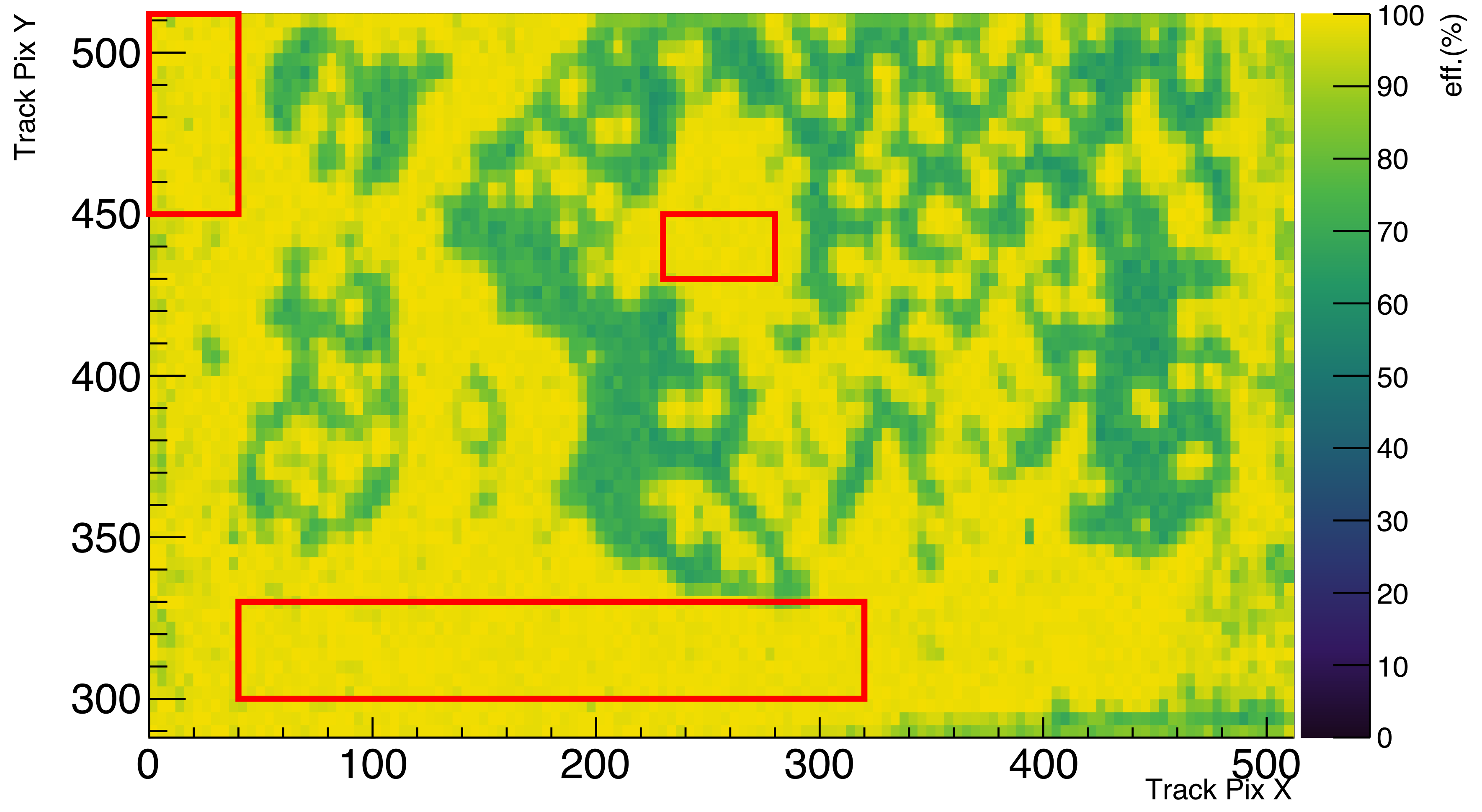




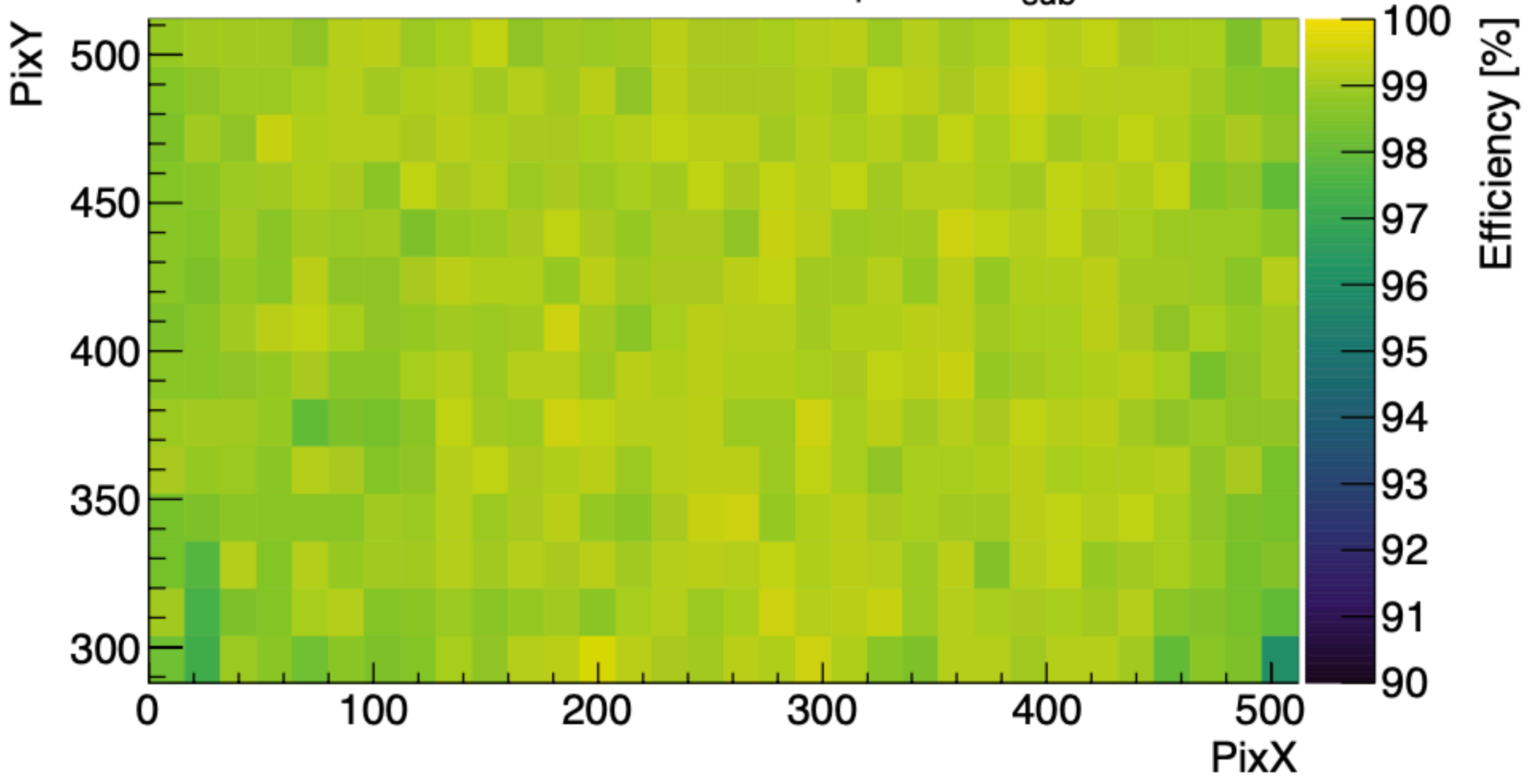
Back Metallisation



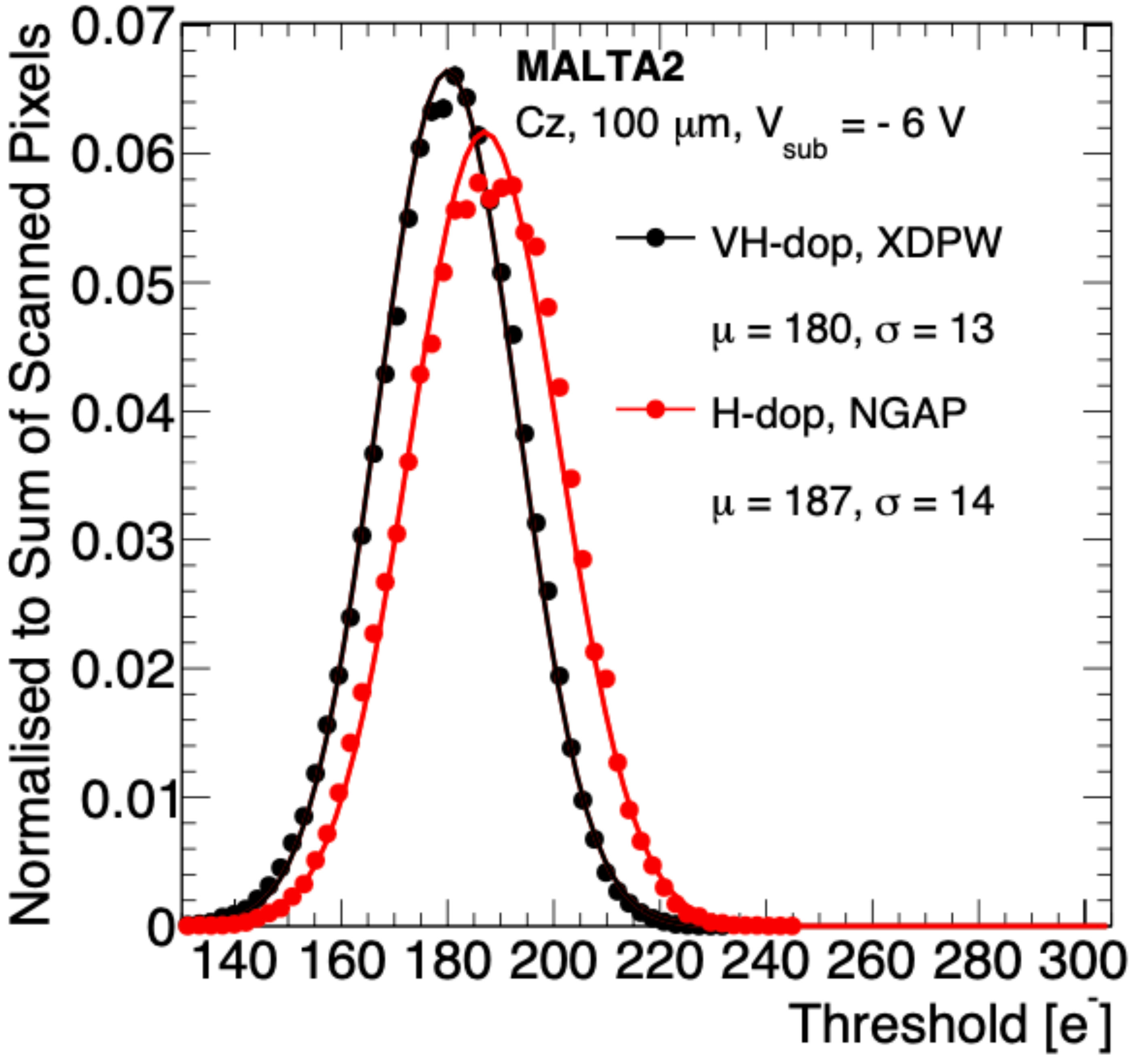
MALTA2, Cz, 100µm, H-dop, NGAP
conductive glue, 10^{15} 1 MeV n_{eq}/cm^2, V_{sub} = -12 V

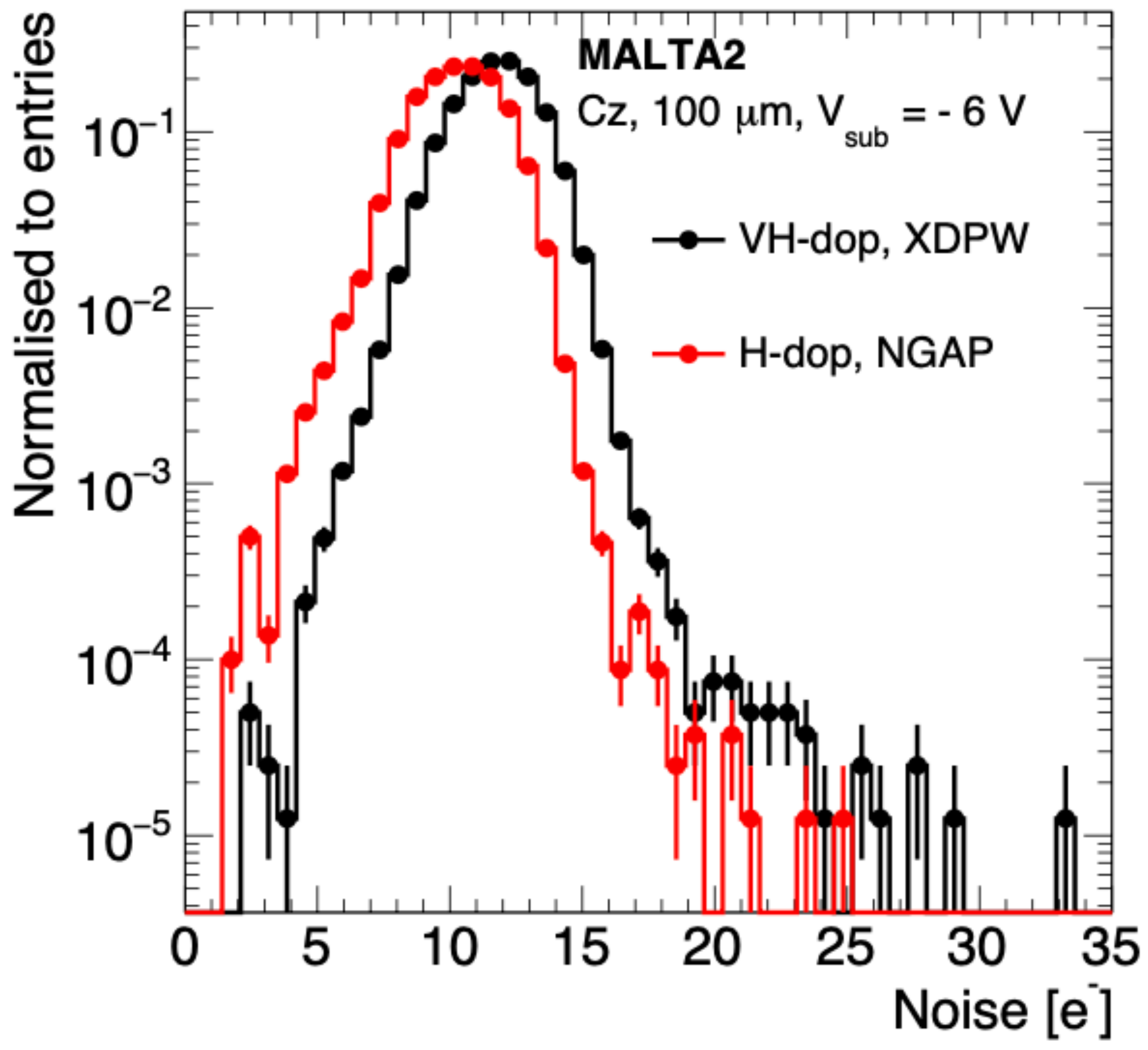


MALTA2, Cz, 100µm, VH-dop, XDPW
back-metal, 10^{15} 1 MeV n_{eq}/cm^2, V_{sub} = -15 V



High vs Very High n- doping layer





Larger noise is observed for the MALTA2 with the very high doping of the n⁻ layer.

- This effect is correlated to the **increase in capacitance due to the thinner depletion zone** around the collection electrode for a higher doped n– layer