16-20 October 2023, Sestri Levante (GE), Italy
International Workshop on Vertex Detectors

Recent results from MAPS prototypes for ITS3

Anna Villani
on behalf of the ALICE collaboration

VERTEX 2023

ALICE

INFN TRIESTE

UNIVERSITÀ DEGLI STUDI DI TRIESTE

Outline

- ITS3: The upgrade of the ALICE Inner Tracking System
- The 65 nm CMOS process
- Prototypes for the ITS3
- Results from laboratory characterization and in-beam measurements

ITS3: an innovative vertex detector

ALICE Inner Tracking System for LHC Run 4

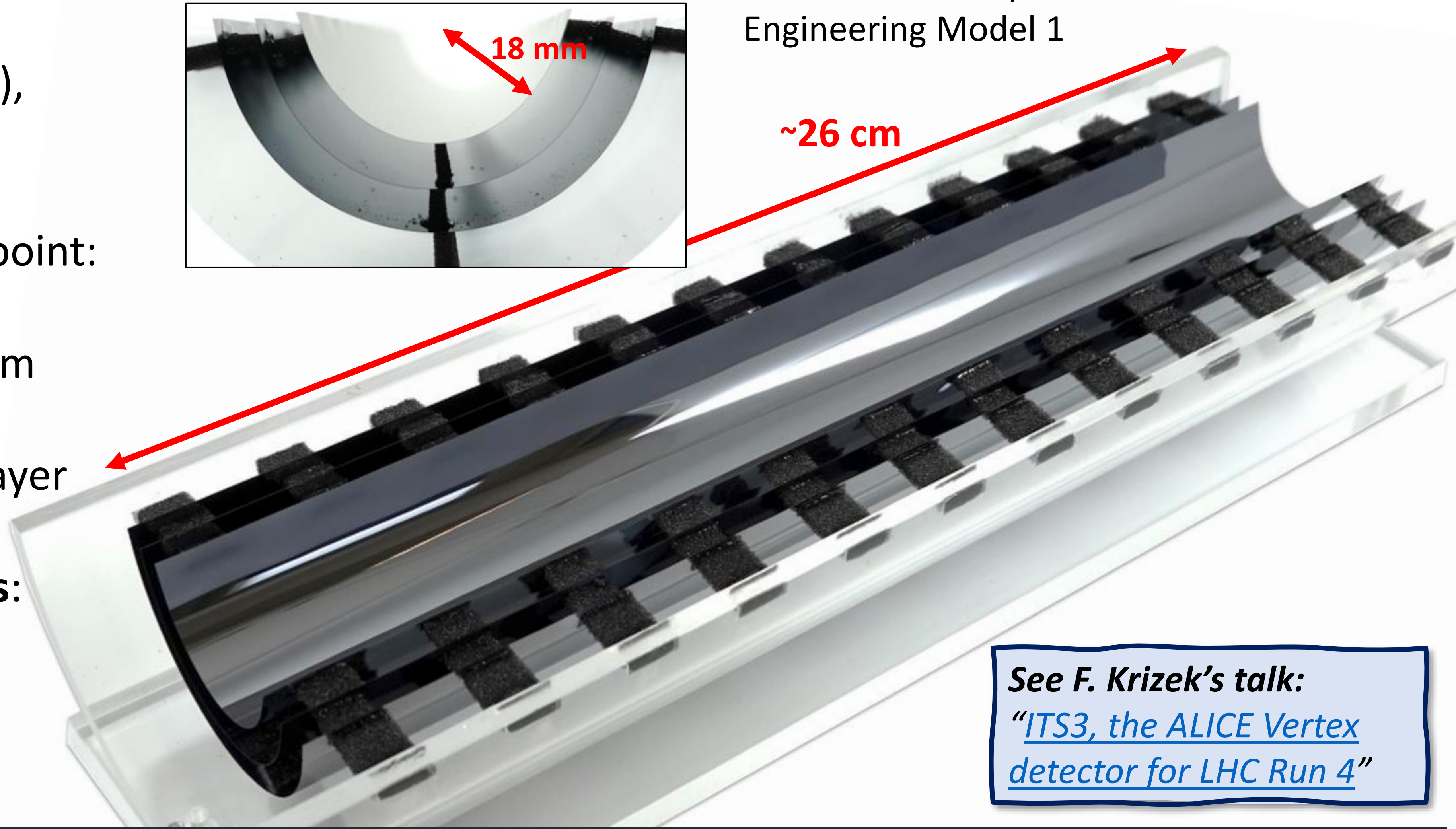
Key elements:

- 6 large-area O(10×26 cm^2), ultra-thin (≤50 µm), flexible MAPS sensors
- Closer to the interaction point: 24 mm (ITS2) → 18 mm
- Reduced and more uniform material budget: 0.3% (ITS2) → 0.05% X_0/layer

Performance improvements:

- Tracking efficiency
- Pointing resolution

Mechanical mockup of three ITS3 half-layers, Engineering Model 1

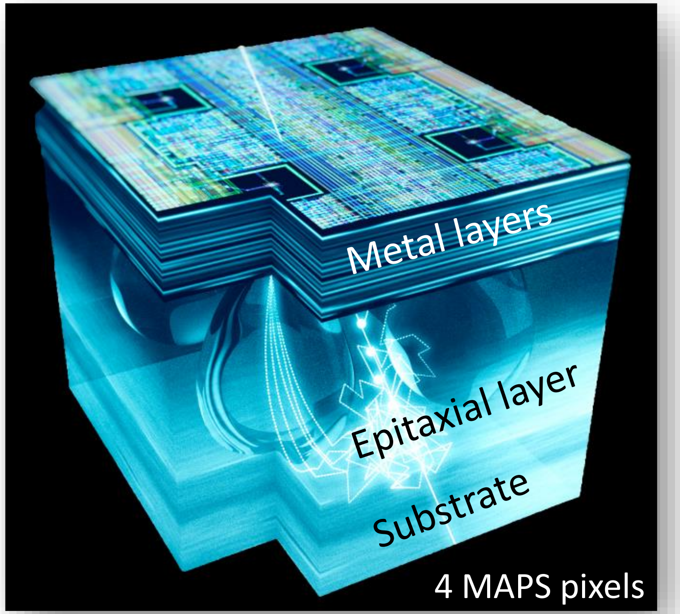


See F. Krizek's talk:
"[ITS3, the ALICE Vertex detector for LHC Run 4]"

The 65 nm CMOS technology

- Tower Partners Semiconductor Co. (TPSCo) 65 nm CMOS imaging process for Monolithic Active Pixel Sensors (MAPS)
- Chosen for ALICE ITS3 detector and under study by the CERN EP R&D on monolithic pixel sensors

Key advantages:	
• High radiation hardness	• 5 µm 2D spatial resolution
• Low power consumption	• Large wafers (Ø 300 mm)



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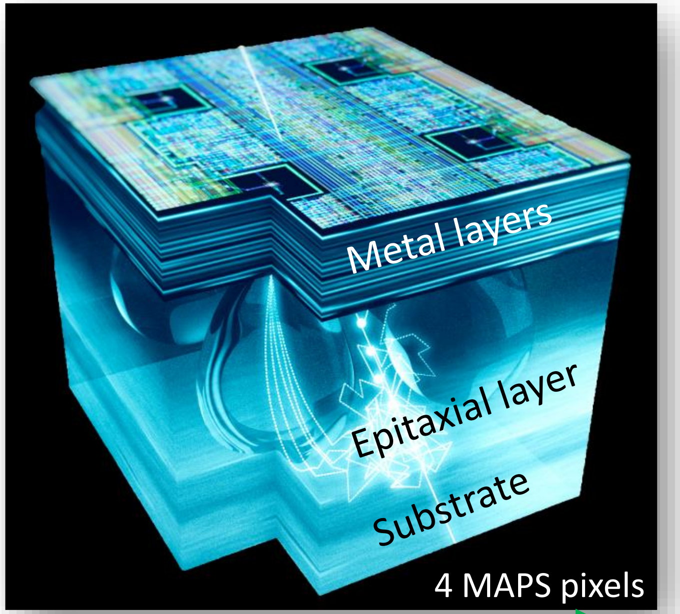

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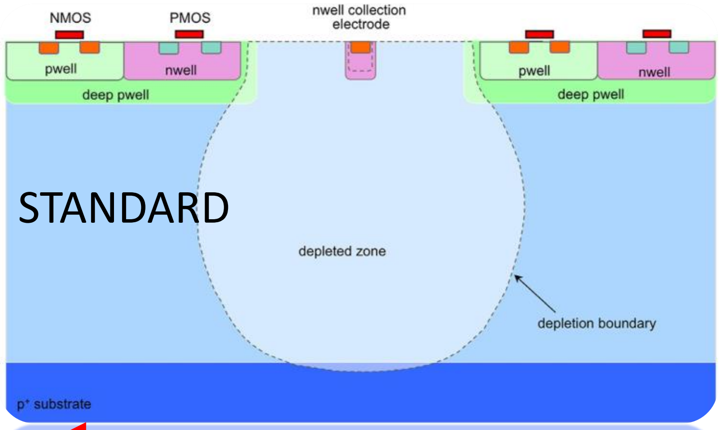
Three process options explored:

Charge collection faster and more efficient



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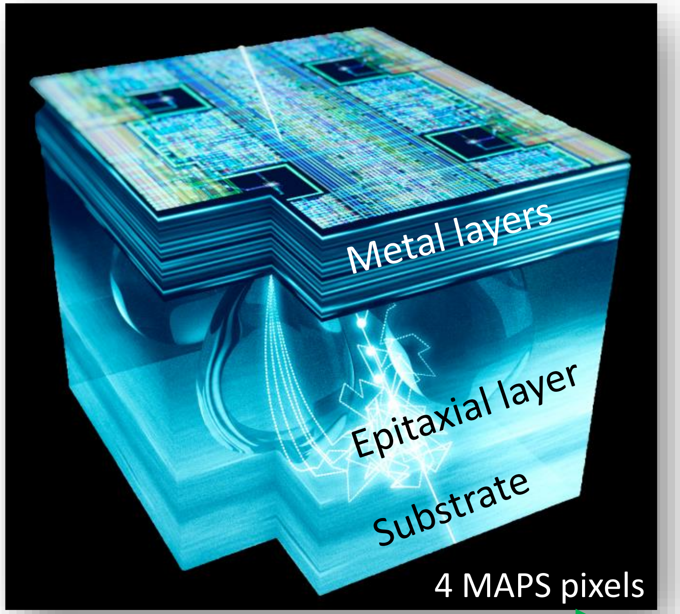

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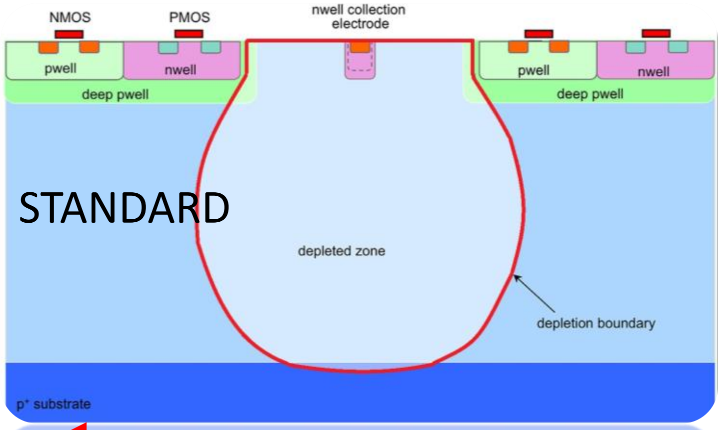

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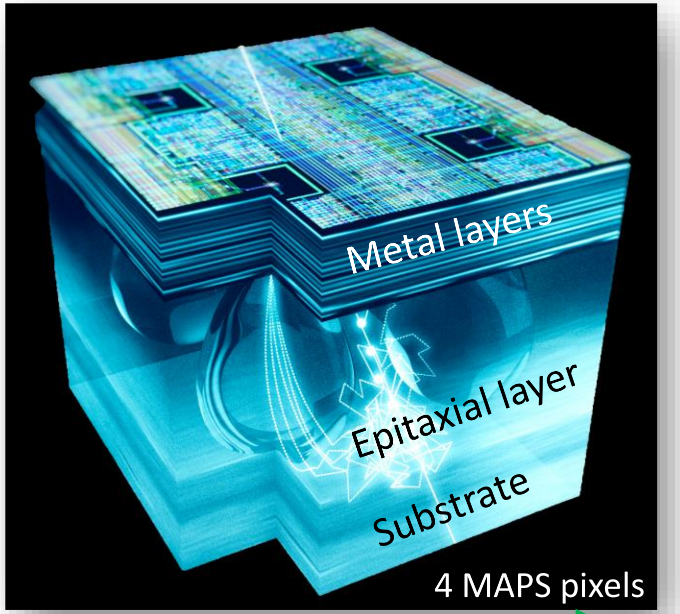

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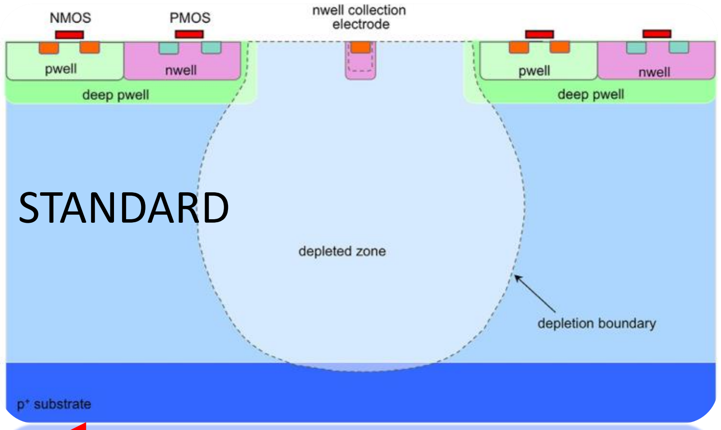

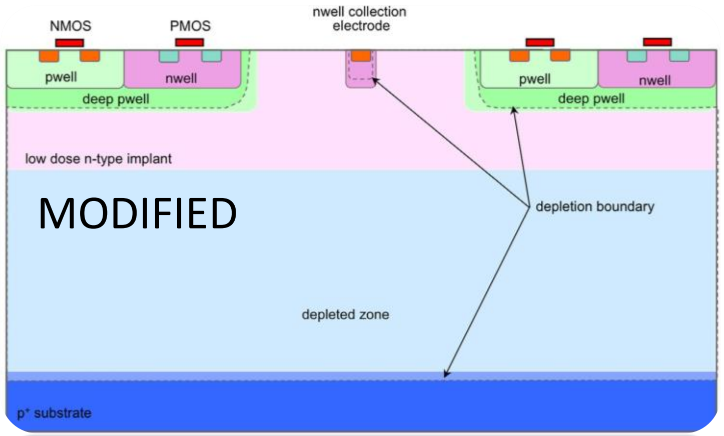

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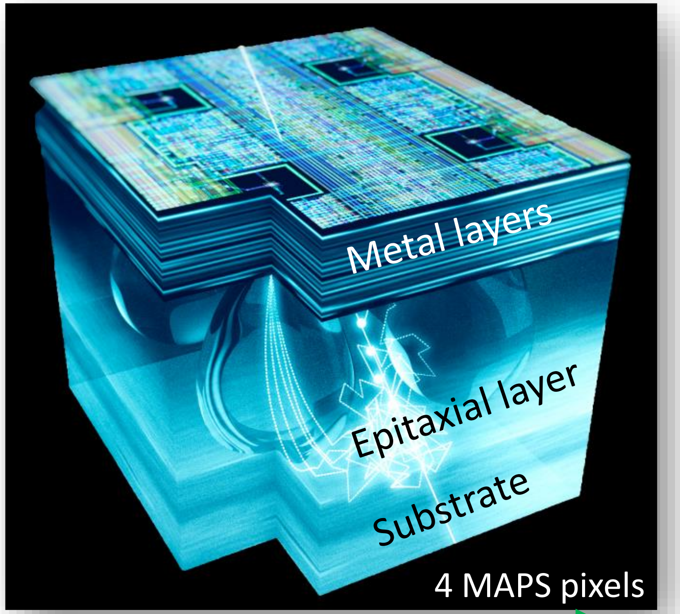

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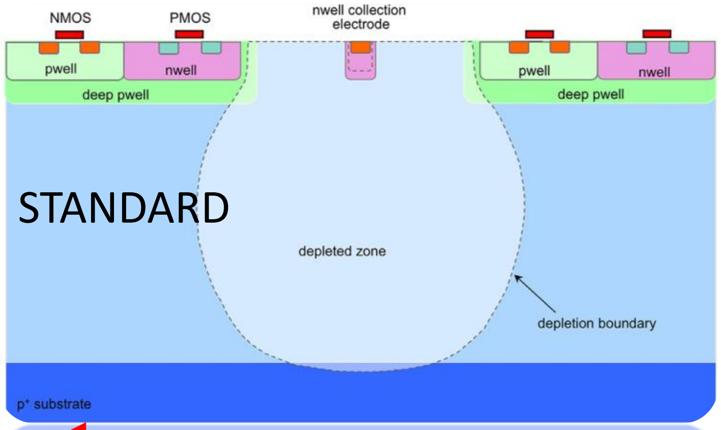

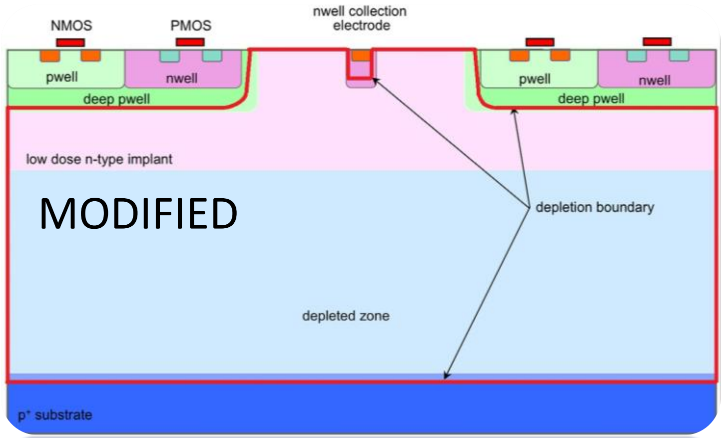

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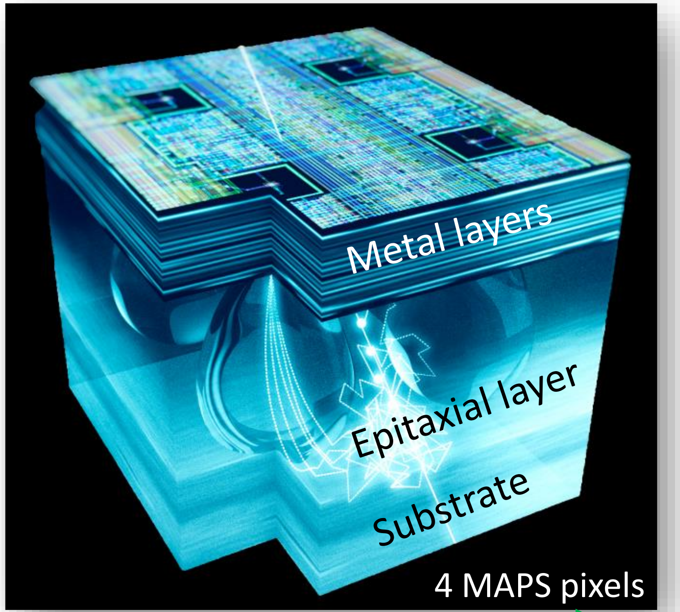

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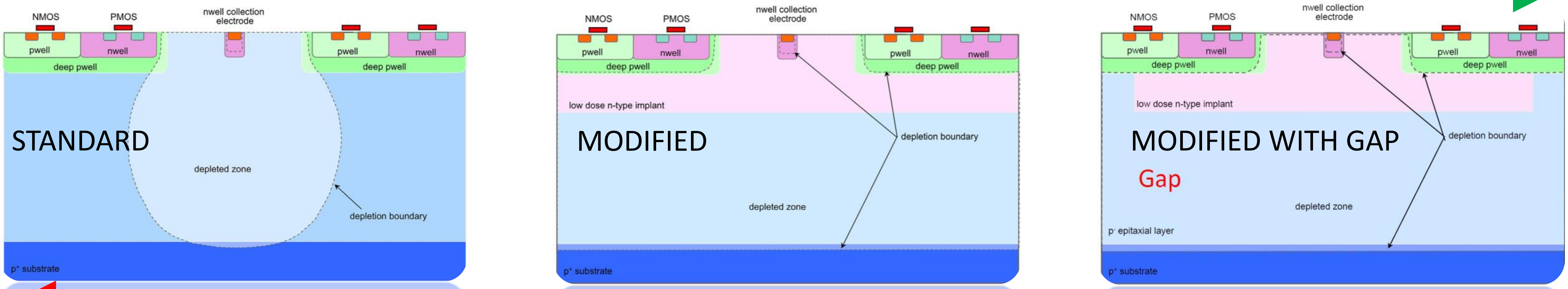

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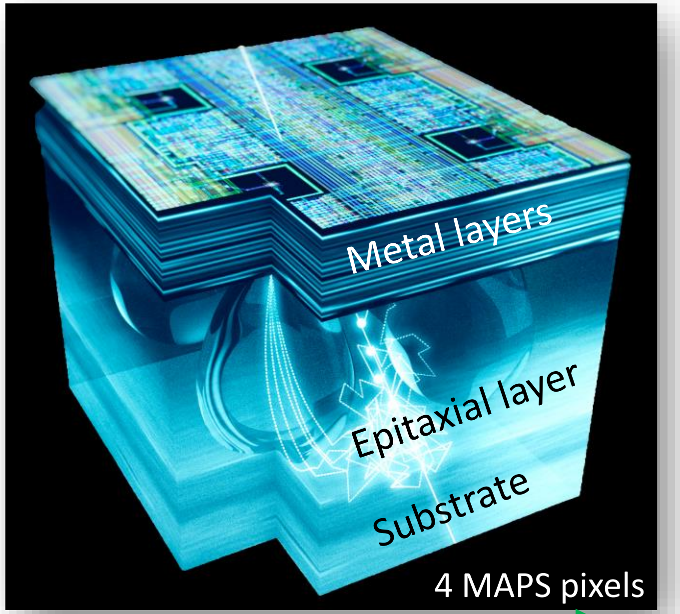

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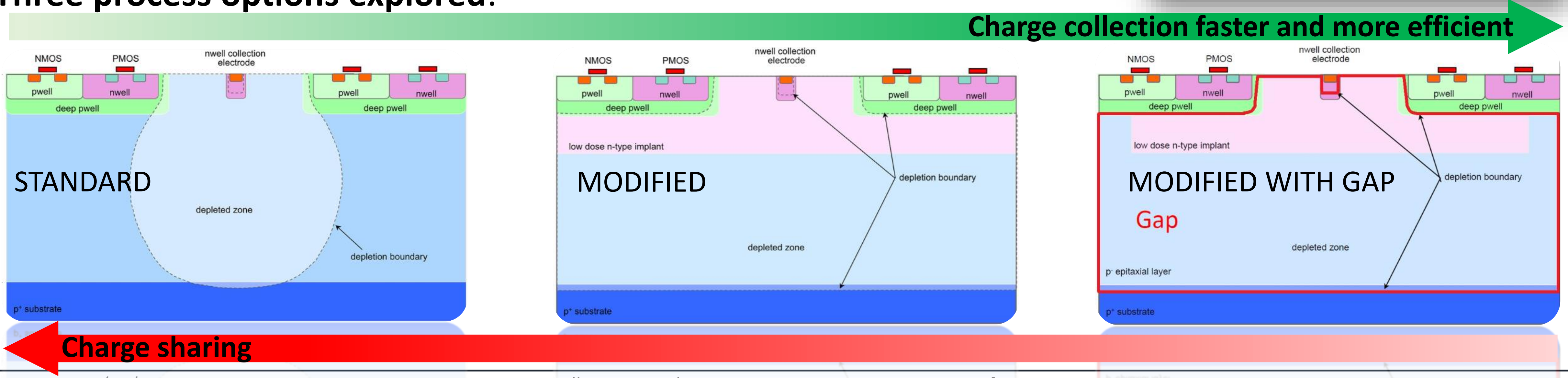
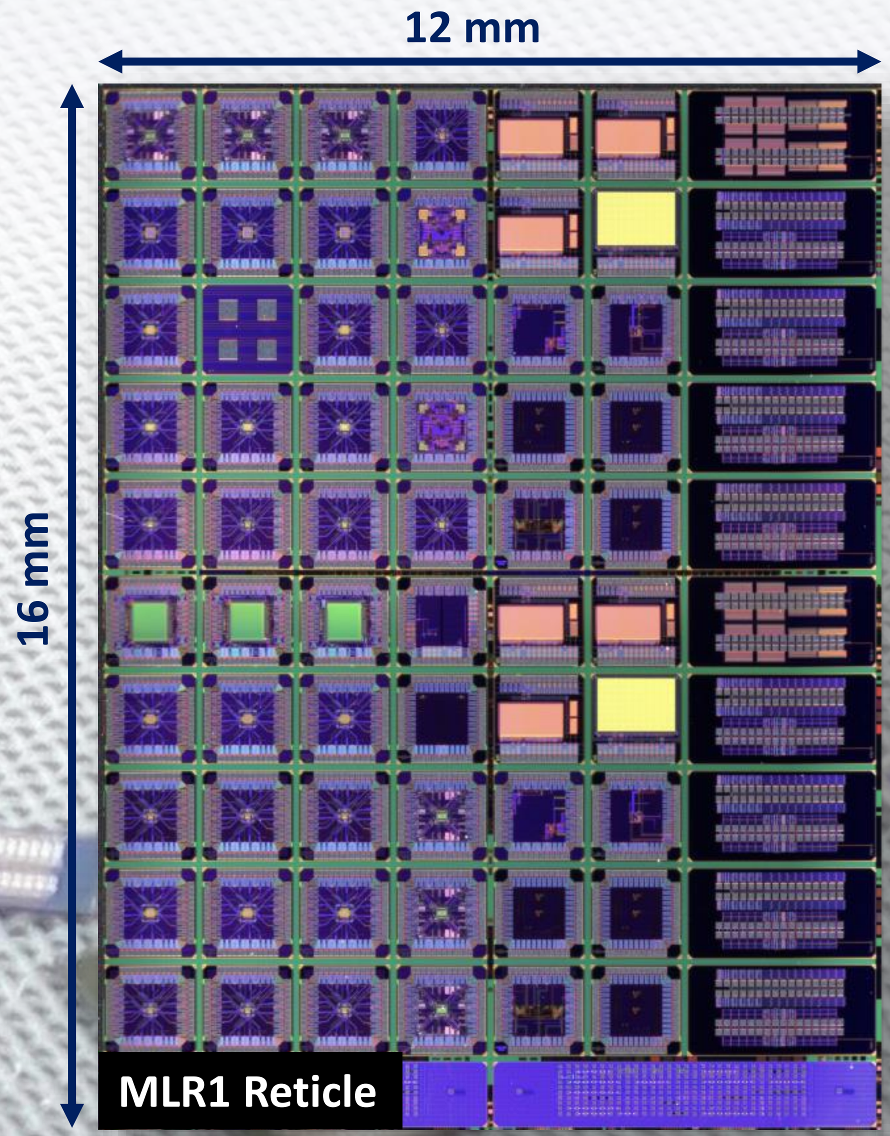
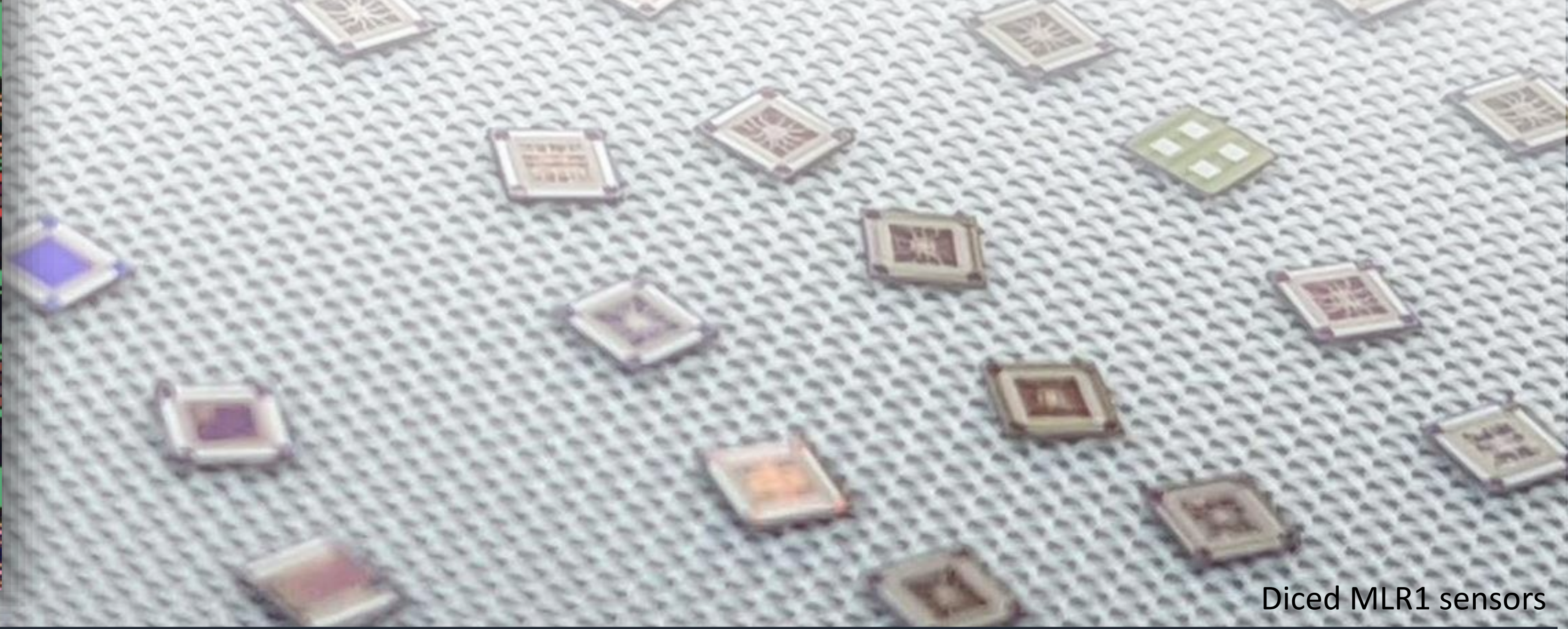


MLR1: first submission in 65 nm

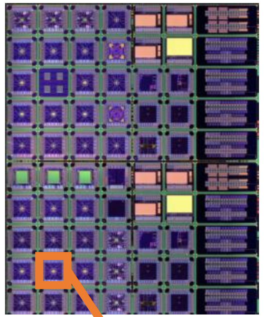


- **M**ultiple **L**ayer **R**eticle **1** (**MLR1**), received in Sep. 2021
- Many prototypes:
  - Transistor test structures → radiation hardness studies
  - Diode matrices → charge collection studies
  - Analog building blocks
  - Digital test matrices

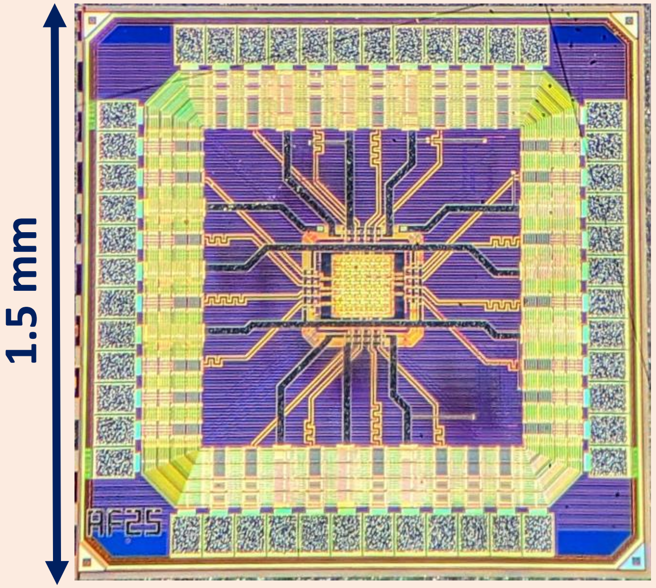


Diced MLR1 sensors

MLR1 sensor prototypes

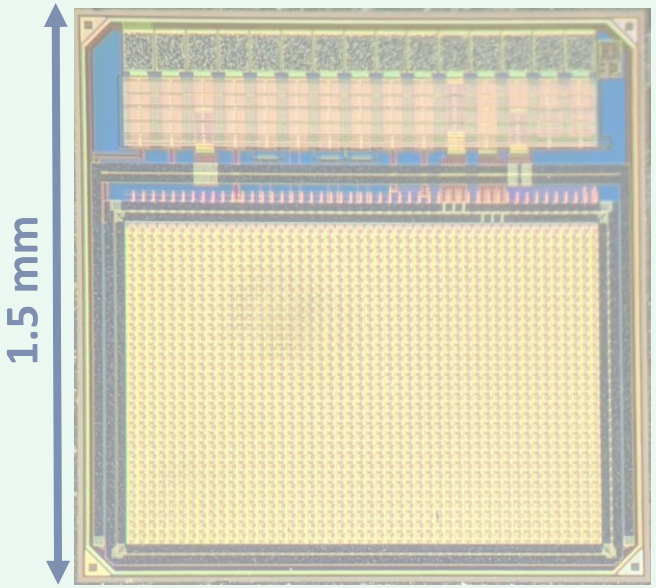


APTS: Analog Pixel Test Structure



- 6×6 pixel matrix
- Pitch: 10, 15, 20, 25 µm
- Analogue readout of central 4×4 submatrix
- Output buffer in two versions: Source Follower (SF) and Op Amp (OA)
- **Goal**: explore pixel designs

CE65: Circuit Exploratoire 65



- 64×32 pixel matrix, 15 µm pitch (3 subvariants: AC, DC and SF)
- 48×32 pixel matrix, 25 µm pitch
- Rolling shutter readout (50 µs integration time)

- **Goal**: explore pixel matrix uniformity and rolling shutter

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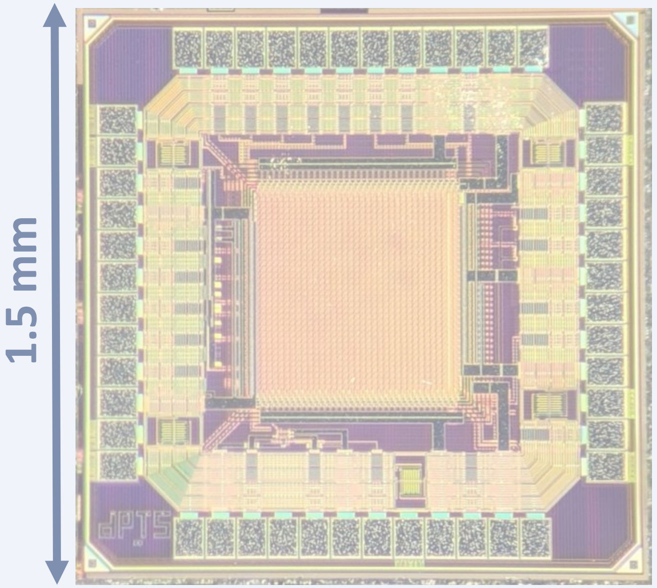
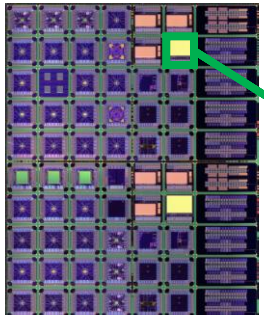


- 32×32 pixel matrix, 15 µm pitch
- Asynchronous digital readout
- Time-encoded pixel position
- Time-over-threshold measurements

- **Goal**: study the in-pixel front-end

MLR1 sensor prototypes



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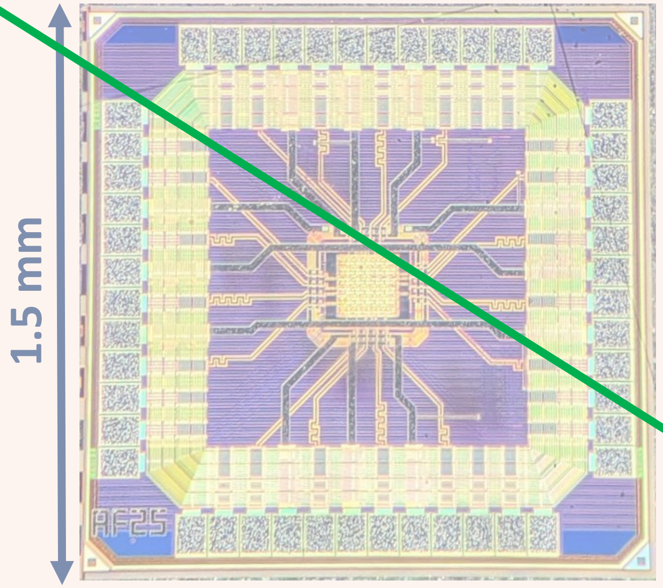

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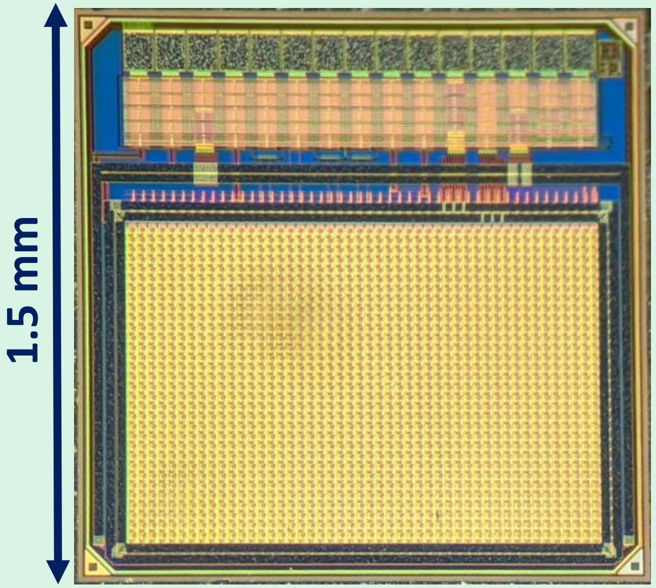

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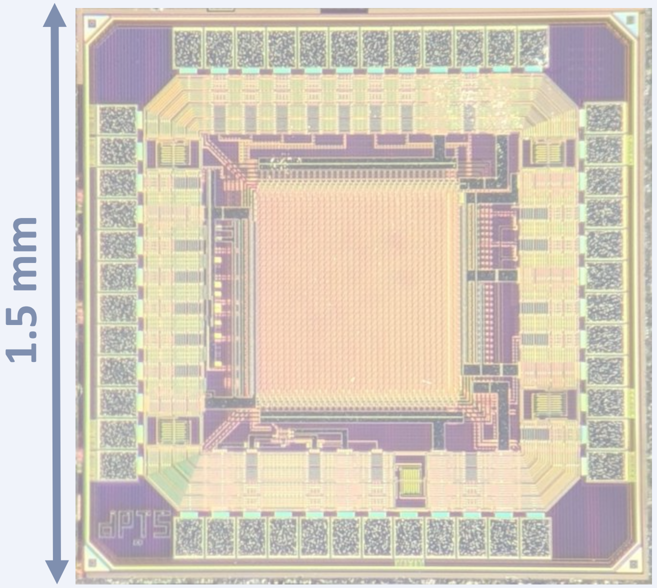

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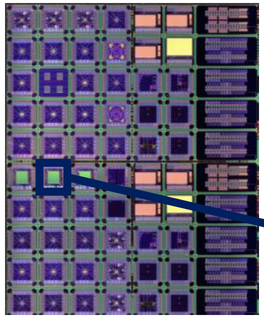

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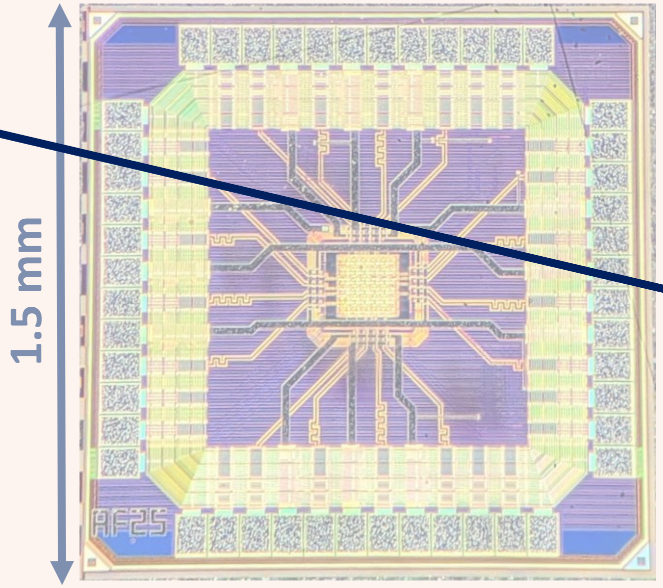

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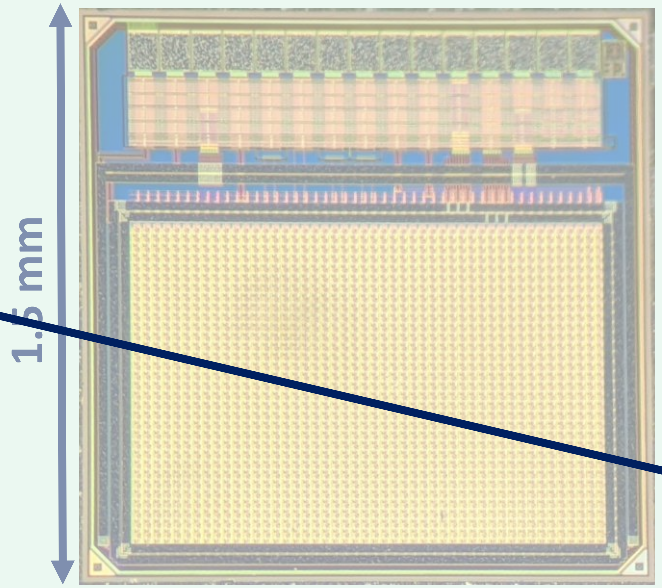

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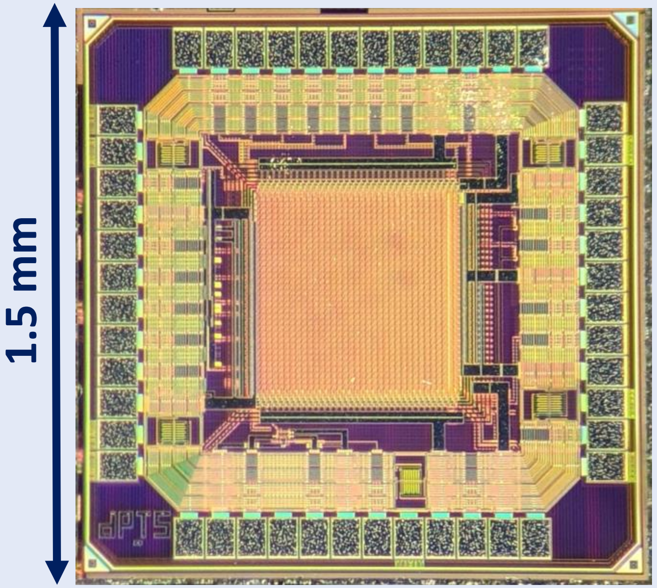

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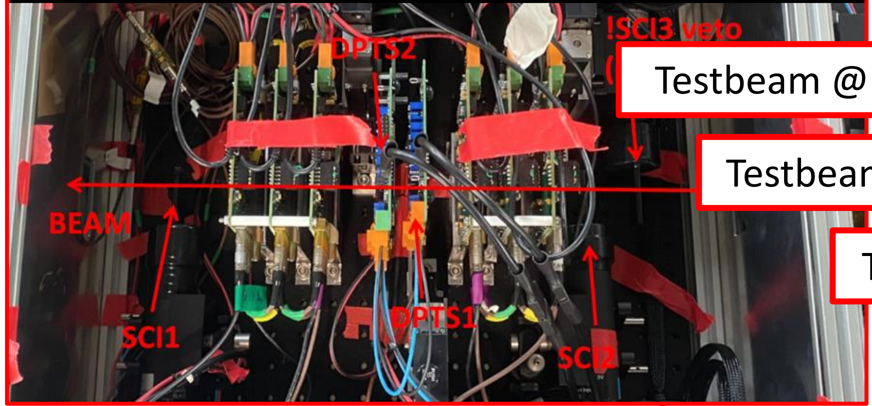
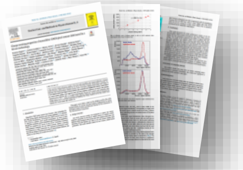
- **Goal**: study the in-pixel front-end

Prototype test campaign

- Laboratory measurements:
  - Definition of the operating conditions
  - Response to X-ray: ^{55}Fe source and fluorescence photons
- Test-beam campaigns @DESY, @MAMI, @CERN PS, @CERN SPS

Testbeam @ DESY 06-13 Sep 2021





2022: https://doi.org/10.1016/j.nima.2022.167213

2023: https://doi.org/10.1016/j.nima.2022.167213

Timeline (2021 – 2022 – 2023):

- 2020: first submission in 65 nm
- 09/2021: received MLR1 chips
- Testbeam @ PS Oct 2021
- Testbeam @ SPS Nov 2021
- Testbeam @ DESY Mar 2022
- Testbeam @ MAMI Apr 2022
- Testbeam @ PS May 2022
- Testbeam @ PS Jun 2022
- Testbeam @ PS Aug 2022
- Testbeam @ SPS Oct 2022
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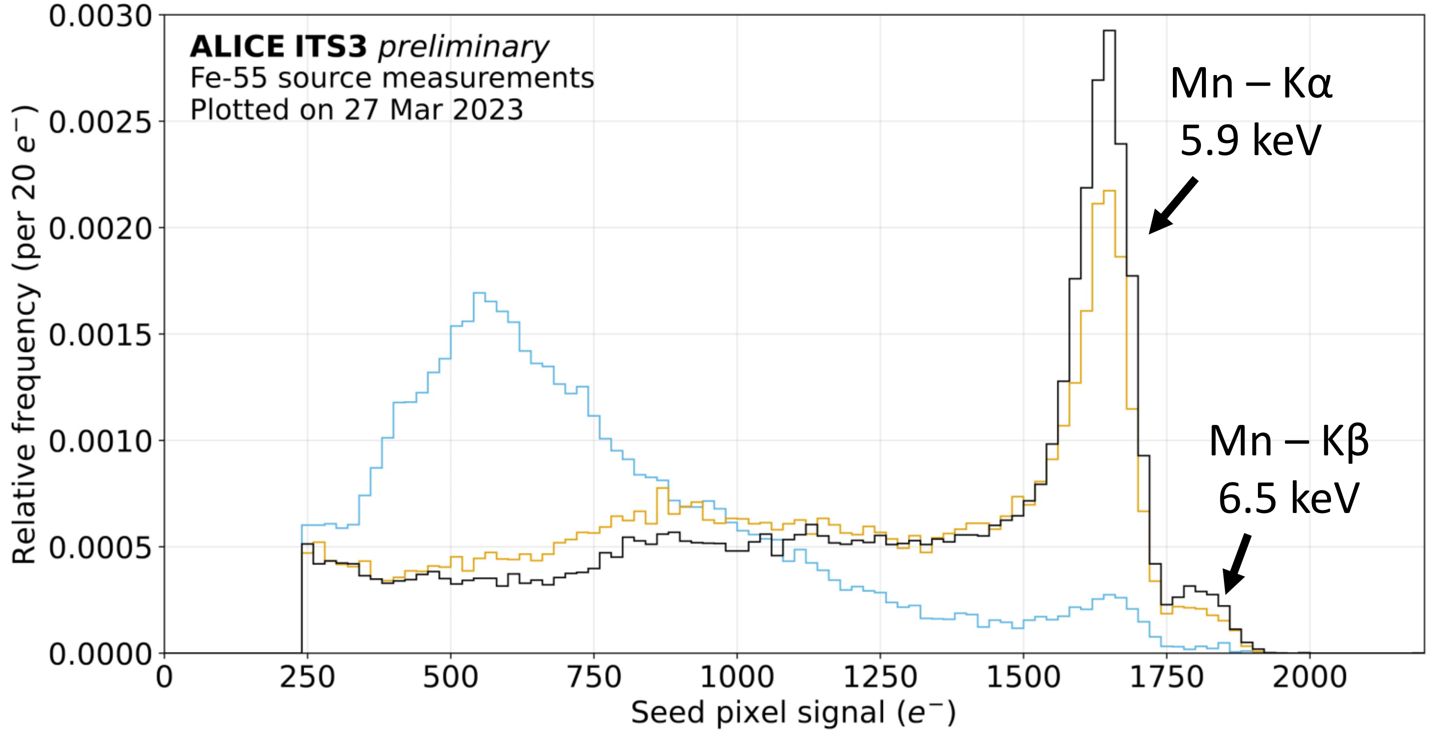
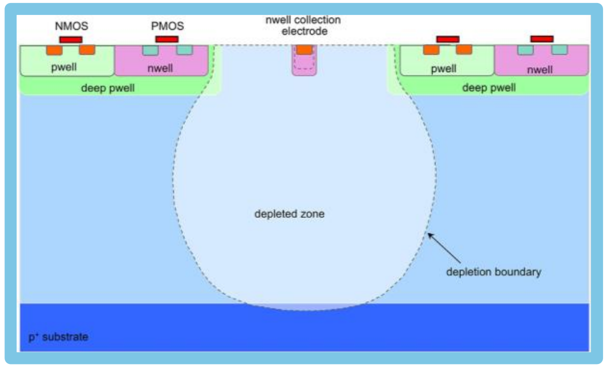
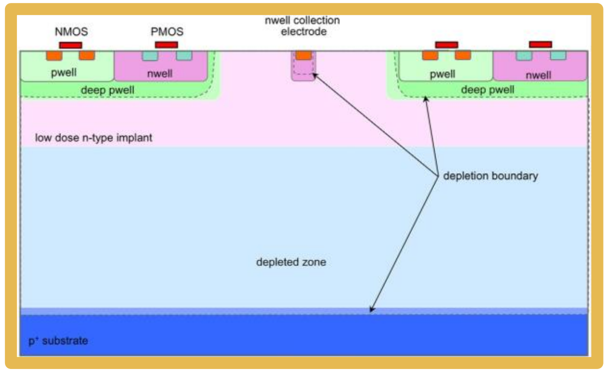
- Testbeam @ SPS Jul 2023

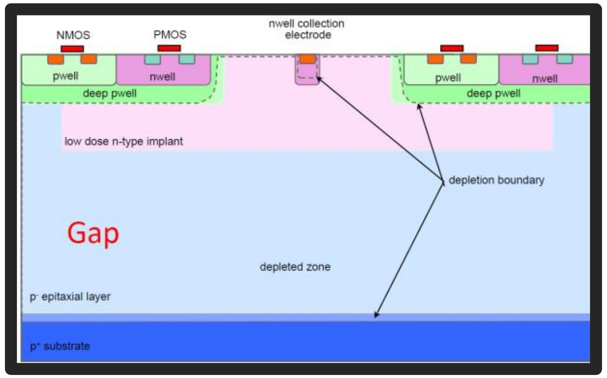
APTS SF: process selection

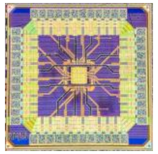
- ^{55}Fe source measurements











Analog **P**ixel **T**est **S**tructure

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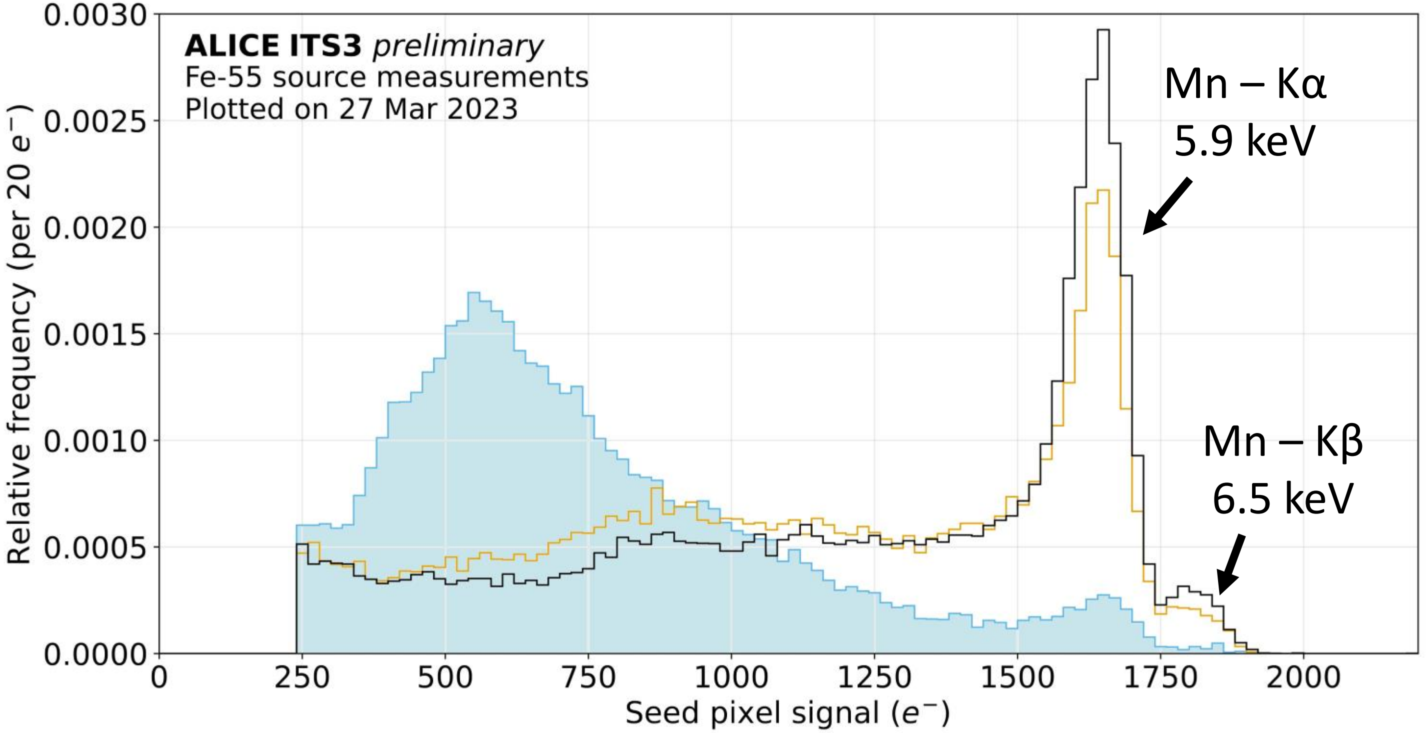
- ^{55}Fe source measurements:
  - Standard process → relevant charge sharing



APTS SF
pitch: 15 µm
split: 4
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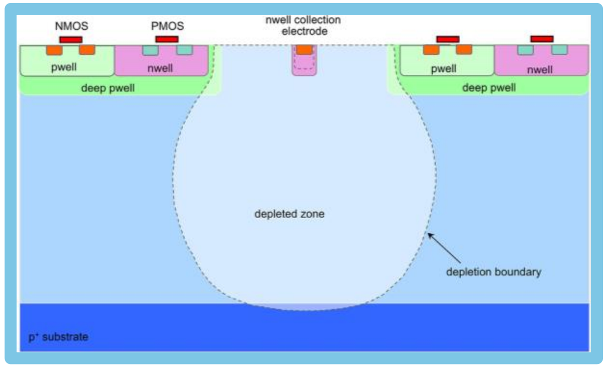
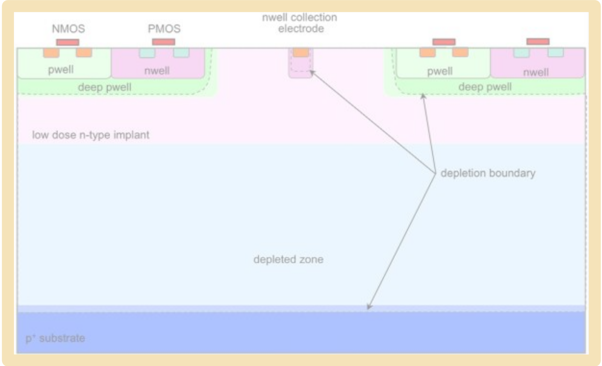
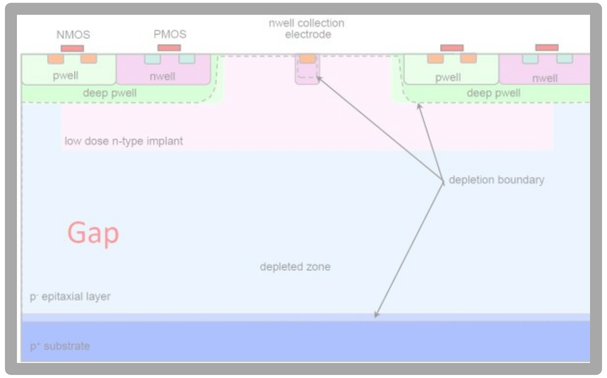
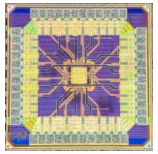
Standard
Modified
Modified with gap









Analog
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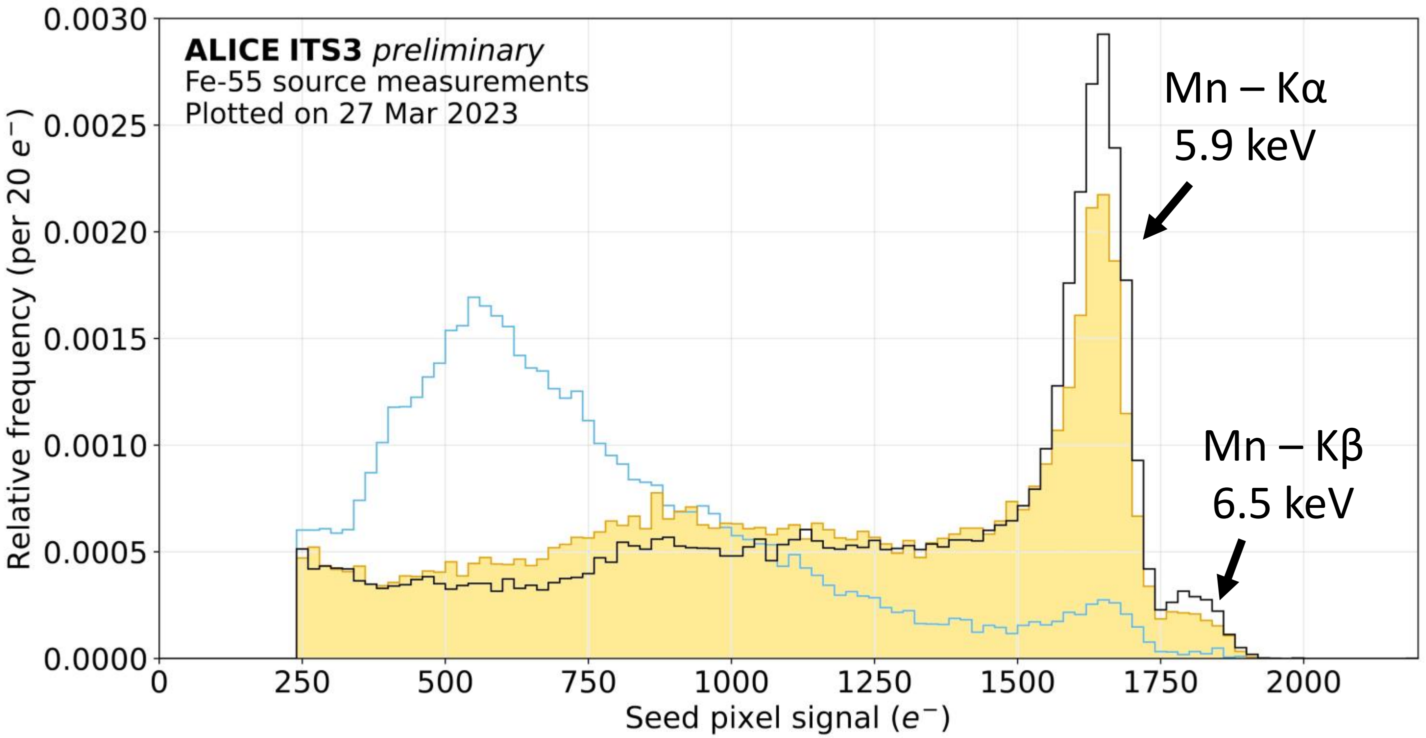
  - Modified process → complete depletion of the active layer, less charge sharing



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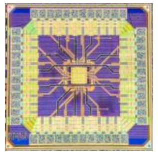

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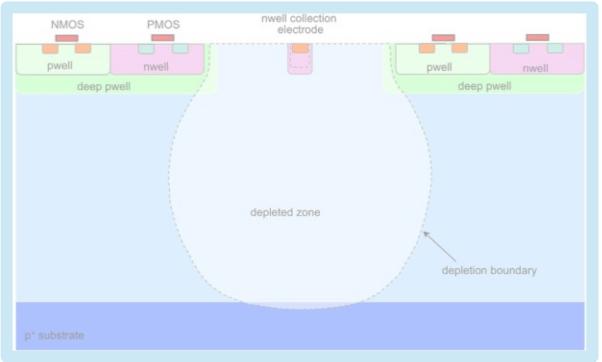

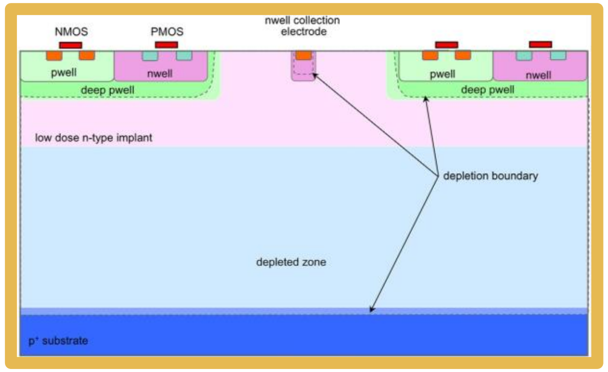

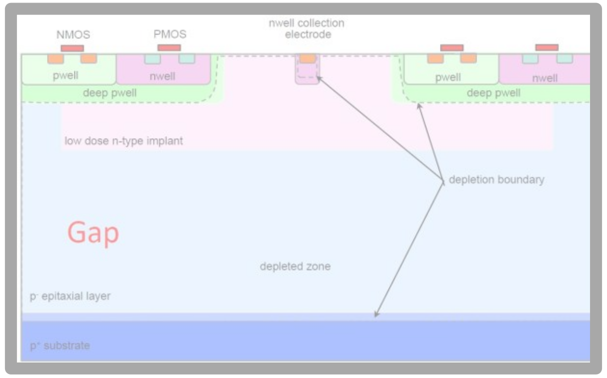

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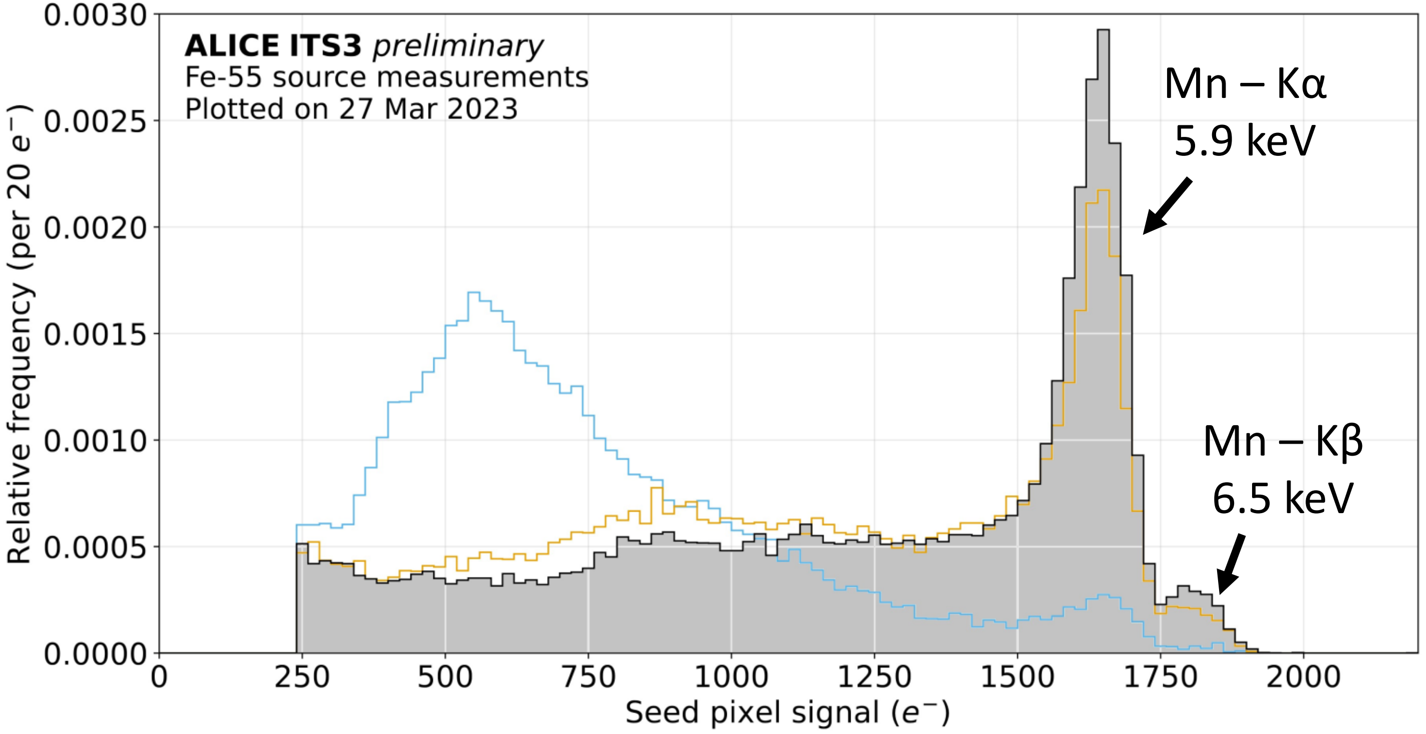
  - Modified process → complete depletion of the active layer, less charge sharing
  - Modified with gap → improved modified process, optimal charge collection



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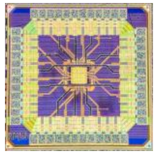

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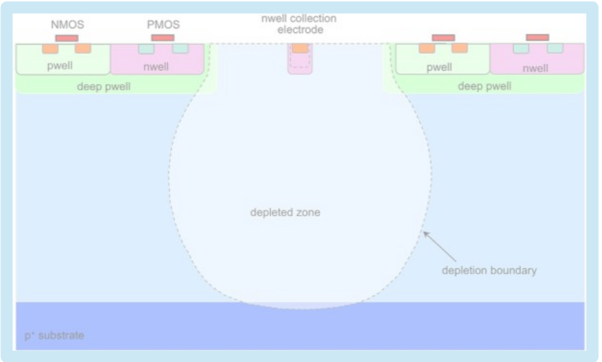
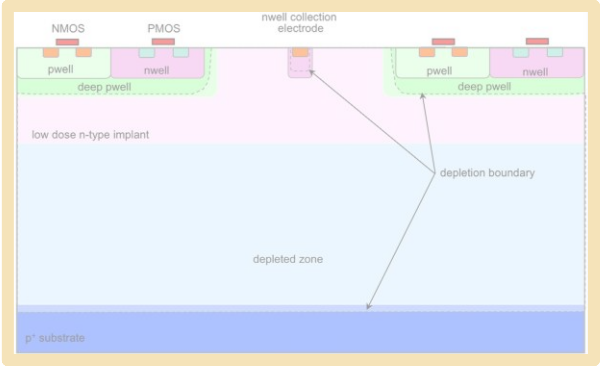
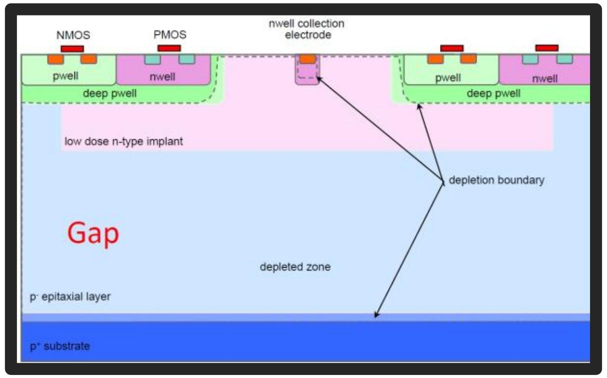
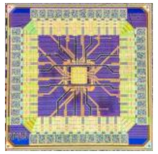




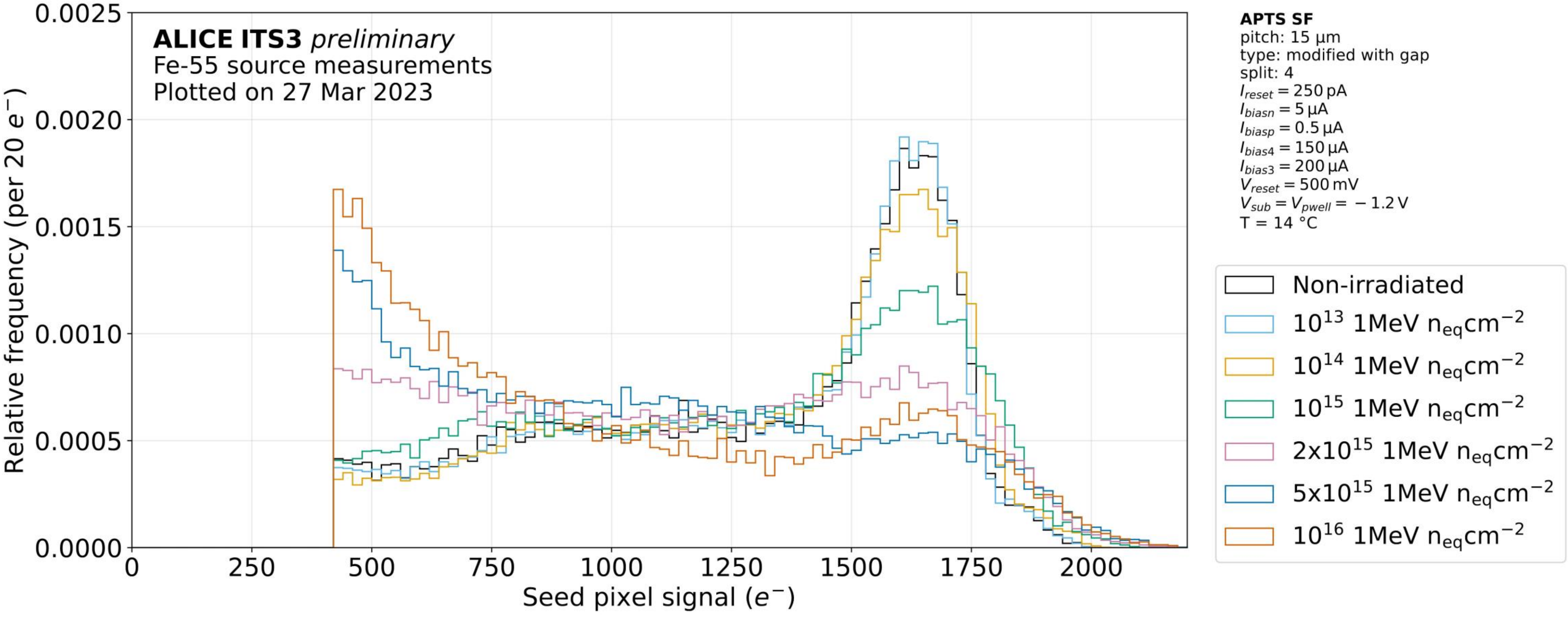


APTS SF: NIEL radiation hardness

- Non-Ionizing Energy Loss (NIEL) affects mainly the charge collection process
- ^{55}Fe source measurements at 14° C, pixel pitch 15µm

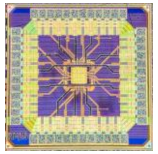


Analog
Pixel
Test
Structure

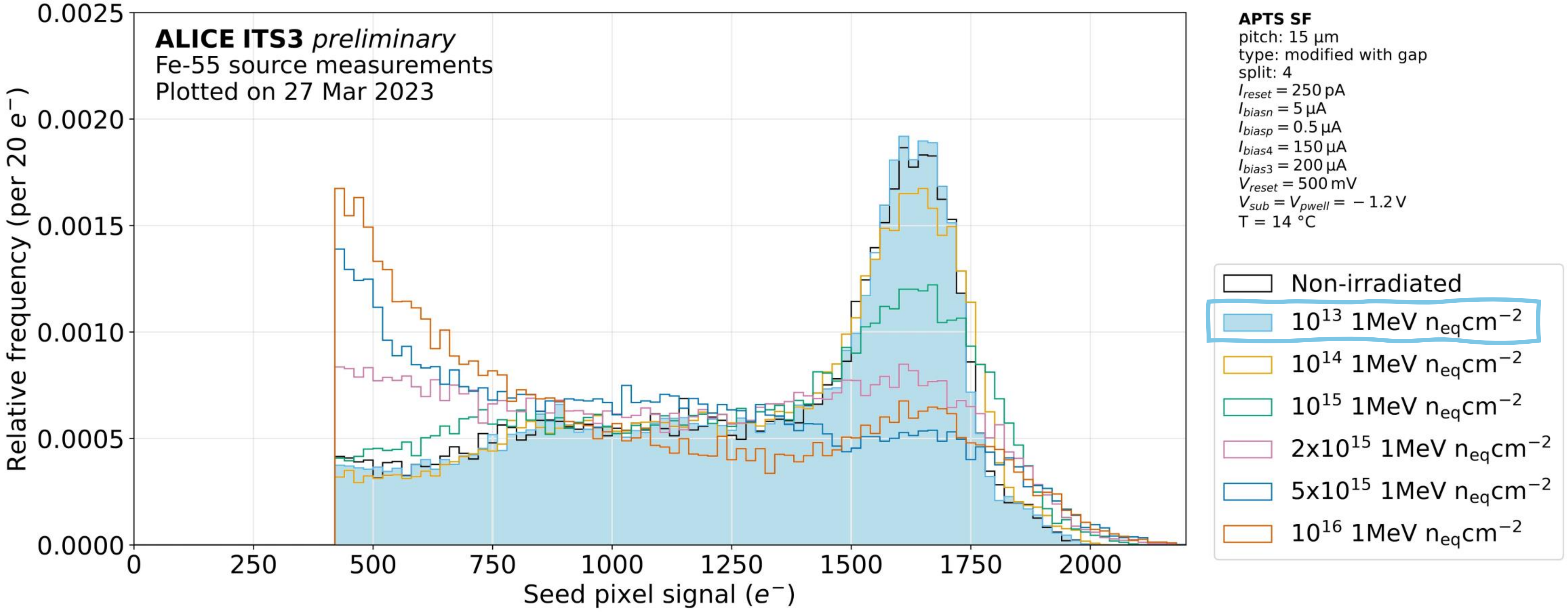


APTS SF: NIEL radiation hardness

- Non-Ionizing Energy Loss (NIEL) affects mainly the charge collection process
- ^{55}Fe source measurements at 14° C, pixel pitch 15µm
  - Beyond the requirements for ITS3

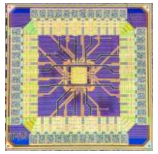


Analog **P**ixel **T**est **S**tructure

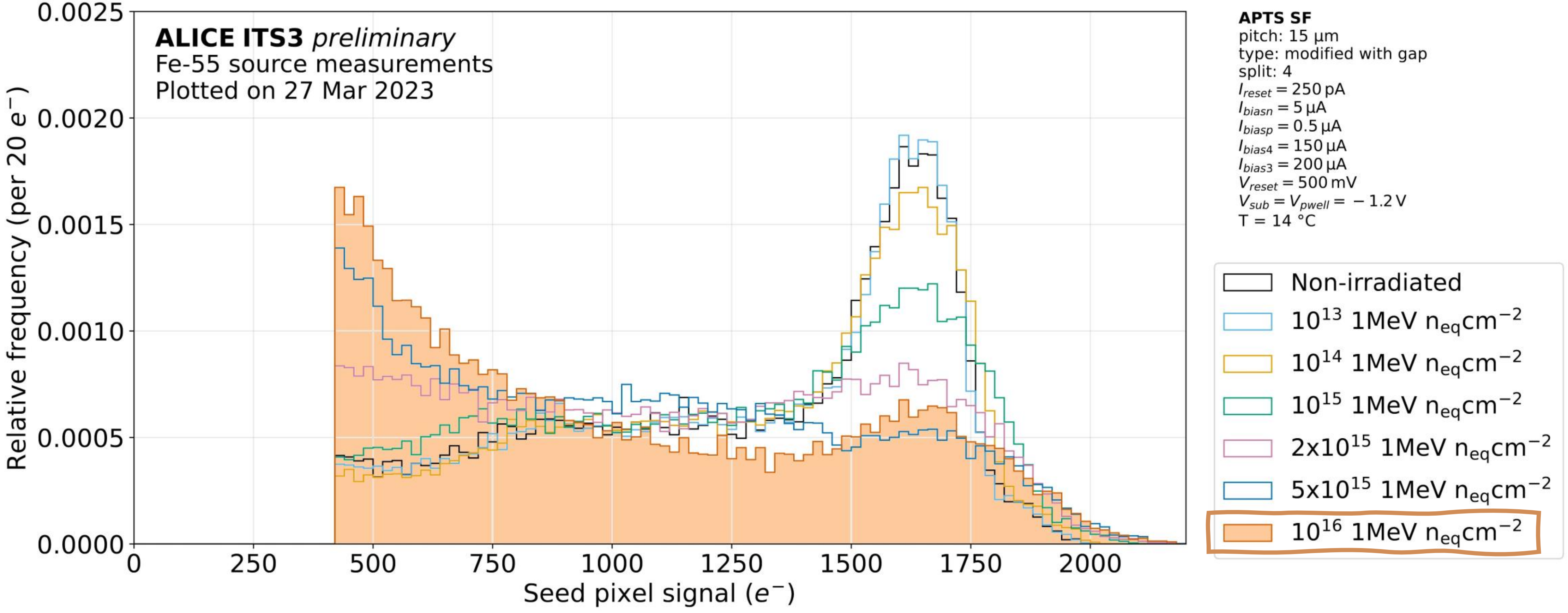


APTS SF: NIEL radiation hardness

- Non-Ionizing Energy Loss (NIEL) affects mainly the charge collection process
- ^{55}Fe source measurements at 14° C, pixel pitch 15µm
  - Beyond the requirements for ITS3, still operational after 10^{16} 1MeV $n_{eq}cm^{-2}$

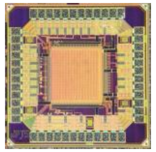


Analog **P**ixel **T**est **S**tructure

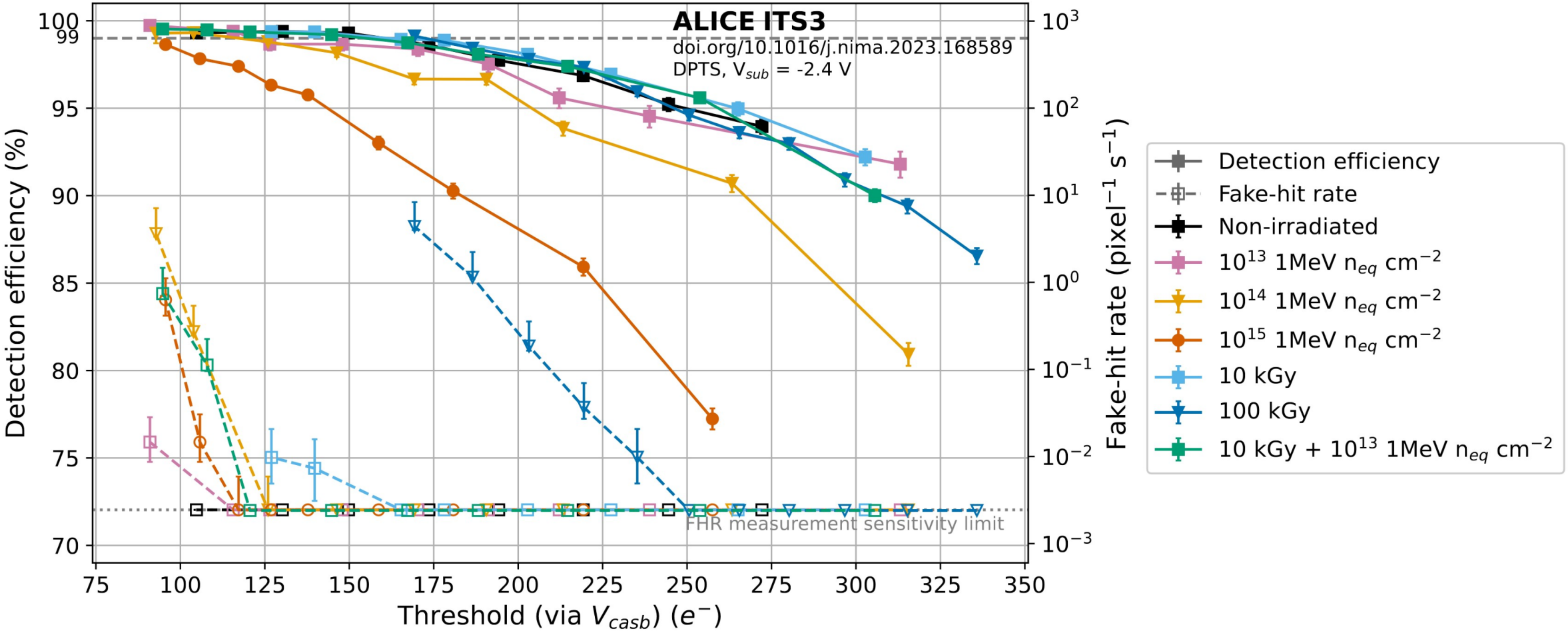


DPTS: NIEL and TID radiation hardness

- Non-Ionizing Energy Loss (NIEL) affects mainly the charge collection process
- Total Ionizing Dose (TID) radiation affects the in-pixel front-end → studied with DPTS

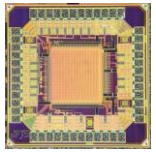


Digital **P**ixel **T**est **S**tructure

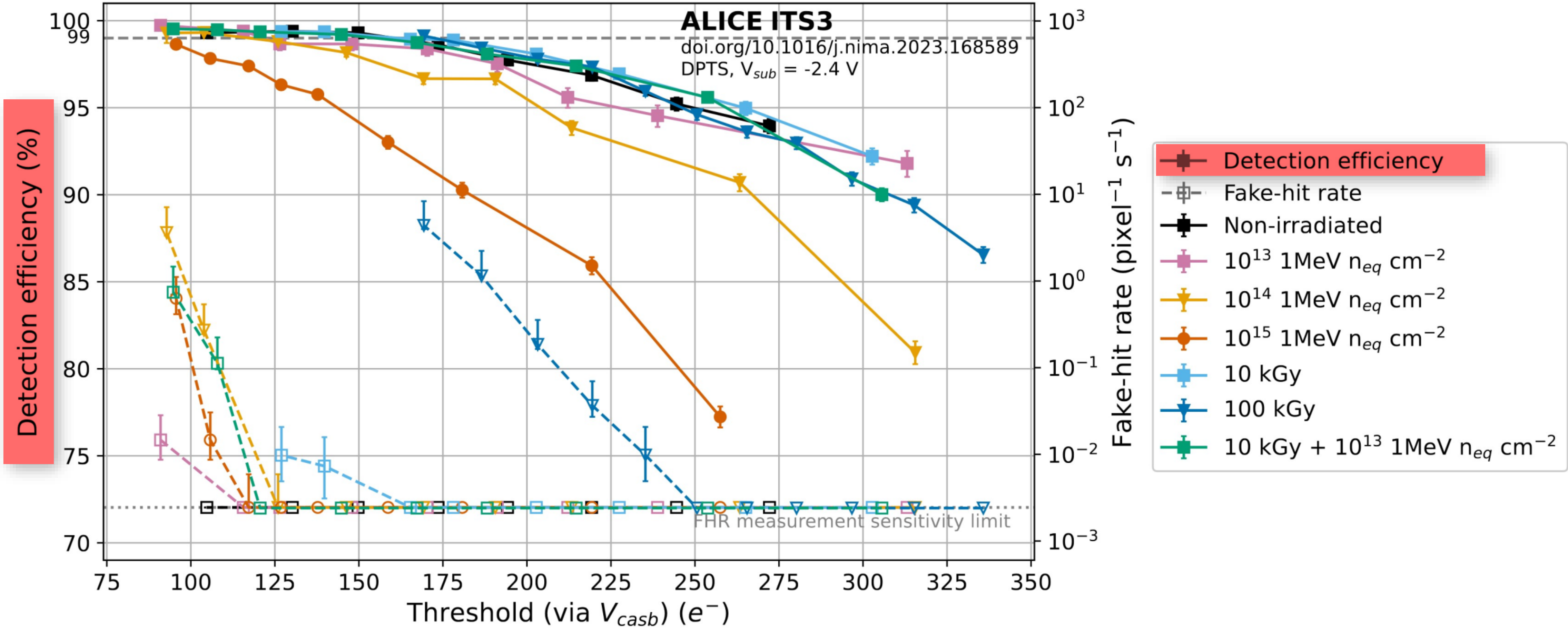


DPTS: NIEL and TID radiation hardness

- In-beam measurements: detection efficiency



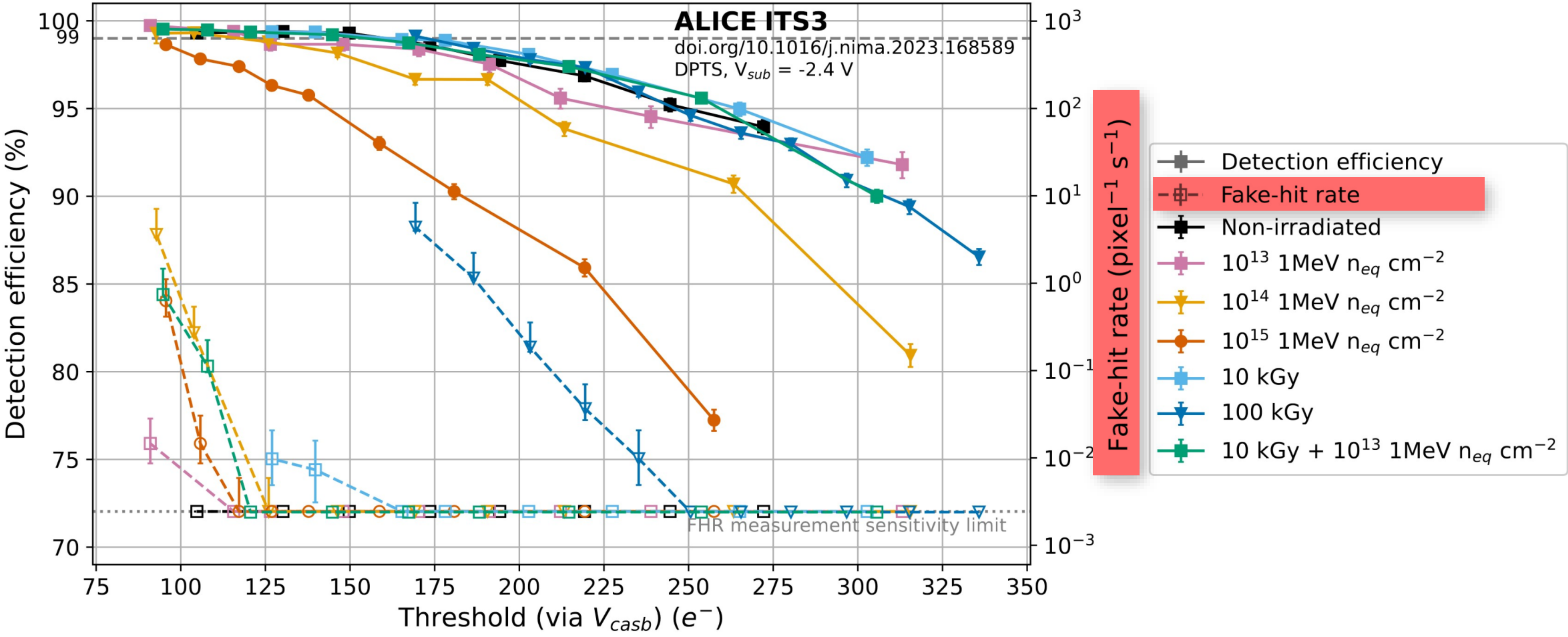
Digital
Pixel
Test
Structure



DPTS: NIEL and TID radiation hardness

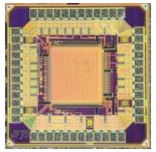
- In-beam measurements: detection efficiency
- Functional characterization: Fake Hit Rate (FHR)

Digital
Pixel
Test
Structure

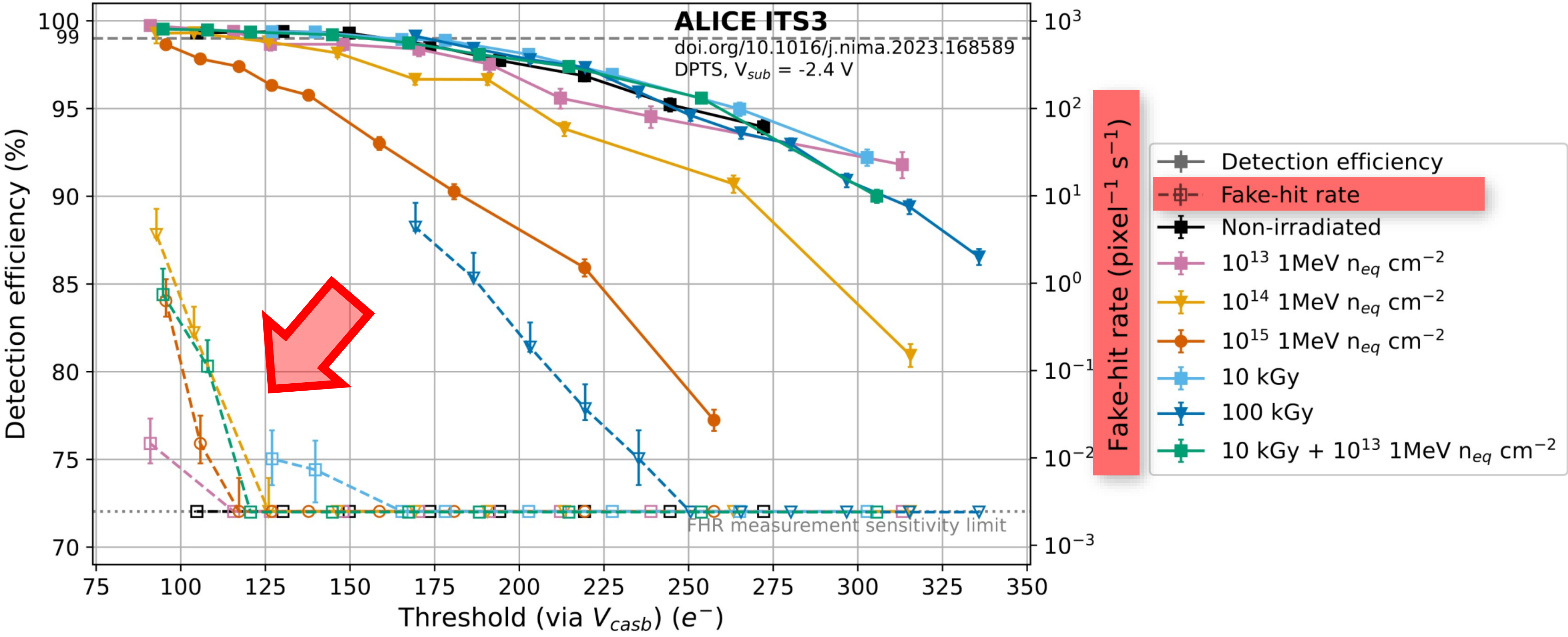


DPTS: NIEL and TID radiation hardness

- In-beam measurements: detection efficiency
- Functional characterization: Fake Hit Rate (FHR)



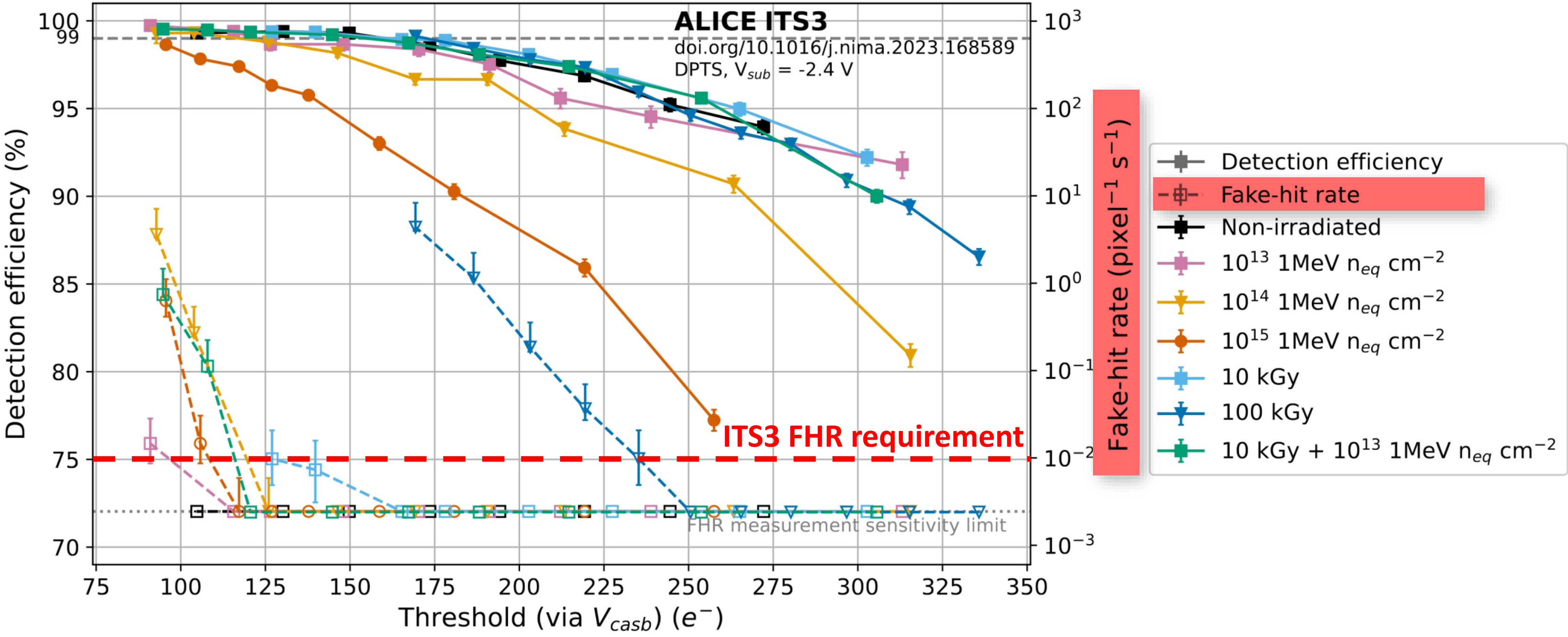
Digital
Pixel
Test
Structure



DPTS: NIEL and TID radiation hardness

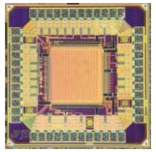
- In-beam measurements: detection efficiency
- Functional characterization: Fake Hit Rate (FHR)

Digital
Pixel
Test
Structure

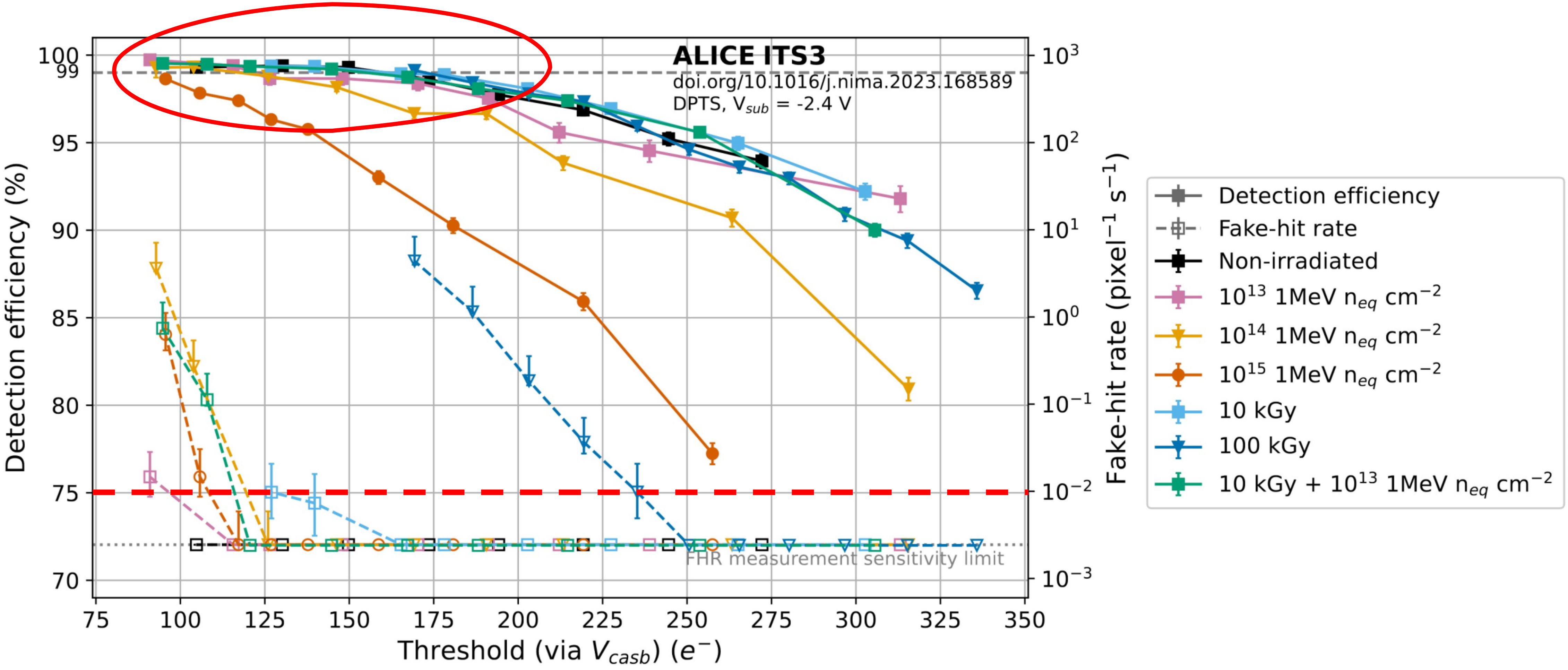


DPTS: NIEL and TID radiation hardness

- Efficiency higher than 99% in a wide range of thresholds

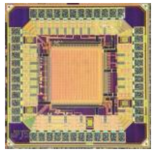


Digital
Pixel
Test
Structure

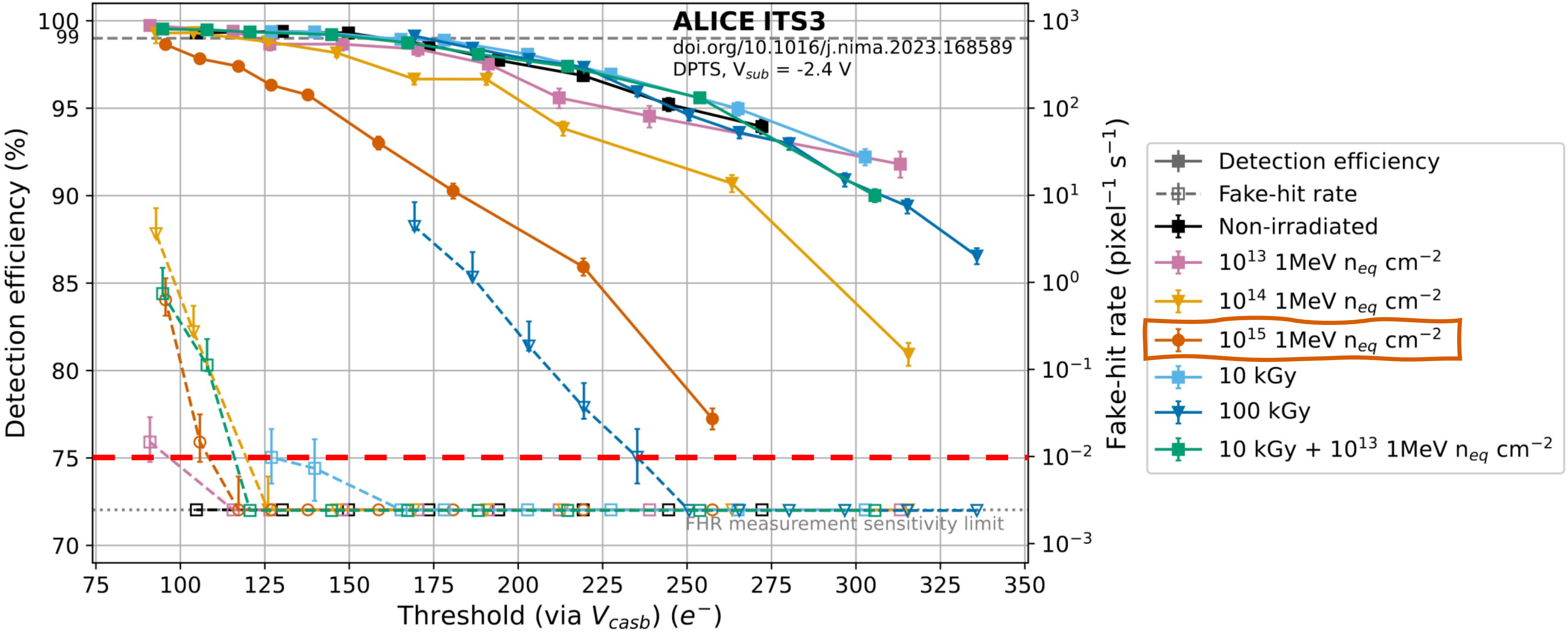


DPTS: NIEL and TID radiation hardness

- Efficiency higher than 99% in a wide range of thresholds
- Efficiency of 99% up to 10^{15} 1MeV $n_{eq}cm^{-2}$

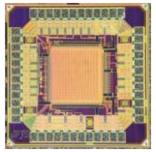


Digital
Pixel
Test
Structure

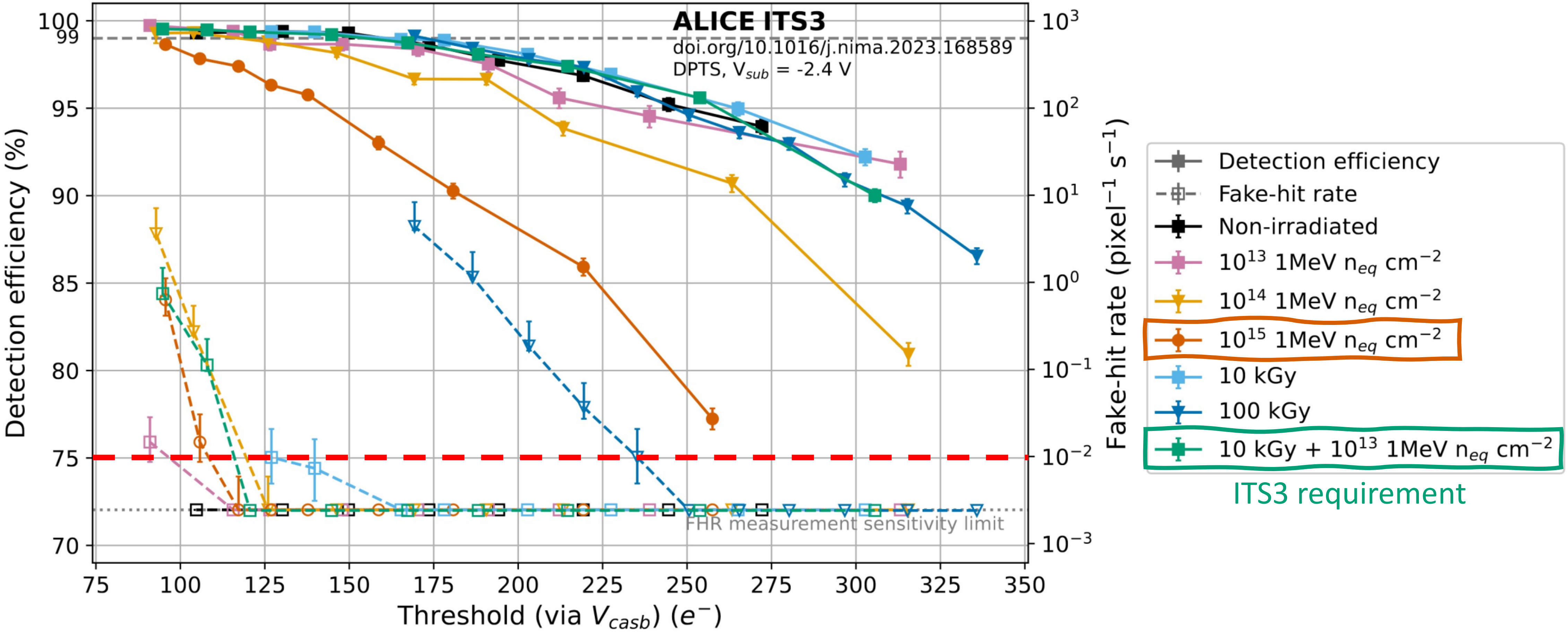


DPTS: NIEL and TID radiation hardness

- Efficiency higher than 99% in a wide range of thresholds
- Efficiency of 99% up to 10^{15} 1MeV $n_{eq}cm^{-2}$
- Efficiency of 99% at ITS3 radiation level

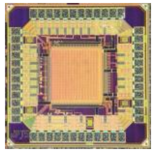


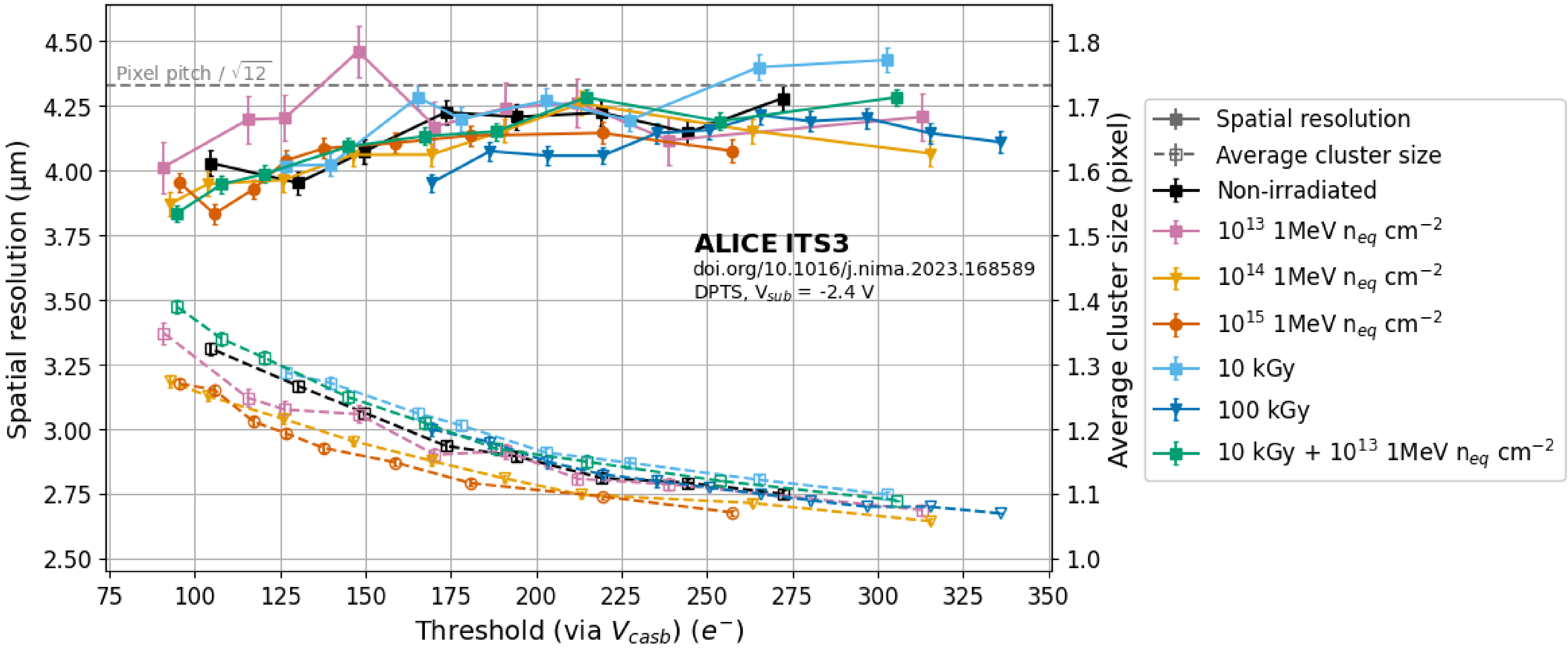
Digital
Pixel
Test
Structure



DPTS: spatial resolution

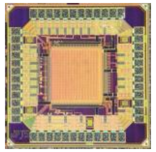
- In-beam measurements



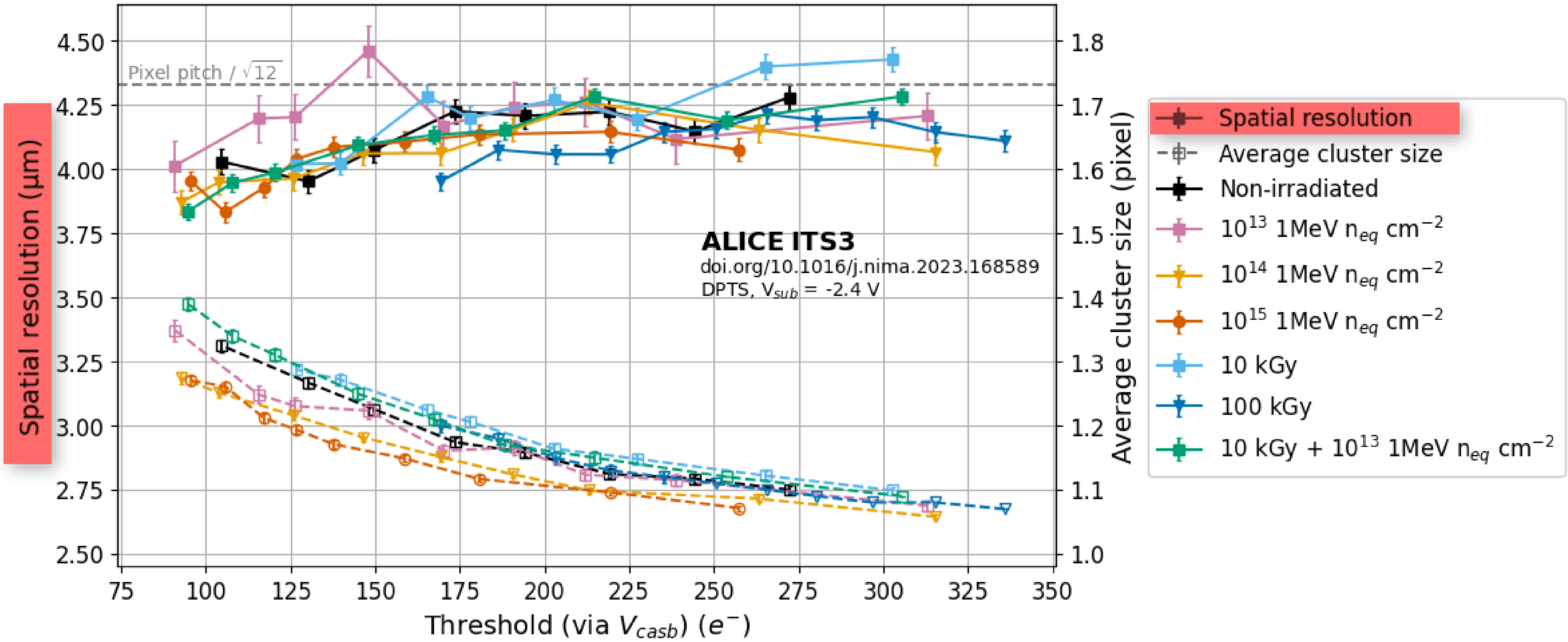


DPTS: spatial resolution

- In-beam measurements: spatial resolution



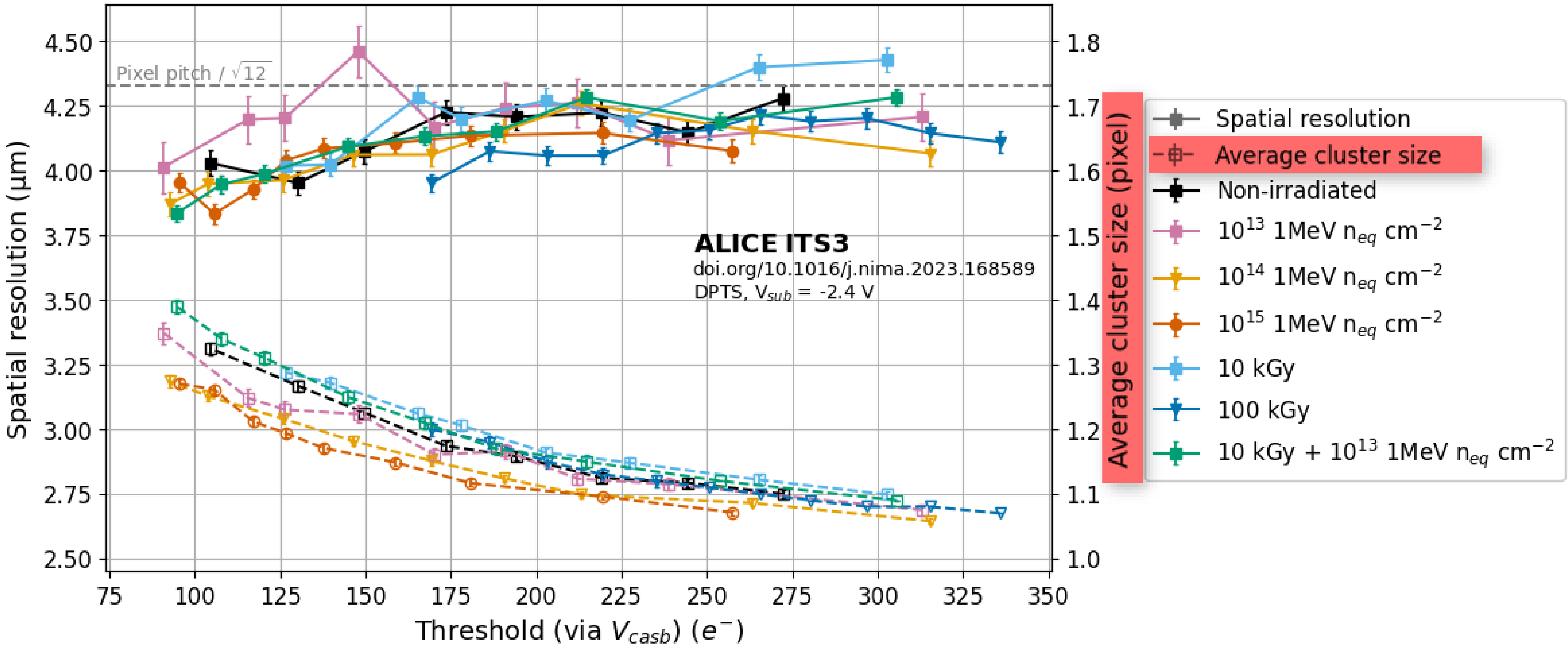
Digital
Pixel
Test
Structure



DPTS: spatial resolution

- In-beam measurements: spatial resolution and average cluster size

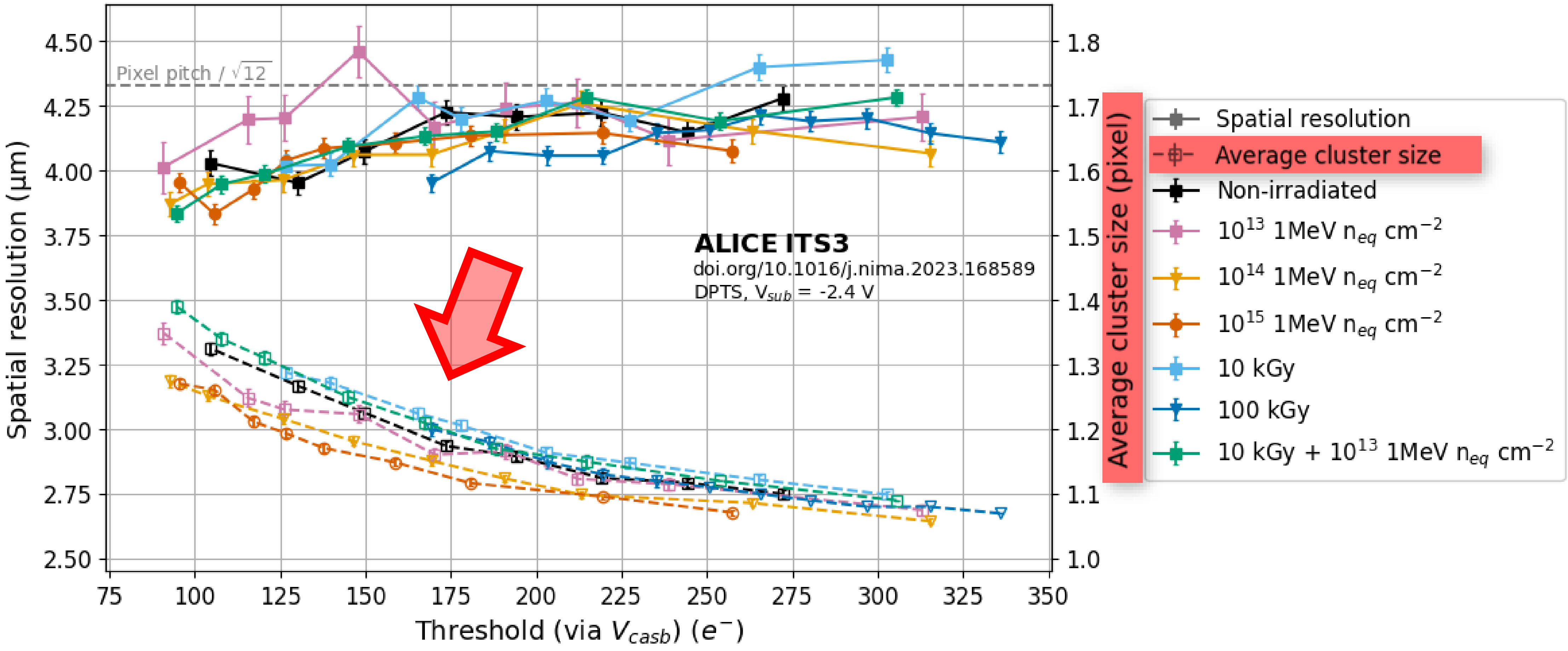
Digital
Pixel
Test
Structure



DPTS: spatial resolution

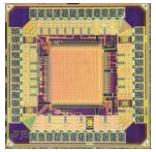
- In-beam measurements: spatial resolution and average cluster size

Digital
Pixel
Test
Structure

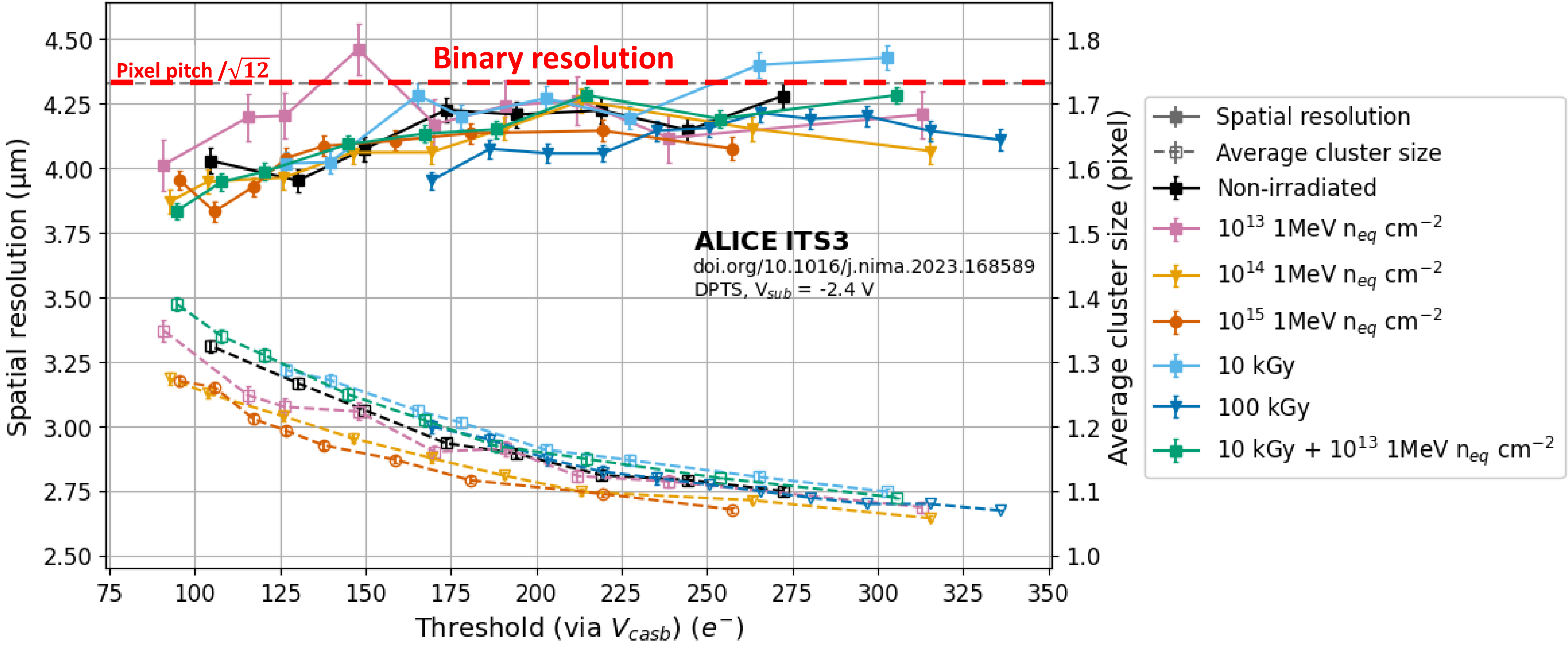


DPTS: spatial resolution

- In-beam measurements: spatial resolution and average cluster size
  - Spatial resolution better than the binary resolution

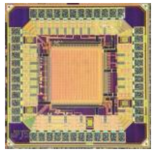


Digital **P**ixel **T**est **S**tructure

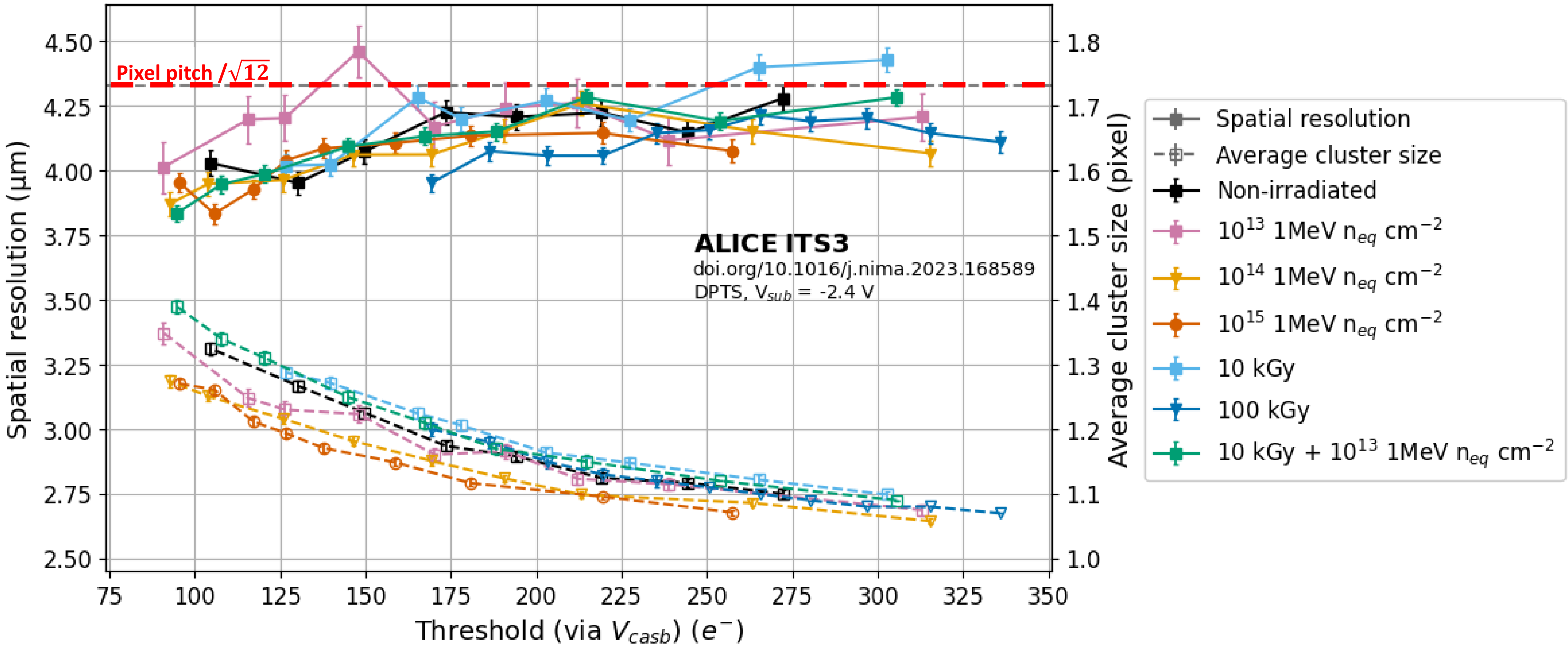


DPTS: spatial resolution

- In-beam measurements: spatial resolution and average cluster size
  - Spatial resolution better than the binary resolution
  - Not affected by the irradiation

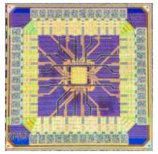


Digital
Pixel
Test
Structure

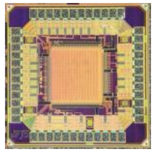


MIP energy loss

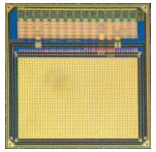
- Compatibility of MIP energy loss measurements between different MLR1 test structures (APTS SF, DPTS, CE65)



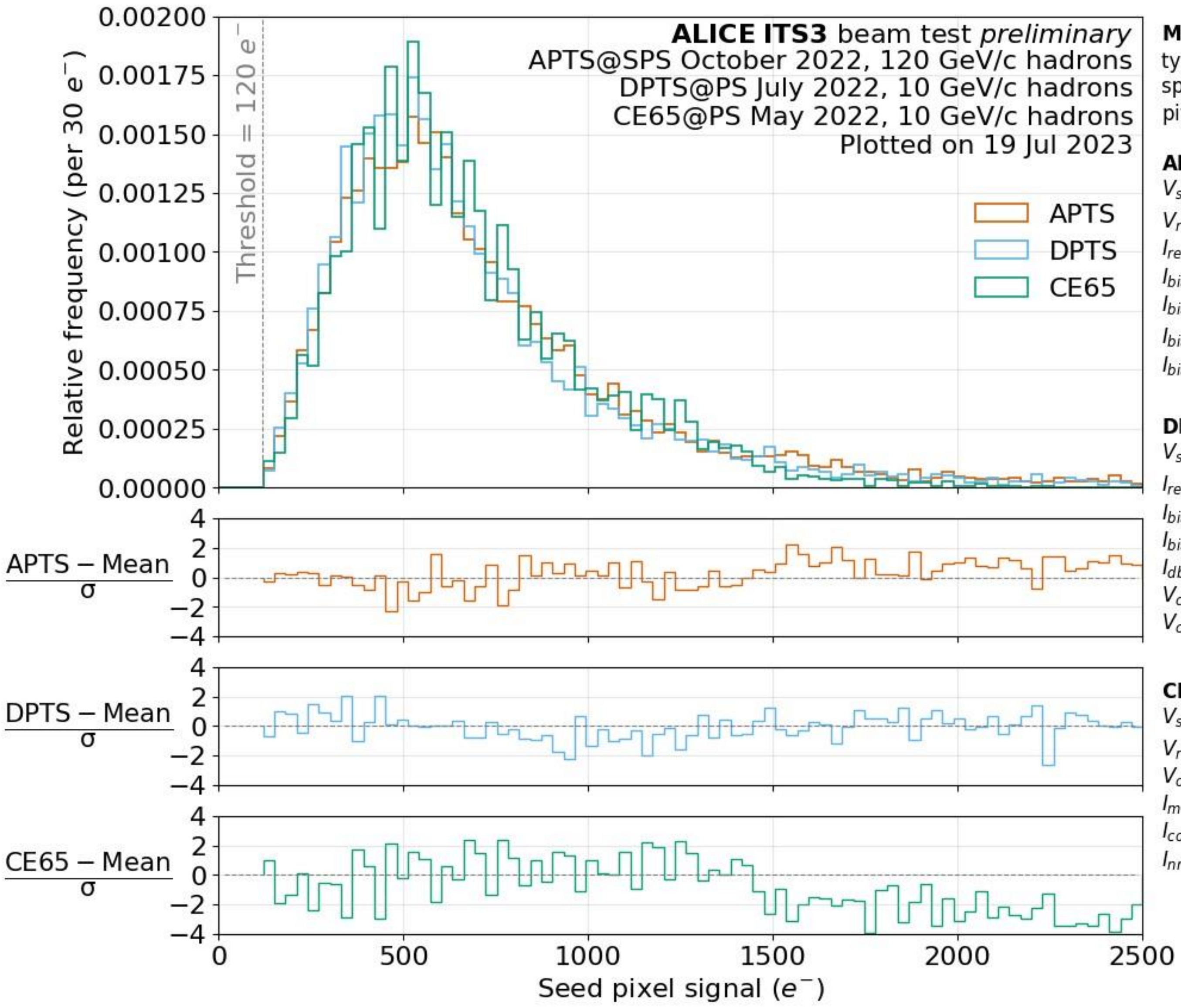
Analog **P**ixel **T**est **S**tructure



Digital **P**ixel **T**est **S**tructure



Circuit **E**xploratoire **65**



MLR1 comparison
type: modified with gap
split: 4
pitch: 15 µm

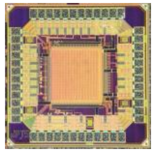
APTS SF
$V_{sub} = V_{pwell} = -2.4\,V$
$V_{reset} = 500\,mV$
$I_{reset} = 100\,pA$
$I_{biasn} = 5\,\mu A$
$I_{biasp} = 0.5\,\mu A$
$I_{bias4} = 150\,\mu A$
$I_{bias3} = 200\,\mu A$

DPTS
$V_{sub} = V_{pwell} = -2.4\,V$
$I_{reset} = 35\,pA$
$I_{bias} = 100\,nA$
$I_{biasn} = 10\,nA$
$I_{db} = 50\,nA$
$V_{casn} = 350\,mV$
$V_{casb} = 500\,mV$

CE65 SF
$V_{sub} = V_{pwell} = 0\,V$
$V_{reset} = 3.3\,V$
$V_{offset} = 0.4\,V$
$I_{mat} = 5\,mA$
$I_{col} = 100\,\mu A$
$I_{nmos} = 1\,\mu A$

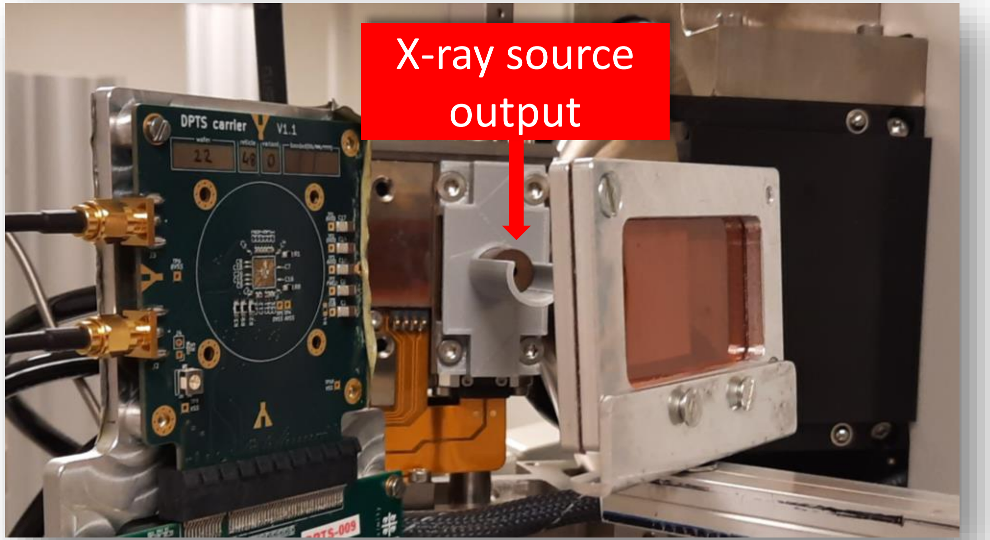
DPTS: X-ray fluorescence

- Fluorescence photons from Sn target



Digital
Pixel
Test
Structure

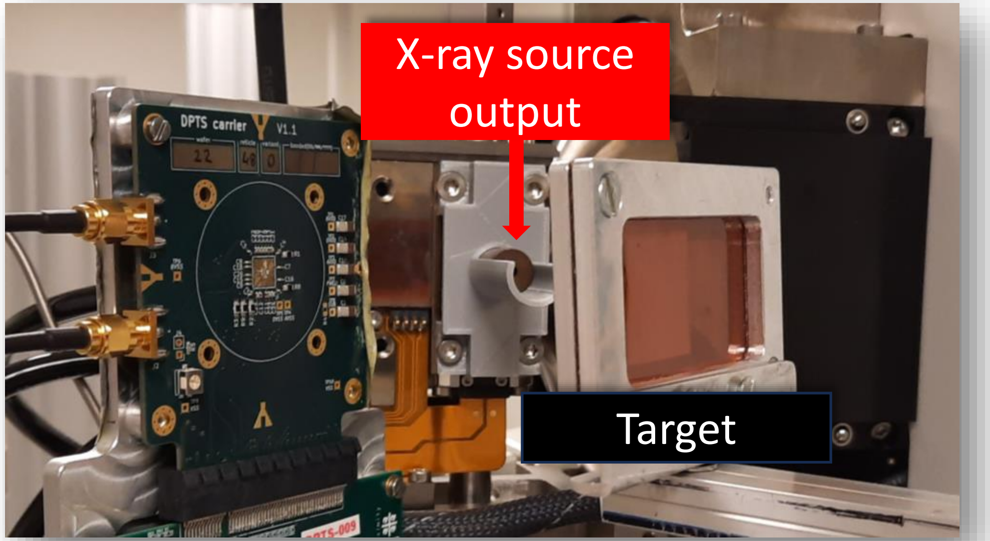
X-ray beam



DPTS: X-ray fluorescence

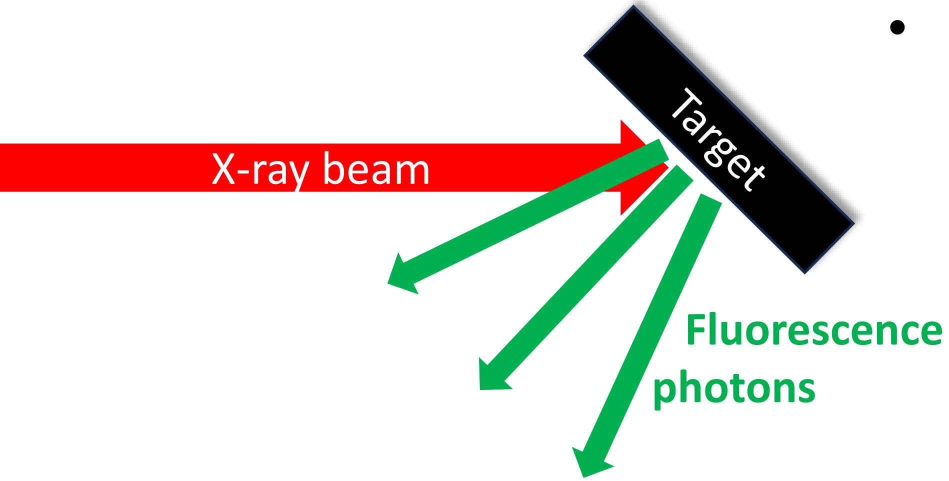
- Fluorescence photons from Sn target

Digital
Pixel
Test
Structure

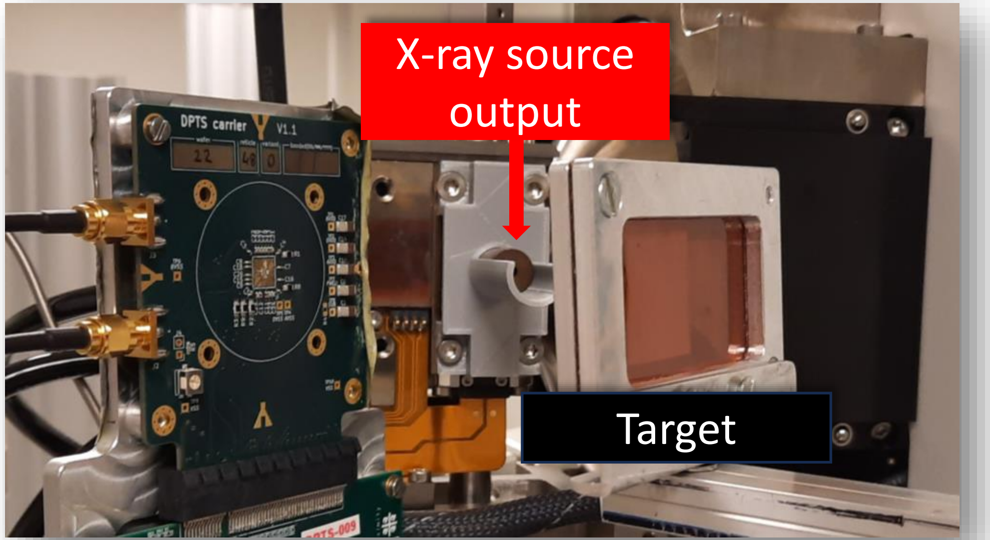


DPTS: X-ray fluorescence

- Fluorescence photons from Sn target

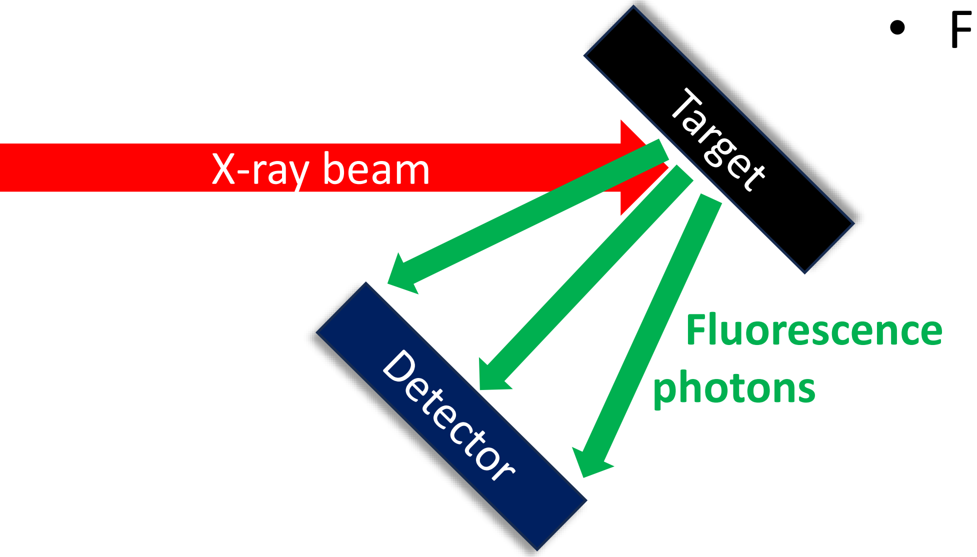


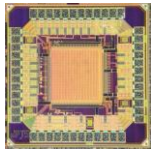
Digital
Pixel
Test
Structure

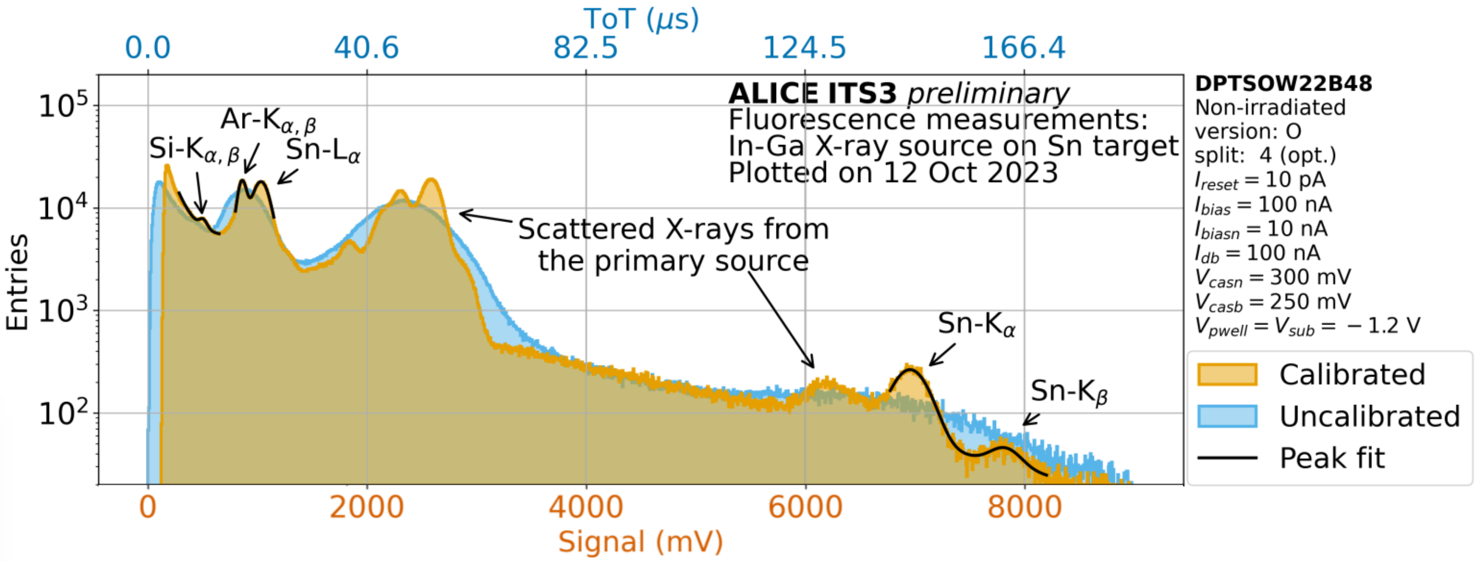


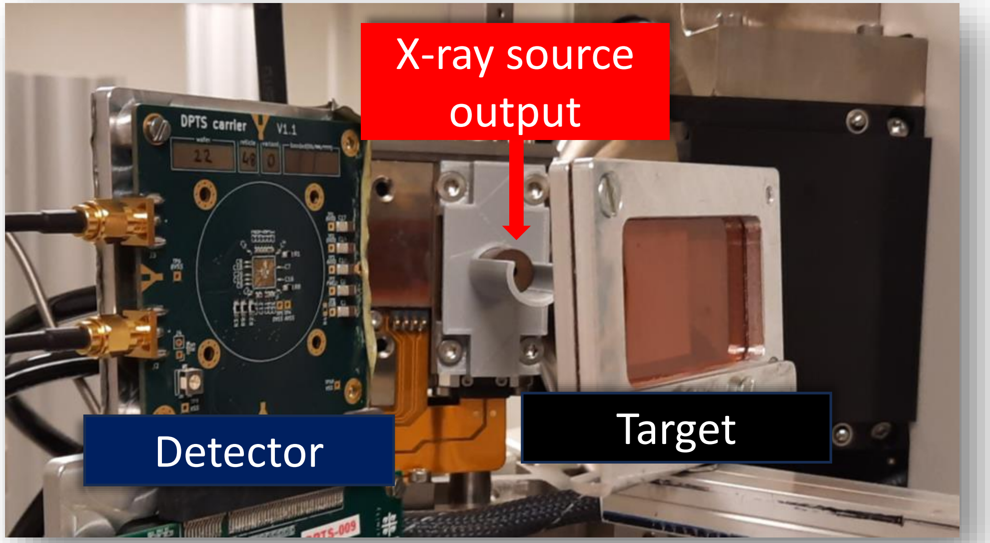
DPTS: X-ray fluorescence

- Fluorescence photons from Sn target

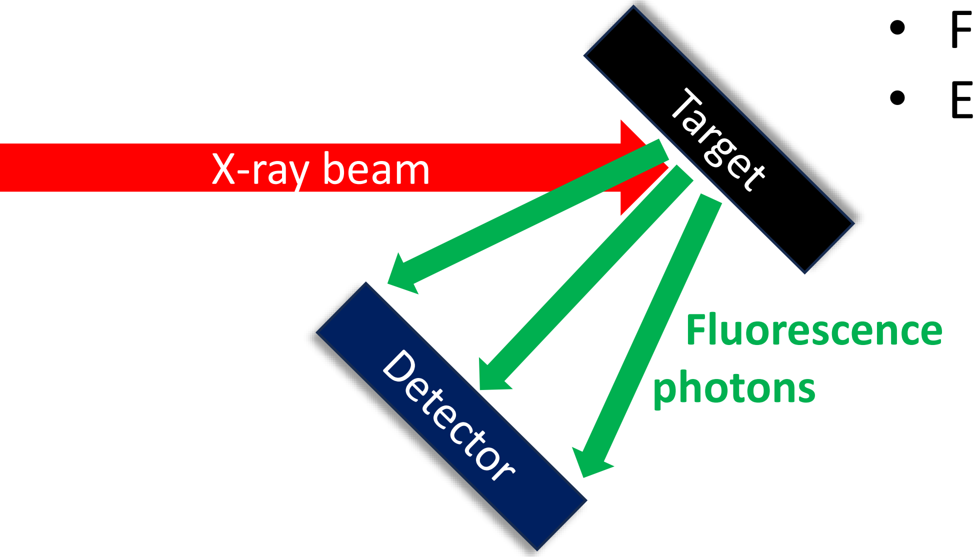




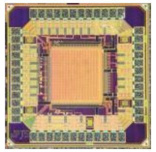




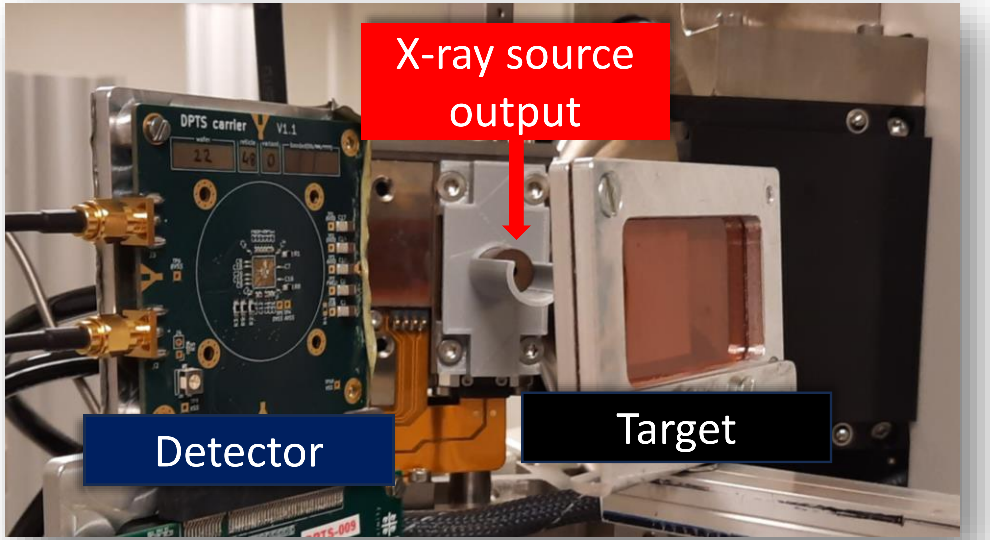
DPTS: X-ray fluorescence

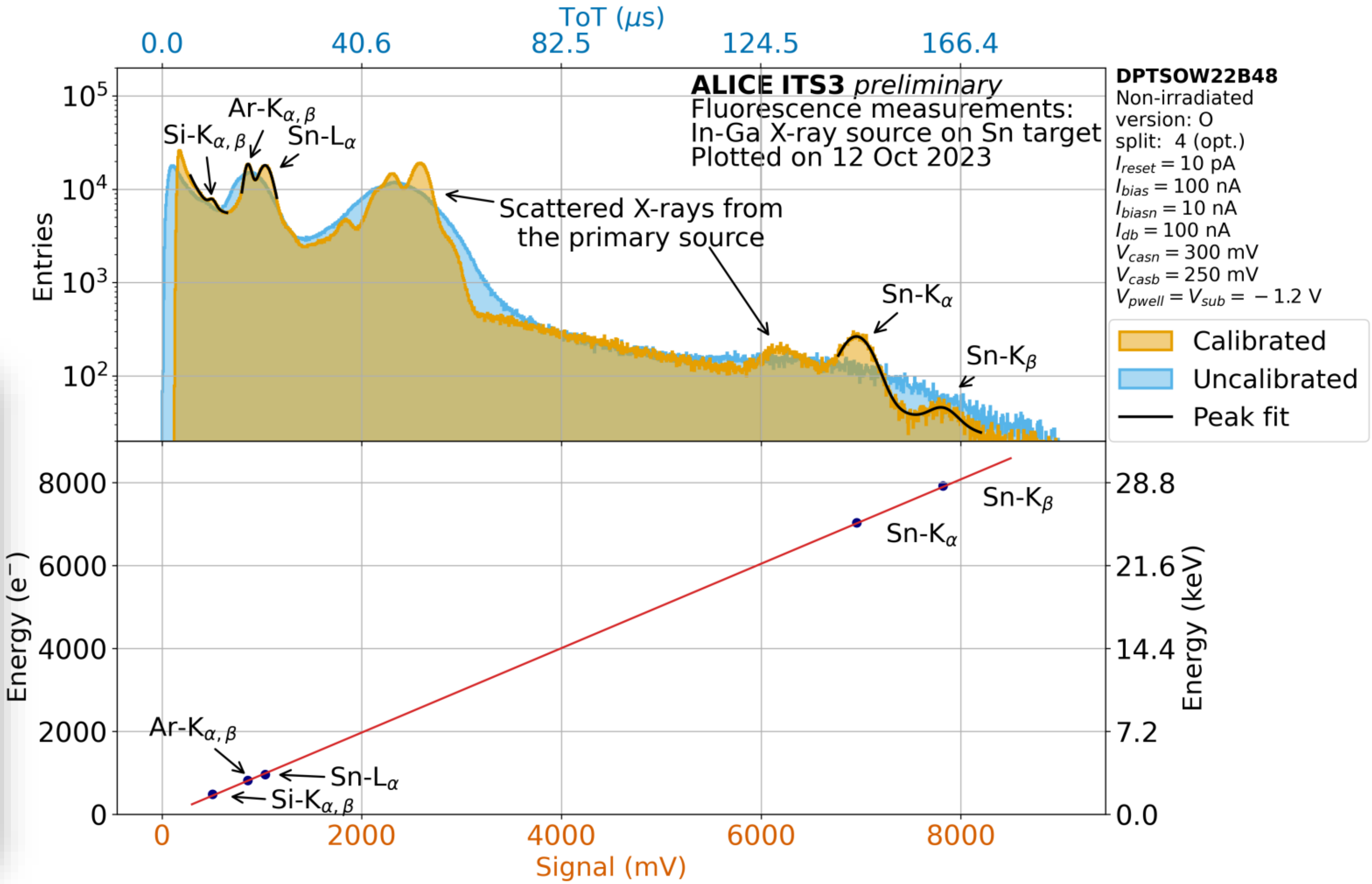


- Fluorescence photons from Sn target
- Energy calibration of the response



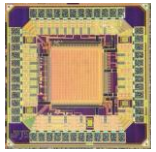
Digital
Pixel
Test
Structure



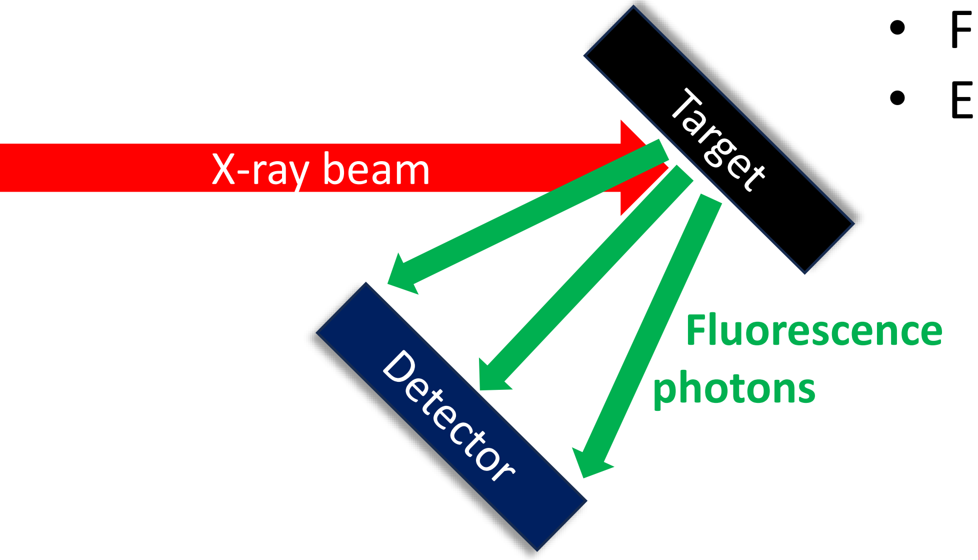


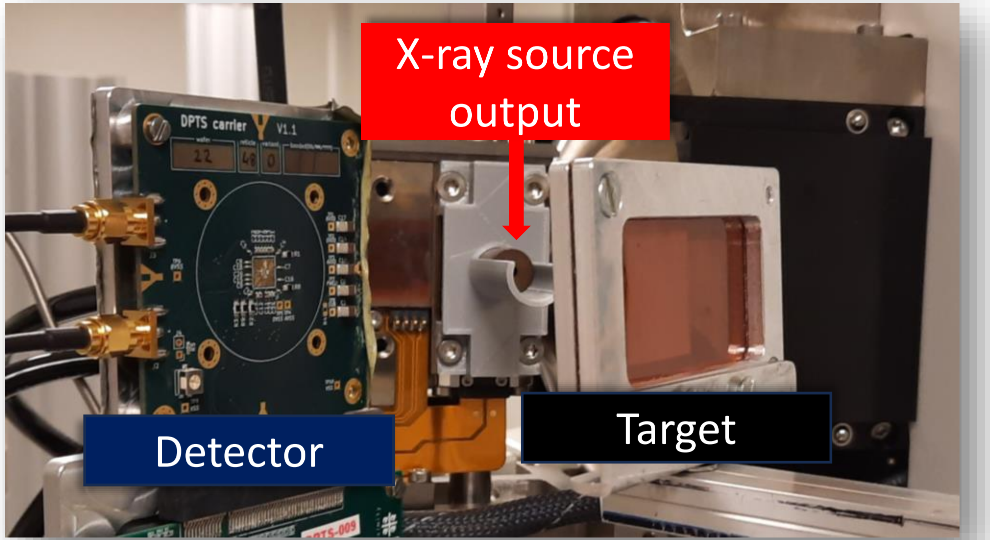
DPTS: X-ray fluorescence

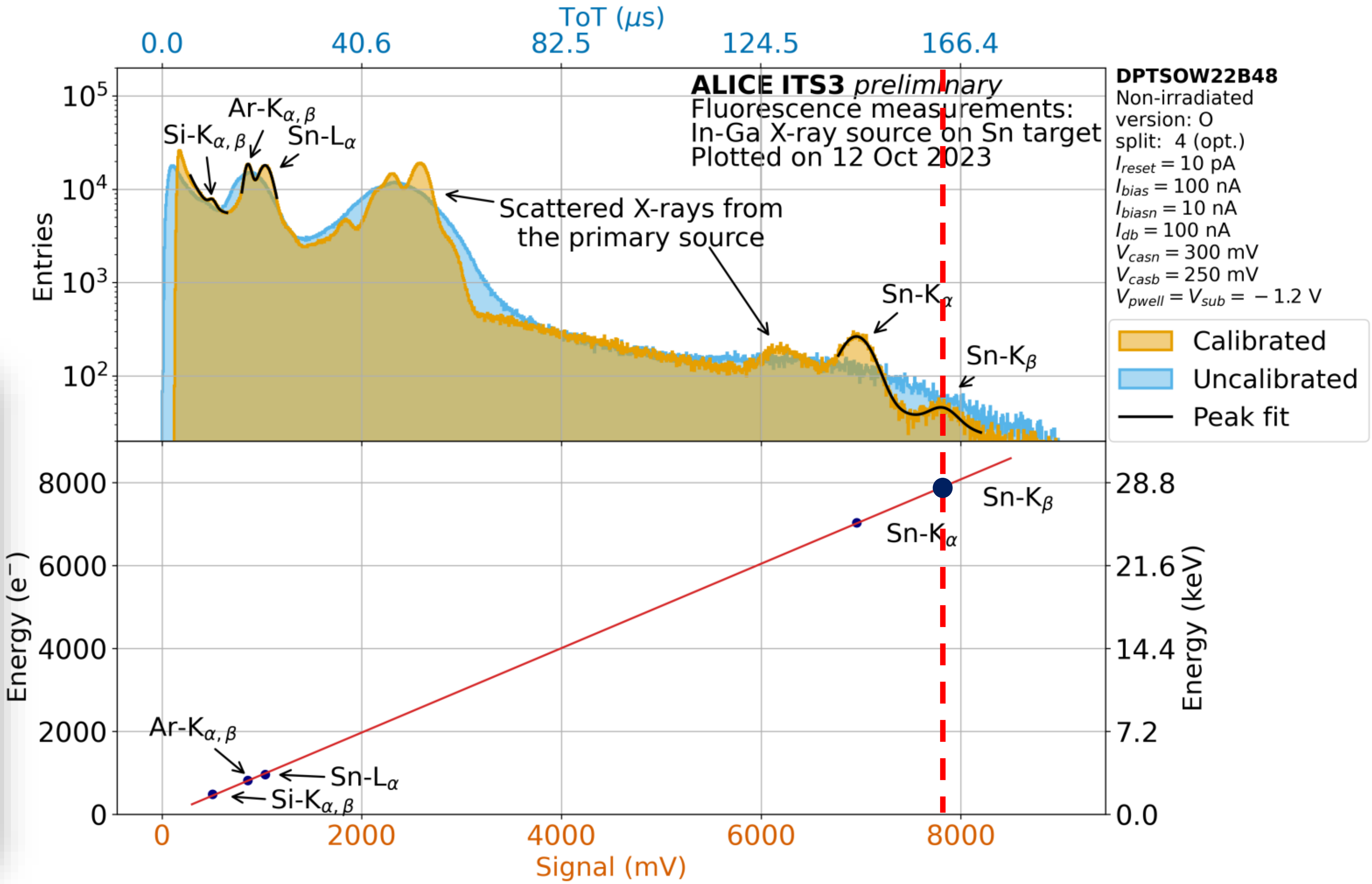
- Fluorescence photons from Sn target
- Energy calibration of the response up to 28.8 keV



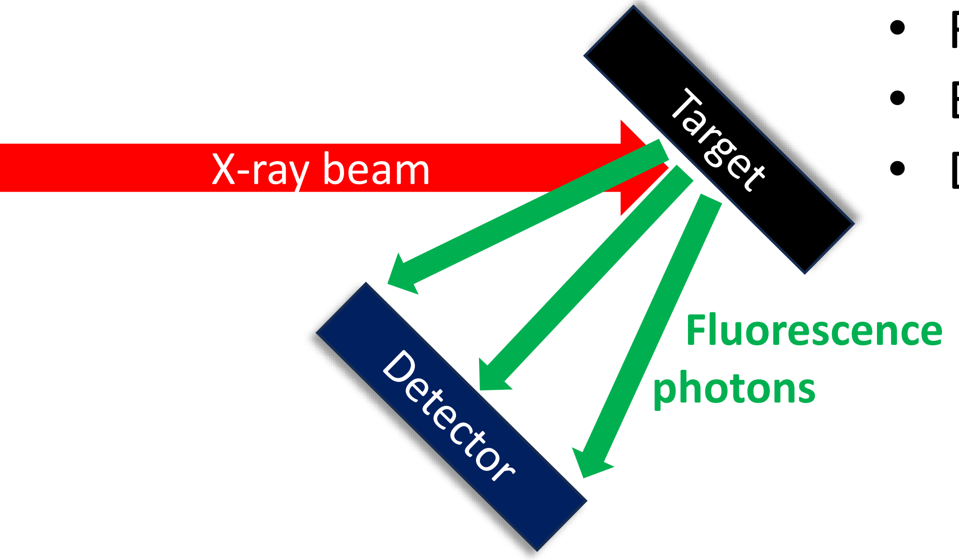
Digital
Pixel
Test
Structure





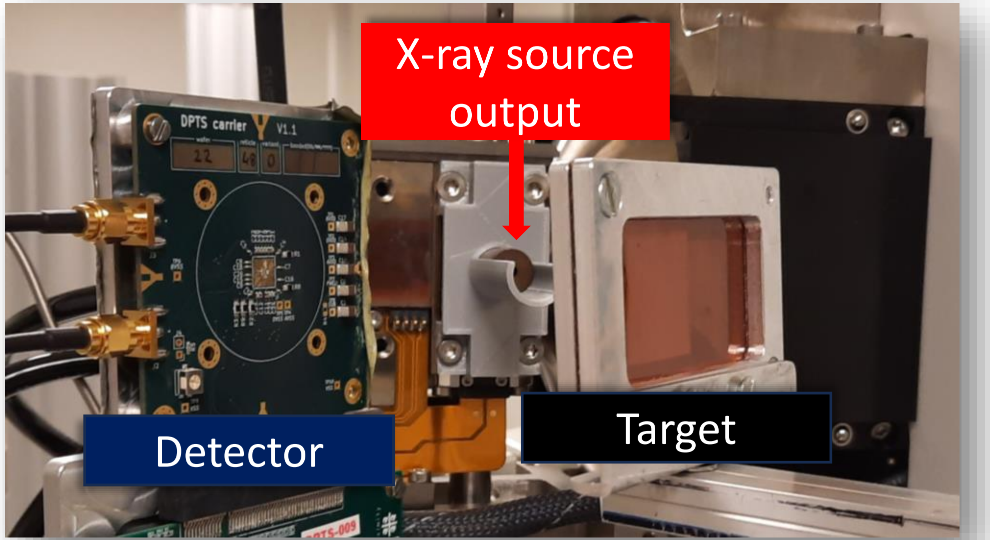


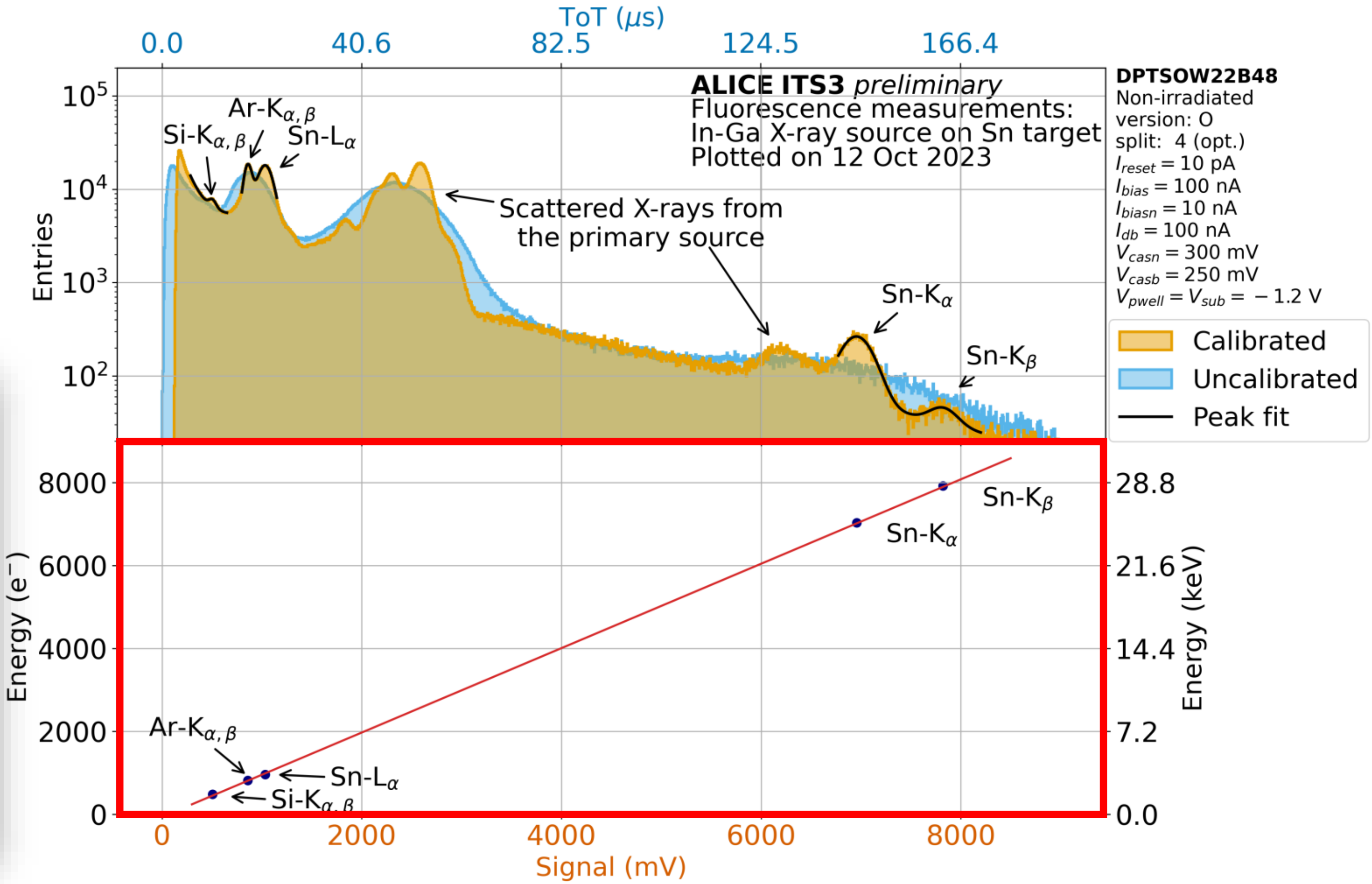
DPTS: X-ray fluorescence



- Fluorescence photons from Sn target
- Energy calibration of the response up to 28.8 keV
- Demonstrated linearity of the response

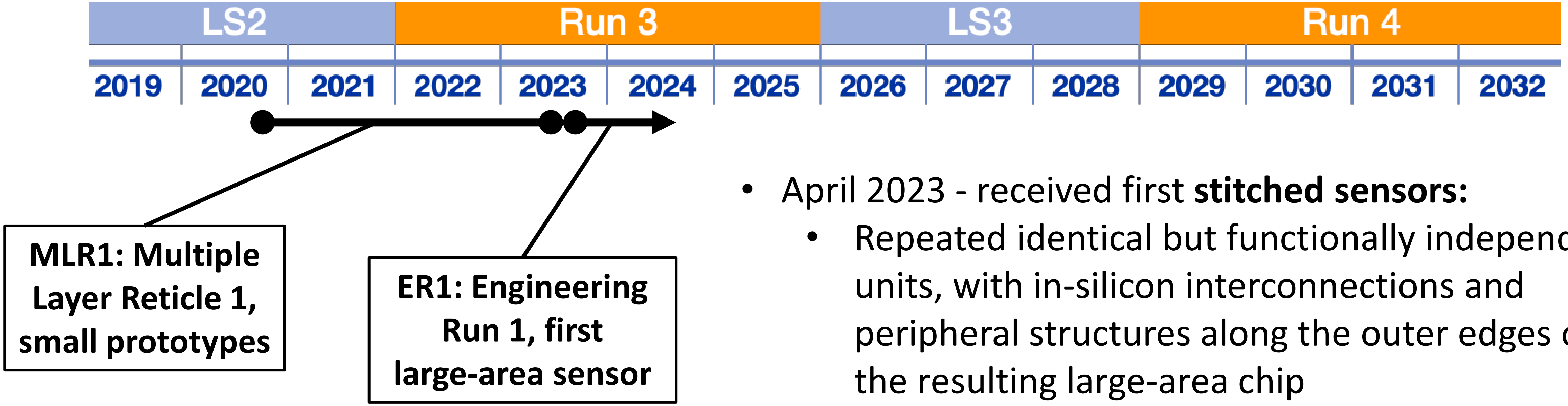
Digital **P**ixel **T**est **S**tructure



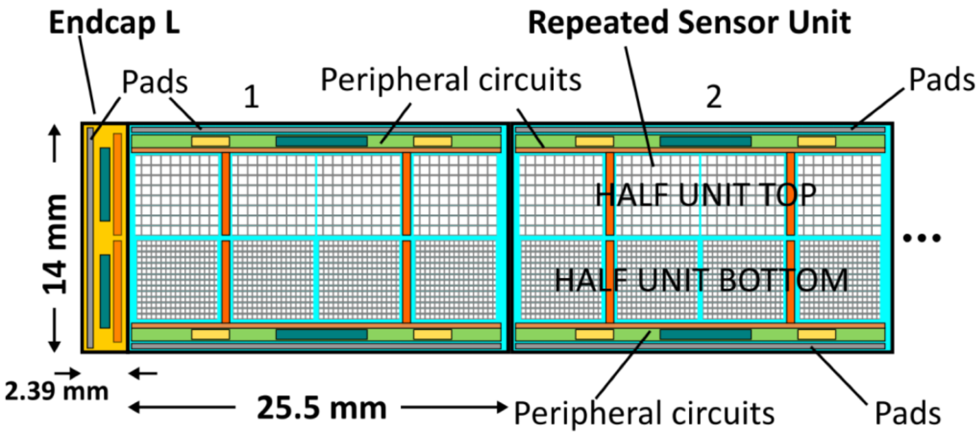


Large-area MAPS

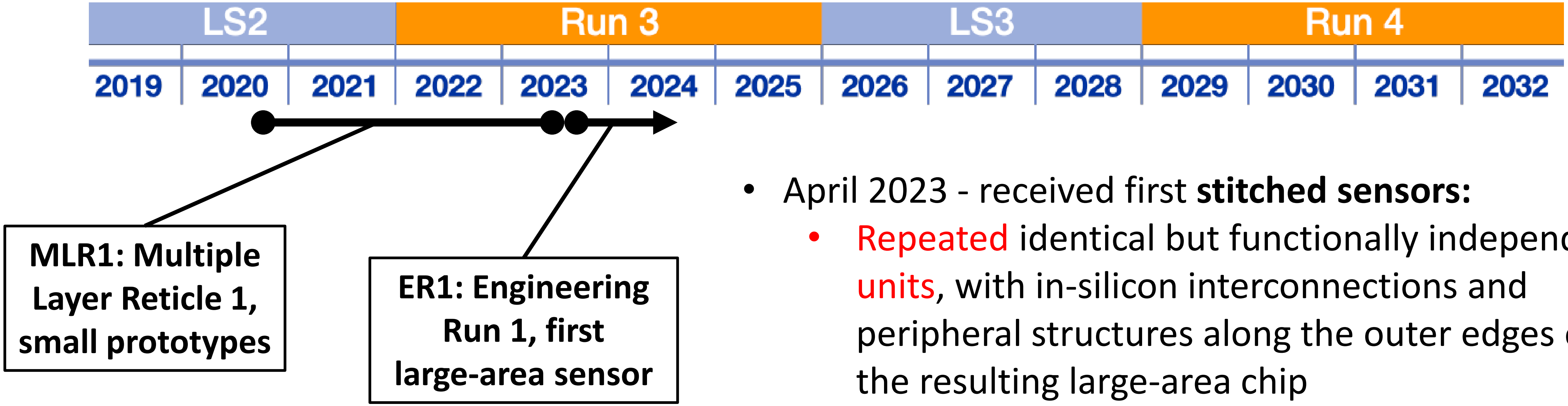
Large-area MAPS: stitching



- April 2023 - received first **stitched sensors:**
  - Repeated identical but functionally independent units, with in-silicon interconnections and peripheral structures along the outer edges of the resulting large-area chip



Large-area MAPS: stitching



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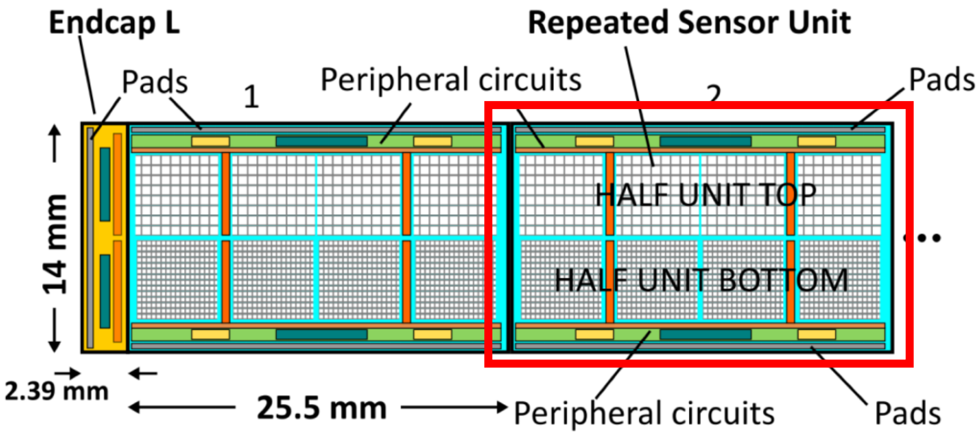
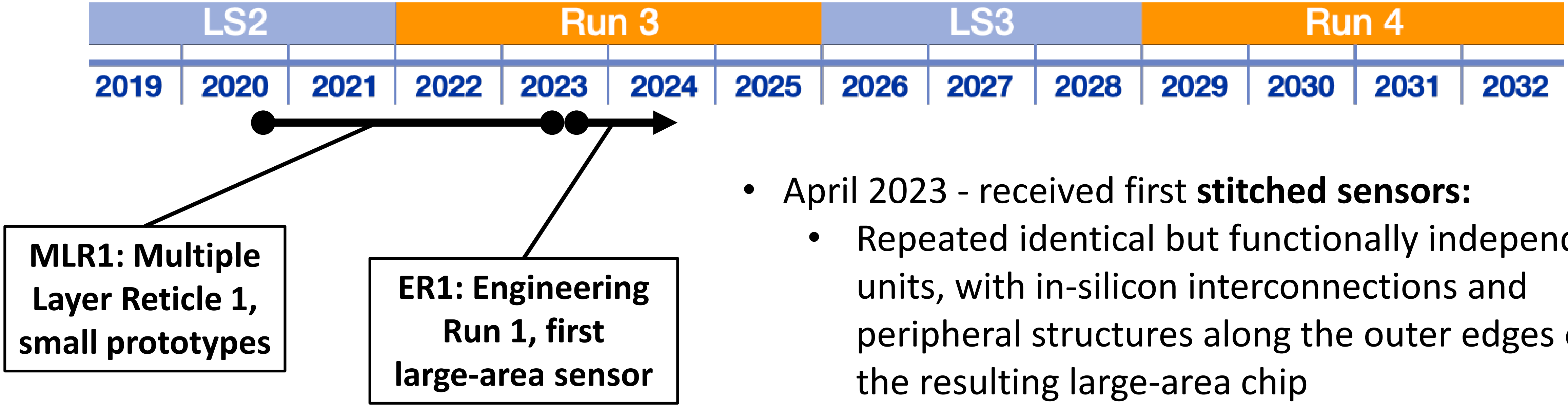
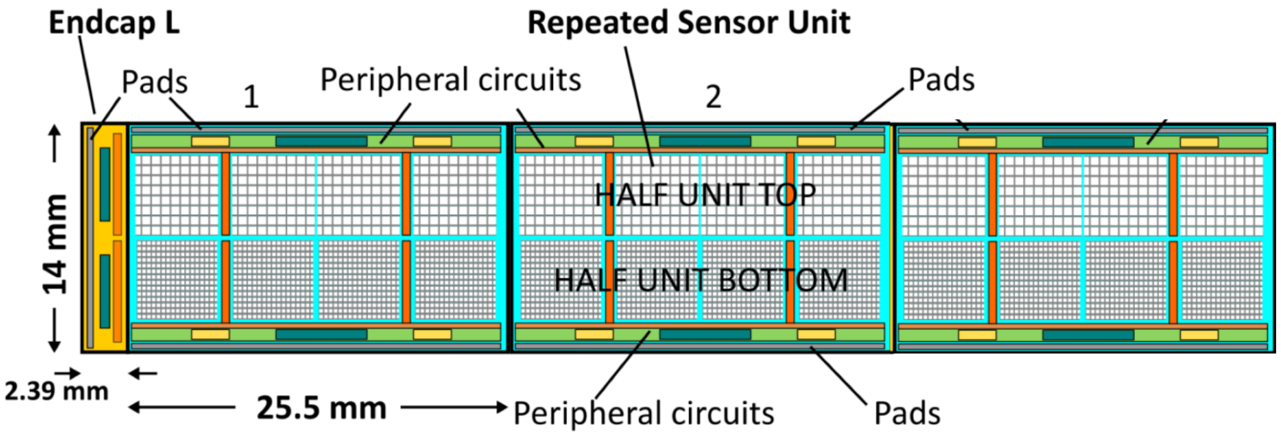


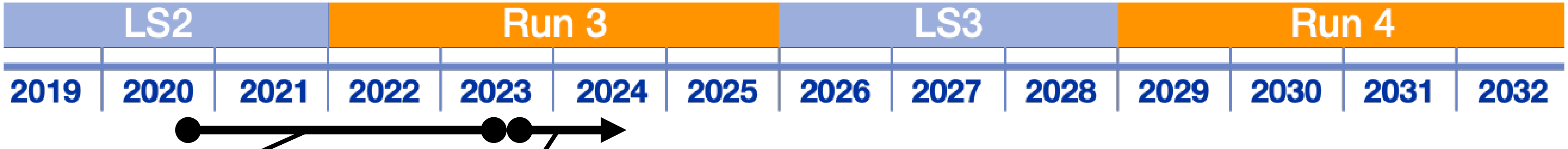
Large-area MAPS: stitching

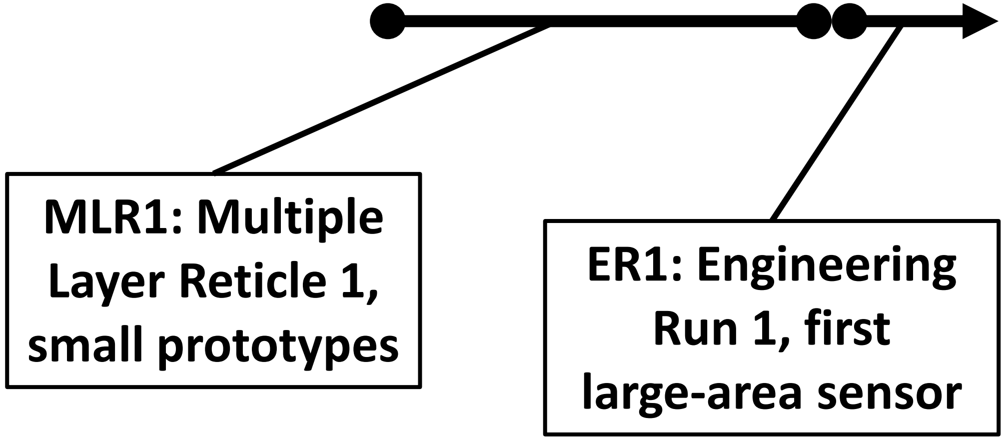


- April 2023 - received first **stitched sensors:**
  - Repeated identical but functionally independent units, with in-silicon interconnections and peripheral structures along the outer edges of the resulting large-area chip

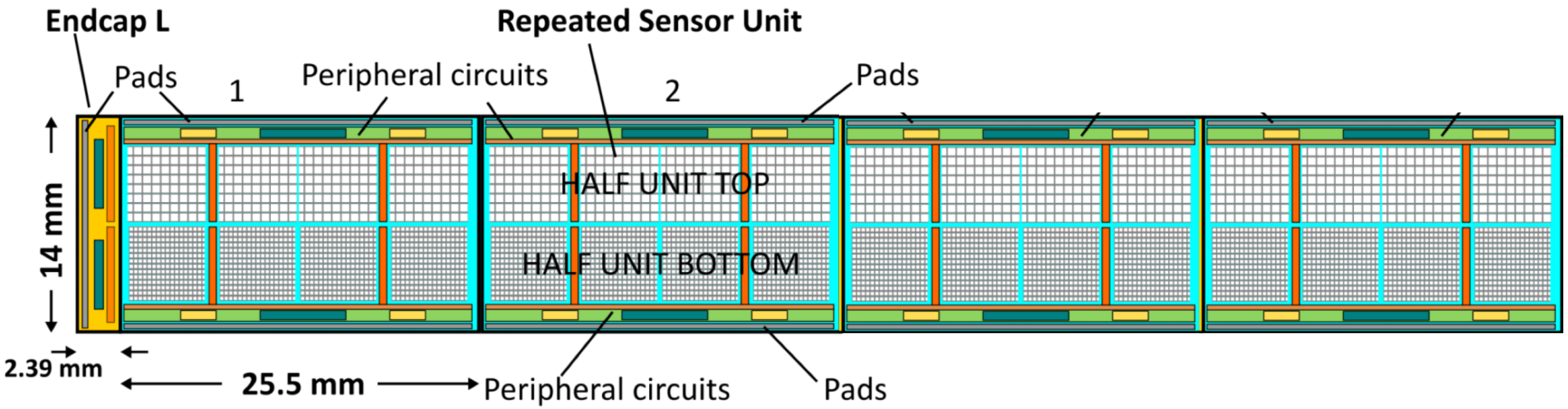


Large-area MAPS: stitching





- April 2023 - received first **stitched sensors:**
  - Repeated identical but functionally independent units, with in-silicon interconnections and peripheral structures along the outer edges of the resulting large-area chip



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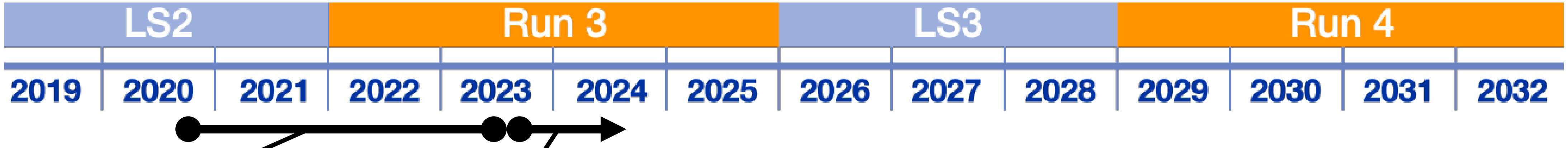

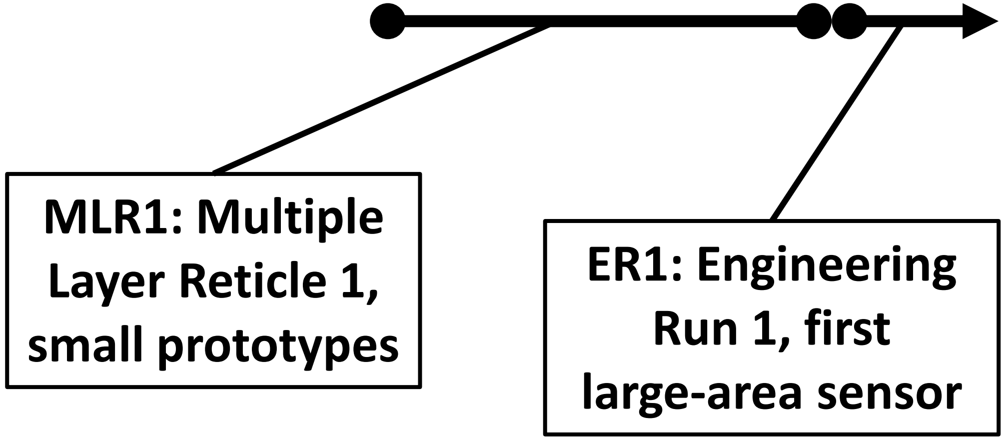

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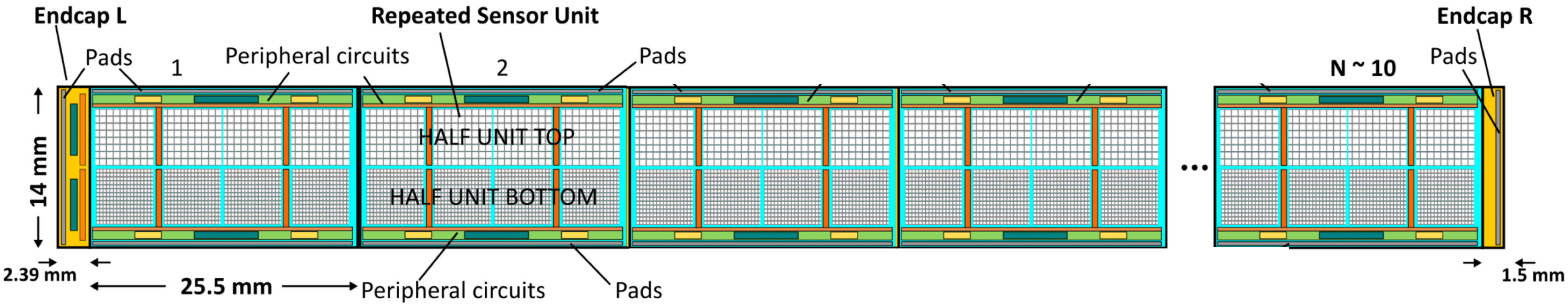
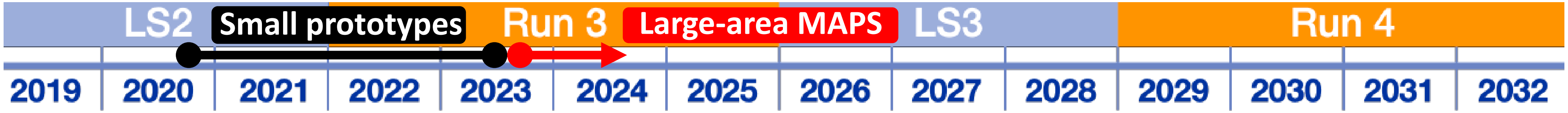
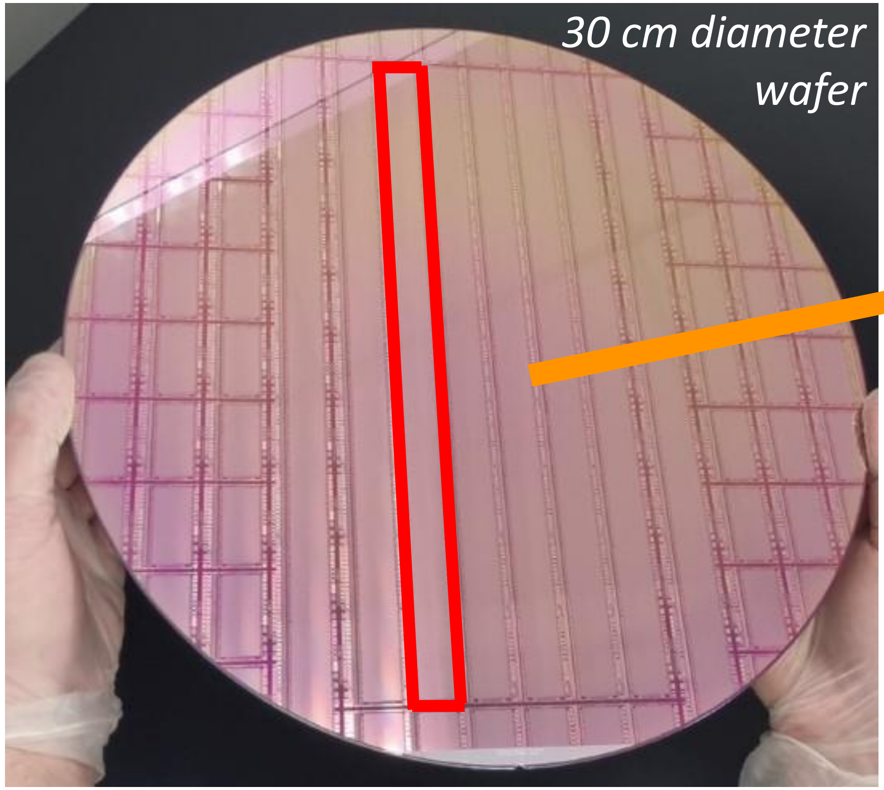


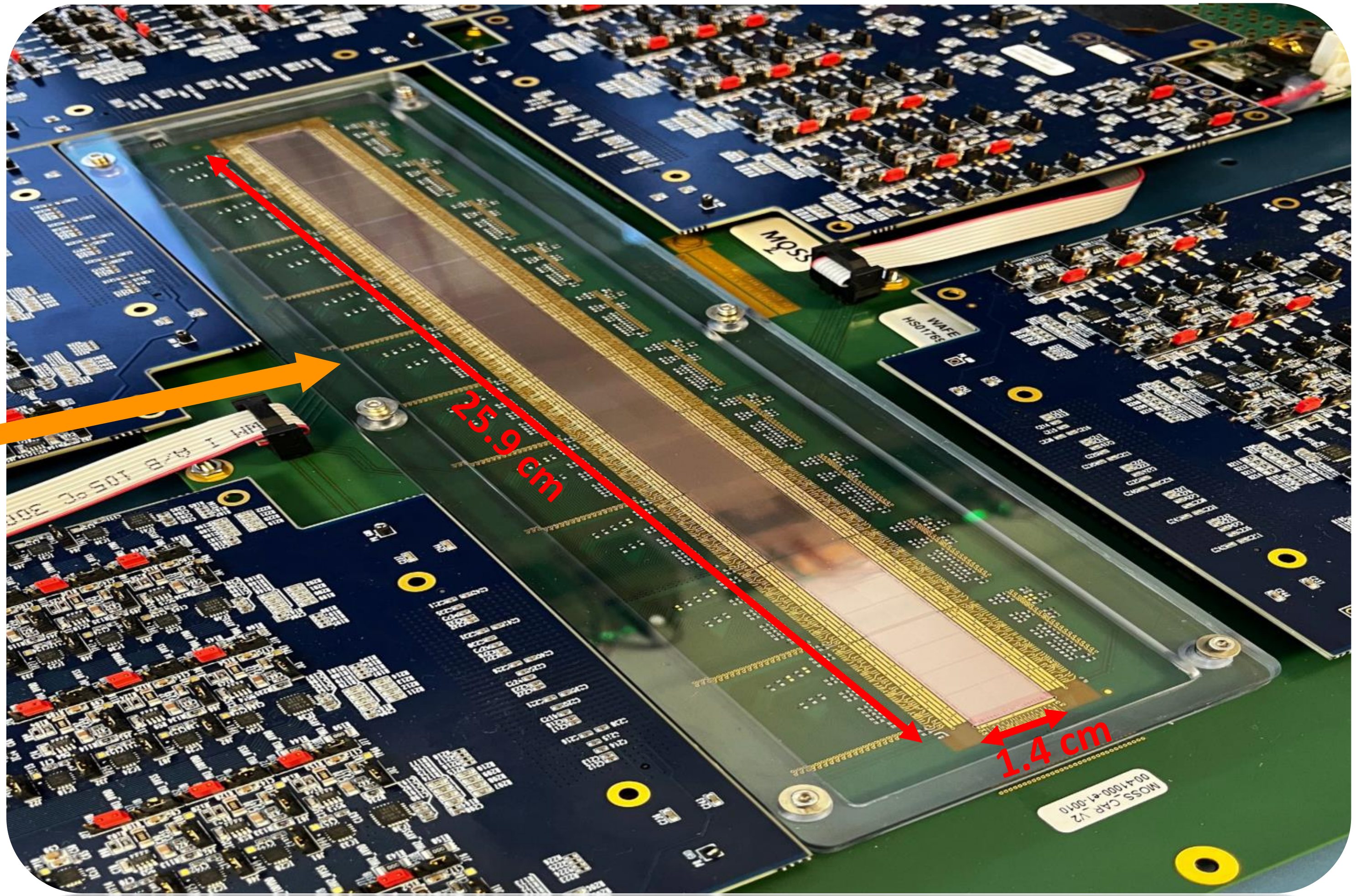
Large-area MAPS characterization



ER1: **MO**nolithic **S**titched **S**ensor, MOSS:

- 25.9 × 1.4 cm^2





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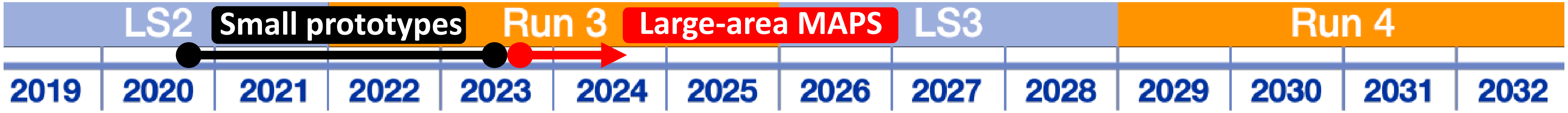

ER1: **MO**nolithic **S**titched **S**ensor, MOSS:

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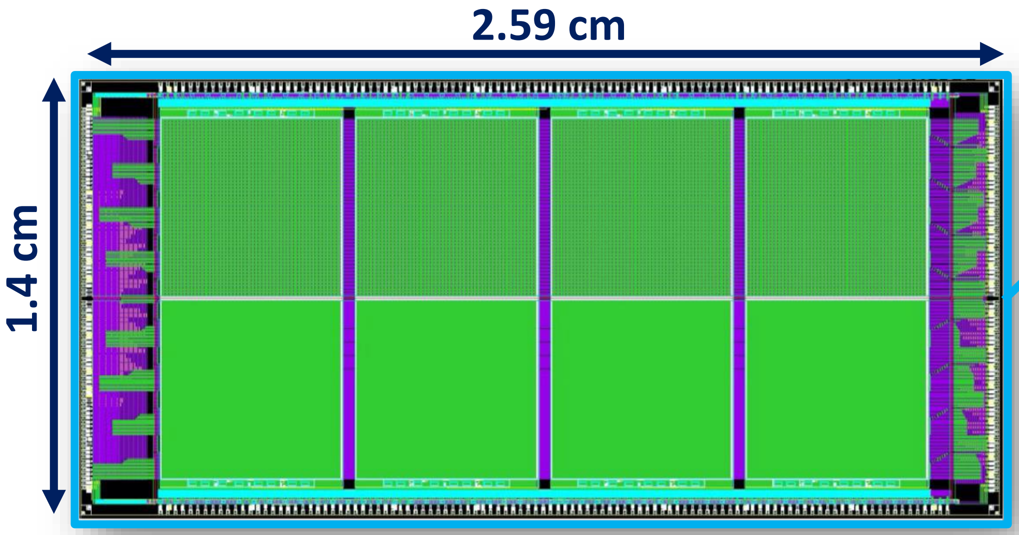
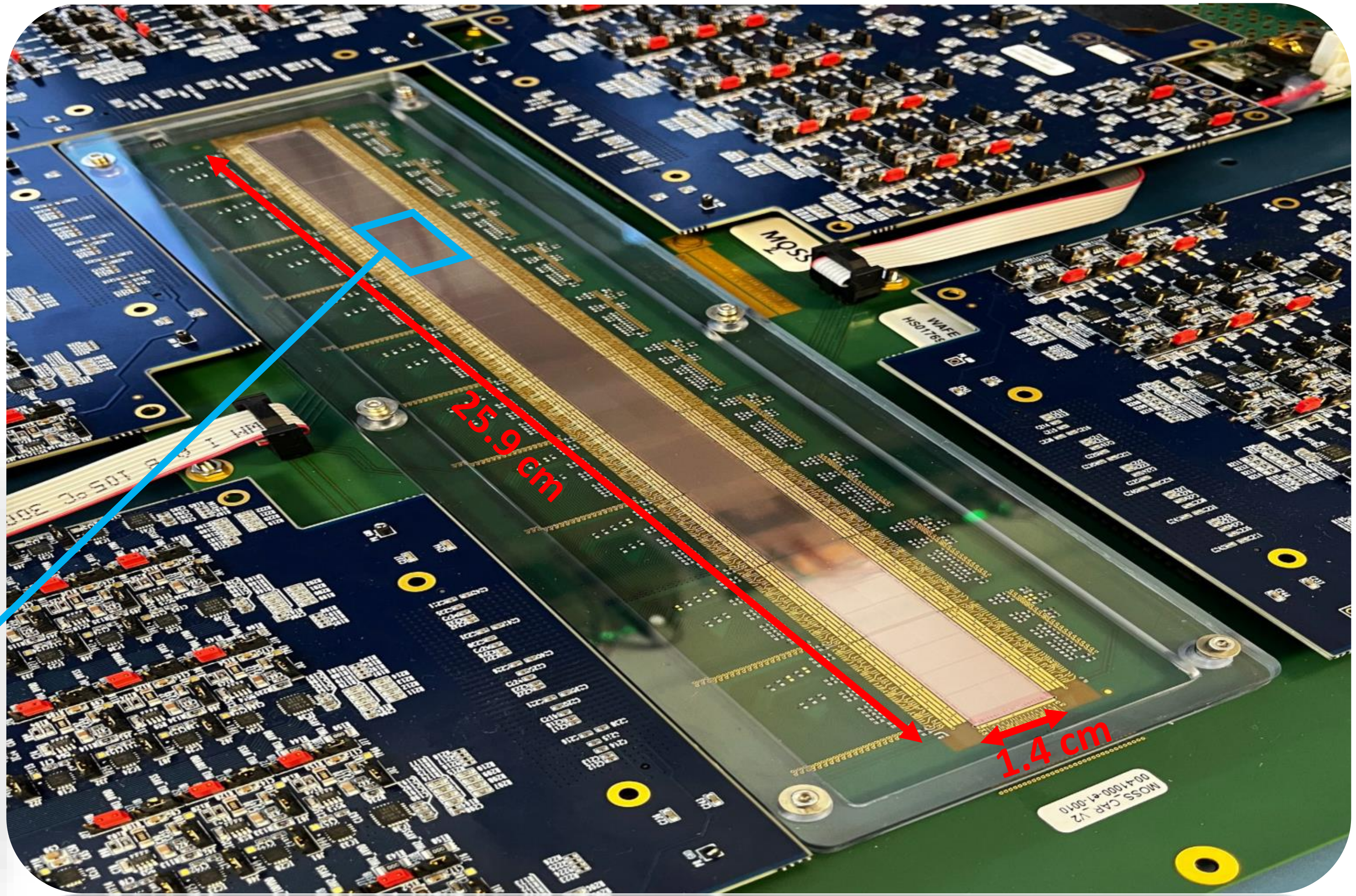
- 10 Repeated Sensor Units (RSU)



Repeated Sensor Unit



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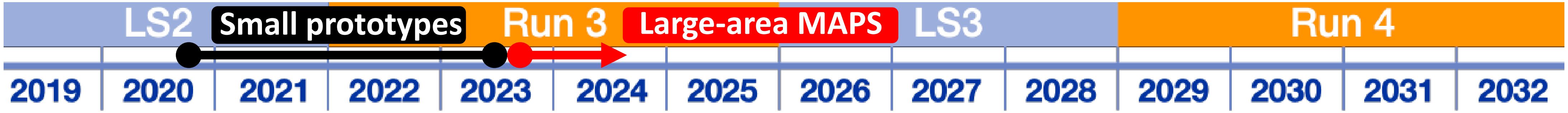
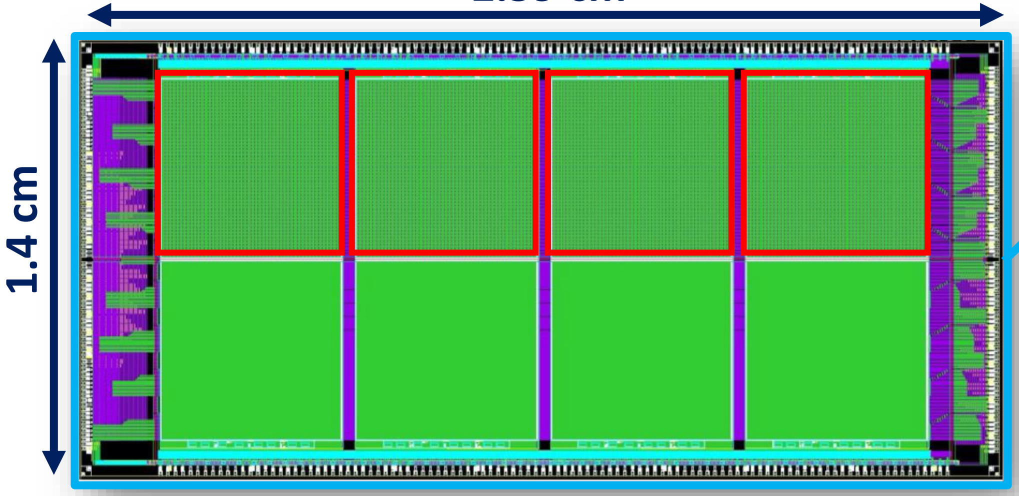
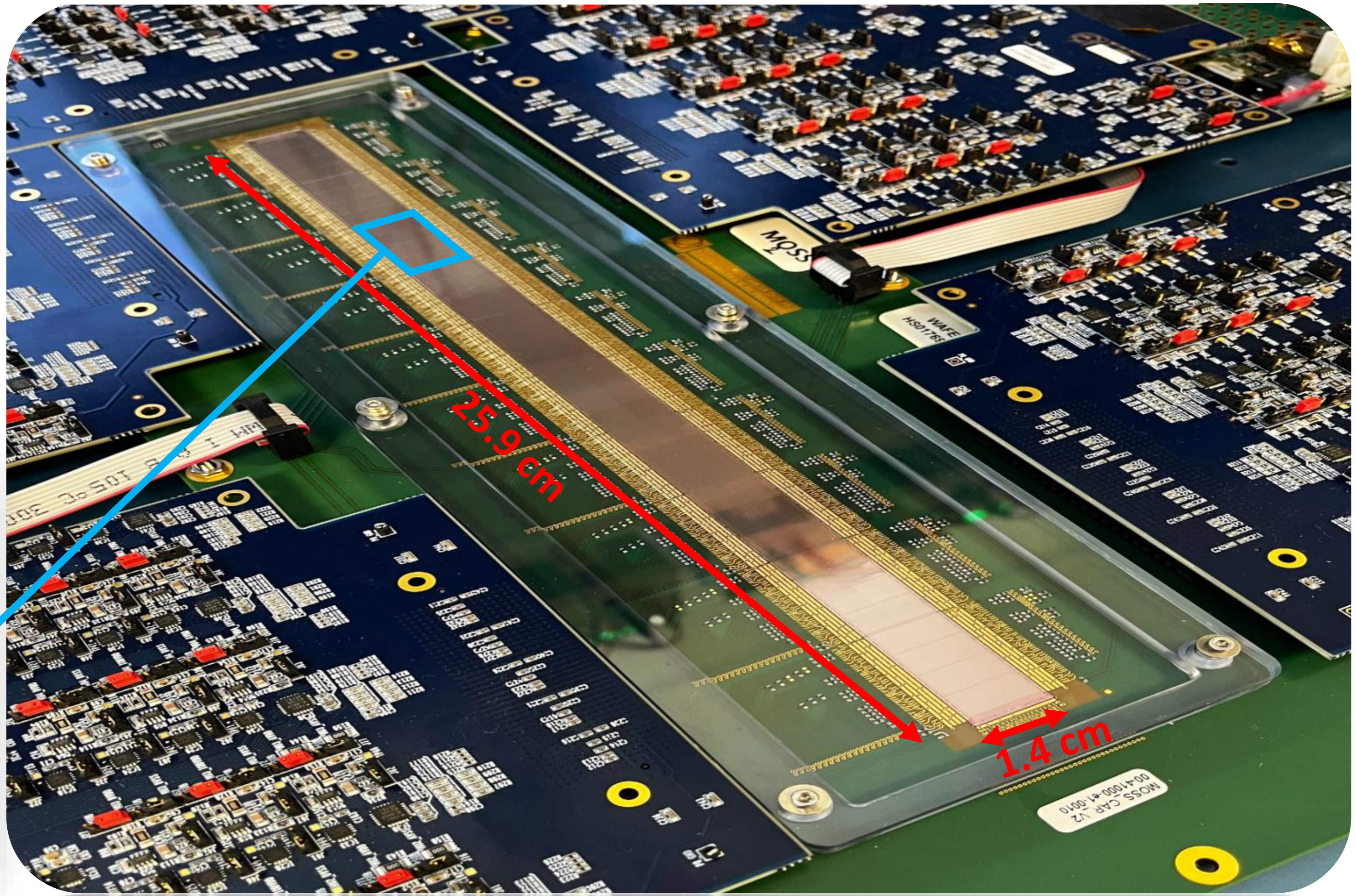


ER1: **MO**nolithic **S**titched **S**ensor, MOSS:

- 25.9 × 1.4 cm^2
- 10 Repeated Sensor Units (RSU)
  - 2 Half Units (HU) with 4 regions (each with different electronic)



Repeated Sensor Unit



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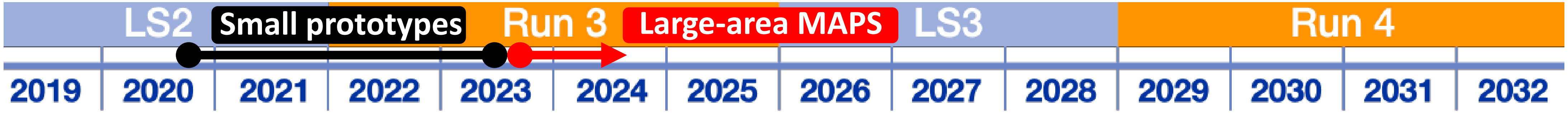

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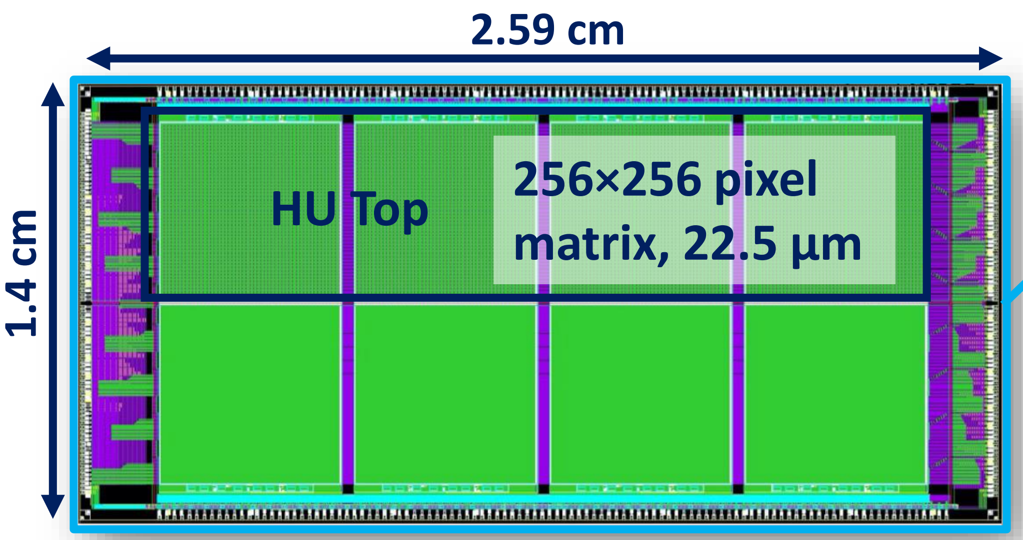
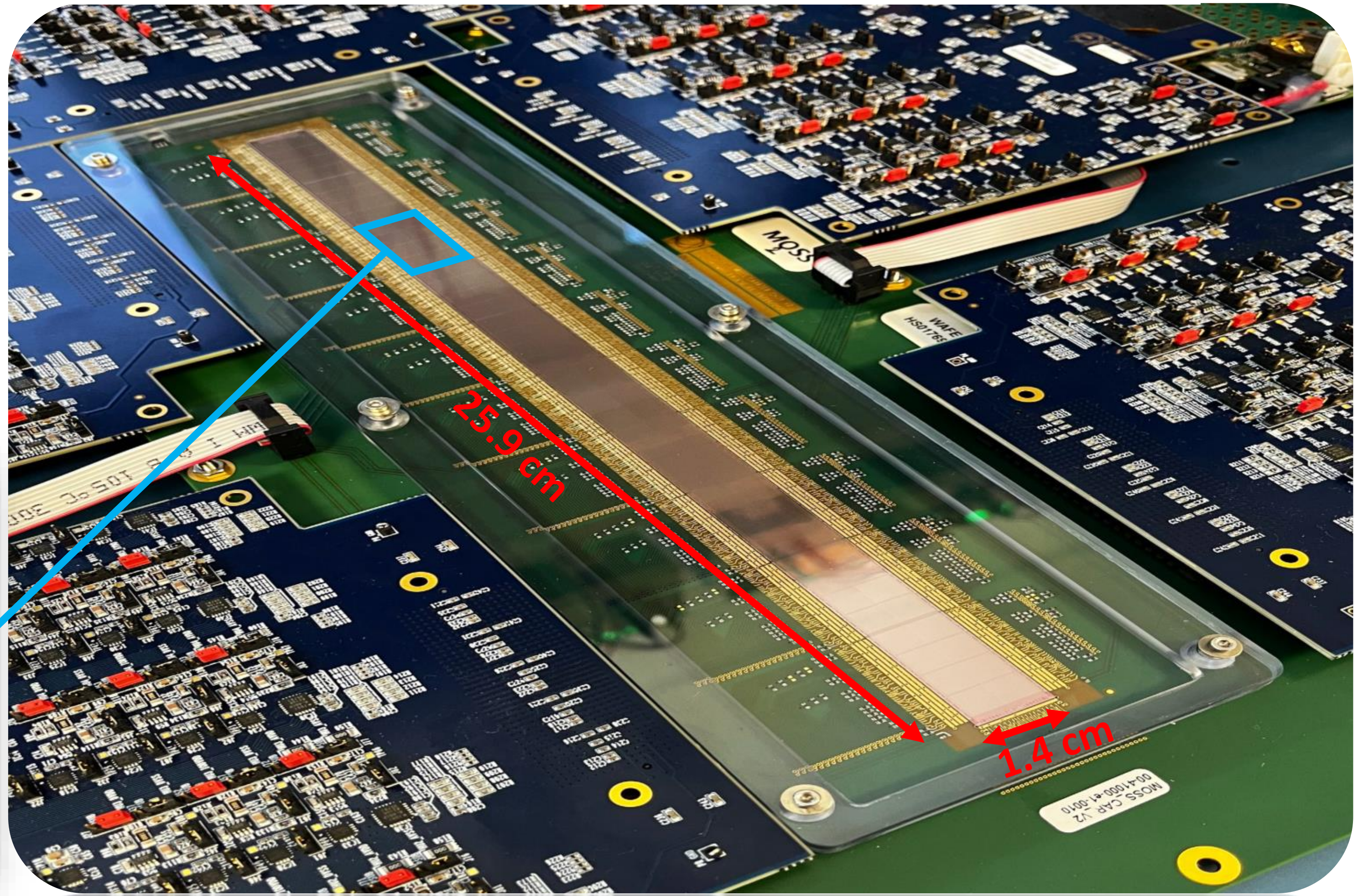
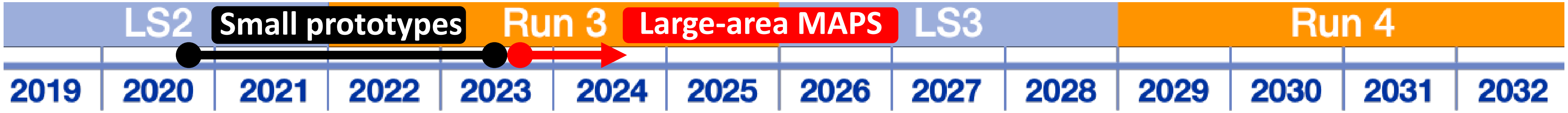


Repeated Sensor Unit



Large-area MAPS characterization



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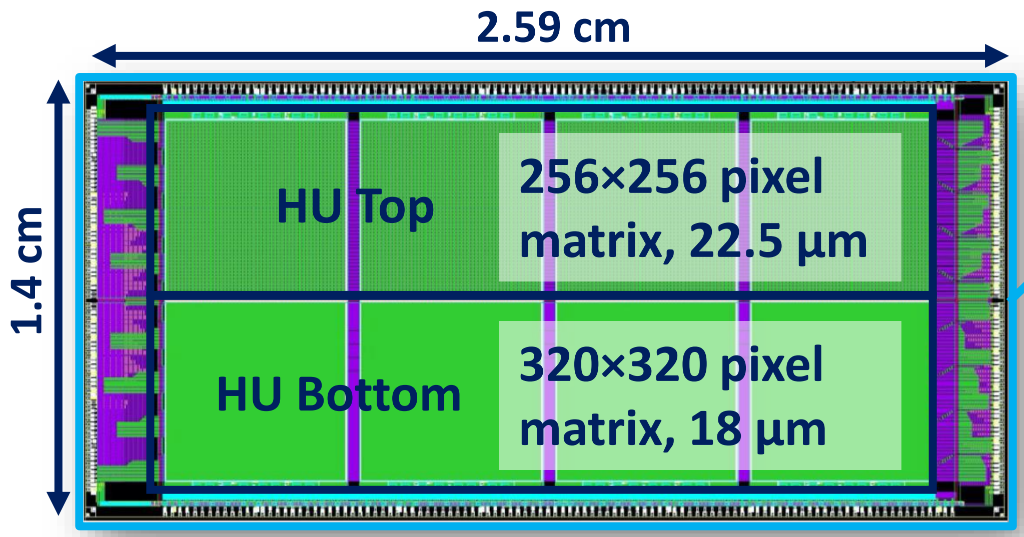
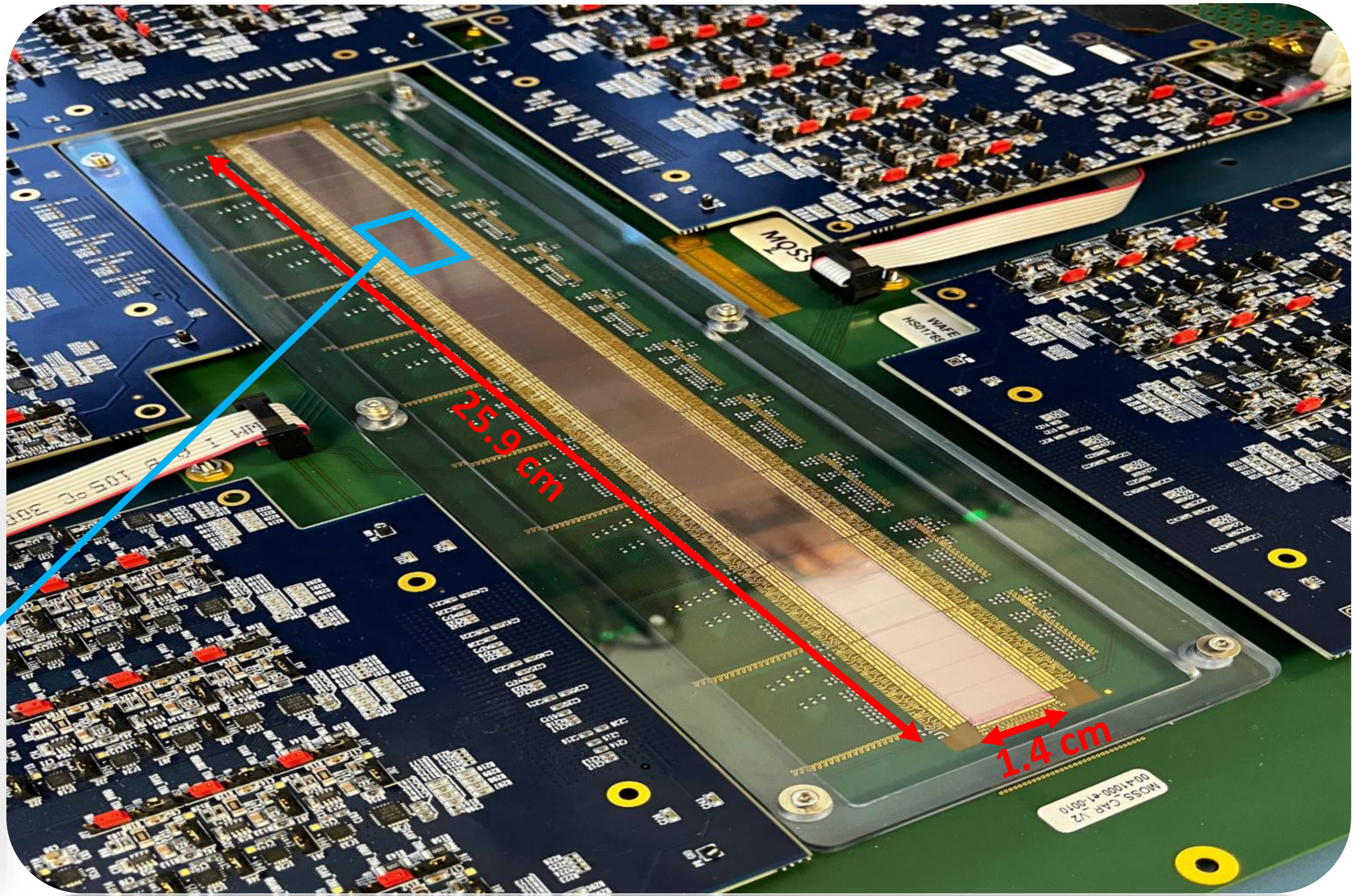
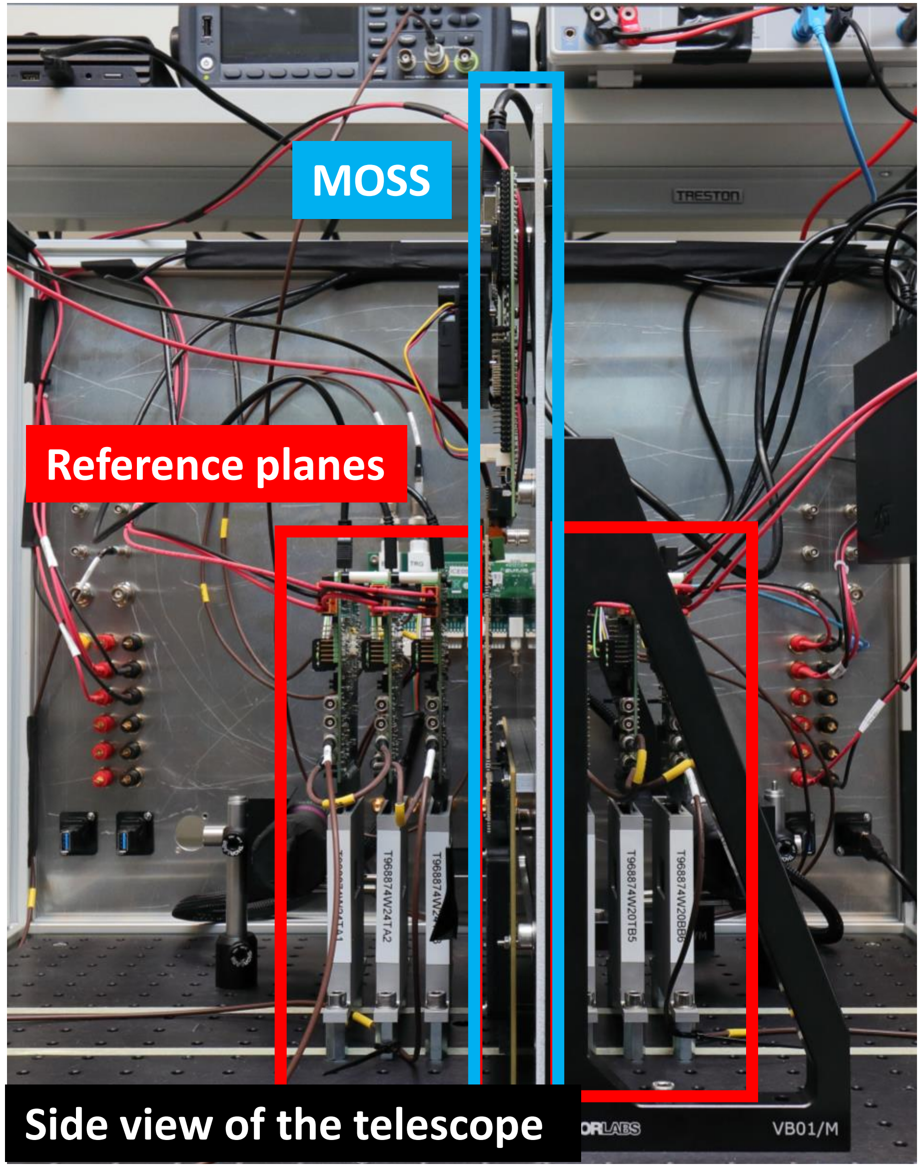


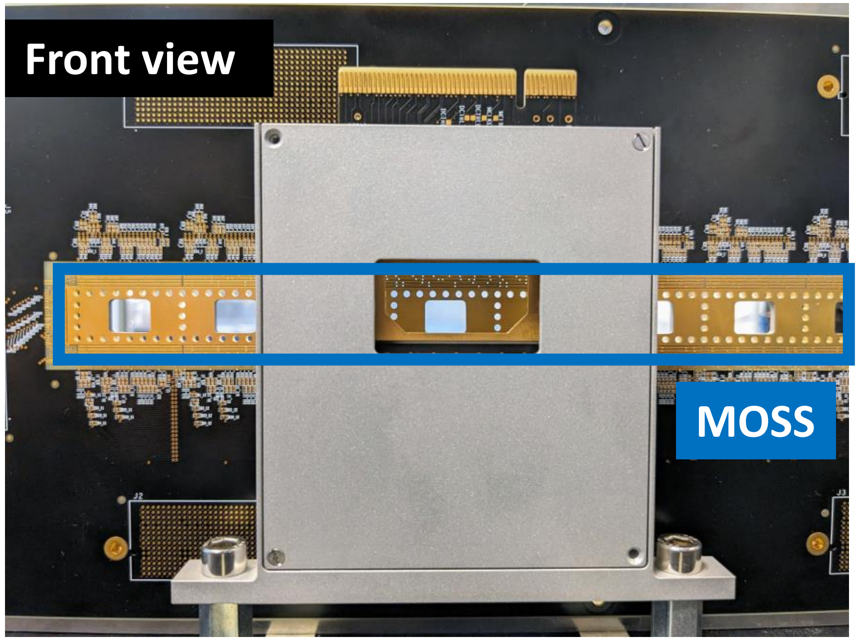
Repeated Sensor Unit



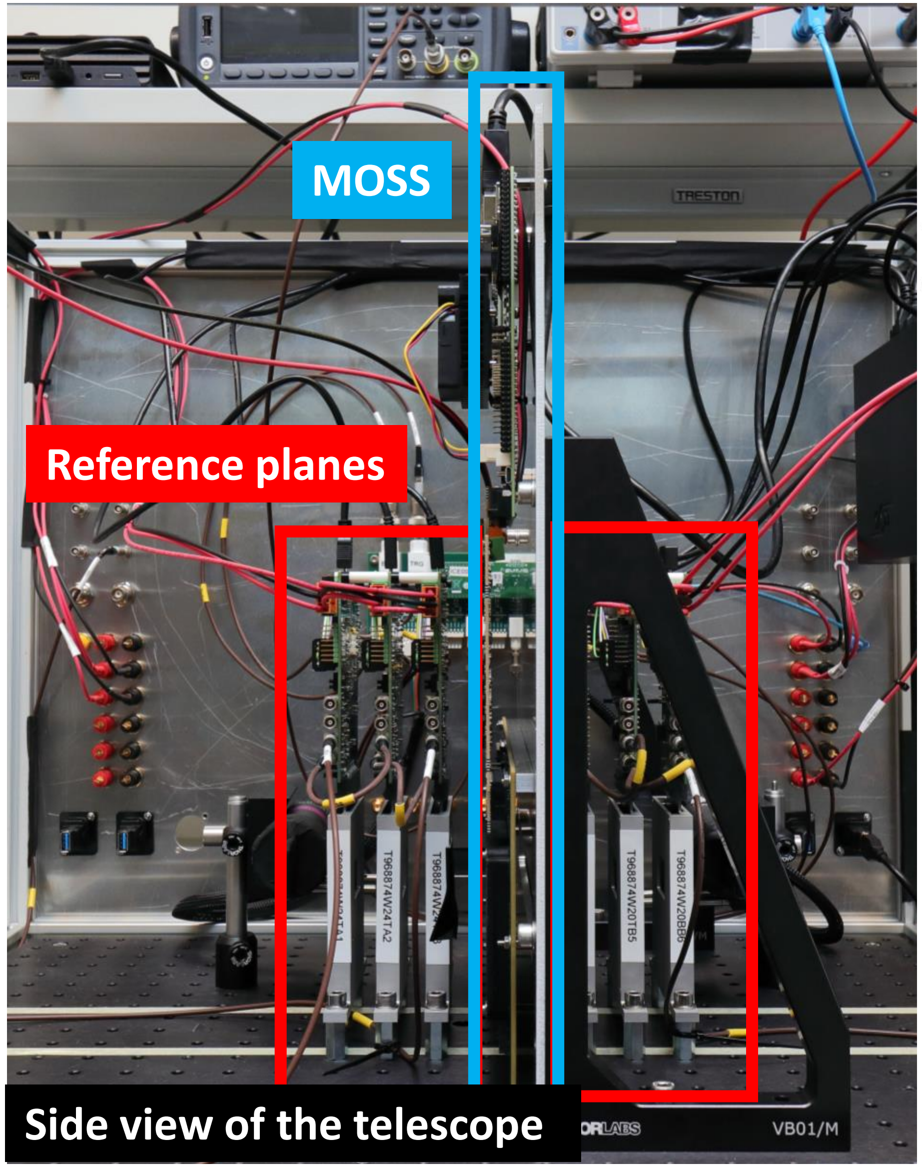
MOSS in-beam measurements



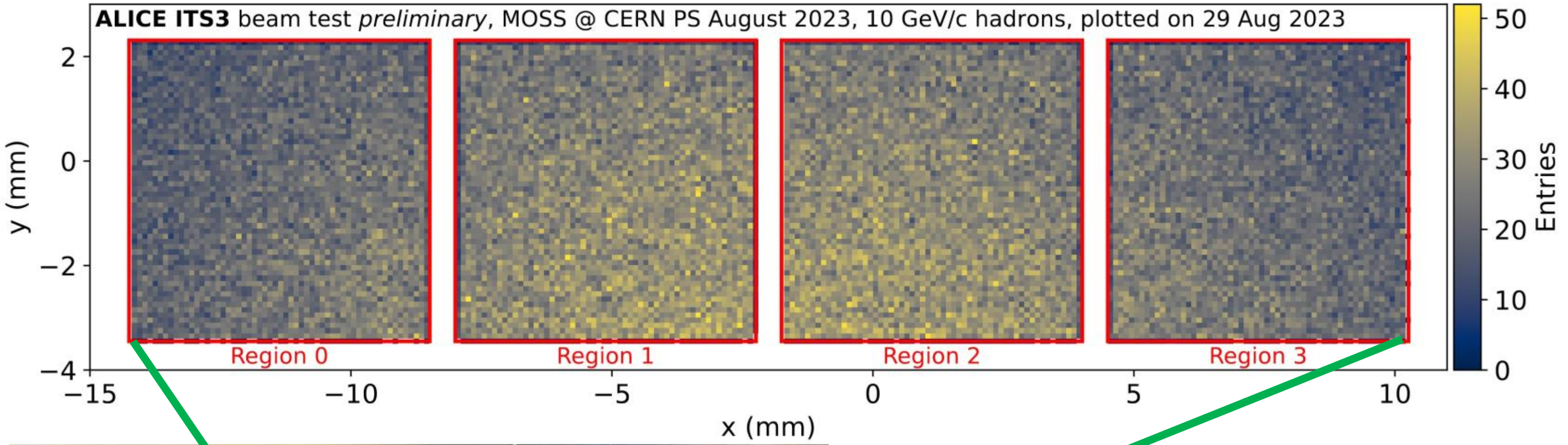
- Testbeam @ CERN PS

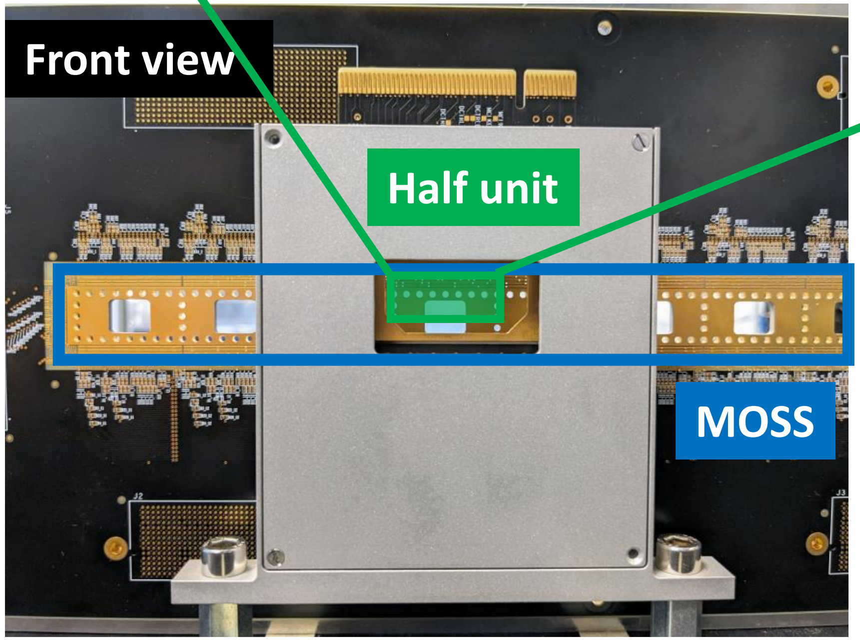


MOSS in-beam measurements

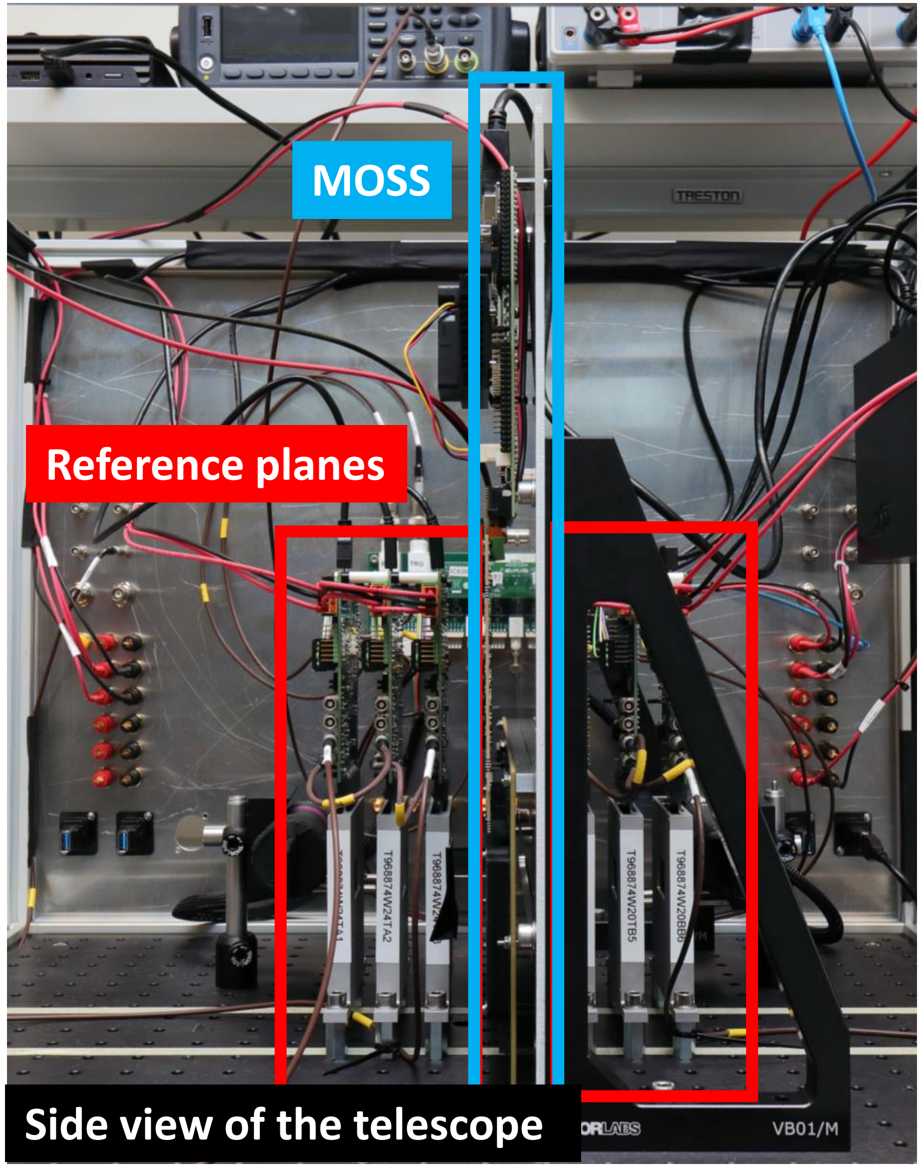


- Testbeam @ CERN PS: hitmaps

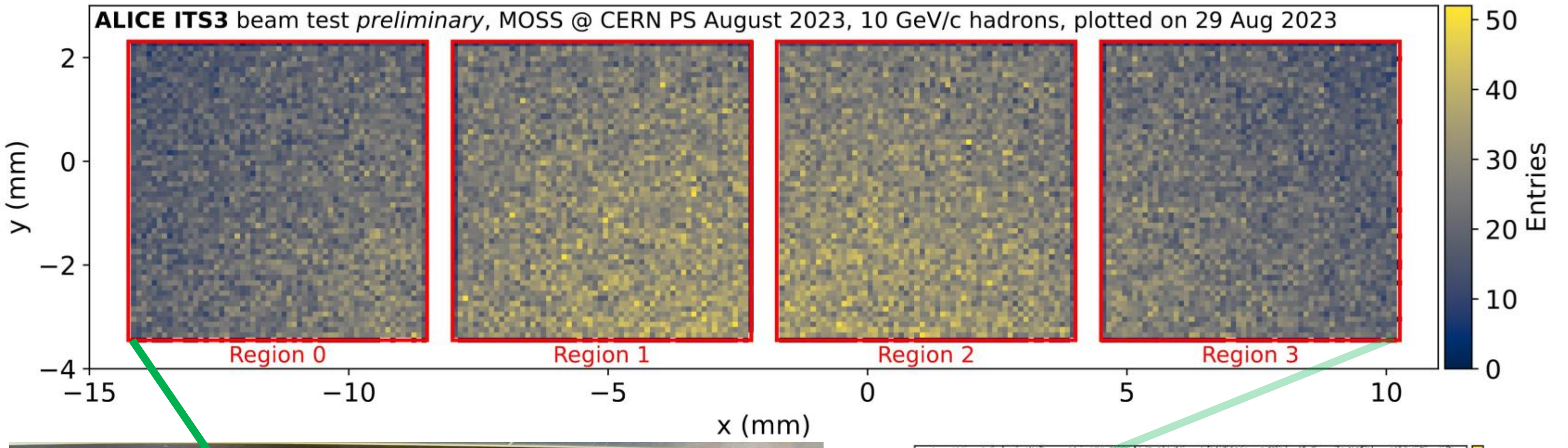


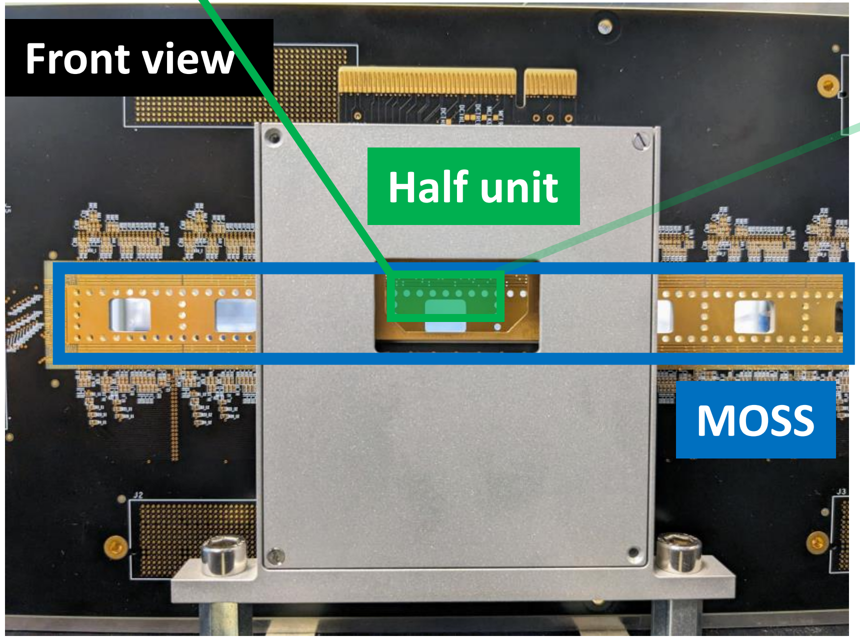


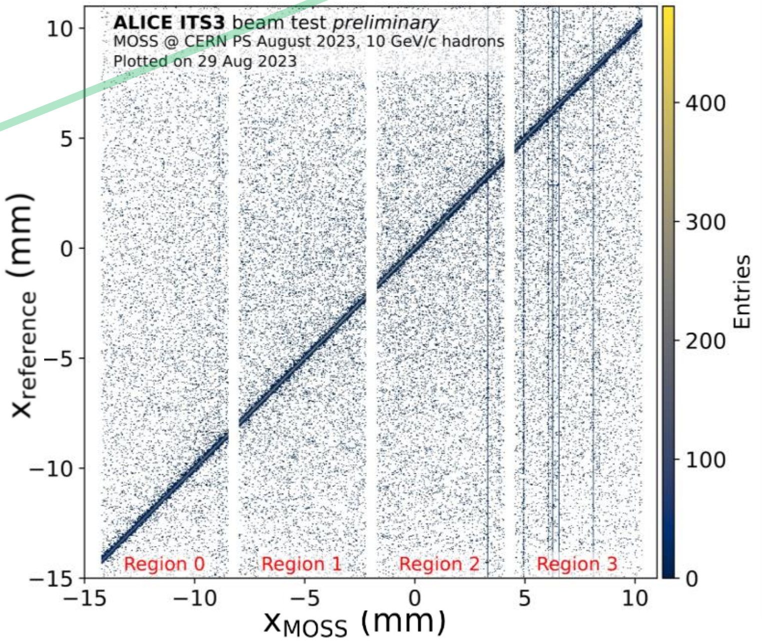
MOSS in-beam measurements



- Testbeam @ CERN PS: hitmaps and correlations







Conclusions

- An **innovative vertex tracker** will be installed in 2026 for the ALICE Experiment. It will be made of large-area, flexible, bent **MAPS detectors**.
- The activities towards ITS3 are going on as scheduled:
  - The **65 nm CMOS process has been validated**
  - The **radiation hardness** for both **TID** and **NIEL** (up to the expected level for the ITS3 of 10 kGy and 10^{13} 1 MeV n_{eq} cm^{-2}) was verified for the first test structures
  - An **excellent response** to X-rays in terms of energetic resolution was obtained
  - First tests on **stitched sensor** are ongoing
- The **ITS3** technology will be the **starting point** for the development of the new tracker for the future experiment **ALICE3**, proposed for run 5 and 6 of LHC

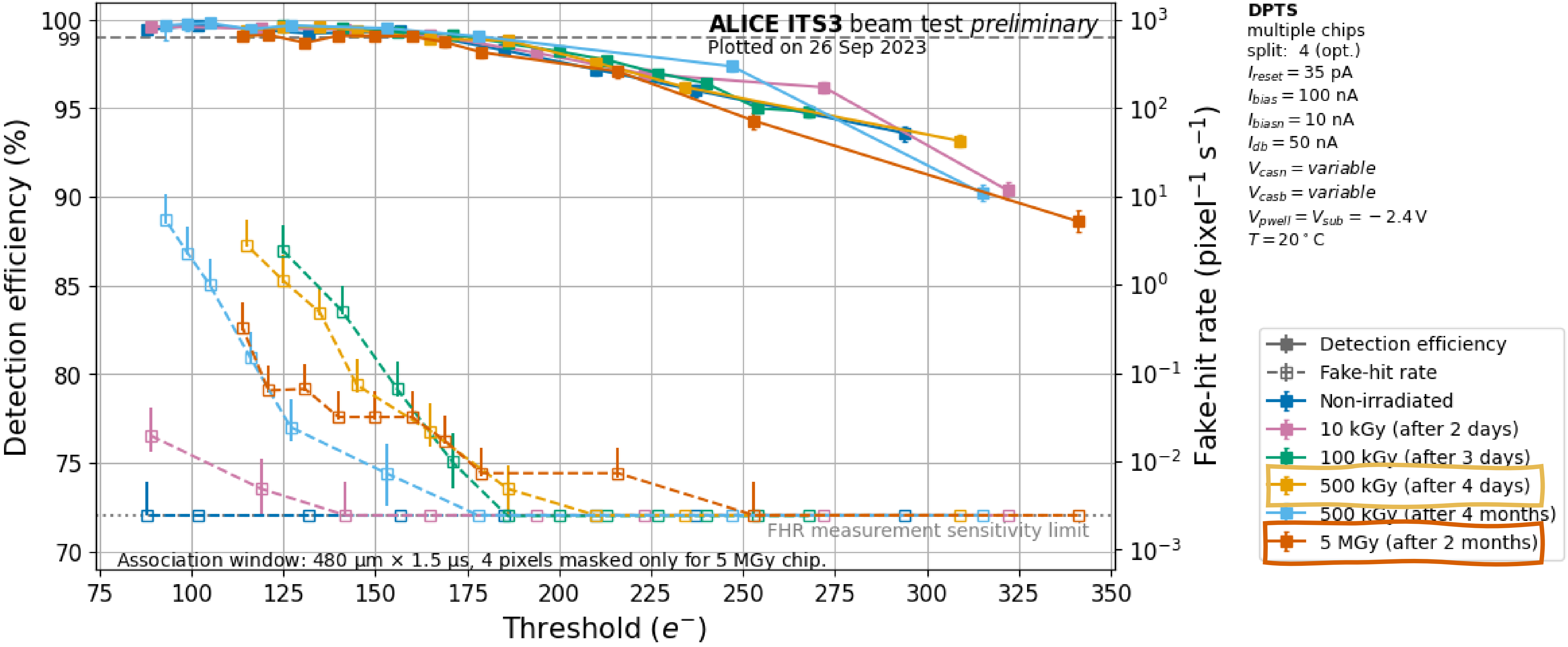

Thanks!

Backup

DPTS: TID radiation hardness

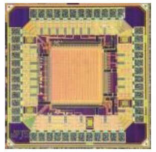
- DPTS performance with a TID radiation level above the ITS3 limit (10 kGy):
  - Efficiency of 99% at 500 kGy TID without annealing
  - Efficiency of 99% at 5 MGy TID after 2 months

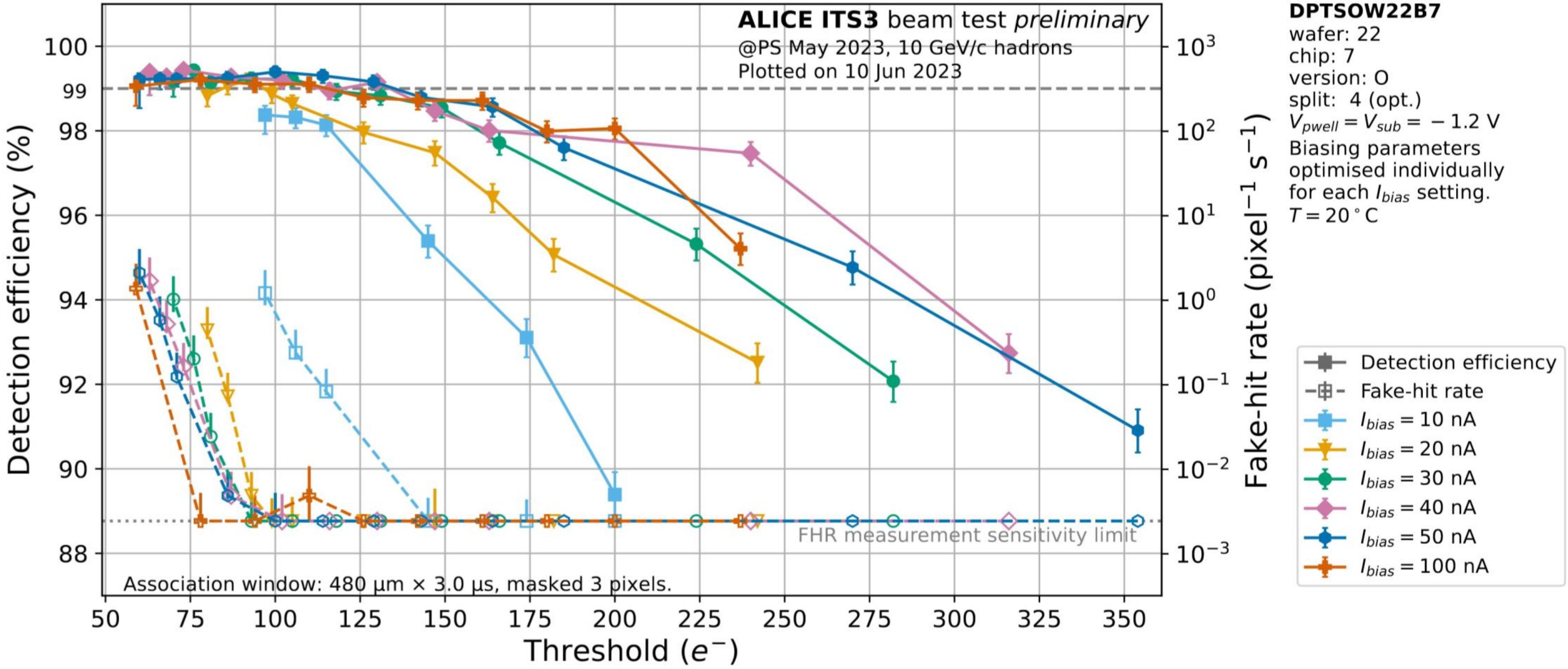
Digital
Pixel
Test
Structure



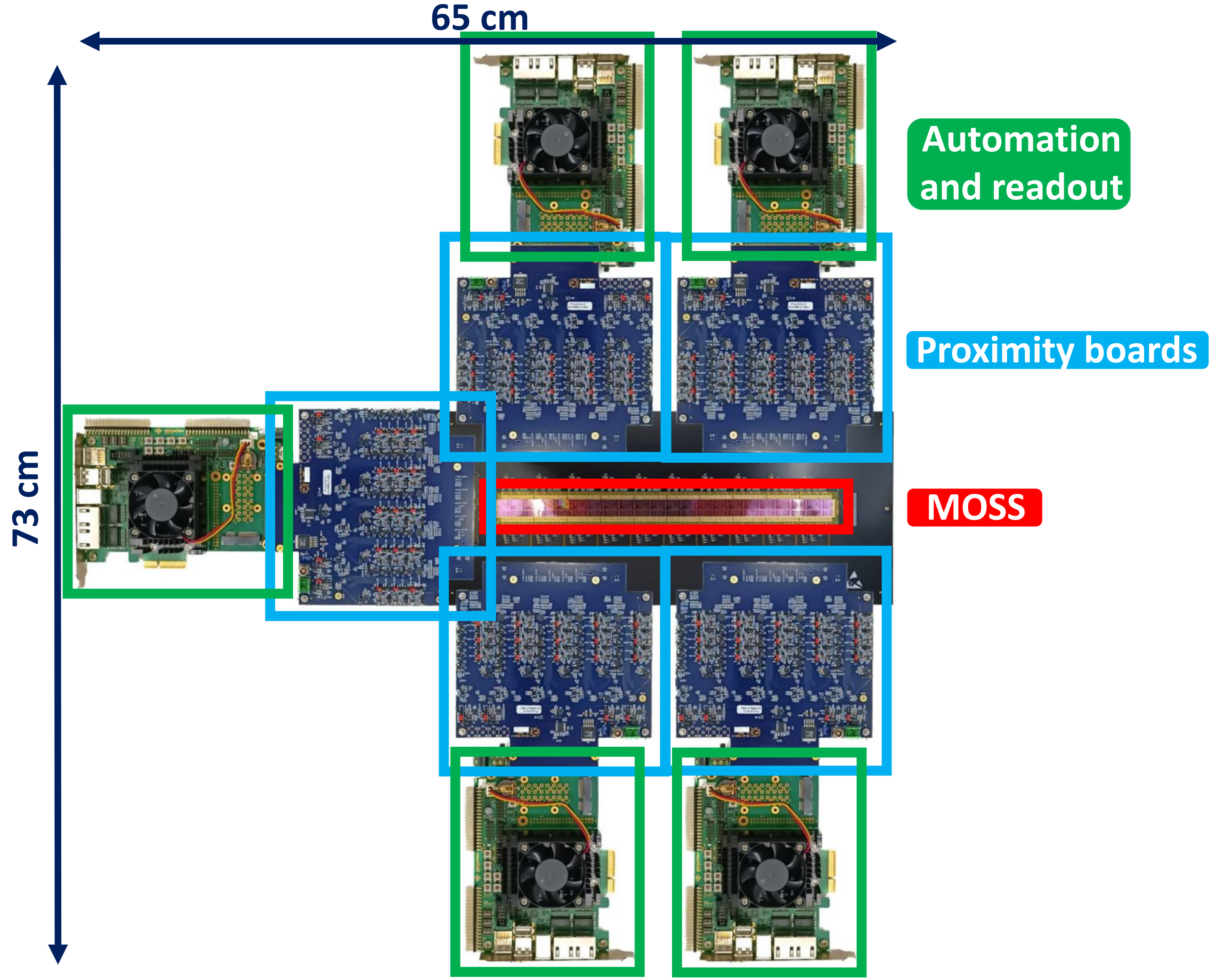
DPTS: power consumption

- ITS3 power consumption requirement: ≤ 40 mW/cm^2
- Lowest possible setting: I_{bias} = 20 nA → power consumption = 10 mW/cm^2





MOSS test system



Bent ITS3 prototypes