Proposal for DMAPS Upgrade of the Belle II Vertex Detector

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On behalf of the Belle II VTX Upgrade Group

outline

- Belle II and SuperKEKB
- The current VXD and the new upgrade VTX
- The TJ-Monopix 2 & the OBELIX design
- TJ-Monopix 2 Lab test & Test Beam
- Conclusions

Belle II and SuperKEKB

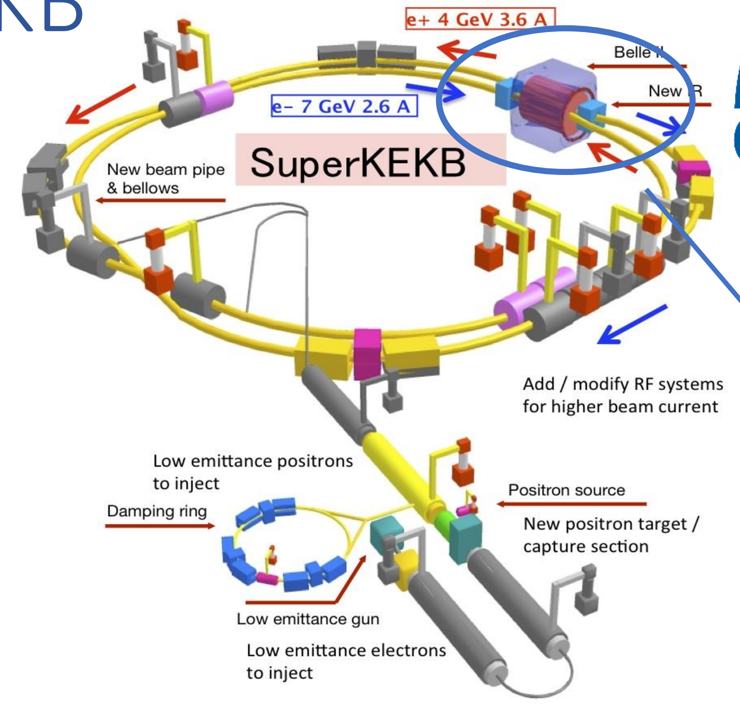
- Located at the SuperKEKB collider in Tsukuba/Japan
- Luminosity frontier experiment, a large ultra-high luminosity asymmetric electron-positron colliding device
- Asymmetric e^+ - e^- collisions at 10.58 GeV

- Current luminosity L_{int} = 428 fb^{-1} since 2019
- Record L_{max} = 0.47 * $10^{35}cm^{-2}s^{-1}$ in June 2022

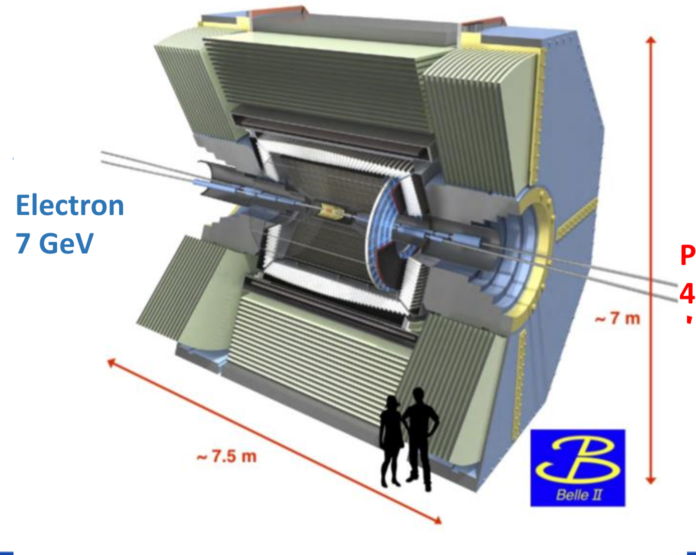
- Long Shutdown1 since June 2022
- Restart at end of 2023

A long way to reach the target peak luminosity:

- Target luminosity L_{int} = 50 ab^{-1}
- Target Peak L_{max} = 6 * 10^{35} $cm^{-2}s^{-1}$



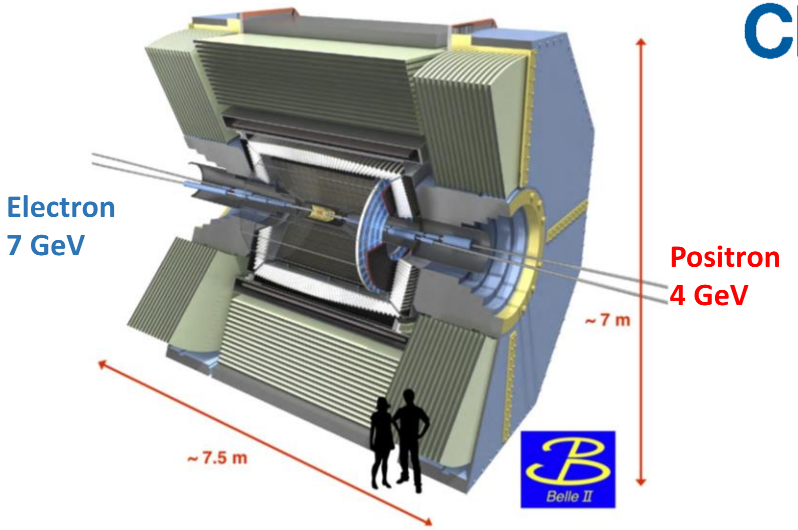
Belle II Detector



Belle II and SuperKEKB

Challenge

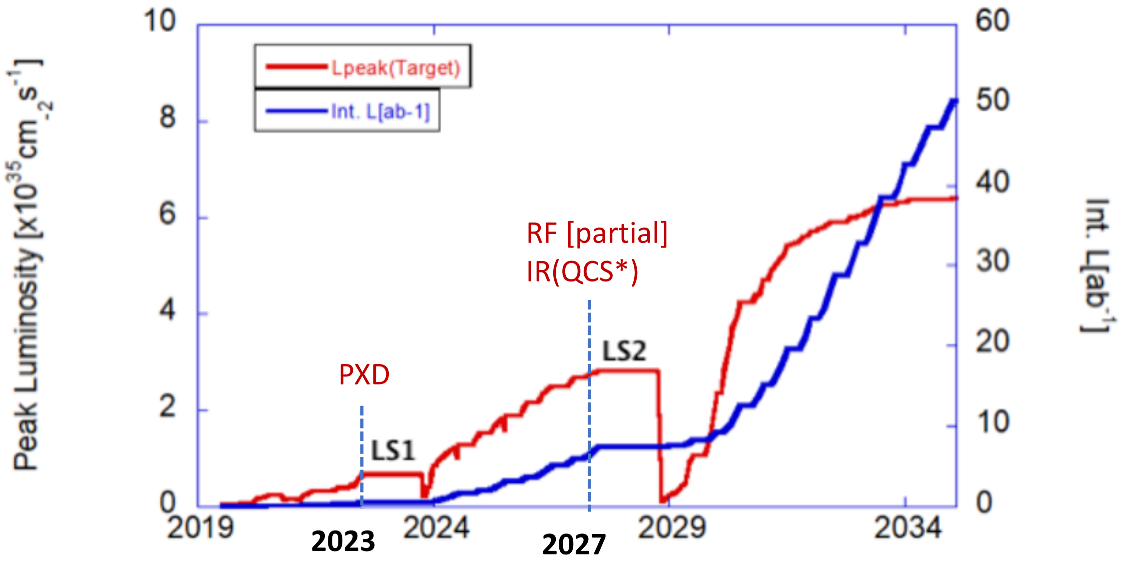
- Machine related beam background will increase with high luminosity (high currents & nano-beam scheme)
- Performance could degrade with higher occupancy from background (track finding efficiency, resolution)
- Potential change in Interaction Region



Goal of the upgrade:

- Upgraded to cope with the higher luminosity provided by the SuperKEKB accelerator
- To be more robust against high background and match possible new interaction region

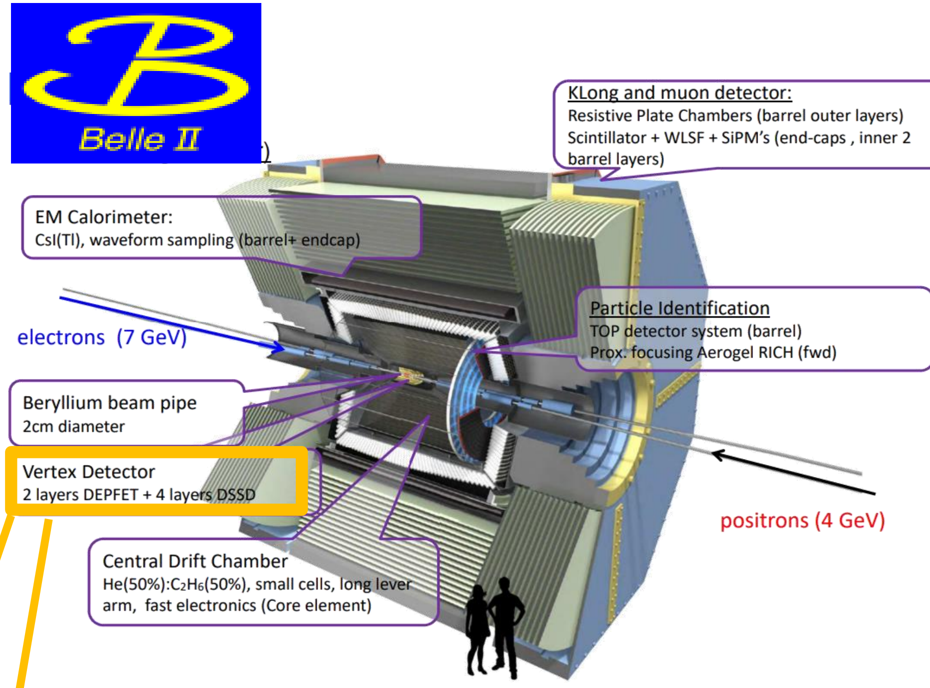
- Intend upgrade during Long Shutdown 2 (2027 or later)

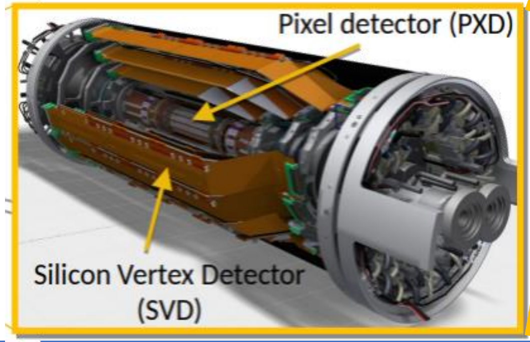


Current vertex detector VXD

- The main tracker device is the central drift chamber (CDC), which is complemented by a vertex detector (VXD)
- Two technology system:
  - Two layers of DEPFET pixel -- PXD see talk Anselm Baur
  - Four layers of double-sided strip detector –SVD see talk Jaroslaw Wiechczynski

- Standalone tracking for low momentum (SVD)
- Current VXD performance good & operating with low background occupancy < 1 % , well below limits (PXD ~ 3% SVD ~ 5%)
- Performance degradation possible for higher occupancy
- Extrapolation to target luminosity has large uncertainty and limited safety margin detector limit



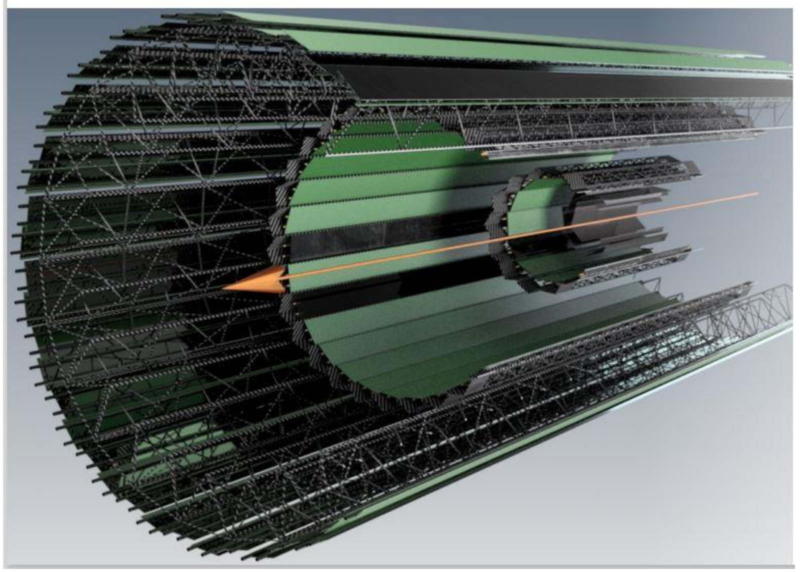


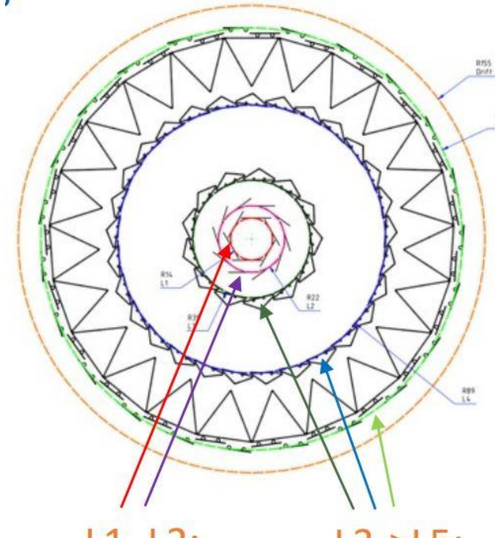
The VTX baseline Concept

- A new fully pixelated CMOS detector proposed to replace the VXD → VTX
- 5 straight fully pixelated barrel layers
  - Same sensor chip for all layers
  - **D**epleted **M**onolithic **A**ctive CMOS **P**ixel **S**ensors - chip size: 2x3 cm^2, moderate pixel pitch 33 μm^2
  - 2 layers iVTX and 3 layers oVTX
  - Power dissipation ~ 200 mW/cm^2
  - Reduced material budget:

    3.8% X_0 → 2.5% X_0 (sum of all layers)
- Increase granularity:
  - Space for SVD
  - Time for PXD

- Requirements:
  - Radiation tolerance
    - TID: ~ 10 Mrad/year
    - NIEL: ~ $5 * 10^{13} n_{eq}/cm^2/year$
  - Hit Rate : up to 120MHZ/cm^2
  - Resolution < 15 μm
  - Trigger at 30KHz average frequency with 5-10μs latency
  - Fast integration time 50-100 ns
  - Reduce occupancy and increase tracking performances

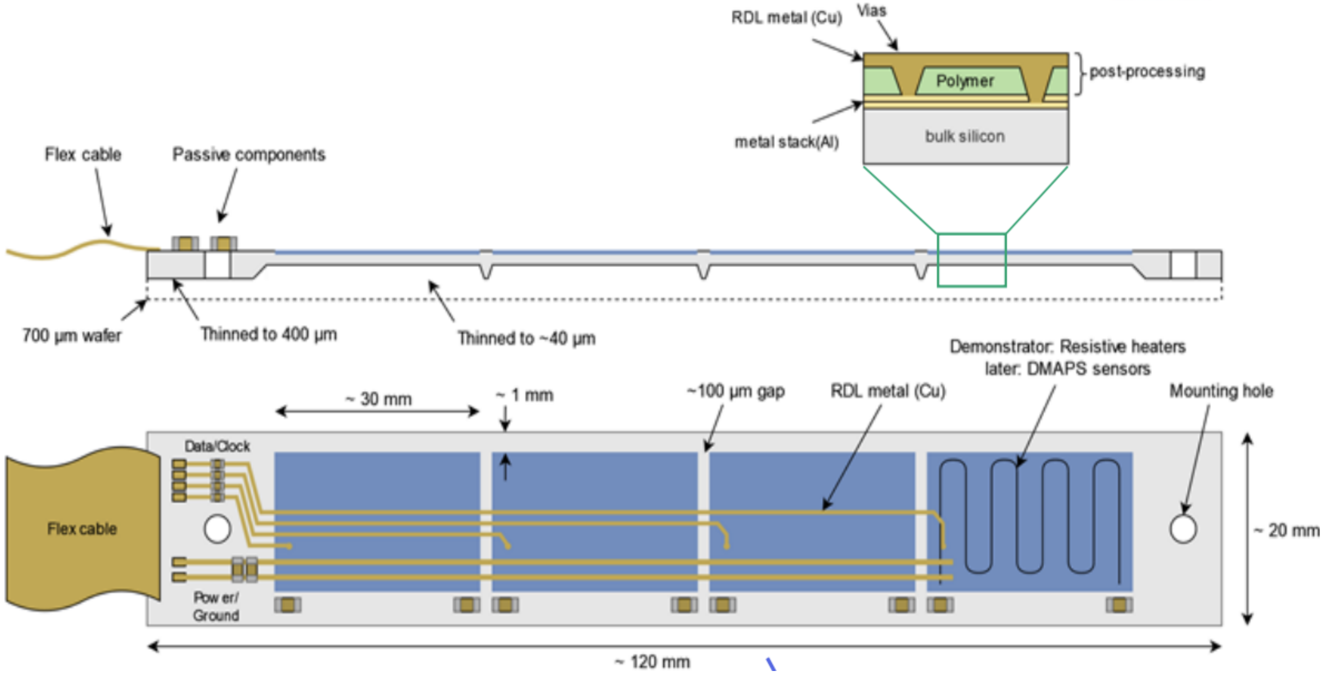


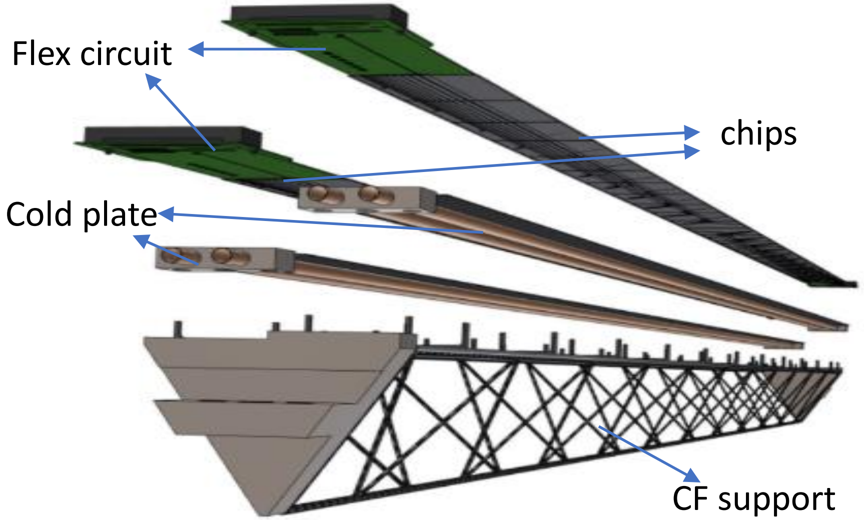


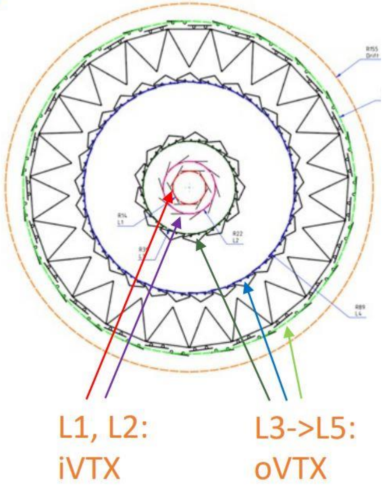
The VTX detector mechanics

- L1 and L2 (iVTX):
  - Radii innermost layer 14mm
  - Self-supported all silicon module
  - 4 contiguous sensors blocks diced out of wafer
  - Interconnected with redistribution layer
  - Heterogeneous thinning
  - Air cooling
  - ~ 0.1% X_0 for L1 &L2

- L3 to L5 (oVTX):
  - Radii outermost layer 140 mm
  - Carbon fiber support frame
  - Cold plate with water cooling
  - ~ 0.4% X_0 for L3, ~ 0.6% X_0 for L4 ~ 0.8% X_0 for L5

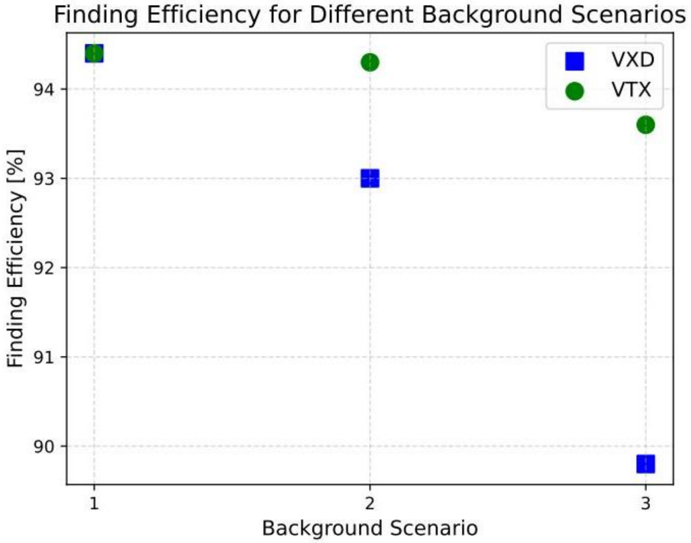






VTX simulated tracking performance

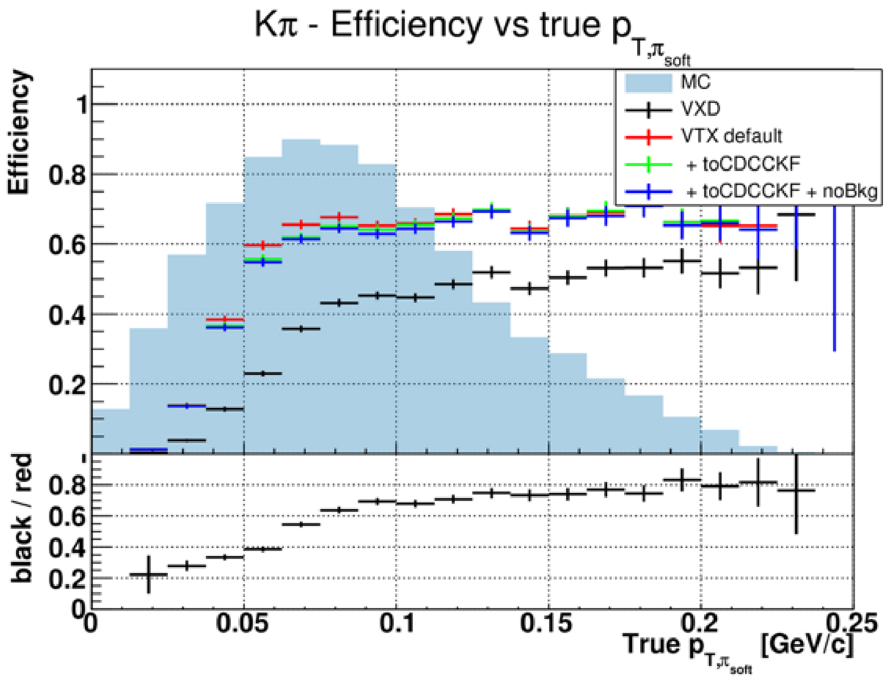
- VTX performance studied based on the tracking of single event, overlaying to signal events different beam background levels:
  - The events are just coming from generic events e+ e- producing a pair of B mesons
  - From optimistic BG scenario 1 to conservative BG scenario 3
- Possibility to include all layers in the tracking
- VTX provides better vertex resolution than the current VXD in the decay channel B^0
- VTX gives better tracking efficiency than VXD for full tracking (vertex tracking combined with CDC), especially at low momentum (soft pions signal in particular).



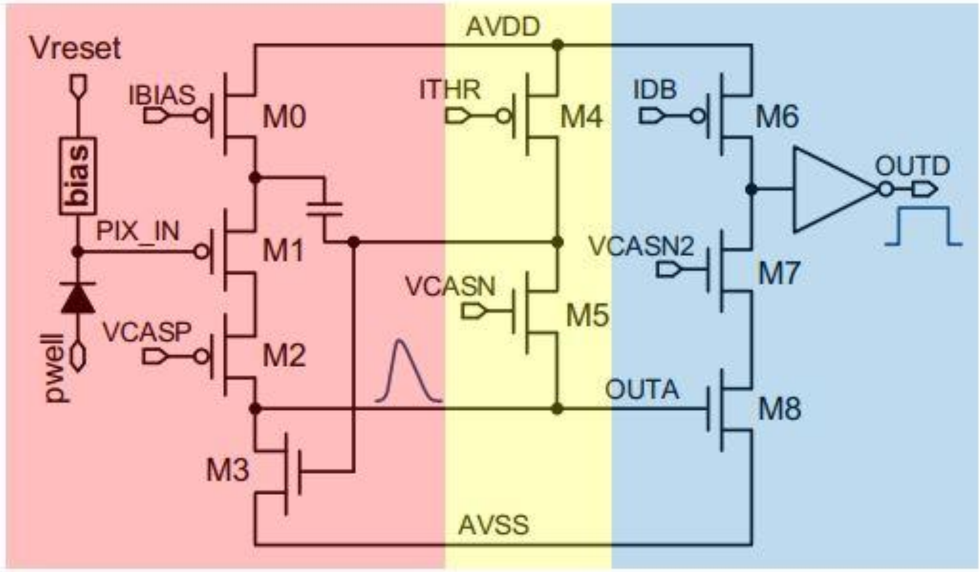
- **Physics benchmarking**

  Soft π reconstruction in $B^0 \rightarrow D^{*-}\mu^+\upsilon_\mu$

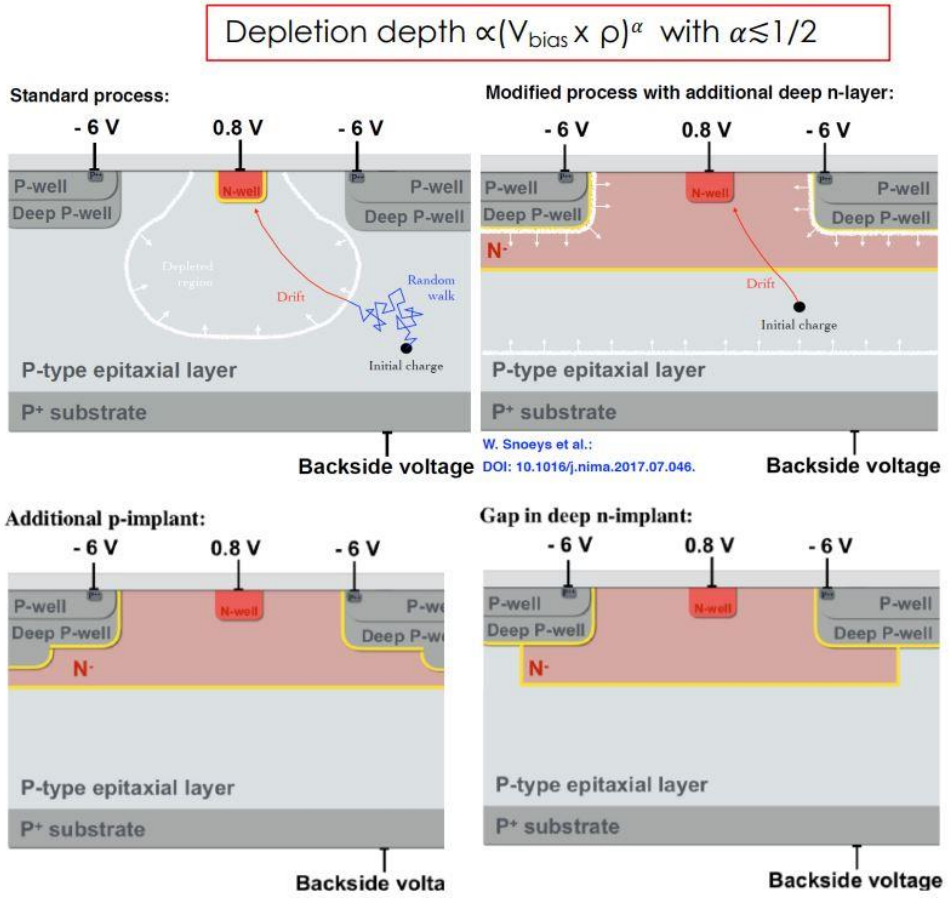
  $\quad\quad \hookrightarrow \overline{D^0}\pi^-$



Technological choice

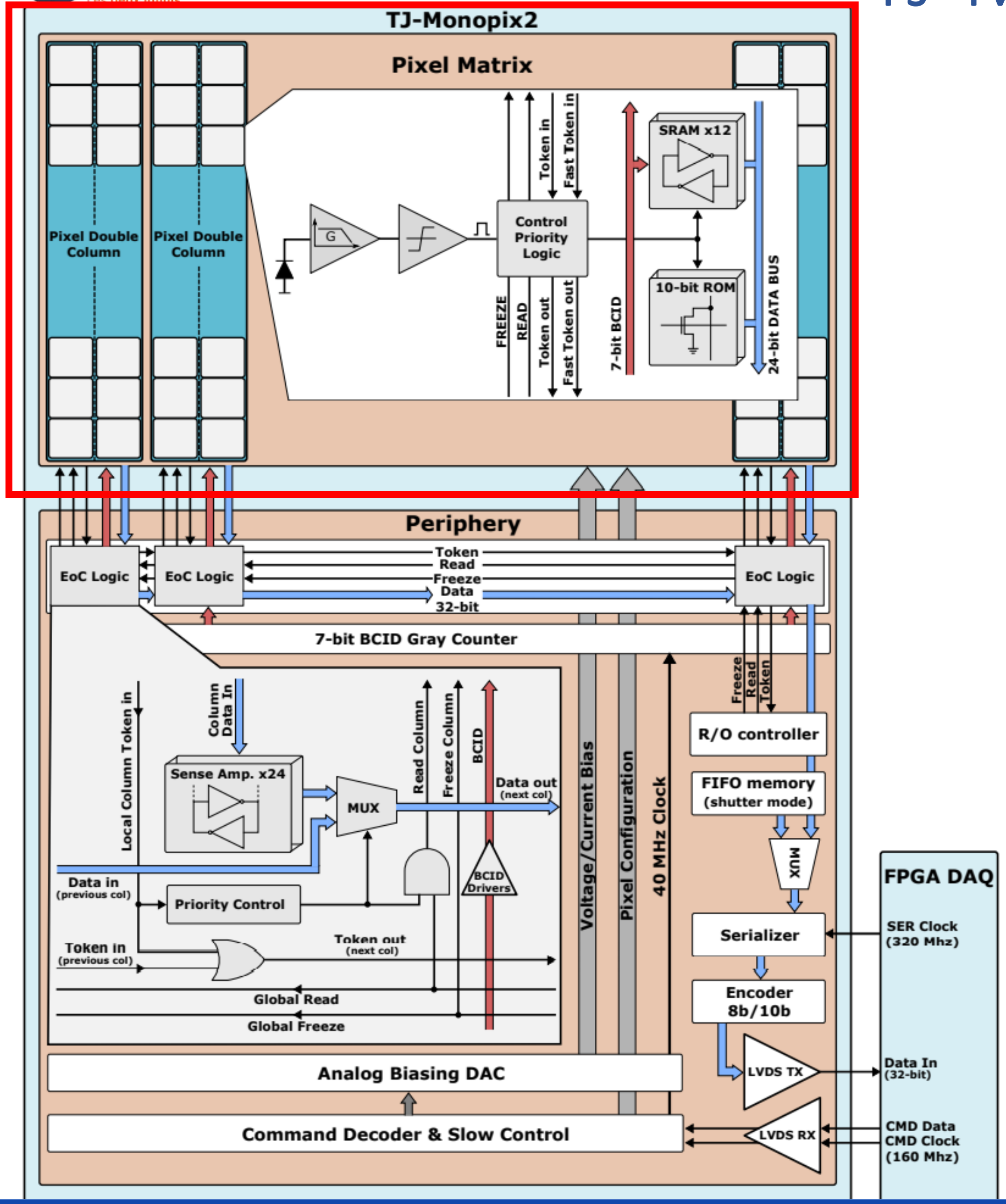


- Depleted MAPS in Tower Jazz 180nm technology:
- Large expertise in the community and many projects
- CMOS pixel sensor + electronics in same silicon die



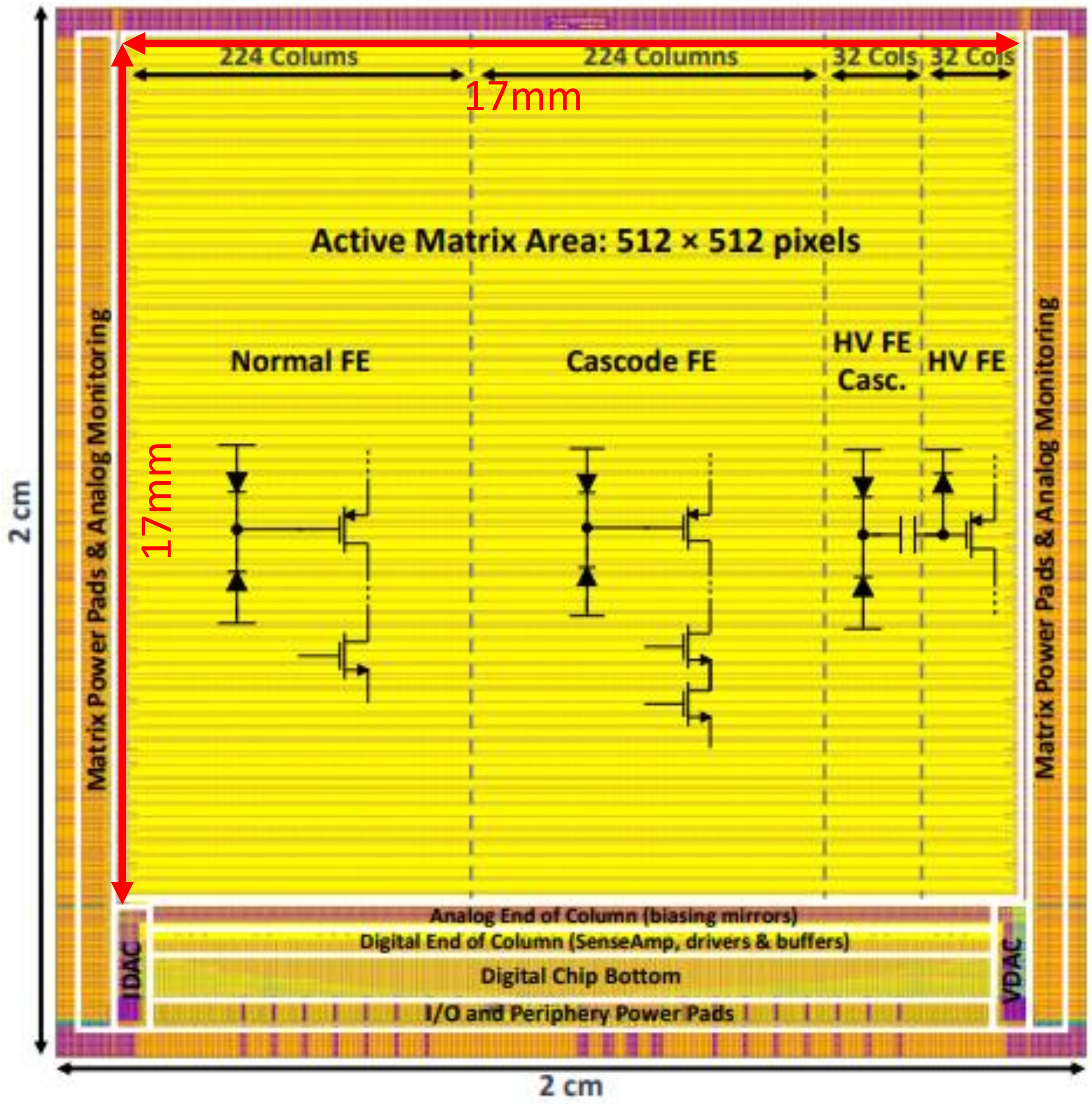
- Small electrode concept:
  capacitance, power, Tpeak, large conversion factor
- Modified process: higher radiation tolerance

TJ-Monopix2



- Developed for ATLAS experiment (2020)
  - FE derived from ALPIDE
  - Column-drain R/O architecture
- Expected from design:
  - 5-10 e− threshold dispersion (tuned)
  - >97% efficiency at 10^{15} n_{eq}/cm²
  - ~ 5 e− noise
  - Fully efficient with hit rate 120 MHz/cm²
  - MIP ~ 2500e−
  - Pixel matrix
  - TJ 180nm technology
- Proposed as starting point for OBELIX design
  - Keep pixel matrix design
  - Trigger adaptation in new digital periphery

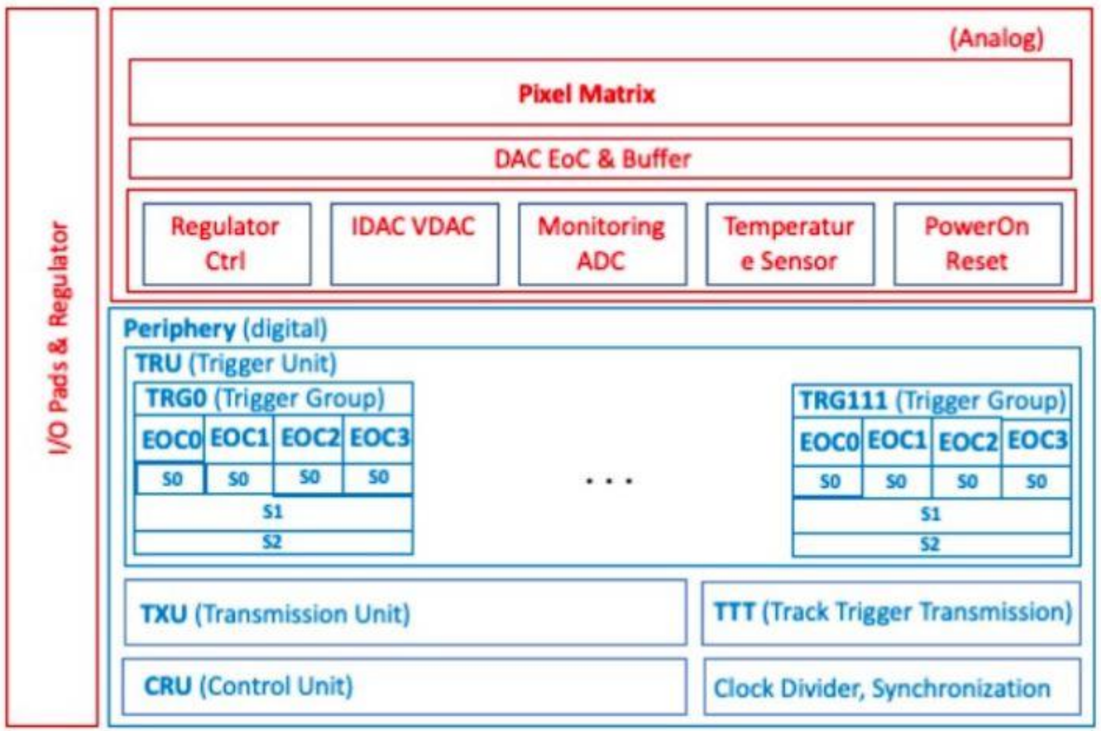
TJ-Monopix2 – pixel matrix

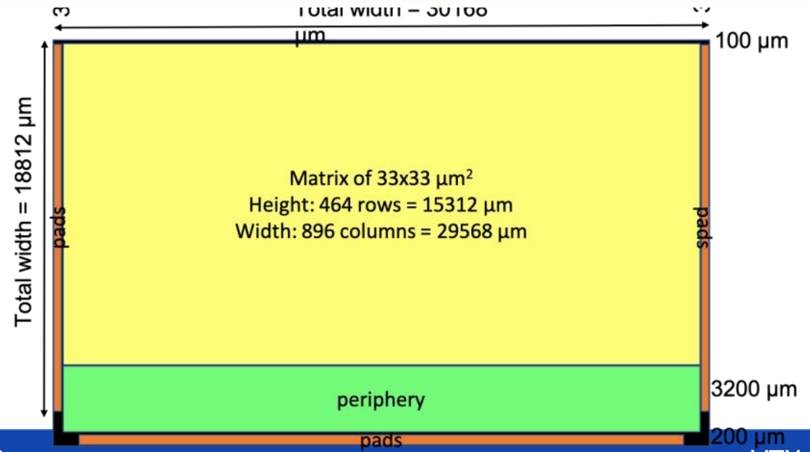


- Pixel pitch: 33.04 × 33.04 µm²
- Pixel matrix: 2 × 2 cm² chip , 512 × 512 pixels
- 4 pixel Front-End (FE) flavors with differences in pre-amplifier, sensor coupling and biasing
  - Normal FE
  - Cascode FE
  - HV Cascode FE
  - HV FE
- Two columns for Analog Monitoring
- Flavor need to be decided for OBELIX
  - Test done in Bonn, Pisa, HEPHY, CPPM, Göttingen, IPHC
  - Detailed information for this part, refer to Lars' talk

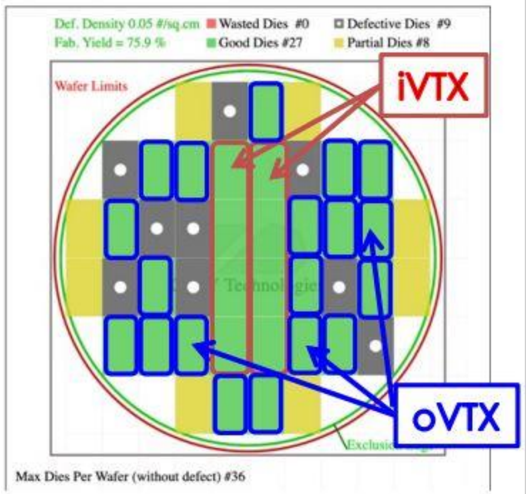
The OBELIX Design

The **O**ptimized **BEL**le II p**IX**el sensor



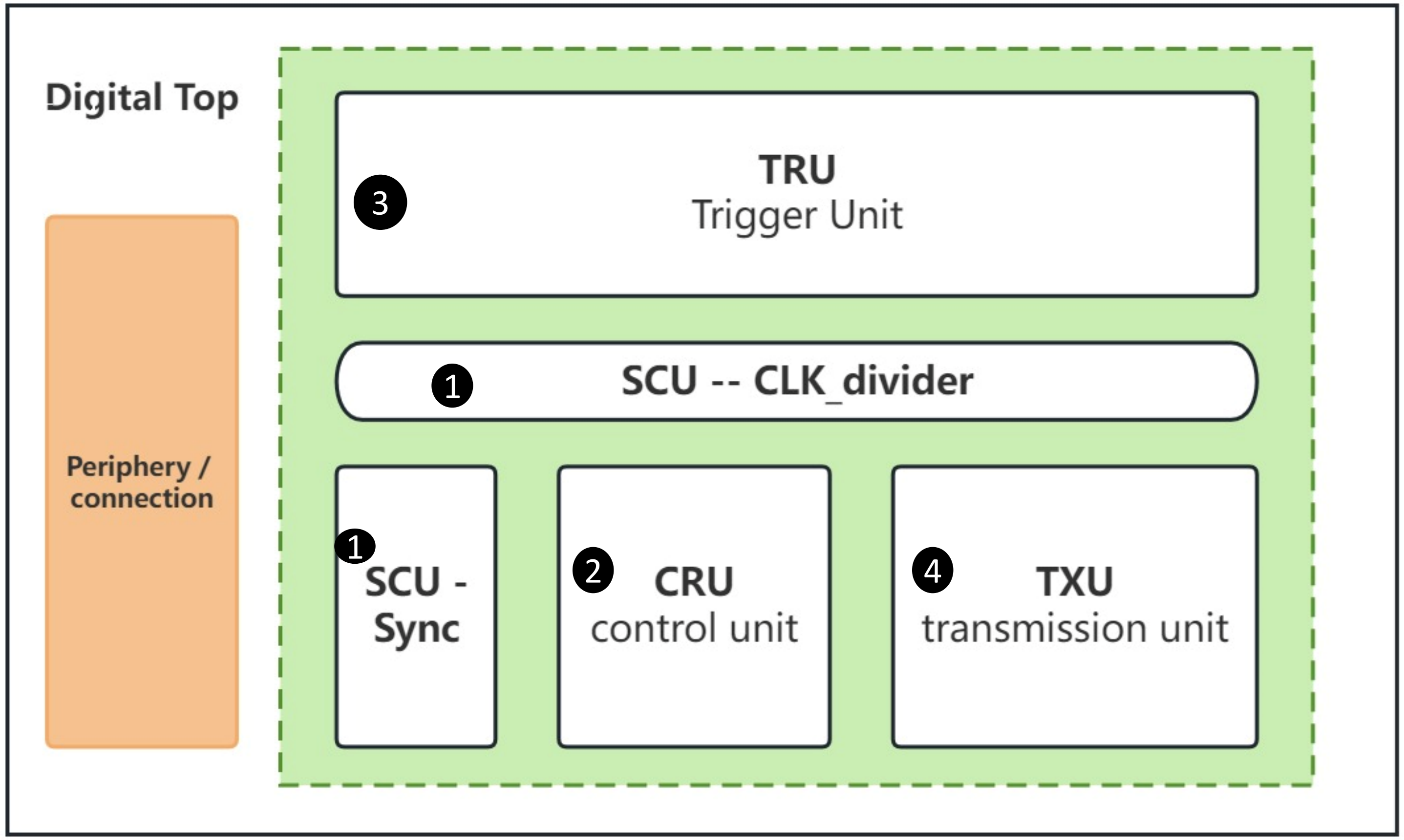


- Main design based on the TJ-Monopix2 chip with TJ180nm
- Chip size optimized to maximize the number of 4 contiguous sensor
- **Pixel Matrix**
  - Transplant from TJ-Monopix2 – radiation tolerance granted
  - Possible power optimisation
  - Freq 10-30MHz
- **New digital periphery**
  - New EoC adapted to Belle II trigger – 30KHz & with 5-10µs latency
  - Main Clk at 160MHz, Single output at 320Mb/s
  - Signal digitization: ToT (7 bits, 20 MHz)
  - RD53B* control protocol
- **Power Pads**
  - Power regulator added
  - Simplified system integration



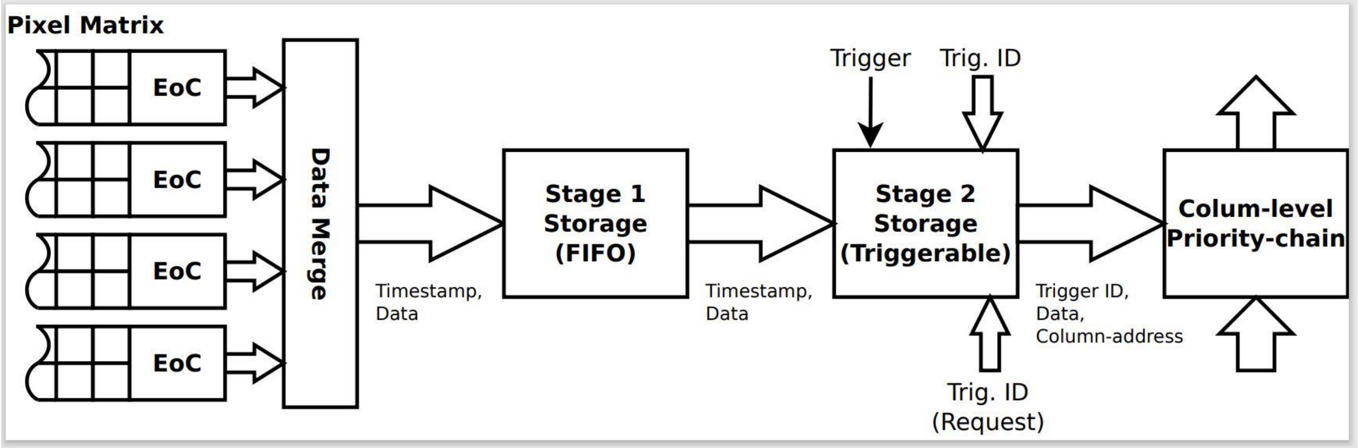
- **RD53B protocol:**
- [RD53B users guide - CERN Document Server]

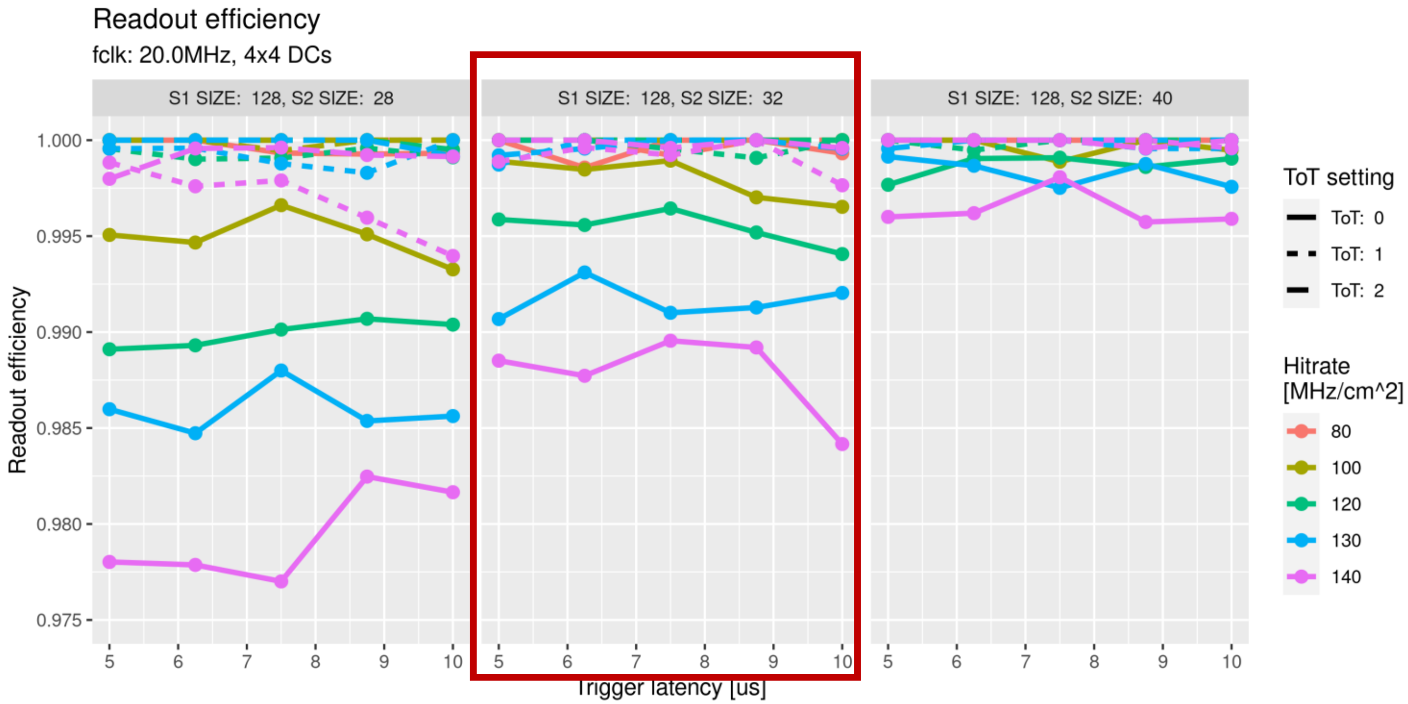
The OBELIX Design



- Module division : 4 main parts
- ❶**SCU – sync & clk divider**: digital clk divider, synchronize circuit & clk divider, RxDat format conversion, main function: clock divider, Rx_data SIPO synchronization
- ❷**CRU – Control Unit**: Implementation RD53B interface, which almost keeps the same design as TJ-MONOPIX II, main functions: command decoder, global configuration
- ❸**TRU – Trigger Unit**:Manage pixel data from the matrix-EOC and wait for the trigger to pick them for output
- ❹**TXU – TX Unit**: generate output data and sequential output, main functions: data framing, serializer

TRU: trigger unit





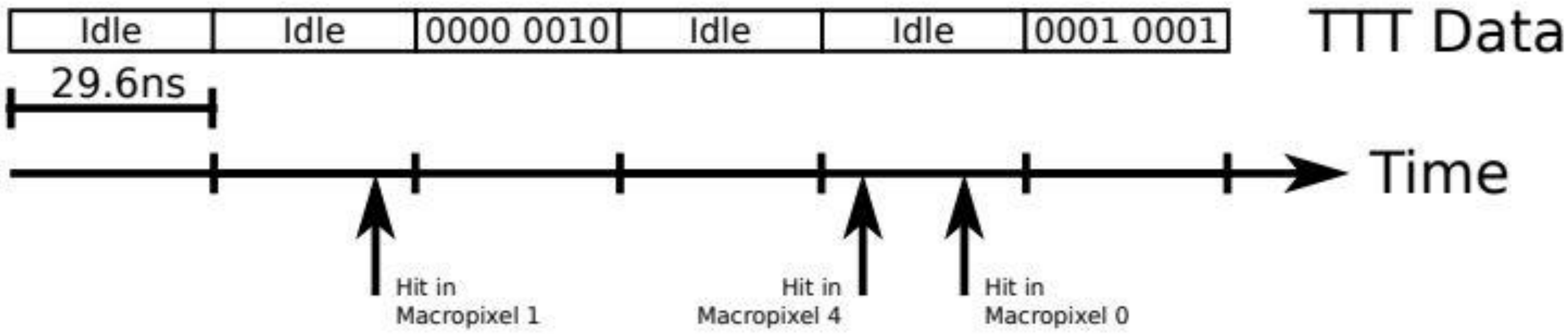
Trigger Unit

- A large secondary trigger
- New End-of-column adapted to Belle II trigger
- Timestamped hits stored in memories
- Read-out when timestamps matched with trigger
- Trigger Groups(TRGs) simply process the pixel data to generate BCID packets
- Trigger memory organized in 112 TRGs, each connected to 4 DCs(EoC)

TRU simulation:

- Simulation included: hit clustering, ToT vs charge
- Trigger latency between 5-10µs
- Can cover hit rate 120MHz/cm^2

TTT: track trigger transmission

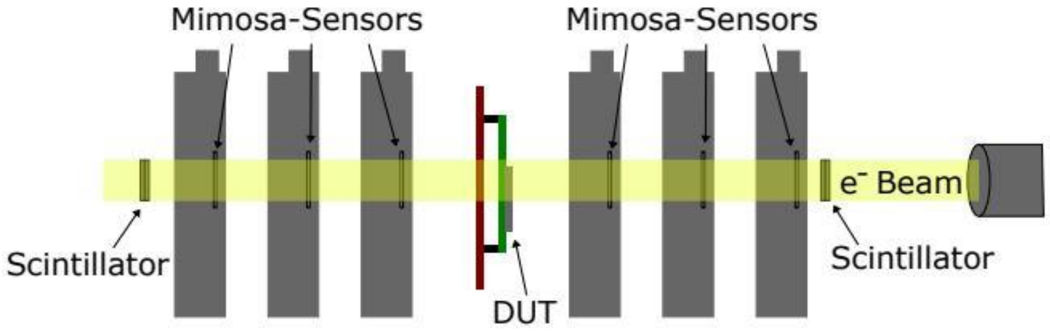


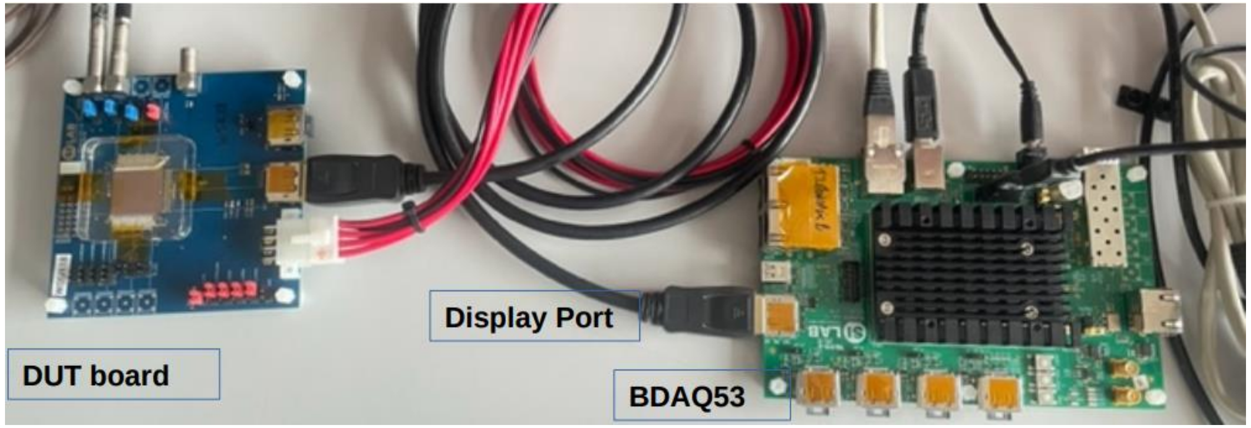
New trigger features TTT : Track Trigger Transmission

- Quickly provide the coarse pixel information of all hits to trigger of Belle II
- Allows a Belle II-trigger based on track information
- Low transmission latency required
- Separate transmission logic independent from normal OBELIX readout system (extra LVDS link)
- Power constrains this function to the oVTX
- 2 to 8 logical macropixels per whole chip (configurable, 8 used for simulation)
- 160MHz DDR transmission(320Mb/s, 8b/10b encoded)

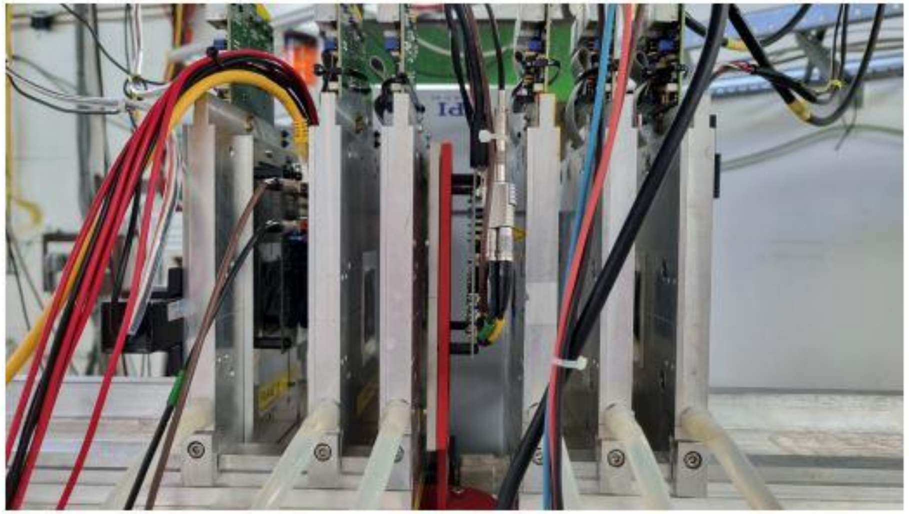
TJ-Monopix2 Test

- TJ-Monopix2 test :
  - **Full chacterization** on bench: threshold scans, calibrations
  - **Test-beams**@DESY: Efficiency/Resolution measurements
  - Radiation hardness (NIEL and TID irradiation campaigns in progress)





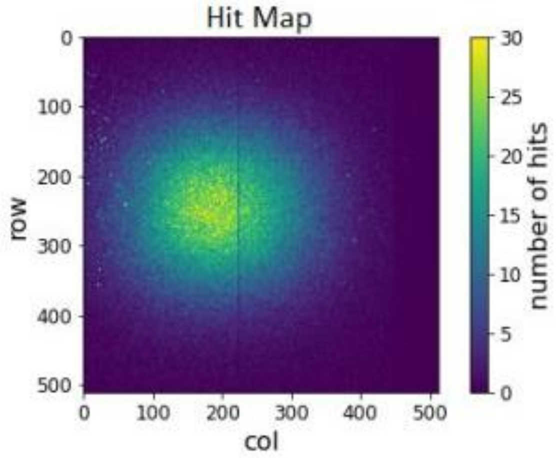
Setup for BDAQ53 Test – developed by Bonn

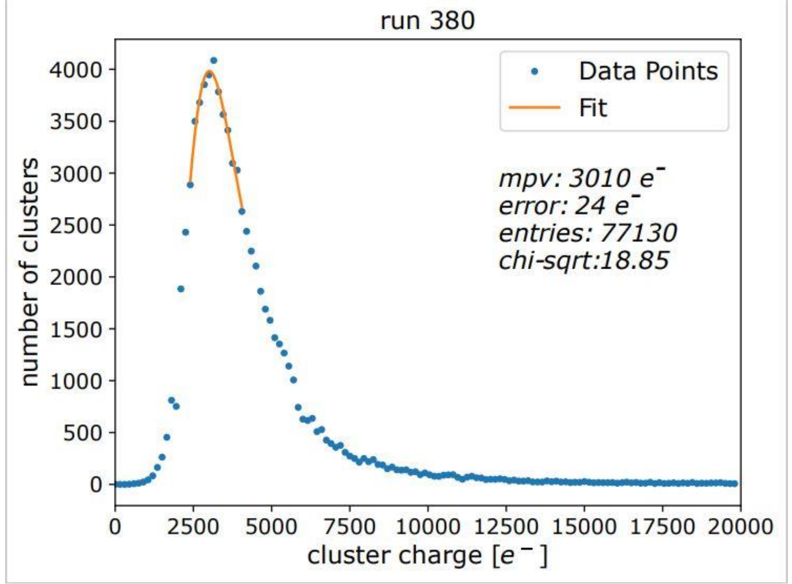


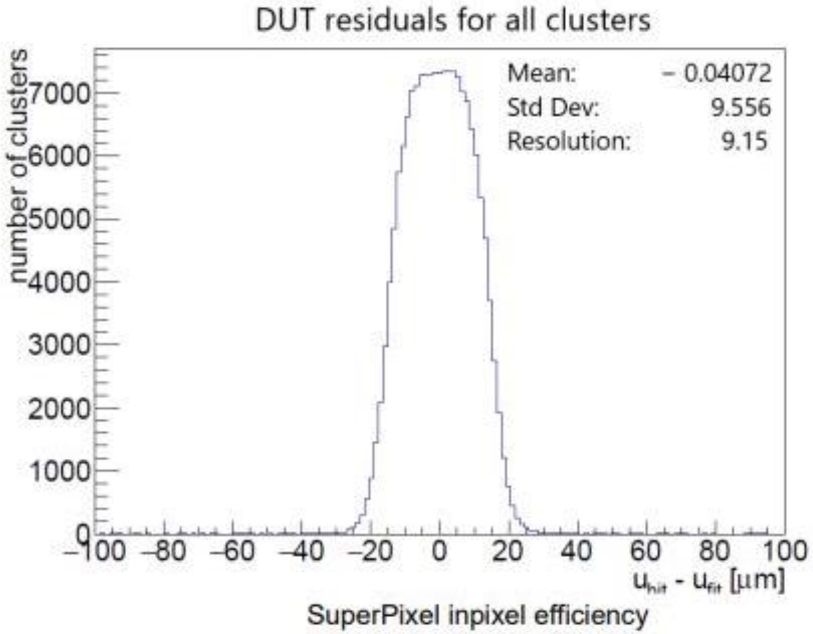
Setup for testbeam – @Desy

Test Beam Results

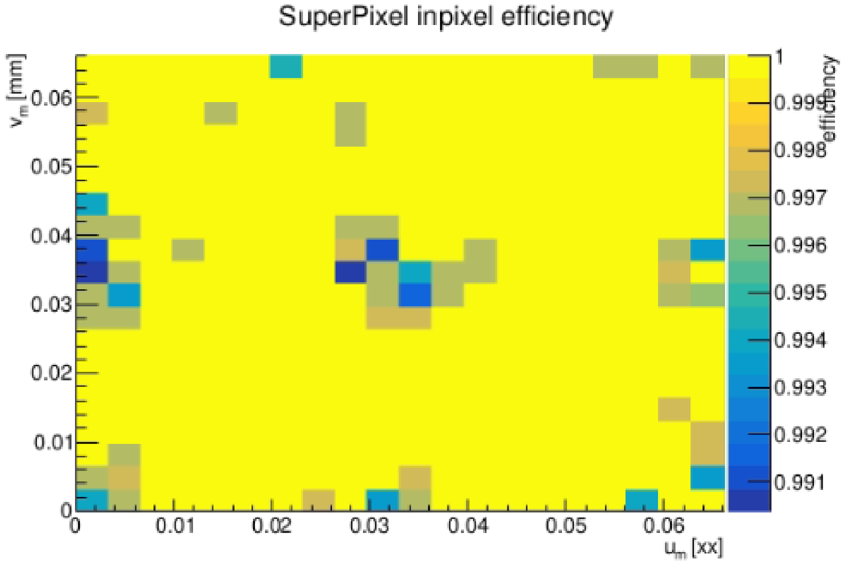
- Performed at DESY in June 2022:
  - Unirradiated chips
  - Preliminary settings used, beam e^- at around 5GeV
  - Use very high threshold ~ 550 e^-
  - Hit efficiency : 99.54 +- 0.04%
  - Cluster position residuals: 9.15 µm

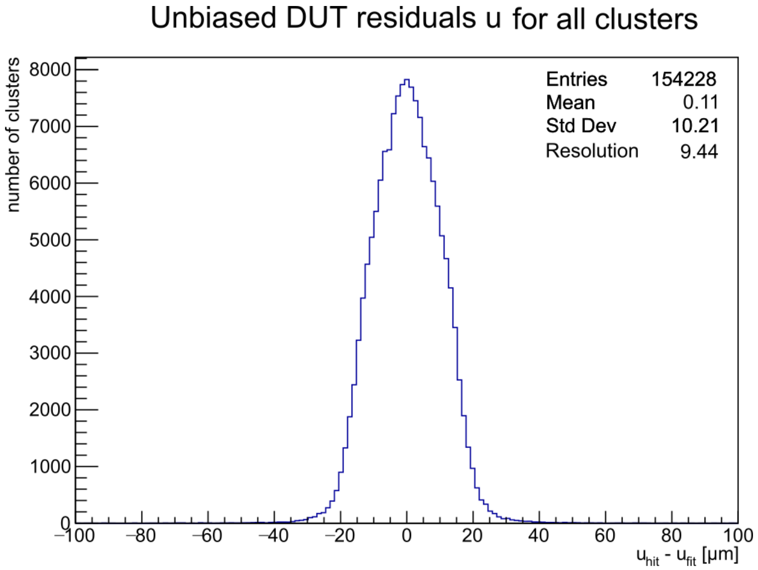






Test Beam Results

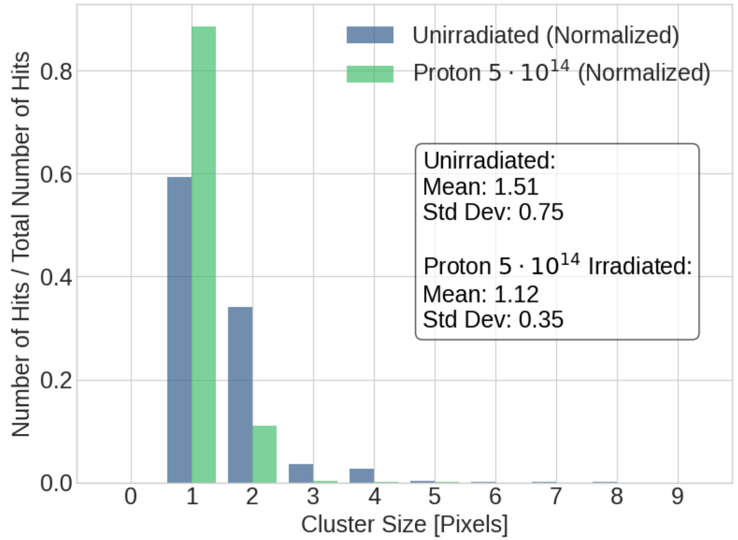




- New test beam in July 2023:
  - Lower threshold settings
  - Irradiated chips
  - Angle scan
- Data analysis on-going

Some preliminary results shown for the irradiated chip at 5* 10^{14} n_{eq}/cm^2

  - Measurements at ~ 310e^- threshold
  - Efficiency of 99.79% for irradiated chip, with small inefficiency in the pixel corners
  - Cluster position residuals : 9.44 µm -> about pitch/√12 ~ 9.5 µm binary resolution
  - Decrease in cluster size after irradiation



W02R05
W05R16

Conclusions

- The new DMAPS VTX will improve the performance of the Belle II vertex detector
- The OBELIX chip is based on the TJ-Monopix2 with TJ180nm technology
- The careful characterization of the TJ-Monopix2 sensor matrix is the key point for the OBELIX design
- Stable module operation over long times and irradiated sensor performance validated in testbeam

Outlook

- Analysis of testbeam with irradiated sensors in July 2023 at DESY
- The OBELIX design is in development, with the aim of submitting in Q4 2023 / Q1 2024
- Will contribute to a conceptual design report (CDR) for the Belle II upgrade by Q4 2023 / Q1 2024

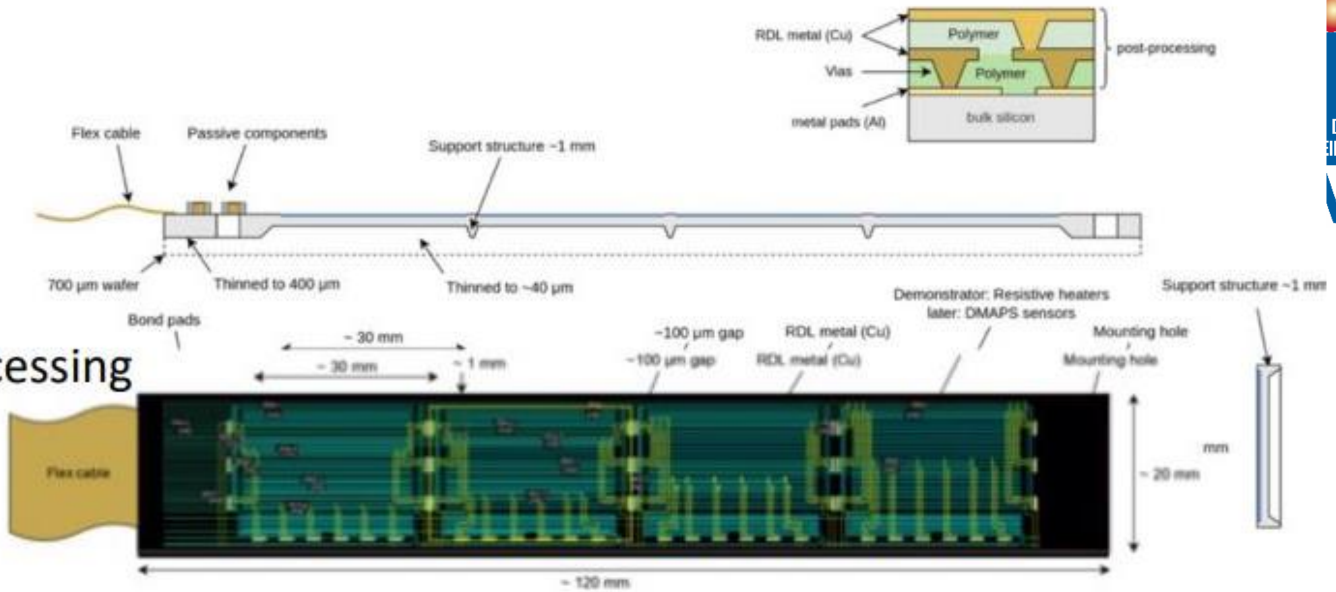
Thanks for your attention

Back up slides

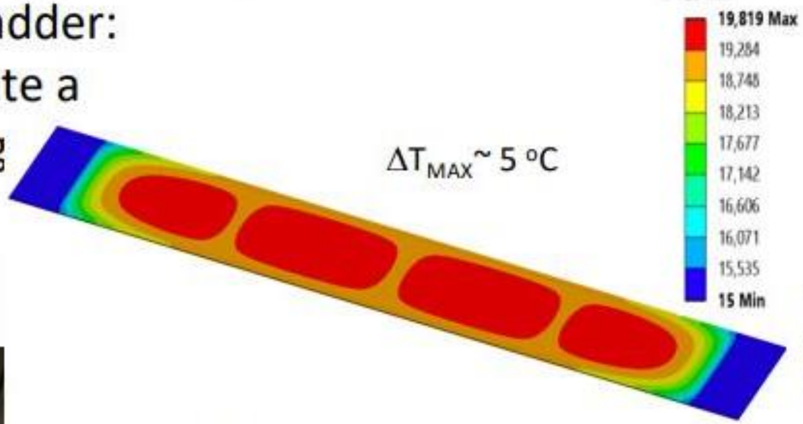
iVTX Demonstrator

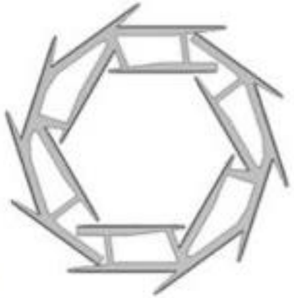
All-Silicon module concept:

- 4 contiguous sensor block diced
- Hetherogeneous thinning for stiffness
- To interconnet sensors on the ladder, a post processing step etches metal strip on the redistribution layer (prototypes in production by IZM-Berlin)

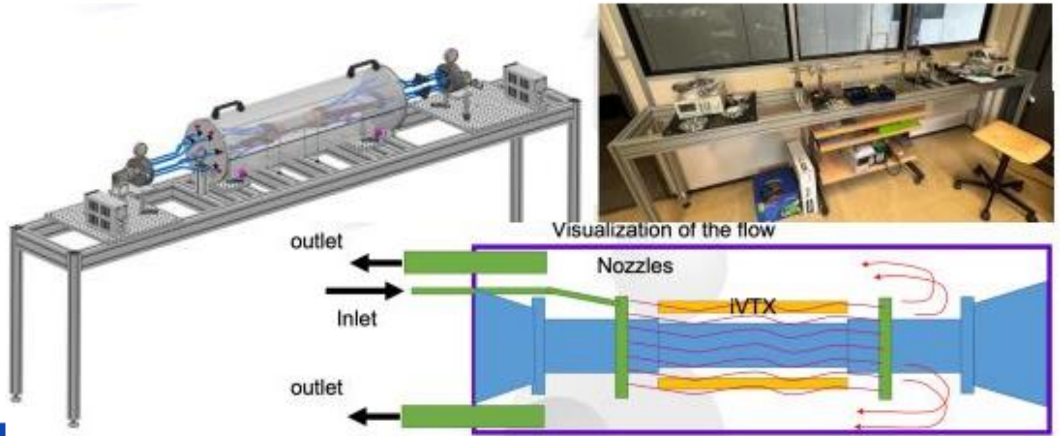


Results from air-cooling simulations on a single ladder: air at 15°C with speed ~10 m/s needed to evacuate a uniform power density of 200 mW/cm^2, reaching a max. temperature of 20°C.





Windmill support structure radii =14 + 22 mm



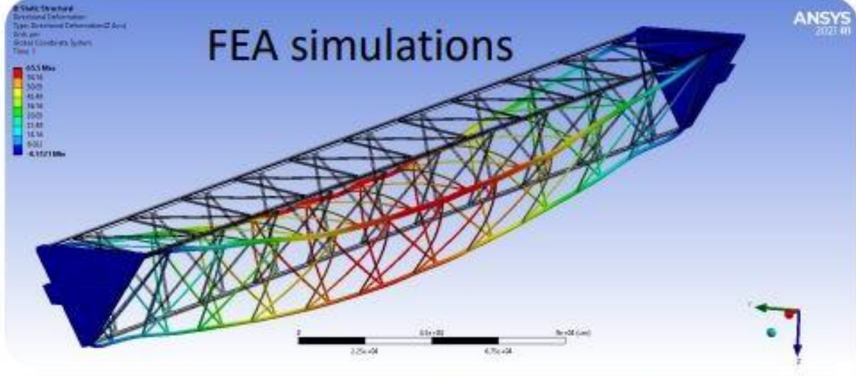
Under set-up @IJCLab (Paris) a test-bench facility to evaluate the efficiency of an air-cooling system for the whole iVTX detector (P~80 W):

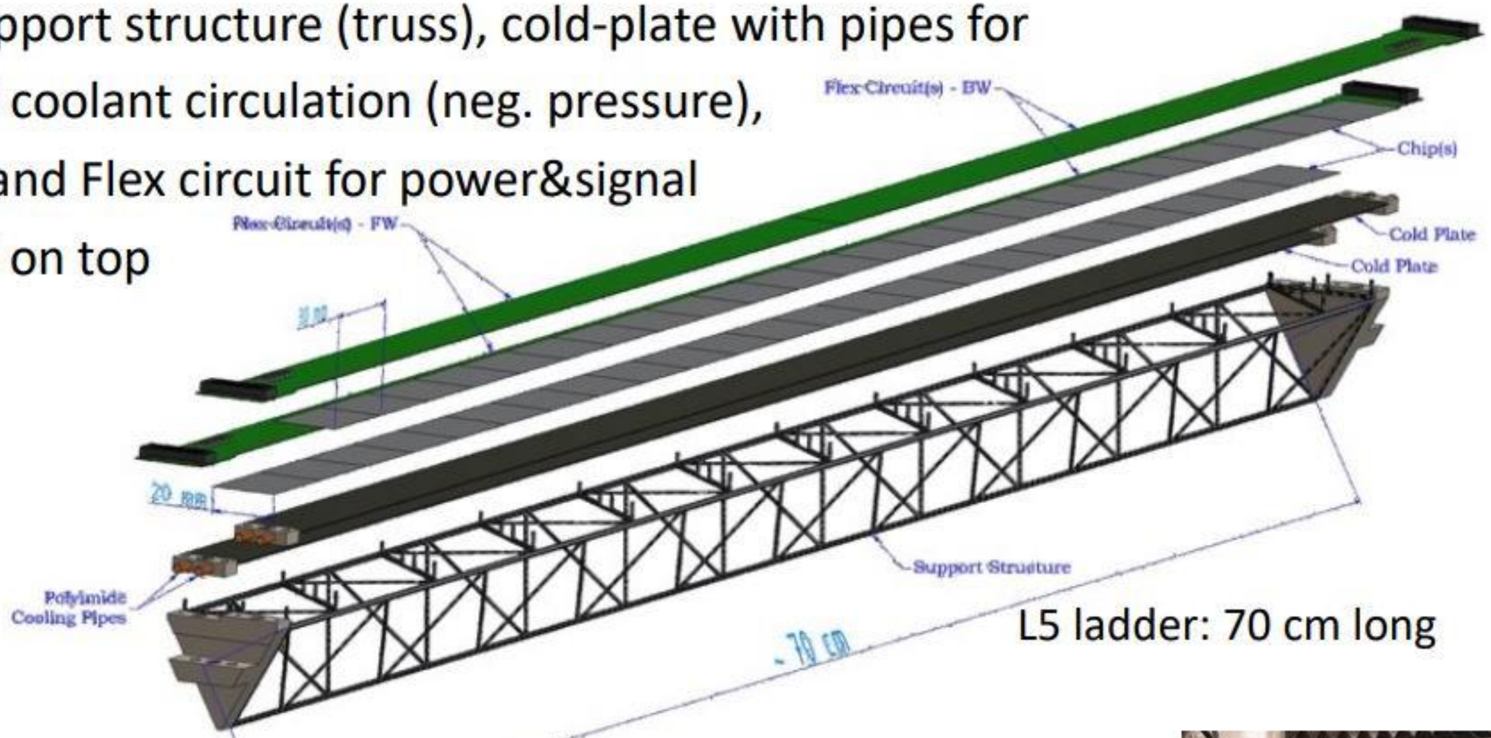
- heat exchange by convection
- air flow through the actual iVTX geometry
- mechanical vibrations with v_{air}~10 m/s to be measured.

oVTX Thermomechanics

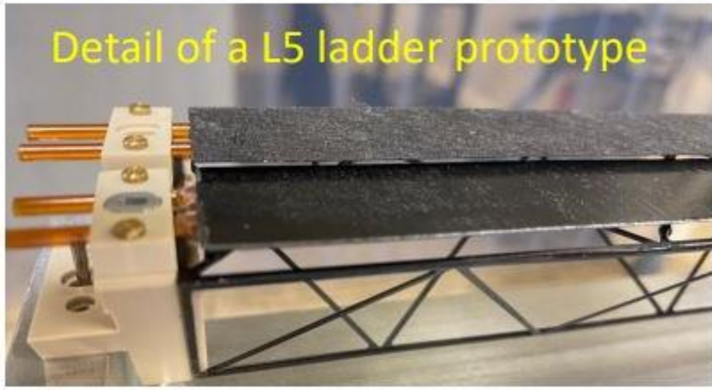
Ladder structure design inspired by ALICE ITS2, composed of:

CF support structure (truss), cold-plate with pipes for liquid coolant circulation (neg. pressure), Chip and Flex circuit for power&signal glued on top





L5 ladder: 70 cm long

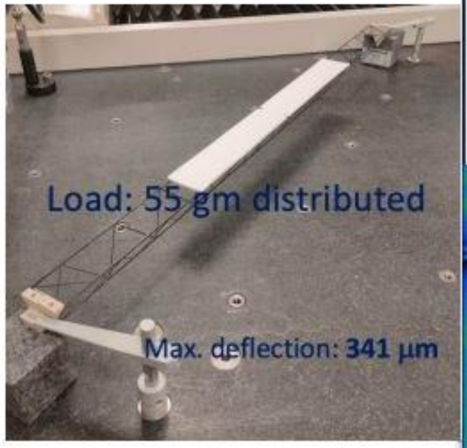


Performed mechanical characterization of the L5 prototype:

- Distortion: measurements of sagitta (~340 um)
- Vibration: 1st resonance frequency (~250 Hz) (<< earthquake f.)

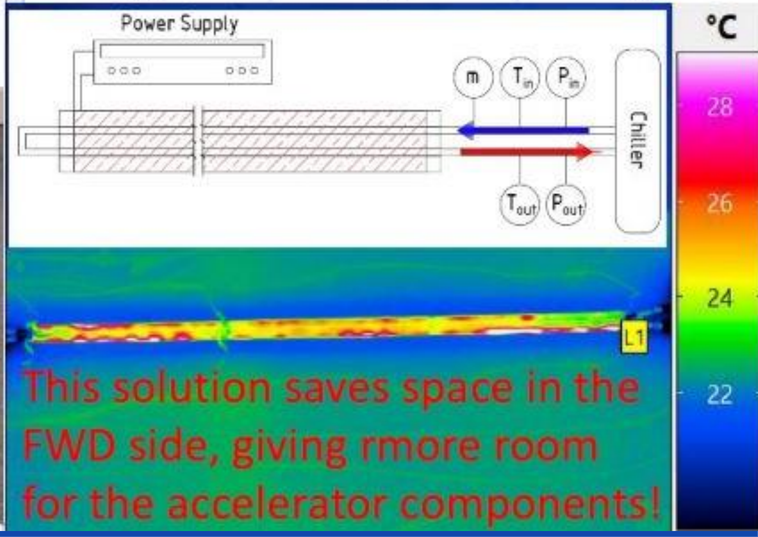
Thermal characterization:

- Used Kapton heaters, inlet (T=10°C) and outlet on one side
- Uniform temperture along the ladder ΔT max=3.3 °C



U-turn flow ΔT_{max}= 3.3 °C

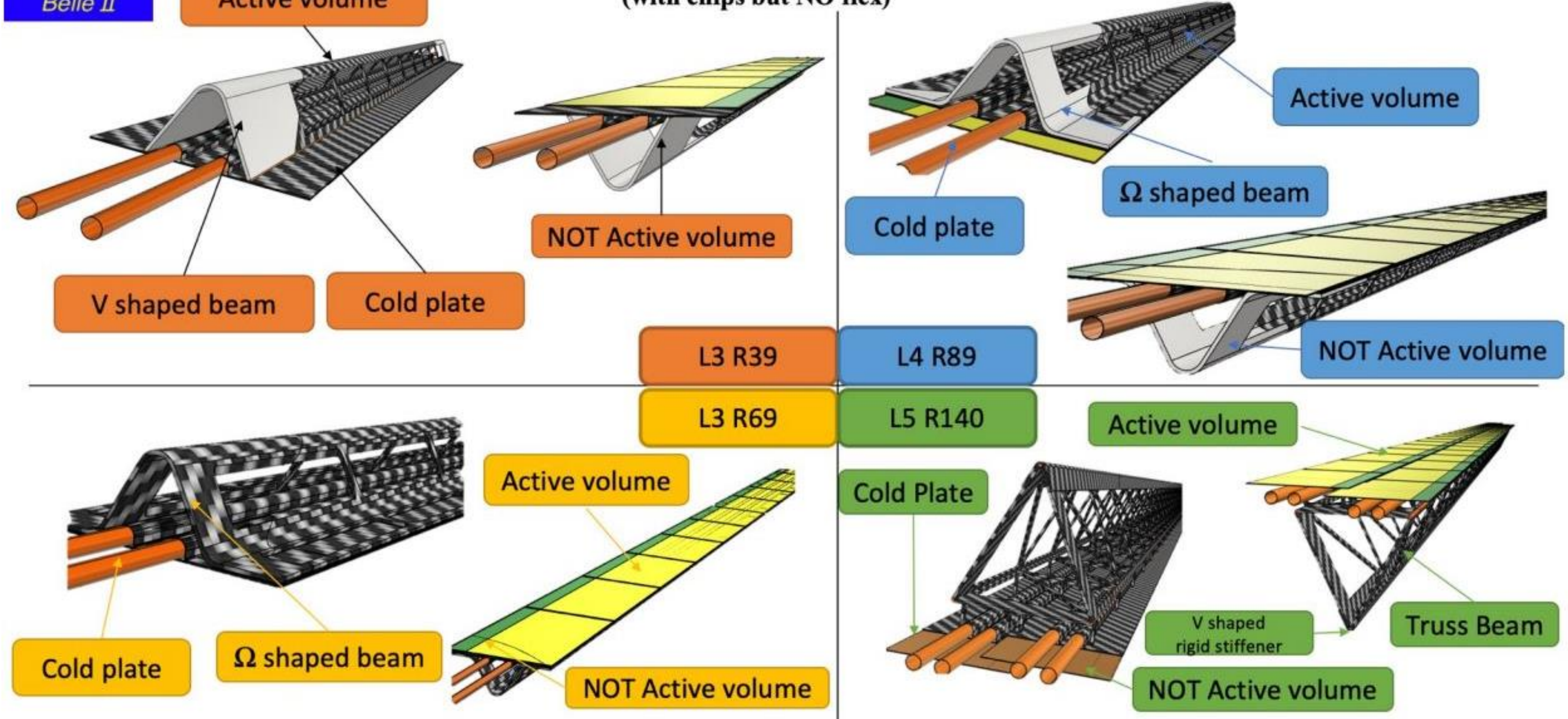
ID	Avg	Min	Max
L1	24.34	22.75	26.08



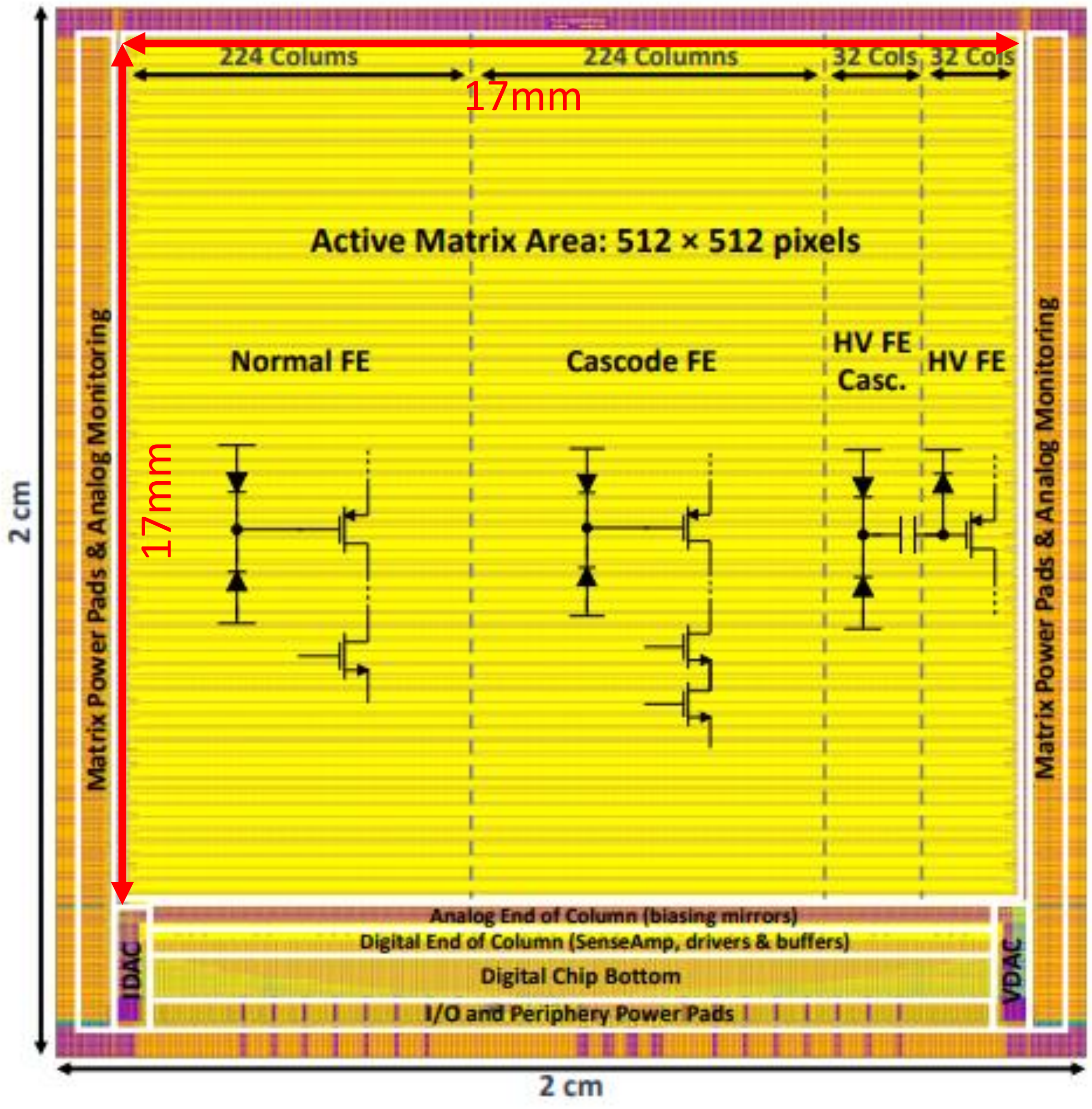
oVTX

Ladders geometry

(with chips but NO flex)



TJ-Monopix2 – pixel matrix



- 4 pixel Front-End (FE) flavors with differences in pre-amplifier, sensor coupling and biasing ;
- - Normal FE => Col_0 to Col_223

  improved TJ-Monopix I FE, DC coupled pixels
- - Cascode FE => Col_224 to Col_447

  Extra cascode transistor that increase the pre-amplifier gain, the aim is to have 50% reduction of threshold dispersion, DC coupled pixel
- - HV Cascode FE => Col_448 to Col_479

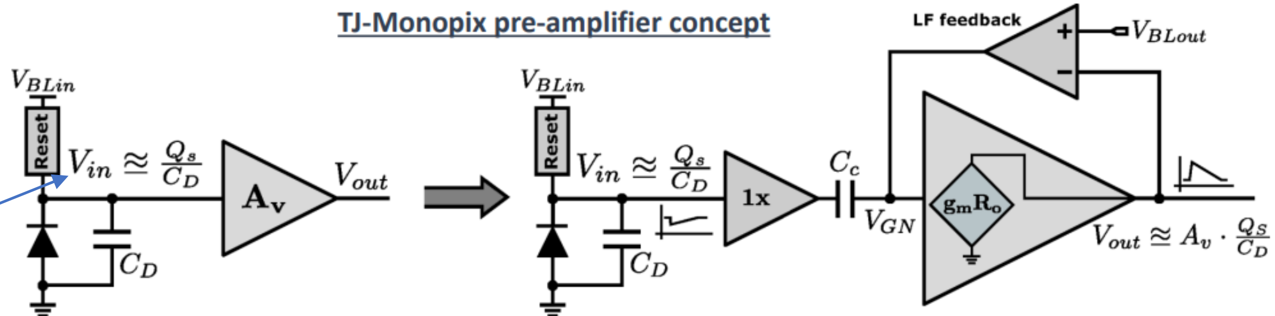
  Front side High Voltage biasing and AC coupled pixel
- - HV FE => Col_480 to Col_511

  Front side High Voltage biasing and AC coupled pixel

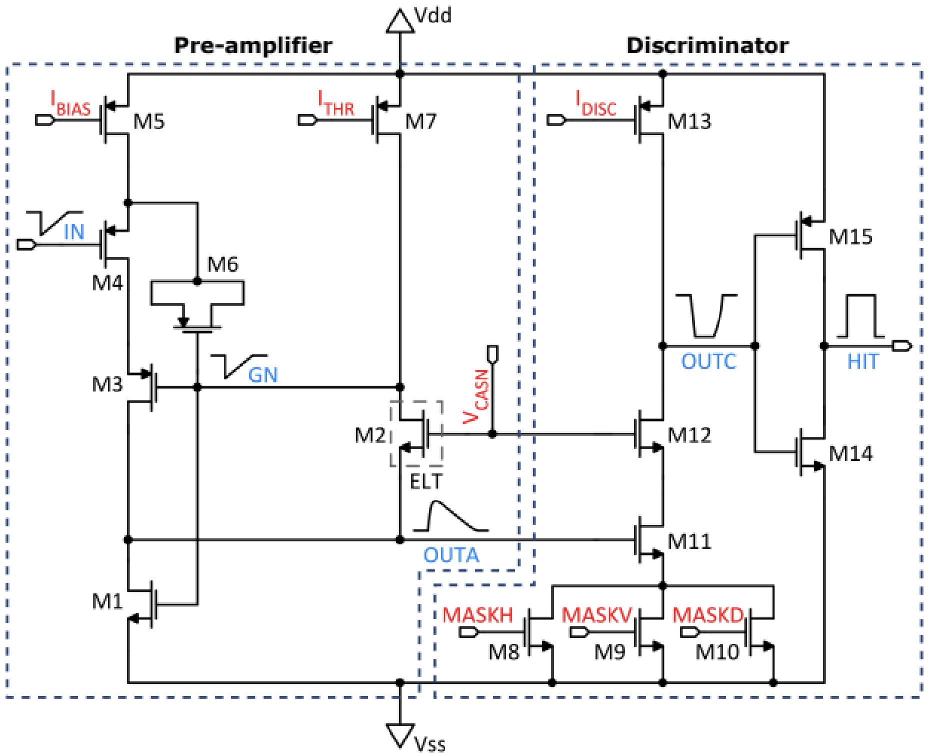
  a variation of the previous one
- Two columns for Analog Monitoring

Pixel Matrix: Analog Front End

Very low input capacitance → High input voltage

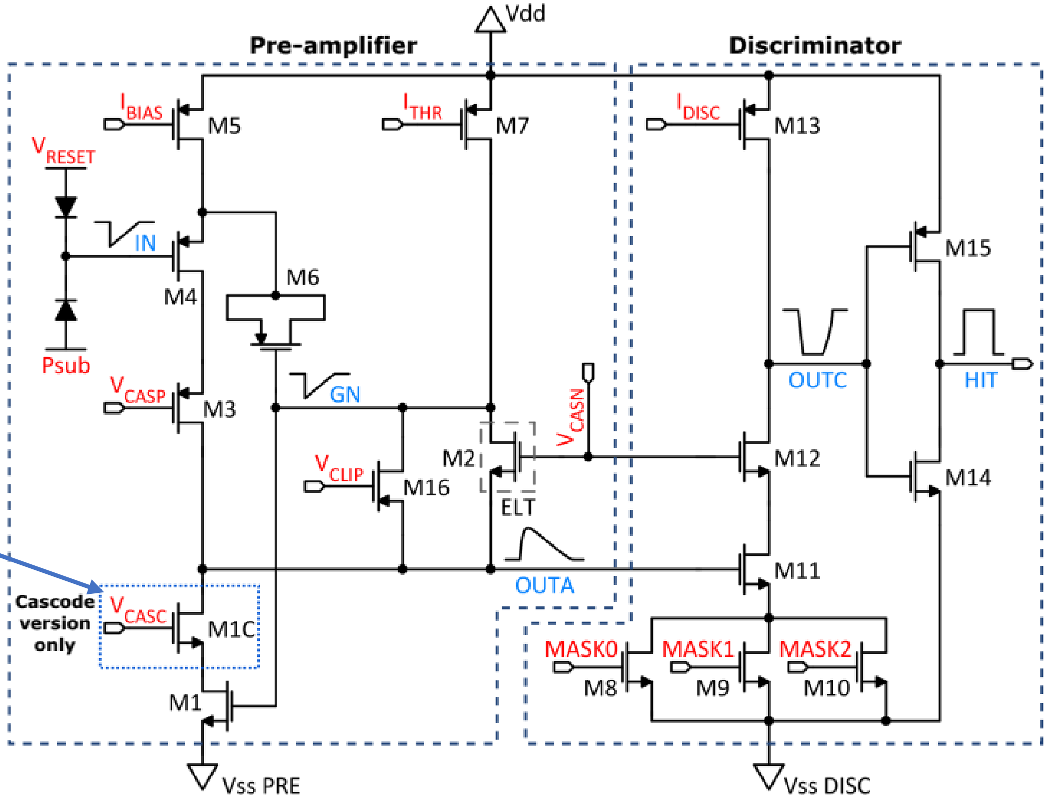


Voltage amplifier



Normal Front End Design

Cascode architecture → High gain



Cascode Front End Design

Pixel Matrix: Analog Front End simulation

Objective : Reduction of the TJ-MONOPIX2 front-end (FE) preamplifier's power consumption

Normal FE pixel preamplifier	Improved normal (FE) pixel preamplifier	Cascode FE pixel preamplifier	Improved cascode (FE_casc) pixel preamplifier
Ibias = 500 nA	**Ibias= 300 nA**	Ibias = 500 nA	**Ibias= 300 nA**
Power consumption = 1µW	**Power consumption = 650nW**	**Power consumption = 1µW**	**Power consumption =650nW**
Peaking Time = 107,48 ns	**Peaking Time = 129,46 ns**	Peaking Time = 132,85 ns	**Peaking Time = 182,34 ns**
Gain = 1,74 mV/e-	Gain = 1,53 mV/e-	**Gain = 3,35 mV/e-**	**Gain = 2,81 mV/e-**
SNR = 39,1	**SNR = 39,13**	SNR = 56	**SNR = 57,33**
ENC = 2,55 e- rms	ENC= 2,55 e- rms	ENC = 1,78 e- rms	ENC = 1,74 e- rms

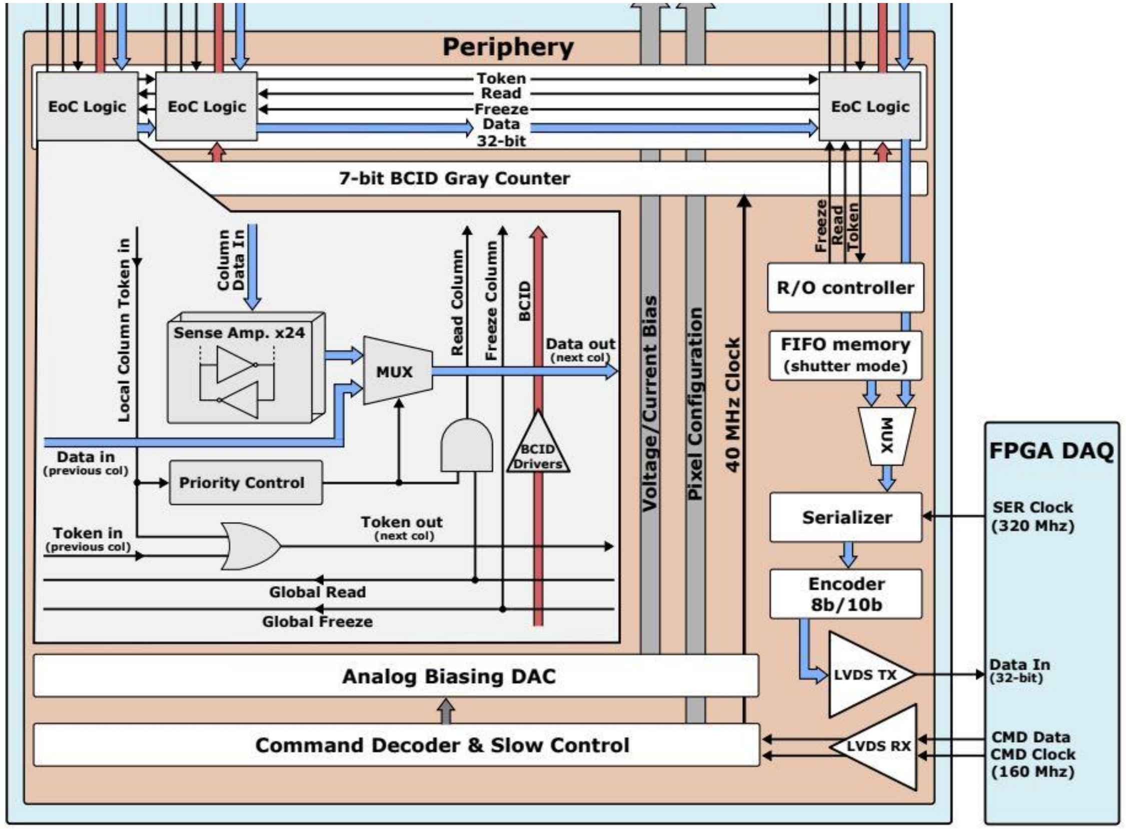
→ The power consumption can be reduced by 35%

Pixel Matrix: Analog Front End simulation

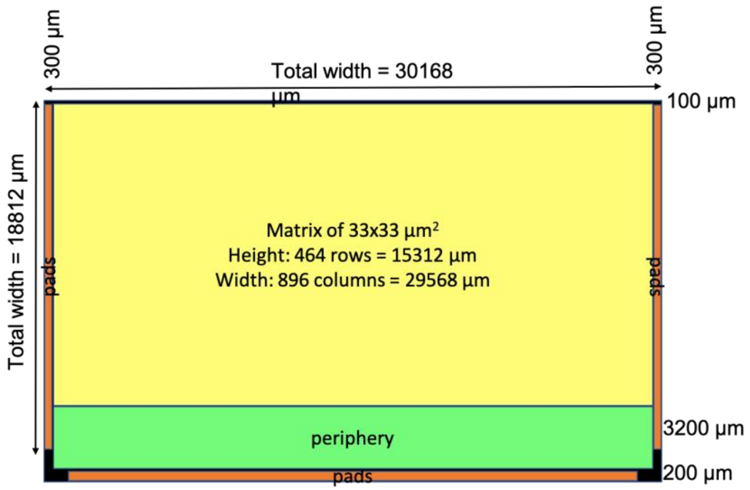
- On going : study of reducing the main biasing current in order to have low power dissipation
  - Lowering the main biasing current from 500 nA to 300 nA leads to a lowering of the power dissipation by 35% (for both Normal FE and cascode FE).
  - However by reducing the current Ibias , we have small variation on peaking time
  - The gain of the preamplifier is also reduced but it can be improved by varying the feedback current Ithr while keeping a signal-to-noise ration (SNR) as high as possible.

The cascode Front End flavor is chosen for OBELIX – so far

OBELIX_V1 : Digital Specifications of Belle II

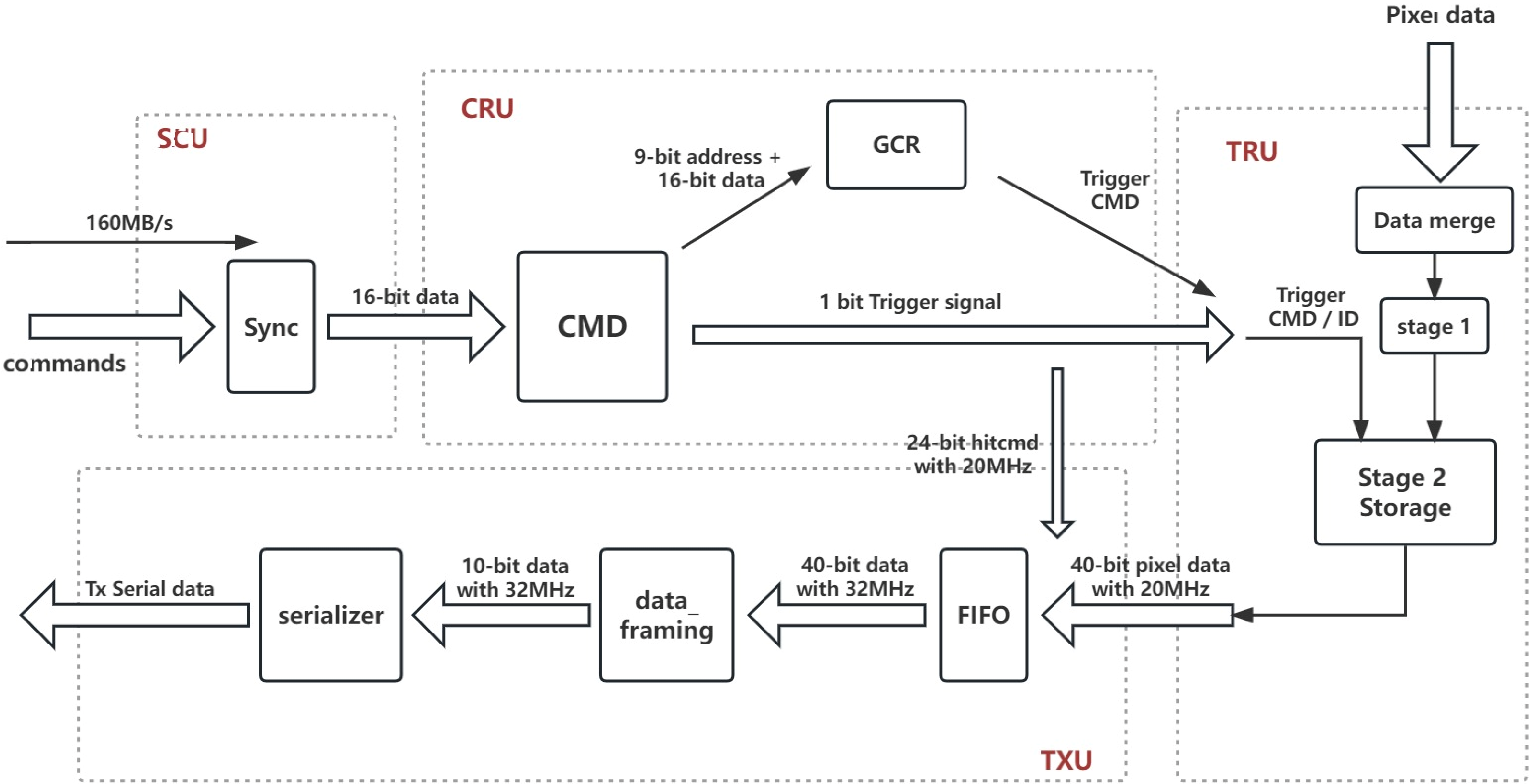


- Main specifications of digital Top
- Main clkin : **160MHz**
- General function clk : from 40MHz to **20 MHz**;
- Single output at **320Mb/s**;
- Area limitation and power consumption ;
- **New End-of-column** adapted to Belle II trigger
- - Timestamped hits stored in memories
- - Read-out when timestamps matched with trigger
- - hit rate ≤ 120MHz/cm2
- **RD53B** control protocol;

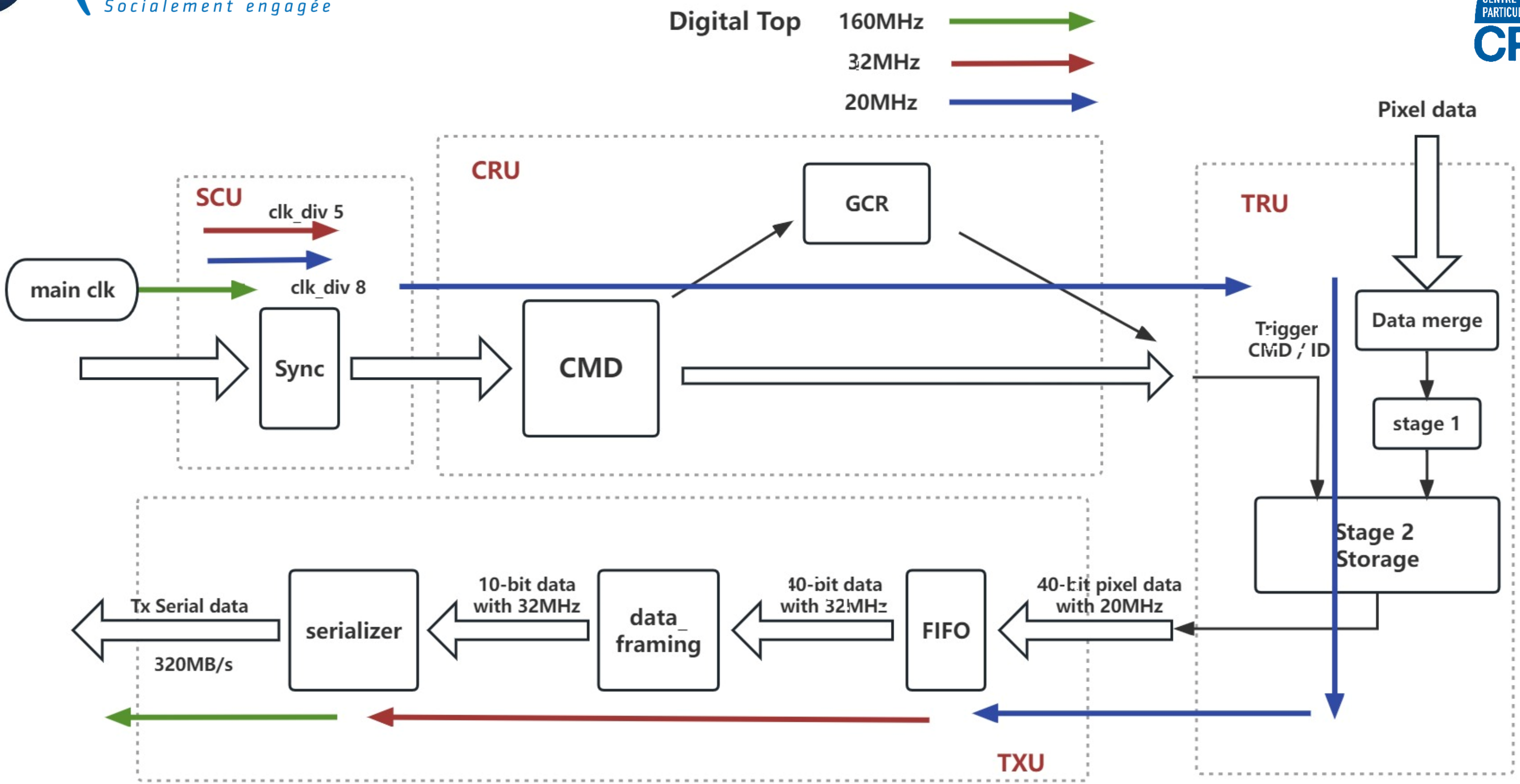


- For IO pins -- LVDS only
- Input --- ClkIn,CmdIn,TTTIn
- Output --- TTTout,DataOut, ClkOut

OBELIX_V1 : Digital Data Path

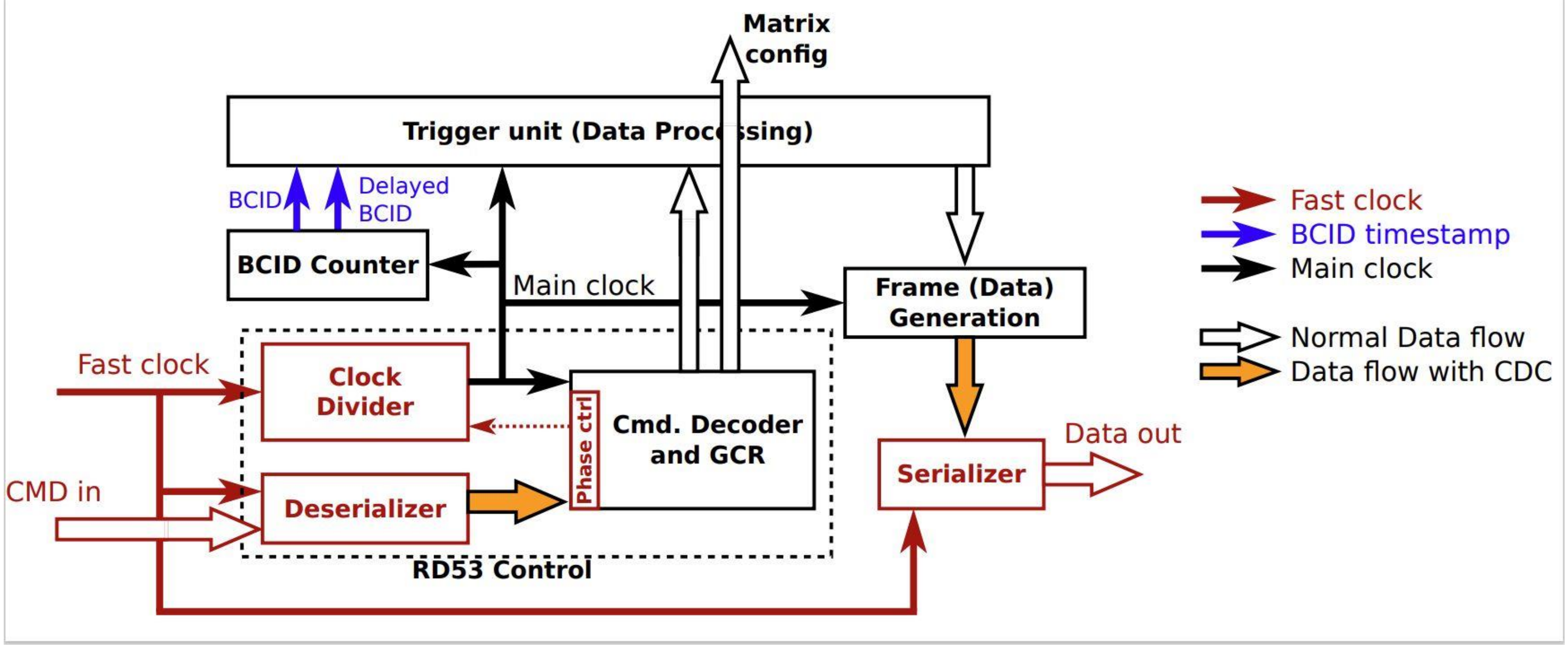


OBELIX_V1 : Digital Clock Path



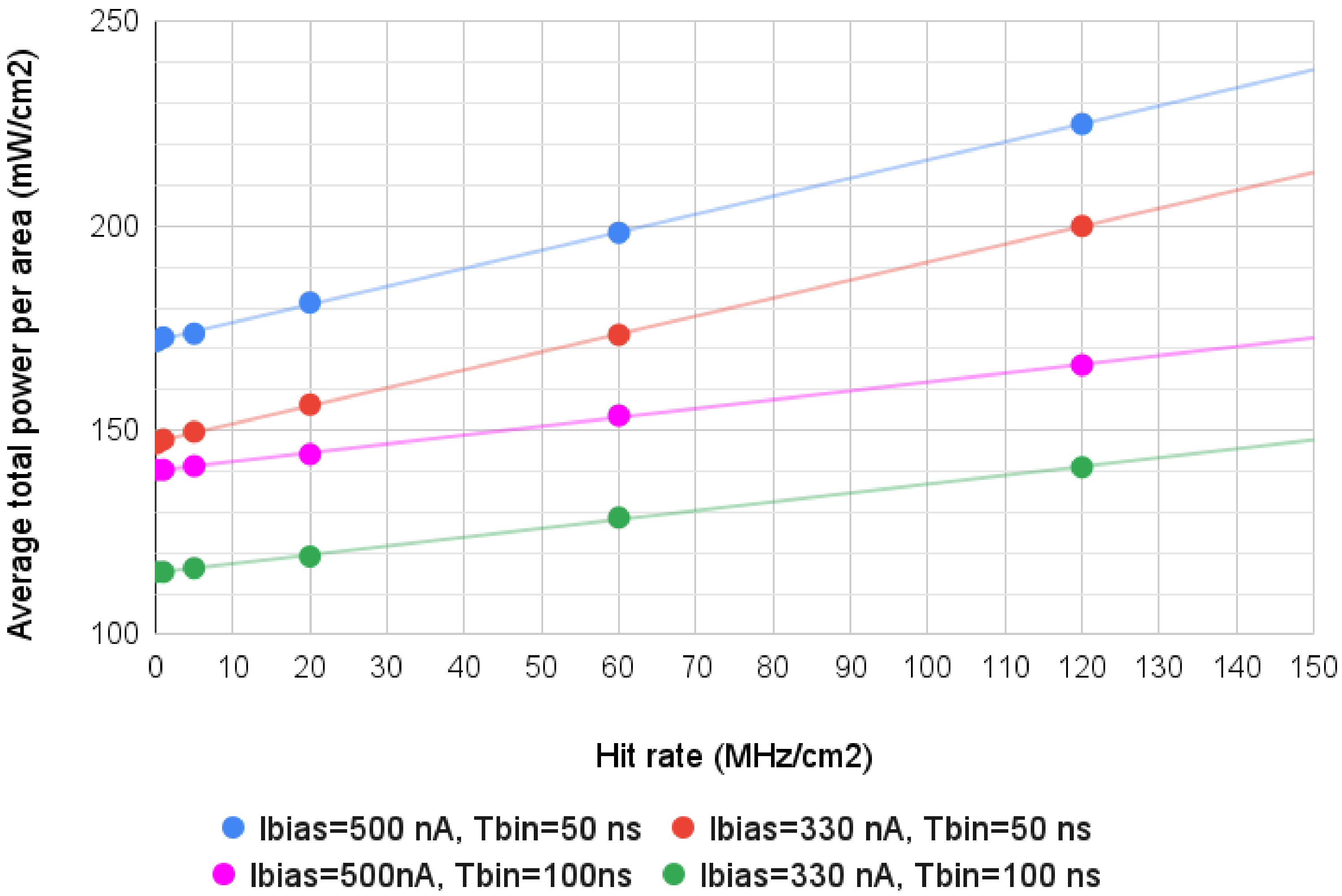
OBELIX_V1 : Digital Clock Path

Real situation



Clock Signal	Ideal	MONOPIX
Main Clock	160MHz	169.7MHz
Divider 8 Clock	20 MHz	21.2 MHz
BCID Clock	20 MHz	21.2 MHz
TXU Clock	32MHz	33.9MHz

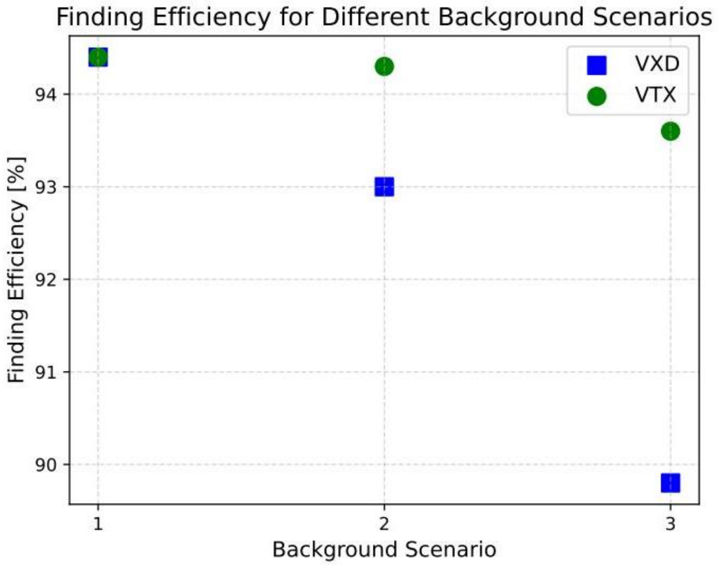
Preliminary from simulations

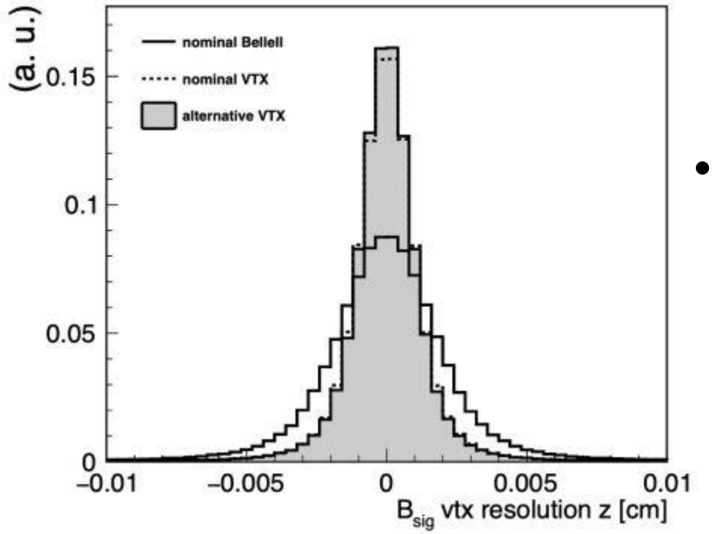


how our expected power change with hit rate for different bias and BCID clock scenarios

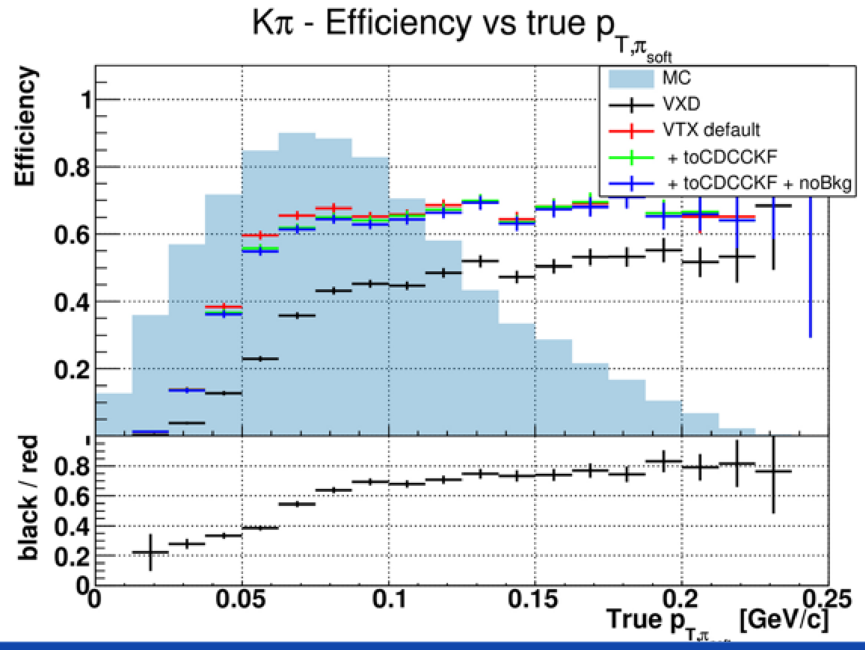
VTX simulated tracking performance

- The performance of the tracking on single tracks. The events are just coming from generic events e+ e- producing a pair of B mesons and 'generic' means that we don't care how they decay.





- VTX provides better vertex resolution than the current VXD in the decay channel B^0



- Focus only on B mesons decaying into the channel indicated.

Docs & Links :

1. All the previous presetation: [VTX talks - Belle II - DESY Confluence]
2. VTX official page: [VTX sensor - Belle II - DESY Confluence]
3. TJ-MONOPIX II: https://cds.cern.ch/record/2782279?ln=fr