Ideas for further upgrades of the CMS Inner Tracker

Duccio Abbaneo

on behalf of the CMS Tracker group

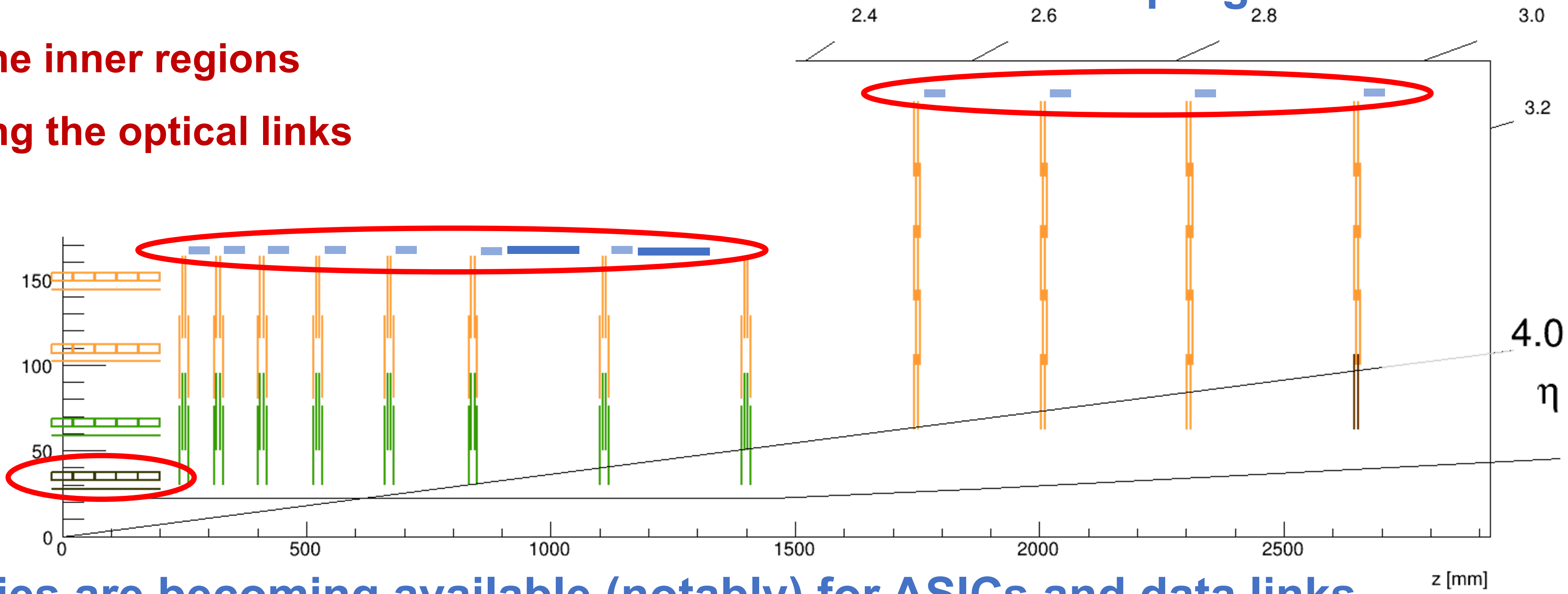
VERTEX 2023

Disclaimer

- There is no agreed plan for a further upgrade of the Inner Tracker
  - Not even within the Tracker group
- Will report some of the ideas being considered
  - Focus on requirements and constraints
  - Touch on some general concepts being explored
  - Will not discuss implementation options/details

Motivations

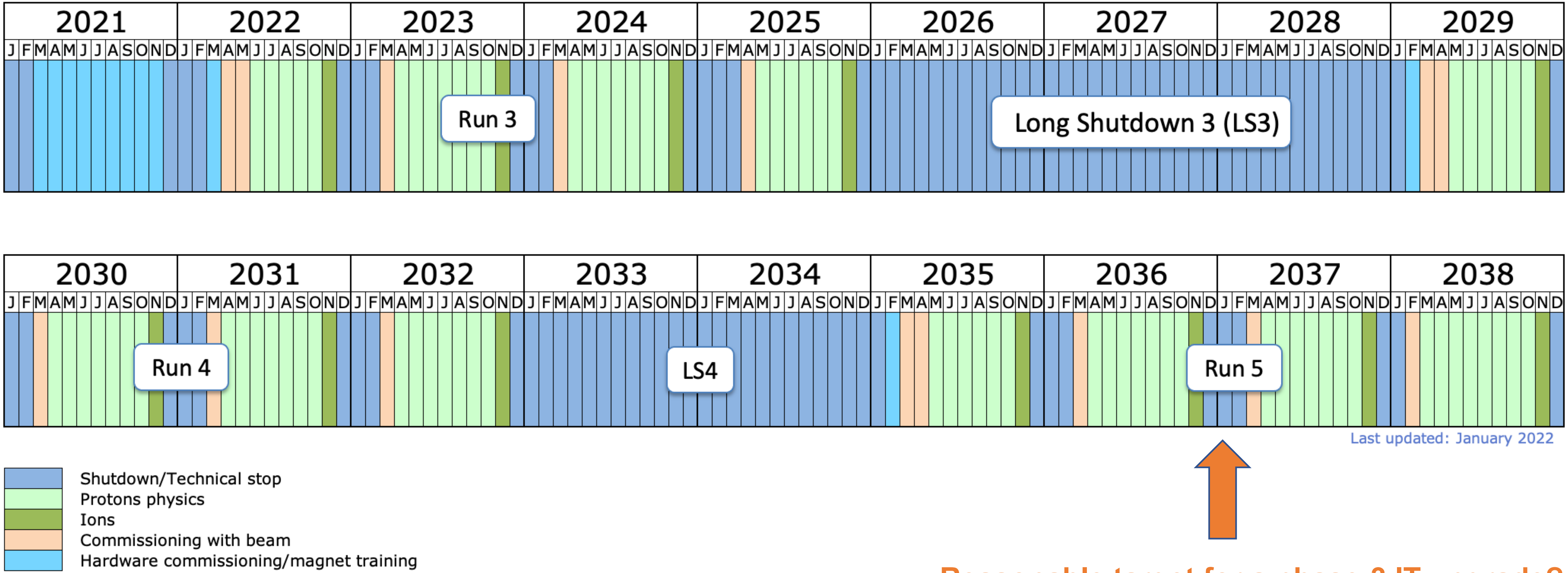
- Some parts of the Inner Tracker will not survive the entire HL-LHC program
  - Modules of the inner regions
  - Boards carring the optical links



- New technologies are becoming available (notably) for ASICs and data links
  - Limited opportunities for real applications on the horizon

- A further upgrade of the Inner Tracker may give an opportunity for an application of the ongoing developments, adding value to the HL-LHC program

Possible timeline

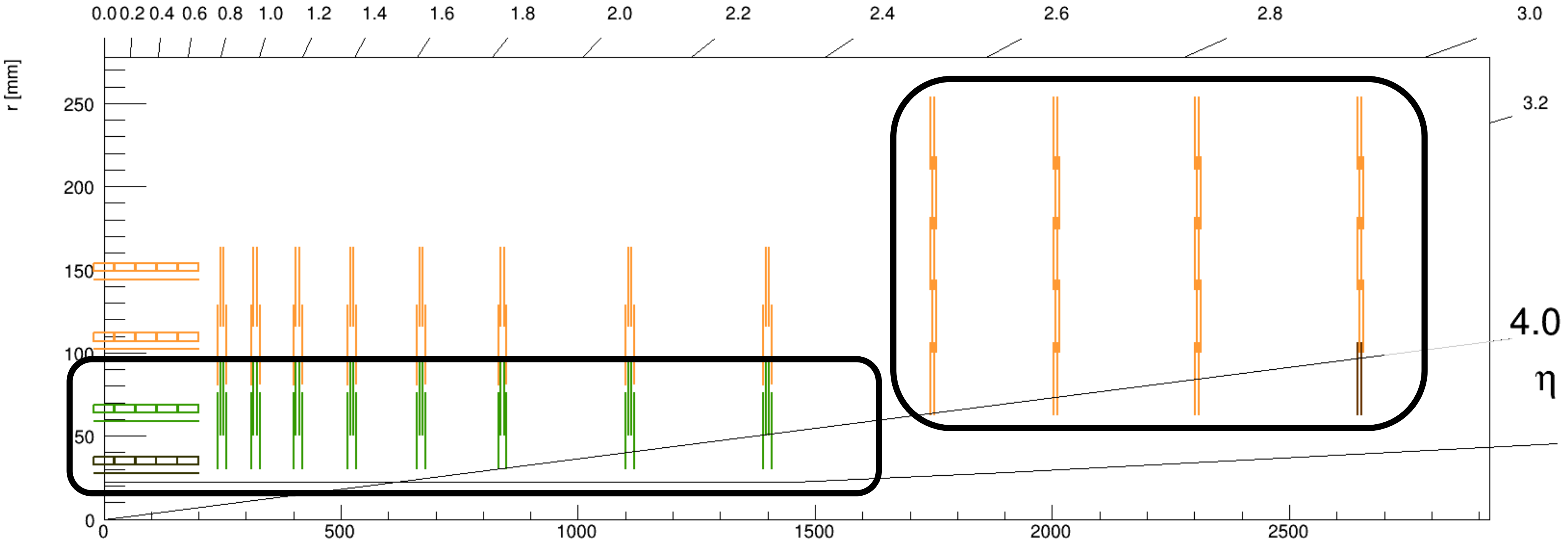


Reasonable target for a phase-3 IT upgrade?

Somewhat less than ½-way of the HL-LHC program in terms of expected luminosity
The target date may change if the HL-LHC program changes

Possible scope

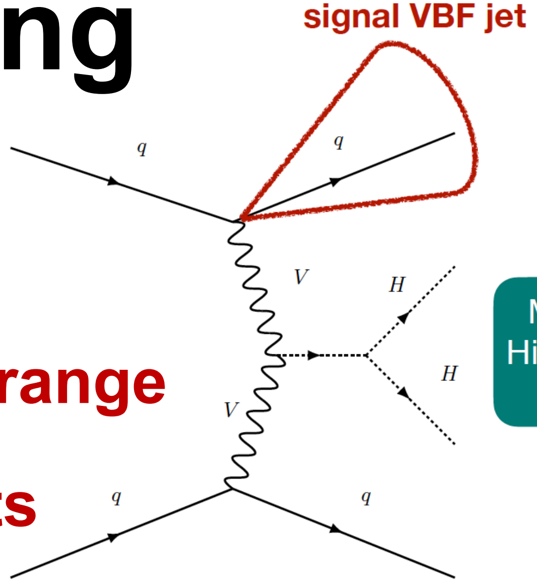
- **Improve the performance of the tracking near the IP**
  - **Re-build inner regions with more advanced technologies**
    - **Improve d_0 and z_0 resolution**
    - **Enhance pileup mitigation and b-tagging ("core business" of the Inner Tracker)**
- **Extend coverage of timing information in CMS from present $\eta \approx 3$ up to $\eta \approx 4$**
  - **Introduce one or two "timing disks" in the forward**



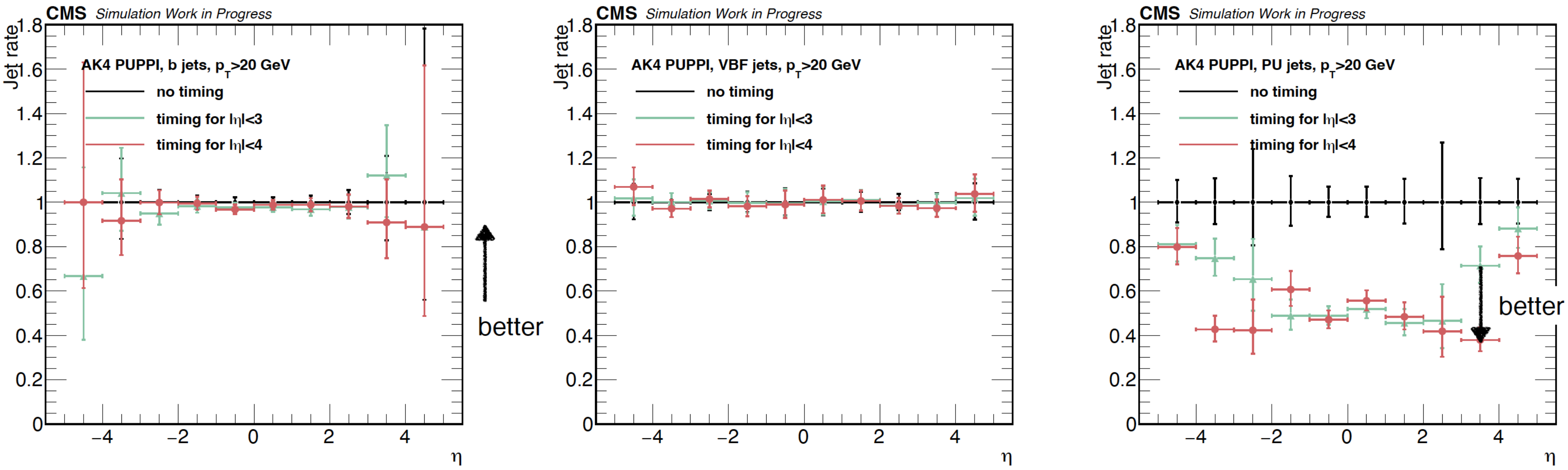
Physics case for forward timing

➢ **Measurement of Higgs self-coupling**

- ❖ **Improved background rejection in the relevant η range**
- ❖ **No significant loss of efficiency for VBF and b jets**



Measurement of Higgs self coupling at HL-LHC

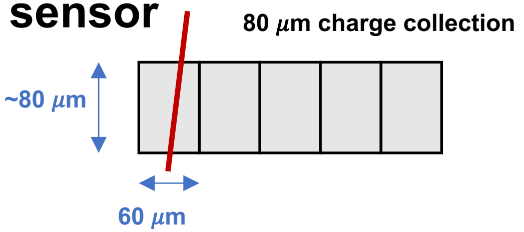


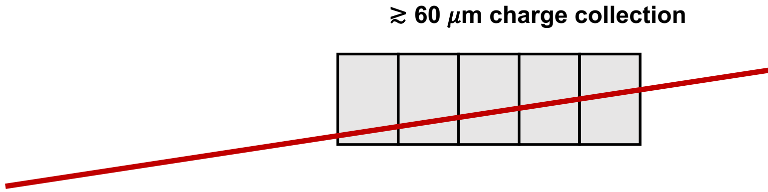
How to improve the inner regions

➢ Smaller pixels?

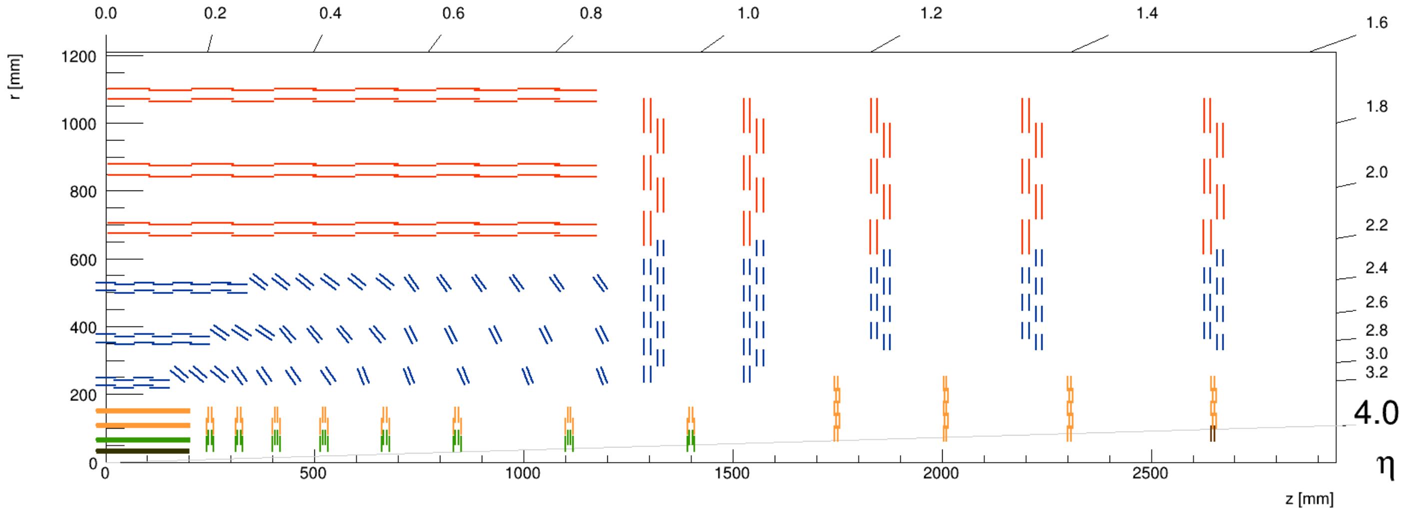
❖ Strawman layout: same concept as in phase-2, scaled down in size by ×0.6

- **25×100 μm^2 pixels ⟶ 15×60 μm^2 pixels in the sensor**
- **Some ~ 80 μm active thickness**
- **Detection threshold and TOT precision scale accordingly**

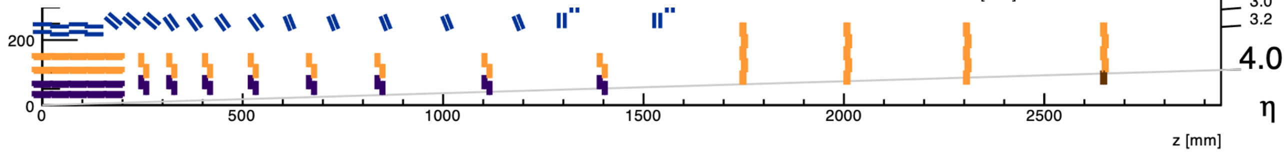




rϕ × y =
25 µm × 100 µm
everywhere



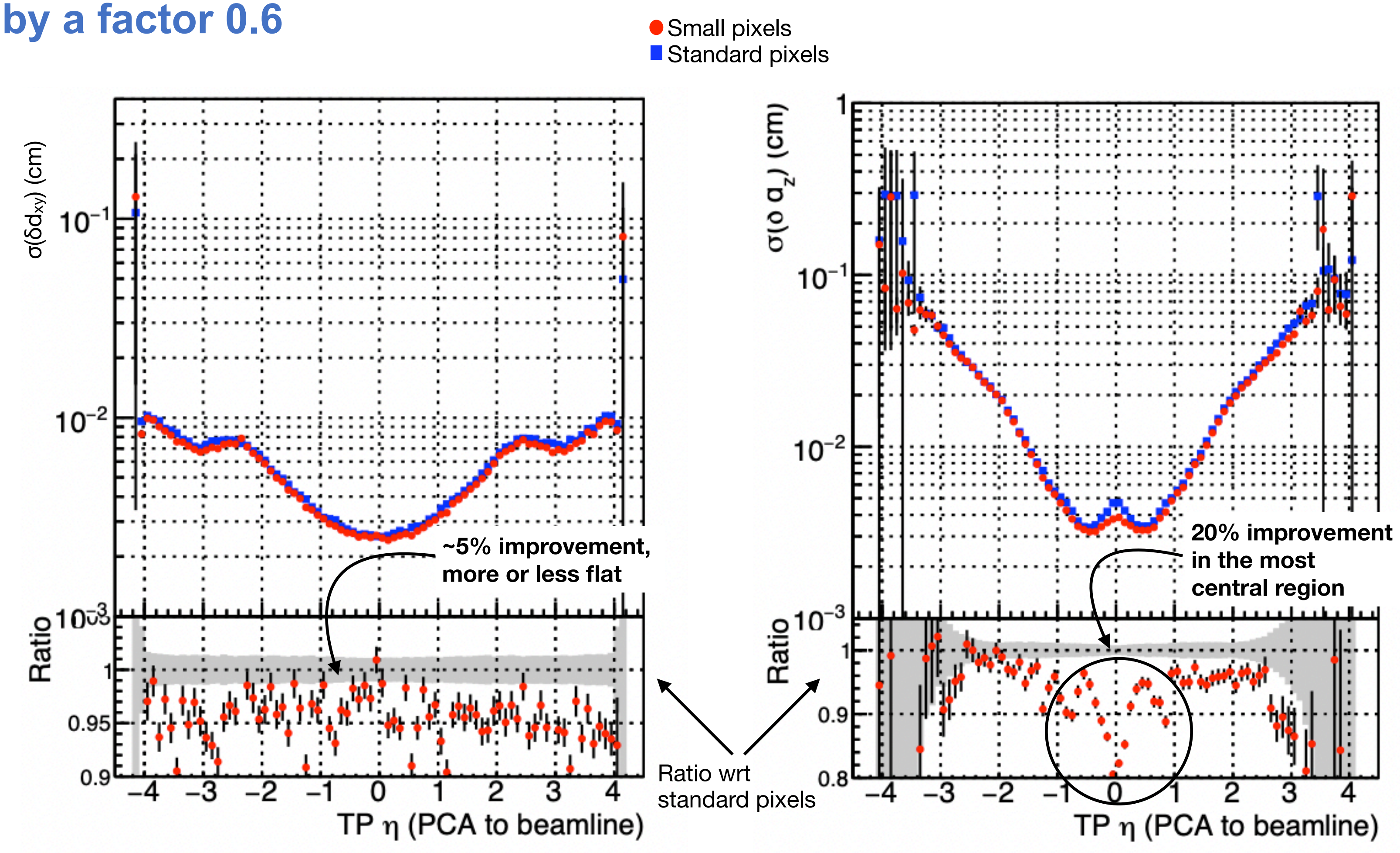
rϕ × y =
15 µm × 60 µm
in inner layer/rings



Performance improvement

- **Input: hit resolution scaled down by a factor 0.6**

$p_T > 0.9$ GeV →



Transverse IP resolution **Longitudinal IP resolution**

- **Output:**
  - **Improvement of ~5% in d_0 and z_0 resolution integrated above 0.9 GeV**
  - **Basically no improvement below 1 GeV**
  - **Improvement from 0 to 10% between 1 GeV and 10 GeV**

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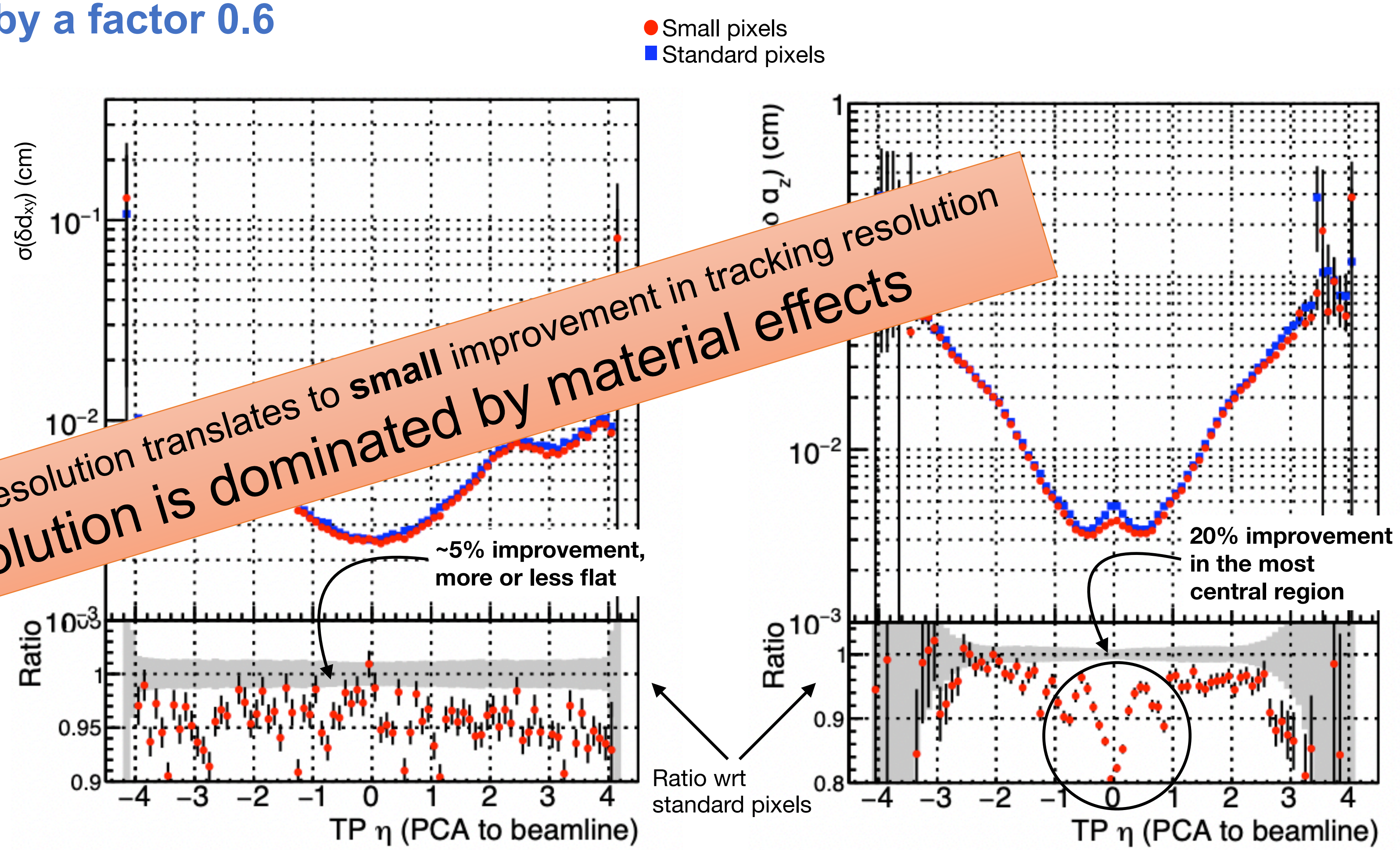

Transverse IP resolution

Longitudinal IP resolution

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  - Improvement of ~5% in d_0 and z_0 resolution integrated above 0.9 GeV
  - Basically no improvement below 1 GeV
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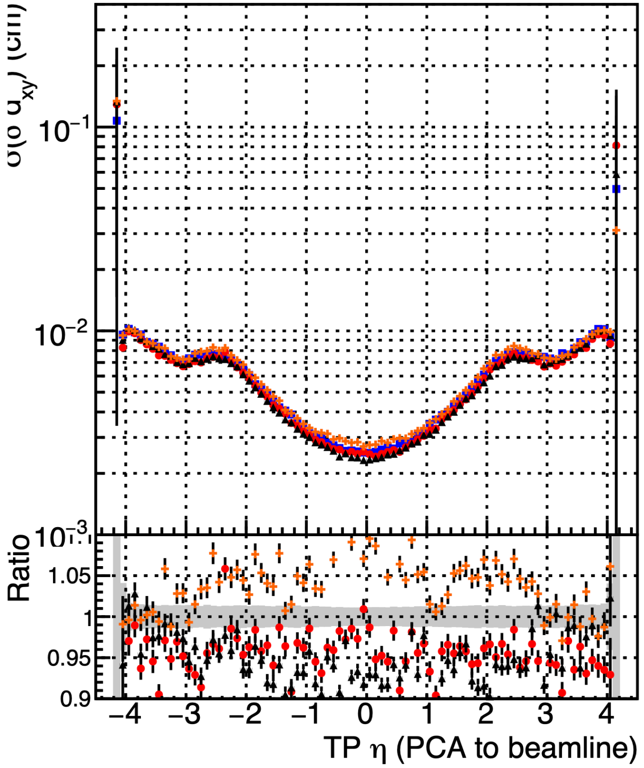
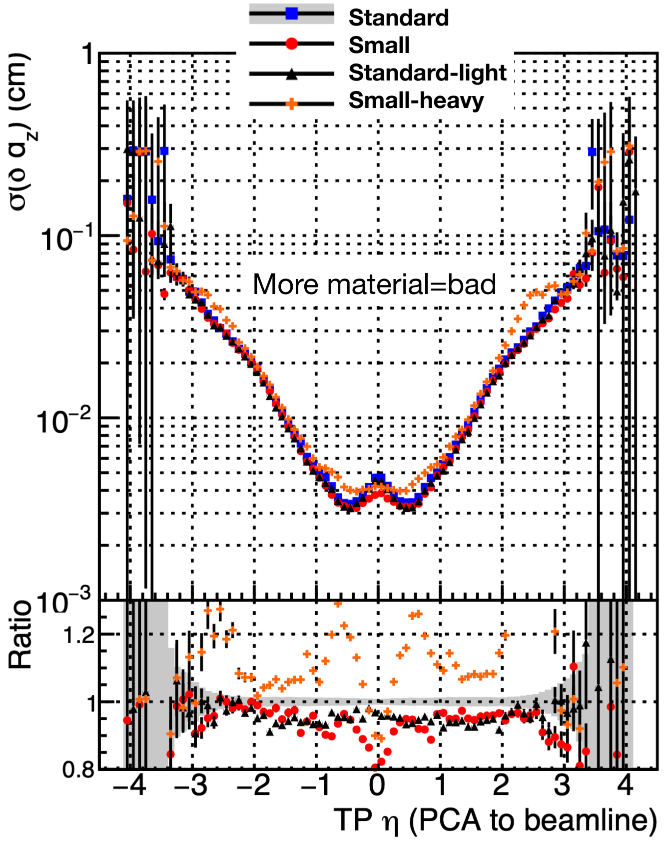
Performance improvement

- **Compare better hit resolution (× 0.6) with variation of material budget (± 15%)**

$p_T > 0.9$ GeV ⟶



Transverse IP resolution



Longitudinal IP resolution

- **Output:**
  - **An increase in material budget can easily outweight any benefit from improved hit resolution**
  - **Reduction of material can be more beneficial than use of smaller pixels**
    - **In most of the η range and except for very high p_T**
  - **Emphasis must be on material reduction**

Development guidelines for inner regions

- **Material budget is substantially driven by power budget**
  - **Power distribution, cooling distribution, cooling contacts**

- **Reducing the power budget is a primary goal for the inner regions**

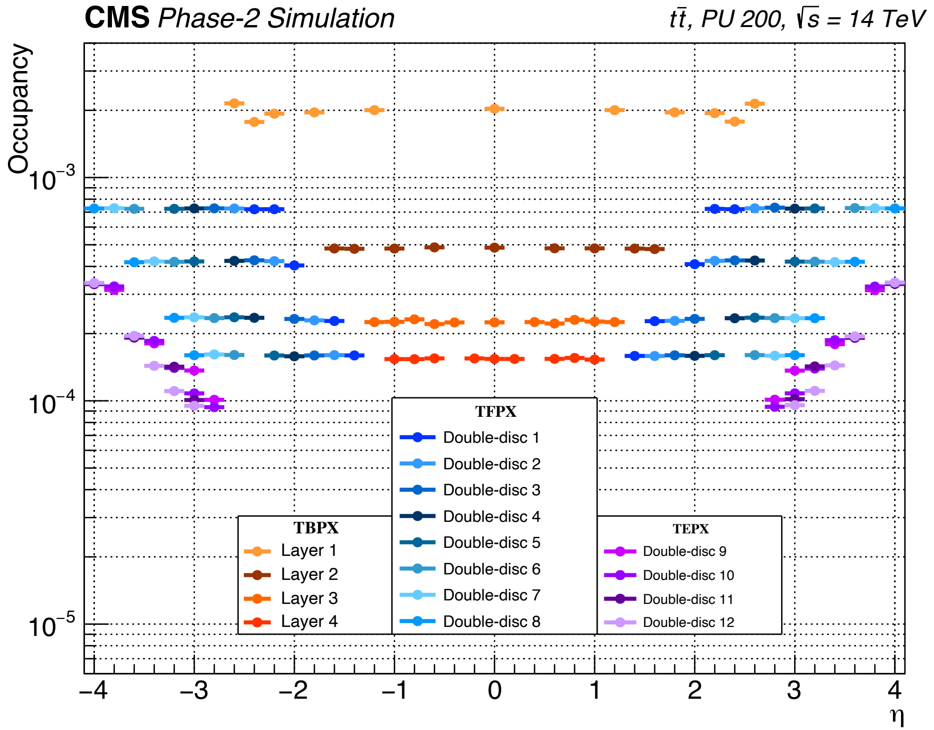
- **Use of 3D sensors is a must (*at least* for TBPX layer 1)**
  - **The use of planar sensors would aggravate the cooling requirements**

- **Granularity and functionality of the phase-2 detector is the good starting point**
  - **Enhancements can be considered only if they do not aggravate the power budget**
  - **Possible increase in granularity is in any case limited by the use of 3D sensors**

- **More aggressive low-mass system design is needed to improve performance**

Timing disks – sensors technology

- **Ideal goal: implement timing precision within same power budget and without degrading the hit resolution**
- **Exploit lower occupancy using resistive LGAD sensors**
  - **Ongoing R&D**
- **Required rad tolerance 3÷4×10^{15} 1 MeV n_{eq} at the lower edge**
- **Possible cell size 100×100 μm^2**
  - **Channel density reduced by a factor of 4 wrt phase-2 detector**
  - **Expected hit resolution ~ 5 μm**
    - **Significantly better than the phase-2 detector**
  - **Expected occupancy of 5×10^{-3} at the lower edge**
    - **If, e.g., the signal is contained in 2×2 cells**
    - **Other (better?) geometries under study**



Timing precision

- **If resistive LGAD can be used and the target performance is achieved:**
  - **Phase-2 tracking layers can be replaced with tracking+timing layers with no drawbacks**
  - **Replacing two disks is straightforward**
  - **Target timing precision on tracks (~ 30 ps) achieved with ~ 50 ps precision on hits**

- **If a different sensor technology has to be used (e.g. trench-isolated LGAD):**
  - **Hit resolution does not profit from charge sharing**
  - **Increase granularity to mitigate degradation of hit resolution**
    - **Trade off with power budget**
      - **Power budget of phase-2 detector can be exceeded for the timing disks, but not by a large factor**
  - **Depending on achievable granularity and power, replacement of one disk only may be preferable**
    - **Aggravates requirement on timing precision ⟶ feeds back into power density**

- **More complex optimization of granularity vs timing precision vs power density vs number of timing layers**

Timing precision

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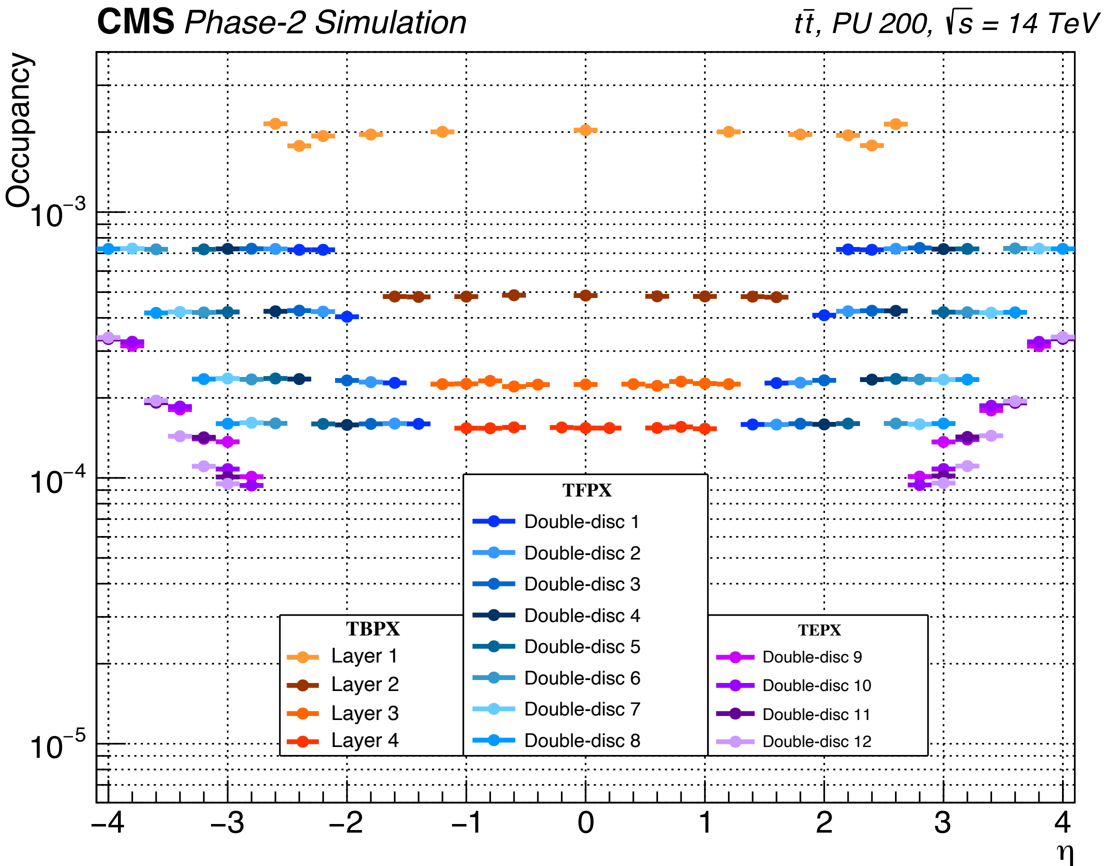
N.B. If resistive LGAD are made to work effectively for TEPX disks, they are a valid upgrade for all the 2×2 modules of the IT

Technically, an upgrade of larger scope would be possible!



First look at chip requirements

Inner regions

Pixel size $25 \times 100\ \mu m^2$

Detection threshold $\ll 900\ e^-$

Power density $\ll 0.6\ W/cm^2$

Timing disks

Pixel size $100 \times 100\ \mu m^2$

Timing resolution < 50 ps

Power density $\lesssim 0.6\ W/cm^2$

Chip size (h × w) $(16.8 \times \sim 21.6)\ mm^2$

Output bandwidth $\lesssim 5$ Gbps

Serial powering infrastructure

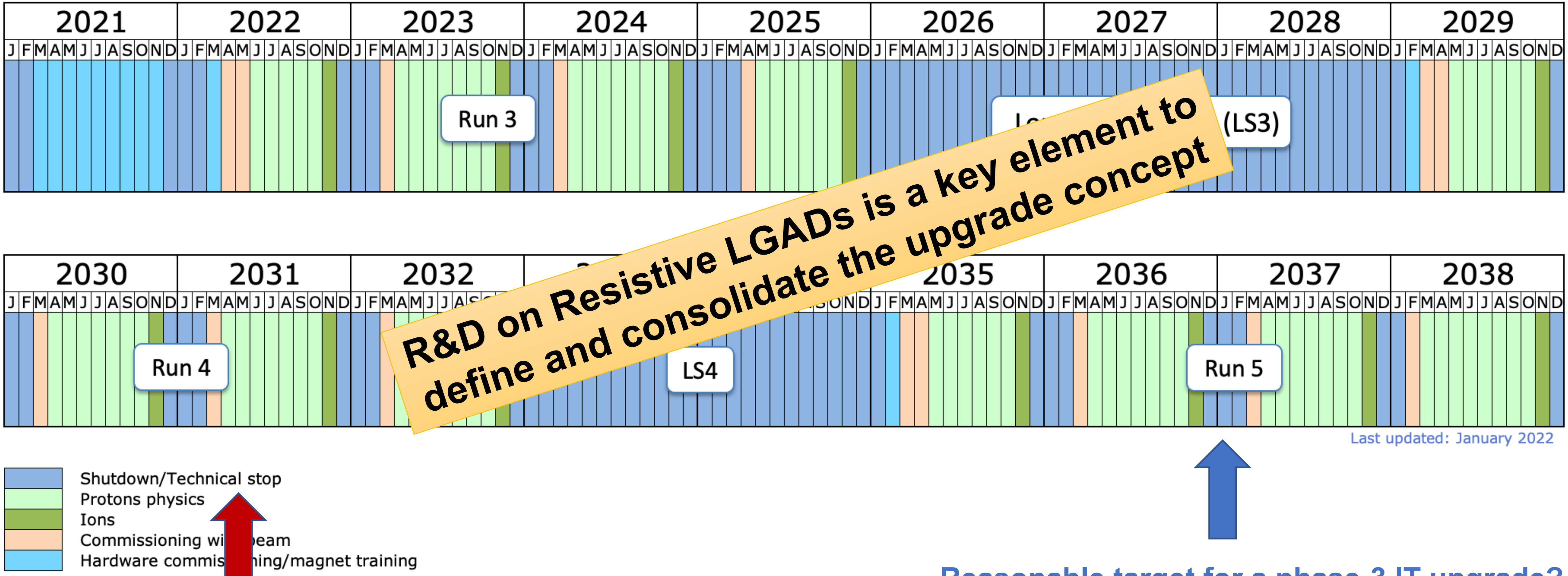
Trigger and latency as in phase-2

Interface to silicon photonics link

Can be configured as a single project - or even a single chip with two options for the front-end part

The requirements seem to be plausible **for a development in 28 nm**

Converge on chip specs



R&D on Resistive LGADs is a key element to define and consolidate the upgrade concept

Submit final chips

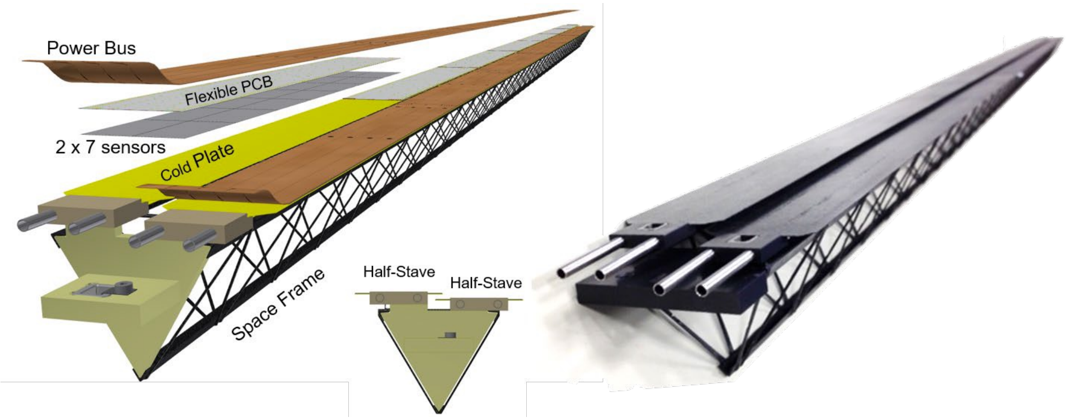
Reasonable target for a phase-3 IT upgrade?

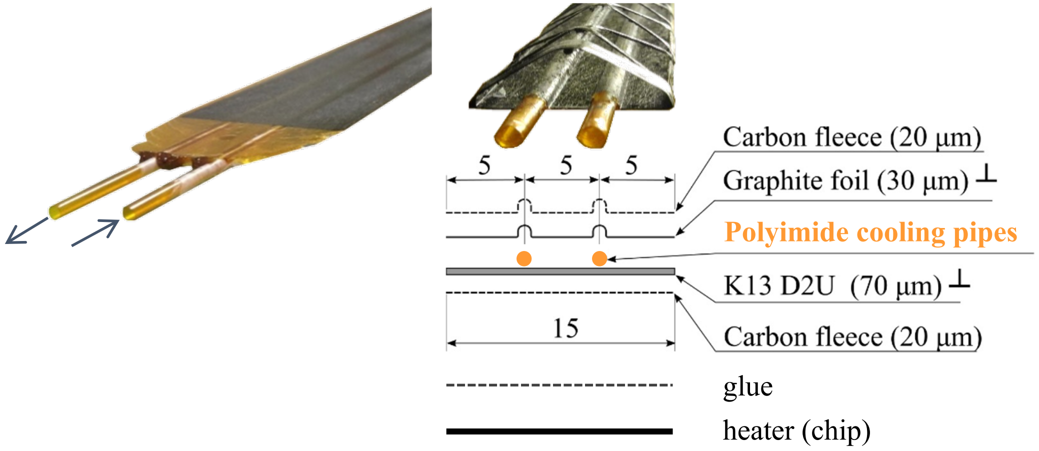
Ideas for low-mass system design

- **Focus initially on TBPX staves** (24 staves in L1, 48 staves in L2)

➢ Cooling distribution and cooling contact embeeded in mechanical structures

Build-up of the cold plate of the ALICE ITS stave
Operated with leakless water cooling

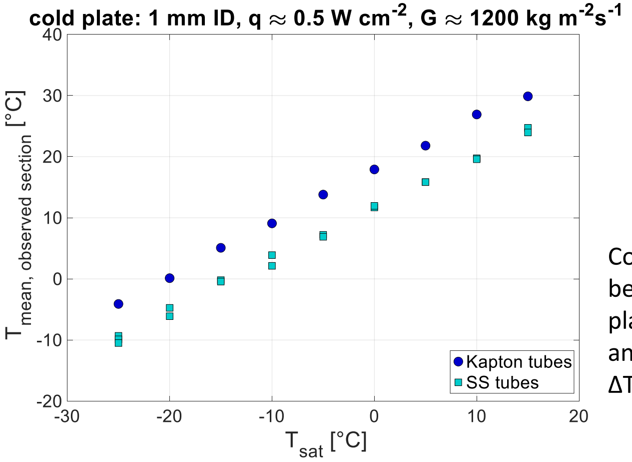




R&D to adapt to high-pressure CO_2 operation
Thick kapton tubes (bad thermally)
Steel tubes (bad for mass)

Titanium is maybe the right choice?

200 mm



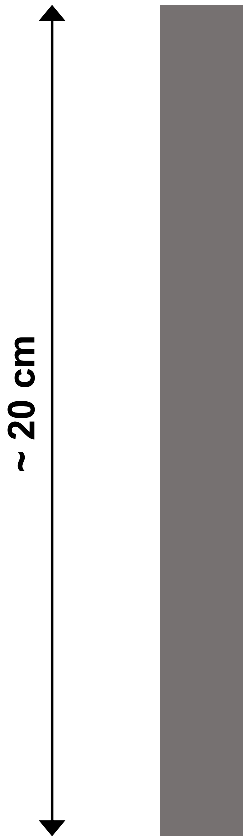
Comparison between cold plates: Kapton and steel version $\Delta T_{KAPTON-SS}$ ~5°C

Ideas for low-mass system design

- **Focus initially on TBPX staves** (24 staves in L1, 48 staves in L2)

➢ Integrated design of stave electronics

Cold plate with embedded pipes



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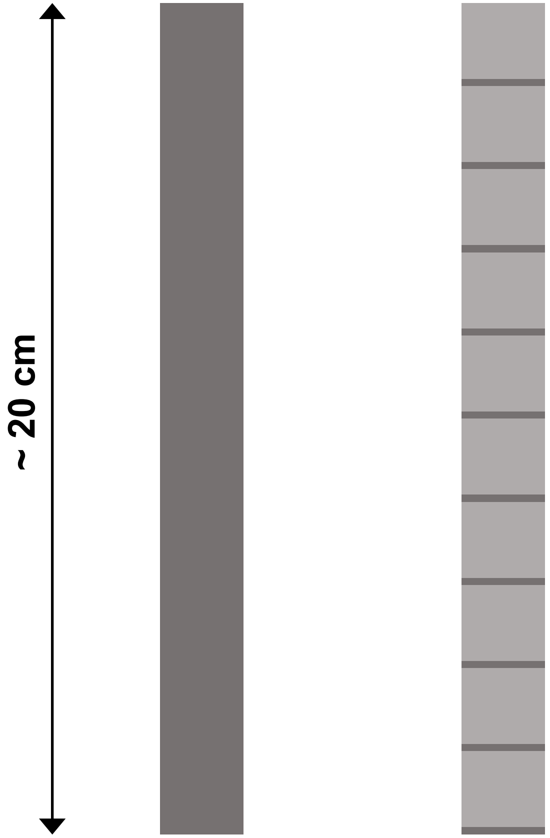
Single-sensor flip-chip assemblies



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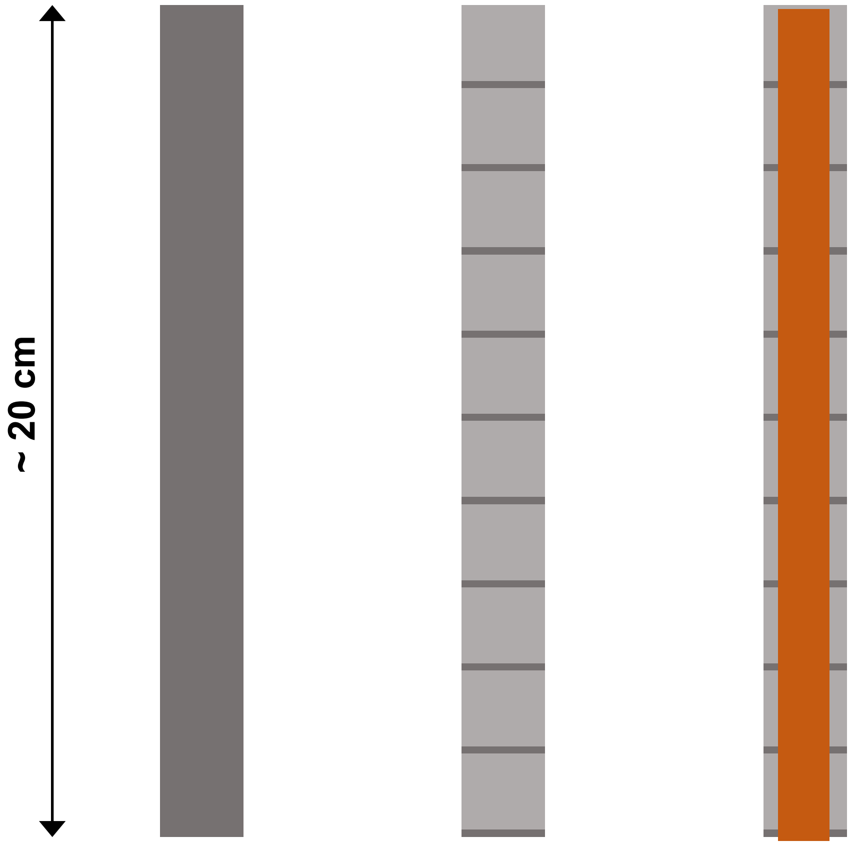
➢ Integrated design of stave electronics

All-in-one flex (Alu + Cu)
wirebonded to the readout chips



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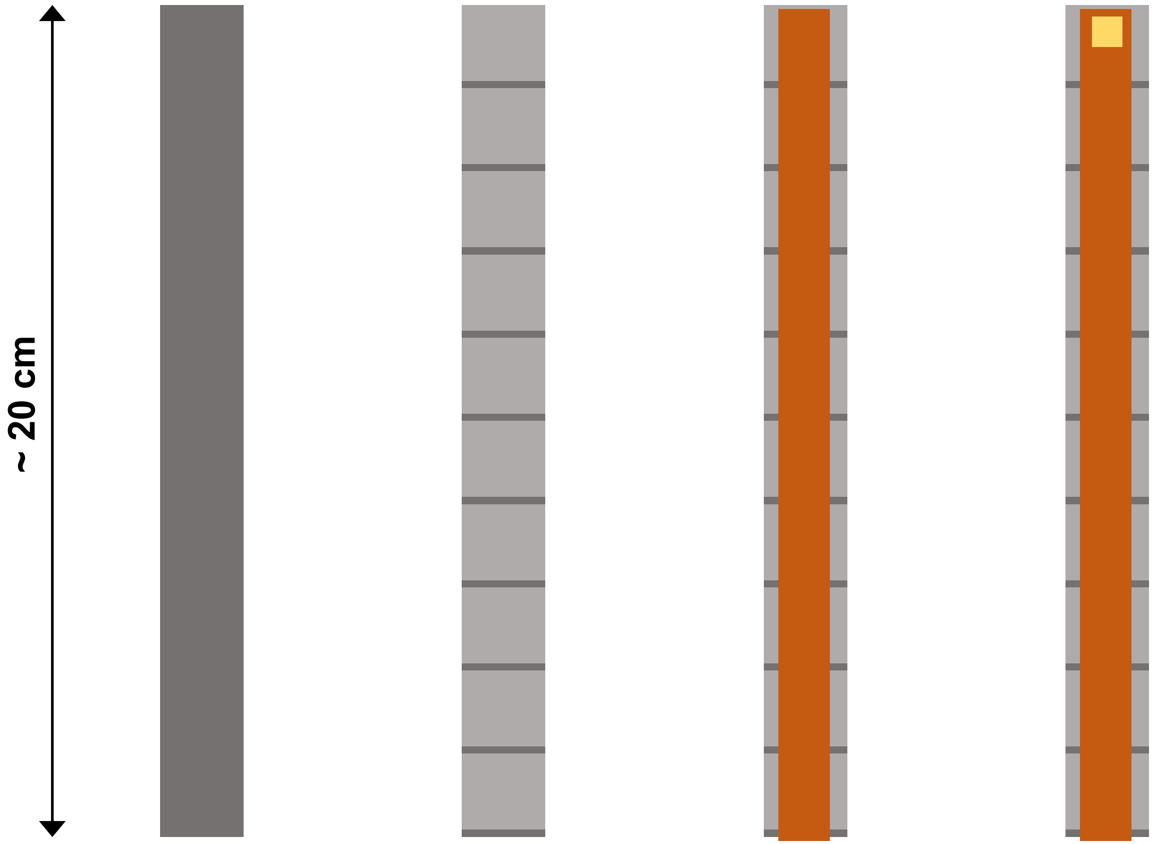
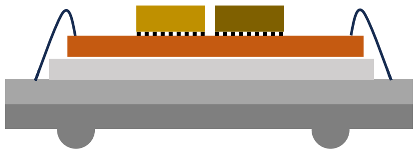
➢ Integrated design of stave electronics

End-of-stave concentrator
chip and photonics link





No on-stave connectors
Minimal thermal interfaces
Reduce e-links length from 2 m to ~ 20 cm
Remove portcards from service cylinder

50G of data: reasonable use of photonics link

Potential for large mass saving

Challenging 10-chip assembly

Thanks for your attention

Questions?