



# The plans of the future upgrade LHCb Tracker (Mighty Tracker)

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KIT - The Research University in the Helmholtz Association - www.kit.edu

# LHCb Upgrade II



- LHCb upgrade II is planned for Long Shutdown 4 to cope with the new operating conditions of High Luminosity LHC (L<sub>int</sub> = 300 fb<sup>-1</sup>, L<sub>inst</sub> = 1.5 x 10<sup>34</sup> /cm<sup>2</sup> /s)
  - Higher radiation dose
  - Increased particle multiplicities and rates
- Principle of LHCb Upgrade II:
  - General layout of the detector remain unchanged
  - Sub-detector (*incl.* Mighty Tracker) will be upgraded



# **Mighty Tracker in LHCb experiments**



- LHCb is a forward-arm spectrometer
- Upgrade I (SciFi Tracker)
  - 3 tracking stations downstream of the magnet
    - Scintillating fibers
  - $\rightarrow$  Now in operation
- Upgrade II (Mighty Tracker)
  - 3 tracking stations
    - Scintillating fibers
    - HV CMOS monolithic active pixel sensor (HV-MAPS)

→ Higher hit-rate capability and radiation hardness to survive in Run 5, 6

![](_page_2_Figure_12.jpeg)

# **Mighty Tracker in LHCb experiments**

![](_page_3_Picture_1.jpeg)

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![](_page_3_Figure_12.jpeg)

# **Mighty Tracker (Outer Tracker)**

![](_page_4_Picture_1.jpeg)

- Moderate occupancy region
  - 6 SciFi layers / station = 18 layers
  - Ongoing R&D to mitigate rad-damage, increase hitrate capability
    - Fibre improvements
    - Cryogenic cooling for lower noise
    - Micro-lens enhanced SiPM to concentrate signal and reduce noise from inactive region ....

![](_page_4_Picture_8.jpeg)

![](_page_4_Picture_9.jpeg)

![](_page_4_Figure_10.jpeg)

![](_page_4_Figure_11.jpeg)

## **Mighty Tracker (Inner Tracker)**

![](_page_5_Figure_1.jpeg)

- 28 HV-MAPS modules / station
- Chips on both side to cover entire module

![](_page_5_Figure_4.jpeg)

![](_page_5_Figure_6.jpeg)

![](_page_5_Figure_7.jpeg)

KIT ASIC and Detector Laboratory, IPE

# **Mighty Tracker**

 Inner Tracker (High occupancy regions)

- 28 HV-MAPS modules / station
- Chips on both side to cover entire module

![](_page_6_Figure_4.jpeg)

![](_page_6_Picture_5.jpeg)

Front view

![](_page_6_Figure_7.jpeg)

KIT ASIC and Detector Laboratory, IPE

# **Mighty Tracker**

 Inner Tracker (High occupancy regions)

- 28 HV-MAPS modules / station
- Chips on both side to cover entire module

![](_page_7_Picture_4.jpeg)

Silicon pixel detector

Sensor and readout electronics in one chip

Readout is isolated from substrate(sensor)

 $\rightarrow$  High bias voltage  $\rightarrow$  Charge collection by drift  $\rightarrow$  rad-hard

![](_page_7_Picture_9.jpeg)

Front view

![](_page_7_Figure_11.jpeg)

# **MightyPix (HV-MAPS for Mighty Tracker)**

![](_page_8_Picture_1.jpeg)

Requirements:

- Pixel size: < 100 µm x 300 µm</p>
- Hit-rate capability: > 17 MHz/cm<sup>2</sup>
- In-time efficiency: > 99% with correct assignment to 25ns bunch-crossing (BX)
- Radiation hardness: > 6 x 10<sup>14</sup> n<sub>eq</sub>/cm<sup>2</sup>
- Noise rate: < 5Hz / pixel</p>
- Power consumption: < 150 mW/cm<sup>2</sup>
- Compatible with the LHCb readout system
  - 4 x 1.28 Gbps data links/chip
  - Slow control
  - Timing and Fast Control (1command / BX)

# MightyPix (HV-MAPS for Mighty Tracker)

![](_page_9_Picture_1.jpeg)

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HV-MAPS from other projects

# **Results from the HV-MAPS Family**

![](_page_10_Picture_1.jpeg)

![](_page_10_Figure_2.jpeg)

MightyPix R&D

Finding optimum pixel size, operating temperature, power consumption for Mighty Tracker using a dedicated prototype and various HV-MAPS chips from other projects

# **MightyPix (HV-MAPS for Mighty Tracker)**

![](_page_11_Picture_1.jpeg)

Requirements:

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- Noise rate: < 5Hz / pixel</p>
- Power consumption: < 150 mW/cm<sup>2</sup>
- Compatible with the LHCb Readout system
  - 4 x 1.28 Gbps data links/chip
  - Slow control
  - Timing and Fast Control (1command / BX) -
- Dedicated prototype

![](_page_11_Figure_14.jpeg)

# **MightyPix1: the First Prototype**

![](_page_12_Picture_1.jpeg)

- The first prototype chip deliciated to Mighty Tracker
  - TSI 180nm process
  - Resistivity of wafer: 370 Ωcm
  - Chip size: Full length (20mm) x ¼ width (5mm)
  - 3 blocks:
    - Pixel Matrix
      - Sensor matrix with analog readout
      - Pixel size: 55 x 165 μm
    - Hit-buffer with ToA and ToT per pixel
    - Digital periphery
      - Column-drain architecture readout logics
      - 1.28Gbps x 1 data link
      - I2C interface for slow control
      - Timing and Fast control command decoder
      - 40MHz to 640MHz PLL x 2 types

![](_page_12_Figure_17.jpeg)

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![](_page_13_Picture_17.jpeg)

# **MightyPix1: the First Prototype**

![](_page_14_Picture_1.jpeg)

29 Columns The first prototype chip deliciated to Mighty Tracker TSI 180nm process Resistivity of wafer: 370 Ωcm **Pixel Matrix** Pixels . Chip size: Full length (20mm) x <sup>1</sup>/<sub>4</sub> width (5mm) 3 blocks: Pixel Matrix Sensor matrix with analog readout Hitbuffers Hit buffer Pixel size: 55 x 165 µm 6b current DACs ColConfig Hit-buffer with ToA and ToT per pixel 10b voltage DACs Col1 Col2 Col27 **Digital periphery** CMOS PLL Column-drain architecture readout logics Confiabits Readout Logic CML PLL 1.28Gbps x 1 data link Singleended 2-wire max. 5 MHz Slow control 32b x 40 MHz (I2C) I2C interface for slow control De-Mux Timing and Fast Serial out FEreset, BXreset, Snapshot Differential 320 Mbps Timing and Fast Control Serializer LVDS Scrambler control command decoder SYNC (TFC) 40MHz to 640MHz PLL x 2 types N. Striebig, KIT

#### **First results of Mightypix1**

![](_page_15_Figure_1.jpeg)

![](_page_15_Picture_2.jpeg)

- Submitted in 2022
- Tests started in Summer of 2023
- Basic functionalities including newly implemented digital interfaces are tested using electrical signals & radioactive sources
  - PLL
  - 1.28 Gbps data link
  - I2C interface
  - TFC command decoder
- Waiting for irradiation and beam tests

# Next Step (MightyPix 2)

![](_page_16_Picture_1.jpeg)

- First full size chip (cf. Mightypix1 = ¼ size)
  - Deleting features for debugging
  - 4 x 1.28Gbp data links
    - ~100% readout efficiency at the hit rate of >17MHz/cm<sup>2</sup>
  - Serial powering and more to test in MightyPix modules

![](_page_16_Figure_7.jpeg)

Simulated Readout Efficiency (MightyPix2)

![](_page_16_Figure_9.jpeg)

# Summary

![](_page_17_Picture_1.jpeg)

- Mighty Tracker is designed for LHCb upgrade II
  - "Hybrid tracker" of SciFi and HV-MAPS (MightyPix)
    - R&D of SciFi for mitigate rad-damage, increase hit-rate capability
    - R&D of MightPix
      - Ist prototype chips (full column-length x 1/4 width of the final chip) were produced
        - Basic functionalities incl. the digital interfaces has been tested
        - Tests with beam is planned in the beginning of 2024 (efficiency, time resolution etc.)
      - Conceptual design of MightyPix 2 has been already started

#### Back up

![](_page_18_Picture_1.jpeg)

#### **HV-MAPS Module (Control & DAQ)**

![](_page_19_Picture_1.jpeg)

![](_page_19_Figure_2.jpeg)

![](_page_20_Picture_0.jpeg)

# Focused Ion Beam Fixing (FIB) of Mightypix1

- There is a mistake in MightyPix1 design
  - Better design verification
    - The mistake was overlooked during the design-verification (simulation)
  - Repairing the mistake by FIB
    - Cutting and adding lines in the chip
    - 5 FIBed chips  $\rightarrow$  4 FIBed and repaired chips
    - 18 more chips were FIBed