





The LHCb Upgrade Programme and the VELO

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 - Requirements move to timing
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Flavour Physics at LHCb

New physics searches with flavour look for the indirect effects on low energy processes, for instance rare b-hadron decays, probing mass scales not directly accessible at the LHC

The LHC provides huge statistics and access to all cand b-hadrons - but **event topology is challenging**; need low material, ability to trigger on low p_T , and particle identification to flavour tag and distinguish topologically similar decays e.g. $B \rightarrow \pi\pi$, $B \rightarrow K\pi$



LHCb is a **general-purpose forward detector** at the LHC which is **particularly suited** to precision measurements in the beauty and charm sectors

- ✓ Δp / p = 0.5% at < 20 GeV/c, 1.0% at 200 GeV/c
- ✓ IP resolution = 15 + 29/ p_T [GeV/c] µm
- ✓ decay time resolution 45 fs for $B_s \rightarrow J/\psi \phi$ and $B_s \rightarrow J/\psi \phi$
- ✓ Kaon ID ~ 95% for 5% $\pi \to K$ mis-id probability
- ✓ full real time reconstruction in the high level trigger



LHCb Detector Performance



LHCb accumulated 9 fb^{-1} of integrated luminosity during LHC Runs 1 & 2

a wealth of further measurements and discoveries including:



and also **intriguing anomalies**: R(D^{*}), angular analysis of $K^*\mu^+\mu^-$...

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mw [MeV]

 $(t-t_o) \mod (2\pi/\Delta m_c)$ [ps]

LHCb

1.9 fb⁻¹

OS tagging

LHCb Upgrade Programme







Current VErtex LOcator (U1)

L-shape hybrid pixel silicon detector modules cooled by biphase CO_2 which passes under the chips in etched microchannels within a silicon wafer cooler (T~-30°C)

- ~ 3 % X_0 radiation length before second measured point on track

Two moveable halves: closer to beam line (R = 8.2mm \rightarrow R = 5.1 mm) for improved IP resolution

• 52 modules, 41M pixels, 208 x 200 µm sensor tiles

New ASIC: VeloPix ~ 20 Gb/s in hottest ASIC for a total of 3 Tb/s for whole VELO

Improved impact parameter and decay time resolution







VELO half being installed

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For more details see talk of Kurt Rinnert on Monday

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SMOG2 and Fixed Target Physics

New SMOG2 system installed to inject various gas species in the LHCb interaction region

- Fixed Target physics at the LHC, in parallel with pp data taking
- Gas cell attached to the VELO, displaced p-gas IP for easy distinction pp data



Physics programme spans over:

- anti-proton production
- Central exclusive production
- X(3872)/psi(2S)
- psi(2S)/ J/psi
- Strangeness production
- $\Lambda_c \to pK\pi$

+ LHCb participation in Heavy Ion runs (PbPb and pPb data taking) down to 30% centrality in LHCb in Run 3



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From Upgrade I to Upgrade II

Upgrade I will not saturate precision in many key observables \rightarrow a further upgrade is necessary to fully realise the flavour-physics potential of the HL-LHC There is steady progress towards plans for an Upgrade II, that will operate in Runs 5 and 6.



Part of the CERN baseline plan.

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From Upgrade I to Upgrade II



Upgrade II

Upgrade II performance must equal or surpass that of Upgrade I, with

- Pile-up reaching values of 40
- 200 Tb/s of produced data

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- charged particle densities up to $1 \times 10^{12}/cm^2$



This is the **intensity frontier**! New, lightweight technologies with high granularity, timing, radiation resistance and innovative data processing all necessary to go to $\mathscr{L} \sim 1 \times 10^{34} \text{ sec}^{-1} \text{cm}^{-2}$

Image credit: Tim Evans VErtex LOcator (VELO) Run 3: pile-up ~5 200 400 600 x (mm) z (mm) ~2000 tracks Ĩ ~6 cm Upgrade II: pile-up ~40 200 400 600 x (mm) z (mm)

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Timing to the Rescue





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Timing Requirements - VELO

Target: 20 ps per track

110

100

90

80

70

60

50

40

0

PV Efficiency [%]

• Key performance requirement for tracking efficiency, ghost rates and background rejection

100

Hit Resolution [ps]

• Demands < 50 ps resolution from sensor \oplus ASIC

 $- \mathcal{L} = 2.0 \times 10^{33} \,\mathrm{cm}^{-2} \mathrm{s}^{-1} (\mathrm{3D})$

 $-\mathcal{L} = 1.0 imes 10^{34} \, \mathrm{cm}^{-2} \mathrm{s}^{-1} \mathrm{(4D)}$ $-\mathcal{L} = 1.5 imes 10^{34} \, \mathrm{cm}^{-2} \mathrm{s}^{-1} \mathrm{(4D)}$



50





Configuration

3D

4D

 $\varepsilon_{\mathrm{long}}\,[\%]$

98.1

98.7

 P_{ghost} [%]

3.2

1.1

 $\varepsilon_{\rm velo}$ [%]

96.6

97.2

Timing Implementation - VELO

Two global approaches to timing implementation investigated:

Adding time stamp to all hits - "4D tracking"

Inherently robust and provides maximum coverage, however places highest demands on ASIC

Adding dedicated timing planes for "per track" timing

• Up to 200% more silicon area required in a second technology, with pitch down to ~150 μ m pitch and 25 ps resolution, can suffer from time dispersion for lower momentum tracks



How to run at high lumi?

Vacuum

VELO relies on many technologies



Mechanics



Sensors and ASICs



Sensors and ASICs

Impact parameter resolution at low p_T is a crucial driver of the final physics performance of LHCb

Typically < 25 μm down to 1 GeV/c

Interplay between innermost radius and material

Examples of two scenarios at the extreme limits - radiation hardness and rate vs material and precision



Scenario "A"

- rates up to 0.25 Tb/ASIC
- fluence > 6×10^{16} 1 MeV n_{eq}/cm^2

Scenario "B"

- pixel pitch < 42 μ m
- "ultra low" material budget





ASICS

to be replaced with ultra high rate, radiation hard, timestamping, low pitch ++ solution

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Sensors and ASICs

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Data Transmission and readout

Current VELO transmits up to 20 Gbps per ASIC and up to 3 Tbps from entire VELO , achieved via

- Fast electrical transmission in vacuum over low mass data tapes
- Vacuum feedthroughs capable of fast data transmission to UHV
- optical transmission over 350m to PCIe40 readout cards
- FPGA which can handle in real time processing of data including time ordering, clustering...



Upgrade II needs

- Bandwidth increase of a factor > 10 (data rate plus additional functionality e.g. timestamp
- huge demands on next generation FPGAs and high speed links e.g. photonic integrated circuits
- Operation in vacuum poses significant challenges (optical feedthroughs, access...)
- distribution of tasks between ASIC/FPGA/GPU/CPU crucial and decisions to be taken on system level

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How to run at high lumi?



High Speed Data Transmission

Electronics

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Sensors and ASICs

Mechanics

Cooling for U1 - microchannels



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Cooling for U1 - microchannels



A Colder, more transparent, future?

Choice of coolant

Evaporative CO₂ cooling is reaching its limit (triple point at -56°C)

A possible replacement could be N₂O which has a similar behaviour and would extend to -164°C, however the heat transfer efficiency is gradually dropping

CF4 could play a role but is disfavoured for environmental reasons

Krypton has very good HTE at lower temperatures - could be conceivably combined with CO₂ in a hybrid system, with similar pressure tolerance requirements (~100 bar), hence compatible for the module design

Super critical (warm) cooling, could be more interesting for linear collider applications where radiation damage is not a consideration. For instance CO₂ (31°C,74 bar), or "super critical krypton" (-64°C,54 bar), allowing thin walls and very good HTE*



Curves show best heat transfer, assuming cooling pipe diameter optimised individually for each point, for different coolants



See <u>presentation</u> by Bart Verlaat, Paolo Petagna, "R&D for a colder future in HEP", Forum on Tracking Detector Mechanics 2019, and <u>presentation</u> by Oscar Augusto, 5th Workshop on LHCb Upgrade II, March 2020, "Cooling, Detector Layout, Mechanics"

*note that krypton is more challenging operationally due to need to apply transcritical cooling to avoid thermal shock

Ceramic

- Different base materials: YSZ, $Al_2O_3, \mbox{AlN}, \mbox{SiC}\ldots$
- Manufacturing based on several layers of a base material (YSZ, Al_2O_3 , AIN, SiC)
 - Possible to embed conductive layers in between ceramics layers and metallize the surface
 - Potential to integrate electronics or high conductivity elements
 - · Mechanically robust, stable, and compatible with high ultra vacuum



- First prototype based on alumina:
 - Initial channel with 70μm width (restrictions)
 - Channels height $100 \mu m$
 - Overall dimensions: 40 × 60mm²



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Silicon Microchannels

Address production cost (yield related)

- Alternative Bonding (anodic bonding..)
- Avoid mask based photolithographic techniques
- Smaller cooling plates

Handle wafer bonded to active silicon (IFIC/MPI-HLL)

 Buried microchannels (CERN/.EPFL)



CMOS compatible process potential post processing step Holds 110 bars, leak tight to 10⁻⁸ mbar l/s

AIDA-2020-NOTE-2020-003 https://indico.cern.ch/event/1324261

Metal tracks

Microchannels

cooling to the tiles

R&D @ CPPM

- Laser etching and anodic bonding
- 5 x 10 channels per wafer
- 200µm x 70µm x 4.5cm per channel
- Next step: connector with anodic bonding



Alexandros Mouskeftaras, Stephan Beurthey, Julien Cogan, Gregory Hallewell, Olivier Leroy, et al.. Short-Pulse Laser-Assisted Fabrication of a Si-SiO2 Microcooling Device. Micromachines, MDPI, 2021, 12 (9), pp.1054. 10.3390/mil2091054. hal-03356892

here silicon interposer + RDL

Most ambitious approach: bring the

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Silicon Microchannels

Address production cost (yield related)

- Alternative Bonding (anodic bonding, no bonding)
- Smaller cooling plates

For LHCb the requirements are extremely stringent due to the high pressure and operation in the LHC vacuum. Just one tiny bonding fault on a wafer can result in the loss of an entire cooling plate.







A choice of smaller plates can give more flexibility for production and mounting, with 3d printed solutions giving more options

Additive manufacture

Cooling plate manufacturing

- Silicon microchannels vs 3D-printing
- Cooling performance, CTE mistmatch, tile attachment, reproducibility
- Materials: Titanium, Ceramics, ...

	Si	Al	Ti	SiC
Thermal cond. (W/m.K)	149	237	6.8	120
Thermal Exp. (ppm/K)	2.6	23.1	8.9	2.8
Density (g/cm ³)	2.3	2.7	4.4	3.2



- 'light' supports for hybrids
- 300 µm support under bond pads (C-side, N-side)





3d titanium printing successful prototyping for LHCb

Lots of activity in AIDAinnova WP10 2021 status report, Marcel Vos and Paolo Petagna

How to run at high lumi?



High Speed Data Transmission

Electronics

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Mechanics



Sensors and ASICs

Ultra low mass foil

Key piece of R&D which can unlock the way to easing the demands of scenario A

- "Mixed vacuum approach" - no worries about ΔP between detector and LHC vacuum - ultra thin geometries are accessible



Foil held under tension across full length of VELO, split into two halves to allow open/ closed positioning. Alternatives: wires, CNT fibre mesh... Operation



Maintenance



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Ultra low mass foil

Key piece of R&D which can unlock the way to easing the demands of scenario A

• "Composite box approach" -Ultra low Z material potential, new shield with very low and consistent thickness, no need for primary vacuum access. Key challenges include maintaining a thin laminate while successfully coating.





30 um skin depth copper "beam facing" (ultimately, may be "split skin" 120/60/30 um critical section

Tests ongoing with stretched wire characterisation and vacuum compatibility checks

Mixed volume solution may also be tried

Conclusions

LHCb Upgrade I: Datataking NOW!

VELO is fully installed and operational

LHCb Upgrade II: unique opportunity for an ultimate precision flavour physics and general purpose experiment in the forward region.

EOI, Physics Case and FTDR approved by LHCC/RB Strong support received in European strategy

Very challenging project \Rightarrow lots of R&D ongoing on all sub-systems New technologies needed, now is a great time to join the collaboration

Useful References

- Cooling options for LHCb Upgrade II, Oscar Francisco
- https://indico.cern.ch/event/1318635/contributions/5551953/
- Microchannel cooling development for LHCb VELO Upgrade I
- https://doi.org/10.1016/j.nima.2022.166874
- Readout firmware for LHCb VELO Upgrade I
- https://cds.cern.ch/record/2789034
- LHCb Readout system for Phase I of the VELO Upgrade
- https://cds.cern.ch/record/2710548?In=en
- LHCb Framework TDR for the LHCb Upgrade II
- [CERN-LHCC-2021-012]





Cooling for U1 - microchannels

Channels integrated in silicon substrate under hybrid pixel tiles

Material budget: 500 µm Si + coolant Very homogenous material distribution Cooling delivered directly under heat sources Thermal contact over flat area No CTE mismatch wrt ASICs and sensor Very efficient cooling performance

- 60 µm glue interface only
- 120/240 µm Si between coolant and electronics
- Very high thermal conductivity (Si 150 W/m.K)
- Very low temperature gradients over substrate

Evaporative cooling \rightarrow fast response to changes in power dissipation

Cooling is so effective that the microchannel can be withdrawn 5 mm from module tip

Challenges: Production (large size of device), Mastery of full silicon process (DRIE, Direct Wafer Bonding), Fluidic connector attachment, QA for proven long term mechanical stability





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Grade 2 printed Ti: a lot of experience in industry (medical, dental)

Advantages

- strong, easy to handle, will not break
- easier to connect CO₂ pipes (welding, brazing)
- Restrictions integrated into inlet
- Fast turnaround for design changes (order of weeks)
- Fast production 25/batch, 1 batch/few days
- cheap (<500 Euro / module, including welding capillaries)

Challenges

- CTE match with silicon is worse (8.6 vs 2.6 ppm/K)
- smaller thermal conductivity (16 vs 150 W/mK)
- smaller radiation length (3.6 vs 9.4 cm)
- irregularities in printing; less flat surfaces?



See presentation by Freek Sanders, "Design and Production challenges for the LHCb VELO Upgrade Modules", CERN Detector Seminar, February 2019

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prototype fitted with heaters

- high pressure test to 250 bar
- Leak tight with 250 µm wall



successful cooling test ($\Delta T \sim 13^{\circ}C$)



successful flow and stability test ($\Delta T \sim 13^{\circ}C$)

R&D 3d printed substrates made extremely rapid progress and were a credible backup alternative for LHCb. At the time of development the microchannels were sufficiently mature to be chosen as the implementation for Run3

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A bit of hi

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Cooling for U1 - microchannels



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3d printed technology already in active development for UII May give the flexibility required for a cooling "skeleton" Many issues of connectivity to be solved

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