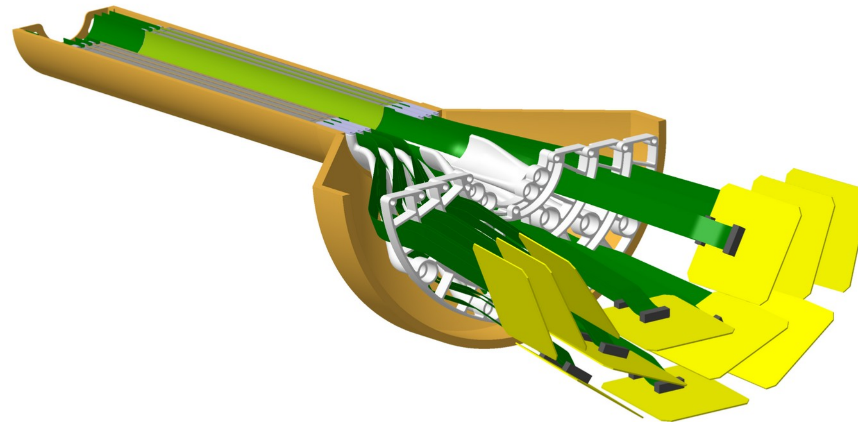
ITS3: next ALICE upgrade of the Inner Tracking System for LHC Run 4

Filip Krizek, NPI CAS

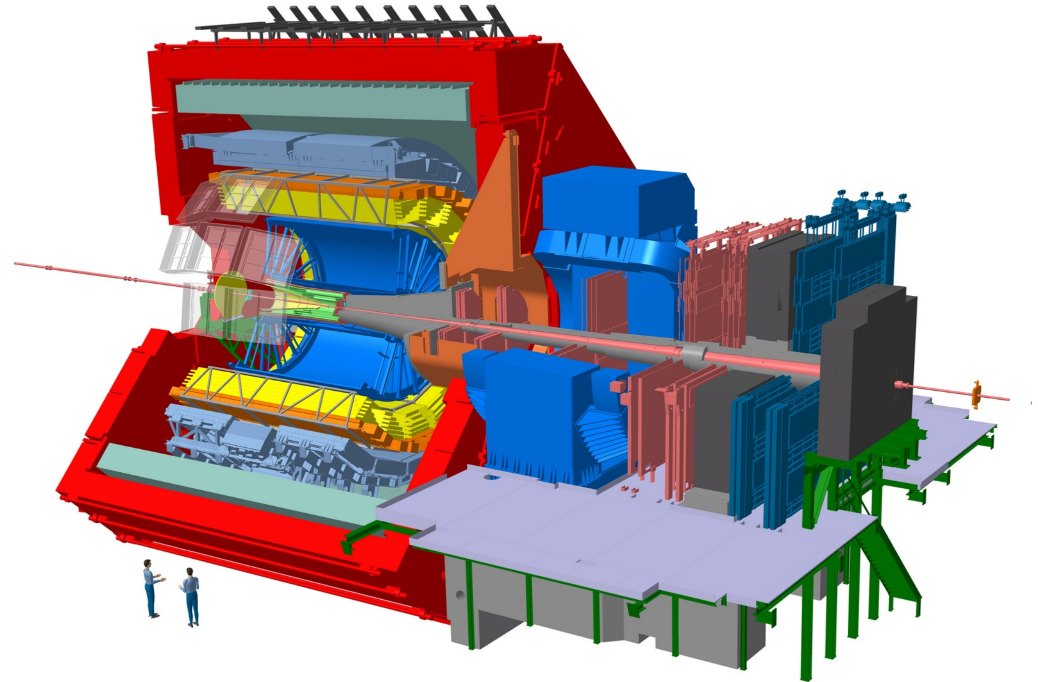
for the ALICE Collaboration



ALICE in LHC Run 3 and Run 4

ALICE

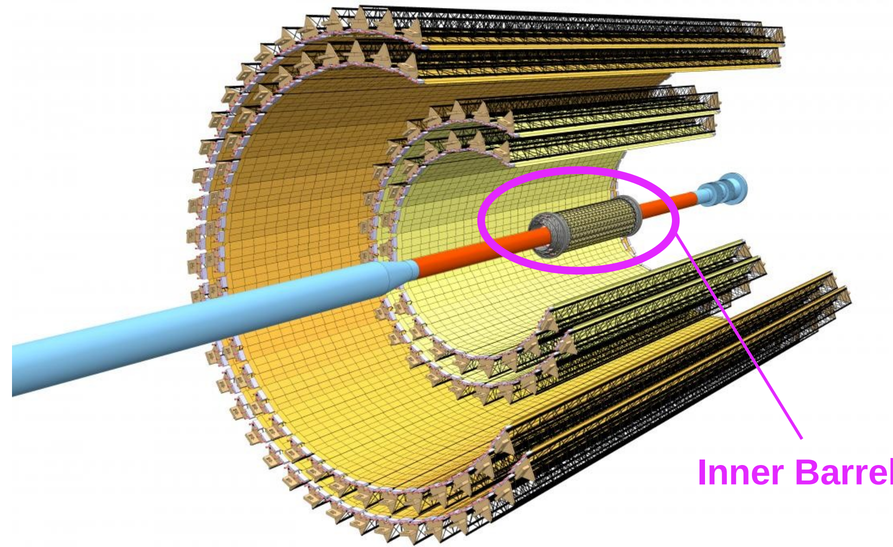
- **ALICE Physics goals for Run 3 & 4**
  - low-p_T open HF hadrons and quarkonia
  - low-mass dielectrons
  - light nuclei, antinuclei and hypernuclei



- **Key Run 3 upgrade:**
  Inner Tracking System (ITS2)

- **Follow up upgrade in Run 4:**
  Inner barrel of ITS (ITS3)
  - installation 2026 - 2028
  - in operation 2029 - 2032

Inner Tracking System in Run 3

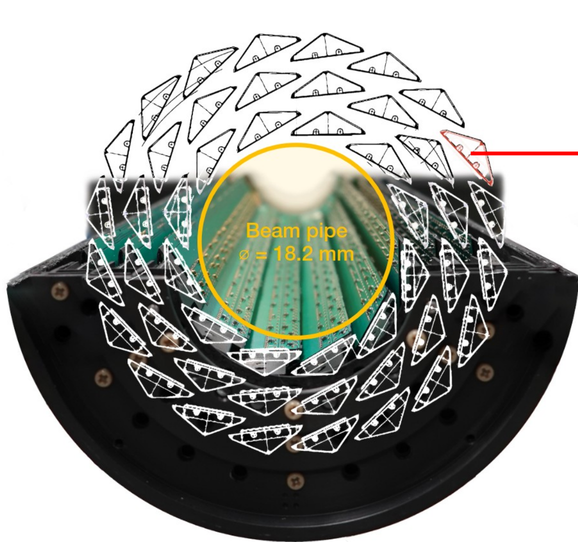


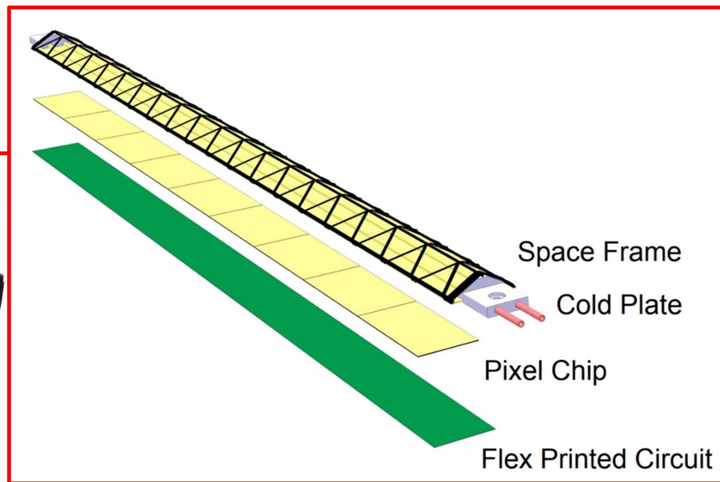
7 layers of Monolithic Active Pixel Sensors (MAPS)

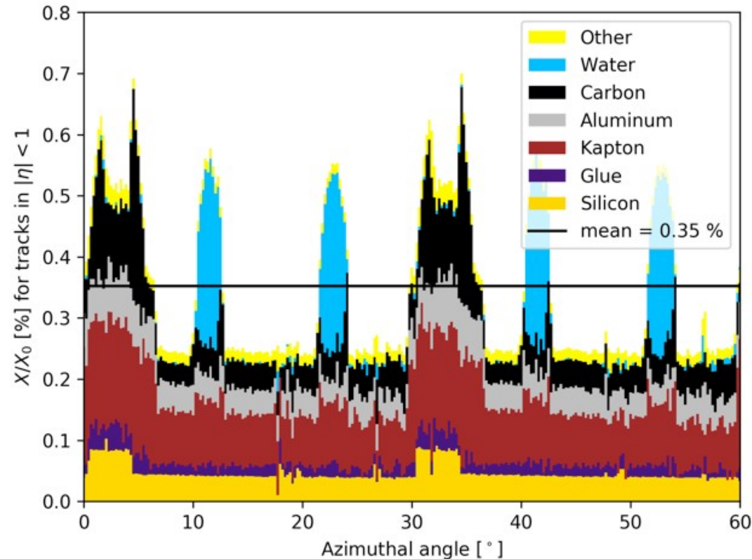
	Layers	Radii (mm)	X_0/layer
Inner Barrel	3	22 - 42	0.35%
Outer Barrel	4	194 - 395	1.1%

More details in talk by Andrea Sofia Triolo from Mon 16th Oct

Material budget considerations for the Inner Barrel of ITS







ITS Inner Barrel has 0.35% X_0/layer but Si makes 1/7th of the total only

Is it possible to further reduce material budget of the inner ITS layers?

- Removal of water cooling → reduce power consumption & move sensor periphery to chip edge
- Removal of circuit board → integrate power and data buses on the chip
- Removal of mechanical support → utilize stiffness of **large size, bent Si wafers**

Inner Barrel of ITS for Run 4 (ITS3)

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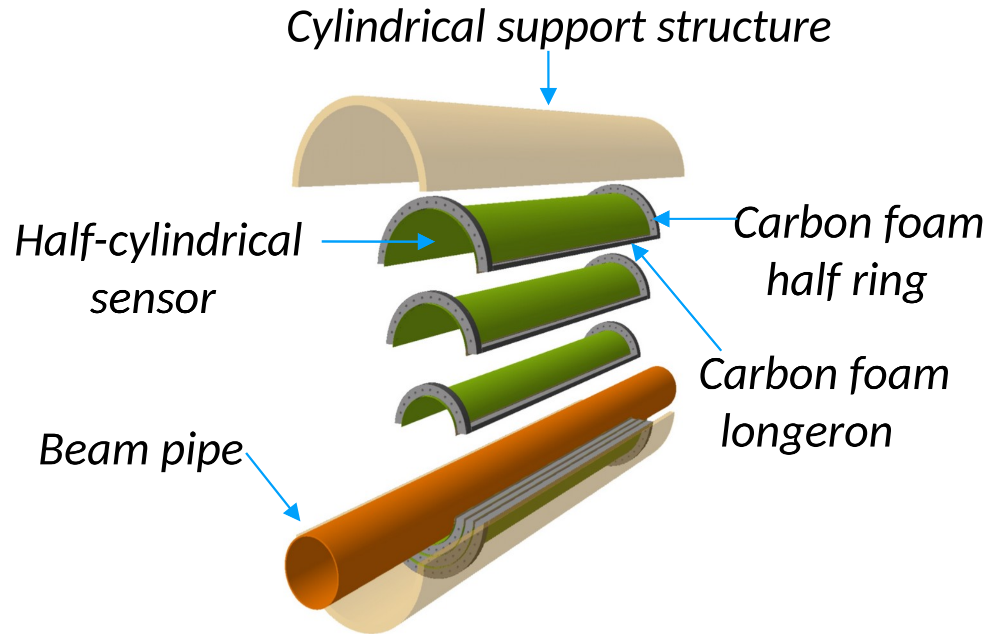

ITS3 will comprise 6 chips only!

Sensor length 266 mm x width 55 / 74 / 93 mm

Thickness $\lesssim$ 50 μm

Radial position **18** / 24 / 30 mm

Mechanical support by carbon foam spacers

Material budget 0.05% X_0/layer

MAPS produced by **65 nm CMOS** process

1D stitching on 300 mm wafers

Spatial resolution requirement 5 μm

Expected TID 10 kGy & NIEL 10^{13} 1 MeV n_{eq} / cm^2

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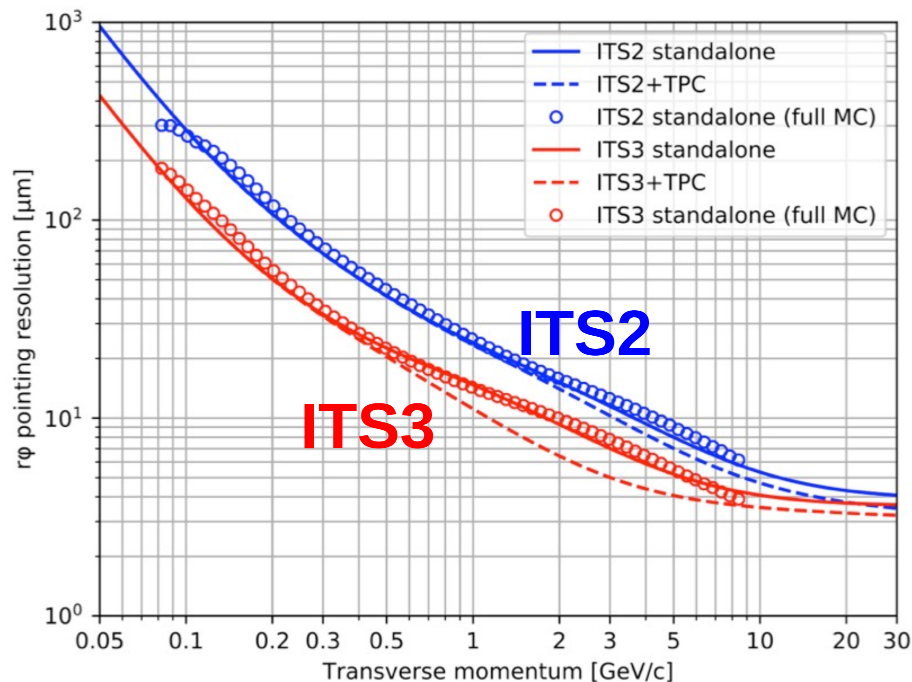
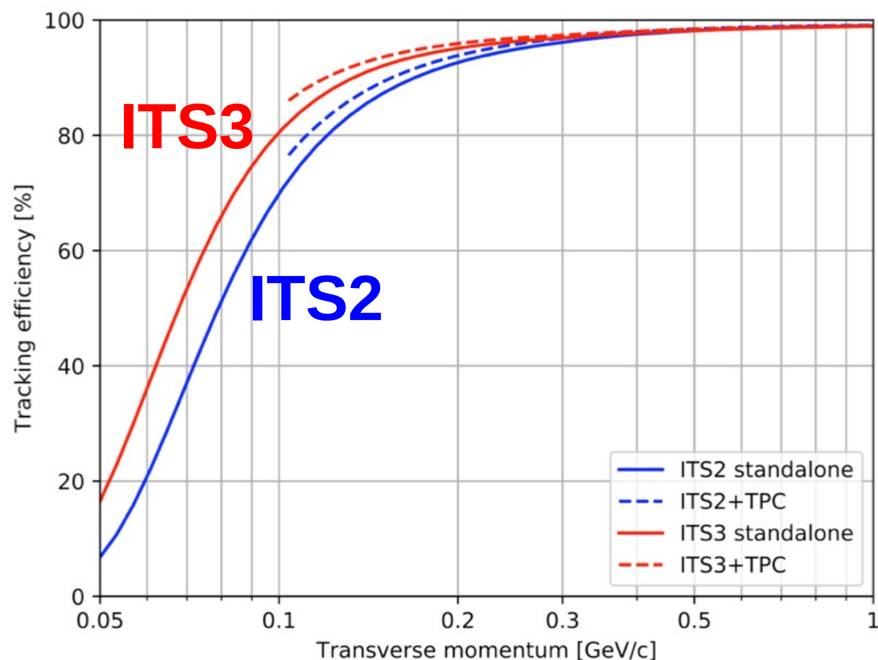
Gain in performance with ITS3





- **Improvement in pointing resolution by a factor of 2** over all momenta
- Increase of tracking efficiency for low-p_T particles and extension of the low-p_T reach

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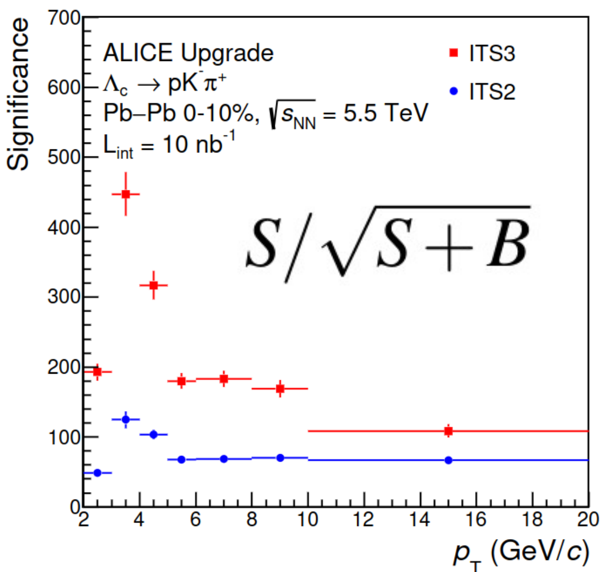
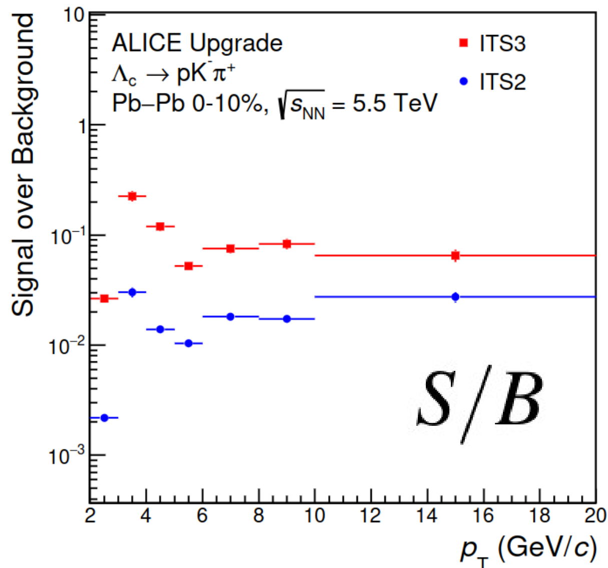
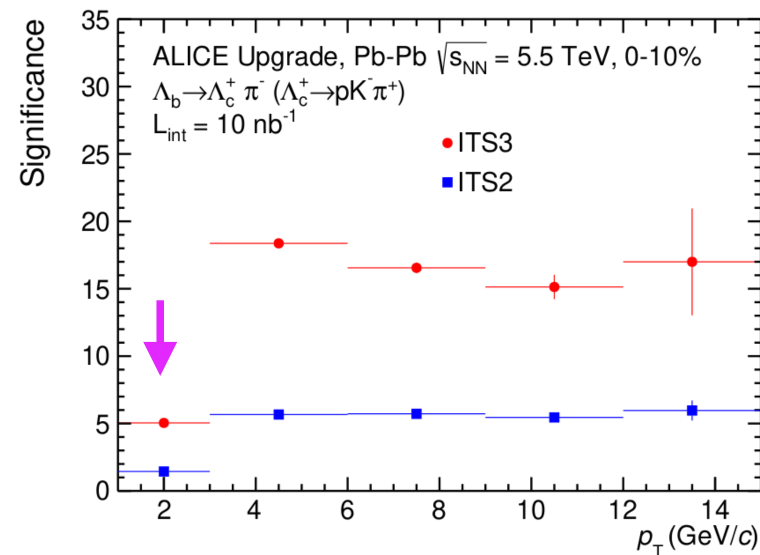
Low-p_T heavy-flavor baryons with ITS3

$\Lambda_c^+ \rightarrow p\, K^- \pi^+$ ($c\tau \sim 59\ \mu m$)

Λ_b^0 via non-prompt Λ_c^+ ($c\tau \sim 369\ \mu m$)







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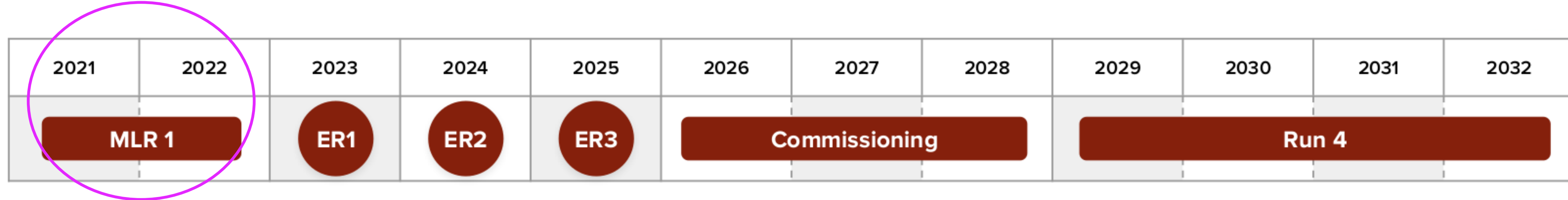
ITS3 R&D lines

- **Sensor design in 65 nm CMOS technology**
- **Bending of thin silicon sensors & their characterization**
- **Mechanical support**

  - Development of assembly procedure

  - Study of carbon foam support structure
- **Air cooling**

Sensor Design



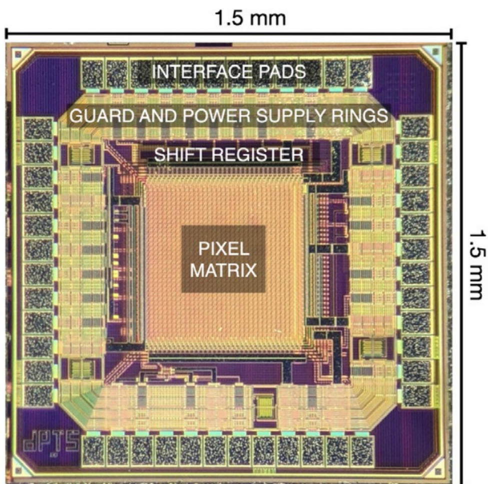
Multi Layer Reticle 1 (MLR1):

- Concentrated effort ALICE ITS3 together with CERN EP R&D
- 3 process variants:

  - *DPTS – Digital Pixel Test Structure*
  - *APTS – Analog Pixel Test Structure*
  - *Circuit Exploratoire 65 nm*

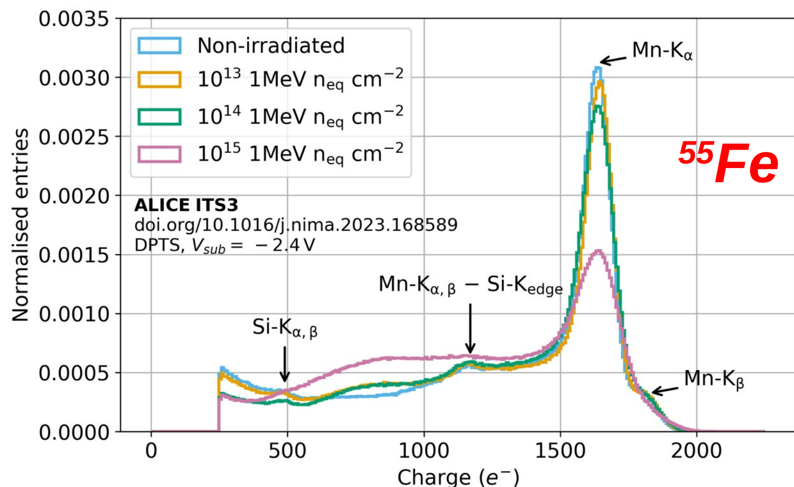
More details in talk by Anna Villani on Wed 18th Oct at 11:30

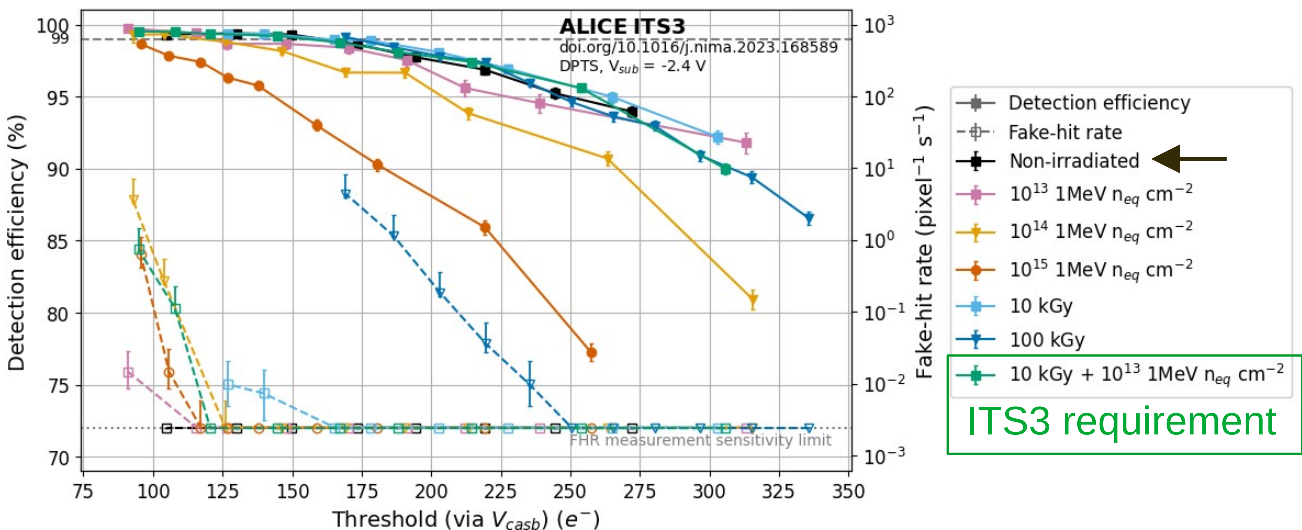
Characterization of DPTS



- DPTS 32x32 pixels
- Pixel pitch 15 μm
- Performance of in-pixel front end

ALICE ITS, NIM A 1056 (2023) 168589

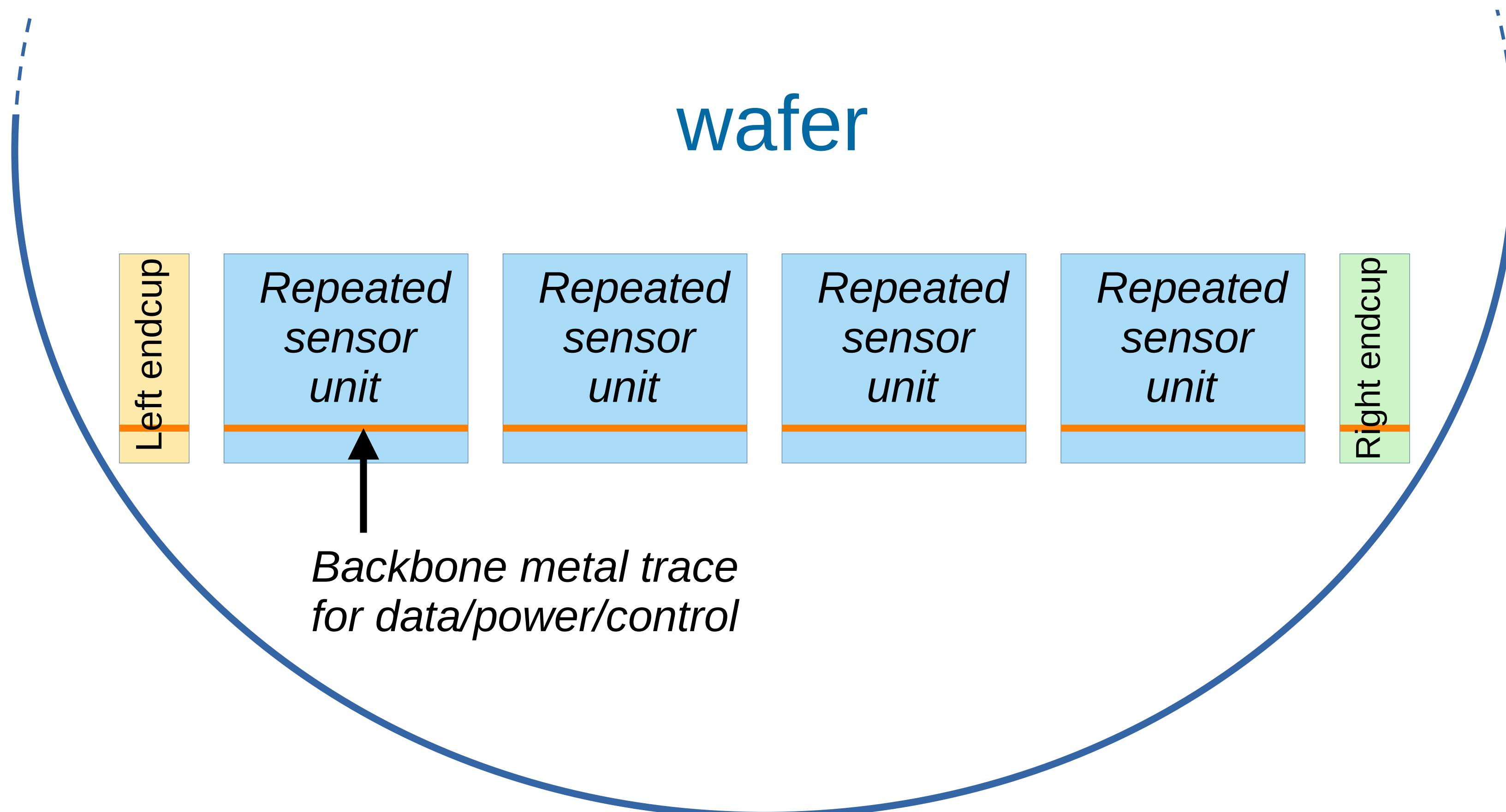




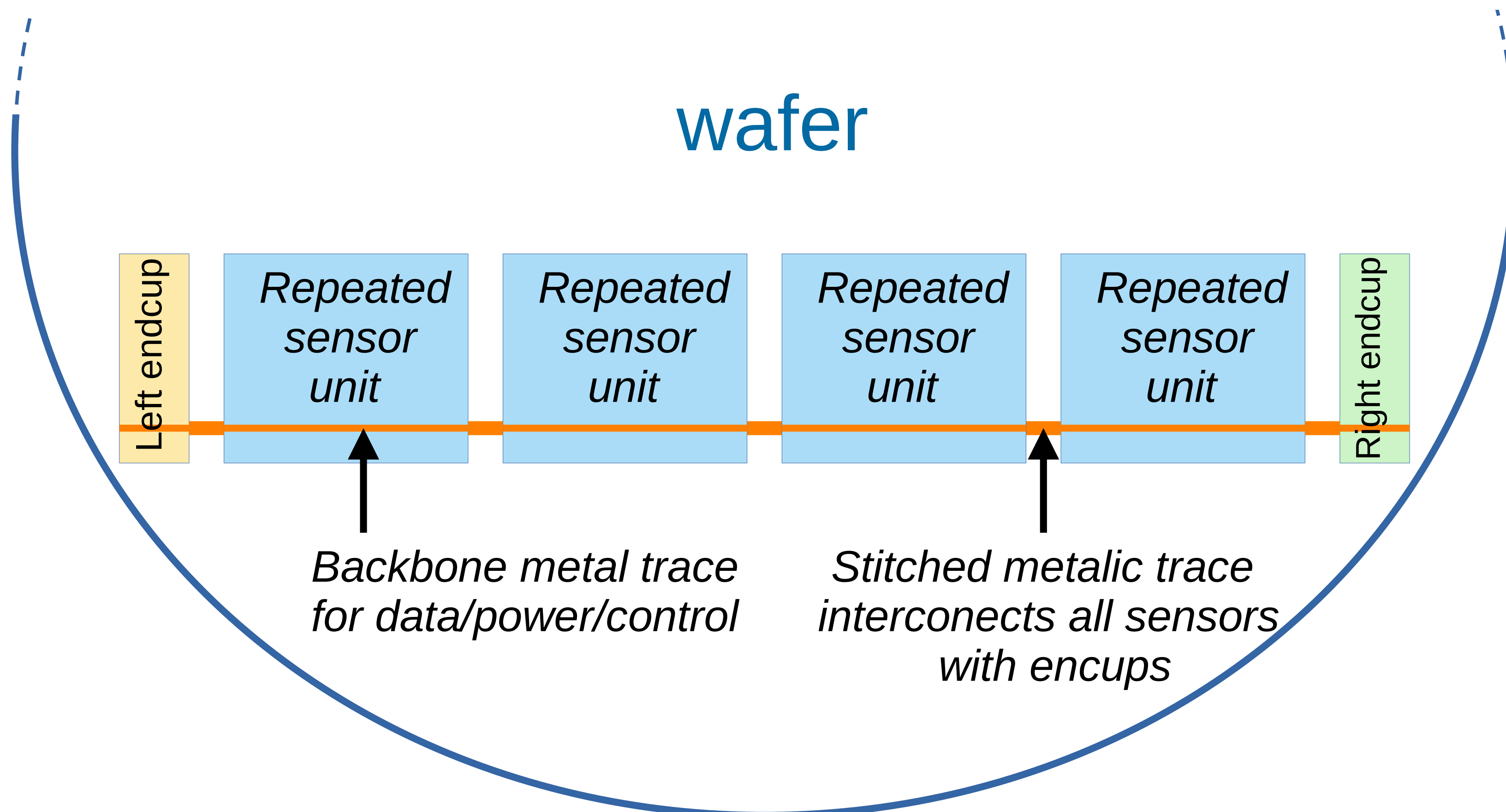
DPTS is sufficiently radiation hard for ITS3

More details in talk by Anna Villani on Wed 18th Oct at 11:30

Stitching in nutshell



Stitching in nutshell



Exploration of sensor stitching on 300 mm wafers in Engineering Round 1

2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032
MLR 1		ER1	ER2	ER3	Commissioning			Run 4			

ER1 targets to explore:
- Stitching in one direction for metal traces of power and data buses
- Production yield
- Power distribution and consumption
- Readout over long distances (26 cm)
- Pixel architecture

ER2: final sensor prototype

ER3: final sensor production

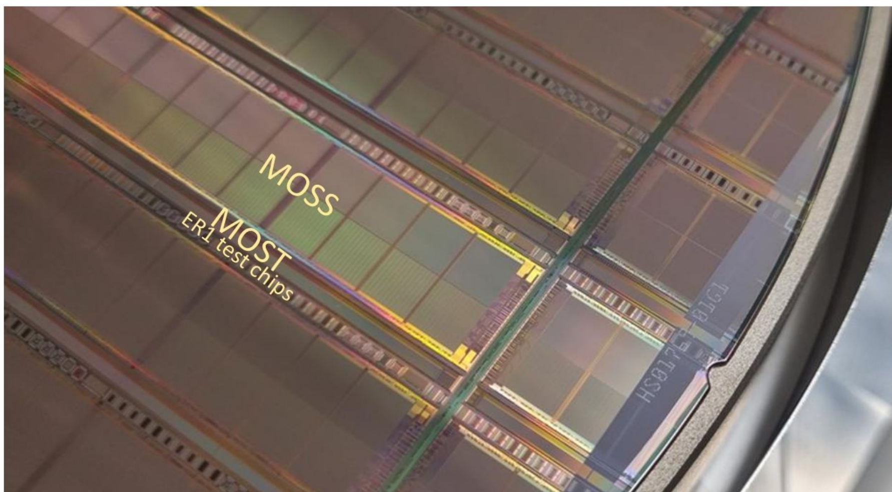
Stitching on 300 mm wafers for 65 nm CMOS technology

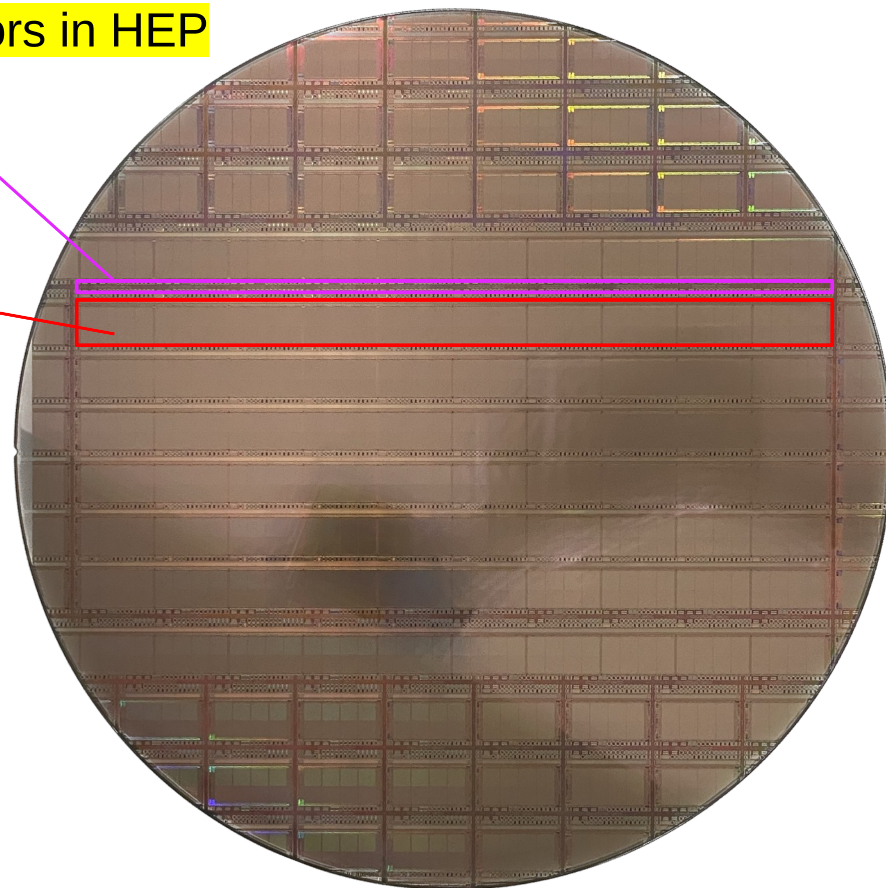
Monolithic Stitched Sensors

First stitched sensors in HEP

Monolithic Stitched sensor with Timing (MOST)
- Size: 2.5 x 259 mm, 0.9 MPixel, digital readout

Monolithic Stitched Sensor (MOSS)
- Size: 14 x 259 mm, 6.72 MPixel, digital readout

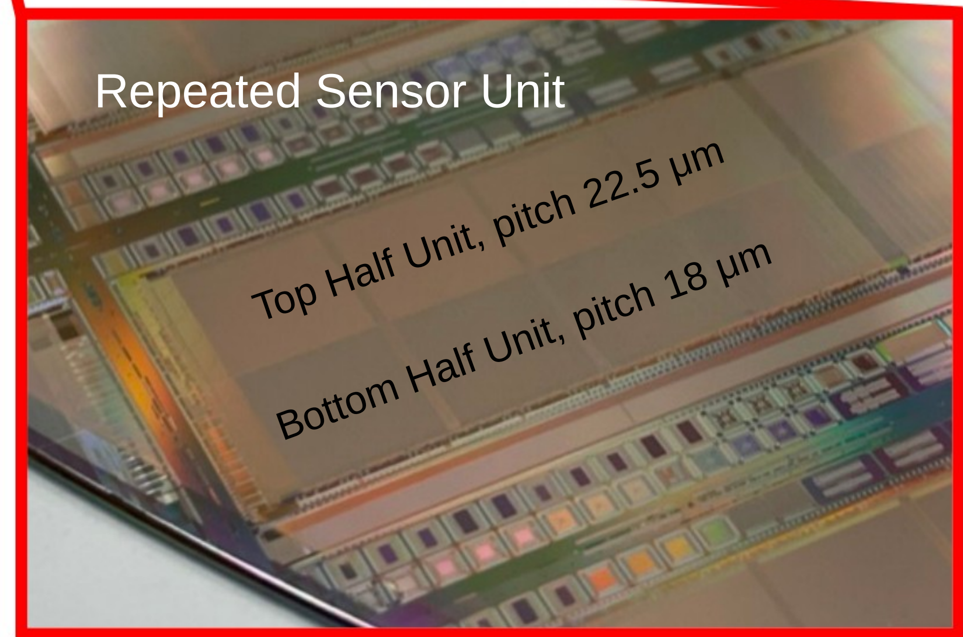




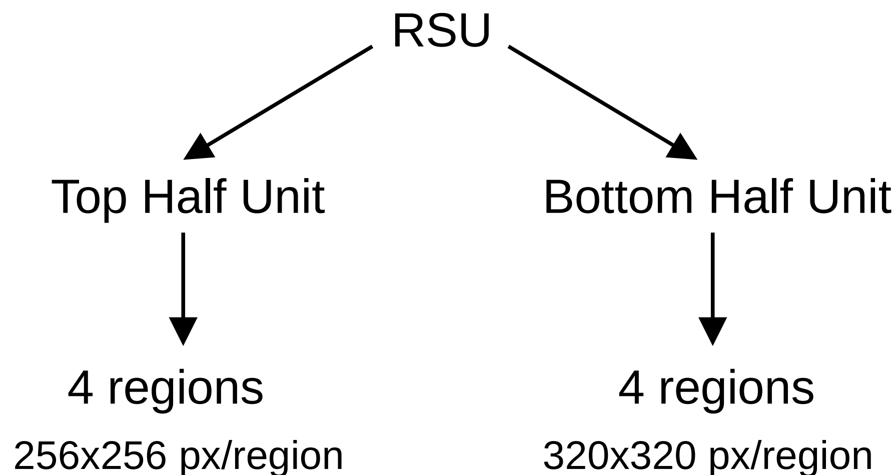
ER1 wafer ∅ 300 mm

MOSS = Monolitic Stitched Sensor

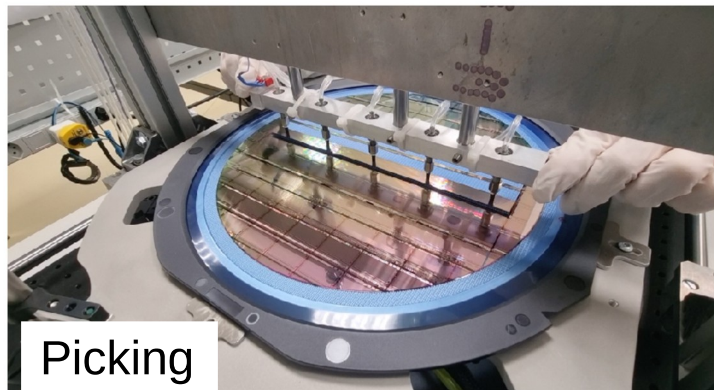
6.72 MPixel

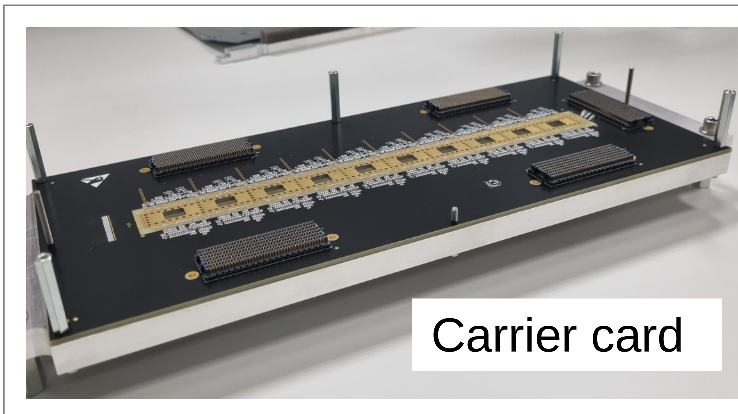


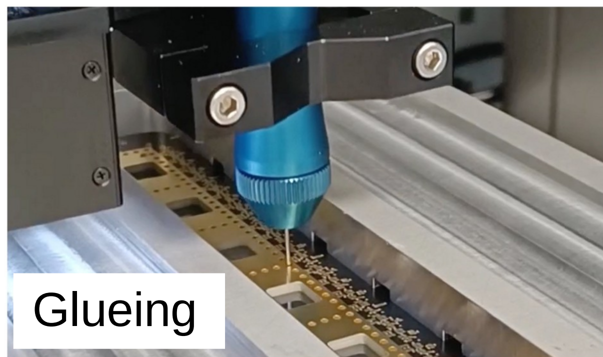
10 Repeated Sensor Units (RSU)

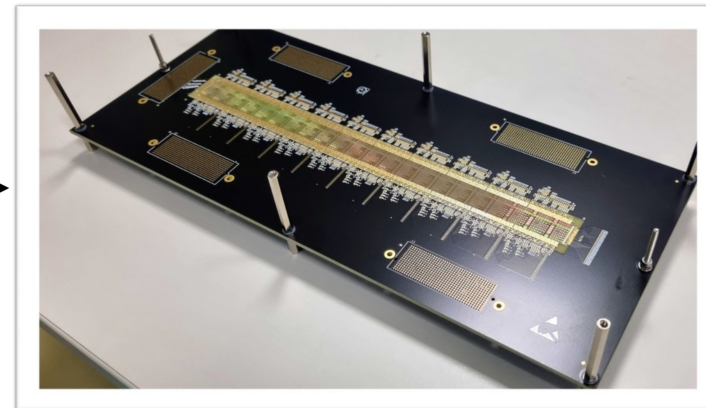


Assembling chip carrier card with MOSS

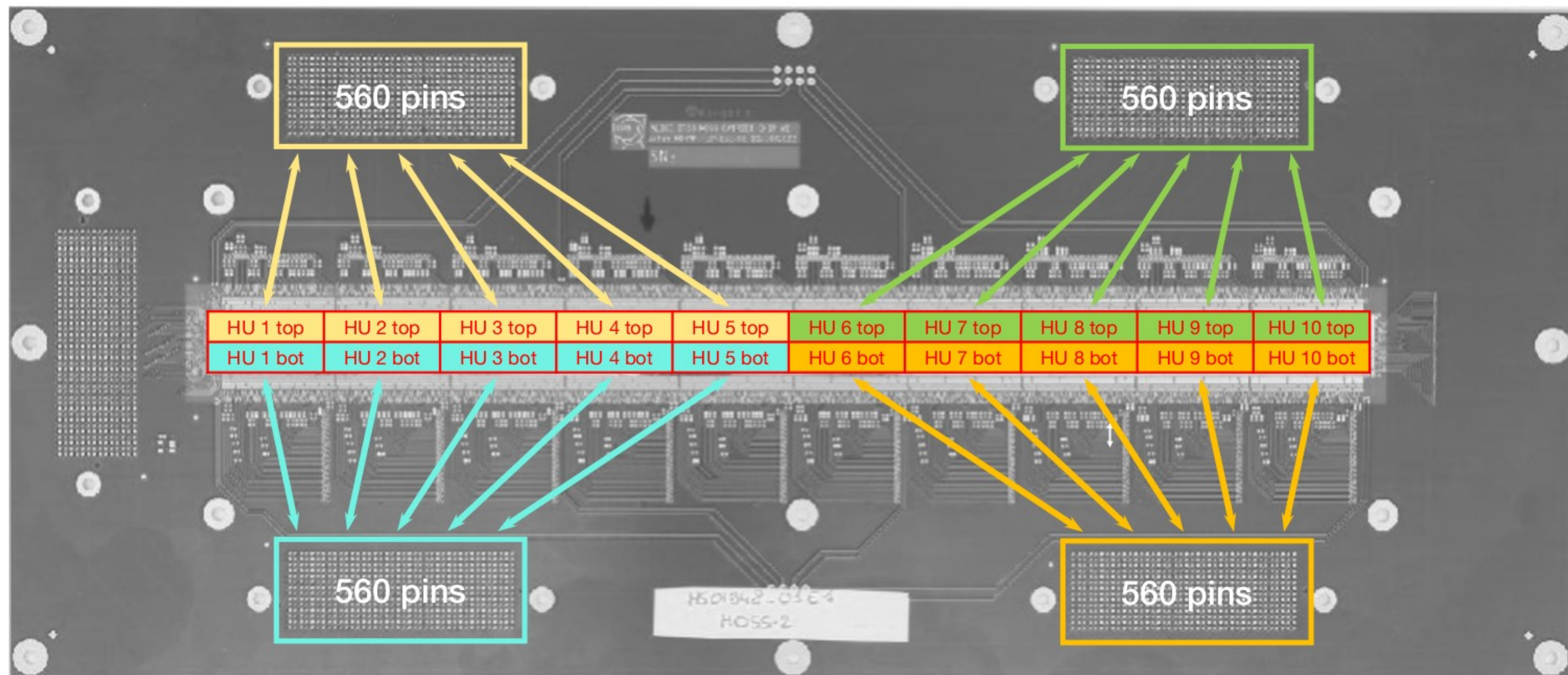




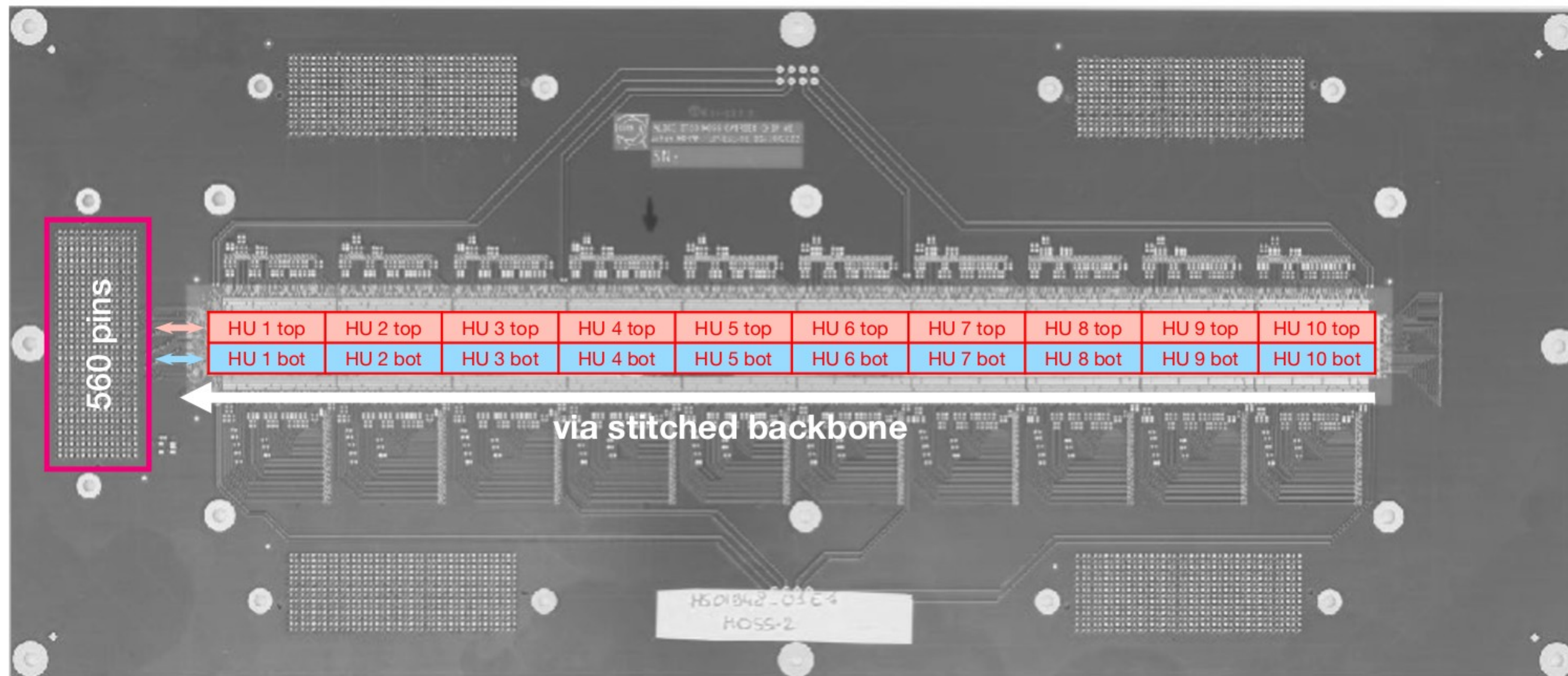




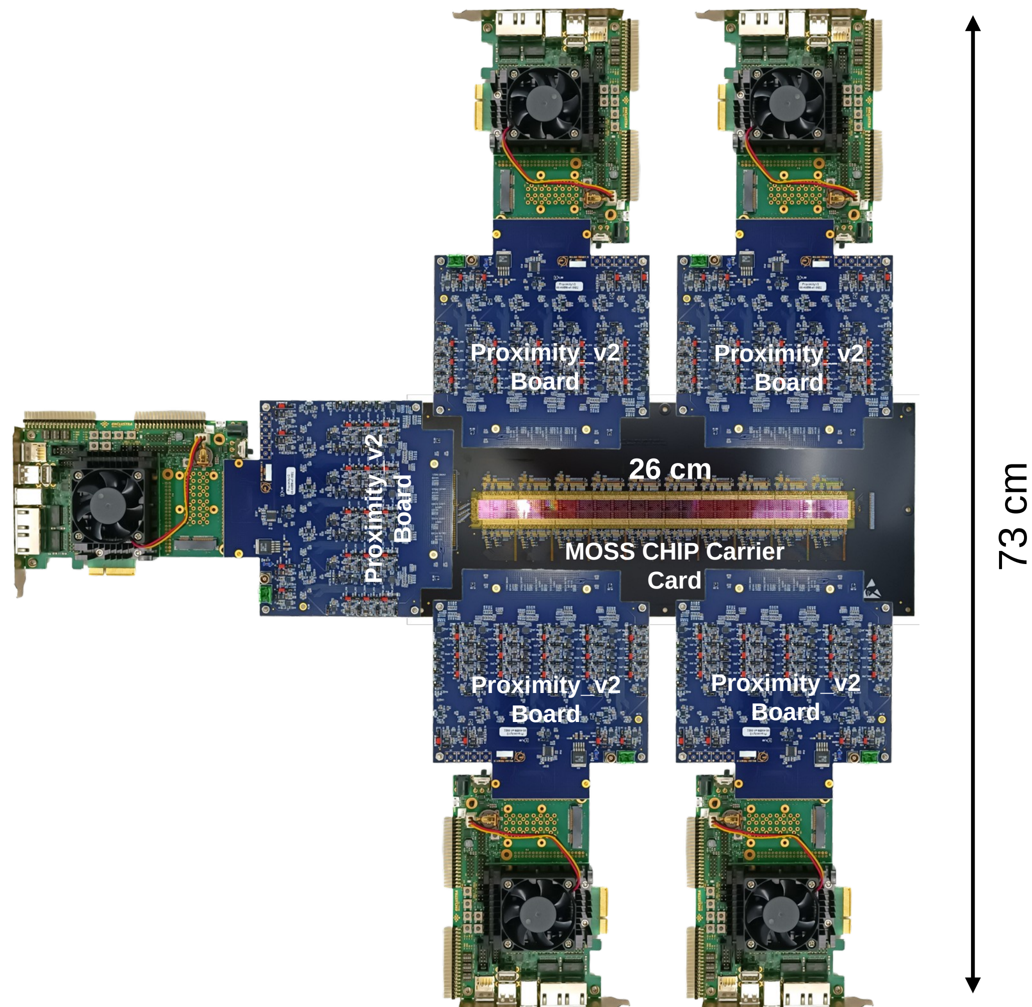
MOSS carrier card



MOSS carrier card



Full MOSS chip test system concept

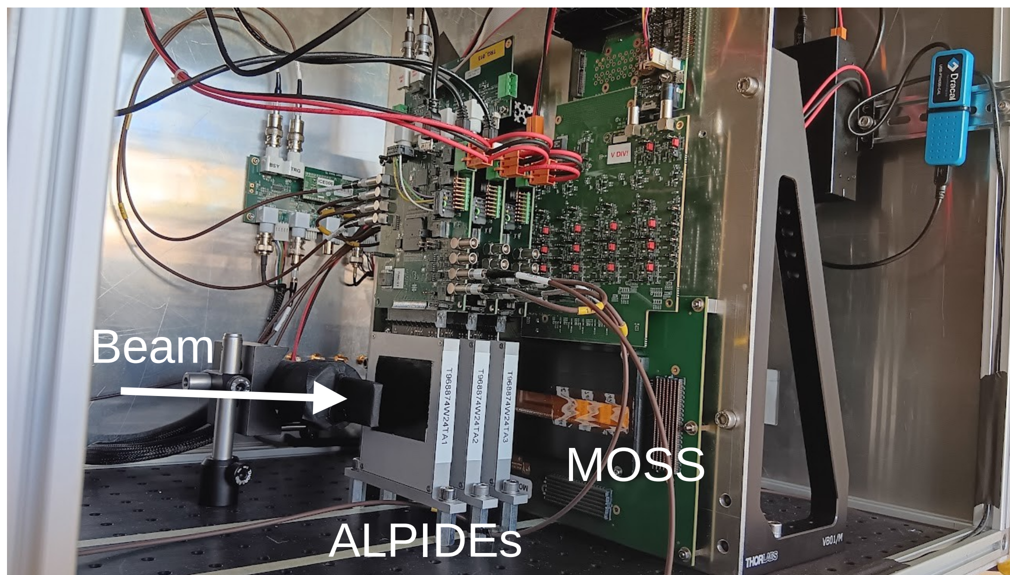


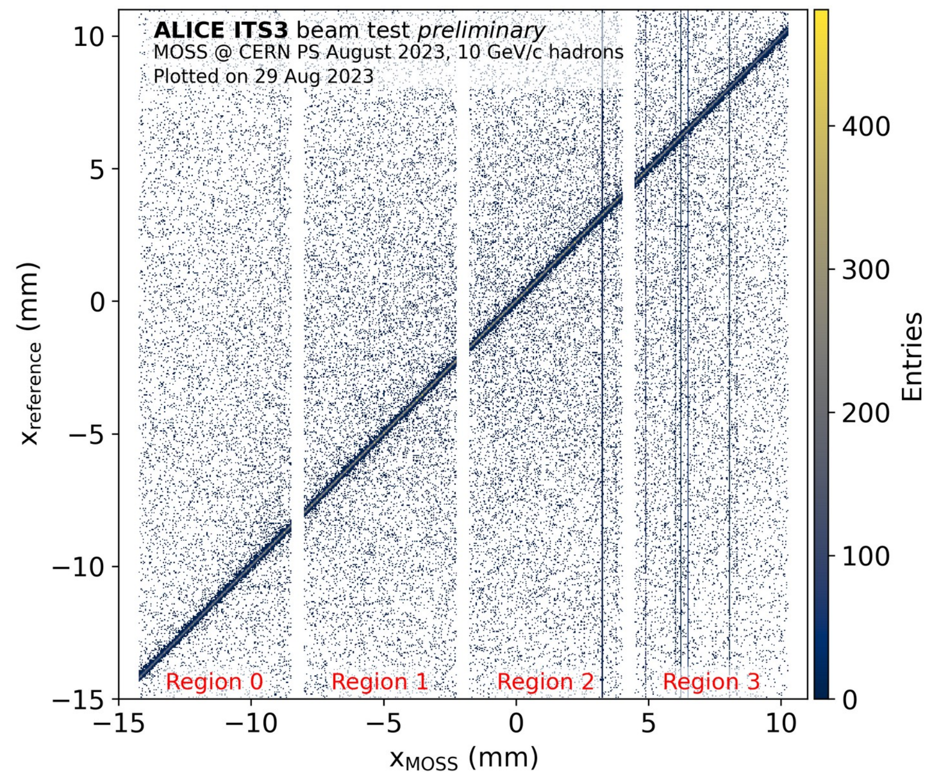
The concept foresees 3 different cards.

- **MOSS-CHIP carrier card**
  2800 pads
- **5x Proximity Board**
  1 card x 4 quadrants + 1 for stitched backbone
  supply of power, control, readout, ADCs
- **5x automation and readout modules**
  steers the proximity boards and interfaces the sensor control and readout with a computer.

Ongoing tests:
- resistance
- power ramps
- test beams

MOSS chip in test beam





Practicing ITS3 assembly

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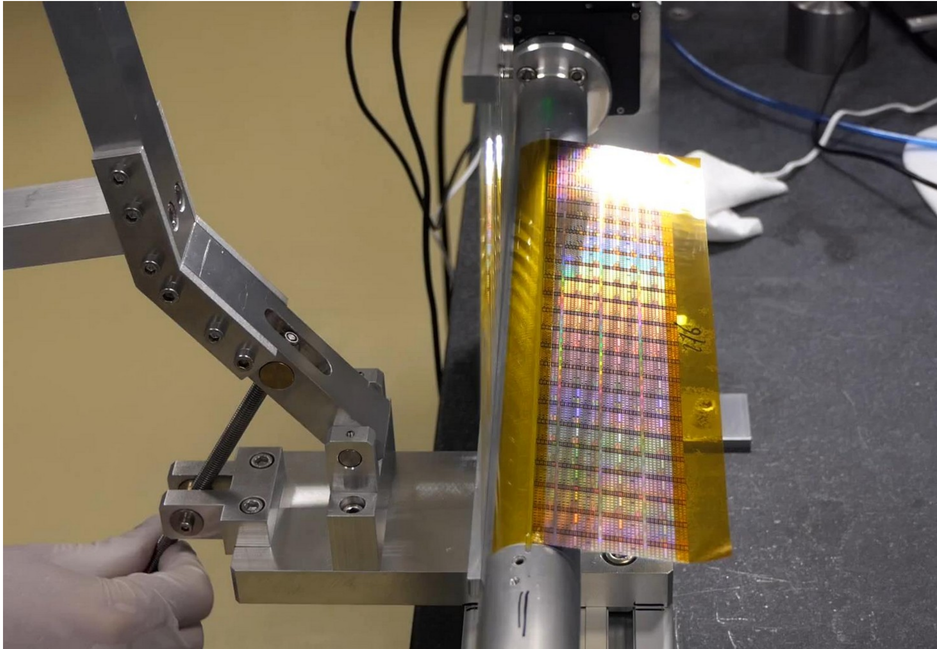
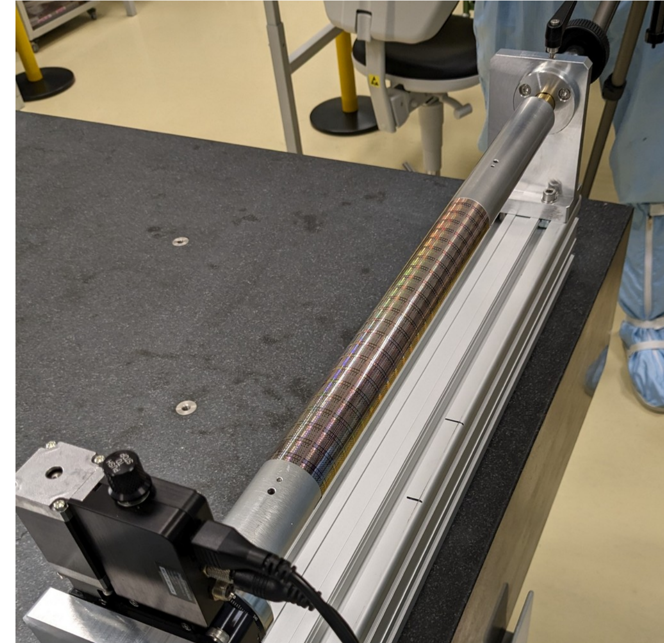
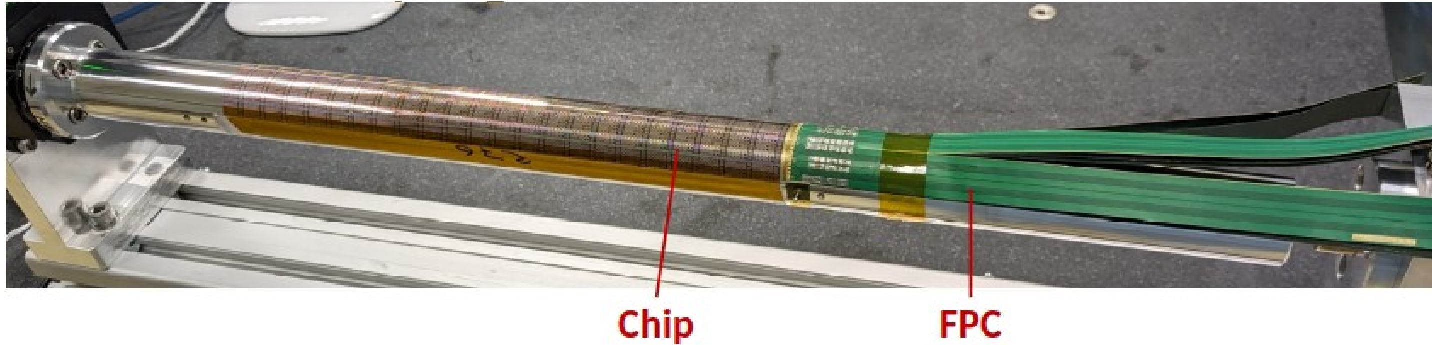
Bending full scale chip, 50 μm thick to radius 19 mm

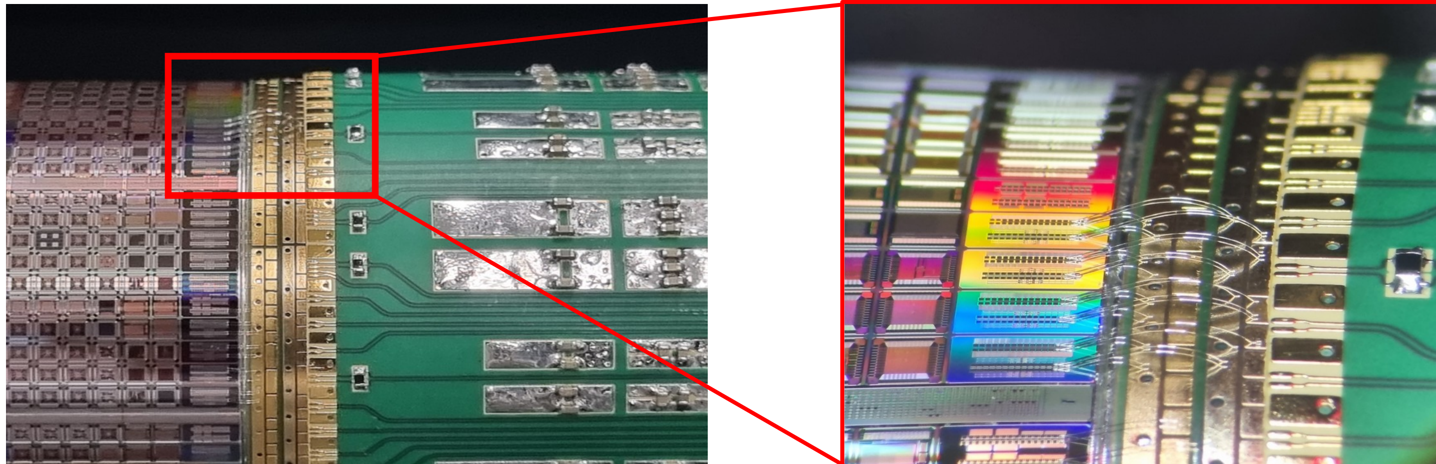




Practicing ITS3 assembly



Aligning FPC and the sensor

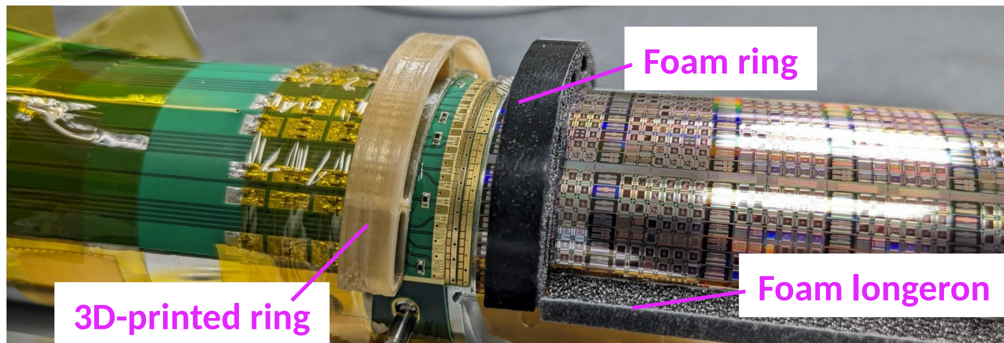


Bonding the curverd sensor

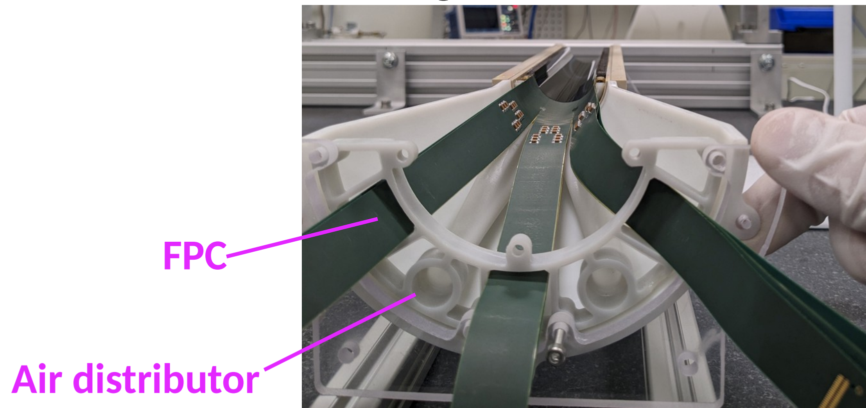
Practicing ITS3 assembly

ALICE

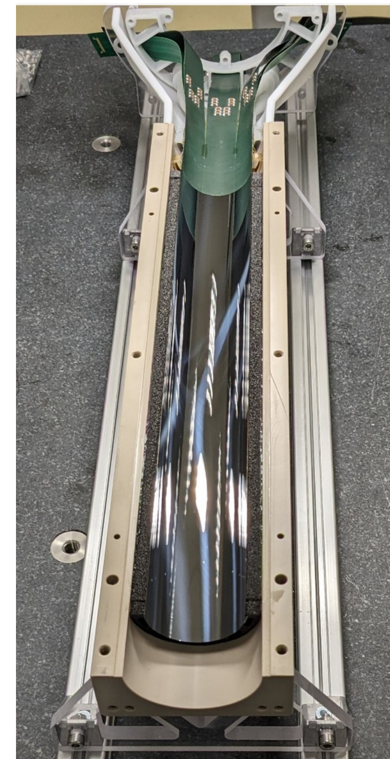
Gluing of foams and additional supports



Gluing of the air distributor

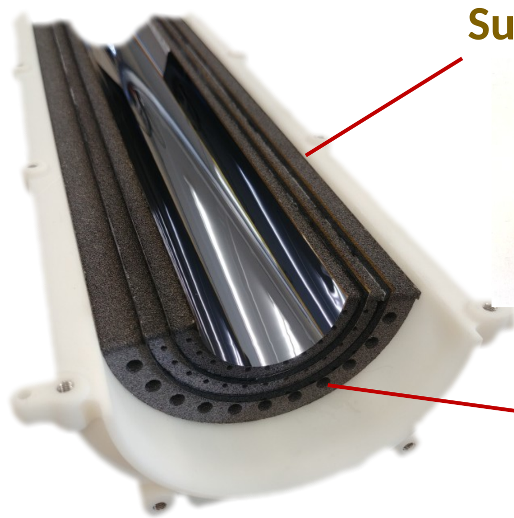


Assembled first layer of ITS3



Mechanics and cooling solutions

- Limited dissipated power ⇒ **air cooling** at ambient temperature
- Low material budget ⇒ **carbon foam** used as **support** and **heat exchanger**



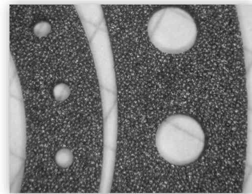
Support

ERG Carbon
@Duocel

ρ = 0.045 kg/dm^3

k = 0.033 W/m·K

Support & **cooling**



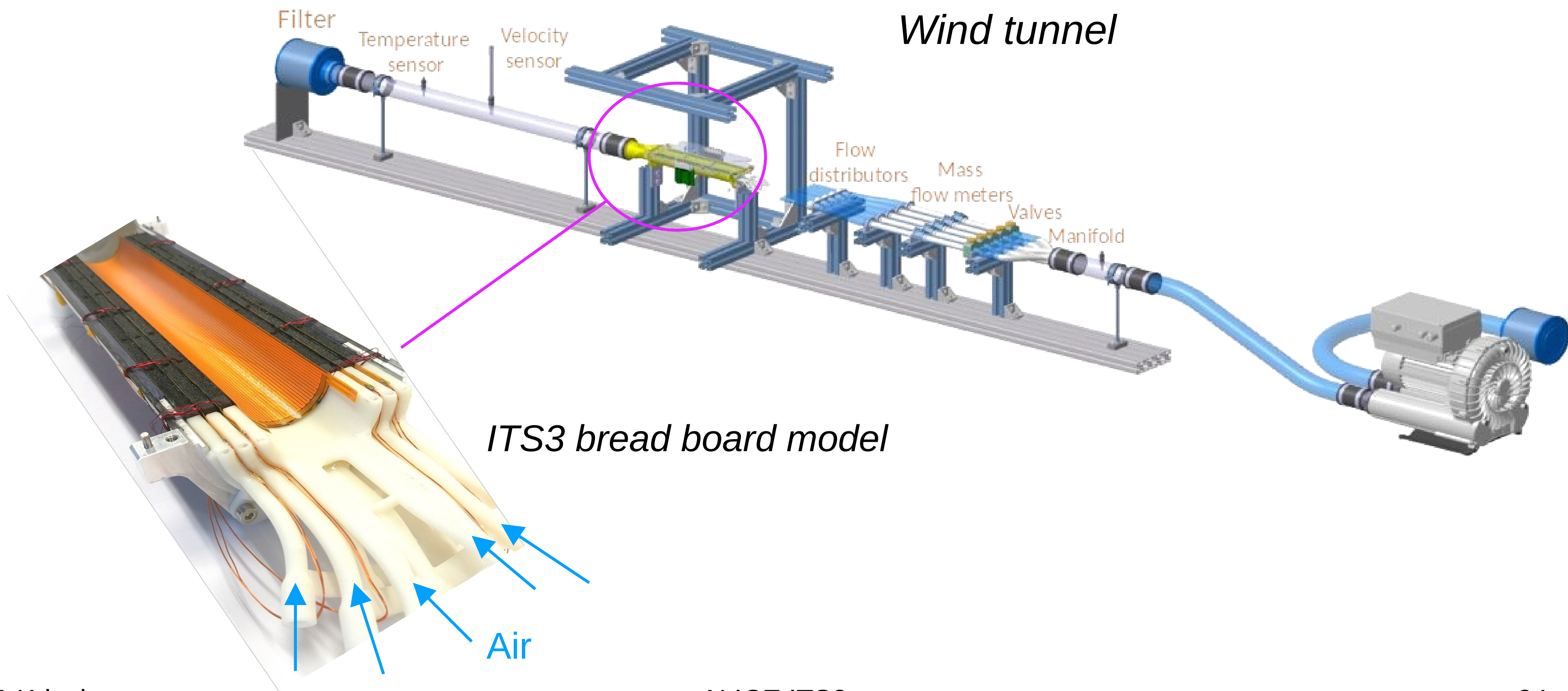
K9

ρ = 0.2-0.26 kg/dm3

k = >17 W/m·K

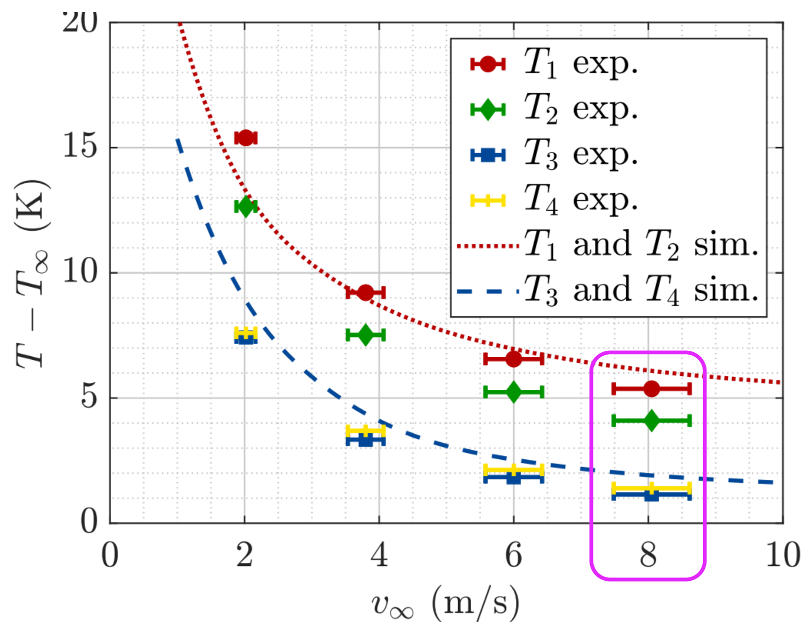
Higher thermal conductivity but also higher density

Thermal and mechanical stability tests

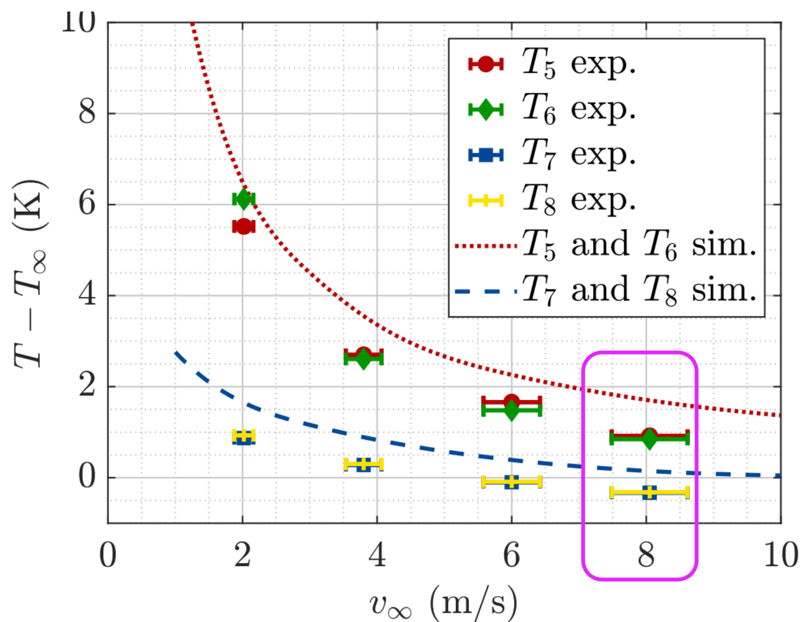


Air cooling

Locations of temperature sensors



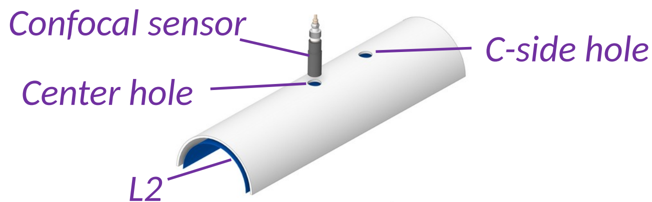
(b) Layer 0 - Endcap

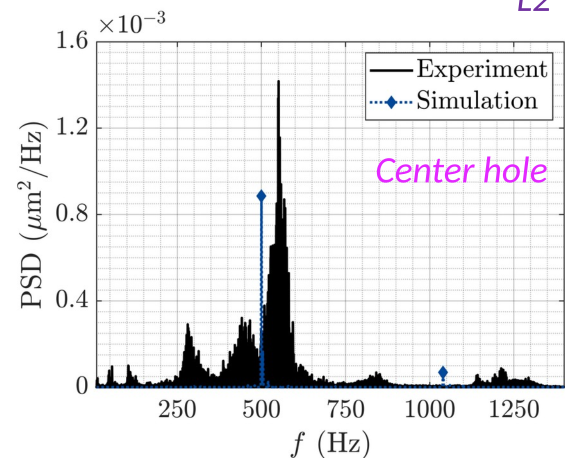


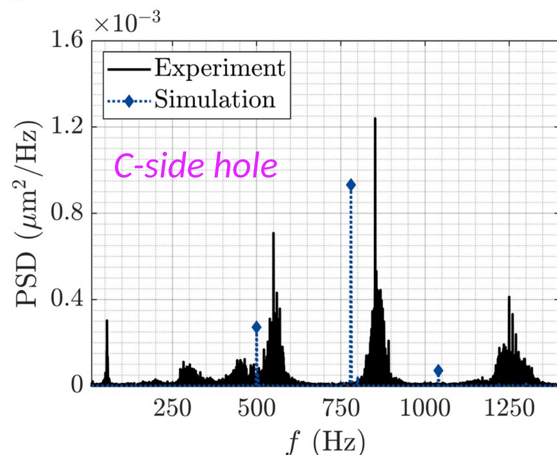
(c) Layer 0 - Matrix

- Sensor temperature must stay < 30 ˚C $\Rightarrow$ 8 m/s room temperature air flow needed
- Good agreement with Computational Fluid Dynamics model

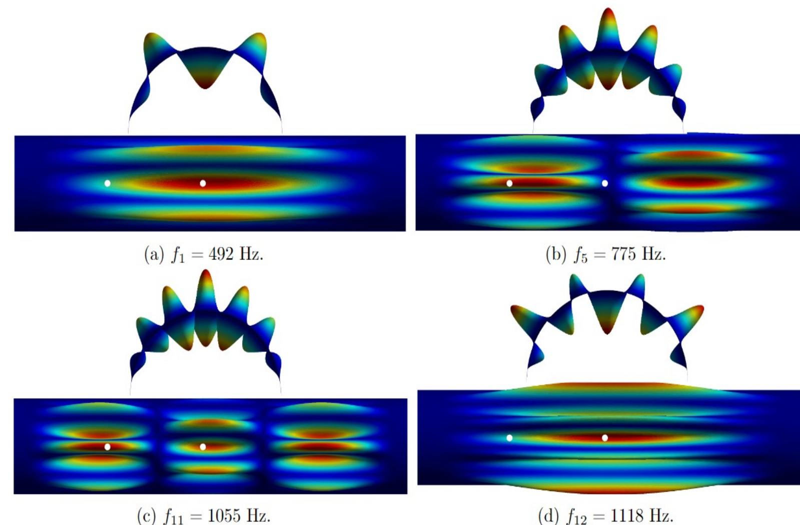
Vibrational tests







Power spectral density of the displacements of Layer 2

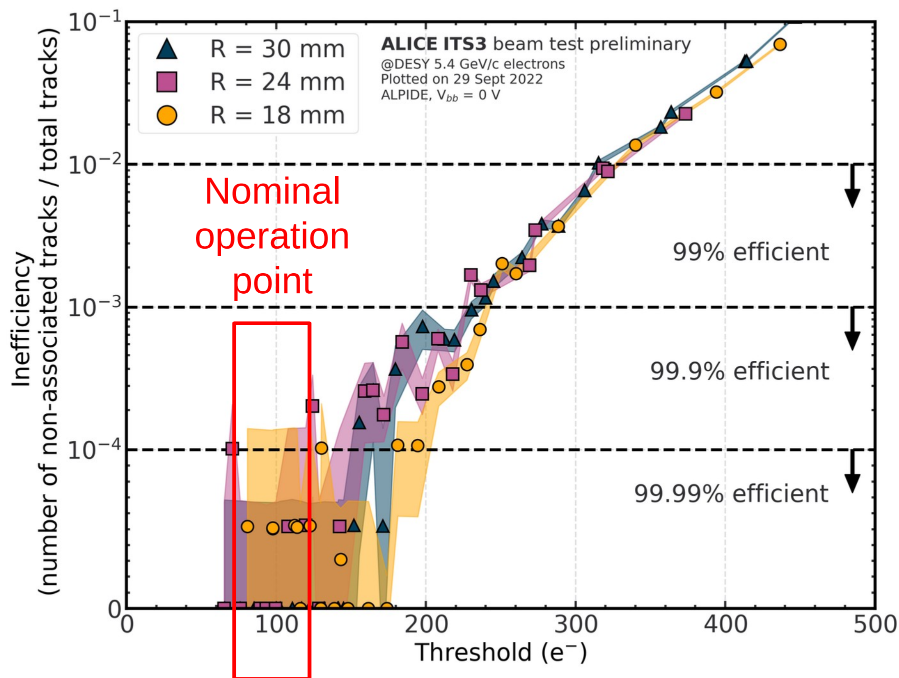


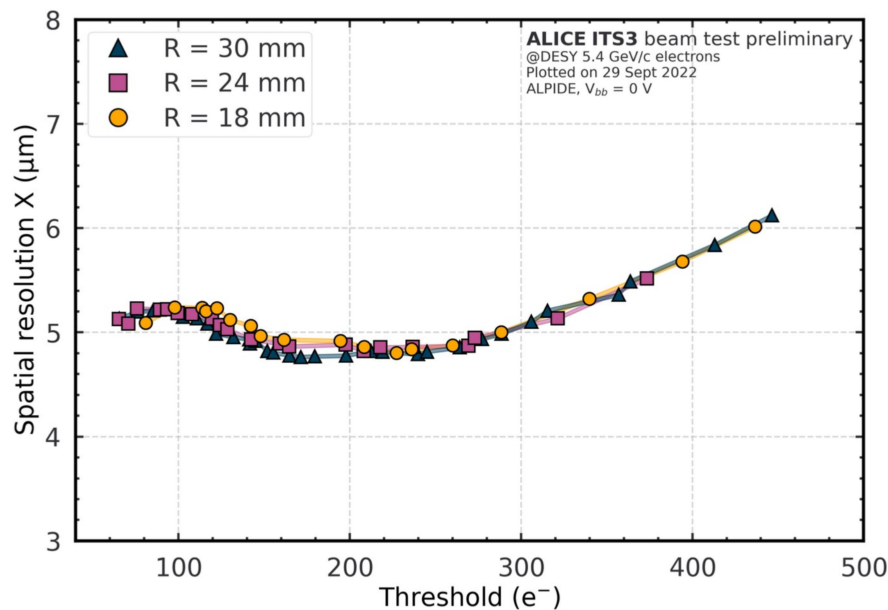
Side and top view of natural frequencies of Layer 2.

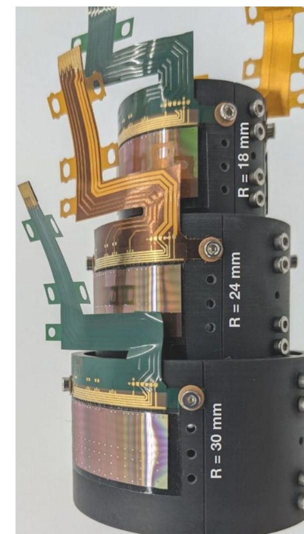
- First natural frequency of L2 with integrated heaters 500 Hz
- Simulation by Computational Fluid Dynamics model with decoupled fluid-structure interaction
- Displacements caused by the air flow < 0.5 μm

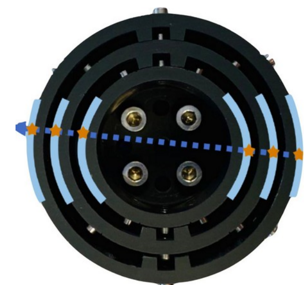
Characterization of bent sensors

- μITS3: 6 ALPIDE chips bent to the same radii as ITS3 layers
- Efficiency and spatial resolution are consistent with flat ALPIDE









See also ALICE ITS, NIM A 1028 (2022) 166280

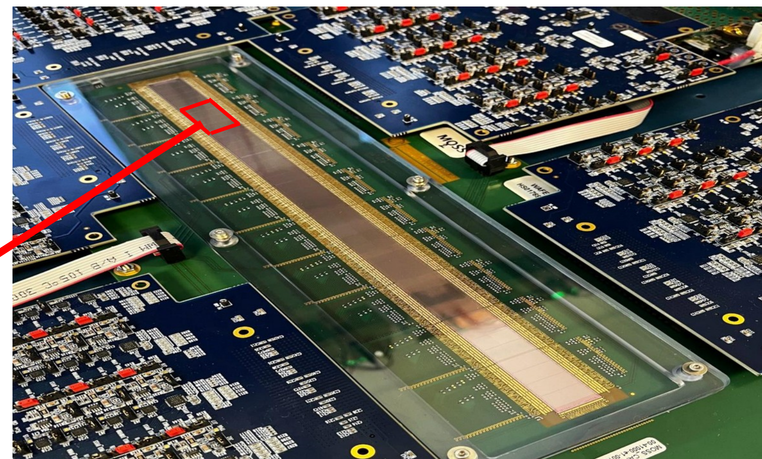
Summary

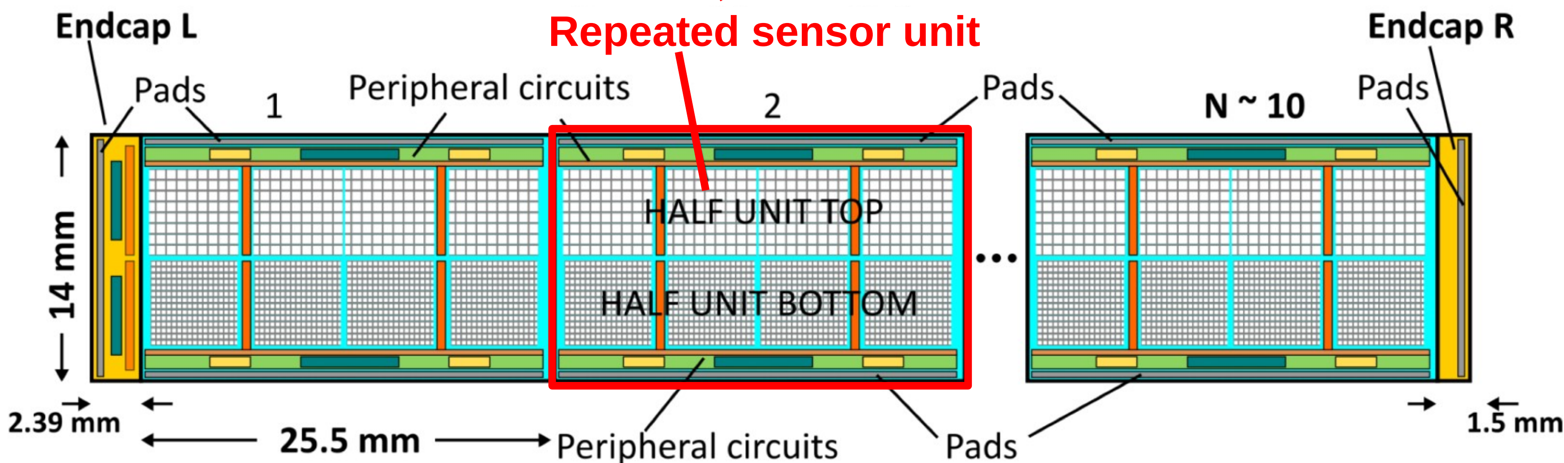
- Technology for ALICE ITS Inner Barrel upgrade for LHC Run 4:
  large scale, bent monolitic active pixel sensors
- R&D :
  - Silicon flexibility and bending proved with routine bending tests
  - Bent and flat sensors have compatible performance
  - Sensors prototypes are radiation hard up to NIEL 10^{14} 1MeV n_{eq} cm^{-2}
  - Characterization of stitched sensors ongoing
  - Investigation of the air cooling and associated vibrations ongoing
- ITS3 R&D paves the way to thin, low-power sensors for the use in future ALICE3

Backup

Monolithic Stitched Sensor

- Size: 14 x 259 mm, 6.72 MPixel
- 10 Repeated sensor units
  - Top half unit pitch: 22.5 x 22.5 μm^2
  - Bottom half unit pitch 18 x 18 μm^2





Reconstruction of hypernuclei with ITS3

$$^{4}_{\Lambda}\mathrm{He} \rightarrow {}^{3}\mathrm{He} + \mathrm{p} + \pi^{-}$$

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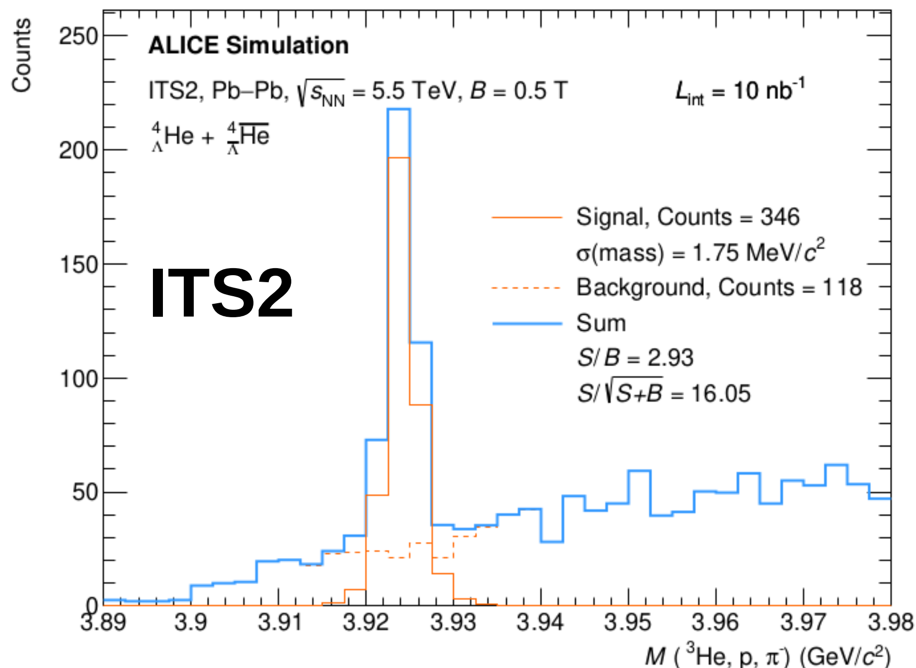
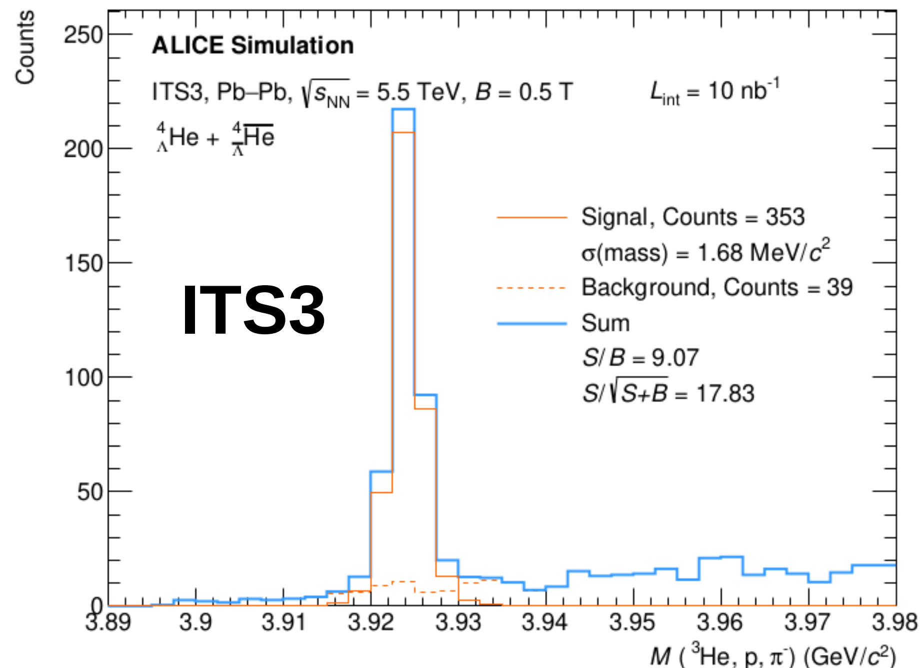
ITS3 improves impact parameter measurements of daugher ^{3}He decay





TPSCo 65 nm CMOS: benefits & features

Tower Partners Semiconductor Company (TPSCo)

- Benefits of 65 nm vs 180 nm

- smaller feature size $\Rightarrow$ better spatial resolution
- larger wafers: 300 mm vs 200 mm $\Rightarrow$ final sensor 27 $\times$ 9 cm^2
- lower voltage : 1.2 vs 1.8 V $\Rightarrow$ lower power consumption
- thinner sensitive layer (~ 10 μm) $\Rightarrow$ lower material budget

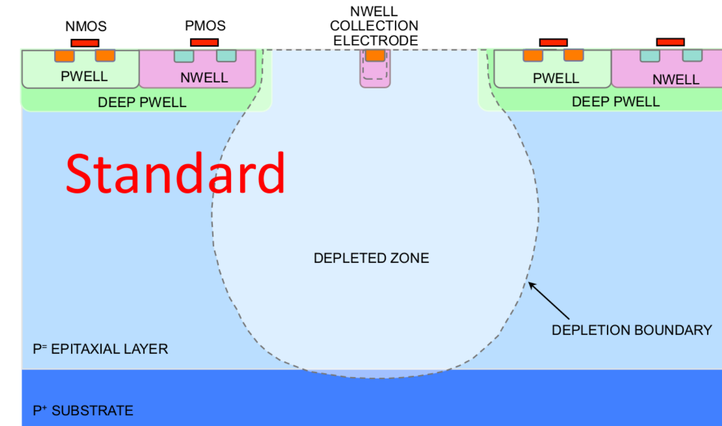
- Provides 2D stitching

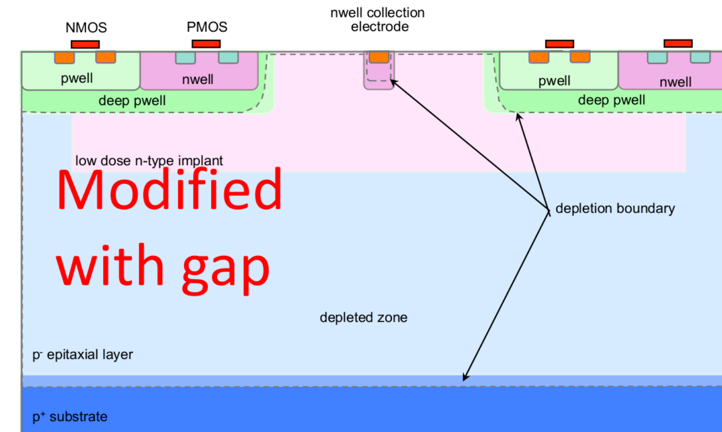
- 7 metal layers

- Process modification for full depleation introduced:

low dose n-type implant with gaps

- reduces charge sharing
- improves detection efficiency and speed





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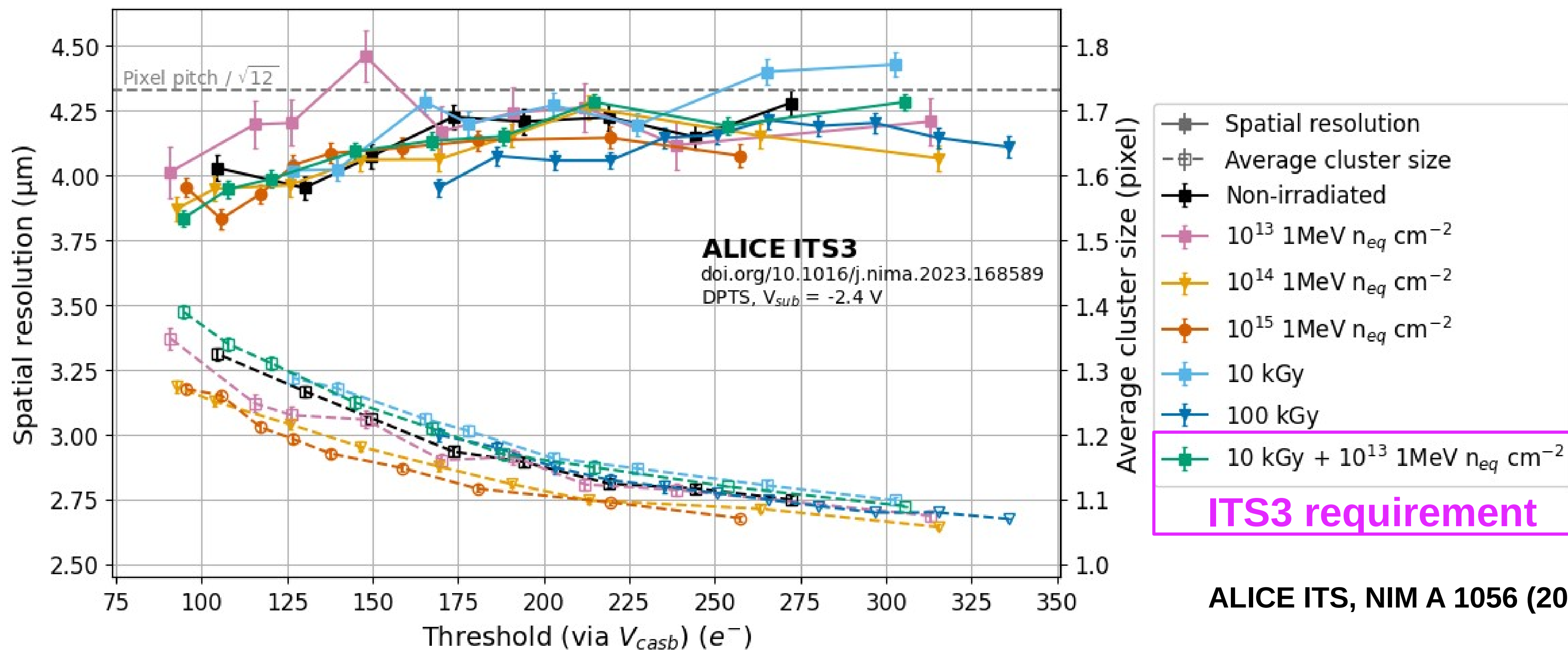
DPTS – Spatial resolution after irradiation



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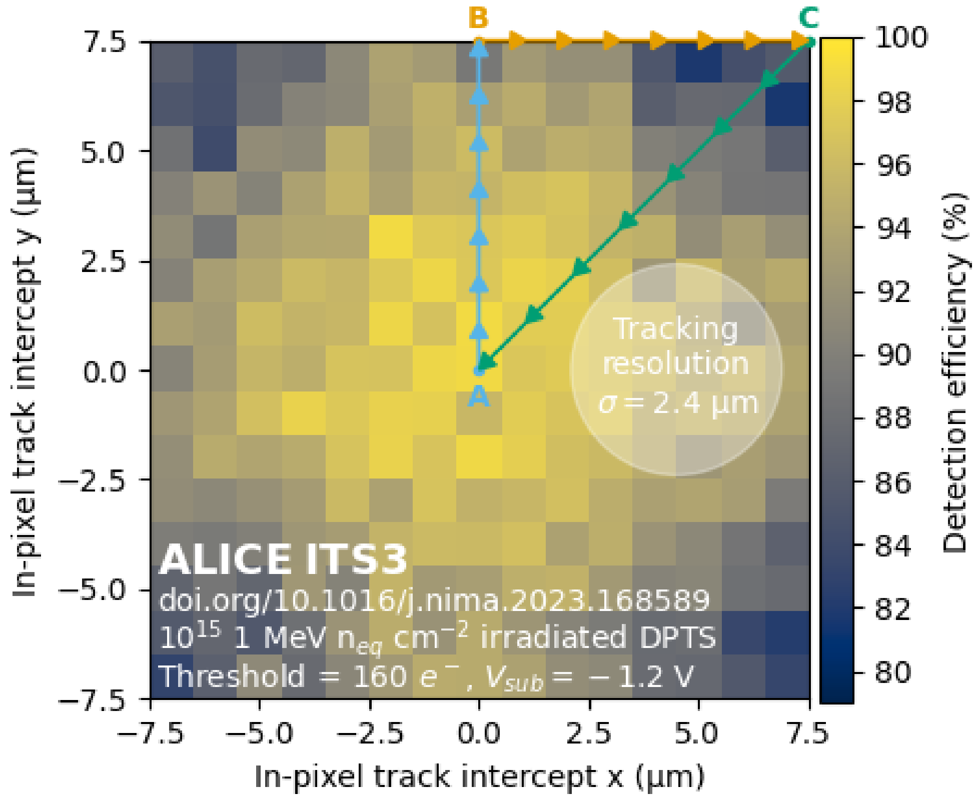
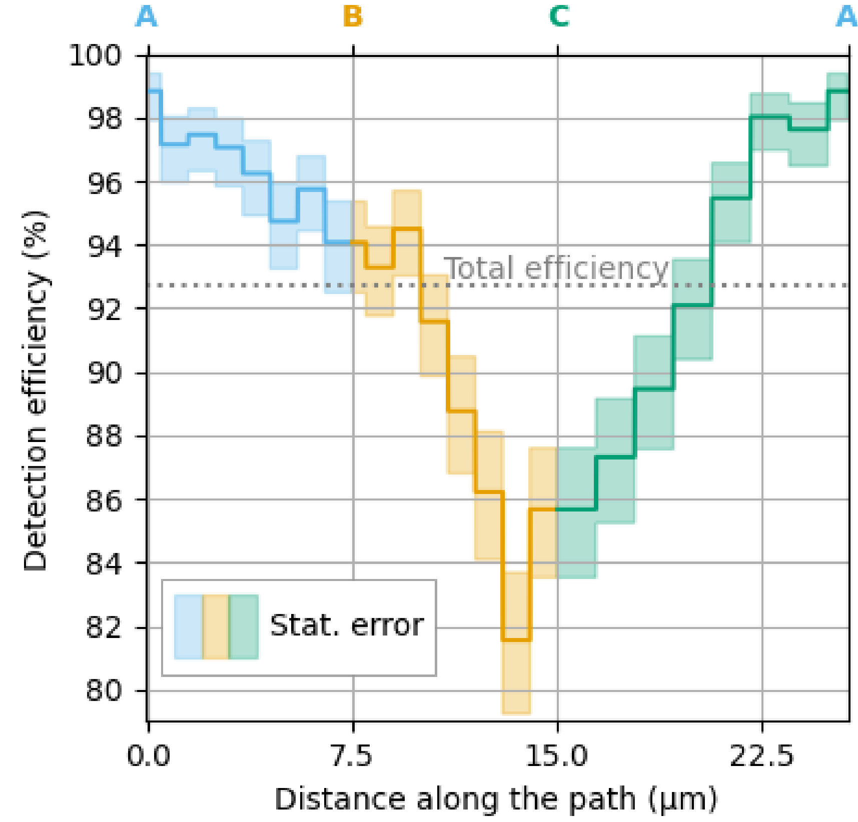
Irradiation does not have stong impact on performance

DPTS in-pixel efficiency for irradiated sensor





10^{15} 1 MeV n_{eq} cm^{-2} irradiated sensor
160 eV threshold
10 GeV positive hadrons

Efficiency losses in pixel corners due to charge sharing

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