Precision Timing with the CMS MIP Timing Detector for High-Luminosity LHC

Giacomo Zecchinelli on behalf of the CMS collaboration

-

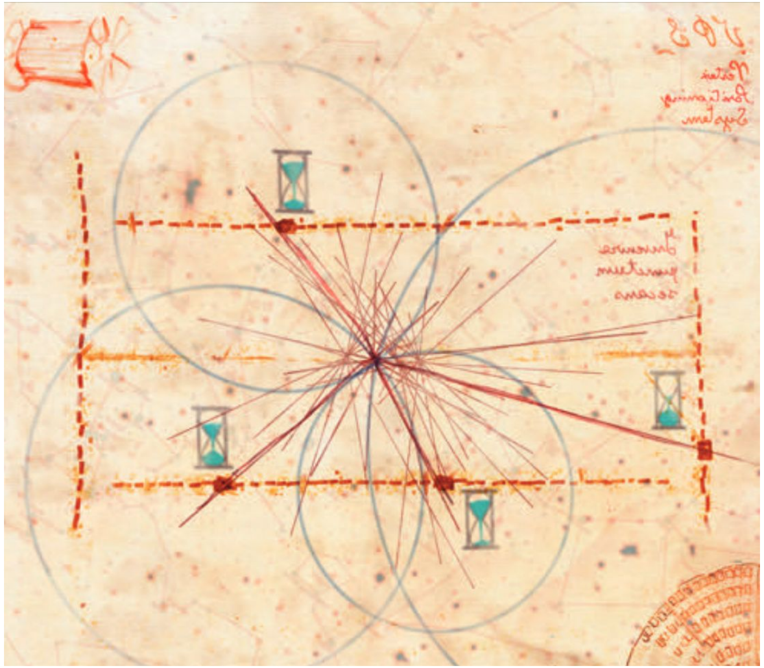
Vertex 2023 - Sestri Levante

17/10/2023

Outline

- Why timing matters
- CMS MIP Timing Detector
- BTL/ETL:
  - Sensors technology, design and performances
  - Electronics and services
  - Assembly and construction
  - Current status

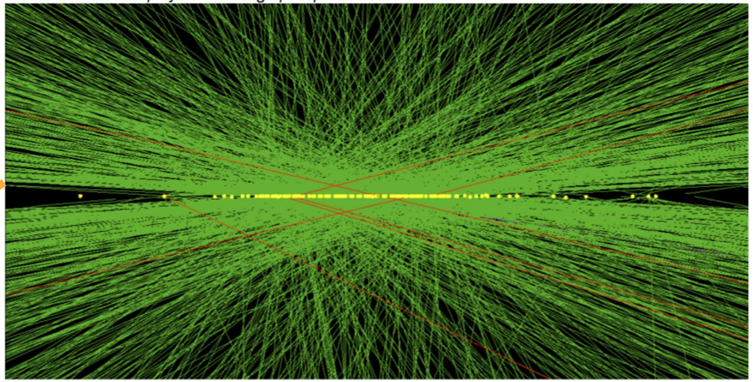
- Summary and Outlook

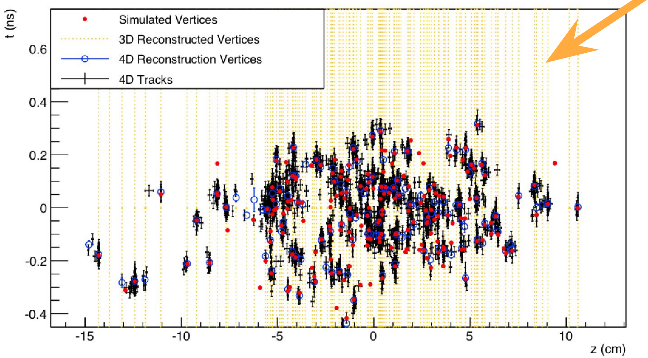


Timing matters

- LHC High Luminosity → large number of interactions per bunch crossing, from <μ> ~40 in Run2 to <μ> ~200
- LHC-HL starts in 2029!
- Timing information for tracks is needed to maintain Run2 physics performance
- CMS targets 30-50 ps per track

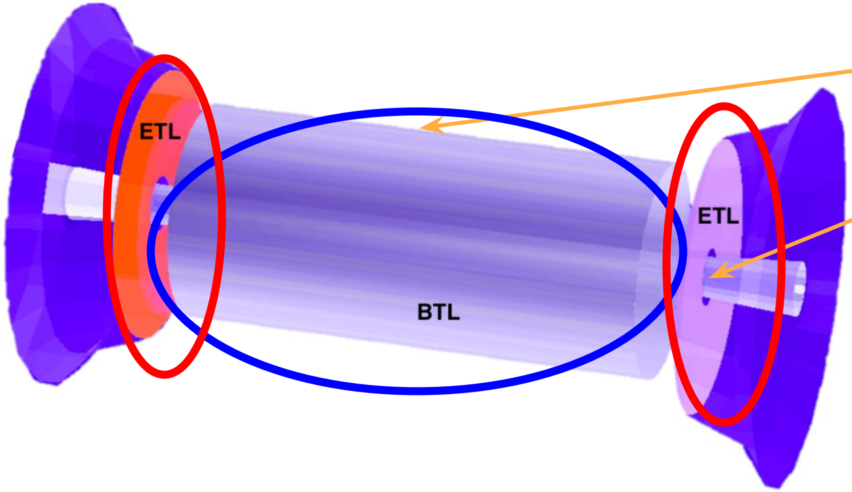
Simulated event display with average pileup of 140

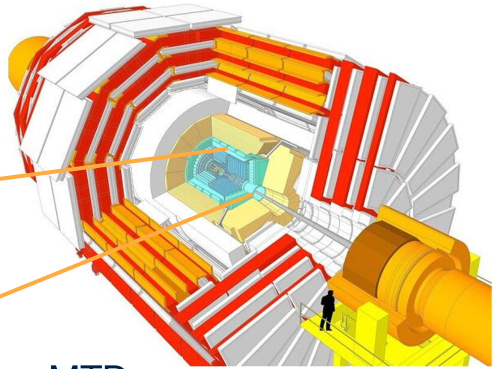




- Improving particle ID
- Extending CMS physics reach

CMS MIP Timing Detector





- MTD :
  - Almost hermetic design, $|\eta| < 3.0$
  - 50-60 ps resolution EoL
  - Barrel and EndCap have different needs

- Barrel Timing Layer - BTL :
  - Sensors: LYSO+SiPM
  - Inner radius: 1148 mm - 40mm thick
  - Length: ± 2.6 m
  - Fluence at 3000 fb^{-1} ~$1.7\times10^{14}\ n_{eq}/cm^2$

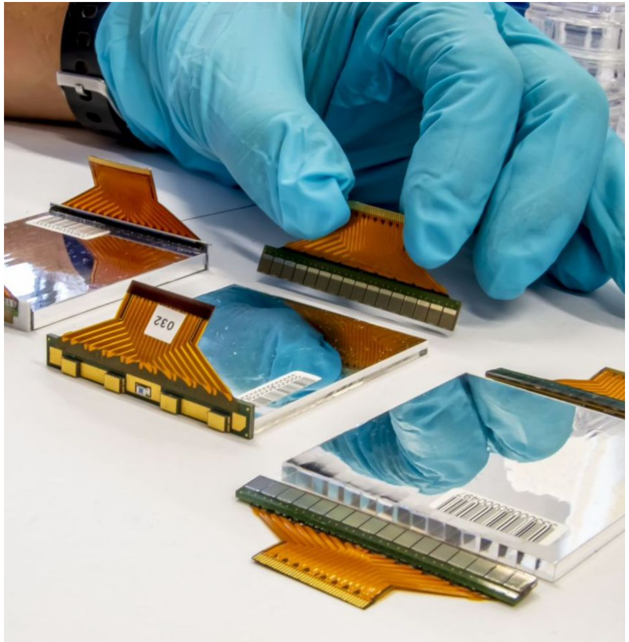
- EndCap Timing Layer - ETL :
  - Sensors: LGAD
  - Radius: 315 mm < r < 1200 mm
  - z-position 3.0 m - 45 mm thick
  - Fluence at 3000 fb^{-1} ~ $1.6\times10^{15} n_{eq}/cm^2$

BTL

BTL - Design

Challenges:

- Timing resolution goal: 30-40 ps at the beginning of operations, <60 ps up to 3000 fb^{-1}
- Radiation hardness: ~1.7×10^{14} n_{eq}/cm^2
- Maintenance free operation inside the tracker cold volume
- Covering ~38 m^2 of area

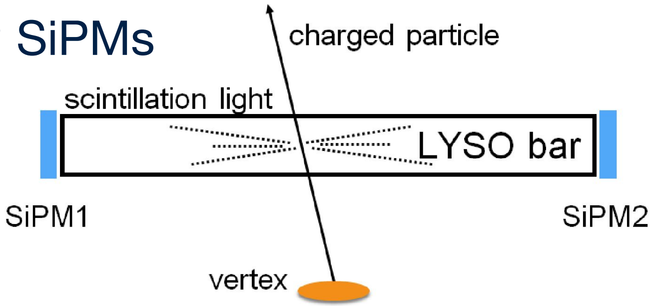


Sensor choices:

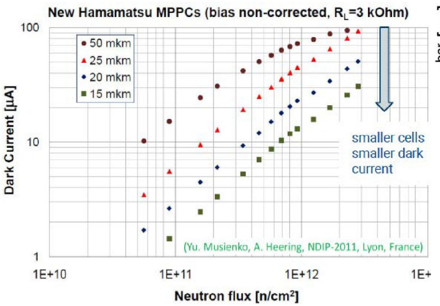
- LYSO crystals as scintillator
  - Radiation tolerance
  - Good light yield
  - Fast rise time
- Silicon Photomultipliers photo-detectors
  - Compact, fast, insensitive to magnetic fields
  - Photo-detection efficiency 20-40%
  - Also rad-hard

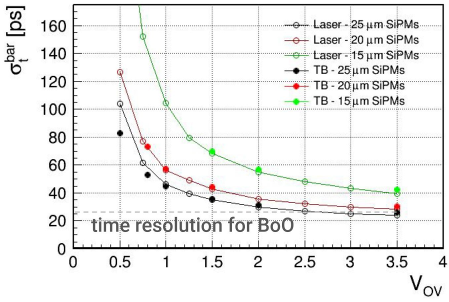
BTL - Sensor optimization

- Sensor geometry: High aspect ratio crystal bar + 2 SiPMs
  - Enhance light collection efficiency
  - Minimize impact point position dependency
  - Minimization of active area and power
  - 2 signals per charged particle, √2 resolution improvement
  - Determination of track position with resolution ~mm



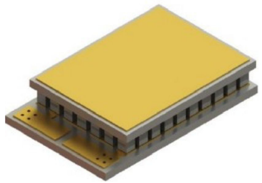
- Trade-off between light collection and Dark Count Rate
  - Optimal SiPM cell size found at 25 μm →higher gain, faster rise time
  - Larger crystal thickness 3.75 mm →bigger energy deposit
  - Both choices increase DCR



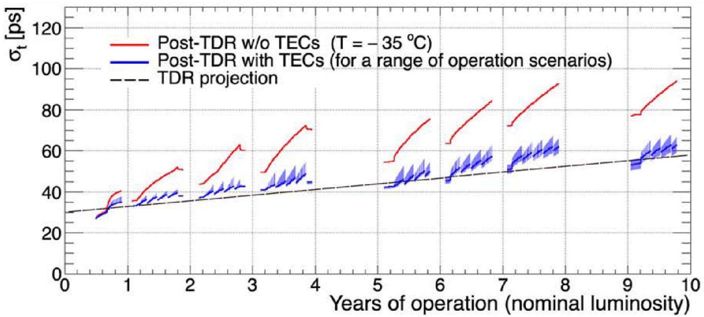


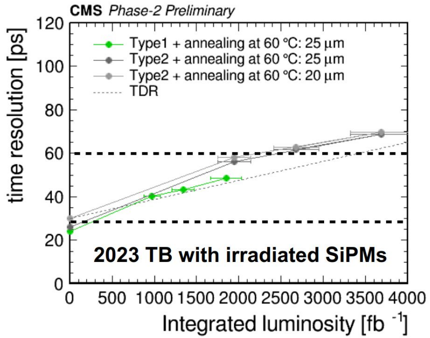
BTL - Sensor optimization

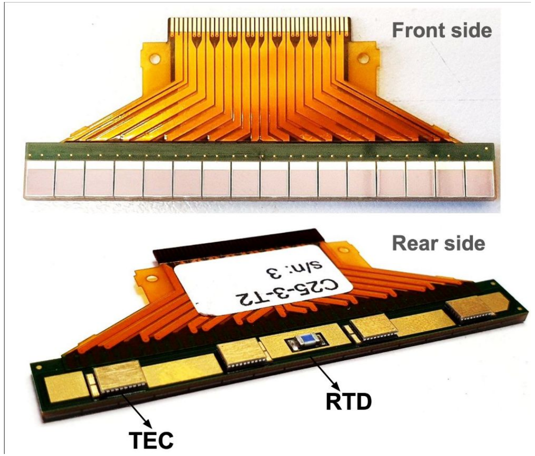
- Minimize SiPM DCR
  - Reduce operation temperature
  - Annealing of SiPMs



➔ Additional Thermoelectric Coolers (TEC) on the SiPMs:
  - Reduce operational temperature from -35 C° (CO_2) to -45 C°
  - Allow annealing in situ during technical stops at 60 C°

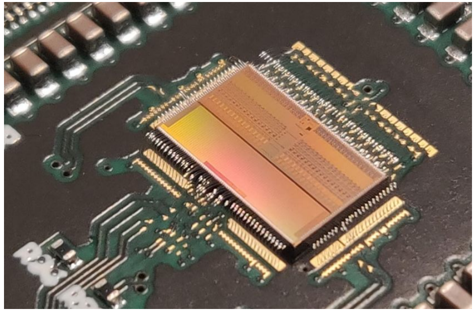


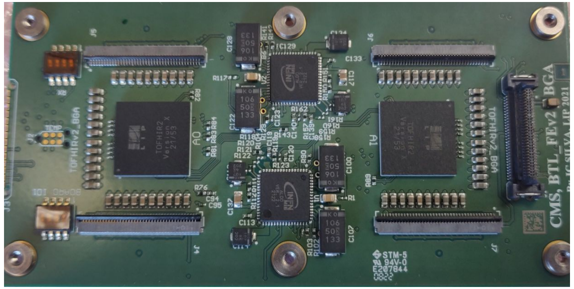


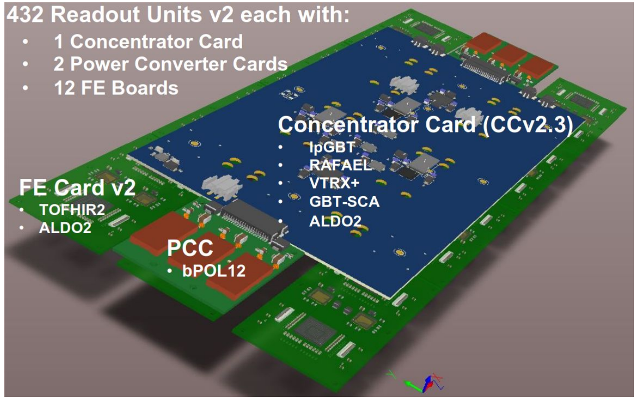


BTL - FE electronics

- Dedicated readout ASIC (TOFHiR2) - derived from TOFPET for PET applications
  - Radiation tolerance
  - Low power dissipation < 1 W/chip
  - DCR suppression - DLED
- FE cards equipped with 2 TOFHiR - 32 SiPM
- CC cards connects 12 FE cards and communicate with backend via VTRx

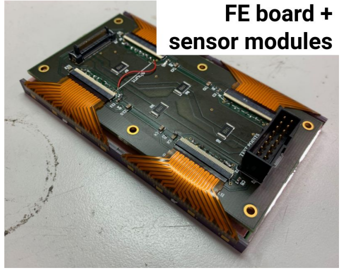


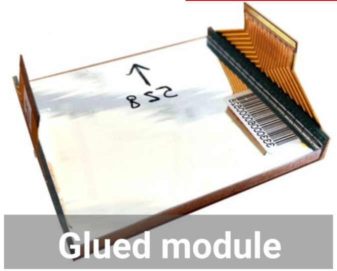




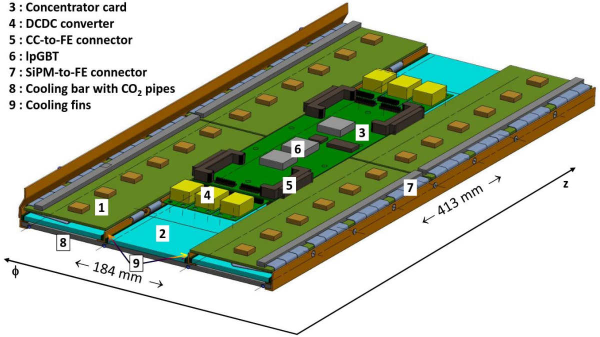
BTL -Detector layout

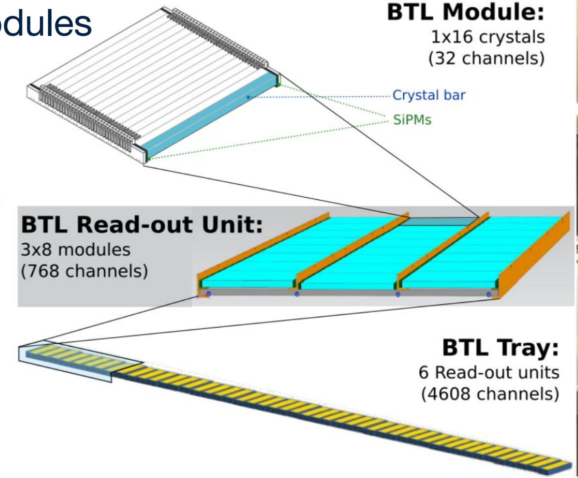
- 16 LYSO bars+ 32 SiPM - 51x57 mm ^{2}
- 2 sensor modules per FE board
- 12 FE per CC - BTL Read-out unit
- 6 BTL RU per tray
- 72 trays (36 in $\phi \times 2$ in η) - 250 x 18 x 2.5 cm
- 331k readout channels, 10368 modules

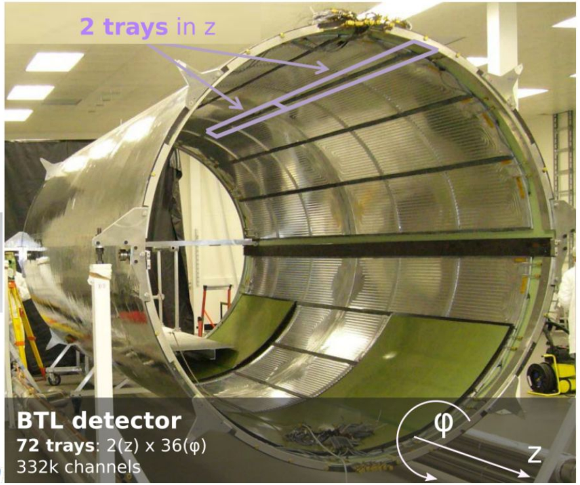




1 : TOFHIR board with 6 ASICs
2 : LYSO array with 16 LYSO bars, bars oriented in ϕ
3 : Concentrator card
4 : DCDC converter
5 : CC-to-FE connector
6 : lpGBT
7 : SiPM-to-FE connector
8 : Cooling bar with CO_2 pipes
9 : Cooling fins







BTL - Status

- Extended effort to meet design performance completed successfully
    - Optimized LYSO thickness and SiPM cell size
    - Optimized SiPM DCR with thermal management
    - Optimized FE to minimize DCR sensitivity till EoL
    - Multiple test beam campaigns, validating the reliability of all the components

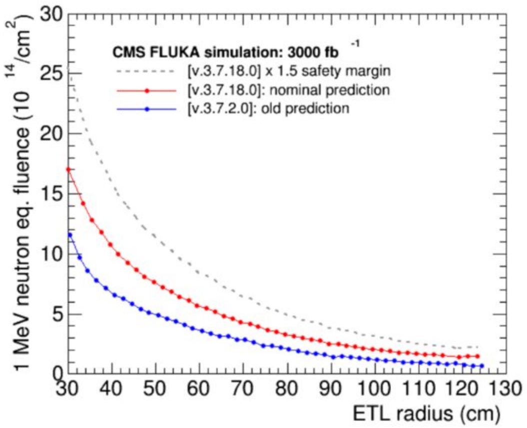
- Prototyping phase finished and moving towards production
    - LYSO pre-production on-going
    - Sensor modules assembly expected to start in Q2 of 2024
    - BTL installation will start in 2025

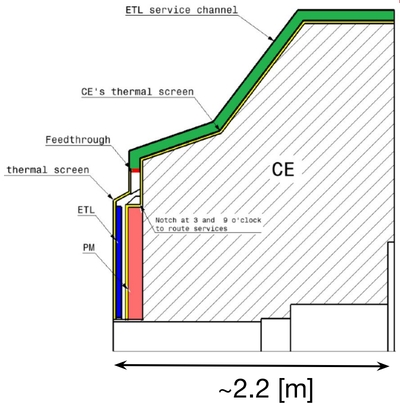
ETL

ETL - design

Challenges:

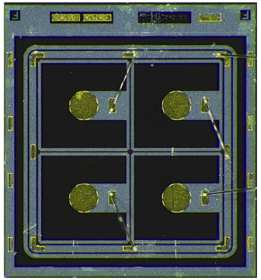
- Withstand the radiation and the particle density of CMS forward regions
- Very tight space
    - z-envelope ~ 45mm





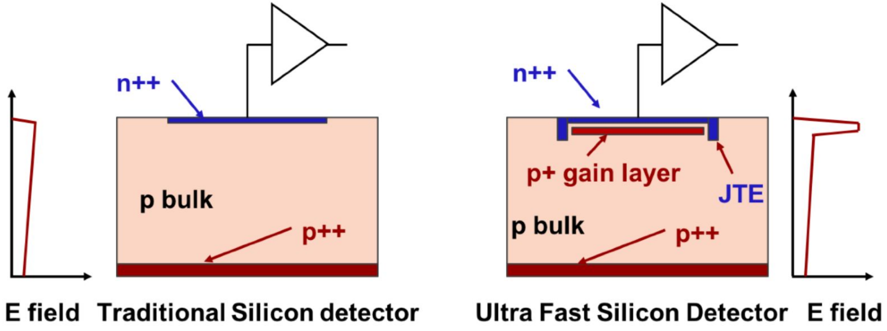
Technology of choice:

- Low Gain Avalanche Diods (LGAD):
    - Radiation hardness
    - Fast rising pulse
    - Relatively thin sensors

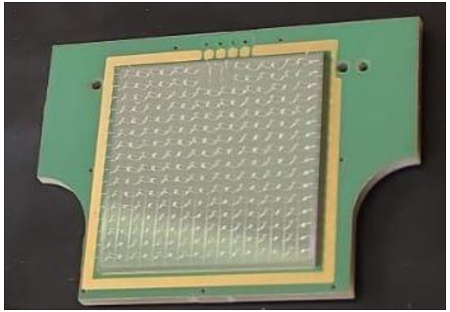


ETL - sensors

- LGADs sensors:
  - Additional gain layer (multiplication implant) proportional to bias voltage
  - Low / moderate gain ~10: low noise, fast slew-rate and fast rising pulse
  - 50µm depletion region → thin sensor
  - Junction Termination Extension (JTE) reduces electric field at perimeter of pads, resulting in no-gain inter-pad gaps. → Need to be sufficiently small for large coverage.



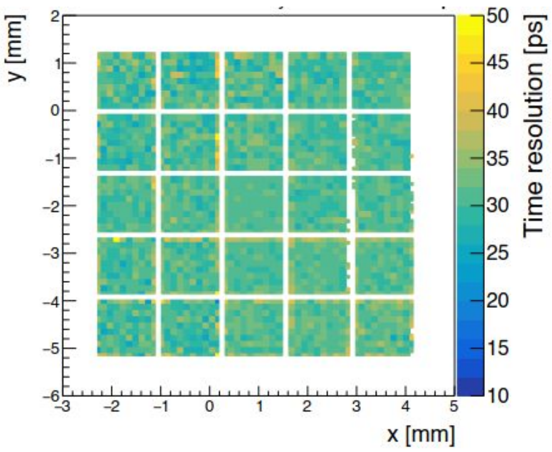
16x16 pixel sensor

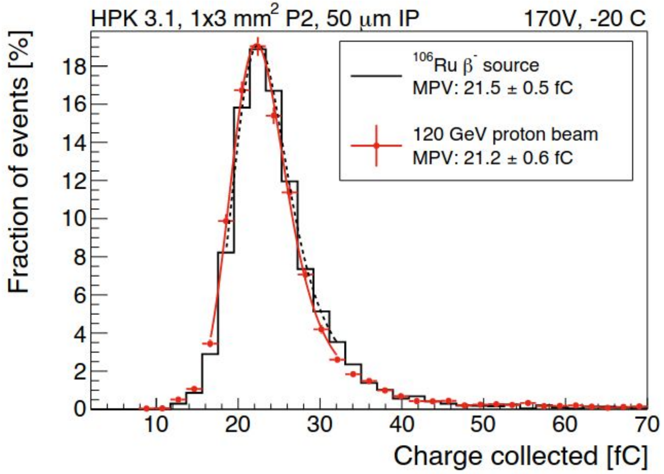


1.3 x 1.3 mm^2 pixels

ETL - sensors

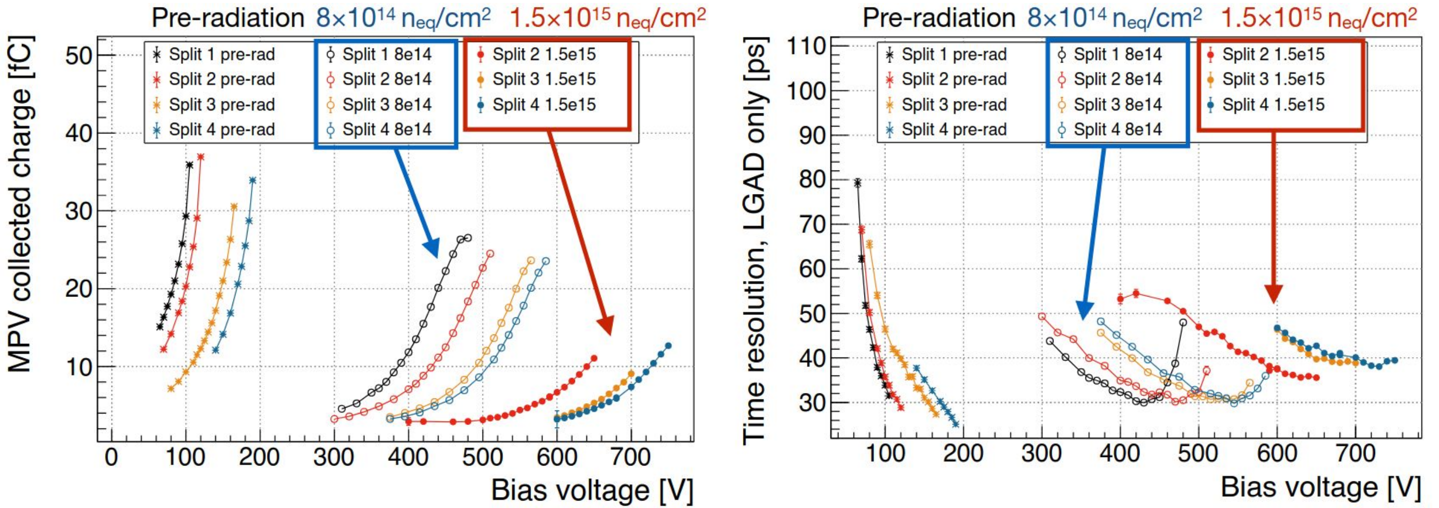
- LGAD sensor performances in ideal conditions (BoL)
- Intrinsic resolution ~30 ps , expected charge deposit 15-35 fC
- Uniform performance across the pads
- Good agreement between test beams and beta source data



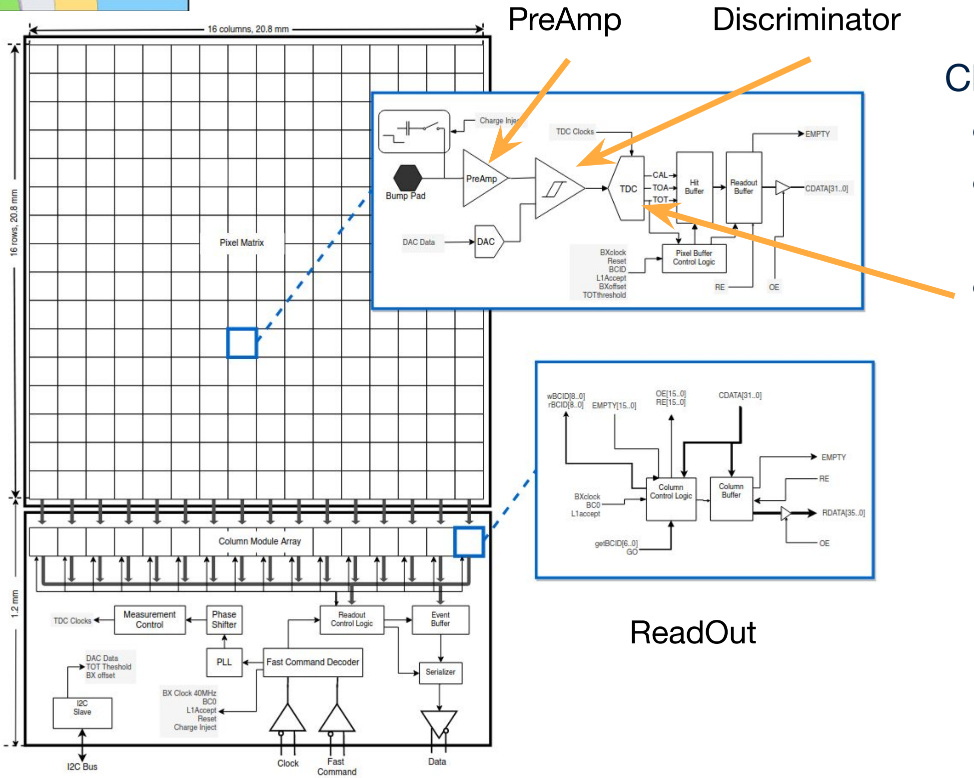


ETL - sensors

- Several test beams performed to measure interpad gap and radiation tolerance:
  - Interpad gap measured to be 70/80 µm - acceptable fill factor
  - To maintain performance, bias voltage need to increase with irradiation
  - Sensors operates safely with bias < 11 V/µm
  - Sensors shows up to 40ps time resolution at 10 fC in EoL conditions

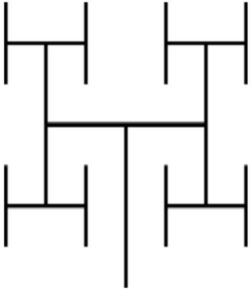


ETL - ETROC



Challenges of the readout electronics:

- Low gain → low deposit charge from sensors
- Sensor resolution ~30 ps → ASIC contribution to time resolution has to be < 40ps
- Low power budget ~ 1W/chip → design dedicated low power TDC

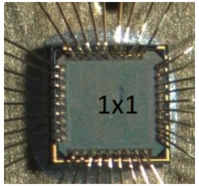


H-Tree clock distribution

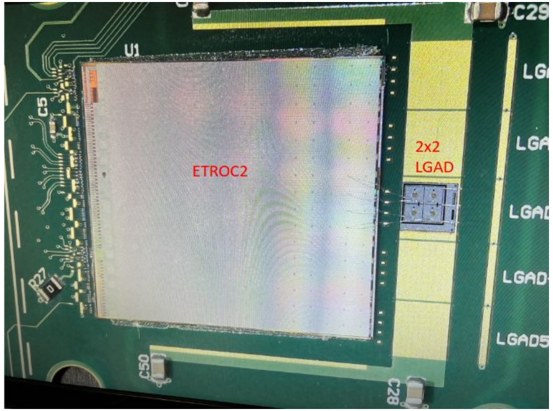
more [here]()

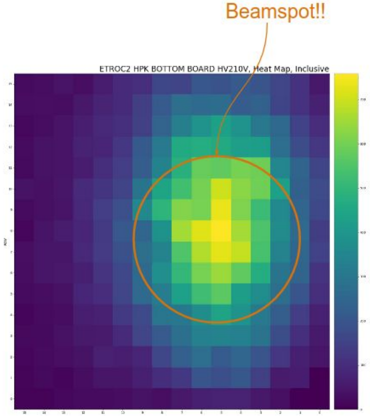
ETL - ETROC

- ETROC prototypes:
  - ETROC0: single analog channel preAmp + discriminator testing core front-end analog performance



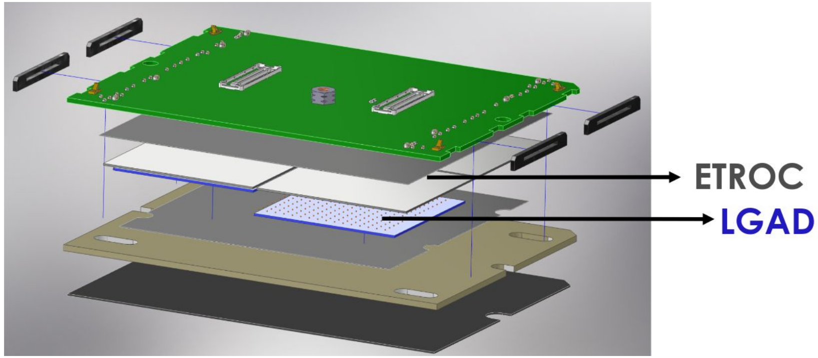
  - ETROC1: 4x4 pixels chip, ETROC0+TDC, test beams with ETROC1 + LGAD sensor showed ~40ps time resolution per single hit
  - ETROC2: - First 16x16 pixels prototype, full functionalities → First ETROC2 + 2x2 LGAD test beams happening now!

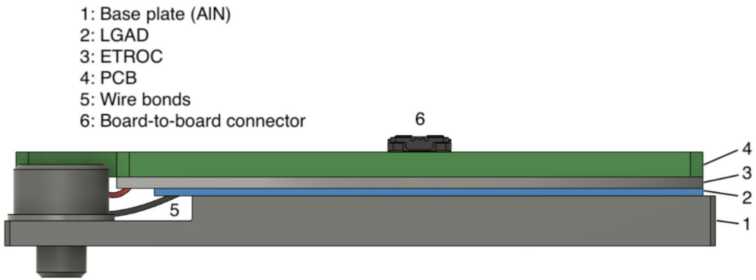




ETL - Modules

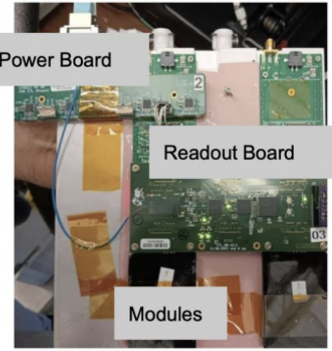
- ETL modules are made of 4 16x16 pixel LGAD sensors, bump bonded to 4 ETROCs
- Sensors are glued on AlN baseplate in thermal contact with the support disk, CO_2 cooled
- Module PCB is glued on the ETROCs
- Modules connects to multi-module readout board that sits on top
- Several sites will assemble the ETL modules - currently testing production throughput

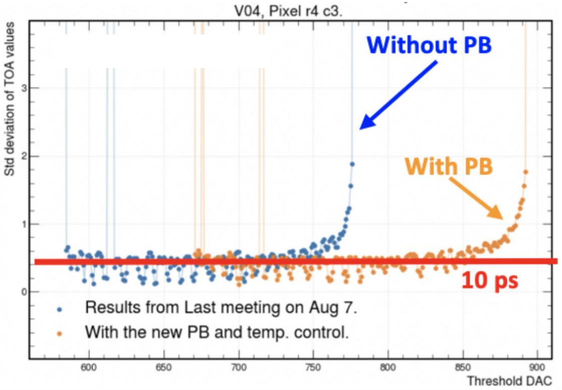


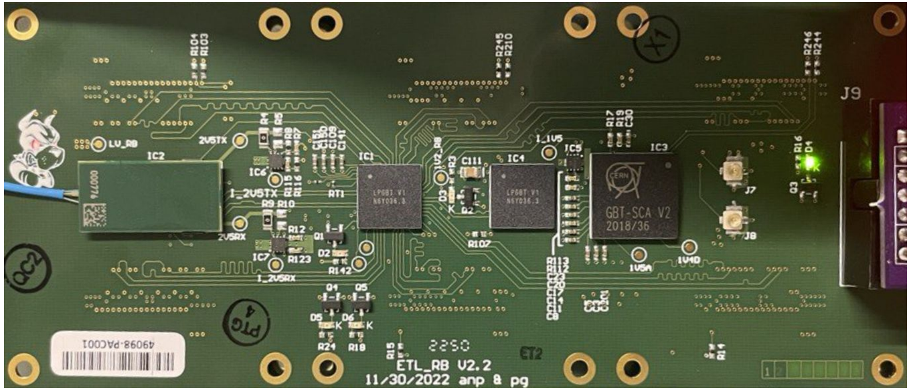


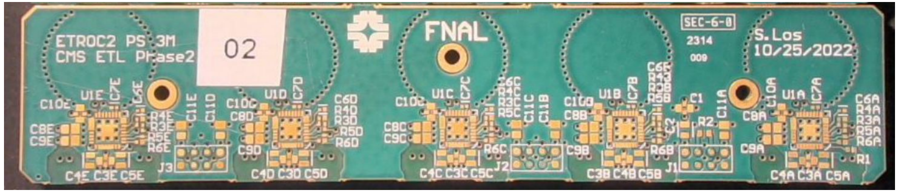
ETL - FE electronics

- Readout board based on CERNs radiation hard GBT chip-set (lpGBT, GBT-SCA) and Optical Link Module, VTRx+
- Custom power board developed at FNAL
- Extensive campaigns of system tests putting together the available prototypes
- Getting ready for TB using ETL full system



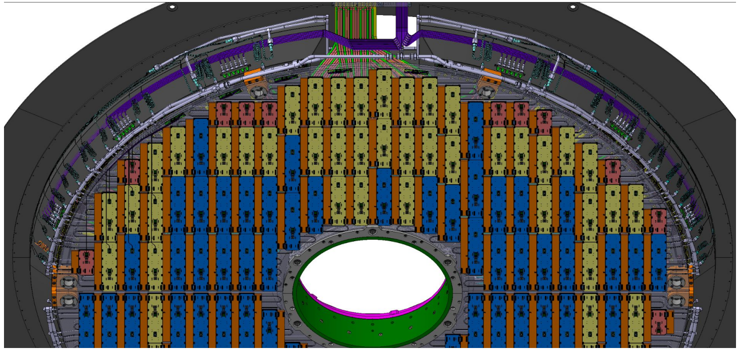


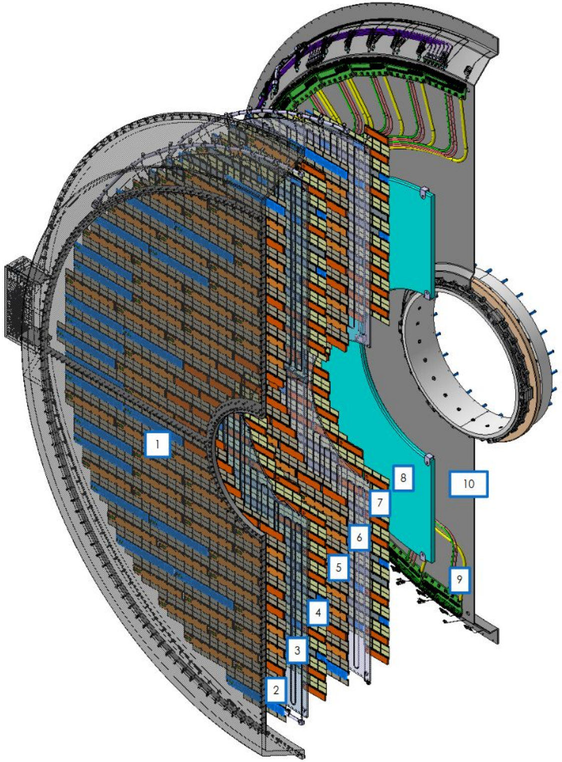




ETL - Detector Layout

- Strong effort to combine inputs from studies into a complete detector design and layout: ~8000 modules (4 sensors each) on 2 EndCaps. ~8M channels in total
- Each detector consists of 2 disks with front and back face instrumented
- Modules + front end electronics and services need to fit in very tight mechanical envelope - total detector z < 99mm





ETL - status

- Final prototype phase, several tests done and still ongoing:
  - LGAD sensor fully characterized, suitable commercial vendors identified
  - ETROC2 ASIC performance studies in full swing, getting ready for ETROC3 submission
  - Full system tests performed on ETROC2 wirebonded with LGADs

- Building the detector:
  - Modules assembly throughput demonstration on-going, at several assembly sites
  - Mechanics design finalized, detector integration planned

Summary and Outlook

- CMS MIP Timing Detector well advanced:
  - BTL:
    - Sensors have been optimized to meet the target performance
    - Reliability and readiness for mass production well demonstrated
    - Entered production phase - modules assembly beginning 2024, tray integration will start end of 2024
  - ETL:
    - LGADs vendors identified, meeting the performance targets
    - Great progress in testing ETROC2, module assembly and system performance
    - Test beams with full system planned for early 2024
    - ETL detector will enter production phase in ~1 year
    - Assembling of the ETL disks will start in 2027

Backup

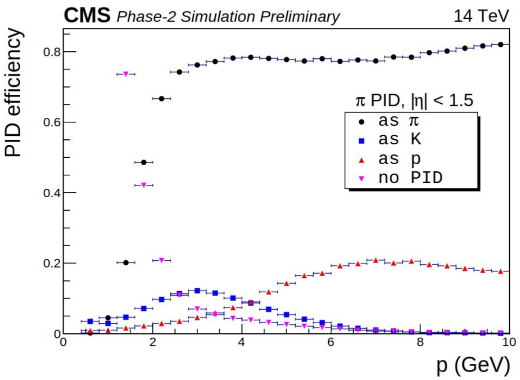
Physics motivation

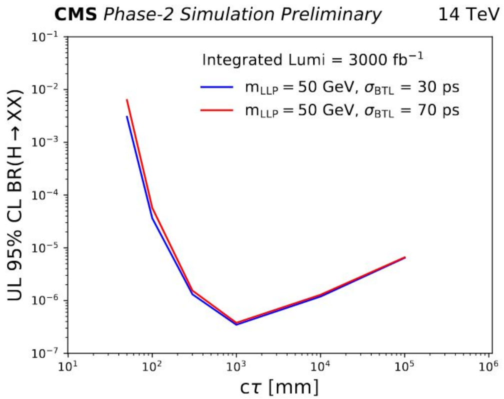
35 ps BTL, 35 ps ETL				
Channel	No MTD	ETL Only	BTL Only	MTD
$bbbb$	0.88	0.90	0.93	0.95
$bb\tau\tau$	1.30	1.38	1.52	1.60
$bb\gamma\gamma$	1.70	1.75	1.85	1.90
Combined	2.31	2.40	2.57	2.66

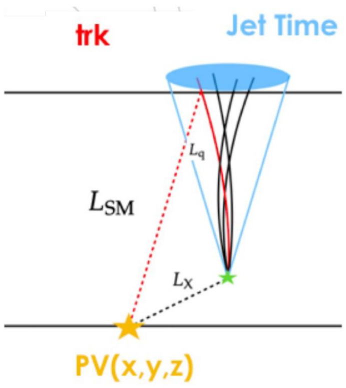
50 ps BTL, 50 ps ETL				
Channel	No MTD	ETL Only	BTL Only	MTD
$bbbb$	0.88	0.90	0.93	0.95
$bb\tau\tau$	1.30	1.36	1.44	1.50
$bb\gamma\gamma$	1.70	1.72	1.78	1.80
Combined	2.31	2.37	2.47	2.53

70 ps BTL, 35 ps ETL				
Channel	No MTD	ETL Only	BTL Only	MTD
$bbbb$	0.88	0.90	0.92	0.94
$bb\tau\tau$	1.30	1.38	1.36	1.44
$bb\gamma\gamma$	1.70	1.75	1.76	1.81
Combined	2.31	2.40	2.41	2.51

- HH measurements
  - improvements in all the HH channels:better lepton isolation, B-tagging, etc…
- Long lived particles
  - displaced jets tagged with jet delay
- improved PID



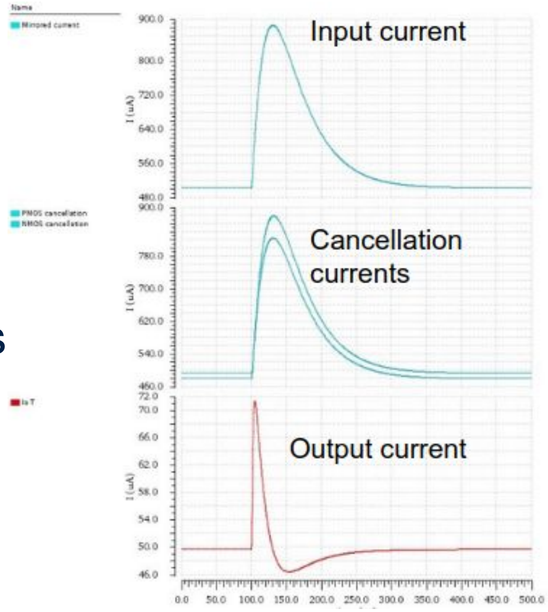




DLED method*

- Inverted and delayed current pulse is added to the original pulse
  - Delay line is approximated by a RC net (200-1800 ps)
  - Short output pulse (< 25 ns)
  - Noise and baseline fluctuations are mitigated

- Simulation of time resolution in EoL conditions shows resolution improvement by a 3.5 factor



*A. Gola, C. Piemonte and A. Tarolli, "Analog Circuit for Timing Measurements With Large Area SiPMs Coupled to LYSO Crystals," in IEEE Transactions on Nuclear Science, vol. 60, no. 2, pp. 1296-1302, April 2013.