

Design and construction of the Inner Tracker for the CMS Phase-2 Upgrade

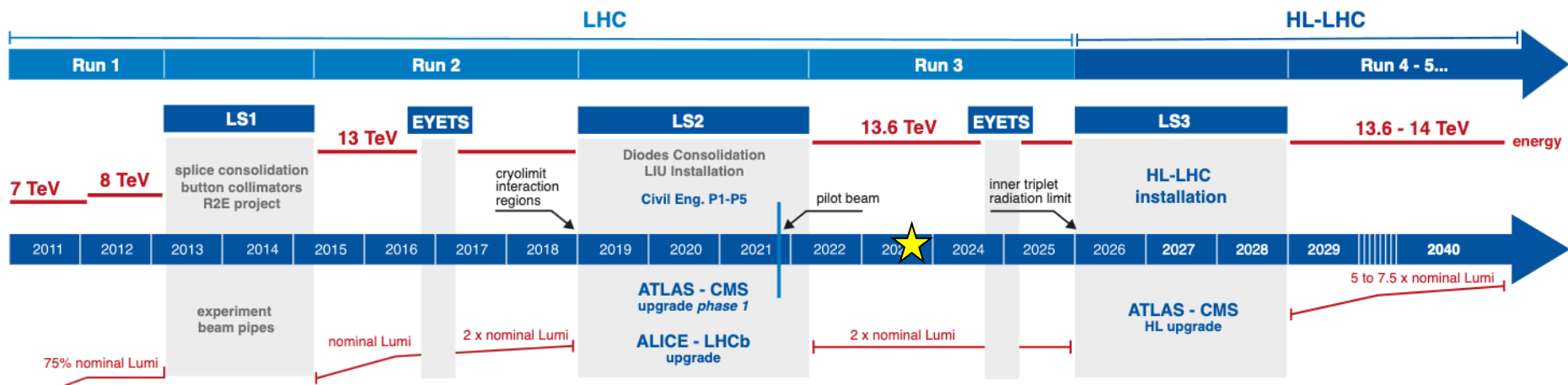
Lea Caminada (PSI | UZH)
on behalf of the CMS collaboration

VERTEX 2023

16-20 October, Sestri Levante, Italy

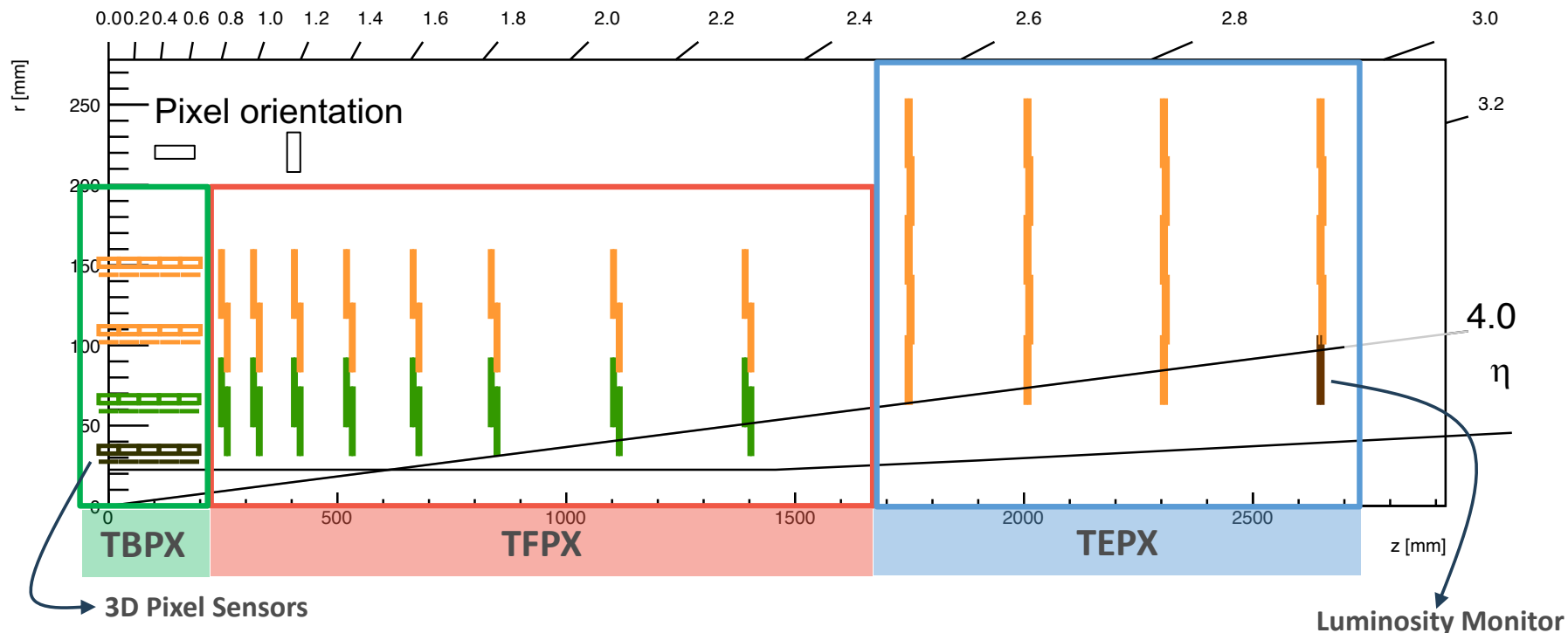
CMS Phase-2 Inner Tracker Upgrade

- HL-LHC will greatly expand the physics potential of CMS, but also bring severe experimental challenges
 - 3-4 x more pileup (up to 200 pp collisions per bunch crossing)
 - Hit rate up to 3.2 GHz/cm² in innermost layer
 - 3 x longer trigger latency (12.5 μs)
 - 10 x more radiation (TID up to 1.2 Grad, fluence of $2.3 \times 10^{16} n_{eq}/cm^2$)
- To maintain or even improve the tracking and vertexing performance with these conditions a new Inner Tracker (IT) will be built featuring
 - Increased granularity and resolution
 - Increased rate and radiation tolerance
 - Reduced material in the tracking volume
 - Increased acceptance in the forward region from $|\eta| < 3$ to 4



https://hilumihc.web.cern.ch/sites/default/files/HL-LHC_Janvier2022.pdf

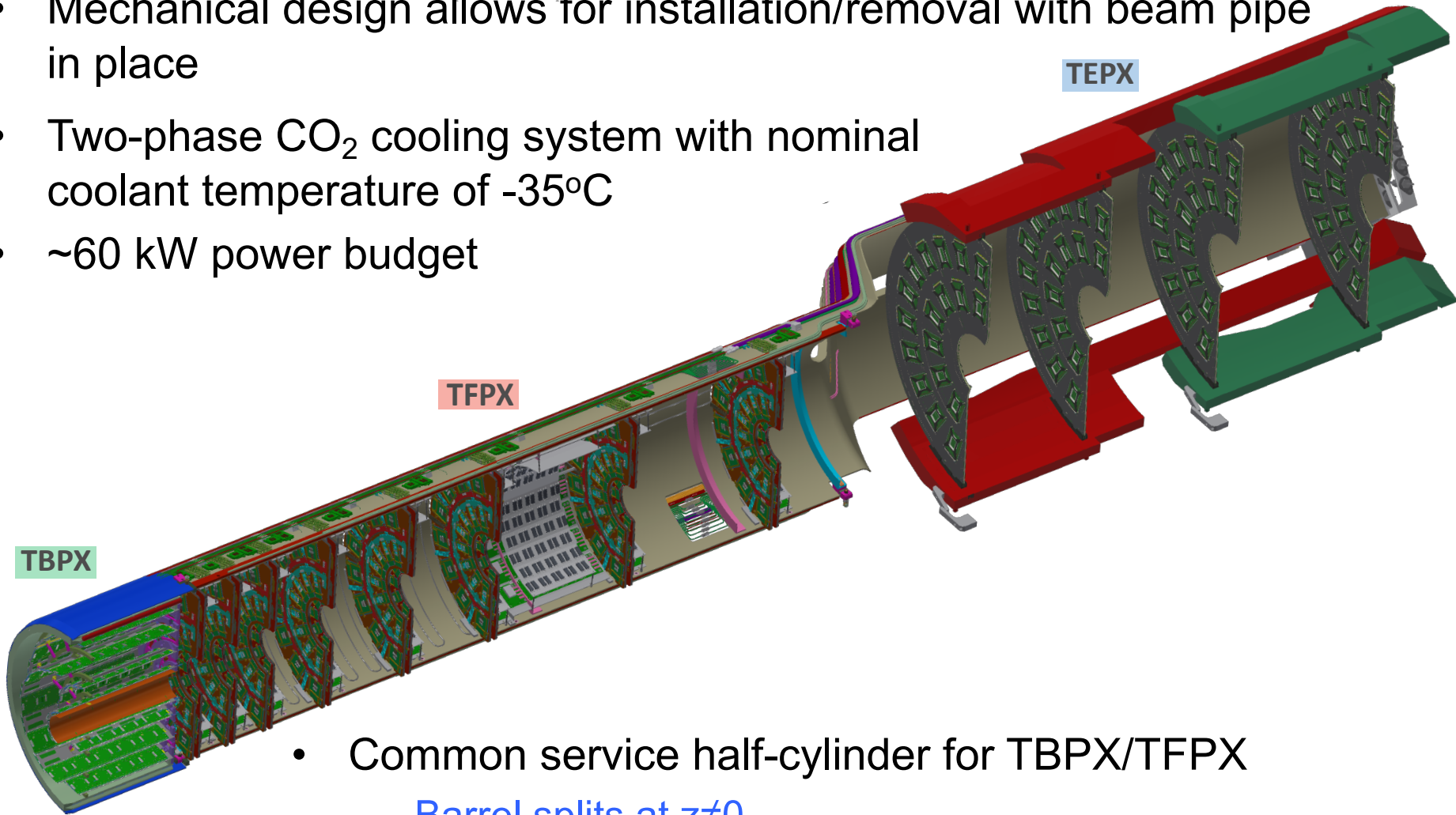
Inner Tracker Layout



- IT built from 3892 modules with either **1x2** or **2x2** readout chips (ROCs)
 - 2 billion pixels with size of $25 \times 100 \mu\text{m}^2$
 - 3D Si sensors in innermost layer (L1), planar Si sensors elsewhere
- Three subsystems:
 - **Tracker Barrel PiXeL (TBPX)**, 4 layers
 - **Tracker Forward PiXeL (TFPX)**, 8 small double-disks on each side
 - **Tracker Extended PiXeL (TEPX)**, 4 large double-disks on each side

Inner Tracker System

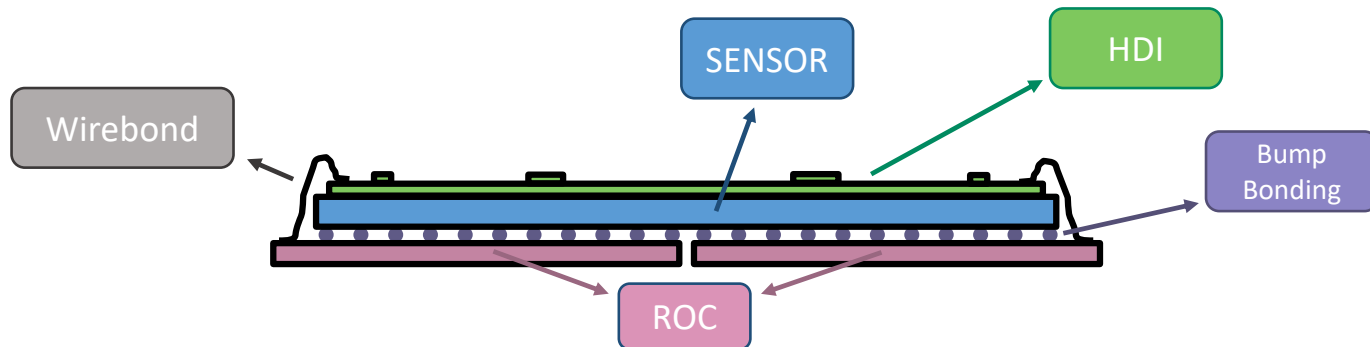
- Mechanical design allows for installation/removal with beam pipe in place
- Two-phase CO₂ cooling system with nominal coolant temperature of -35°C
- ~60 kW power budget



- Common service half-cylinder for TBPX/TFPX
 - Barrel splits at $z \neq 0$
- TEPX split in two mechanical units to enable installation

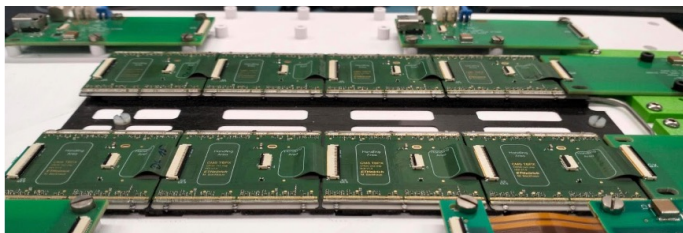
Inner Tracker Modules

- Simple design with ROC as only active electronics on the module
- Serial powering scheme with up to 11 modules per chain
- High Density Interconnect (HDI):
 - Flexible PCB containing only passive components
 - Contains return path for supply current
 - Careful design for low material budget
 - HV capable up to 1000V
- Different module flavors depending on module location (due to different layout of serial powering and mounting scheme)

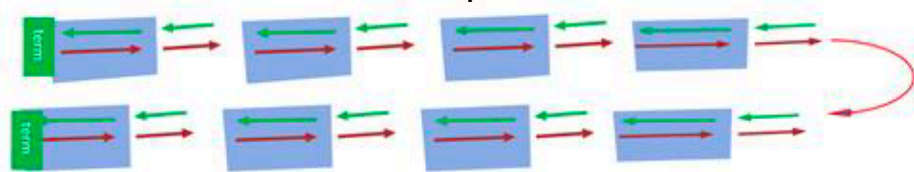


Inner Tracker Modules

Ladders in TBPX

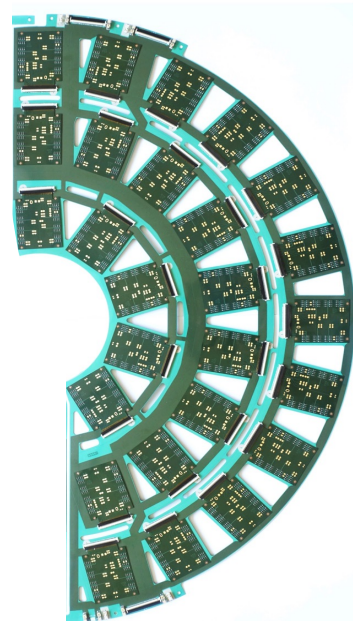
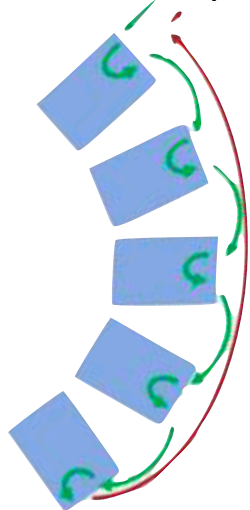


SP current path

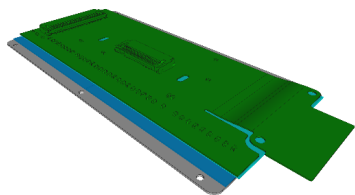


Half-disks in TFPX/TEPX

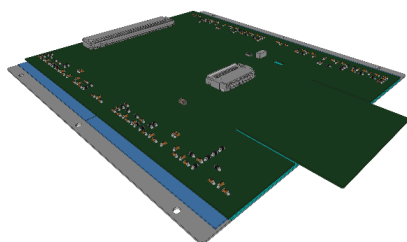
SP current path



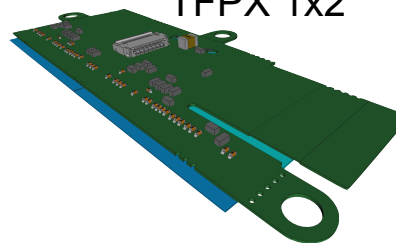
TBPX 1x2



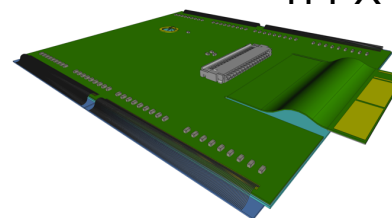
TBPX 2x2



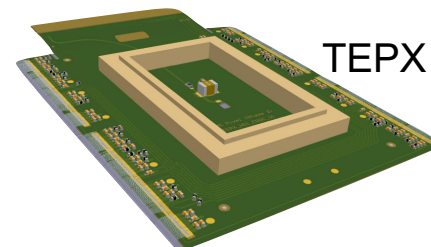
TFPX 1x2



TFPX 2x2

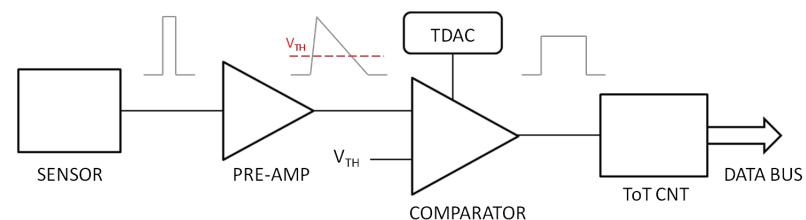
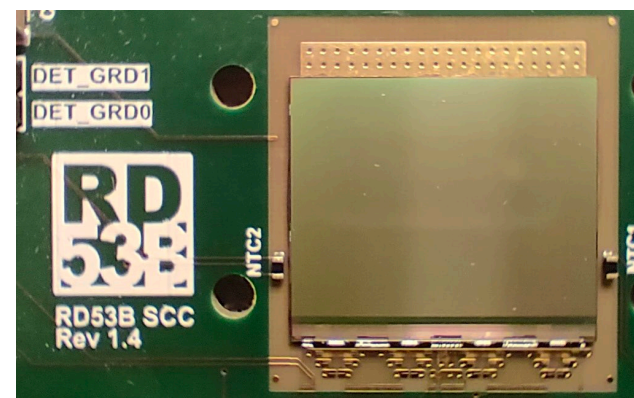
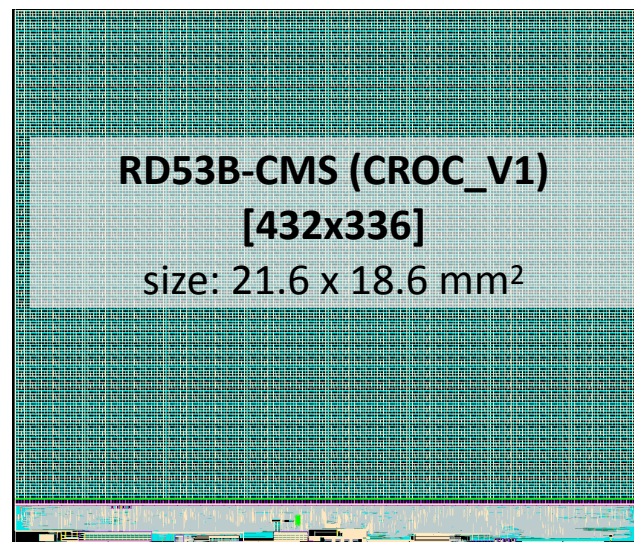


TEPX 2x2

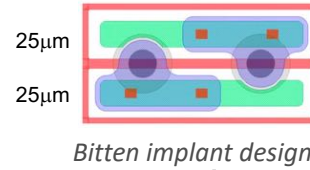


CMS Readout Chip (CROC)

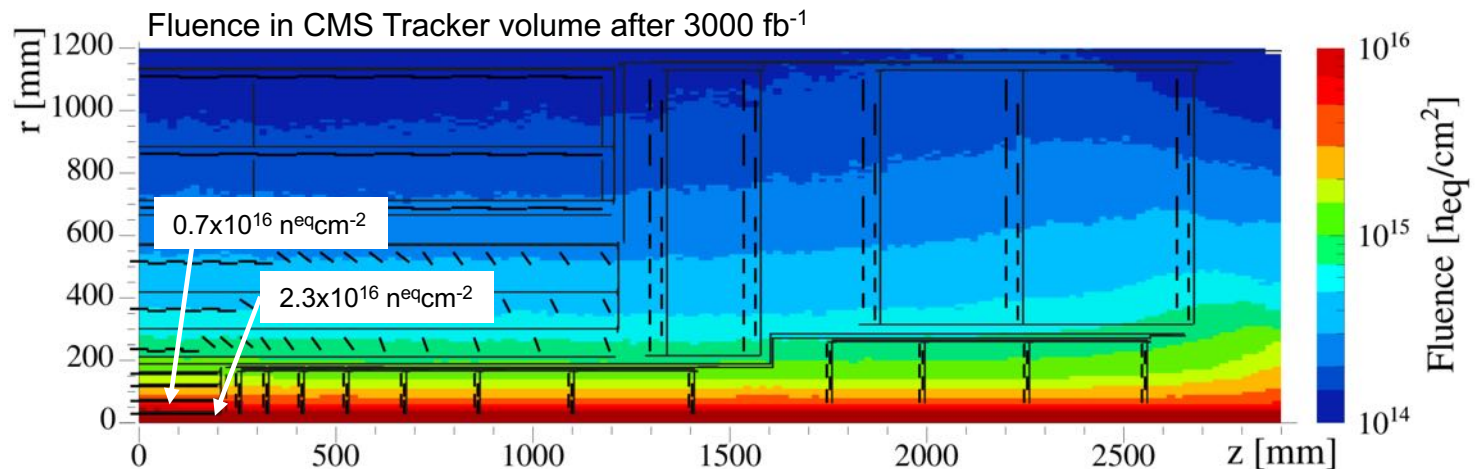
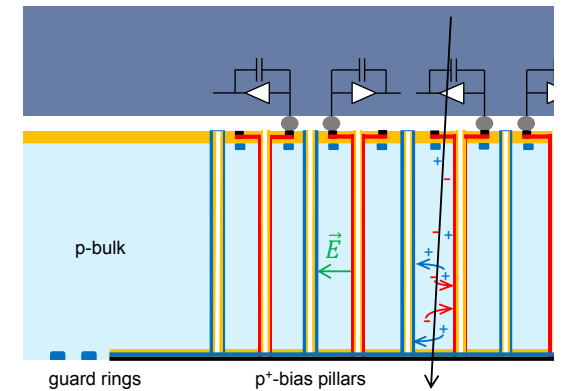
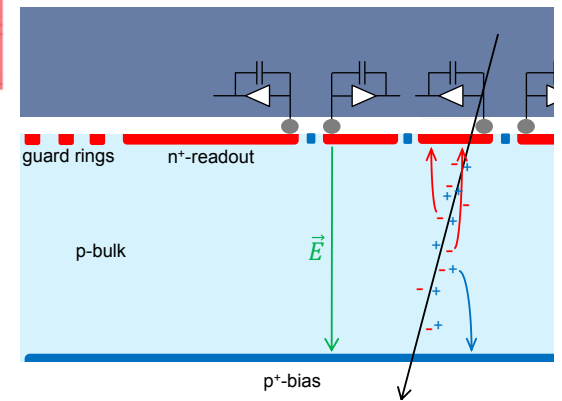
- CROC 65nm CMOS ASIC developed by joint ATLAS-CMS RD53 collaboration
- Full size prototype thoroughly tested and validated, final version submitted
- $50 \times 50 \mu\text{m}^2$ cell size
- 3.5 GHz/cm^2 hit rate
- Radiation tolerance up to 1 Grad
- Linear analog front-end design
 - Low, adjustable threshold $< 1000 e^-$
 - Adjustable feedback to cope with large sensor leakage currents
- 4-bit digital readout with time-over-threshold (ToT) counter
- Up to $4 \times 1.28 \text{ Gbps}$ output links (configurable)



Sensors

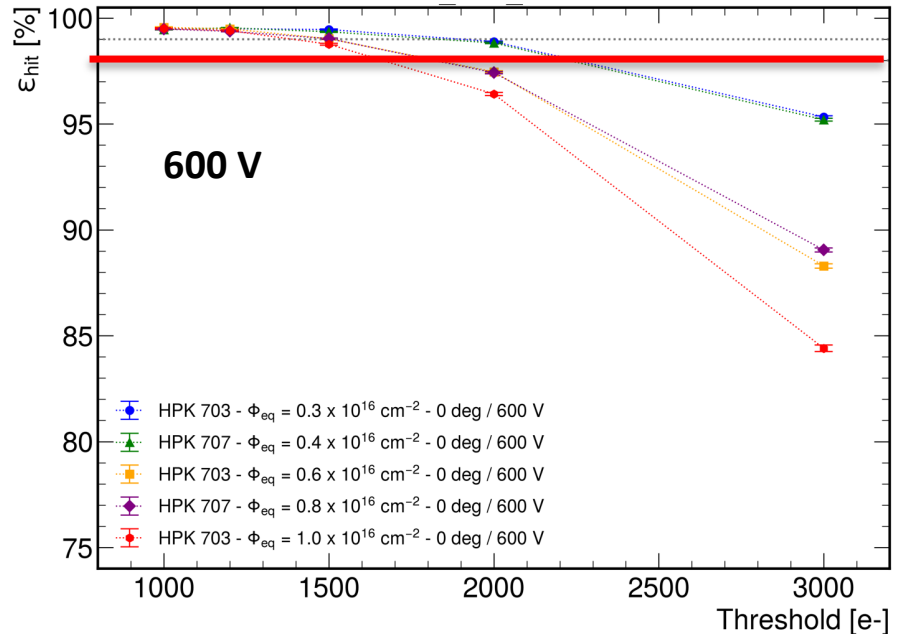
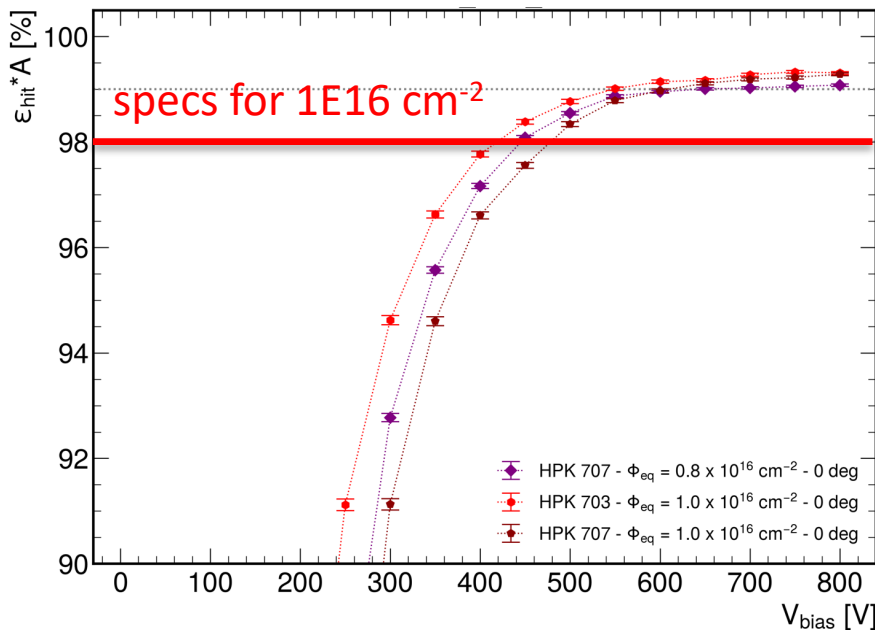


- Planar Si sensors (150 µm thickness, n-in-p)
 - Less production steps due to single-sided processing, but Parylene coating needed for edge isolation
 - 11 ke⁻ of charge for MIP
 - Higher radiation tolerance due to reduced thickness (and reduced bias voltage)
- 3D Si sensors in L1
 - Lower leakage current, necessary for safe margin to thermal runaway after irradiation ($\phi=1.5 \times 10^{16} \text{ n}_{\text{eq}} \text{ cm}^{-2}$)
 - Replacement of TBPX L1 and TFPX R1 foreseen



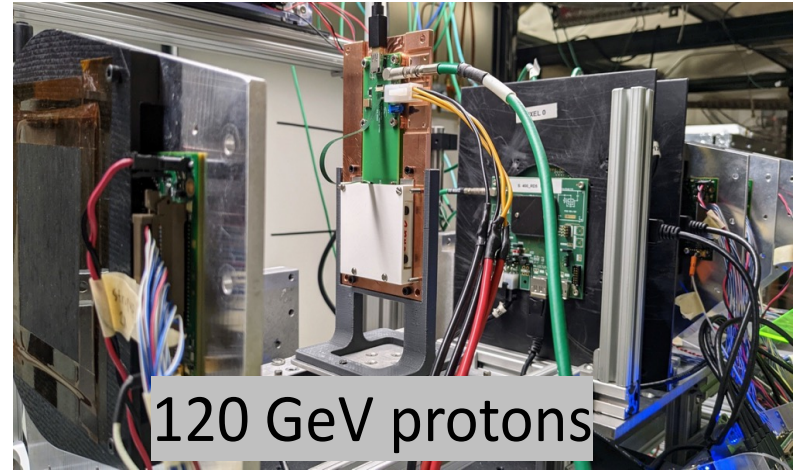
Hit efficiency

- Single-chip assemblies with planar sensors irradiated up to $\phi=1 \times 10^{16} \text{ n}_{\text{eq}} \text{ cm}^{-2}$ at CERN PS (23 GeV protons)
- Performance in terms of hit efficiency, noise and resolution measured in test beam at DESY
- Excellent performance with hit efficiency $> 98\%$ and $< 1\%$ noisy pixels
- Resolution better than binary resolution even at highest fluence

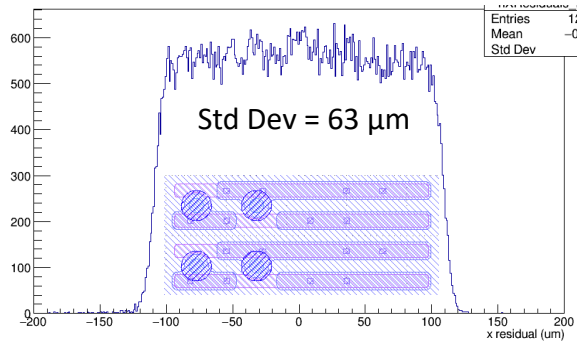


Validation of full module

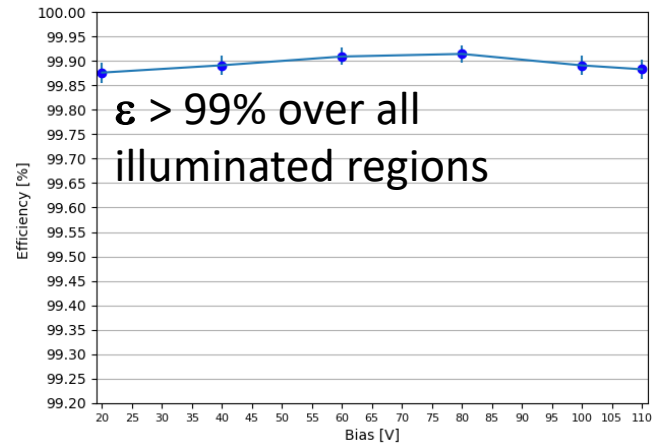
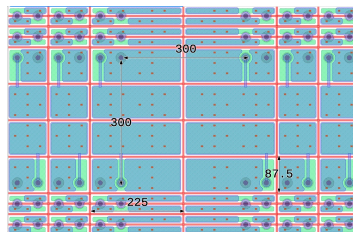
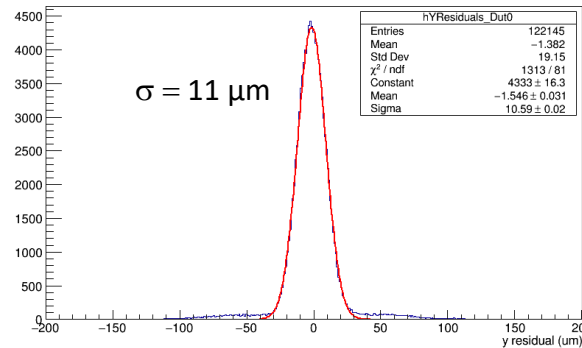
- TBPX 2x2 module in FNAL testbeam
- Excellent performance confirmed
- Studied larger cells in inter-CROC regions (columns of $225 \times 25 \mu\text{m}^2$) \rightarrow residuals as expected
- Analysis of data of irradiated modules underway



x residuals (225 μm side)

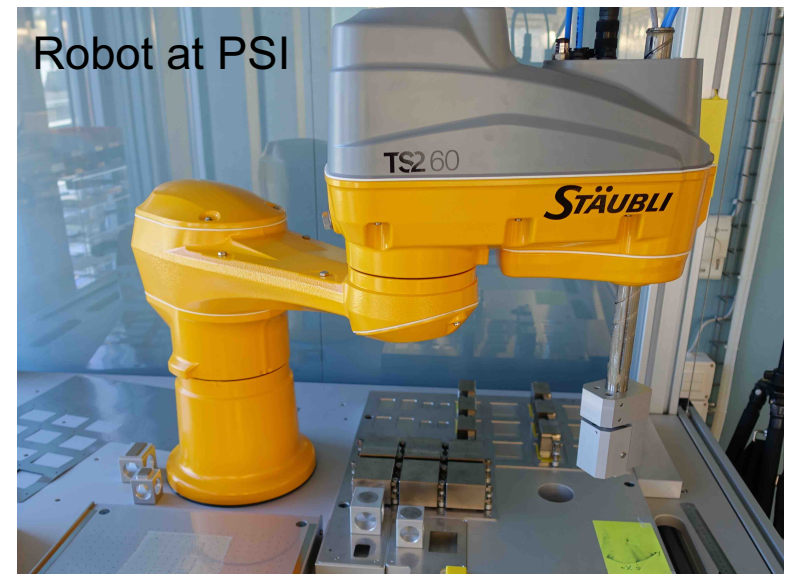
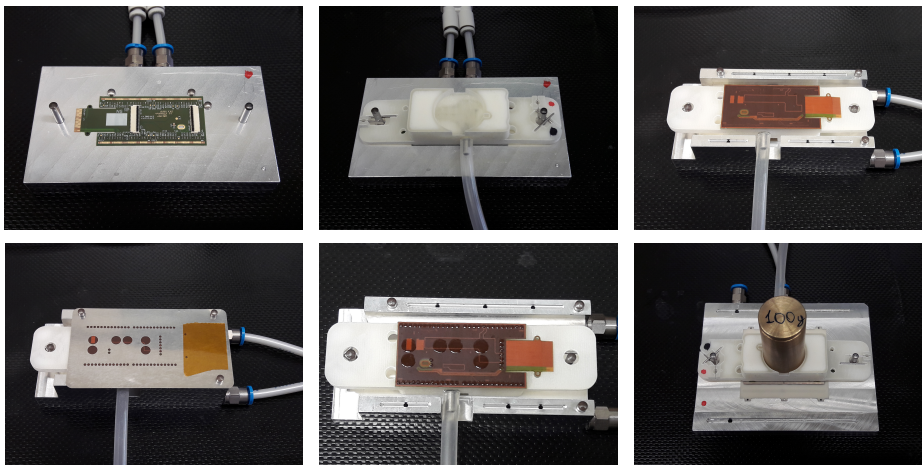


y residuals (25 μm side)



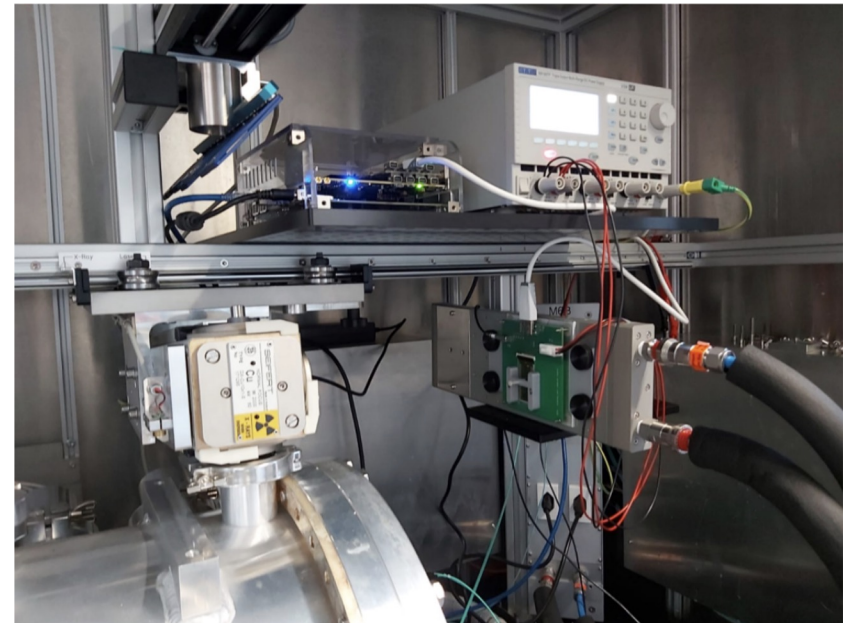
Module Production

- Module production and testing done in 12 different centers in Europe (TBPX/TEPX) and USA (TFPX)
 - 3 vendors qualified for hybridization
- 6000 modules to be built (3892 to be installed)
 - Expect maximum throughput of 300 modules per month
 - Production will start in summer 2024
- Prototype modules built in different centers, demonstrated assembly accuracy in the range of 10-20 μ m
- Assembly by jigs (TBPX) or more automated procedures using gantry (TFPX) or robotic arm (TEPX)



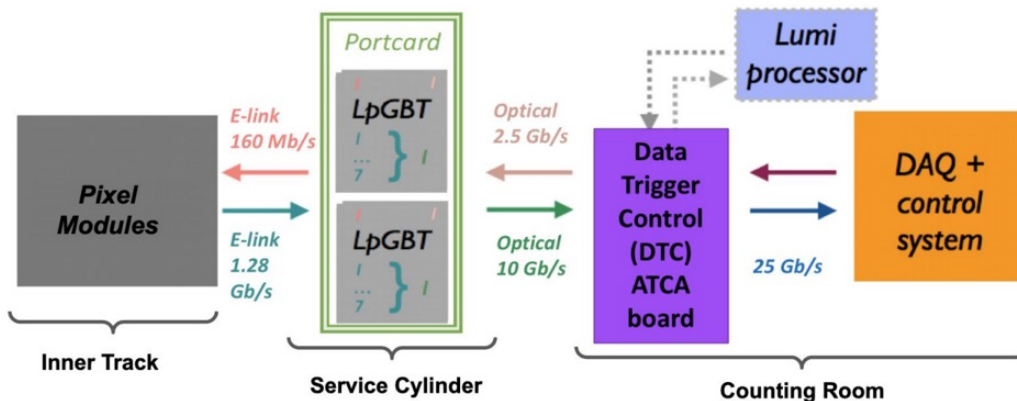
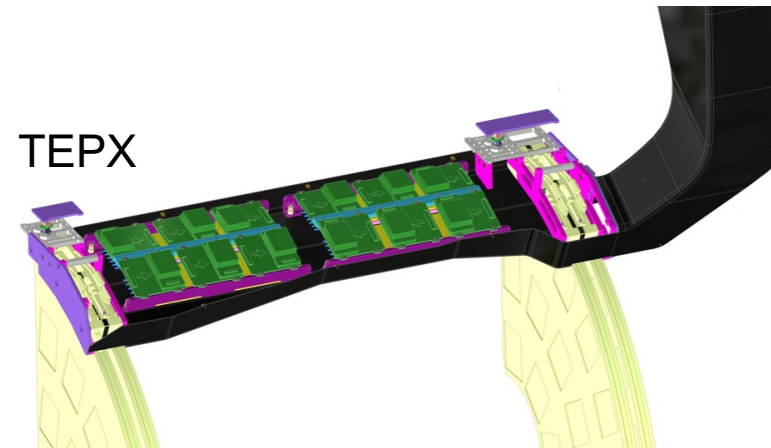
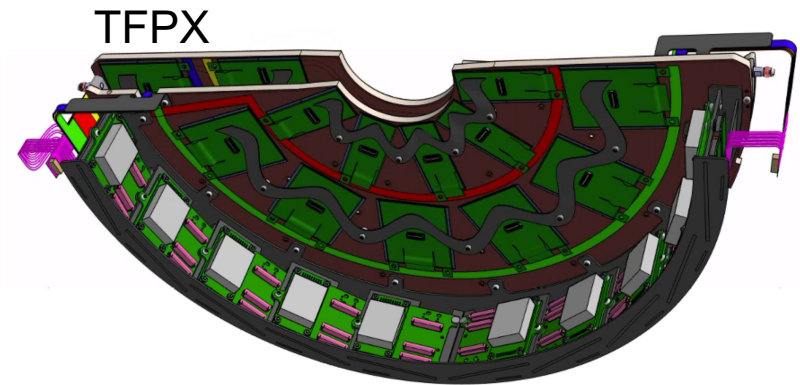
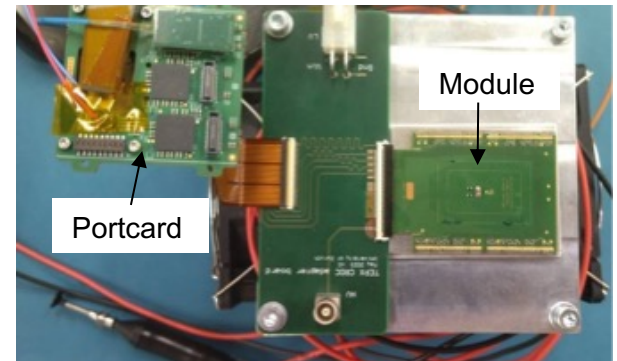
Module Testing

- Quick module functionality test after assembly, including optical inspection
- Full module qualification after coating
 - IV curves
 - ROC and pixel functionality
 - Bump-bonding
 - Thermal cycling
 - High-rate x-ray tests and x-ray calibration for subset of modules
- Coldbox to test up to 8 modules at a time



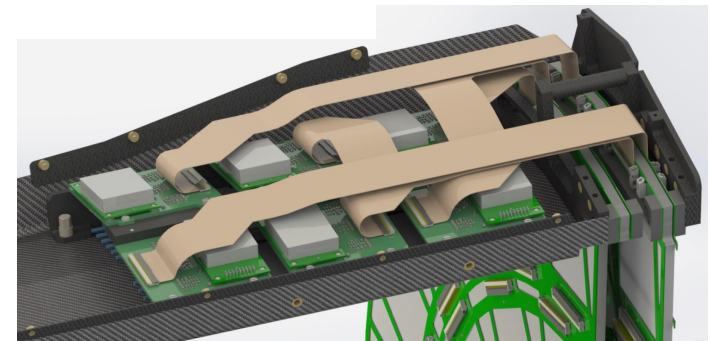
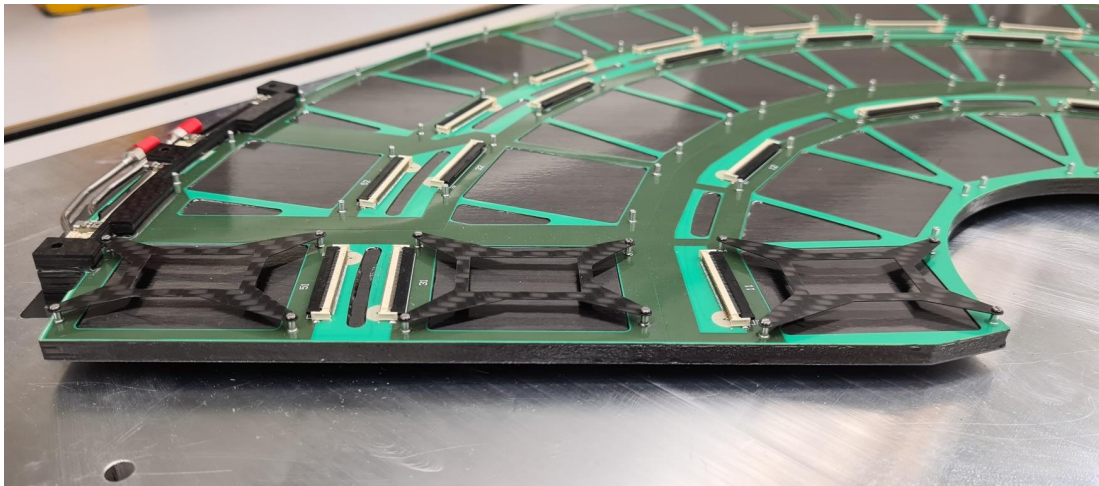
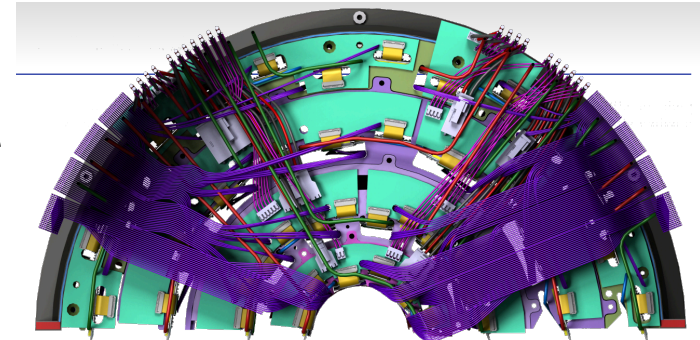
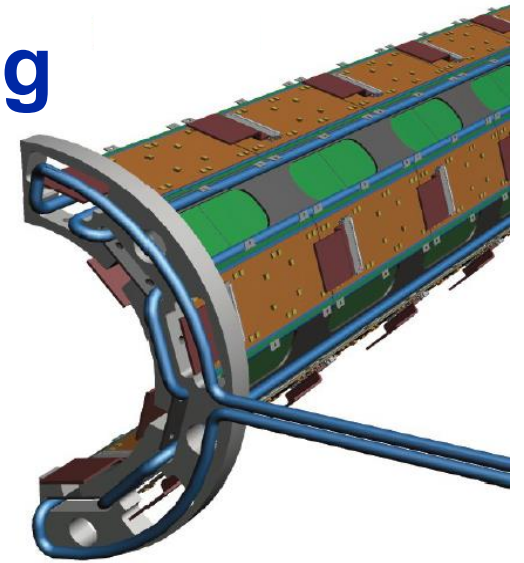
Readout system

- Up to 6 electrical up-links at 1.28 Gbps per module to IpGBT
- One electrical down-link at 160 Mbps per module for clock, trigger and commands
- Auxiliary electronics and opto-converters hosted on 680 portcards located on cartridges (TBPX/TFPX) or supplies (TEPX)
- DAQ made from 28 Data Trigger Control (DTC) boards

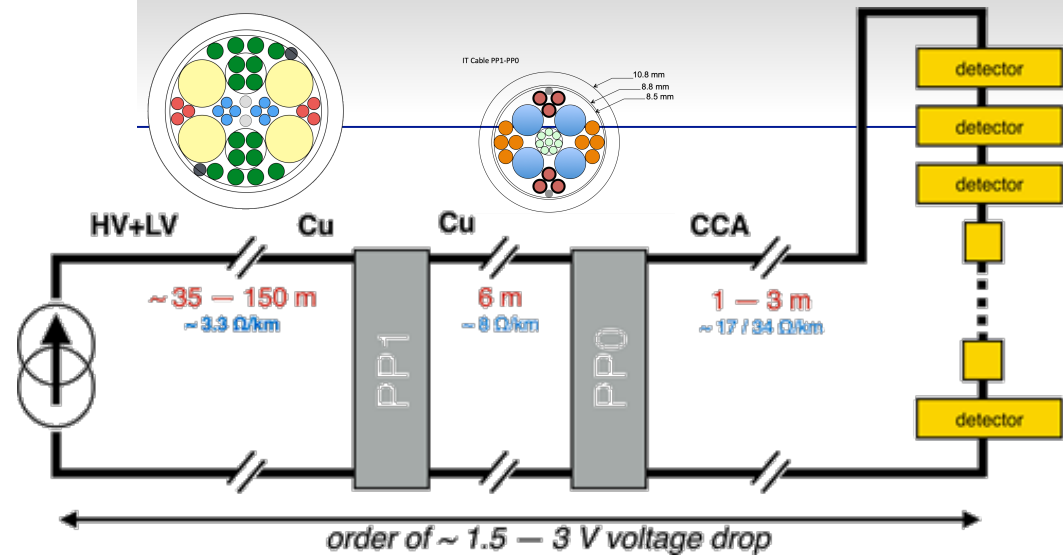
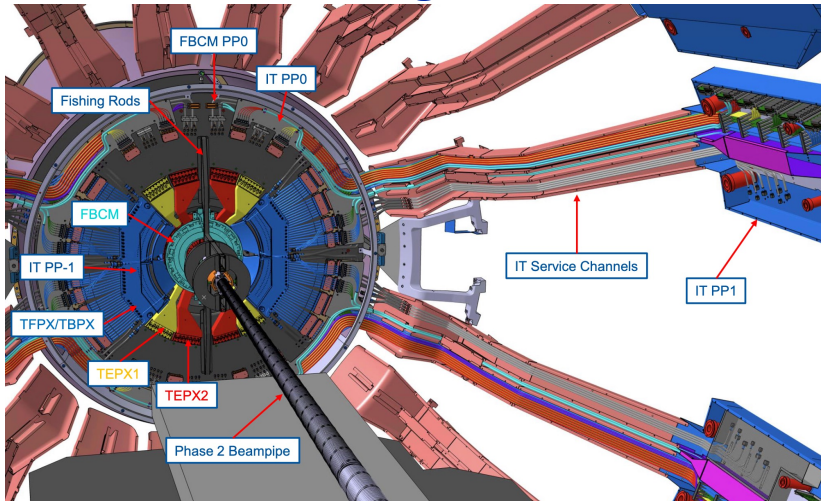


Mechanical support and cabling

- Light Carbon Fiber structures with embedded thin-walled Titanium cooling pipes
- TBPX made from ladders of 4 or 5 modules, complex elink routing at enflange to portcards
- Disks with flat geometry, elinks routed through disk PCB, flex cables connect to portcards



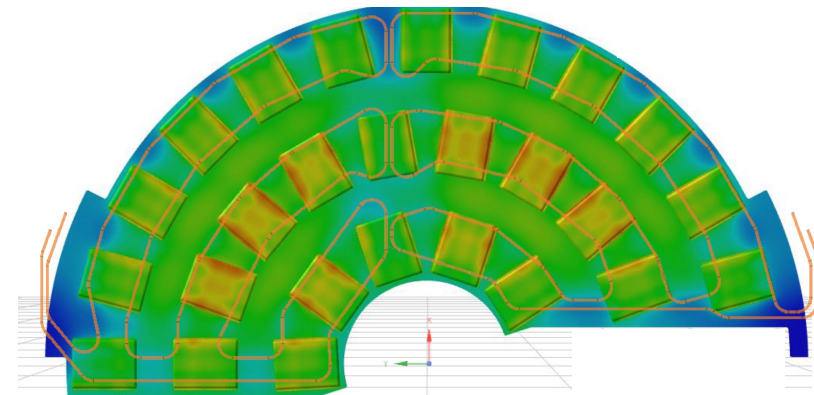
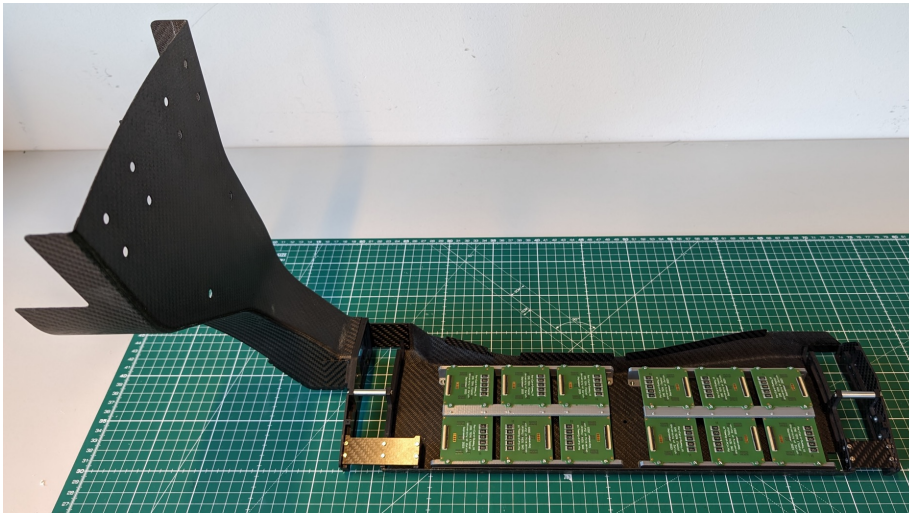
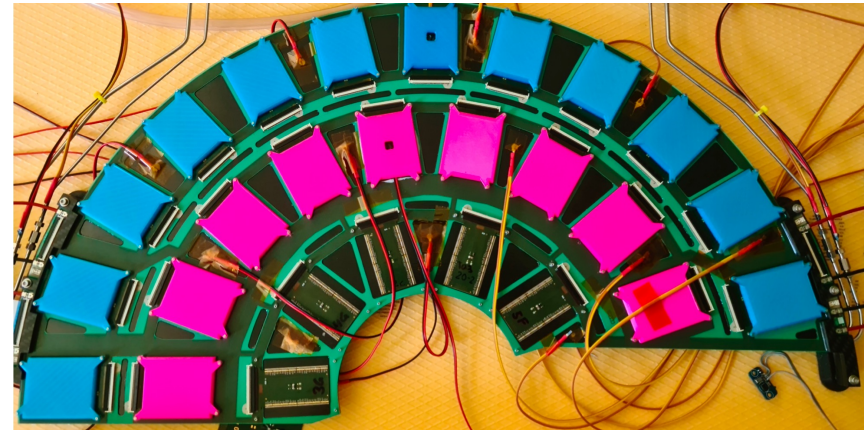
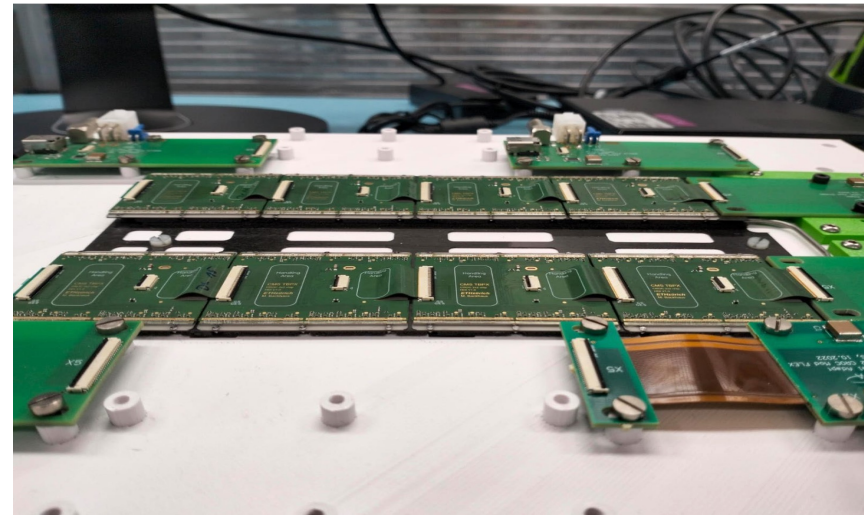
Power system



- Serial powering used to supply ~60kW
- 500 SP chains (164@4A, 336@8A) with 5-11 modules per chain
- ROCs within modules powered in parallel
- HV distributed in parallel to modules
- DCDC converters on portcards for optoelectronics and IpGBT
- Preheaters for each cooling loop
- Power supply within experimental cavern

System test

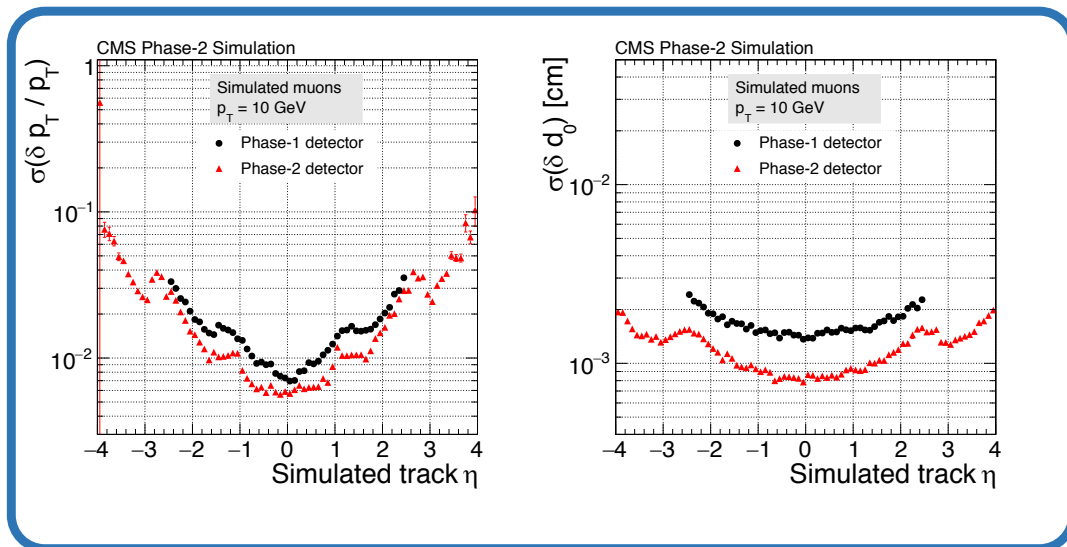
- System tests of all IT subsystems ongoing to gain experience in operation
- Qualify electrical and optical links
- Investigate performance of SP chains and thermal behavior
- Establish testing and calibration procedures for detector integration



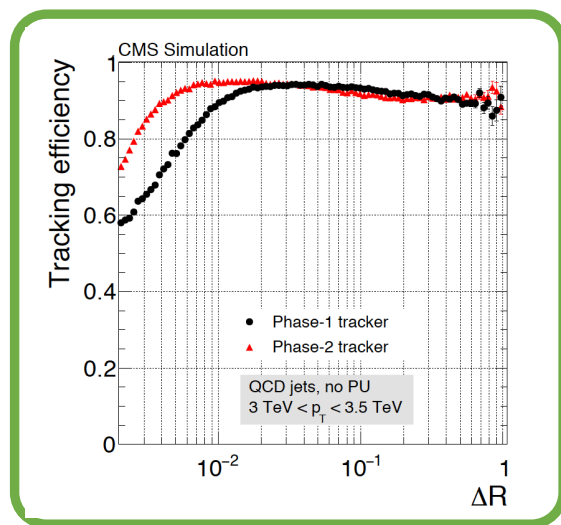
Expected performance

- Improvements on all physics observables even at highest pileup thanks to increased granularity with smaller pixels

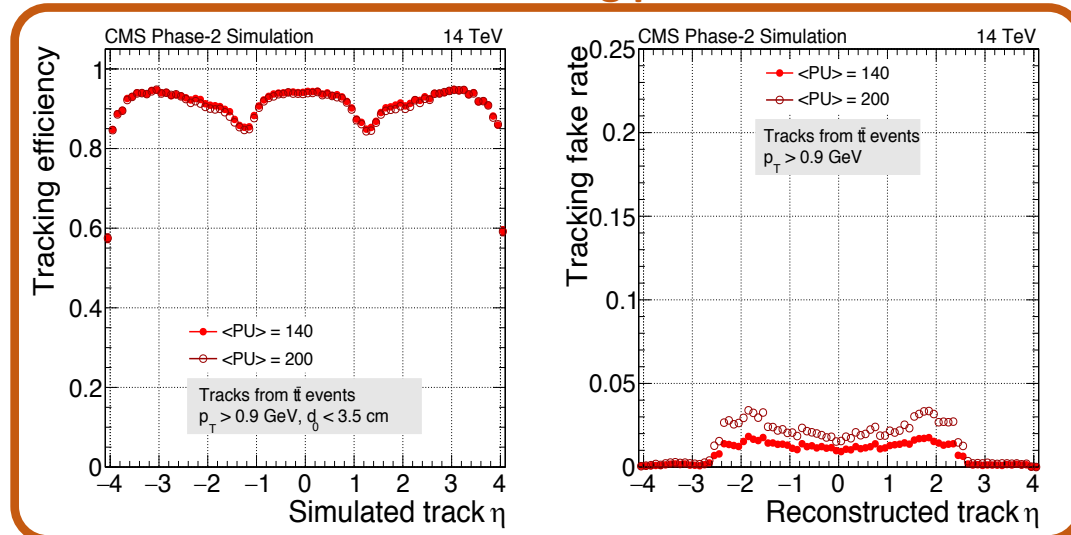
Improved resolution



Improved efficiency in high p_T jets



Robust track finding performance



Summary

- Phase-1 CMS pixel detector will be replaced by Phase-2 Inner Tracker system for operation at HL-LHC
- Highlight in the design of the Phase-2 IT is increased granularity and extended acceptance in the forward region from $|\eta| < 3$ to 4
- Performance of all module components has been validated, CROC and sensors in fabrication, module production will start in summer 2024
- Prototypes of all components (serial powering, readout electronics, modules) available and being tested in system tests
- CMS Phase-2 is a challenging project with lots of activities in detector construction ahead of us



THANK YOU