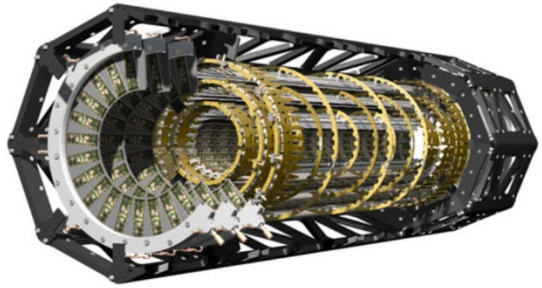


Operational Experience and Performance with the ATLAS Pixel Detector at the Large Hadron Collider

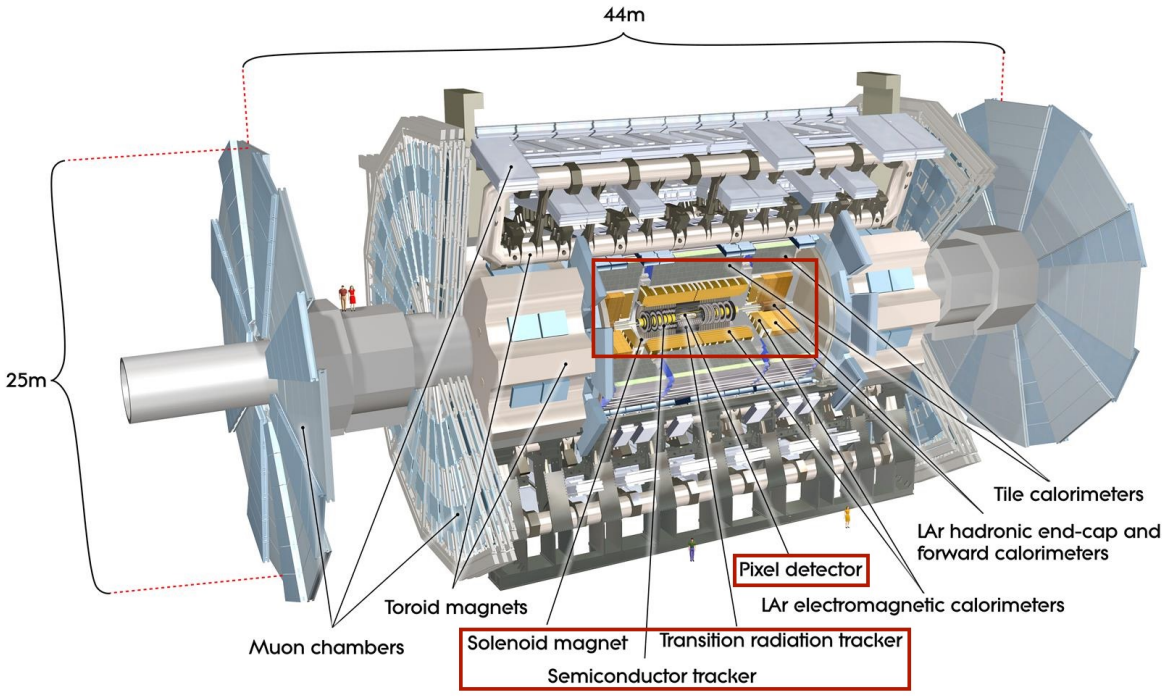
Martin Kocian *for the ATLAS Collaboration*

Vertex 2023, Sestri Levante

16 October 2023

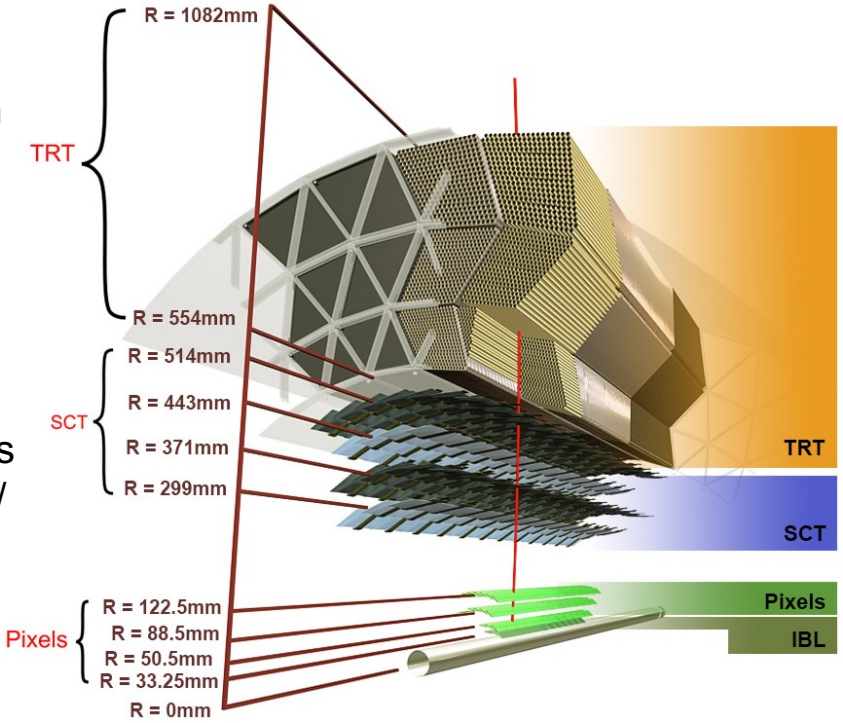
SLAC NATIONAL ACCELERATOR LABORATORY

The ATLAS Inner Detector



The ATLAS Inner Tracker:

1. Pixel
2. Silicon Strip Detector (SCT)
3. Transition Radiation Tracker (TRT)



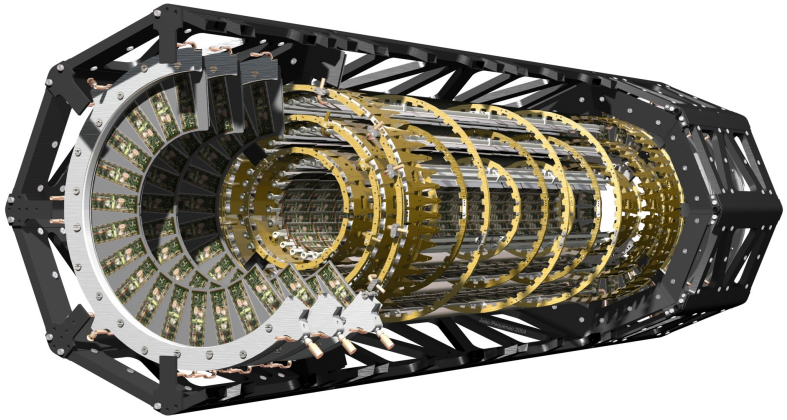
TRT:
- 350000 channels
- 130 μm resolution
- 4 mm element size

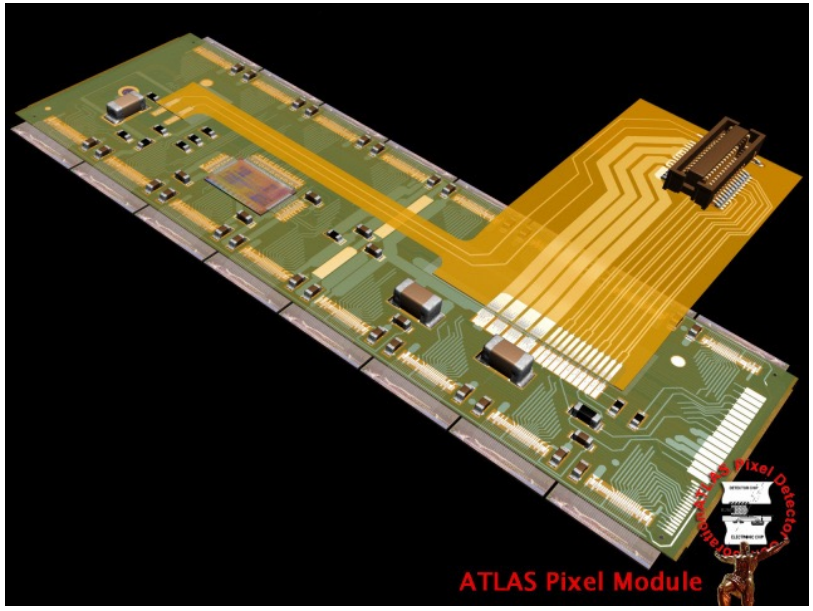
SCT:
- 6.3 million channels
- 17 μm x 570 μm resolution
- 130 μm x 12 cm element size

PIX/IBL:
- 92 million channels
- 10 x 115 μm (PIX)/ 8 x 40 μm (IBL) resolution
- 50 μm x 400 μm / 250 μm (IBL) element size

The Pixel Detector

- Three barrel-layers and 2 x 3 endcap-disks.
- Barrel radii 5.05 cm (B-layer), 8.85 cm (Layer 1), 12.25 cm (Layer 2).
- Angular coverage $|\eta| < 2.5$
- 1744 modules.
- 1.7 m^2 of silicon.
- C_3F_8 evaporative cooling.
- 43 institutes participate.





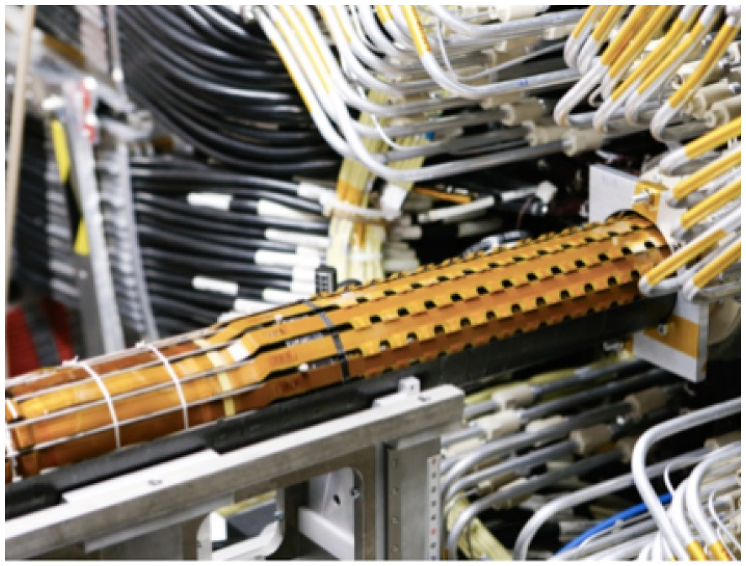
Each pixel module consists of

- 1 planar n-on-n sensor 60.8 mm x 16.4 mm active area, 250 μm thick.
- 16 FEI3 frontend chips plus one controller (MCC) in 0.25 μm CMOS technology.
- 1 flex that provides the electrical connections.

Additional properties:

- The frontends are bump-bonded to the sensors with solder and indium bumps.
- 46080 pixels per module.
- 8-bit Time-over-threshold information per hit.
- Radiation hard to 1 x 10^{15} n_{eq}/cm^2.

IBL (Insertable B-Layer)



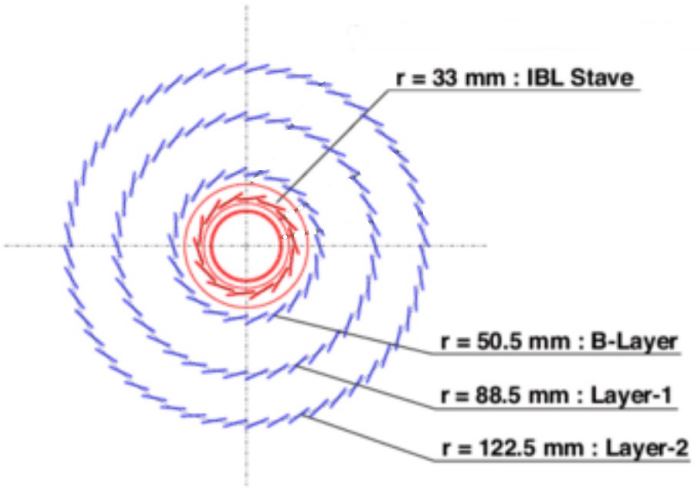
- New innermost layer of the Pixel Detector, added in the 2013-2014 LHC long shutdown 1.
- 14 staves in a turbine-like geometry at a radius of 3.3 cm.
- 448 FEI4 frontends.
- CO_2 evaporative cooling.
- Rad hard up to 5 x 10^{15} n_{eq}/cm^2.

Frontend Chip (FEI4):

- 26880 pixels.
- 336 rows (phi) and 80 columns (z).
- 2 cm x 1.8 cm in size.
- 130 nm CMOS.
- Solder-bump-bonding to sensors.
- 4-bit time-over-threshold information.

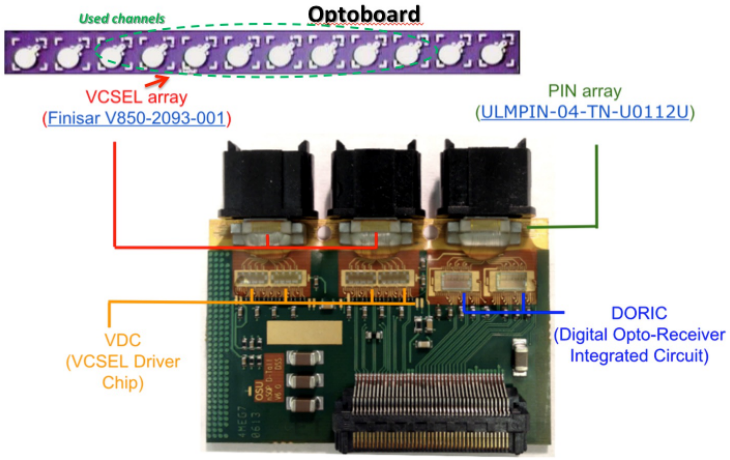
Sensors:

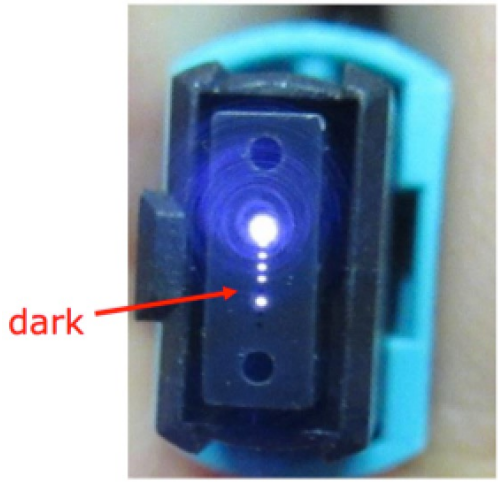
- Central-η region uses 200 μm thick planar sensors.
- High-η region has 230 μm thick 3D-sensors.
- Single-chip-modules for 3D and double-chip modules for planar.



Pixel Hardware Status

- Opto-electrical conversion boards were replaced on the detector in early 2021 because of dying VCSELs (root cause unknown).
- No new failures since then.
- Total number of disabled modules very stable. There were, however, some recoveries during LS2 and some new failures since then.
- Detector in great shape after 15 years of operation!
- Two more years to go before complete replacement.

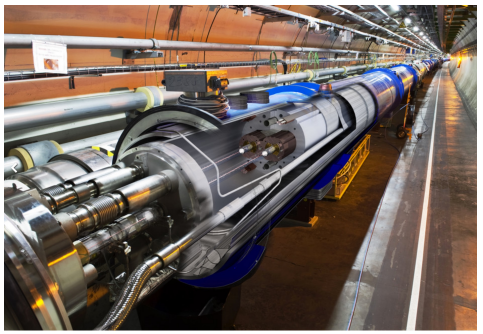




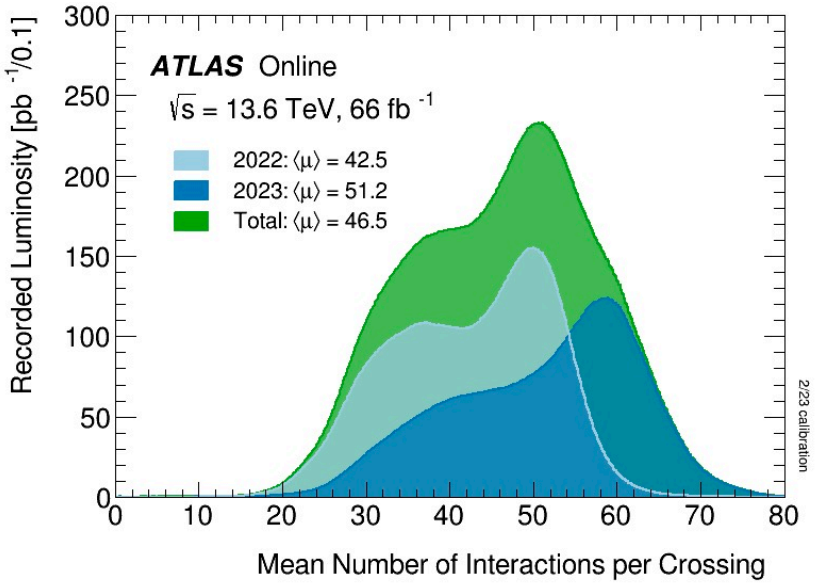
Disabled Modules

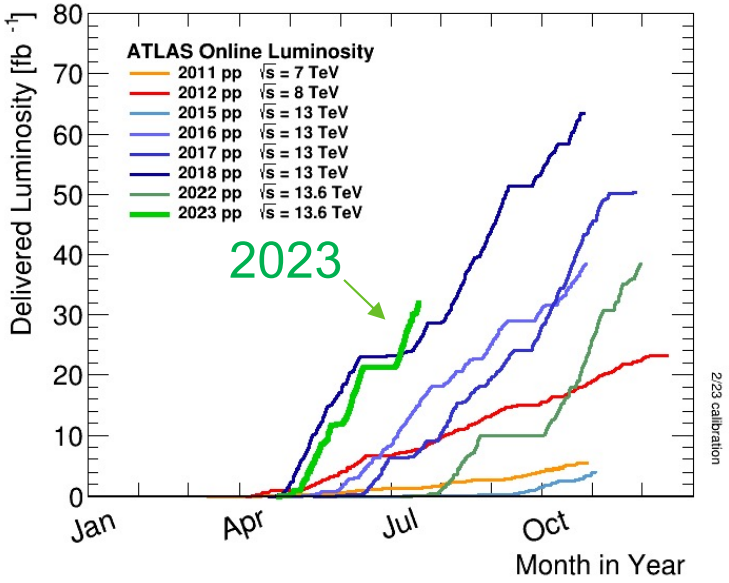
Layer	Disabled/Total 2018	Disabled/Total 2023	Percentage 2023
Disks	15/288	13/288	4.5
B-Layer	18/286	15/286	5.2
Layer 1	29/494	22/494	4.5
Layer 2	33/676	43/676	6.4
Total (Pixel)	95/1744	93/1744	5.3
IBL (Frontends)	3/448	4/448	0.9
Total	**98/2192**	**97/2192**	**4.4**

LHC Status



- In 2023, LHC was able to increase the instantaneous luminosity without running into thermal issues in the arcs, which was previously thought to be the limiting factor.
- This means that the pile-up in 2023 was substantially increased w.r.t 2022, resulting in more challenging conditions for Pixel.
- The 2023 pp run was proceeding nicely but then got cut short in early July because of a vacuum leak.





Pixel Performance Overview

- 99.8 % data quality efficiency in Pixel in 2023.
- Average deadtime of 0.03 % during stable beams on the entire 2023 dataset.
- Extremely stable running this year with no major issues.

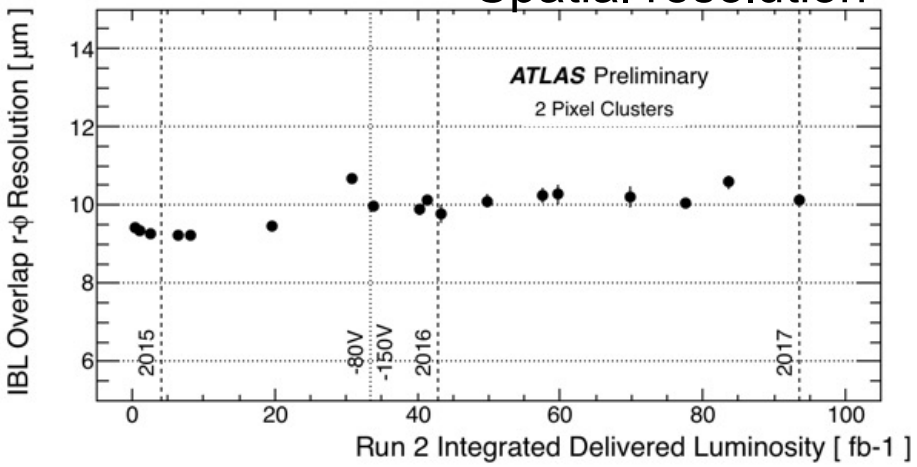
ATLAS pp Run-3: 2023

Trigger	Inner Tracker			Calorimeters		Muon Spectrometer			Magnets	
L1+HLT	Pixel	SCT	TRT	LAr	Tile	MDT	RPC	TGC	Solenoid	Toroid
97.5-99.6	99.8	99.7	100	99.5	99.6	99.7	99.9	99.8	100	100

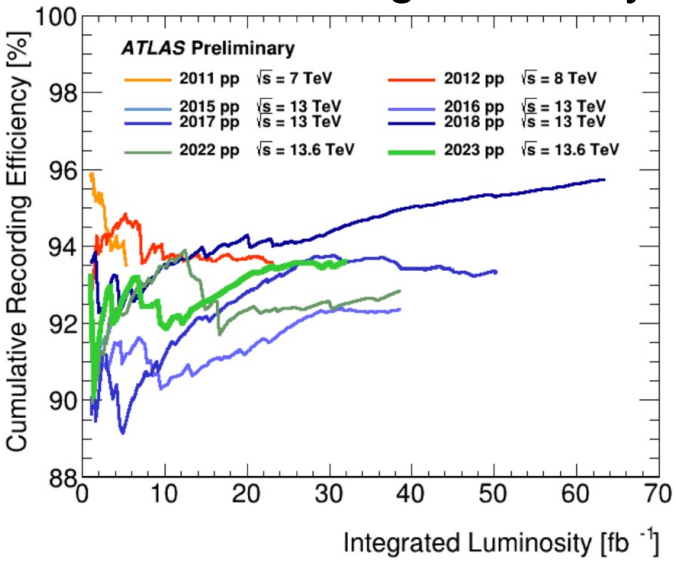
Good for physics: 94.6%-96.5% (27.2-27.8 fb^{-1})

Data Quality Efficiency

Spatial resolution



ATLAS Recording Efficiency



Threshold Evolution

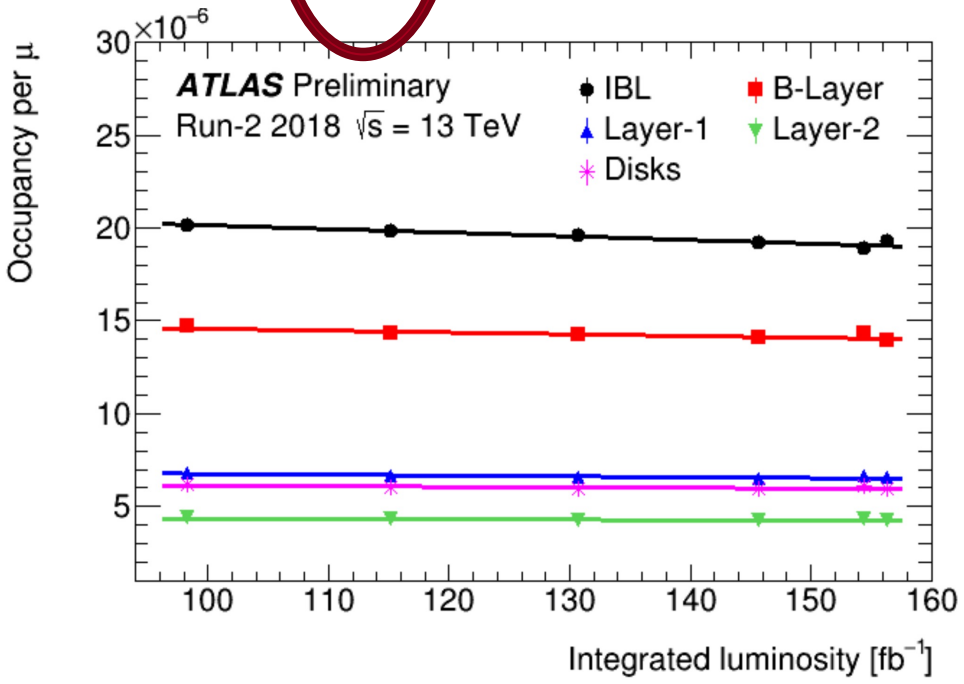
Thresholds in electrons

Layer	2015	2016	2017	2018	2022	2023
IBL	2500	2500	2500	2000	1500	1500
B-Layer	3500	5000	5000	4300*	3500*	4700
Layer1/2	3500	3500	3500	3500	3500	4300
Disks	3500	3500	4500	3500	3500	4300

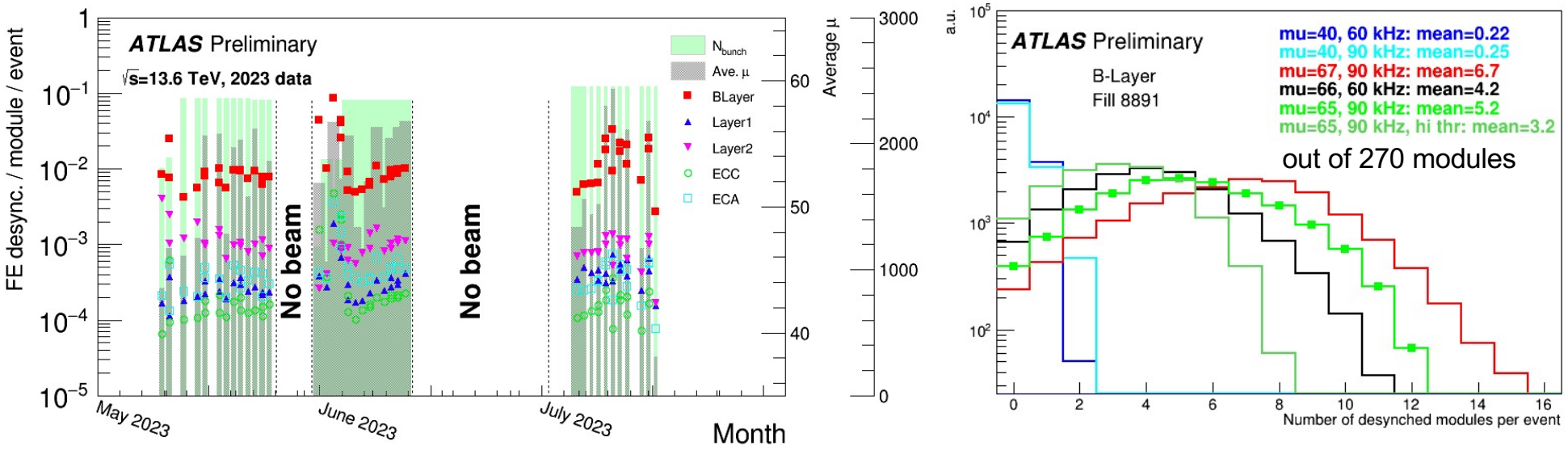
*Inner part of the B-layer only. Higher in higher eta regions.

Increased Thresholds in 2023

- Originally, the thresholds were optimized to balance bandwidth versus hit-on-track efficiency.
- This balance was impacted by radiation damage on the one hand, and LHC performance on the other hand.
- With increased machine performance, frontend limitations start to play a more significant role (cf. following slides).



Intra-module desynchronization



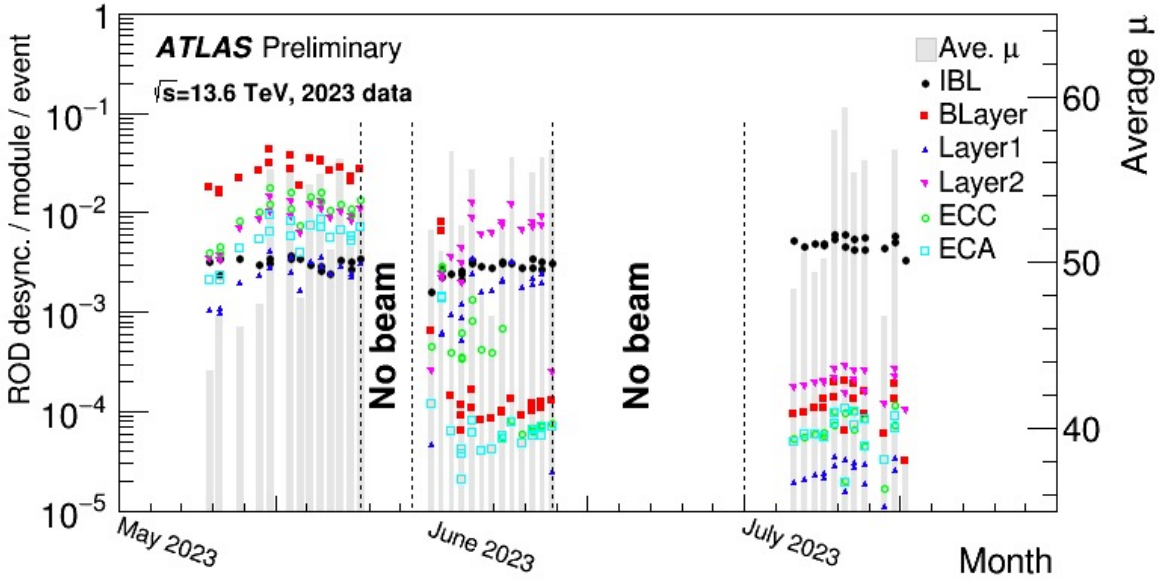
- The Pixel layer modules consist of multiple frontends and one controller.
- If conditions get too harsh, single frontends can desynchronize.
- This leads to unusable events from this module until the next ATLAS event-counter-reset (ECR) which happens every 5 seconds.
- Increasing the threshold helps because it decreases the number of digital hits inside the frontend chips.
- The B-layer is affected the most.

ROD-level Desynchronization and Smart L1-Forwarding

SLAC

PROBLEM:

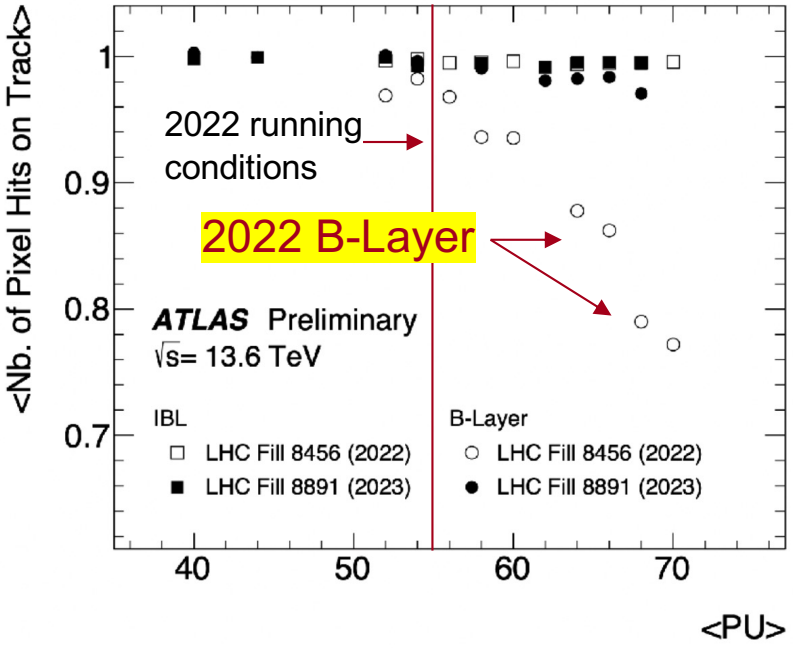
- The Pixel/IBL modules can only handle up to 16 triggers at a time.
- The ATLAS trigger system cannot guarantee that this limit will not be exceeded as the time that a trigger is processed inside a module varies with occupancy.
- Once a trigger has been missed, the module will be desynched until the next ATLAS event-counter reset (up to 5 s).



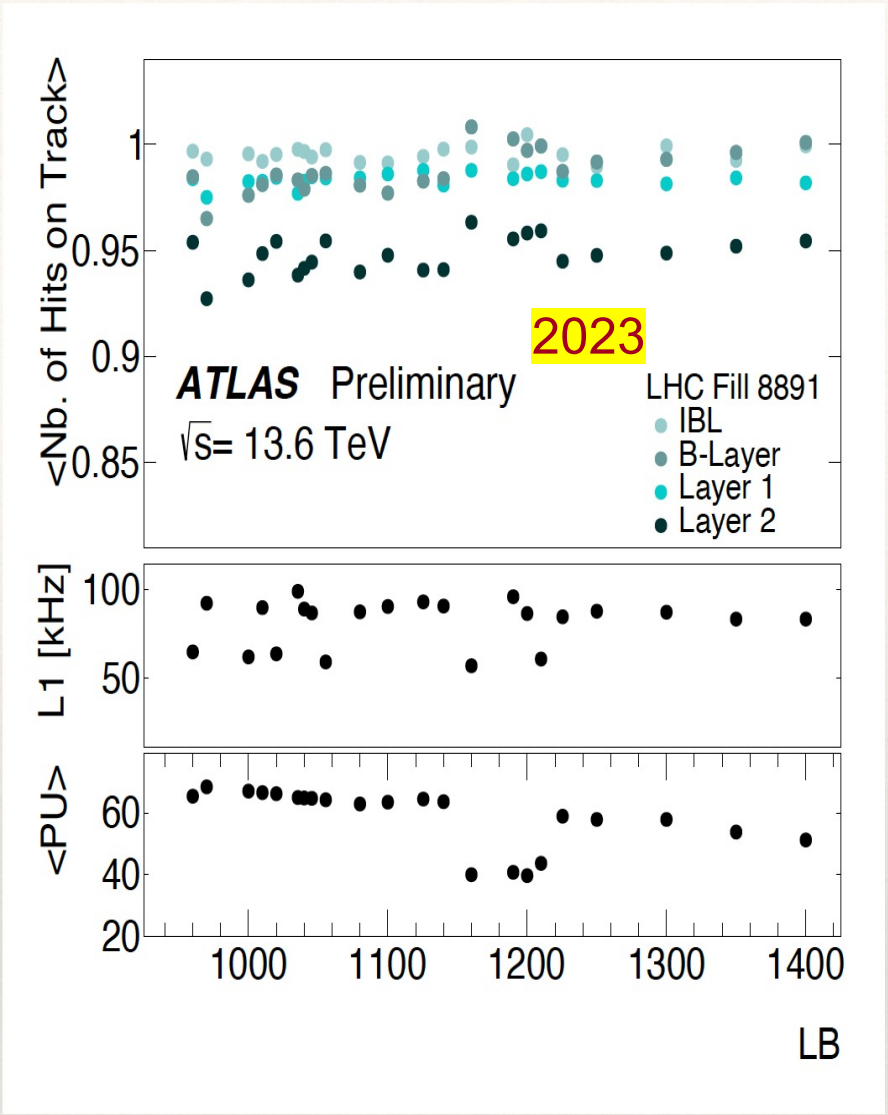
SOLUTION:

- New firmware deployed following a major effort of development and testing.
- Keeps track of the number of pending triggers for each module.
- If a module would not be able to handle a trigger, it is not sent. Instead, the firmware inserts a dummy fragment into the data stream and keeps track of the L1ID.
- This way, only single events are lost, while all subsequent events are in synch.
- Improvement by several orders of magnitude in Pixel desynchronization.
- The same mechanism is in preparation for the IBL FW.

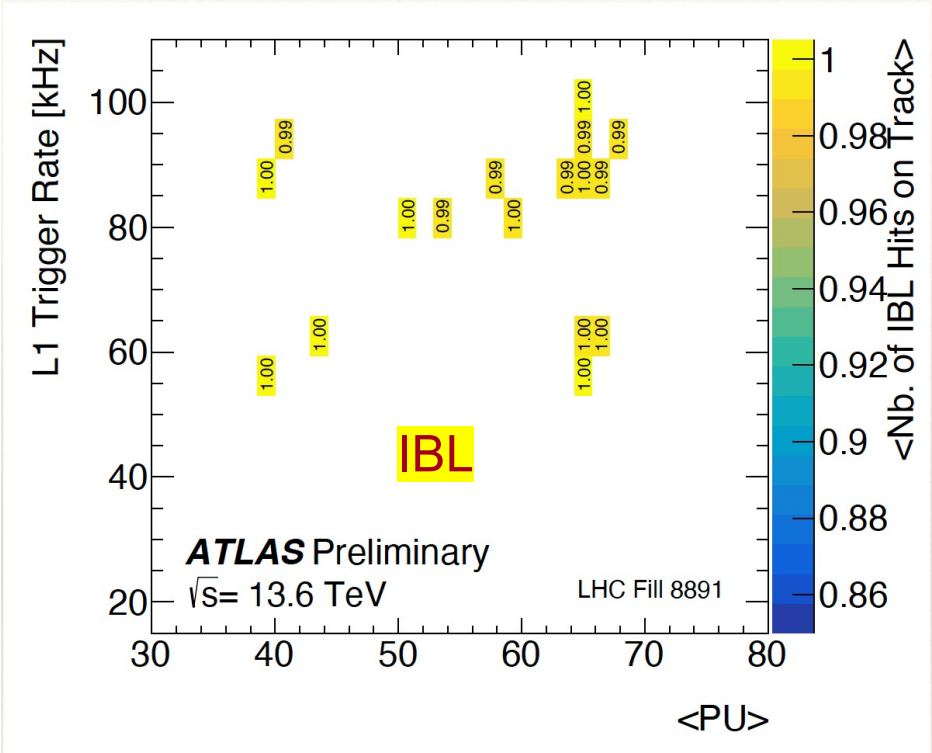
Hit-on-Track Efficiency at High Pile-Up

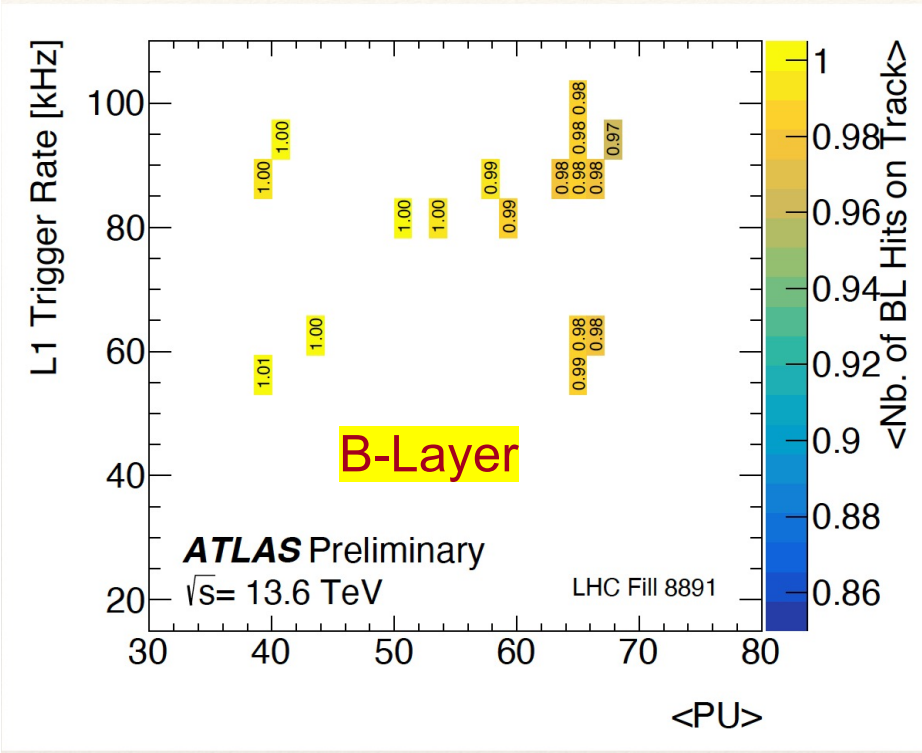


- In 2022, the B-layer efficiency was good up to a pile-up of 55 (LHC limit in 2022) but dropping fast above that.
- Not a bandwidth problem, but an issue with the frontends (that were built for a PU of 23).
- With the increased 2023 thresholds and smart firmware, the B-layer efficiency remains stable even at high pile-up.
- IBL does not show this problem as it uses different frontend chips.



Hit-on-Track Efficiency Exploration

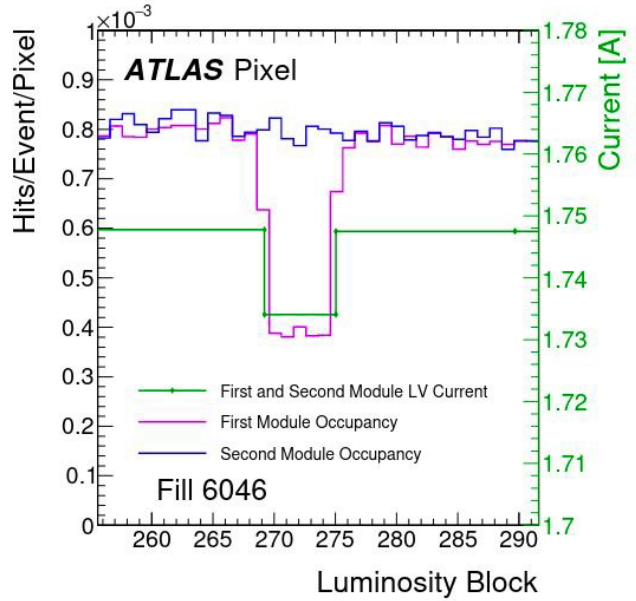


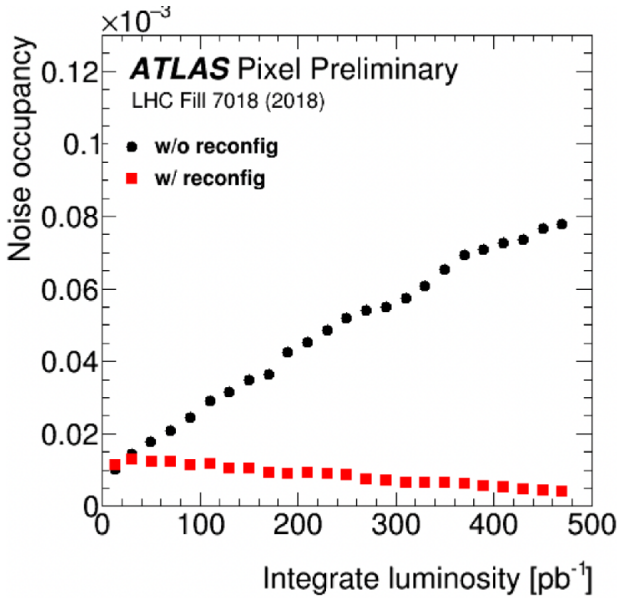


- The hit-on-track efficiency depends on the trigger rate as well as on the pile-up.
- In a special run, the parameter space was explored.
- With the new thresholds, the B-layer efficiency is very stable.
- IBL shows stable efficiency even with low thresholds because it uses different frontend chips.

Reconfiguration at ECR

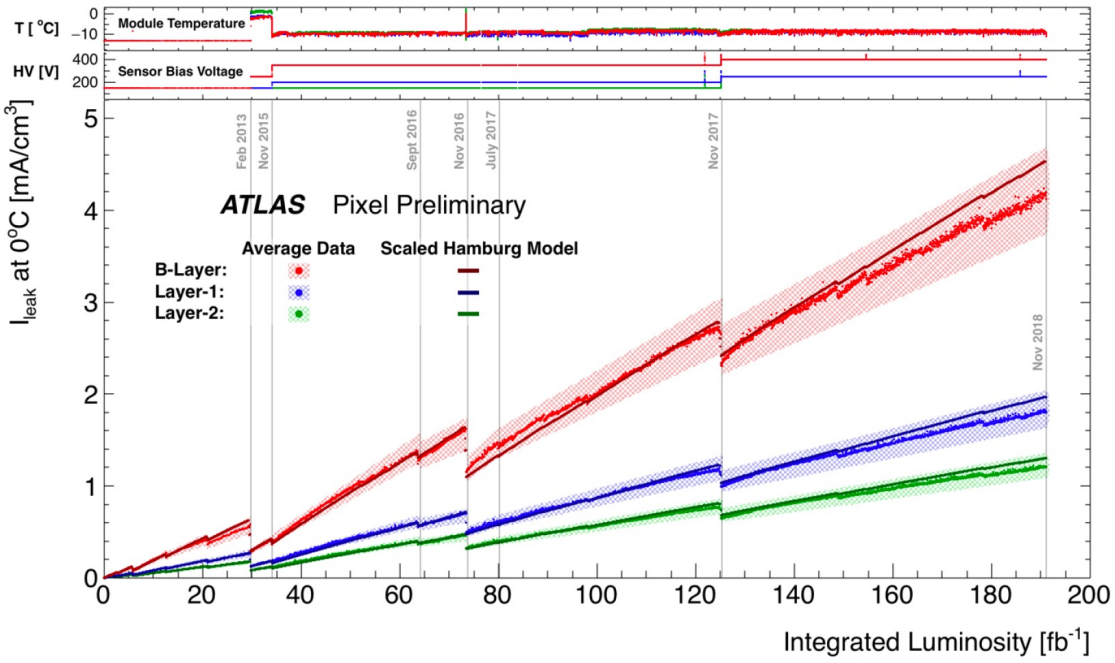
- Single Event Upsets (SEUs) can compromise the functioning of the frontend chip.
- If global registers get hit, the entire module can start misbehaving.
- If pixel registers are hit, this can result in silent or noisy pixels.
- Already in Run 2, a global register reconfiguration for IBL every 5 s was implemented.
- In 2023, global reconfiguration for one frontend per module per ECR in Pixel was deployed, i.e. every FE is reconfigured every 80 s.
- Pixel level reconfiguration in IBL was deployed in 2023 after upgrading the ROD OS from xilkernel to Linux. Every pixel register gets updated every 11 minutes.
- This has led to substantially lower noise in IBL.
- The reconfiguration adds no deadtime for ATLAS, because it happens inside the ”ECR gap”, a 2 ms busy-period that is generated in ATLAS every 5 s.



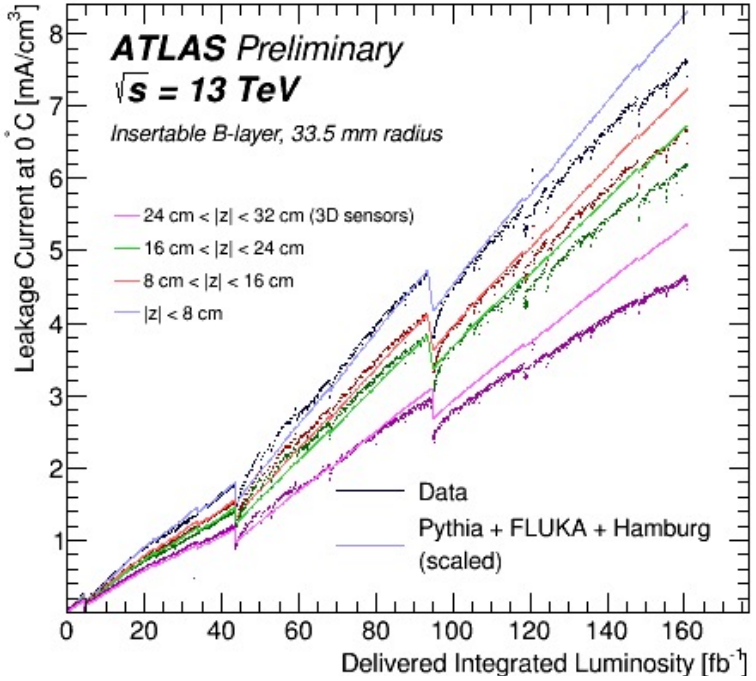


Leakage Current

Pixel



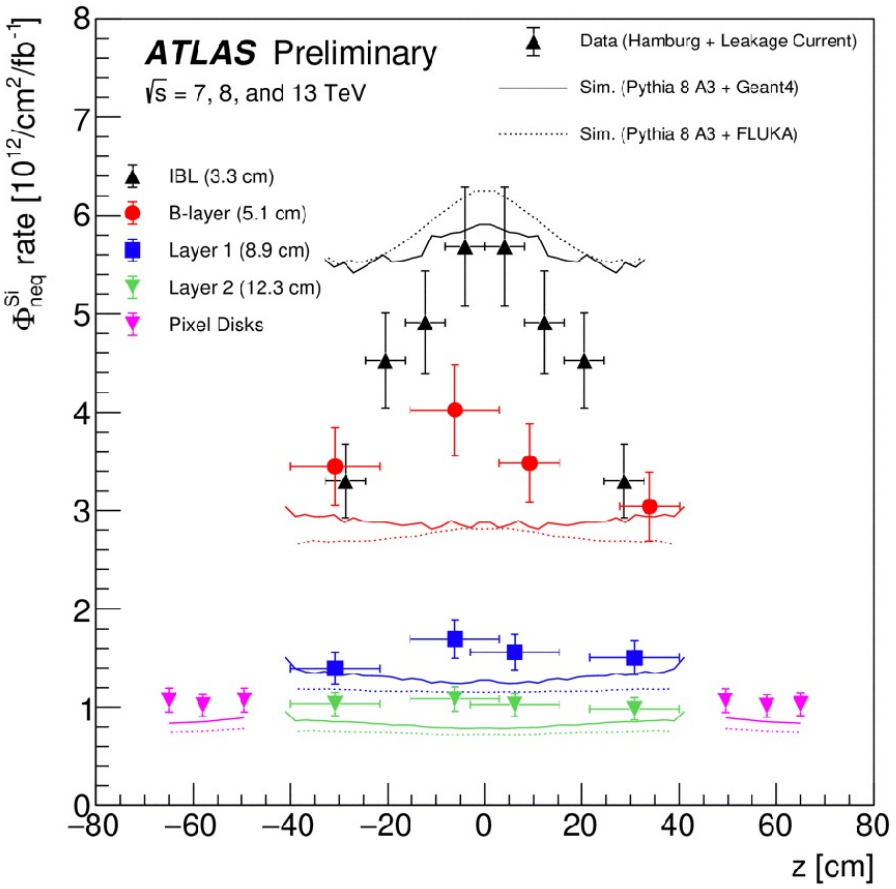
IBL



- Comparison of the leakage current with the Hamburg model shows similar features for Pixel and IBL.
- A scaling factor (per layer for Pixel, per z range for IBL) is needed for the the Hamburg model to match the data.
- Towards the end of run 2 the leakage current is overestimated by the model.
- Using the Hamburg model to extrapolate the leakage currents to the end of run 3, we find that the final currents at the current operating temperature of -12 °C will be well below the operational limits of the high voltage power supplies and services.

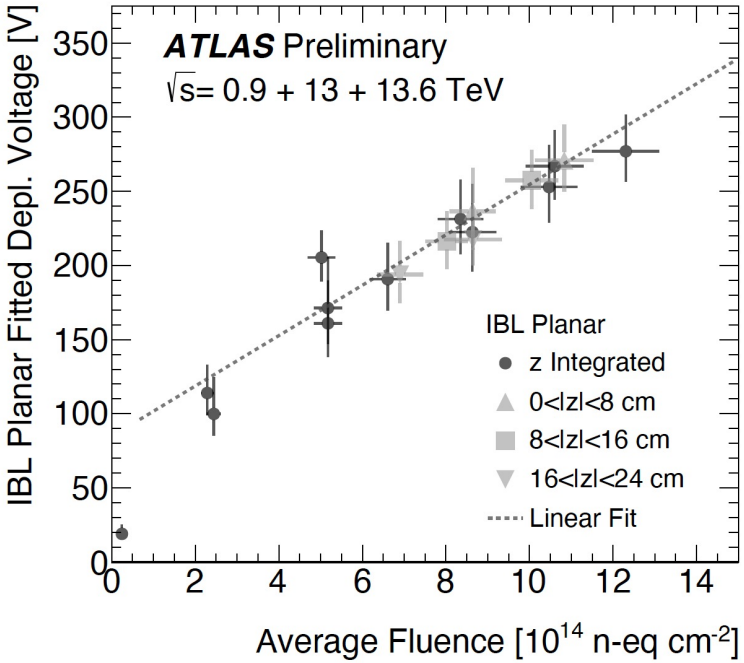
Fluence vs. z

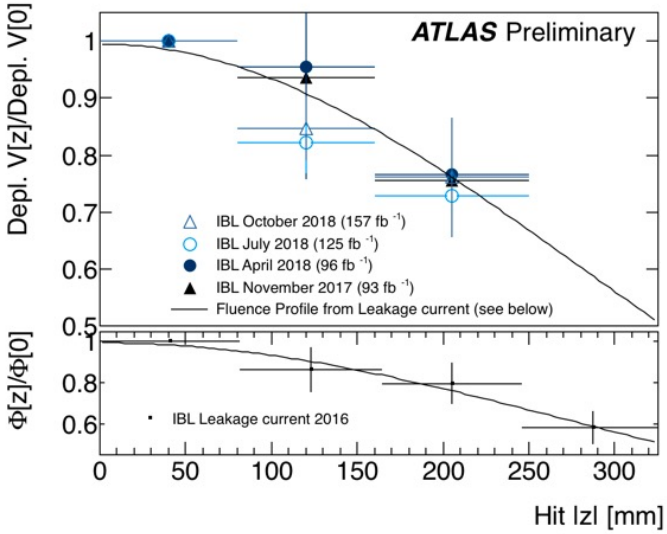
- Comparison of simulated fluence (Geant4/Fluka) with the fluence obtained from the leakage currents using the Hamburg model.
- Simulated fluence for Pixel slightly below leakage current fluence.
- IBL simulated fluence quite flat along z. The leakage current fluence has a strong z dependence.

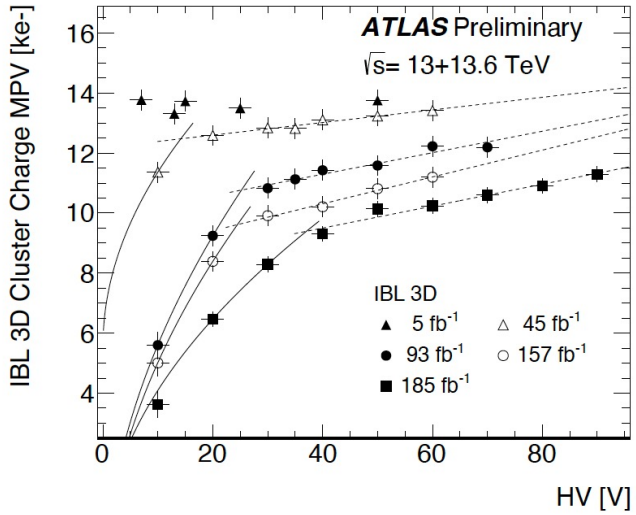


Depletion Voltage IBL

- Depletion voltage increasing with fluence.
- Depletion voltage for planar at 270 V in 2023, for 3D at 37 V (CNM) and 28 V (FBK).
- Well below operational limit of 1000 V (planar) and 500 V (3D).
- Clear Z-dependency.

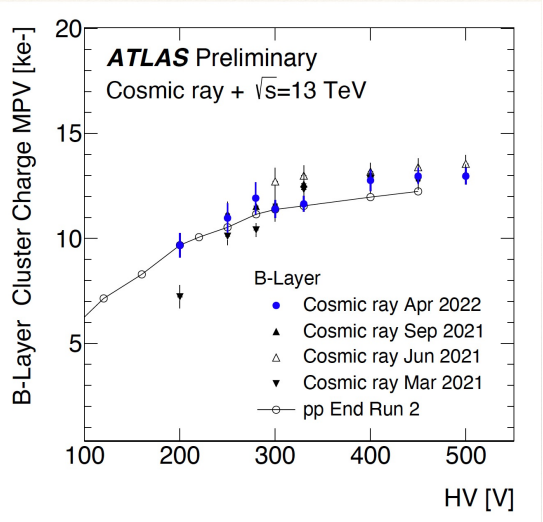


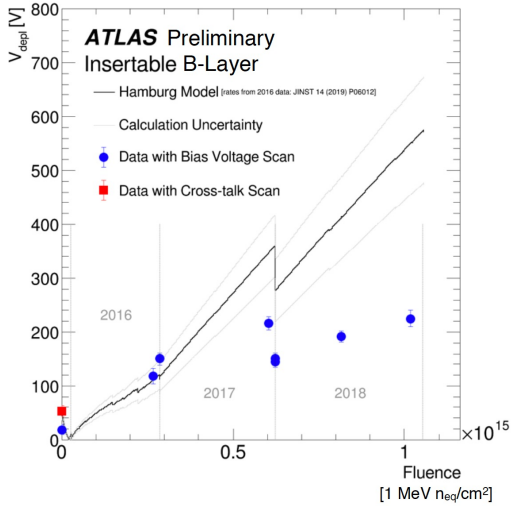




Depletion Voltage B-Layer

- Depletion voltages are lower than Hamburg model predictions.
- Depletion voltages well below operations limit (1000 V IBL planar, 500 V IBL 3D, 600 V Pixel).
- Raising the bias voltage over time because of the linear rise of the collected charge above the depletion voltage.





Depletion voltage

Layer	Depletion voltage
IBL planar	270 V
IBL 3D FBK	28 V
IBL 3D CNM	37 V
B-Layer	230 V

Bias voltage

Layer	2015	2016	2017	2018	2022	2023
IBL	80 V	150 V	350 V	400 V	450 V	450 V
B-Layer	250 V	350 V	350 V	400 V	450 V	450 V
Layer 1	150 V	200 V	200 V	250 V	300 V	350 V
Layer 2	150 V	150 V	150 V	250 V	300 V	350 V
Disks	150 V	150 V	150 V	250 V	300 V	350 V

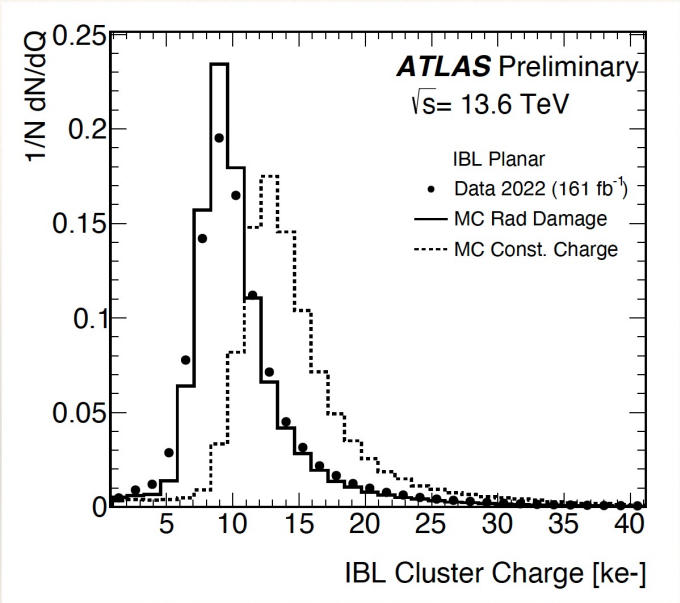
Radiation Damage Simulation

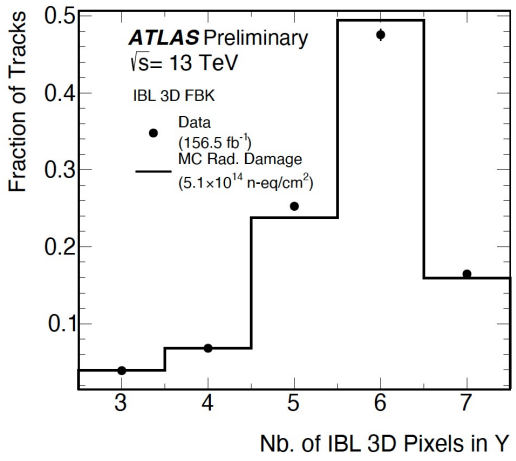
SLAC

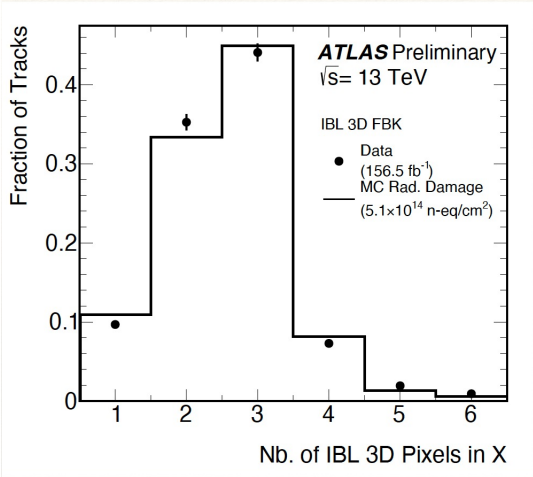
Fluence

Layer	End of Run 2 [n_{eq} cm^{-2}]	Now [n_{eq} cm^{-2}]	End of Run 3 [n_{eq} cm^{-2}]	Specification [n_{eq} cm^{-2}]
IBL	9 x 10^{14}	1.2 x 10^{15}	2.1 x 10^{15}	**5 x 10^{15}**
B-Layer	4.5 x 10^{14}	1.0 x 10^{15}	1.5 x 10^{15}	**1 x 10^{15}**

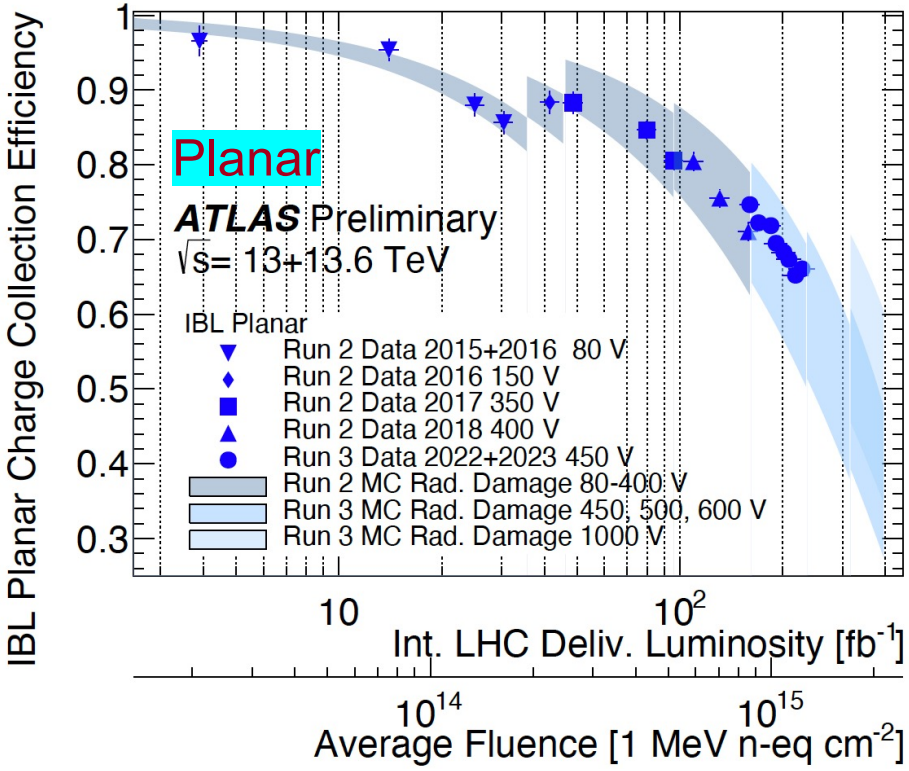
- Radiation damage has a significant impact on the performance of the detector.
- Models are used to understand and predict radiation damage effects.
- The standard ATLAS Monte Carlo now includes Pixel/IBL radiation damage effects.
- The radiation damage digitizer provides a good description of the data at various fluences.
- Simulation is also important to predict performance for the remaining years of running.

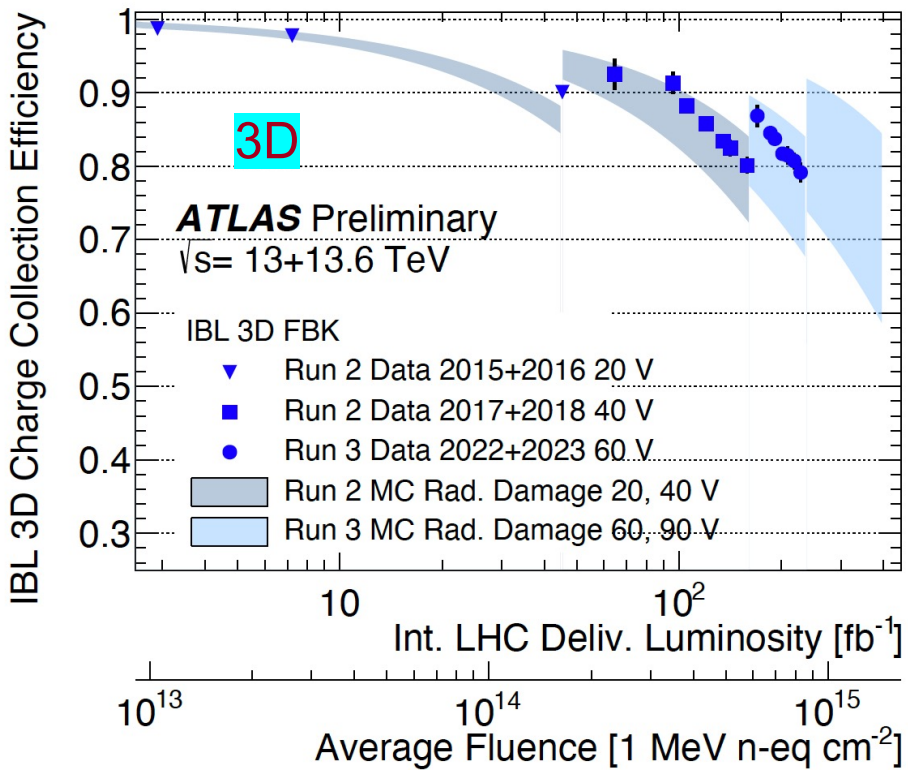






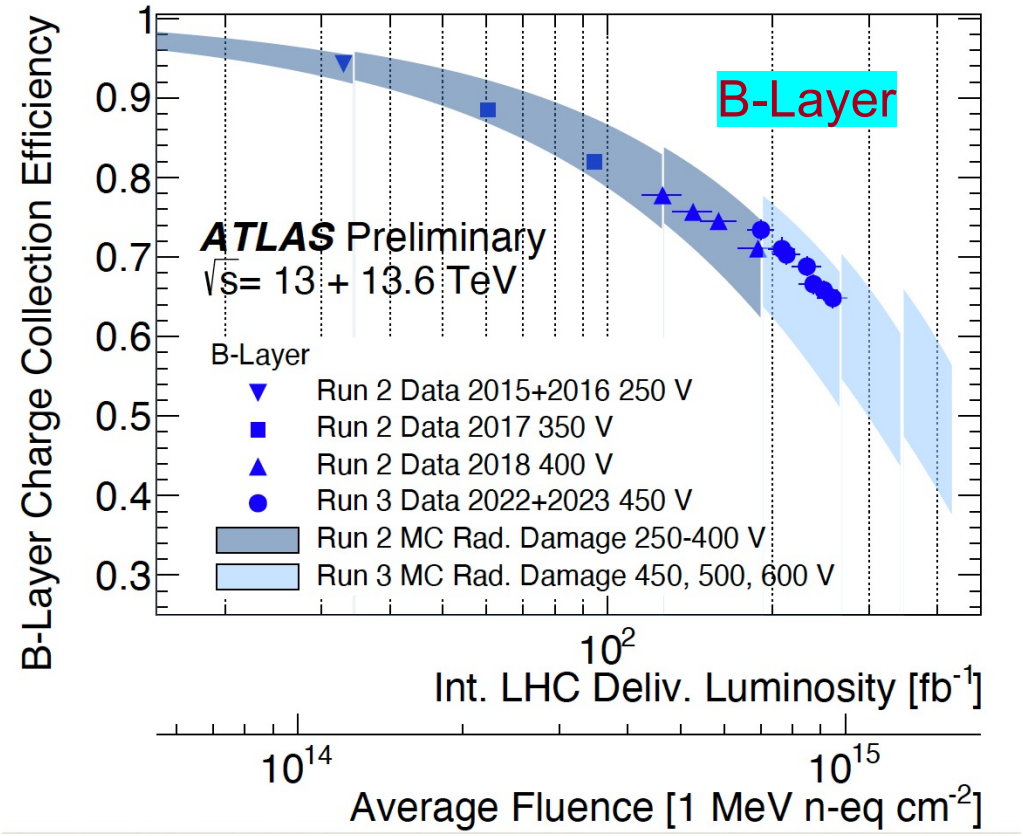
Charge Collection Efficiency IBL





- Simulation until the end of Run 3.
- HV setting changes cause discontinuities in simulation bands.
- 3D more radiation hard than planar (but also lower fluence).
- Charge is not the same as hit efficiency!

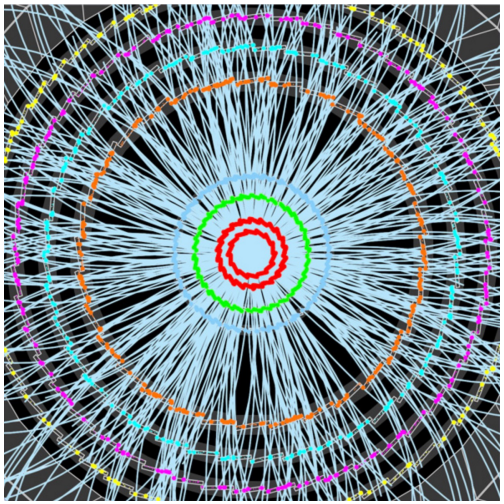
Charge Collection Efficiency B-Layer



- Simulation until the end of Run 3 (end of life).
- HV setting changes cause discontinuities in simulation bands.
- Past spec of 10^{15}neq/cm^{-2} at the end of Run 3.

Summary and Conclusion

- Run 3 is the final run for the current Pixel detector.
- The ATLAS Pixel detector has delivered excellent performance.
- The operational parameters have been retuned to guarantee optimal data quality and efficiency.
- Firmware improvements to counteract SEUs and desynchronization have been successfully deployed.
- There is a highly evolved effort to simulate all aspects of radiation damage.
- Depletion voltage and leakage current are well under control.



Backup

SLAC

Data Quality Efficiency

SLAC

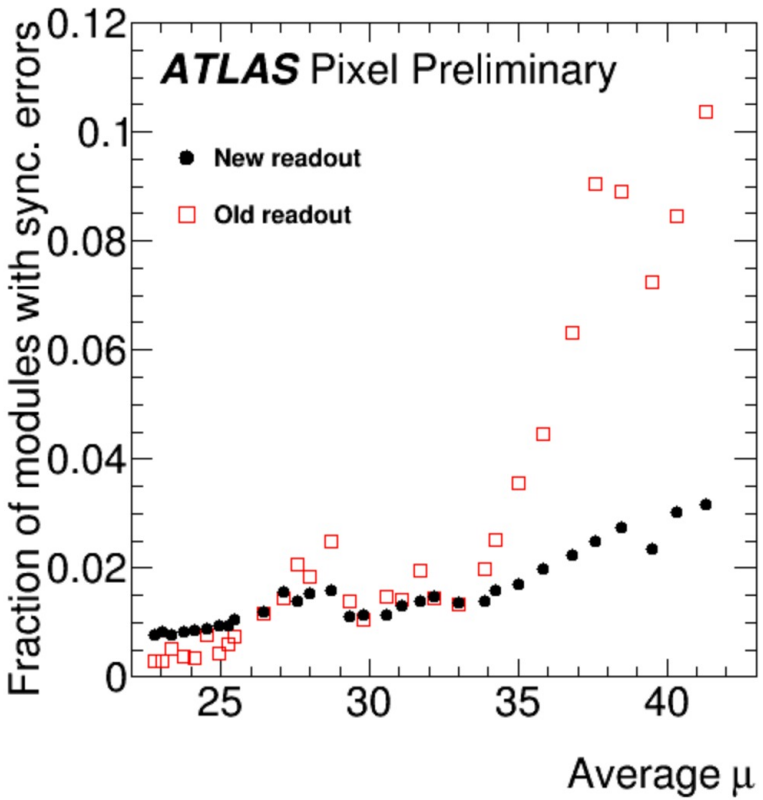
ATLAS pp Run-3: 2023

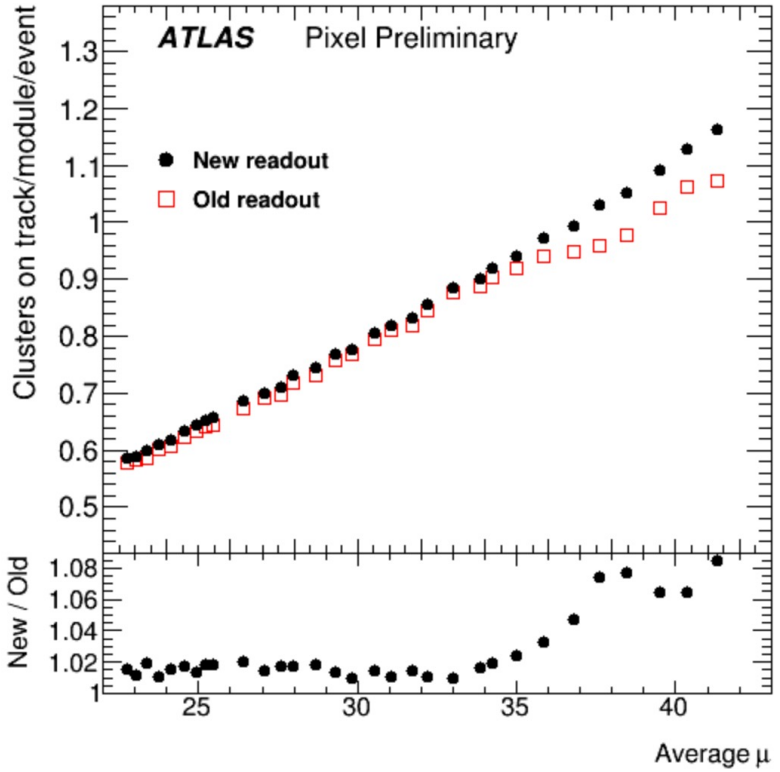
Trigger	Inner Tracker			Calorimeters		Muon Spectrometer			Magnets	
L1+HLT	Pixel	SCT	TRT	LAr	Tile	MDT	RPC	TGC	Solenoid	Toroid
97.5-99.6	99.8	99.7	100	99.5	99.6	99.7	99.9	99.8	100	100

Good for physics: 94.6%-96.5% (27.2-27.8 fb^{-1})

Luminosity weighted relative detector uptime and good data quality efficiencies (in %) during stable beam in pp collision physics runs at $\sqrt{s}$=13.6 TeV for the 2023 Run-3 period, corresponding to a delivered integrated luminosity of 30.6 fb^{-1} and a recorded integrated luminosity of 28.8 fb^{-1}. Runs with specialized physics goals or non-standard running conditions, amounting to 1.1 fb^{-1}, are not considered and thus not included in the denominator of the efficiency calculation. Dedicated luminosity calibration activities during LHC fills used 0.35% of recorded data in 2023 and are included in the inefficiency. When the stable beam flag is raised, the tracking detectors undergo a so-called "warm start", which includes a ramp of the high-voltage and turning on the pre-amplifiers for the Pixel system. The inefficiency due to this, as well as the DAQ inefficiency, are not included in the table above, but accounted for in the ATLAS recording efficiency. The luminosity good for physics is 27.2-27.8 fb^{-1}, with the lower number being applicable to analyses relying on triggers based on electrons, photons or non-isolated tau leptons at L1. It is reduced to 25.8 fb^{-1} for analyses relying on triggers based on jets at L1 or HLT. The trigger DQ inefficiencies are due to trigger commissioning in early 2023 and an occasion of mistimed jet triggers in May 2023.

Desynchronization

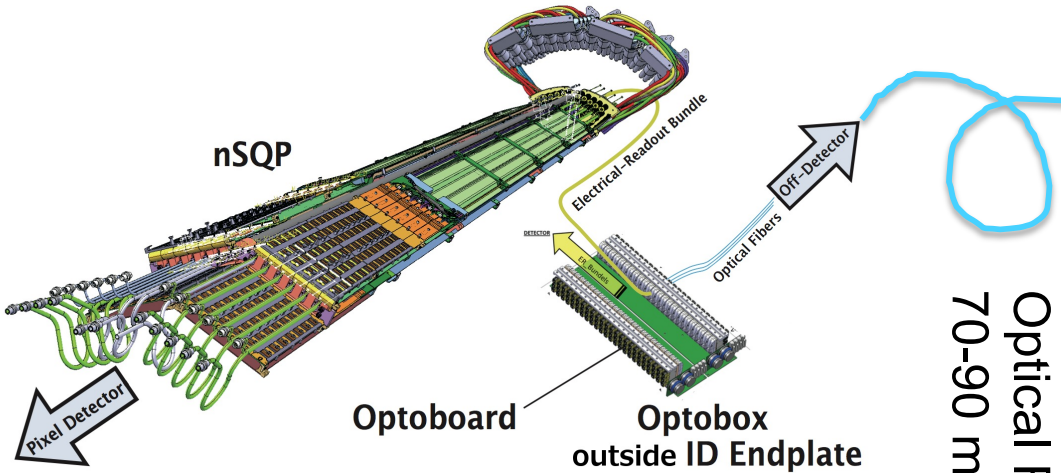




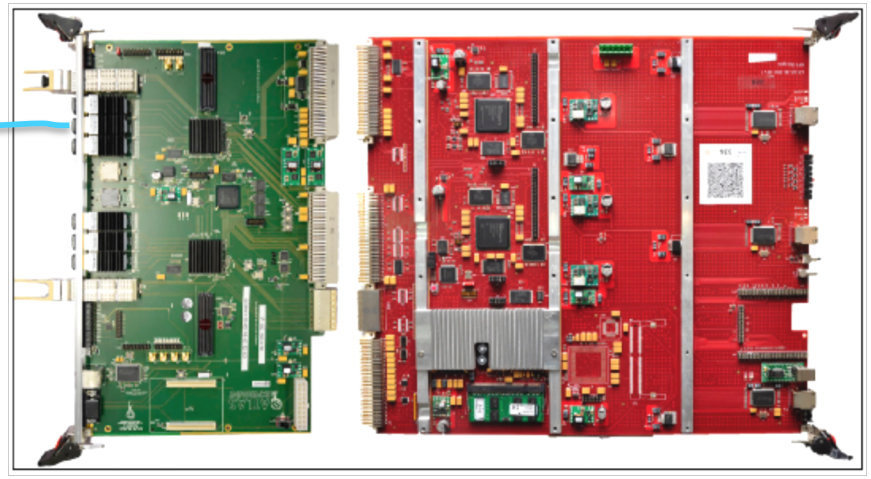
- Luminosity and pile-up are much larger than originally specified.
- High occupancy can lead to buffer overflows resulting in event fragments being associated with the wrong event ("desynchronization").
- A periodic reset of the frontend ASICs and of the firmware in the backend every 5 seconds was introduced to resynchronize all data sources.

Substantially improved data taking efficiency!

Readout System



Optical Fiber
70-90 m



On-detector

Off-detector

- On-detector (as of 2014):
  - Readout per module (no multiplexing) at 80 Mbps (Layer 2, disk 1/3) and 160 Mbps (others).
  - Configuration and commands to the modules at 40 Mbps.
  - 6.6 m (IBL 5 m) of twisted pair electrical readout cable.
  - Conversion into optical signals on ID endplate.
- 70-90 m of optical rad-hard multimode fiber.
- Off-detector (now unified using IBL readout hardware everywhere):
  - 116 Back-of-crate cards (BOC) and readout drivers (ROD) in VME crates.
  - 2 (4) s-link fibers for Pixel (IBL) data output at 160 MB/s per s-link.
  - Spartan 6 and Virtex 5 FPGAs.
  - PowerPC on Virtex 5 (ROD) heavily used for configuration and monitoring.