DRD3 - Solid State Detectors
- Research Proposal -

DRD3 Proposal Team

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1 Scope of the DRD3 collaboration

The DRD3 collaboration has the dual purpose of pursuing the realization of the strategic developments outlined by the Task Force 3 (TF3) in the ECFA road map [2] and promoting blue-sky R&D in the field of solid-state detectors.

1.1 The DRD3 working group structure

The DRD3 structure is based on grouping activities broadly focused on common goals. At the moment, the following eight working groups are foreseen [1]:

- WG1 Monolithic CMOS sensors
- WG2 Sensors for tracking and calorimetry
- WG3 Radiation damage and extreme fluences
- WG4 Simulation
- WG5 Characterization techniques, facilities
- WG6 Wide bandgap and innovative sensor materials
- WG7 Interconnect and device fabrication
- WG8 Dissemination and outreach

The work in the WGs is organized around research goals (RG), presented in the subsequent sections of this document.

1.2 The DRD3 proto-collaboration

The interest of the physics community in the DRD3 program has been evaluated via questionnaires.

Presently, the DRD3 proto-collaboration comprises 119 groups from 28 countries, for about 900 interested people (see Annex, page 47). Figure 1 shows the geographical distribution of the DRD3 institutes: $\sim 70\%$ are from Europe, 15% from North America, 10% from Asia, 5% from South America.

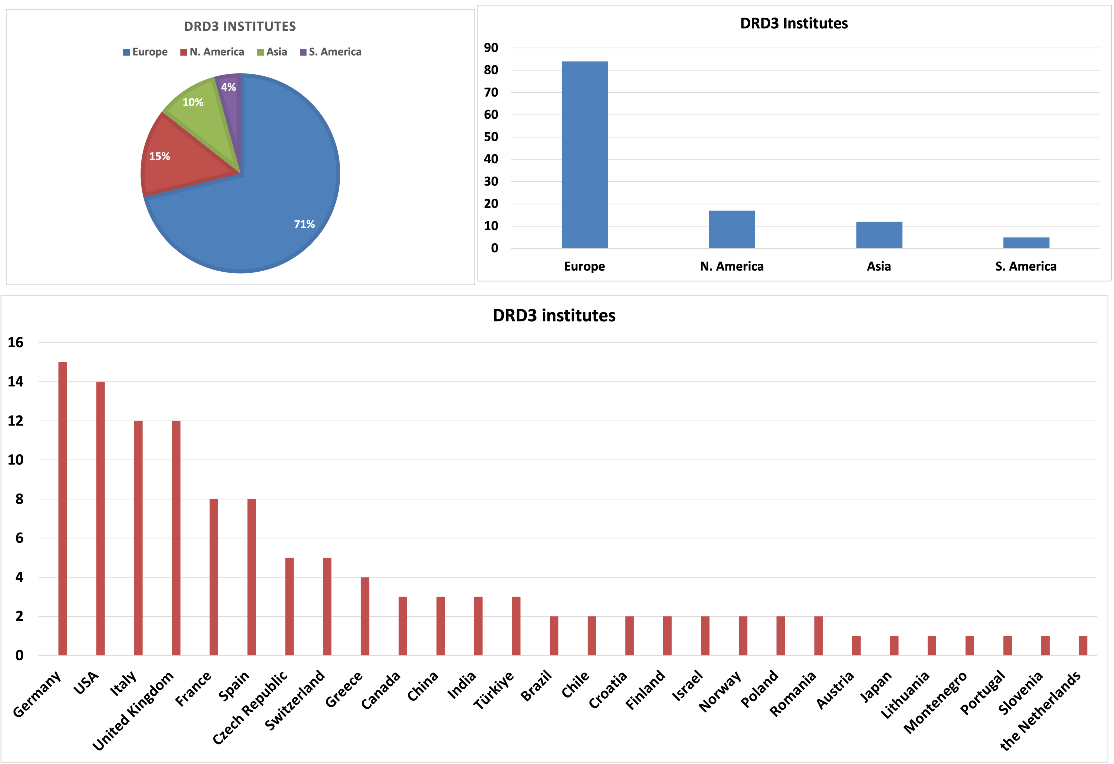


Figure 1: Top: Continent of origin of the DRD3 institutes. Bottom: number of DRD3 institutes per country

1.3 Strategic R&D

The four strategic Detector R&D Themes (DRDT), identified in the ECFA roadmap process [2], are shown in Table 1:

DRDT 3.1 **CMOS sensors**	**DRDT 3.2** **Sensors for 4D-tracking**
DRDT 3.3 **Sensors for extreme fluences**	**DRDT 3.4** **A demonstrator of 3D-integration**

Table 1: The four strategic DRDTs of the DRD3 collaboration

The activities of five WGs map directly into a DRDT, while three WGs are transversal, and their activities benefit all DRDTs. The relation between DRDTs and WGs is shown in Fig. 2.

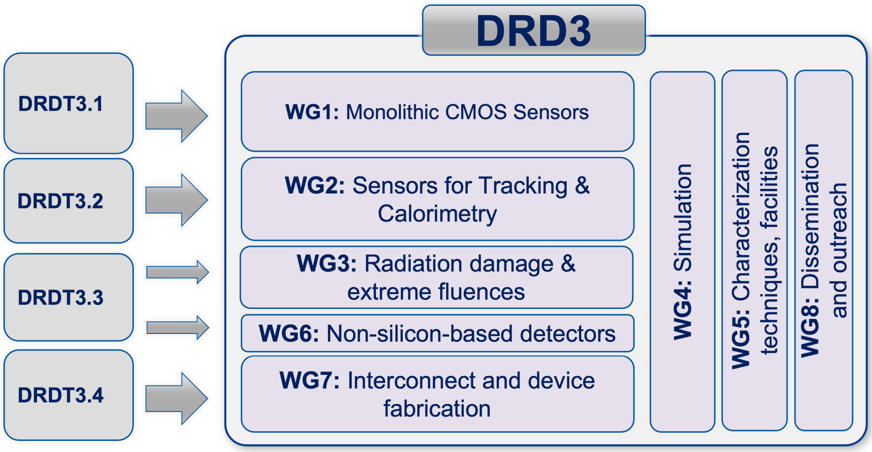


Figure 2: Relationship between DRDTs and Working Groups (WGs)

The implementation of the strategic R&Ds, as defined by the road-map, will happen via several work packages (WP), each focused on a given topic. The envisioned WPs are listed in Table 2. Additional WPs might be defined.

Figure 3 shows the timeline of experiments that are already planned or at the proposal level. In the following, their needs are used to define the most important strategic R&D for the next few years.

1.4 Common R&D

One of the main goals of the DRD3 collaboration is to foster blue-sky research and collaboration among groups. The main tool to achieve these goals is creating a fund to finance selected common projects (CP). It is foreseen that each proposed CP finds 50% of the financing among the proponents, while DRD3 finances the other 50%. In order to access the DRD3 contribution, each CP has to be presented to the collaboration to

DRDT	WP	Title
3.1	1	DMAPS: spatial resolution
3.1	2	DMAPS: timing resolution
3.1	3	DMAPS: read-out architectures
3.1	4	DMAPS: radiation tolerance
3.2	5	4D tracking: 3D sensors
3.2	6	4D tracking: LGAD
3.3	7	Extreme fluence: wide band-gap materials (SiC, GaN)
3.3	8	Extreme fluence: diamond based detectors
3.3	9	Extreme fluence: silicon detectors
3.4	10	3D Integration: fast and maskless interconnect
3.4	11	3D Integration: in house post-processing for hybridization
3.4	12	3D Integration: advanced interconnection techniques for detectors
3.4	13	3D Integration: mechanics and cooling

Table 2: DRD3 work packages. Additional WPs can be added.

Figure 3: Timeline of the near-term R&D

be evaluated. This research fund is financed by an annual fee of about 2,000 CHF each institute must pay.

1.5 DRD3 research structure

Figure 4 graphically shows the DRD3 research structure.

- Research is organized in working groups (WG)
  - WGs focus their activities around research goals (RG)
- The ECFA R&D roadmap identified four strategic Detector R&D Themes (DRDT)
  - The implementation of the DRDTs happens via work packages (WP) with associated deliverables.
- The DRD3 collaboration promotes blue-sky R&D via common projects (CP).

The relationship between work packages and research goals if shown in Section 10.

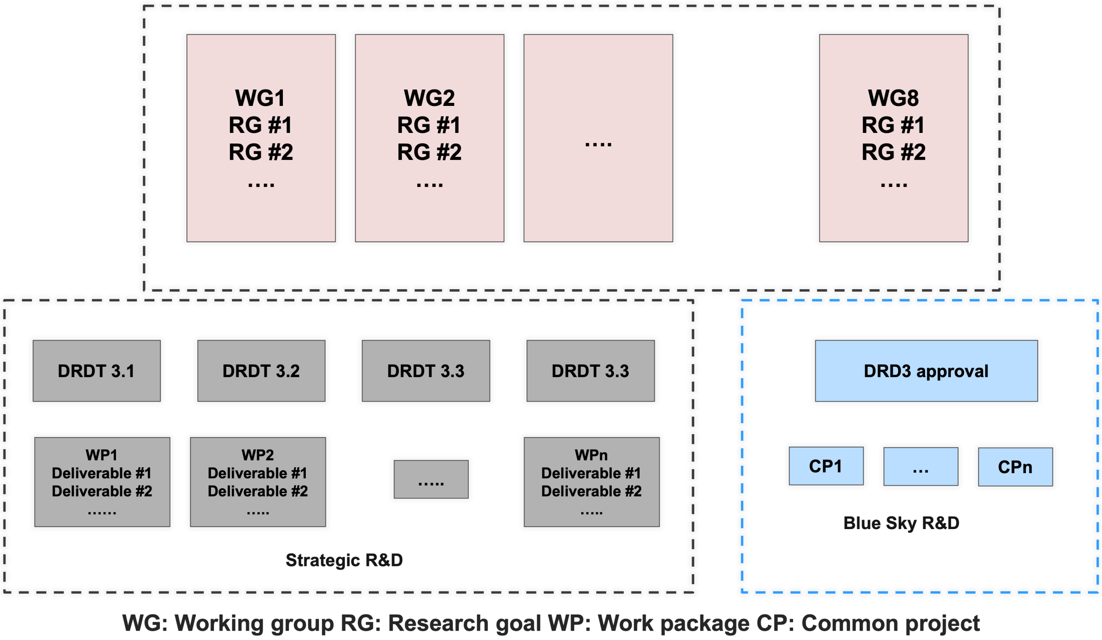


Figure 4: The DRD3 structure

1.6 Institutes participation to working groups and work packages

Figure 5 reports the number of institutes willing to contribute to each working group or work package. The figures show that the collaboration is well distributed among WGs and WPs.

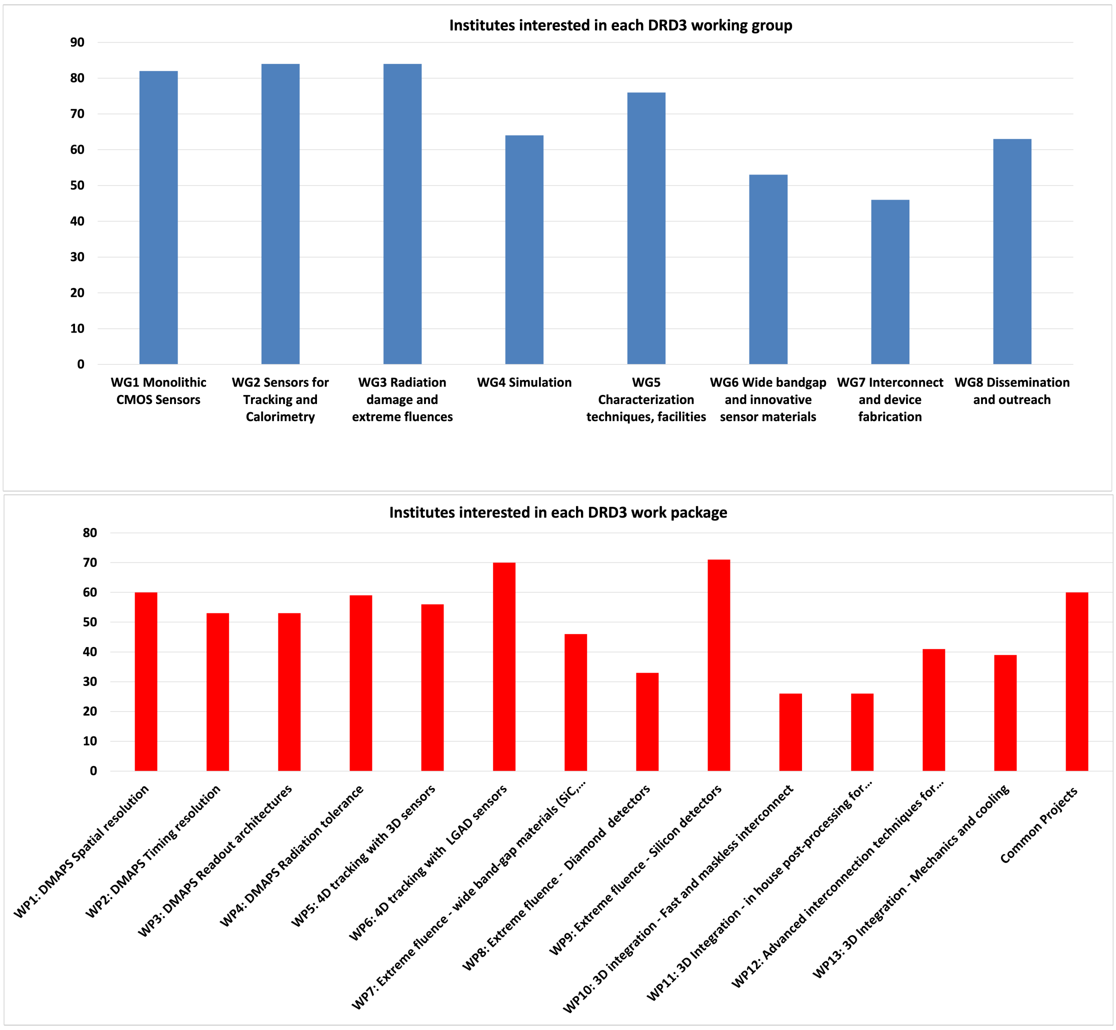


Figure 5: Top: number of institutions interested in each working group. Bottom: number of institutions interested in each work package

Figure 6 details the number of institutes interested in each WG for each country.

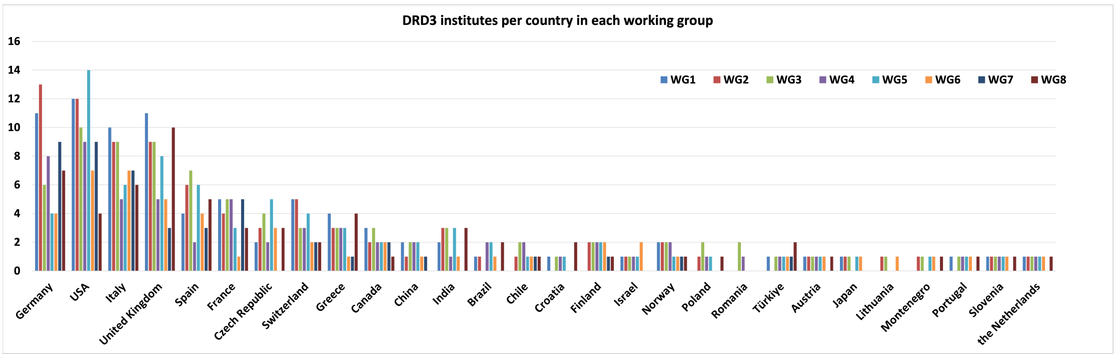


Figure 6: Number of institutes interested in each WG for each country.

2 WG1: Monolithic CMOS sensors

WG1 aims to advance the performance of monolithic CMOS sensors for future tracking applications, tackling the challenges of very high spatial resolution, high data rate, and high radiation tolerance while maintaining low mass, covering very large areas, reducing power, and keeping an affordable cost. WG1 will explore high-precision timing for applications such as Timing Layers and in full 4D tracking. It will also consider application in the electromagnetic section of a High Granularity Calorimeter. WG1 includes the design and experimental evaluation of fabricated sensors, and the development of suitable data acquisition systems. WG1 will benefit from synergies and common areas with other DRD3 WGs, and close collaboration with DRD7 for readout architectures and DRD8 for integration (DRD8 still to be formed).

2.1 WG1 Research Goals

The R&D program can be divided into three phases according to the timelines of the strategic programs: (i) the initial stepping stones developments of ALICE-3, LHCb-2, EIC, Belle-3, ATLAS, CMS, and HGCAL (DRD6); (ii) the subsequent further developments for e^+e^- colliders; (iii) and, lastly, the R&D for MC and FCC-hh. This proposal details the deliverables for the first R&D phase up to 2027 and highlights the R&D path from 2027 on. Several research goals (RG) and common areas (CA) are identified to be developed in available technology processes. The specification values below are expected to be significantly advanced or reached in at least one technology by the end of the first phase (<2027). The summary of the research goals is presented in Table 3.

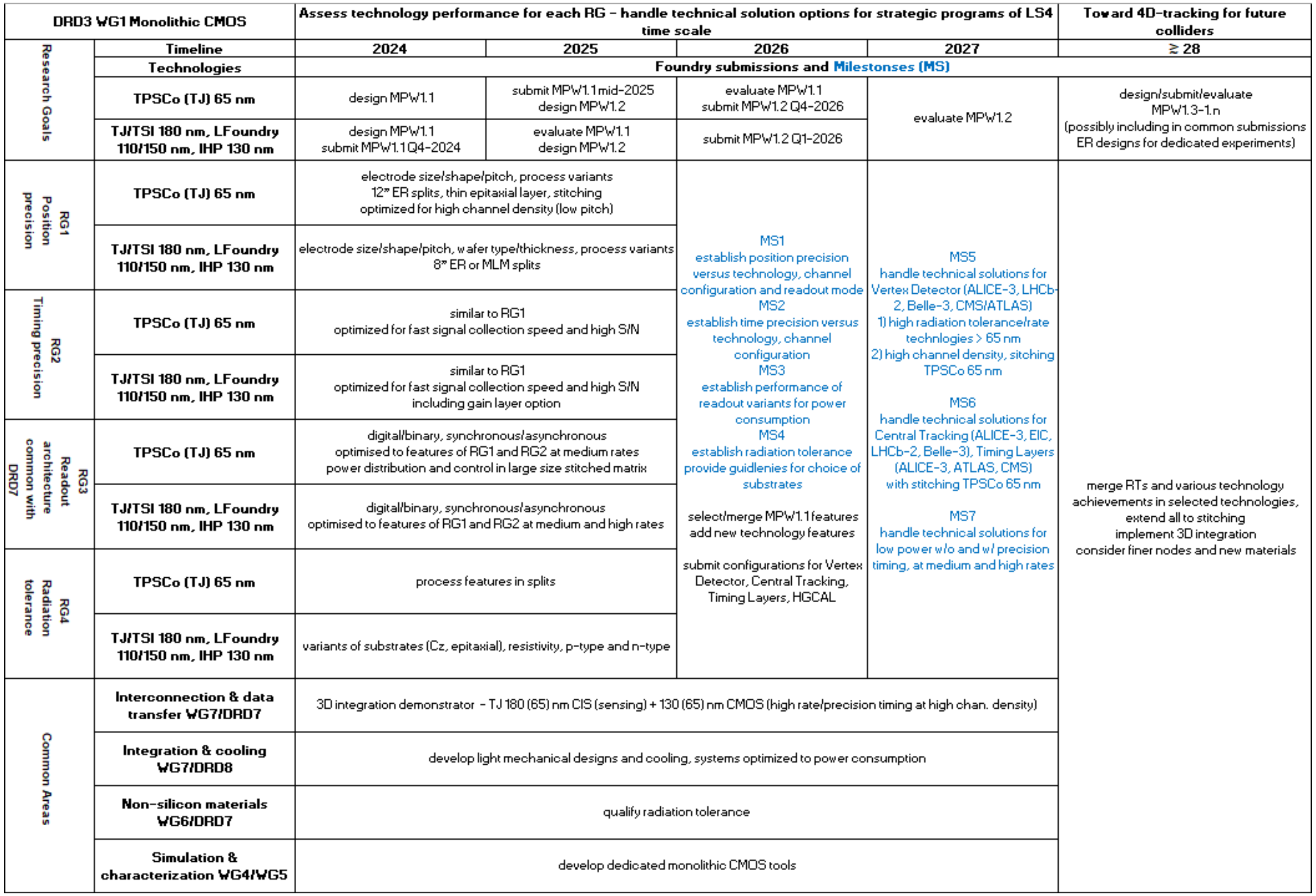
WG1 research goals <2027	
	Description
RG 1.1	Spatial resolution: ≤ 3 μm position resolution
RG 1.2	Timing resolution: towards 20 ps timing precision
RG 1.3	Readout architectures: towards 100 MHz/cm^2, 1 GHz/cm^2 with 3D stacked monolithic sensors, and on-chip reconfigurability
RG 1.4	Radiation tolerance: towards 10^{16} n_{eq}/cm^2 NIEL and 500 MRad

Table 3: WG1 research goals for < 2027

The list of common areas identified so far is the following:

- CA 1.1: Interconnection and data transfer;
- CA 1.2: Integration;
- CA 1.3: Non-silicon materials;
- CA 1.4: Simulation and characterisation.

The R&D deliverables are Multi-Project Wafer (MPW) submissions in different technologies and foundries as presented in Fig. 7. They cover four research goals to address the strategic program performance requirements outlined in the EFCA Detector R&D roadmap [2]. The MPW features and timeline are summarized in Fig. 7, while more details on the potential and complementarity of the various technologies are presented in the following section. Once the DRD3 collaboration is formed, the MPW details will be fine-tuned to ensure proper coverage of all the parameters. Developments in the common areas within DRD3 and with other DRDs will also be better defined. Particularly this can concern developments of complex readout architectures and first evaluation of the 3D integration of a sensitive CMOS chip with an independent digital chip in collaboration with DRD7.



DRD3 WG1 Monolithic CMOS		Assess technology performance for each RG – handle technical solution options for strategic programs of LS4 time scale				Toward 4D-tracking for future colliders
Research Goals	**Timeline**	**2024**	**2025**	**2026**	**2027**	**≥ 28**
	Technologies	**Foundry submissions and Milestonses (MS)**				
	TPSCo (TJ) 65 nm	design MPW1.1	submit MPW1.1 mid-2025 design MPW1.2	evaluate MPW1.1 submit MPW1.2 Q4-2026	evaluate MPW1.2	design/submit/evaluate MPW1.3-1.n (possibly including in common submissions ER designs for dedicated experiments)
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	design MPW1.1 submit MPW1.1 Q4-2024	evaluate MPW1.1 design MPW1.2	submit MPW1.2 Q1-2026		
RG1 Position precision	**TPSCo (TJ) 65 nm**	electrode size/shape/pitch, process variants 12" ER splits, thin epitaxial layer, stitching optimized for high channel density (low pitch)		MS1 establish position precision versus technology, channel configuration and readout mode MS2 establish time precision versus technology, channel configuration MS3 establish performance of readout variants for power consumption MS4 establish radiation tolerance provide guidlenies for choice of substrates select/merge MPW1.1 features add new technology features submit configurations for Vertex Detector, Central Tracking, Timing Layers, HGCAL	MS5 handle technical solutions for Vertex Detector (ALICE-3, LHCb-2, Belle-3, CMS/ATLAS) 1) high radiation tolerance/rate technlogies > 65 nm 2) high channel density, sitching TPSCo 65 nm MS6 handle technical solutions for Central Tracking (ALICE-3, EIC, LHCb-2, Belle-3), Timing Layers (ALICE-3, ATLAS, CMS) with stitching TPSCo 65 nm MS7 handle technical solutions for low power w/o and w/ precision timing, at medium and high rates	merge RTs and various technology achievements in selected technologies, extend all to stitching implement 3D integration consider finer nodes and new materials
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	electrode size/shape/pitch, wafer type/thickness, process variants 8" ER or MLM splits				
RG2 Timing precision	**TPSCo (TJ) 65 nm**	similar to RG1 optimized for fast signal collection speed and high S/N				
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	similar to RG1 optimized for fast signal collection speed and high S/N including gain layer option				
RG3 Readout architecture common with DRD7	**TPSCo (TJ) 65 nm**	digital/binary, synchronous/asynchronous optimised to features of RG1 and RG2 at medium rates power distribution and control in large size stitched matrix				
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	digital/binary, synchronous/asynchronous optimised to features of RG1 and RG2 at medium and high rates				
RG4 Radiation tolerance	**TPSCo (TJ) 65 nm**	process features in splits				
	TJ/TSI 180 nm, LFoundry 110/150 nm, IHP 130 nm	variants of substrates (Cz, epitaxial), resistivity, p-type and n-type				
Common Areas	**Interconnection & data transfer WG7/DRD7**	3D integration demonstrator – TJ 180 (65) nm CIS (sensing) + 130 (65) nm CMOS (high rate/precision timing at high chan. density)				
	Integration & cooling WG7/DRD8	develop light mechanical designs and cooling, systems optimized to power consumption				
	Non-silicon materials WG6/DRD7	qualify radiation tolerance				
	Simulation & characterization WG4/WG5	develop dedicated monolithic CMOS tools				

Figure 7: WG1 research goals and technology developments planning

2.2 Technology processes

The technology processes shortly introduced below complement one another in terms of features that are beneficial for the research goals of monolithic sensors in DRD3. All of the described technologies are accessible to the HEP community, usually through direct collaboration with institutes or through framework contracts with the foundries. The features available in these technologies are attractive for HEP detectors as their combination provides a complementary set of parameters to optimize the performance of future monolithic sensors:

- Wafer sizes of 200 mm and 300 mm;
- High resistivity bulk through high resistivity epitaxial and Czochralski substrates of p- and n-type;
- Processes with node sizes ranging from 65 nm to 180 nm and potential to optimize implant designs for charged particle detection (e.g. radiation hardness, timing resolution, etc.);
- Availability of MPWs and/or dedicated engineering runs with large reticles (in some cases, including options of reticle stitching or 3D stacking to logic wafers).

TPSCo 65 nm Developing the 65 nm technology to achieve the highest position precision in large-area sensors is an important goal. This technology uses an epitaxial layer, which is currently fixed at 10 μm. It features seven metal layers at this stage and the manufacturer offers engineering run submissions in 300 mm wafers. The stitching method to reproduce the reticle pattern (25 mm × 32 mm) can be used to allow large sensitive areas over a full wafer. Wafers can be thinned to much less than 50 μm. The small technology node allows the highest channel density achieved so far with pitches below 20 μm. Fully exploiting this high granularity potential will, however, need development of low-power readout coupled with a specific voltage distribution to cope with large active areas. The potential for a precise timing measurement will also be evaluated for the characteristic features of this technology. To further extend the ability to implement new functionalities and to increase the rate capability at high channel density, 3D stacking of the analog-sensitive component with a separate logic wafer will also be explored. Developments in the TPSCo 65 nm technology are recent and have been driven by the ALICE ITS3 project. A dedicated engineering run for ITS3 is foreseen in spring 2024. It will substantially advance the knowledge of the technology and also offer the possibility for few development chiplets developed by experts having contributed to the first submissions. In the first R&D phase proposed above, two engineering runs are currently planned, the first one around mid-2025, and the second early 2026. They will include the development of complex architectures, in collaboration with DRD7, that eventually could be ported to other technologies.

LFoundry 110 nm The LF11IS is an automotive-grade CMOS Image Sensor node offering a six aluminum layer (BEOL) stack. Access to fabrication is possible through regular MPW and Multi-Layer Mask (MLM) runs. The foundry allows for custom high-resistivity substrates on Front-Side Illuminated (FSI) and/or Back-Side Illuminated (BSI) process flows, including the possibility of using a dedicated maskset for backside lithography. While the maximum reticle size is 26 mm × 32 mm, the LF11IS technology has a stitching option. Based on this technology, sensors on active fully-depleted thicknesses ranging from 50 to 400 μm have been developed. The flexibility of the foundry process and product engineering teams allows exploring multiple wafer splits (n-epi thickness, n- or p-type starting substrate, substrate resistivity, implementation of a gain layer creating a monolithic LGAD, FSI or BSI process on different wafer thicknesses). In the framework of ARCADIA, INFN and LFoundry agreed on the terms to allow for the participation of third-party design groups to joint production runs. In this case, the third-party design group will be provided with regular access to the CMOS LF11IS iPDK (Interoperable Process Design Kit) for the implementation of proprietary architecture and sensor designs. Other than providing a library of signal samples for the chosen sensor geometry, INFN handles the sensor integration to the third-party design and final Design Rule Checking (DRC) of the design database during the preparation for the tapeout. This option enables a straightforward, low-risk, and very fast ramp-up of the R&D on sensors using LF11IS technology for new groups and design teams. This technology will develop 100 ps, 100 μm pixels (20-30 ps with additional gain layer). It will use n-epi active layer on p^+ substrate or high resistivity n-type substrate, thinned down to 100-400 μm.

IHP 130 nm The Silicon Germanium BiCMOS 130 nm process from IHP microelectronics combines state-of-the-art Heterojunction Bipolar Transistors (HBTs) performance and the advantages of a standard CMOS process. HBTs are ideal for high-performance timing applications thanks to their enhanced bandwidth and a better noise-power ratio than CMOS transistors. The process features a large n-well collection electrode that hosts the electronics. A nested p-well contains nMOS and PNP-HBT transistors. Isolation of the bulk of pMOS transistors from the collection n-well will be explored in future submissions. A small-scale demonstrator achieved a timing resolution of 20 ps at an analog power density of 2700 mW/cm^2 and 30 ps at 360 mW/cm^2. Preliminary radiation characterization shows good radiation tolerance. Sensors are implemented in high resistivity substrates up to 4 kΩ·cm and can be equipped with a Picosecond Avalanche Detector (PicoAD) gain layer for improved timing performance. The latest prototype with a 50 μm pixel pitch targets sub-10 ps timing resolution.

LFoundry 150 nm The LFoundry 150 nm process (LF15A) is a mixed digital/high-performance analog, high-voltage CMOS technology node. It features up to six layers of aluminum interconnection, with the possibility of an additional thick layer of top metal, particularly suited to efficiently route power lines to large pixel matrices. This process includes as well a deep p-well layer, which is useful for embedding digital logic inside the collecting electrode. The foundry offers standard and high-resistivity wafers, and has shown to be open to process modifications. There are typically two MPW shuttle runs organized per year. MLM engineering runs are also possible and can be particularly cost-effective for joint submissions handled by several teams. The LF15A technology has been successfully used in the past years for tracking based CMOS demonstrators (e.g. LF-CPIX, LF-MONOPIX chips, and RD50-MPW chips) and for non-amplified

CMOS timing sensor concepts with performance better than 100 ps (CACTUS chips). Characterization of irradiated samples has shown the technology to be radiation tolerant up to dose levels suitable for the innermost layers of tracking detectors at the HL-LHC. The community is currently negotiating a framework agreement with this foundry to produce a certain number of submissions over a fixed period, taking advantage of special conditions and potentially lower production costs. This technology will develop fully depleted 50-250 μm thin sensors, with <25 μm pixels and use >2 kΩ·cm high resistivity substrates. It will also explore 30 ps/MIP timing with 250 μm pixels.

TSI 180 nm The TSI Semiconductors 180 nm is a high-voltage CMOS technology. As part of its standard layer stack, it has a deep n-well, typically used to host low-voltage readout electronics while isolating them from the high-voltage substrate. It also has a deep p-well that integrates digital readout electronics within the deep n-well. It features a total of seven metal layers. TCAD models are available. Fabrication on high-resistivity substrates is possible, and the foundry can manufacture designs on wafers provided by the customer. Stitching is possible too. The maximum reticle size is 2.1 cm × 2.3 cm. High-voltage CMOS sensors in this technology have demonstrated a time resolution of 2.4 ns at low noise rates and shown an excellent performance concerning efficiency and noise even after irradiation with protons and neutrons with fluence up to 2×10^{15} $\mathrm{n_{eq}/cm^2}$. The smallest pixel pitch demonstrated so far is 25 μm. Submissions to this foundry are engineering runs, although wafer sharing is possible. TSI 180 nm is the technology for the pixel tracker of the Mu3e experiment (MuPix), and LHCb is considering it for the proposed Mighty Tracker upgrade (MightyPix). Sensors in this technology have been thinned down to 50 and 70 μm, and demonstrated to work efficiently in the framework of the Mu3e experiment (50 μm for the vertex layers, and 70 μm for the outer tracker layers). This technology has been used to develop prototypes and final sensors for several other particle physics applications (e.g. CLICpix, ATLASpix), for test beam instrumentation (e.g. TelePix), and for applications in space (e.g. AstroPix). The TSI process is layout compatible with the aH18 process of ams-osram.

TowerJazz 180 nm The Tower Semiconductor 180 nm CMOS imaging process is well-established in the HEP community. It provides cost-effective manufacturing and prototyping on 200 mm wafers. It features six metal layers plus the possibility for a final thick metal layer that can be used to facilitate signal and power distribution. The process includes deep p-wells to allow full CMOS functionality to embed digital and analog electronics side-by-side in the pixel. The foundry offers to produce on foundry-supplied and customer-supplied (after approval) wafer stock. Sensors have been successfully produced on epitaxial (up to 30 μm thickness) and high-resistivity Czochralski substrates, with a typical device thickness of 100 μm although the community has experience also with 50 μm and 300 μm devices. Through close collaboration with the foundry, the implantation profiles can be optimized for specific sensor needs, which has been done successfully to achieve high radiation hardness. The possibility to combine different implants in the pixel and optimize implantation profiles together with Tower engineers will be an essential means to develop optimized sensors for radiation hardness and timing capabilities. Prototyping takes advantage of regularly offered MPWs (up to four yearly shuttle runs). Also, MPW runs allow process modifications in individual layers related to charge collection. This process has been successfully used recently for a large family of small-electrode monolithic CMOS sensors ranging from ALPIDE and MIMOSIS sensors to radiation hard sensors like TJMonoPix and MALTA. With a reticle size of 30 mm × 25 mm, it provides sufficient space to prototype multiple sensors in a single engineering run for maximum processing flexibility and cost-effective prototyping.

3D stacking option Recently Tower Semiconductor and its European representative company Etesian have advertised the possibility of using waferstacking of the 180 nm CMOS Image Sensors (CIS) to its 130 nm mixed signal CMOS. The foundry performs the stacking, and it is offered to customers through a PDK. The 3D stacked 180 nm CIS + 130 nm CMOS is also accessible through regular MPWs organized by the foundry. This 3D stacked technology promises the potential for HEP sensors as 3D-stacked monolithic sensors with an optimized sensor layer and a 130 nm signal processing layer for more complex logic as required for high-rate and timing applications. The radiation tolerance is expected to be the same as that of the individual processes. This technology will develop 3D stacking, timing through different geometries with/without internal gain, and on-sensor time-stamping. It will use different resistivity substrates to expand to high radiation tolerance. Knowledge obtained in a medium node size (180 nm, 130 nm) provides cost-effective information on 3D integration that can be transferred to the 65 nm 3D stacked CIS + CMOS also offered by Tower.

3 WG2: Sensors for tracking and calorimetry

WG2 aims to advance the performance of sensors for 4D tracking, and it is aligned with the goals of DRDT2. The scope of WG2 is quite broad, as it addresses the R&D of sensors for very different environments: vertex or tracker, low/high radiation, low/high occupancy, low/high power, and low/high material budget. Presently, sensors with 4D capabilities are foreseen in many systems, from Time-of-Flight systems with only 1-2 layers of sensors with the best possible resolution to large 4D trackers with many layers. In this latter case, if the temporal resolution is good enough, recognition algorithms can use four coordinates in the reconstruction, simplifying the pattern recognition. Broadly speaking, the challenges at Hadron colliders are mostly linked to radiation levels (mainly in the vertex detector) and high occupancy. In contrast, at lepton colliders, the challenges are related to material budget and low power consumption.

It is noted that the various developments comprise studies on the sensor production techniques including e.g. passive CMOS sensor technologies.

3.1 Spatial and temporal resolutions at extreme radiation levels

For this R&D, the new innermost layers of ATLAS/CMS and the LHCb velo pixel systems are used as stepping stones for the formidable developments needed for FCC-hh. Due to their short drift path and low depletion voltage, 3D sensors are strong candidates for these upgrades.

- **RG 2.1 Reduction of pixel cell size for 3D sensors.**
  - 2024-2025: 3D sensors test structures with pixel size smaller than the current $50 \times 50\ \mu m^2$ or $25 \times 100\ \mu m^2$
  - 2026-2028: Large size 3D sensors with reduced pixel size.
- **RG 2.2: 3D sensors with a temporal resolution of about 50 ps.**
  - 2024-2025: Production of a small matrix with pitch $42 \times 42\ \mu m^2$ or $55 \times 55\ \mu m^2$ to be connected with existing read-out ASICS
  - 2026-2028: Production of large-size sensors (using the selected geometry from the R&D runs) and interconnection with custom-made read-out ASIC

3.2 Spatial and temporal resolutions at low radiation levels and low material and power budgets

Future upgrades beyond LHC phase-II might seek to introduce 4D layers at moderate radiation levels (1 - 3 $\cdot 10^{15}$ $\mathrm{n_{eq}/cm^2}$), with a spatial resolution of about 10 - 30 μm. Sensors for lepton colliders require a very low material budget and minimal power consumption. Presently, sensors with moderate values of internal gain, the so-called Low-Gain Avalance Diodes (LGAD), are the most promising candidates. In fact, low gain allows for an increased signal size while keeping the noise constant, an important feature in timing applications. Low gain is also important for applications that require a low material budget as the sensor can be very thin, and the power of the electronics can be reduced since the "first amplification stage" is contained in the sensor itself. The LGAD design can be employed also in the MAPS design.

- **RG 2.3: LGAD Sensors with very high fill factor, and an excellent spatial and temporal resolution.**
  - 2024-2025: LGAD test structures of different technologies (TI-LGAD, iLGAD, RSD, DJ-LGAD), matching existing read-out ASICs.
  - 2026-2028: Large LGAD sensors based on the best-performing technology.
- **RG 2.4: LGAD sensors for Time of Flight applications**
  - 2024-2026: Production of LGAD (RSD) sensors with large size for Tracking/Time of Flight applications to demonstrate yield and doping homogeneity. Study of spatial and temporal resolutions as a function of the pixel size.
  - 2026-2028: Structures produced with vendors capable of large-area productions to demonstrate the industrialization of the process.

3.3 WG2 Research Goals

Table 4 list the WG2 research goals.

WG2 research goals <2027	
	Description
RG 2.1	Reduction of pixel cell size for 3D sensors
RG 2.2	3D sensors for timing (50 × 50 μm, $<$ 50 ps)
RG 2.3	LGAD for 4D tracking $<$ 10 μm, $<$ 30 ps, wafer 6" and 8"
RG 2.4	RSD for ToF (Large area, $<$ 30 μm, $<$ 30 ps)

Table 4: WG2 research goals for $<$ 2027

4 WG3: Radiation damage and extreme fluence operation

This WG aims to provide a fundamental scientific understanding of radiation damage processes in solid-state detectors and detector materials at low, high, and extreme radiation levels of up to 5×10^{18} cm^{-2} and 5000 MGy, as anticipated for the forward calorimeters in the FCC-hh after an integrated luminosity of 30 ab^{-1}. The existing and newly generated knowledge will be used to optimize the radiation tolerance of the various detector types under development within the collaboration through defect and material engineering, device engineering, and optimization of operational conditions. The work is organized in two areas. The first is the study of the radiation damage mechanisms in detector materials, including the formation of microscopic defects and their impact on device performance; the second is the study and modeling of radiation damage to devices. In both areas, the full range from very low to high fluences and finally up to extreme fluences beyond 2×10^{16} cm^{-2} has to be covered. The latter work covers the Roadmap DRDT 3.3. on extreme fluence operation, while WG3 reaches deeply into all four Roadmap DRDTs for solid-state detectors wherever radiation damage is of concern.

4.1 Radiation damage and hardening studies at material level

Understanding radiation damage at the microscopic level and the consequences on materials and device properties is a necessary prerequisite for efficient and successful detector development. Comprehensive investigations of defects generated in irradiated sensors providing accurate evaluations of defect concentrations and trapping parameters can be achieved by employing specific spectroscopic techniques based on capacitance or current measurements (e.g. DLTS, TSC, TSCap). Such methods have been successfully applied on fabricated silicon sensors up to fluences of about 10^{15} $\mathrm{n_{eq}/cm^2}$. They provide both the characteristics of radiation-induced defects that are also fundamental input parameters to sensor performance simulations under various conditions and knowledge for developing material and defect engineering strategies. As the extrapolation of damage parameters to higher fluences has proven to be too pessimistic, and the defect formation process is not a linear function of fluence, further characterization work at higher fluences is essential but exceeds the range of applicability of present experimental characterization methods. Therefore, the understanding of the radiation damage at extreme fluences requires, in addition, comprehensive modeling of defect generation, including the higher order radiation-induced defects, and the employment of other techniques suitable for detecting defects in large concentrations, i.e., above 10^{16} cm^{-3}, such as EPR, FTIR, XRD, Raman, and PL. Even more demanding is the understanding of radiation damage in wide band gap (WBG) and other materials where presently, compared with silicon, significantly less knowledge exists. In addition, the changes of the fundamental semiconductor properties (e.g., carrier mobilities, carrier lifetime) at extreme fluences are very poorly known, although they are needed for any detector design work. These challenges will be addressed in the years to come, starting with developing the defect-engineered strategies for obtaining detailed and precise electrical characterization of point and cluster defects generated by irradiations up to fluences of 10^{16} $\mathrm{n_{eq}/cm^2}$ by means of DLTS, TSC, and

TSCap techniques. Highly irradiated devices (above 10^{17} $\mathrm{n_{eq}/cm^2}$) will start to be investigated by EPR, FTIR, XRD, Raman and PL, to provide the needed information about the chemical structure of radiation-induced defects and their introduction rates, to be used in developing a realistic radiation model up to extreme radiation fluences. The change in the carrier lifetime and mobility will be evaluated from carrier lifetime and Hall effect measurements.

4.2 Radiation damage and hardening studies at device and system levels

The detector community will need a wide variety of radiation damage studies in the near and long term. Tracking and timing detectors, including, for example, several configurations of LGAD and 3D sensors, are already aimed at the earliest LHC upgrades. These will continue to need regular irradiations with various particle species up to approximately 5×10^{16} $\mathrm{n_{eq}/cm^2}$. Technology development in new directions will also need radiation testing and radiation damage modeling; this includes large area and thick silicon devices, applications for the LHCb and ALICE upgrades, the Electron-Ion Collider, and space-based detectors. New efforts in high-granularity calorimetry and quantum-imaging detectors are already seeking characterization within radiation contexts. Devices proposed for later upgrades need radiation damage studies in the near term too, for evaluation of monolithic CMOS and ASICs. Within the community, there are already calls for facilities able to provide up to 10^{18} $\mathrm{n_{eq}/cm^2}$, with multiple beam energies and species. TCAD and GEANT4 simulations are underway for new structures and require validation with data. Data are urgently needed from TCT instruments and testbeams, combined with dedicated data collected by the LHC experiments for leakage current and depletion.

New sensor materials are under exploration, requiring either new or extended parameterized models of their radiation damage response. These include all materials studied in WG 6, particularly the wide bandgap semiconductors, which may benefit from reduced cooling requirements. Radiation studies are also needed for new vertical and heterogeneous integration techniques that are directly connected to materials improvements. The foundational research toward understanding how fundamental material properties, such as mobility, effective dopant concentrations, and carrier lifetimes, must also continue and reach a more solid standing. The semiconductor detector community needs to understand the validity limit of the current models (e.g., Hamburg Model) and understand where the presently used non-ionizing energy loss (NIEL) hypothesis fails to determine the best directions in defect and device engineering. New sensor materials are under exploration, requiring either new or extended parameterized models of their radiation damage response. These include all materials studied in WG 6, particularly the wide bandgap semiconductors, which may benefit from reduced cooling requirements. Radiation studies are also needed for new vertical and heterogeneous integration techniques that are directly connected to materials improvements. The foundational research toward understanding how fundamental material properties, such as mobility, effective dopant concentrations, and carrier lifetimes, must also continue and reach a more solid standing. The semiconductor detector community needs to understand the validity limit of the current models (e.g., Hamburg Model) and understand where the presently used non-ionizing energy loss (NIEL) hypothesis fails to determine the best directions in defect and device engineering. New sensor materials are under exploration, requiring either new or extended parameterized models of their radiation damage response. These include all materials studied in WG 6, particularly the wide bandgap semiconductors, which may benefit from reduced cooling requirements. Radiation studies are also needed for new vertical and heterogeneous integration techniques that are directly connected to materials improvements. The foundational research toward understanding how fundamental material properties, such as mobility, effective dopant concentrations, and carrier lifetimes, change with irradiation must also continue and reach a more solid standing. The semiconductor detector community needs to understand the validity limit of the current models (e.g., Hamburg Model) and understand where the presently used non-ionizing energy loss (NIEL) hypothesis fails to determine the best directions in defect and device engineering. We do not lose sight of the fact that technology transfer beyond High Energy Physics, for example, medical imaging, dosimetry, nuclear safety, and security, requires rigorous radiation validation.

The present community for developing radiation-tolerant semiconductor detectors includes many institutes comprising university groups and national laboratories. Regular training is being offered at nearly all of them to expand the community and develop expert junior researchers. Milestones to be achieved in the next three years include (i) improved or new models for new materials and extreme radiation conditions; (ii) a transfer of information from models to simulations; and (iii) sufficient irradiation facilities and test beam support for this diverse program. Critical infrastructures on the timescale of six years are the reliable availability of facilities providing integrated fluence on the order of 10^{18} $\mathrm{n_{eq}/cm^2}$, in both charged and neutral species.

4.3 WG3 Reasearch Goals

The research goals of WG3 are summarized in Table 5.

WG3 research goals <2027	
	Description
RG 3.1	Build up data sets on radiation-induced defect formation in WBG materials
RG 3.2	Develop silicon radiation damage models based on measured point and cluster defects
RG 3.3	Provide measurements and detector radiation damage models for radiation levels faced in HL-LHC operation
RG 3.4	Measure and model the properties of silicon and WBG sensors in the fluence range 10^{16} to $10^{18}\mathrm{n_{eq}cm^{-2}}$

Table 5: WG3 Research goals for < 2027

5 WG4: Simulation

The simulation work will be dedicated to the development of common simulation packages, tools, and radiation models. There will be two lines of activities that will be pursued: TCAD tools and so-called MC tools. While the former is commonly used in sensor design, process simulation, and radiation damage modeling the latter are extensively tested in sensor performance evaluation (with particle and Transient Current technique) benefiting from much faster code and integration of other software packages e.g. GEANT4.

Another important activity in WG4 will be the continuation of radiation hardness modeling, bulk, and surface, starting from the defect level using mainly TCAD, but also MC tools. Radiation hardness models for WBS will be explored and developed.

The WG4 will be an important part of many Work Packages: it will contribute to the simulations of sensor development and performance in WG1 and WG2, it will collaborate with WG3 to incorporate in the simulation the latest understanding of radiation damage, it will be used to optimize the developments of common tools(WG5), and will ease the use of WBS (WG6) by incorporating their properties in the simulation package.

5.1 Activities

The following activities are foreseen in the WG4

- TCAD activities will focus on providing verification of tools (mainly Silvaco and Synopsys, but also looking to other tools emerging) implementation of new physics models (impact ionization, mobility parametrization etc.), exporting tools, communication with software companies (e.g. implementation of WGS) and keeping the implementation of common solutions to device simulations.

- TCAD simulations will be complemented with charge transport simulation tools - Monte Carlo tools - allowing detailed studies of complex sensor performance. Different tools have been developed so far, but currently, the most supported and advanced tool is Allpix Squared, which will form the main/production framework, while other tools will continue to be used as verification and development tools. It is foreseen that improvements in MC simulations will eventually be integrated into AllPix2. The biggest obstacle for Monte-Carlo tools is currently the lack of implementing adaptive/time-dependent weighting and electric fields in induced current simulations.

- Modeling of the radiation damage in simulations has been evolving over the last two decades, but there is not a general model that, starting from the defect levels, comprehensively describes all the macroscopic properties of silicon. This is even more so at extreme fluences (WG3).

- Development of signal processing tools that can be used with MC and TCAD tools and general digitization models for different sensors technologies,

5.2 WG4 Research Goals

The research goals of WG4 are summarized in Table 6.

WG4 research goals <2027	
	Description
RG 4.1	Flexible CMOS simulation of 65 nm to test design variations
RG 4.2	Implementation of newly measured semiconductor properties into TCAD and MC simulations tools
RG 4.3	Definition of benchmark for validating the radiation damage models with measurements and different benchmark models.
RG 4.4	Developing of bulk and surface model for $10^{16}\text{cm}^{-2} < \Phi_{eq} < 10^{17}\ \text{cm}^{-2}$
RG 4.5	Collate solutions from different MC tools and develop an algorithm to include adaptive electric and weighting fields

Table 6: WG4 Research goals for < 2027.

6 WG5: Techniques, infrastructures and facilities for sensors characterisation

WG5 involves the establishment of a community-driven working group that focuses on the development, improvement, and dissemination of methods and techniques for characterizing sensors. By bringing together experts and leveraging collective resources, the working group aims to foster collaboration, knowledge sharing, and innovation in the field of sensor characterization within the particle physics community.

This working group operates across different Detector R&D Themes (DRDT) along three activity lines:

- Actively engage in the development, improvement, and diffusion of cutting-edge methods and techniques for sensor characterization. This involves exploring novel approaches and refining existing methodologies to assess and understand the performance and behaviour of sensors.
- The working group facilitates sharing of knowledge, resources, and expertise among participating researchers and institutions by identifying common infrastructures for sensor testing and fostering joint research activities. These collaborative endeavours aim to develop and deliver state-of-the-art infrastructures, as the Caribou data acquisition system, specifically designed for the comprehensive testing and evaluation of sensors.
- Promoting the use of unique characterization facilities. These facilities may possess rare capabilities, specialized equipment, or specific expertise in sensor characterization. The project seeks to raise awareness and encourage researchers to leverage these facilities to explore advanced characterization methods. The project aims to foster collaboration between researchers and these facilities, facilitating access to specialized resources.

6.1 Working group implementation

The working group implements two types of activities to fulfill its objectives. Firstly, there are joint research activities that involve the creation or improvement of new testing methods or testing infrastructures. These activities are structured as dedicated work packages with specific research goals and are time-limited. They address specific R&D projects, such as the development of techniques like TPA-TCT or defect spectroscopy methods.

Secondly, the working group engages in networking activities aimed at coordinating access to unique testing infrastructures. These infrastructures may include high-energy or high-intensity beams, micro-beam TRIBIC facilities, and EMC assessment laboratories, among others. The focus of these activities is to increase awareness among researchers about the availability of these facilities for sensor characterization. Additionally, the working group organizes dedicated workshops to provide training on different sensor characterization techniques. These workshops serve to educate researchers on the use of new and existing characterization methods and will be organized with the help of WG8.

6.2 WG5 Research Goals

The research goals of WG5 are summarized in Table 7.

WG5 research goals <2027	
	Description
RG 5.1	Develop TPA-TCT
RG 5.2	Common infrastructure
RG 5.3	Networking and training on methods

Table 7: WG5 research goals for < 2027.

7 WG6: Wide bandgap and innovative sensor materials

Wide band-gap (WBG) semiconductors have some attractive properties and also some associated problems.

Whilst a wide bandgap reduces the leakage current, maintaining low noise levels even at high temperatures, it also increases the electron-hole generation energy. This increase implies that the number of electron-hole pairs generated for the same deposited energy is lower in WBG materials.

However, the substantial reduction of the noise level ensures that the overall signal-to-noise ratio (SNR) for WBG-based detectors is high enough, even after irradiation. In addition, the high breakdown field allows operation at high internal electric fields, minimizing the carrier transit time and the trapping probability.

Other innovative semiconductors, such as 2D materials, require investigation. However, their current level of development for use in experiments is still relatively low. As a result, a Blue-sky funding scheme should be applied to support further research in these areas.

WG6 is well aligned with the DRDT3.2 and DRDT3.3 since WBG semiconductors can be used for timing applications due to the high carrier saturation velocity, and their radiation hardness make them suitable materials to be used at extreme fluences with the added advantage that they can be operated without cooling.

7.1 Diamond

The high energy physics community has extensively studied diamond as a wide band-gap semiconductor material for sensors; experiments, and accelerators have used diamond-based beam conditions monitors successfully for decades. A polycrystalline synthetic diamond (pCVDD) with a wafer charge-collection-distance (CCD) of 400 microns is available today, and the aim is to increase the quality to 500 microns and improve wafer uniformity. Diamond detectors have been tested for radiation hardness and can withstand protons, neutrons, and pions at various energies. However, at a fluence of 10^{17} cm^{-2} 24 GeV protons, the Schubweg or average distance a carrier traverses before being captured is approximately 16 microns, resulting in a significant reduction in signal efficiency. 3D diamond detectors with a femtosecond laser process to convert diamonds into graphite electrodes can address this problem. The first 3D diamond detector device is planned for use in the ATLAS Phase-II upgrade as a small beam condition monitor, and it represents a stepping stone towards larger area applications needed for future projects like the FCC-hh. Further studies and innovative geometries are needed to comprehensively assess 3D diamond detectors' radiation tolerance. This includes studies of charge multiplication via impact ionization through adapted electrode geometries to improve radiation tolerance and timing performance.

7.2 Wide-band semiconductor

SiC Recently, the use of SiC in power devices has become widespread, and the quality of this material has reached levels comparable to that of silicon. Additionally, 150mm SiC wafers have become standard in the semiconductor industry, and soon 200mm wafers will be introduced to the market. The high-quality material required for SiC sensors is typically epitaxially grown using Chemical Vapour Deposition (CVD), which allows for precise control of crystal film thickness, doping, and homogeneity. Recently, SiC epitaxial layers up to a thickness of 200 μm have been obtained. However, the material's resistivity must be increased to deplete these layers with reasonable bias voltages. Alternatively, MIP detection in thin layers with reasonable SNR would need signal amplification in the material.

In the mid-term, SiC could be used as beam loss and intensity monitors, as well as in medical applications like (micro-)dosimetry and neutron/plasma detection in high-temperature environments.

In the coming years, the main technological challenges for SiC detectors will involve studying the radiation hardness of high-quality materials and understanding the defect traps. This will aid in fabricating more radiation-hard materials and developing reliable simulation tools necessary for designing new detectors and predicting their performance in extreme fluence environments. Recent studies have shown that SiC detectors have better timing performance than silicon detectors, necessitating further research to explore the possibility of including a gain layer into the bulk as done for the standard LGAD. A multiplication mechanism in SiC diodes has been observed after neutron irradiation, but it is not yet understood.

GaN is the most rapidly growing semiconductor material used in industrial applications such as telecommunications, power management, high-temperature operation, optoelectronics, and aerospace. However, defects in the GaN crystal, such as dislocations and unintentional doping, still present a challenge in terms of device-level performance. In the past decade and due to the rapid improvement of material quality of epitaxially grown films, the promise of GaN as a detector material has been demonstrated by several groups. Nevertheless, the widespread use of GaN devices in higher radiation environments (HL-LHC and beyond) will require development to improve their radiation hardness, which in turn requires a thorough understanding of the displacement damage and resulting material defects in GaN, and designing devices using predictive models calibrated to irradiated GaN on native substrates and on SiC. This aligns well with developments in the industry where material quality is perceived as the key to the development of fast RF devices with sub-ns resolution (5G and beyond) and monolithic designs of GaN embedded in Si or SiC substrates for fast power switching and nuclear technology applications.

7.3 WG6 Research Goals

The research goals of WG6 are summarized in Table 8.

WG6 research goals <2027	
	Description
RG 6.1	3D diamond detectors, cages / interconnects, base length 25 μm , impact ionization
RG 6.2	Fabrication of large area SiC and GaN detectors, improve material quality and reduce defect levels.
RG 6.3	Improve tracking capabilities of WBG materials
RG 6.4	Apply graphene and/or other 2D materials in radiation detectors, understand signal formation.

Table 8: WG6 research goals for < 2027

8 WG7: Sensor interconnection techniques

Interconnections are one of the critical aspects of future detector and electronics evolution. They have a fundamental role for integrating the sensor and readout ASICs, and in constructing multi-tier electronics. Interconnection technologies enter at different stages of detector construction: from the fast hybridization necessary for the qualification of prototypes to the reliable flip-chip of modules and they need to assure reliable operation for years under stringent radiation, thermal and mechanical specifications. Special interconnections are also key to resolving specific problems, for example in terms of pitch or mechanical/electrical properties.

The goal of the DRD3 interconnection task is to organize the different technological readiness levels of interconnection solutions and the effort towards future advances in the field to match the requirements of future detectors in a coherent and coordinated way.

Very late during the editorial activity of this Research Proposal, it was suggested to add some Mechanics and Advanced Cooling R&D to the interconnection WG. Due to the timing of the request, it was impossible to integrate this in the present document, which will happen in later versions after a discussion with interested institutes in the community. This prospective has anyway been included in the Mapping Tables 11, 12, 13.

8.1 Maskless interconnections: anisotropic conductive films or pastes (ACF, ACP)

Small-pitch hybrid pixel detectors produced with solder bump-bonding techniques are widely used in current and future HEP experiments. The cost of the complex metallization and interconnect processing, performed in highly specialized foundries, dominates the production cost per unit area, and the need to process whole readout wafers dominates the prototyping costs. In addition, this introduces a long turnaround time during the prototyping phase, where several submissions are made and usually a limited number of devices are used for the test. The DRD3 interconnection working package studies technological alternatives to the standard flip-chip techniques to develop fast, possibly in-house, connection processes able to be used for fast testing of new productions, and possibly at the device level. The advantage of avoiding specialized hybridization vendors translates into significant savings of time and money.

Interconnection of large-pitch hybrid pixel detectors is also very important. The technologies used in small-pitch interconnection are an overkill in this case, driving to an increase of cost and complexity. Development of a fast, cheap and reliable interconnection process can be very beneficial for these applications.

Anisotropic Conductive Films (ACF) and Anisotropic Conductive Pastes (ACP) are interconnection technologies based on microscopic conductive particles suspended in an adhesive medium, a film, or a paste. Thermocompression of the ACF/ACP between two conductors results in a permanent attachment and a reliable electrical connection only in the direction of the compression. ACF is the dominating interconnect technology for displays (LCD and OLED) and is widely used also in e.g. camera modules and RFID manufacturing. For the application of HEP pixel detectors, critical parameters such as bonding force, adhesive film thickness, particle material, diameter, and density of particles need to be developed for the specific layout and topology of the respective sensors and readout ASICs. One of the main advantages of these technologies is that they may not require lithographic masks for deposition, are affordable, and can be performed in-house by many laboratories. Processing can happen both at die-to-die and die-to-wafer levels.

Additional advanced interconnect technologies such as nano-wires or additive micro-structured ink-jet printing will be investigated for specific applications as possible alternatives to conductive adhesives. This study needs to be complemented with an investigation of the radiation resistance of these new technologies.

Relevant short-term (3 years) research goals in this development are (i) consolidate the connection yield necessary for tracking detectors applications; (ii) demonstrate a process optimization that could satisfy pixel pitch of the order of $30\mu m$ or below. In the mid-term (3-6 years), the main research goals are to test and verify (i) the radiation hardness of the process to fluences and doses typical of future experiments at colliders and (ii) the reliability of the technology under the thermal and mechanical specifications determined by the above applications.

8.2 Improvement and diffusion of classical interconnection technologies

Classical interconnection techniques provided to High Energy Physics Experiments by commercial vendors and RTOs are nowadays reaching the necessary standards in terms of yields and typical technical specifications but remain expensive and time-consuming processes. The construction of the LHC upgraded trackers for High Luminosity coming in parallel for several detectors on the same timescale also showed that the production capacity of most of these vendors can be easily saturated. Progress can be achieved following two directions. The first is to make the most common interconnection techniques affordable to existing infrastructure in home laboratories. This can be achieved, for instance, with the introduction of maskless processes. The second is to organize and sponsor the development of advanced processes and the cooperation of commercial vendors and academic groups to address specific complex issues: for example, the need for smaller pixel pitches, the resolution of process temperature constraints, the electrical properties of interconnections in terms of maximum current or capacitance, or the technique used by industry in the interconnection (die-to-die or die-to-wafer).

In the short-term, research goals are the development of maskless post-processing for some of the most standard technologies. In the mid-term, (i) the most standard technologies should be available in full or in part inside specialized academic laboratories and (ii) a device-to-wafer approach to favour the multi project wafer (MPW) submissions, where only a small part of each production wafer is used by a collaboration.

8.3 3D and vertical integration for High Energy Physics silicon detectors

3D and vertical integration are technologies already largely used in electronics. They are available via industry, and in this way, they profit from the commercial drive coming from consumer electronics. The use in High Energy Physics experiments has already been probed to some extent to merge - for instance - tiers in different technologies. A typical example is a digital layer connected to an analog tier built in a different process. Vertical integration might also have a fundamental role in the integration of different devices which need to be interconnected and that in today's detectors are exchanging data via external solutions such as flexible circuits. The vertical stacking can also allow to contact / power / read a lower tier through an intermediate one with the use, for instance, of specific vias. The interconnection Work Package of DRD3 should coordinate the access to specific industrial processes for laboratories involved in High Energy Physics detectors. While single groups might still be able to deal with secondary industrial actors in the field of vertical integration, the mediation of DRD3 will have a larger chance of success for the involvement of big industrial players, granting continuity and resources. Research goals for the short-term are (i) the demonstration of wafer-to-wafer process in front-end to sensor connection; (ii) the demonstration of the use of TSV to pass power or data through sensors or front-end layers. For the mid- and long-term, the goal is to demonstrate the interconnection capability for post-processed devices.

8.4 WG7 Research Goals

WG7 research goals <2027	
	Description
RG 7.1	Yield consolidation for fast interconnections
RG 7.2	Demonstration of in-house process for single dies and pixel interconnections for a range of pitches (down to $< 30\mu m$)
RG 7.3	Development of maskless post-processing for classical bump-like interconnection technologies
RG 7.4	Development of wafer-to-wafer in presently advanced interconnection technologies
RG 7.5	Development of VIAS in multi-tier sensor/front-end assemblies

Table 9: WG7 Research Goals for < 2027

9 WG8: Outreach and dissemination

WG8 aims at promoting outreach and disseminating the activities of the DRD3 collaboration in coordination with other similar international and ECFA activities.

The WG8 activities can be broadly divided into:

- Disseminating knowledge on solid-state detectors to people working in high-energy physics (training, lectures, mobility)
- Disseminating knowledge on solid-state detectors to high-school students and the general public.

9.1 Disseminating knowledge on solid-state detectors to people working in high-energy physics

These activities aim to provide training and disseminate the experimental techniques needed in DRD3 activities.

- Organize schools for Ph.D. students and young post-docs on TCAD, FPGA programming, GEANT, AllPix2, SIMDET.
- Organize stages for undergraduate students and promote exchange programs between labs. Financial support might be offered
- Participation in instrumentation schools, offering lectures on DRD3 topics (for example, the CERN or FNAL schools)
- Share knowledge of measurement techniques such as device characterizations using IV, CV characteristics, transient studies using TCT, detector telescopes built using beta sources, handling and measurements of irradiated sensors
- Present DRD3 work at conferences, providing opportunities for young researchers to be speakers at important international conferences.
- Publish papers and proceedings so that the DRD3 activities are documented in printed papers.

One exciting aspect is to create partnerships between established and new laboratories so that the upcoming groups can profit from the accumulated knowledge of the more experienced groups.

The DRD3 website will be the point of entry to advertise all DRD3 activities. It will contain links to the DRDs meetings; it will list opportunities for conferences, stages, and so on. It will also collect documentation on how to perform the various experimental techniques.

9.2 Disseminating knowledge on solid-state detectors to high-school students and the general public

Many of the DRD3 members are engaged in outreach activities at various levels, such as high-school seminars, hands-on experiments for young students, and community meetings. WG8 aims to collect materials and suggestions for these activities so that it will be easier for new members to carry on the same activities in new places.

9.3 WG8 Research Goals

The research goals of WG8 are summarized in Table 10.

WG8 research goals <2027	
	Description
RG 8.1	Design and set-up of the DRD3 web site
RG 8.2	Collection of the outreach material
RG 8.3	Set-up and organize schools and exchange programs
RG 8.4	Set-up of the DRD3 conference committee

Table 10: WG8 research goals for < 2027

10 Relationship between work packages and research goals

Tables 11 - 13 show the various links between the work package and the research goals.

DRDT:		3.1 Monolithic CMOS sensors				3.2 4D Tracking		3.3 Extreme Fluence			3.4 Intercon.			
Workpackage:		Spatial resolution	Temporal resolution	Read-out architecture	Radiation Tolerance	3D sensors	LGAD	Wide band-gap materials	Diamond	Silicon	maskless interconnect	in house post-processing	advanced interconnect	mechanics and cooling
RG Description														
1.1	Spatial resolution: ≤3 μm position resolution	X											X	X
1.2	Temporal resolution: towards 20 ps timing precision		X										X	X
1.3	Readout architectures: towards 100 MHz/cm^2, and 1 GHz/cm^2 with 3D stacked monolithic sensors				X								X	
1.4	Radiation tolerance: towards 10^{16} $\mathrm{n_{eq}/cm^2}$ NIEL and 500 MRad				X									
2.1	Reduction of pixel cell size for 3D sensors					X					X	X		X
2.2	3D sensors for timing (50 × 50 um, < 50 ps)					X					X	X		X
2.3	LGAD for 4D tracking < 10 um, < 30 ps, wafer 6” and 8”						X				X	X		X
2.4	RSD for ToF (Large area, < 30 um, < 30 ps)						X				X	X		X
3.1	Build up data sets on radiation-induced defect formation in WBG materials							X	X					
3.2	Develop silicon radiation damage models based on measured point and cluster defects	X	X	X	X	X	X			X				
3.3	Provide measurements and detector radiation damage models for radiation levels faced in HL-LHC operation	X	X	X	X	X	X			X				
3.4	Measure and model the properties of silicon and WBG sensors in the fluence range 10^{16} to $10^{18}\mathrm{n_{eq}cm^{-2}}$							X	X	X				

Table 11: WG1,2,3: mapping of DRDTs, WPs, and research goals

DRDT:		3.1 Monolithic CMOS sensors				3.2 4D Tracking		3.3 Extreme Fluence			3.4 Intercon.			
Workpackage:		Spatial resolution	Temporal resolution	Read-out architecture	Radiation Tolerance	3D sensors	LGAD	Wide band-gap materials	Diamond	Silicon	maskless interconnect	in house post-processing	advanced interconnect	mechanics and cooling
RG Description														
4.1	Flexible CMOS simulation of 65 nm to test design variations	X	X	X	X									
4.2	Implementation of newly measured semiconductor properties into TCAD and MC simulations tools	X	X	X	X	X	X	X	X	X				
4.3	Definition of benchmark for validating the radiation damage models with measurements and different benchmark models.	X	X			X	X	X	X	X				
4.4	Developing of bulk and surface model for $10^{16}\text{cm}^{-2} < \Phi_{eq} < 10^{17}$ cm^{-2}							X	X	X				
4.5	Collate solutions from different MC tools and develop an algorithm to include adaptive electric and weighting fields	X	X			X	X							
5.1	Develop TPA-TCT	X	X			X	X			X				
5.2	Common infrastructure	X	X	X	X	X	X	X	X	X				
5.3	Networking and training on methods	X	X	X	X	X	X	X	X	X				

Table 12: WG4,5: mapping of DRDTs, WPs, and research goals

DRDT:		3.1 Monolithic CMOS sensors				3.2 4D Tracking		3.3 Extreme Fluence			3.4 Intercon.			
Workpackage:		Spatial resolution	Temporal resolution	Read-out architecture	Radiation Tolerance	3D sensors	LGAD	Wide band-gap materials	Diamond	Silicon	maskless interconnect	in house post-processing	advanced interconnect	mechanics and cooling
RG Description														
6.1	3D diamond detectors, cages / interconnects, base length 25 μm , impact ionization					X			X					
6.2	Fabrication of large area SiC and GaN detectors, improve material quality and reduce defect levels.							X						
6.3	Improve tracking capabilities of WBG materials					X	X	X						
6.4	Apply graphene and/or other 2D materials in radiation detectors; understand signal formation.						X	X		X				
7.1	Yield consolidation for fast interconnections					X	X				X			
7.2	Demonstration of in-house process for single dies and a range of pitch (down to $< 30\mu m$) pixel interconnections					X	X				X	X		
7.3	Development of maskless post-processing for classical bump-like interconnection technologies					X	X				X	X		
7.4	Develop wafer-to-wafer in presently advanced interconnection technologies					X	X					X	X	
7.5	Develop VIAS in multi-tier sensor/front-end assemblies	X	X	X	X	X	X					X	X	

Table 13: WG6,7: mapping of DRDTs, WPs, and research goals

11 DRD3 Resources (2024 - 2026)

11.1 List of research goals

Table 14 lists the DRD3 research goals. Additional RGs can be added following the request of DRD3 collaborators.

WG1 research goals	
RG 1.1	Spatial resolution: ≤ 3 μm position resolution
RG 1.2	Timing resolution: towards 20 ps timing precision
RG 1.3	Readout architectures: towards 100 MHz/cm^2, and 1 GHz/cm^2 with 3D stacked monolithic sensors
RG 1.4	Radiation tolerance: towards 10^{16} n_{eq}/cm^2 NIEL and 500 MRad

WG2 research goals	
RG 2.1	Reduction of pixel cell size for 3D sensors
RG 2.2	3D sensors for timing (50×50 μm, < 50 ps)
RG 2.3	LGAD for 4D tracking < 10 μm, < 30 ps, wafer 6” and 8”
RG 2.4	RSD for ToF (Large area, < 30 μm, < 30 ps)

WG3 research goals	
RG 3.1	Build up data sets on radiation-induced defect formation in WBG materials
RG 3.2	Develop silicon radiation damage models based on measured point and cluster defects
RG 3.3	Provide measurements and detector radiation damage models for radiation levels faced in HL-LHC operation
RG 3.4	Measure and model the properties of silicon and WBG sensors in the fluence range 10^{16} to $10^{18} n_{eq} cm^{-2}$

WG4 research goals	
RG 4.1	Flexible CMOS simulation of 65 nm to test design variations
RG 4.2	Implementation of newly measured semiconductor properties into TCAD and MC simulations tools
RG 4.3	Definition of benchmark for validating the radiation damage models with measurements and different benchmark models.
RG 4.4	Developing of bulk and surface model for $10^{16} cm^{-2} < \Phi_{eq} < 10^{17}$ cm^{-2}
RG 4.5	Collate solutions from different MC tools and develop an algorithm to include adaptive electric and weighting fields

WG5 research goals	
RG 5.1	Develop TPA-TCT
RG 5.2	Common infrastructure
RG 5.3	Networking and training on methods

WG6 research goals	

RG 6.1	3D diamond detectors, cages / interconnects, base length 25 μm , impact ionization
RG 6.2	Fabrication of large area SiC and GaN detectors, improve material quality and reduce defect levels.
RG 6.3	Improve tracking capabilities of WBG materials
RG 6.4	Apply graphene and/or other 2D materials in radiation detectors understand signal formation.

WG7 research goals	
RG 7.1	Yield consolidation for fast interconnections
RG 7.2	Demonstration of in-house process for single dies and a range of pitch (down to <30 μm) pixel interconnections
RG 7.3	Development of maskless post-processing for classical bump-like interconnection technologies
RG 7.4	Develop wafer-to-wafer in presently advanced interconnection technologies
RG 7.5	Develop VIAS in multi-tier sensor/front-end assemblies

WG8 research goals	
RG 8.1	Design and set-up of the DRD3 web site
RG 8.2	Collection of the outreach material
RG 8.3	Set-up and organize schools and exchange programs
RG 8.4	Set-up of the DRD3 conference committee

Table 14: List of Research goals 2024 - 2026

11.2 DRD3 Resources

The questionnaire asked resources for the following two categories:

- **Present situation:** Resource allocation expected on existing funding lines for the period 2024-26.
- **Strategic R&D:** Resource allocation coming from the funding requests for strategic R&D you intend to file.

Table 15 shows the resources available to DRD3.

	Present situation			Strategic R&D	
	Permanent [FTE/y]	Non Permanent [FTE/y]	Budget [kCHF/y]	Non Permanent [FTE/y]	Budget [kCHF/y]
Total	182.27	171.14	5327.5	193.68	8469.25

Table 15: DRD3 resources per year in the period 2014 - 2016

11.3 Resources for each research goal

In this section, the resources for each research goal are presented. Table 16 lists the resources for each research goal while Figure 8 shows the same information graphically.

	Present situation			Strategic R&D	
Research goal	Permanent [FTE/y]	Non Permanent [FTE/y]	Budget [kCHF/y]	Non Permanent [FTE/y]	Budget [kCHF/y]
1.1	16.5	15.8	531.3	18.2	18.2
1.2	10.8	11.8	354.3	12.4	12.4
1.3	12.1	12.5	397.2	14.0	14.0
1.4	12.5	11.5	412.3	12.7	12.7
Total	52.0	51.5	1695.2	57.3	57.3
2.1	3.4	5.0	83.6	4.8	5.1
2.2	8.5	6.9	266.3	7.1	6.1
2.3	11.9	12.9	328.2	13.7	11.3
2.4	4.9	6.8	145.4	5.0	4.4
Total	28.7	31.6	823.4	30.7	27.0
3.1	3.6	4.2	100.1	3.7	4.3
3.2	4.1	2.5	114.8	5.8	5.7
3.3	9.8	6.7	203.8	6.6	6.6
3.4	7.2	8.4	157.3	8.5	9.1
Total	24.8	21.8	576.0	24.5	25.7

4.1	3.7	2.9	82.1	3.4	3.4
4.2	5.6	5.6	114.2	6.0	5.9
4.3	2.1	1.7	54.9	2.6	2.5
4.4	4.4	3.3	144.8	3.8	3.8
4.5	1.7	1.8	28.2	1.7	1.9
Total	17.4	15.3	424.2	17.5	17.4
5.1	2.9	2.4	47.8	2.3	2.2
5.2	5.8	5.2	141.9	5.8	6.0
5.3	3.8	3.3	100.8	2.4	2.4
Total	12.6	10.9	290.5	10.4	10.6
6.1	1.5	1.6	47.5	0.9	0.8
6.2	3.9	2.4	160.6	3.8	3.5
6.3	1.8	1.9	146.1	2.8	2.3
6.4	2.5	1.5	20.2	1.6	2.2
Total	9.6	7.5	374.5	9.1	8.8
7.1	2.2	1.1	60.3	3.6	1.9
7.2	3.5	1.9	125.9	4.6	2.6
7.3	3.5	1.7	90.6	4.7	2.6
7.4	4.5	2.9	147.9	4.7	4.9
7.5	1.6	1.3	48.8	1.2	1.9
Total	15.3	8.8	473.4	18.6	14.0
8.1	0.5	0.4	25.2	1.2	0.8
8.2	1.3	1.5	13.6	2.7	1.9
8.3	5.2	4.6	244.2	4.9	5.0
8.4	3.3	2.4	129.9	2.9	2.4
Total	10.3	8.9	413.0	11.6	10.2

Table 16: Resources per year for each research goal in the period 2024 - 2026

Figure 8: Resources per year for each research goal in the period 2024 - 2026

11.4 List of working groups

The DRD3 working group list is reported here, as shown in the introduction:

- WG1 Monolithic CMOS Sensors
- WG2 Sensors for Tracking and Calorimetry
- WG3 Radiation damage and extreme fluences
- WG4 Simulation
- WG5 Characterization techniques, facilities
- WG6 Wide bandgap and innovative sensor materials
- WG7 Interconnect and device fabrication
- WG8 Dissemination and outreach

11.5 Resources for each working group

By combining the research goals of the same working group, Figure 9 shows the resources for each working group.

Figure 9: Resources per year for each working group in the period 2024 - 2026

12 Path to the DRD3 collaboration

The institutes participating in the proposal must designate a contact person who will serve as a member of the provisional institution board at the time of the submission of the proposal. Additionally, these participating institutions are expected to provide a comprehensive list of individuals involved in the project.

Following the submission of the proposal and before its final approval by the DRDC, the DRD3 proposal team will act as a search committee for the collaboration board chair. The election of the collaboration board chair, utilizing the CERN e-voting system, will occur immediately after the proposal's approval and prior to the inaugural meeting of the collaboration, expected to occur in the first quarter of 2024. This process is essential to establish a functional structure for the collaboration right after its inaugural meeting. The DRD3 proposal team will collaboratively prepare the agenda and program for the inaugural meeting in collaboration with the collaboration board chair. This marks the conclusion of the DRD3 proposal team's mandate.

The collaboration board chair will then assemble a search committee responsible for selecting a candidate pool for the role of spokesperson. These candidates will present their vision for the DRD3 collaboration at the kickoff meeting, including proposals for working group conveners. The spokespersons' elections will take place during the kickoff meeting of the collaboration, thereby establishing the operational functionality of the collaboration. The spokespersons and the collaboration board chair will formulate a Memorandum of Understanding (MoU) for the collaboration and guide its formation by overseeing the establishment of all collaboration bodies. During the interim period before the preparation and endorsement of the DRD3 MoU, the DRD3 proposal team advises adhering to the rules outlined in the RD50 MoU.

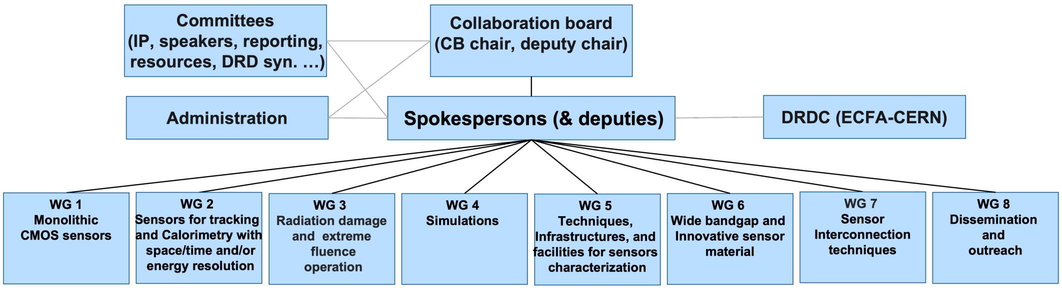


Figure 10: DRD3 organizational chart

12.1 Funding for DRD3 strategic R&D

Funds for the strategic R&D come from national funding agencies and other sources and belong to the respective institutes. The strategic R&D will be the focus of the DRDC reviews.

12.2 Funding for DRD3 blue-sky R&D

Each institute will contribute to the DRD3 Blue-sky common fund. The amount of this levy is expected to be initially 2,000 CHF per year. The new DRD3 CB will define the rules for the funding scheme.

12.3 Funding for DRD3 operation

Each institute will contribute to the cost of the DRD3 collaboration with the host institution covering most of these costs. These costs include, for example, the personnel for administrating the DRD3 collaboration. The new DRD3 CB will define the amount of this levy. We encourage the DRDC to establish a common secretariat for the DRDs.

12.4 Funding presently available in the RD50 collaboration

At the end of 2023, the RD50 collaboration will cease to exist. The funding still present in the RD50 common fund will be transferred to the DRD3 collaboration. This fund will be managed by and available to former RD50 members.

13 Annex - I: List of institutions

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Table 17: List of DRD3 institutions

14 Annex - II: DRD3 Proposal Team

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The workshop speakers listed in [1] are acknowledged for their significant contributions.

15 Acronyms used in the proposal

- ACF: Anisotropic Conductive Films
- ACP: Anisotropic Conductive Pastes
- BEOL: Back-End Of Line
- BSI: Back-Side Illuminated
- CA: Common Area
- CP: Common Project
- DJ-LGAD: Deep-Junction LGAD
- DLTS: Deep Level Transient Spectroscopy
- DMAPS: Depleted Monolithic Active Pixel Sensor
- DRC: Design Rule Checking
- DRDT: Detector R&D Theme
- EPR: Electron Paramagnetic Resonance
- FD-MAPS: Fully-Depleted Monolithic Active Pixel Sensor
- FSI: Front-Side Illuminated
- FTIR: Fourier Transform Infrared Spectroscopy
- iLGAD: inverted LGAD
- iPDK: Interoperable Process Design Kit
- LGAD: Low-Gain Avalanche Diode
- MAPS: Monolithic Active Pixel Sensor
- MC: Monte Carlo
- MPW: Multi-Project Wafer
- PDK: Process Design Kit
- PL: Photo Luminescence
- RG: Research Goal
- RTO: Research and Technology Organisations
- SiC:Silicon Carbide

- SoA: Silicon on Aluminum
- TCT: Transient Current Technique
- TI-LGAD: Trench-Isolated LGAD
- TPA: Two-Photon Absorption
- TRIBIC: Time Resolved Ion Beam Induced Currents
- TSC: Thermally Stimulated Currents
- TSCap: Thermally Stimulated Capacitance
- TSV: Through Silicon Vias
- WBS: Wide Band-Gap Seminconductor
- XRD: X-Ray diffraction

16 References

References

[1] DRD3 group. Implementation of TF3 Solid State detectors. Technical report, 2023.

[2] ECFA Detector RD Roadmap Process Group. The 2021 ECFA detector research and development roadmap. Technical report, Geneva, 2021.