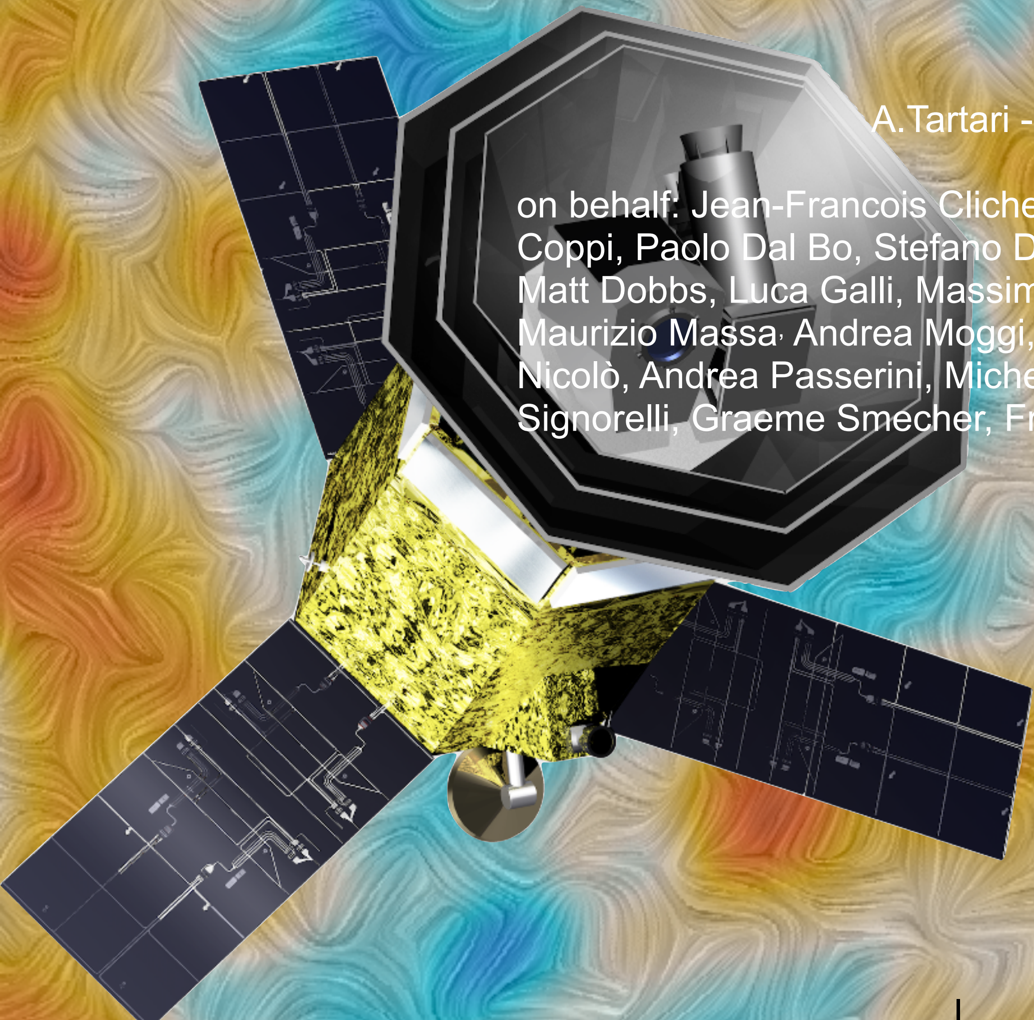
Workshop LiteBIRD-Italia 2023 @ INFN-LNF

SCU Tests and qualifications



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Summary

- Early acceptance tests in 2021
- First performance tests in 2022 McGill (G. Conenna's talk)
- Where do we stand
- Path toward TRL6

jargon: SCU = SCA + SCE (A: assembly, U: unit, E: enclusoure)

2021

- SCA breadboard ready in May 2021
- Test board (SCA tester) ad hoc design to control the SCA breadboard in test phase: ready in June 2021
- Communication protocol tested at UniMiB before shipment to Pisa
- Functional tests in a dedicated EMI shielded room
- Shipment to McGill of 2 boards, including test reports - July 2021

Acceptance tests (2021)

SCA P0 breadboard ready (May 2021):

- Voltages OK test points
- switching enabled
- Clock OK
- etc.

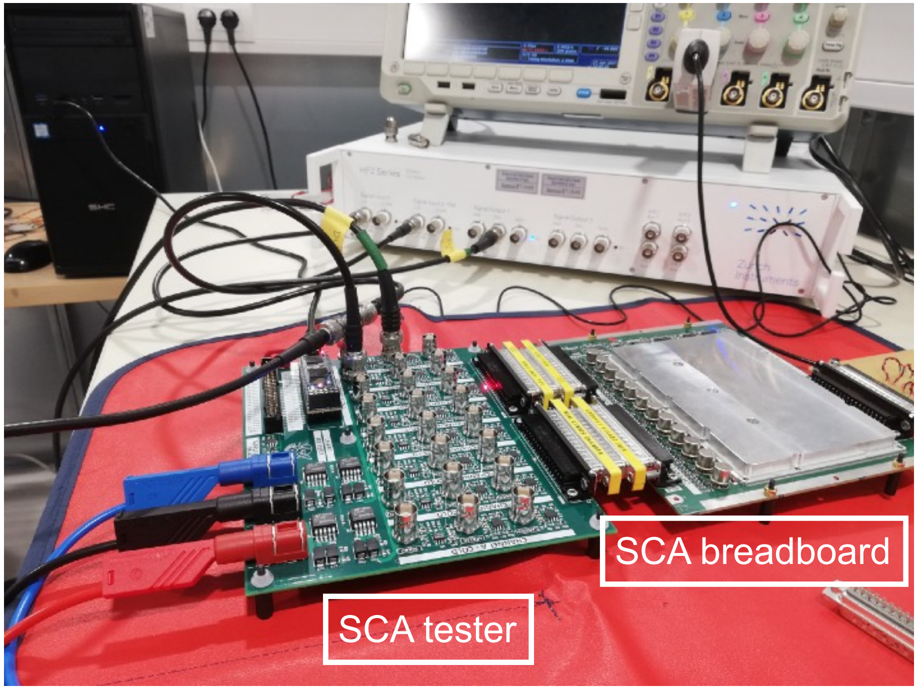
⇒ ready to move to functional tests

SCA-P0 v1.1 : first ignition measurements

PARAMETER	SCA/P0#1 13/05 – A.P.	SCA/P0#2 17/05 – L.S.	SCA/P0#3 17/05 – L.S.	SCA/P0#4 17/05 – L.S.	SCA/P0#5 17/05 – L.S.	UNITS	TEST POINT
POWER: V_{HOT} ACTIVE							
V_{Hot}	5.502	5.501	5.502	5.497	5.498	V	TP1
I_{Hot}	283	285	286	327	328	mA	SUPPLY METER
V_{Cold}	3.9	3.7	3.5	3.3	3.6	mV	TP2
+5V	4.948	4.962	4.953	4.959	4.955	V	TP3
+3V3	3.264	3.267	3.286	3.270	3.284	V	TP4
$XCVR_{HVcc}$	3.254	3.258	3.276	3.260	3.274	V	U200.14
$XCVR_{HVen}$	3.290	3.289	3.284	3.282	3.283	V	U200.18
$XCVR_{CVcc}$	1.898	2.037	1.957	1.902	1.912	V	U201.14
$XCVR_{CVen}$	12	11	14	16	15	mV	U201.18
$Q18_{Drop}$	2.00	1.80	1.78	2.50	1.75	mV	
$Q21_{Drop}$	4.920	4.933	4.925	4.931	4.927	V	
POWER: V_{COLD} ACTIVE							
V_{Cold}	5.504	5.508	5.505	5.505	5.508	V	TP2
I_{Cold}	285	255	284	286	254	mA	SUPPLY METER
V_{Hot}	379	0	381	380	0.8	mV	TP1
+5V	4.962	4.968	4.966	4.988	4.970	V	TP3
+3V3	3.264	3.271	3.286	3.271	3.290	V	TP4
$XCVR_{HVcc}$	1.186	0	1.968	1.880	0	V	U200.14
$XCVR_{HVen}$	220	0	221	219	0.4	mV	U200.18
$XCVR_{CVcc}$	3.252	0	3.276	3.260	0	V	U201.14
$XCVR_{CVen}$	3.245	3.268	3.265	3.249	3.287	V	U201.18
$Q18_{Drop}$	4.934	4.940	4.938	4.960	4.942	V	
$Q21_{Drop}$	1.75	1.86	1.77	1.72	1.57	mV	
POWER: V_{HOT} AND V_{COLD} ACTIVE							
V_{Hot}	5.502	5.501	5.502	5.497	5.497	V	TP1
I_{Hot}	283	286	287	328	328	mA	SUPPLY METER
V_{Cold}	5.502	5.502	5.533	5.533	5.533	V	TP2
I_{Cold}	2	2	2	2	2	uA	SUPPLY METER
+5V	4.948	4.961	4.953	4.959	4.955	V	TP3
+3V3	3.264	3.267	3.286	3.270	3.285	V	TP4
$XCVR_{HVcc}$	3.254	3.258	3.276	3.260	3.274	V	U200.14
$XCVR_{HVen}$	3.290	3.289	3.284	3.282	3.283	V	U200.18
$XCVR_{CVcc}$	1.898	2.034	1.955	1.899	1.910	V	U201.14
$XCVR_{CVen}$	12	11	14	16	15	mV	U201.18
$Q18_{Drop}$	2	2	1.78	2.5	1.76	mV	
$Q21_{Drop}$	4.920	4.933	4.925	4.931	4.926	V	
COMMUNICATIONS							
$nIFEN_{TO}$			659			us	TP11
$SCLK_{fmin}$			1.55			KHz	-
DAC_{Waves}	OK		OK			-	TP12
CHANNEL REFERENCE VOLTAGES							
CHA_{REF43}	2.501	2.501	2.500	2.500	2.502	V	U4.8
CHA_{Vref}	2.503	2.503	2.502	2.502	2.504	V	U5.9
CHA_{Vdac}	4.541	4.535	4.539	4.536	4.541	V	U5.1
CHB_{REF43}	2.501	2.501	2.500	2.502	2.500	V	U4.8
CHB_{Vref}	2.503	2.504	2.502	2.503	2.502	V	U5.9
CHB_{Vdac}	4.540	4.545	4.542	4.537	4.531	V	U5.1
CHC_{REF43}	2.500	2.502	2.500	2.502	2.500	V	U4.8
CHC_{Vref}	2.502	2.503	2.502	2.503	2.502	V	U5.9
CHC_{Vdac}	4.534	4.538	4.533	4.542	4.535	V	U5.1
CHD_{REF43}	2.501	2.501	2.500	2.500	2.502	V	U5.1
CHD_{Vref}	2.503	2.503	2.502	2.502	2.504	V	U4.8
CHD_{Vdac}	4.543	4.536	4.542	4.536	4.539	V	U5.9

Functional tests (2021)

- SCA I/O connected by simple loopback circuits
- SCA driven by SCA tester
- SCA tester:
- talks with SCA through an ad-hoc communication protocol (agreed with McGill team)
- converts single-ended to differential lines and vice-versa, for use with laboratory instrumentation

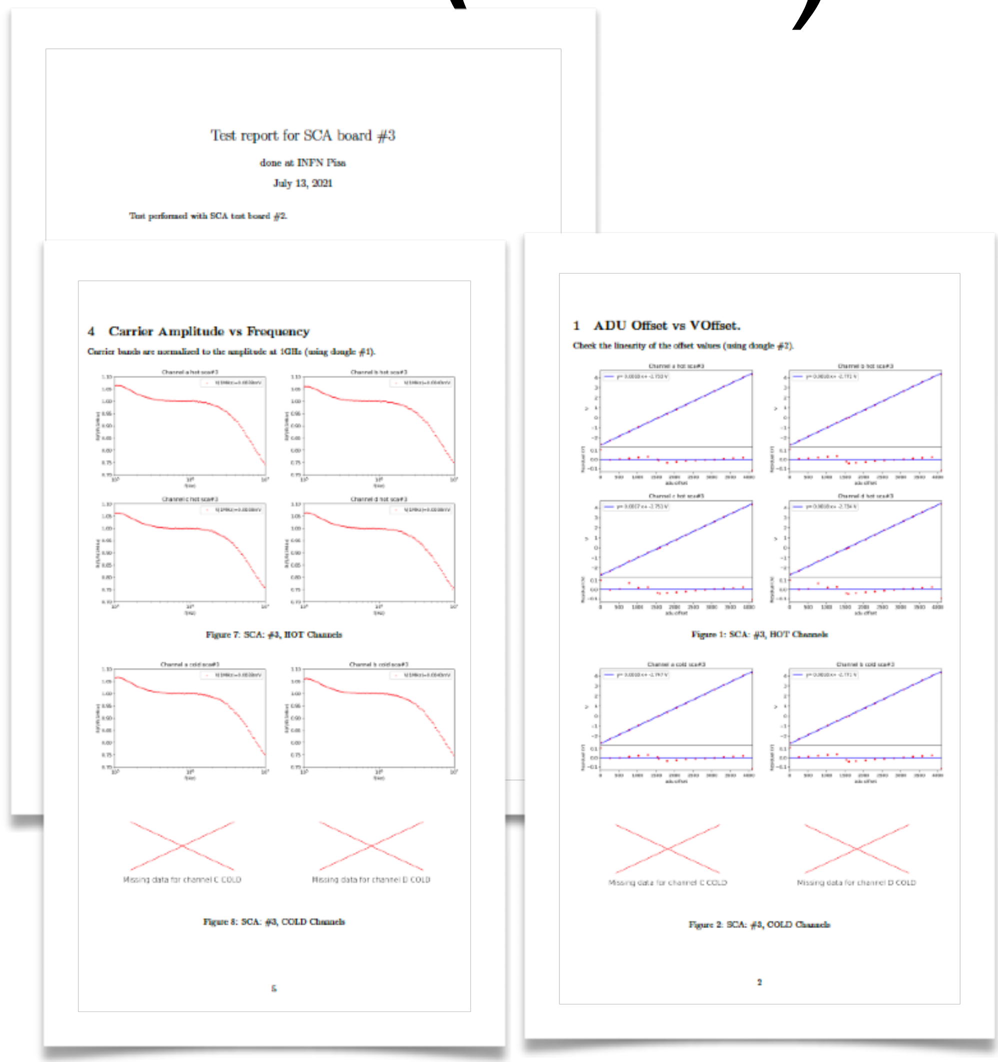


Functional tests (2021)

- SQUID bias (current range)
- Onset of the Flux Locked Loop operation
- Frequency bandwidth in the nominal FDM range (1-5 MHz)
- Cross-talk among the 4 channels living on the same board
- Reporting in a standard sheet

➡ no anomalies detected

➡ Shipment to McGill and Victoria U (Canada) of prototype #3 - #4



Performance test (2022)

- July 2022 - McGill (first post-Covid LiteBIRD mission), 2 weeks

- Test results:
- hardware interfaces with the Signal Processing Assembly (SPA)
- communication interfaces with SPA
- correct operation of the performance redundancy scheme (towards a “hot” and a “cold” D/A assemblies, under CSA/Mc Gill responsibility) by means of Teledyne relays
- the board delivers the desired current range for SQUID bias and heating (if needed)
- noise performances of the SCA breadboard, and end-to-end noise
- bandwidth in a full FDM configuration
- bonus: SCA tester performances as a back-end to replace SPA for SCA testing

Now (spring 2023)

- Feedback from McGill test campaign: slight modification to the breadboard on the FLL path
- Test in progress in McGill (remote control of the experimental set-up from Milano and Pisa)
- Firm conclusion: noise added by LB breadboard prototype not exceeding the noise added by the COTS board (SPT3G). See G. Conenna's talk
- Where do we stand in terms of TRL?

TRL status

- What is SCA current TRL? (assuming standard solutions adopted for thermo-mechanical aspects)

ECSS-E-AS-11C
1 October 2014

Table 4-2: TRL summary: Milestones and work achievement (*reproduced from ISO 16290:2013*)

Technology Readiness Level	Milestone achieved for the element	Work achievement (documented)
TRL 1 - Basic principles observed and reported	Potential applications are identified following basic observations but element concept not yet formulated.	Expression of the basic principles intended for use. Identification of potential applications.
TRL 2 - Technology concept and/or application formulated	Formulation of potential applications and preliminary element concept. No proof of concept yet.	Formulation of potential applications. Preliminary conceptual design of the element, providing understanding of how the basic principles would be used.
TRL 3 - Analytical and experimental critical function and/or characteristic proof-of-concept	Element concept is elaborated and expected performance is demonstrated through analytical models supported by experimental data/characteristics.	Preliminary performance requirements (can target several missions) including definition of functional performance requirements. Conceptual design of the element. Experimental data inputs, laboratory-based experiment definition and results. Element analytical models for the proof-of-concept.
TRL 4 - Component and/or breadboard functional verification in laboratory environment	Element functional performance is demonstrated by breadboard testing in laboratory environment.	Preliminary performance requirements (can target several missions) with definition of functional performance requirements. Conceptual design of the element. Functional performance test plan. Breadboard definition for the functional performance verification. Breadboard test reports.
TRL 5 - Component and/or breadboard critical function verification in a relevant environment	Critical functions of the element are identified and the associated relevant environment is defined. Breadboards not full-scale are built for verifying the performance through testing in the relevant environment, subject to scaling effects.	Preliminary definition of performance requirements and of the relevant environment. Identification and analysis of the element critical functions. Preliminary design of the element, supported by appropriate models for the critical functions verification. Critical function test plan. Analysis of scaling effects. Breadboard definition for the critical function verification. Breadboard test reports.

SCA breadboard model

Where do we go

A plan to TRL6 (see Pinchera's talk)

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Technology Readiness Level	Milestone achieved for the element	Work achievement (documented)
TRL 6: Model demonstrating the critical functions of the element in a relevant environment	Critical functions of the element are verified, performance is demonstrated in the relevant environment and representative model(s) in form, fit and function.	Definition of performance requirements and of the relevant environment. Identification and analysis of the element critical functions. Design of the element, supported by appropriate models for the critical functions verification. Critical function test plan. Model definition for the critical function verifications. Model test reports.

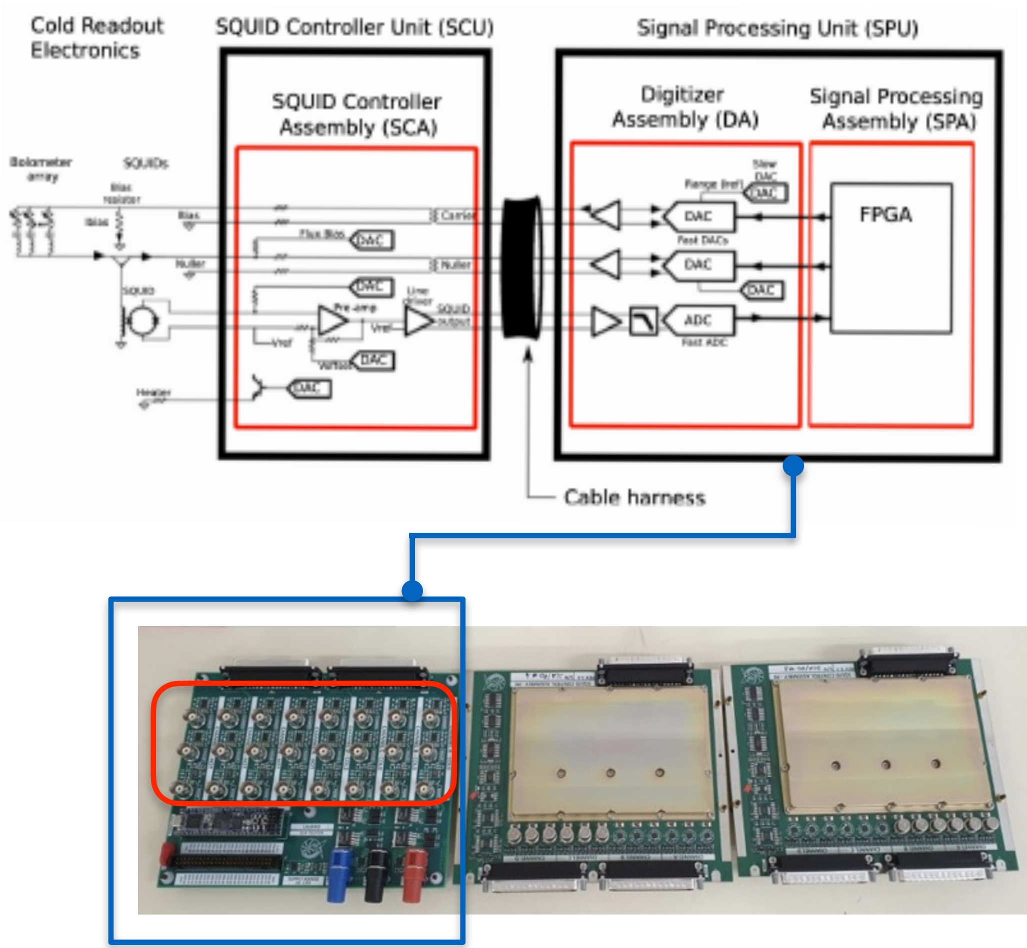
- The key point: "performance in the lab ⇒ performance in relevant environment". Environment: vacuum, temperature TBD.
- Recover the critical functionalities first. Functional tests in RE.
- Evaluate performances.

Where do we go

- Tests in relevant environment (on the breadboard first, and then on engineering models) requires
  - the definition of a test support electronics - the Electrical Ground Support Electronics (EGSE) - i.e. **representative downstream and upstream electronics (wrt the SCA)**.
  - the thermo-vacuum environment.
  - a control software

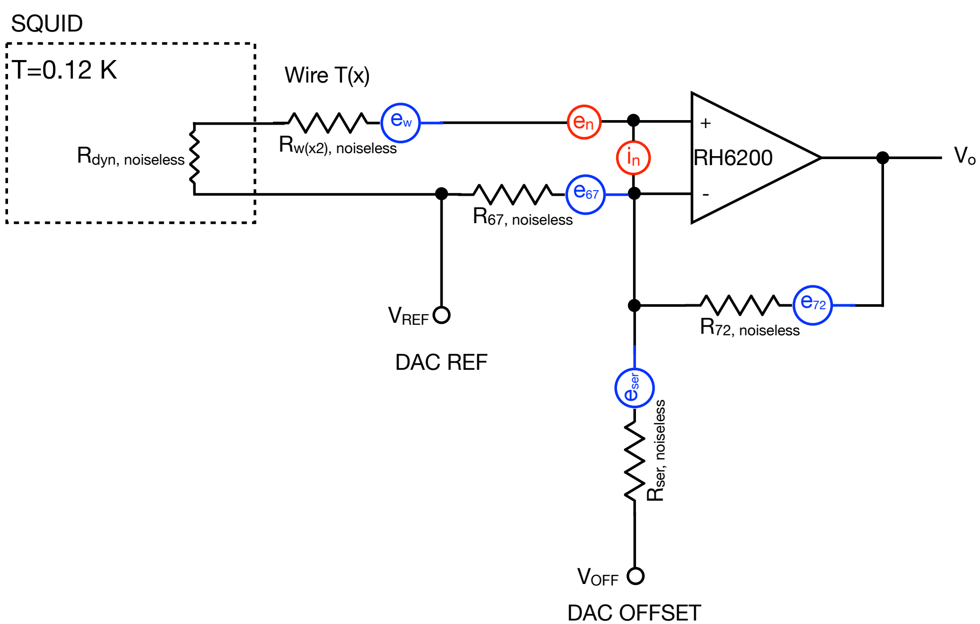
➡ a relevant task, to be defined in all the details, also with some input from the TASI study (M. Zannoni's talk)

➡ Progress from TRL4 to TRL6 will require a substantial and rigorously scheduled experimental activity. No show stopper expected.



Where do we go

- Performance evaluation is sensitive to the thermo-vacuum environment, to a proper grounding, to the harness resistance and temperature, and to the load represented by the SQUID in the bias point. Note in preparation.
- Details TBD (how many boards can/should we run simultaneously?)



$$e_{n,t}^2 = e_n{}^2 + 4k_BTR_{\|} + (i_nR_{\|})^2 + i_n{}^2(2R_w + R_{dyn})^2 + 8R_wk_B < T >_{5-250}$$

Where do we go

- The **SCA tester board** was our basic EGSE in this phase, although overall grounding configuration not faithfully reproducing LiteBIRD one.
- A dedicated study needed - use the SPA as a EGSE for SCA (and vice-versa)?
- Early vibration tests. Preliminary FEM done. Not emphasised here, but needed and fundamental (see M. Massa's talk).
- To do: ho do we feed the Instrument Model with SCA+SPA performance data?
- Modelling activity is essential to provide a synthetic description of detector readout. LiteBIRD note#72 ⇒ to be continued