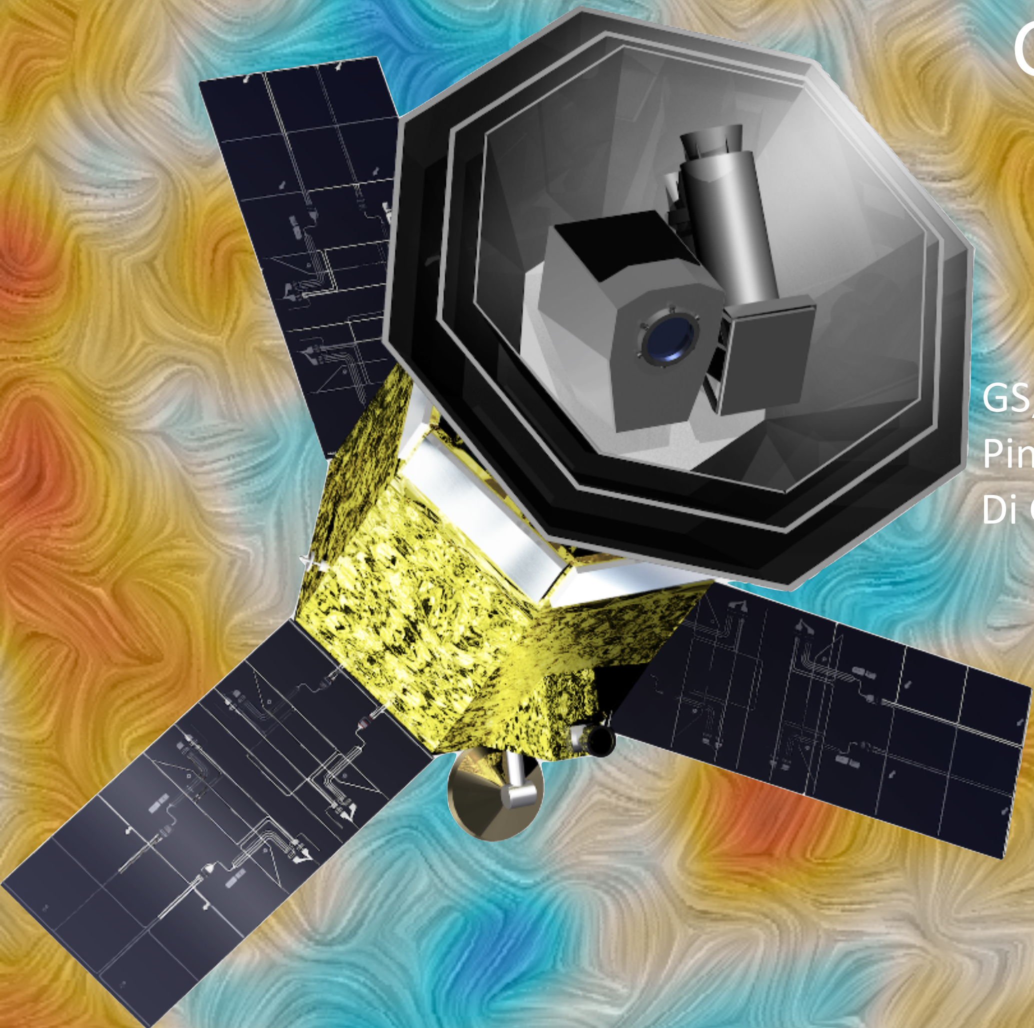
MHFT Readout Electronics Status and Plans

Giovanni Signorelli
INFN Pisa (Italy)

GS, J. Montgomery, M. Zannoni, A. Tartari, M. Pinchera, M. Massa, A. Moggi, G. Conenna, E. Di Giorgi, P. Dal Bo, A. Limonta, A. Passerini, F. Paolucci, S. Della Torre + many others

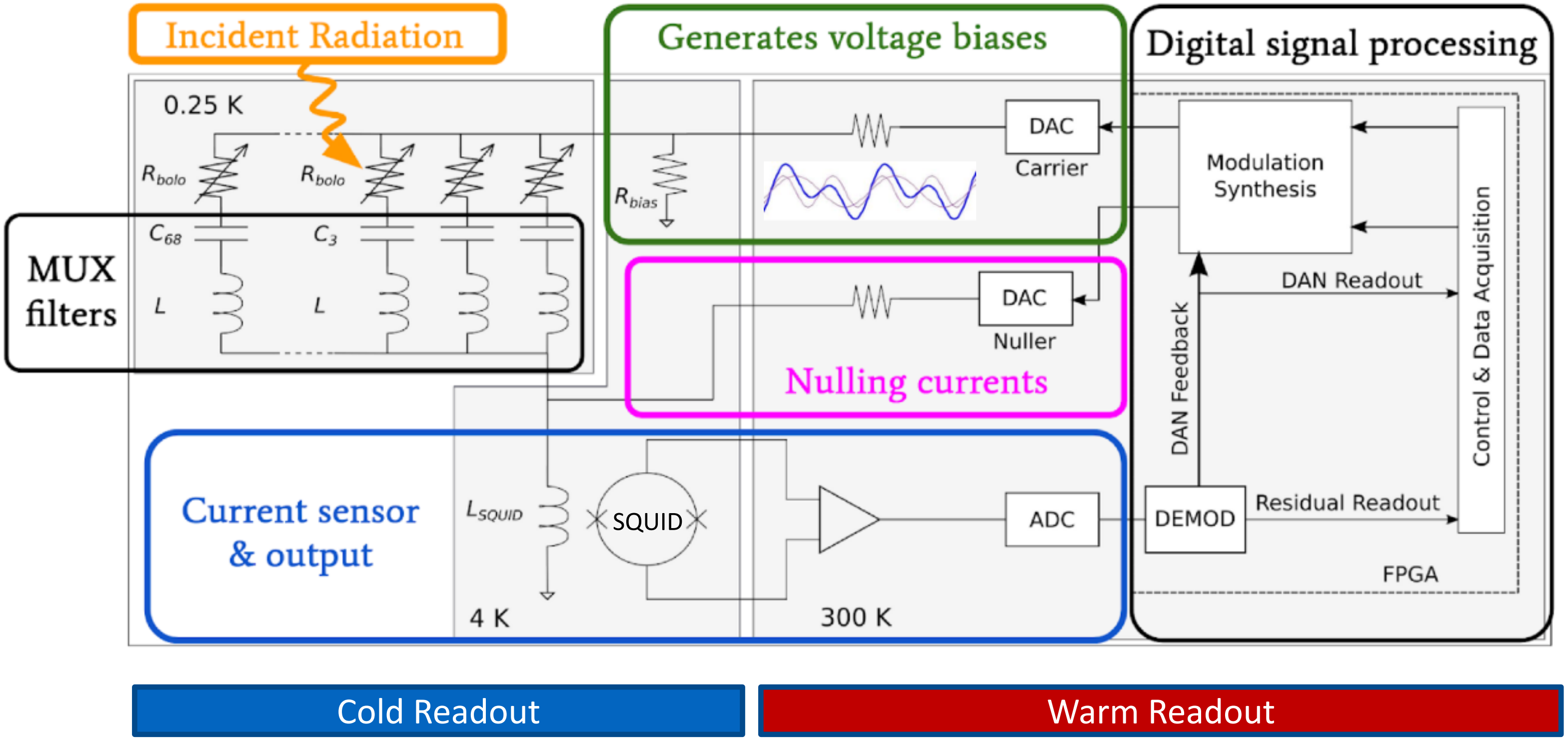


23/03/2023

Warm Readout Schematics

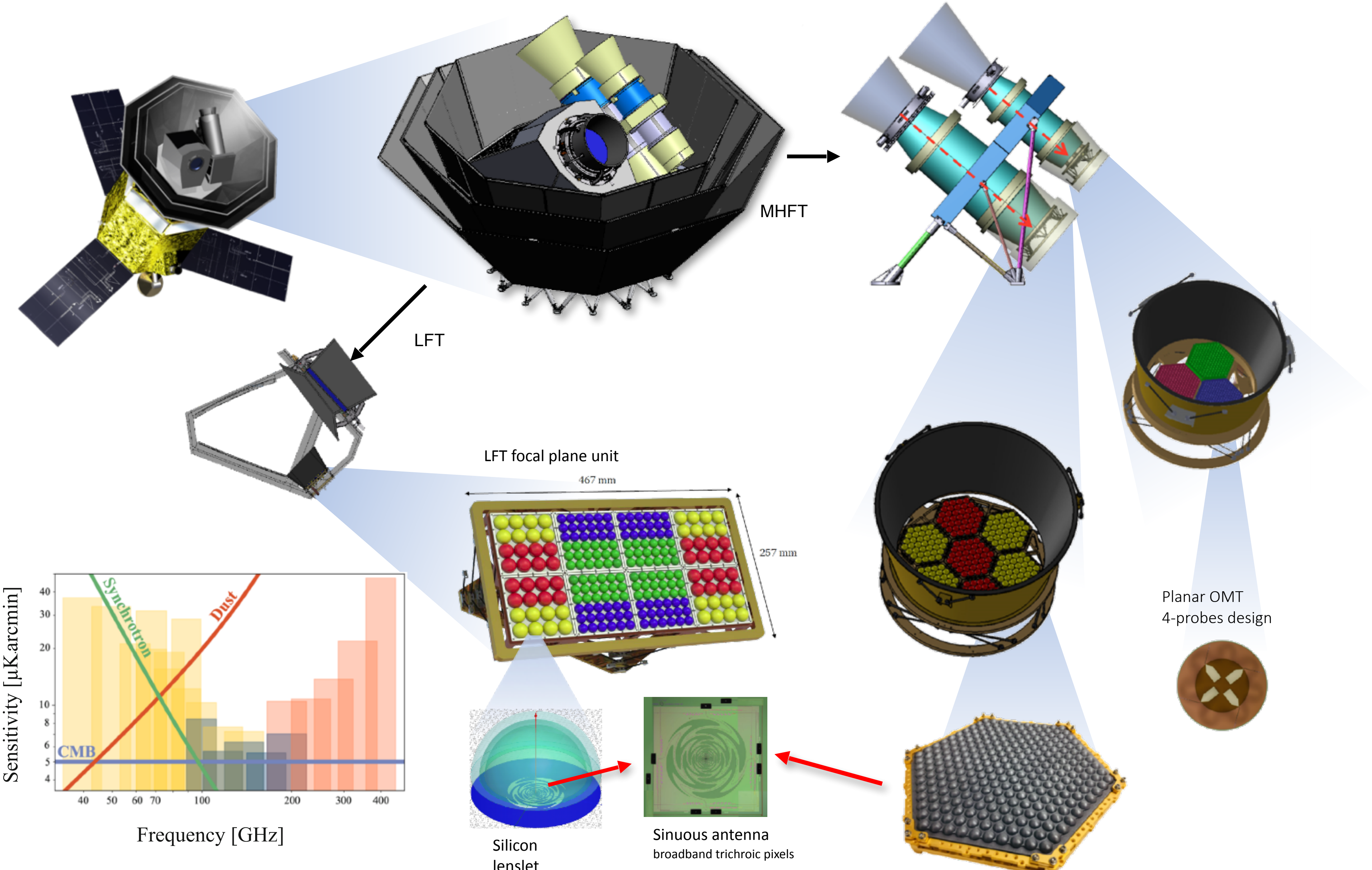
LiteBIRD TES sensors are read by means of FDM = Frequency Domain Multiplexing. Each TES, acting as a variable resistance sensitive to varying incoming microwave radiation, modulates a current that is read by a SQUID.

When each TES is put in series to a superconducting LC filter, a sum of sinusoids can be used to read with a single SQUID a large number (>60) of detectors in parallel.



LiteBIRD Warm Readout is defined as the hardware required to bias and read the SQUIDs, multiplex the signals used to operate and record the output of the bolometer detectors, process the resulting signals from the SQUIDs, and provide the resulting science data to its destination.

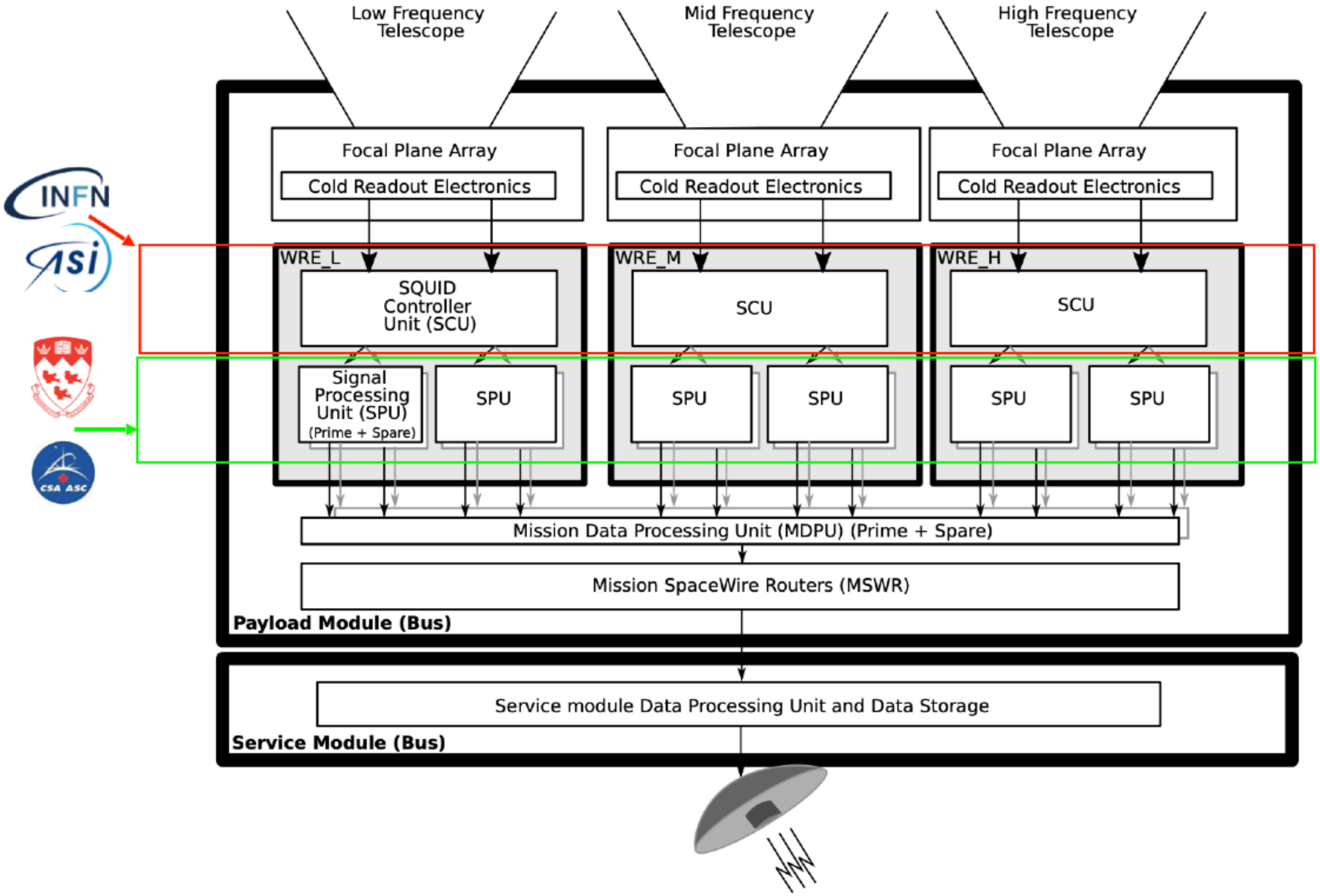
Three telescopes → same readout



It is composed of two logic blocks: the SQUID Controller Units (SCU) and the Signal Processing Units (SPU)

SCU – the (mostly analog) frontend readout – is provided by INFN with ASI (Italy)

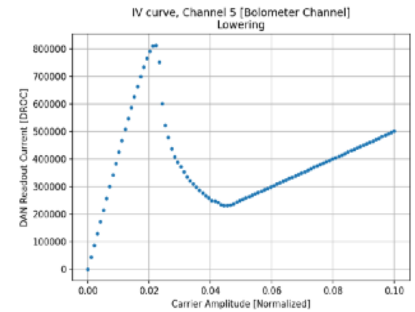
SPU – the digital section (FPGA + digitizers) – is provided by McGill with CSA (Canada)



Design of the WRE = SPU + SCU

WRE (Electronics): **Signal Processing Assembly → Digitizer Assemblies → SQUID Controller Assemblies**
WRE (Enclosures): **Signal Processing Unit ———————————————--→ SQUID Controller Units**

CSA/ McGill Heritage:



2013: Precursor analog hardware (SCA+DA) reached TRL-5

↓

2019: Updates to SCA and DA required for LiteBIRD

→ CSA partnered with INFN to develop the LiteBIRD-suitable SCA/SCU

do radiation qualification of DAC used on the DA

↓

2021: Digital hardware, updated DA, thermal/mech (SPU) and radiation-tolerant firmware reached TRL-5

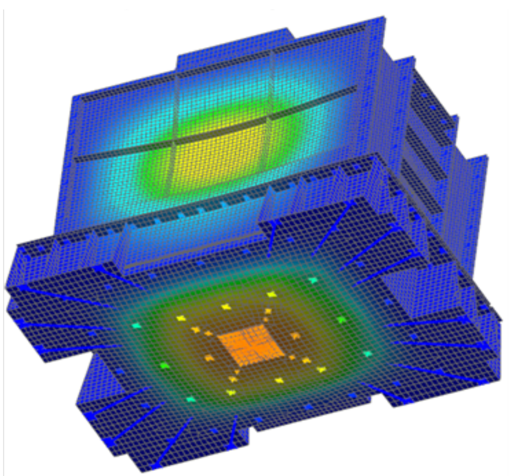
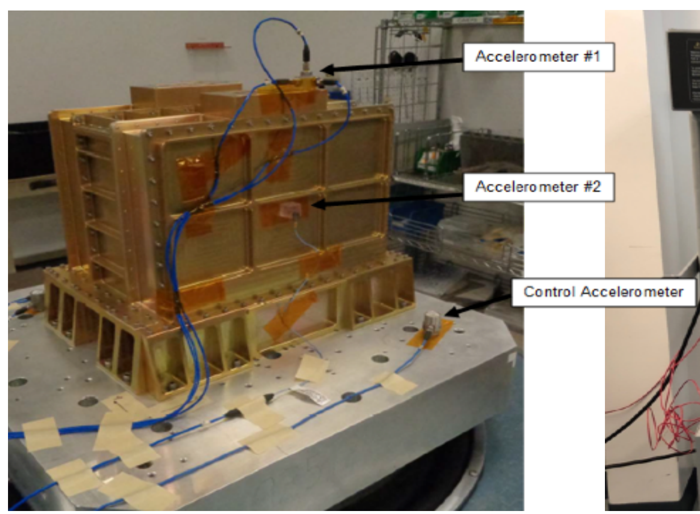


Figure 3-19: Vibration Mode #2, 614 Hz, LiteBIRD Analysis Model

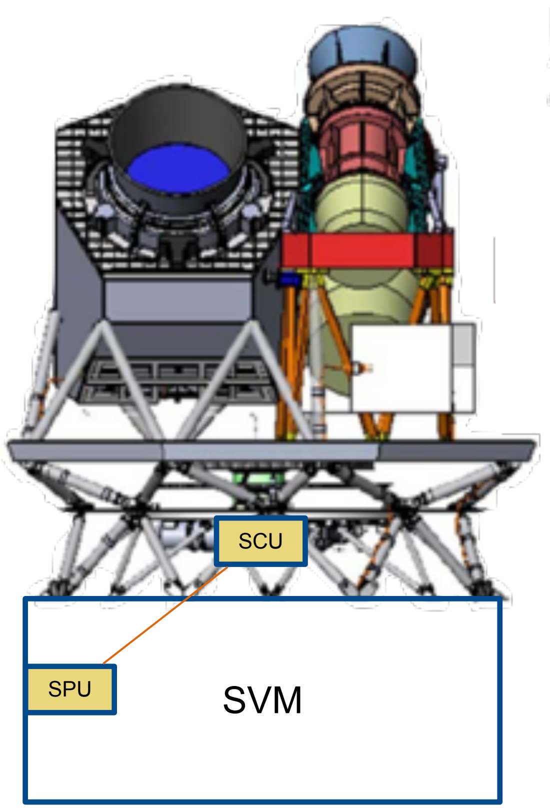


Status of SCU

SCU branched to a separate development being handled by INFN.

SCU is placed outside the service module, close to the focal planes and sitting besides the cryocoolers

We give more details on the SCU development → take all WRE at the same level of maturity



This is why we have an independent documentation for SCU

	Technical Feasibility of SQUID controller units	**Date:** 15 Mar 2023 **Page:** : - 1 – **Ref :** **Version :** 1.0

Technical Feasibility of

SQUID Controller Units

for Phase-A2 Review

	Name	Date & visa
Prepared by	Giovanni Signorelli Michele Pinchera Andrea Tartari Maurizio Massa Andrea Moggi Mario Zannoni Giulia Conenna	15 March 2023
Approved by		

Version	date	Modifications	Name
1.0	15/03/2023	Version for Phase A2 KP Review Panel	G. Signorelli

References

SCU Design Definition and Justification

The SQUID Controller Units (SCU) are in charge of performing the front-end readout of the TESs of the three telescopes: LFT, MFT ad HFT.

They provide bias (carrier) and nuller signals to the bolometers on 4 SQUID modules; they bias and retrieve signals from the SQUIDs.

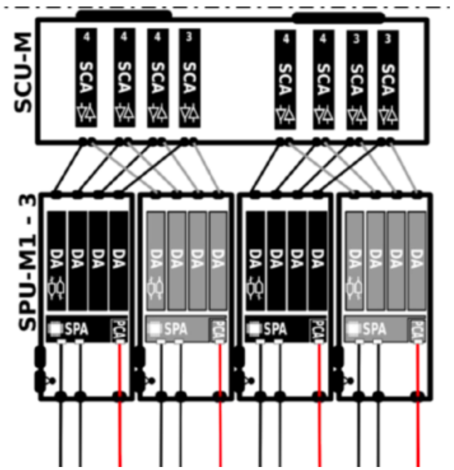
They are designed to

- Send the bias signals (1 to 5 MHz carriers) to the TESs on the focal plane;
- Provide a single SQUID bias in the range 0–400 µA;
- Readout and amplify (x60) the signals from a single SQUID (expected signal in the range 1–9 mV);
- Provide a heater current for trapped flux removal (through a +5V generator);
- Send the nulling signal to the SQUID input coil;
- Send an extra flux bias to the SQUID through the input coil;
- Implement "performance" redundancy on the warm readout side (1xSCA → 2xSPA) w/mechanical relays

At the time of the writing of this presentation a discussion is ongoing on adopting a different philosophy, "functional redundancy", in which it is acceptable to have a degradation in the performance of the instrument, that can be compensated otherwise.

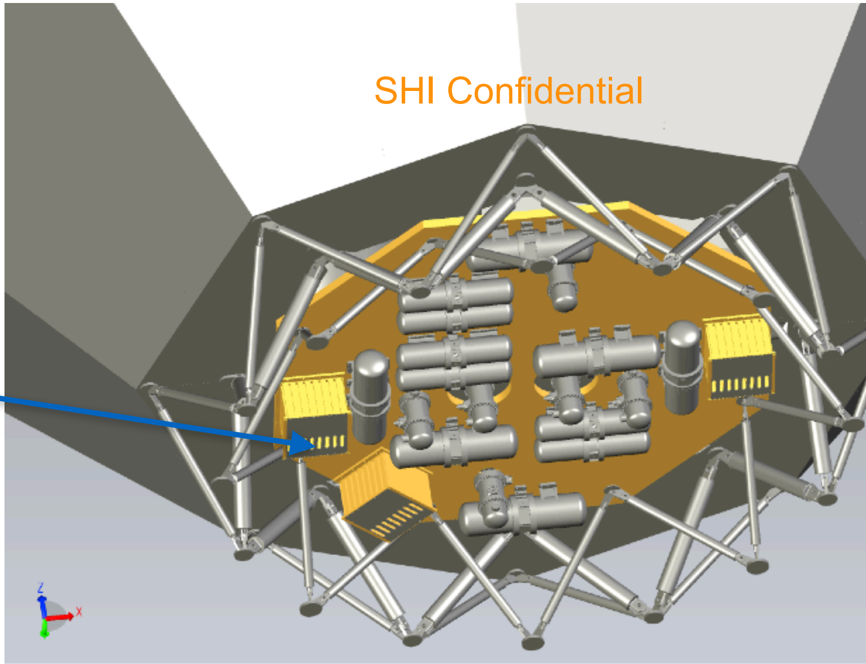
The main difference with the presented design is that with the "functional redundancy" philosophy each SCA is connected one-to-one with a single SPA, eliminating the need of the relays.

This modification simplifies the design and the presented schedules and AIV are compatible with the alternative redundancy scheme

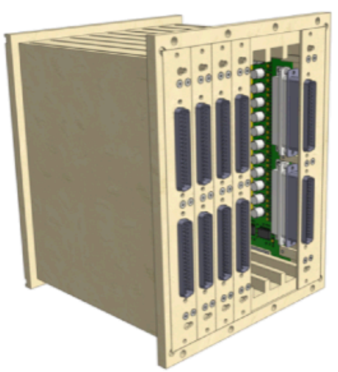


SCE - Mechanical & Thermal design

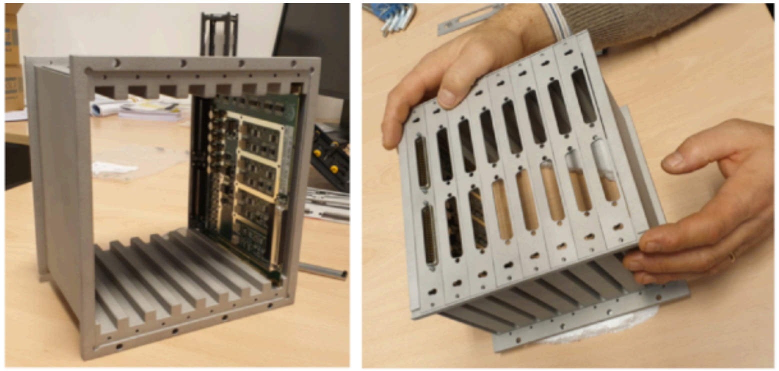
- Mechanical enclosure (SCE) holds 8 SCA boards
- Placed in a “hostile” environment
    - Prototype-0 of SQUID controller enclosure designed
        - Built a preliminary 3D printed version
        - Built a EDMachined version complete of electroplating
        - EMI shields for the boards
    - Under JAXA-INFN NDA
        - Routing of cables, positioning of the units
        - Refine form factor, interfaces
        - Improve thermal contact, simplify tests



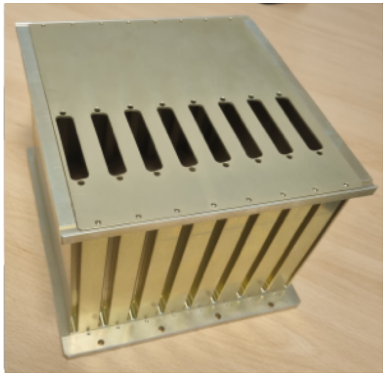
Design



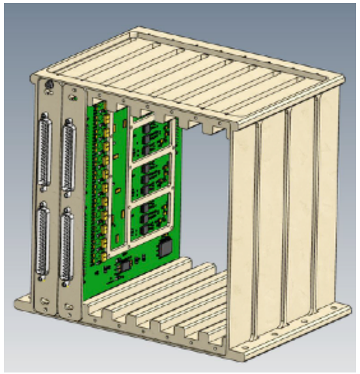
3D printed prototype



EDM prototype

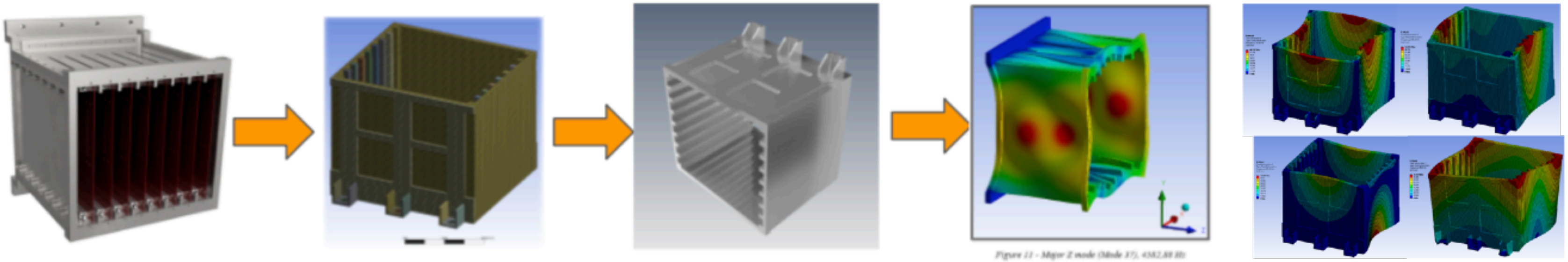


New design



SCE - Mechanical & Thermal design

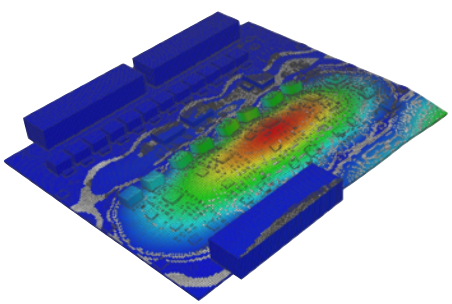
- The resent design is a consequence of several simulations and subject to future tests

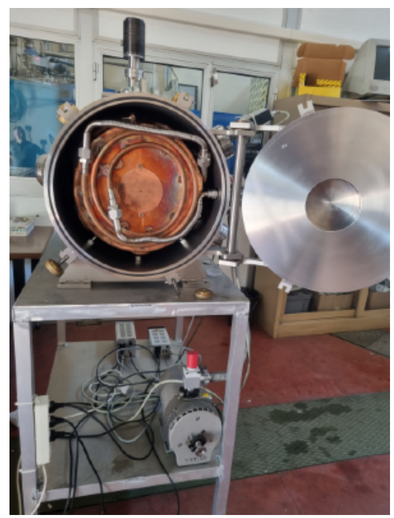


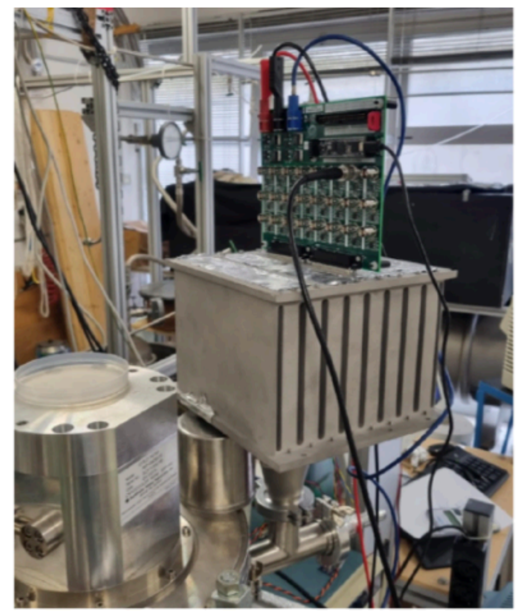
Mode	Frequency [Hz]
1	517,67
2	595,18
3	769,81
4	935,18
5	954,9
6	1017,8
7	1077,1
8	1165,3
9	1269,5
10	1487,8

- The present prototypes are being used in INFN-PI cryogenic test facilities for SCA performance tests
- Thermal analysis under developement, to be carried on at a dedicated facility in INFN-LNF
- Includes thermal study of SCA

Power dissipation on SCA

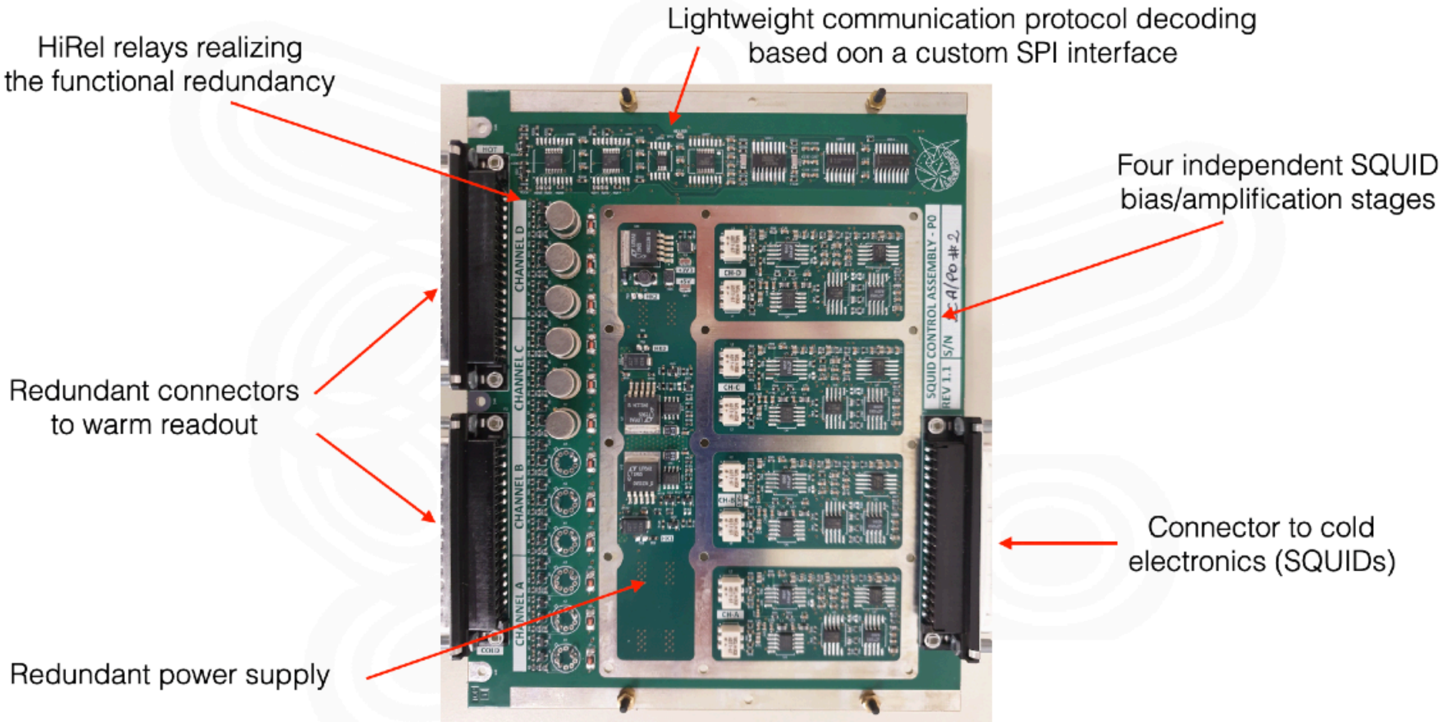






SCA design according to requirements

All the functions have been implemented in a breadboard which is fully form-fit since, despite being populated with COTS components, already contains the footprint of flight components.



The present design is under revision by an industrial partner (Thales Alenia Space Italy, TASI) for

- confirmation / check of our design solutions
- verification of space rules/flight components
- cost evaluation and planning for the procurement of the boards (SCA)

The SCU will then be assembled, tested and qualified under INFN/ASI responsibility

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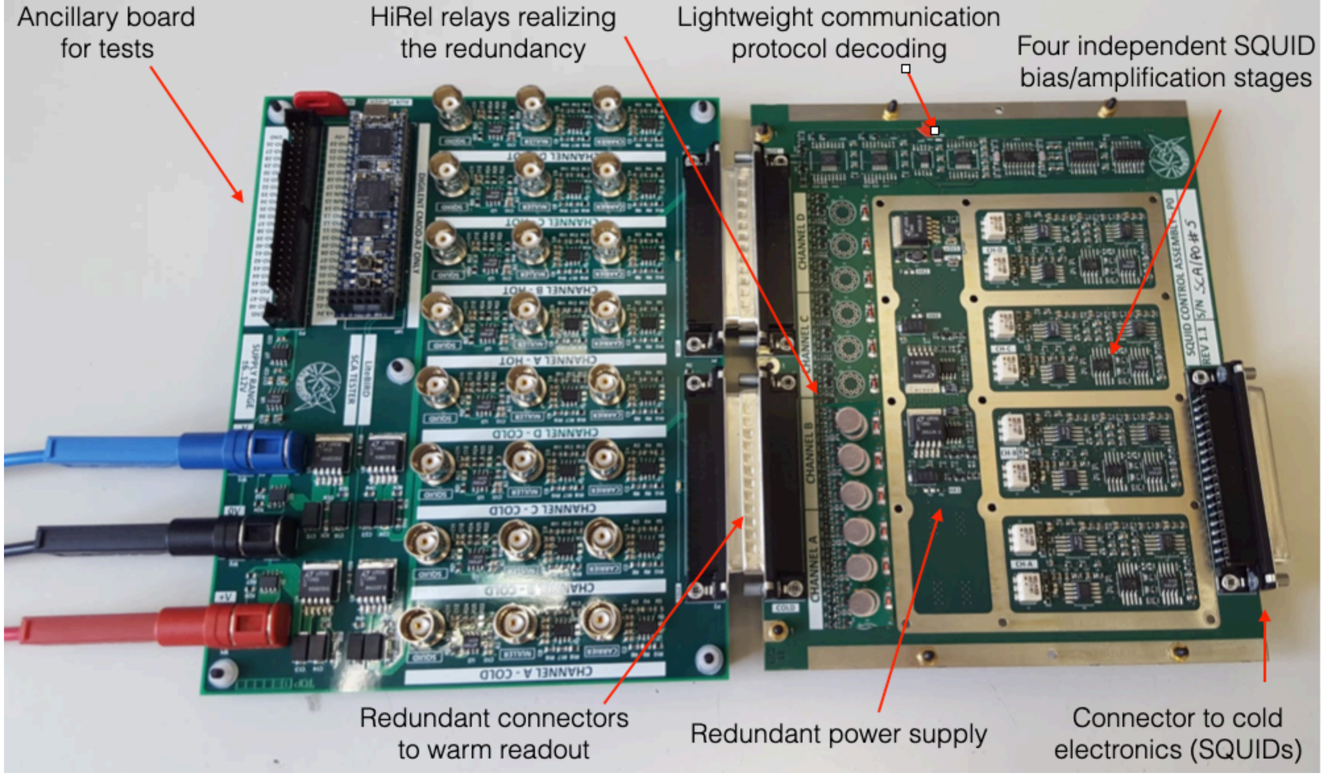

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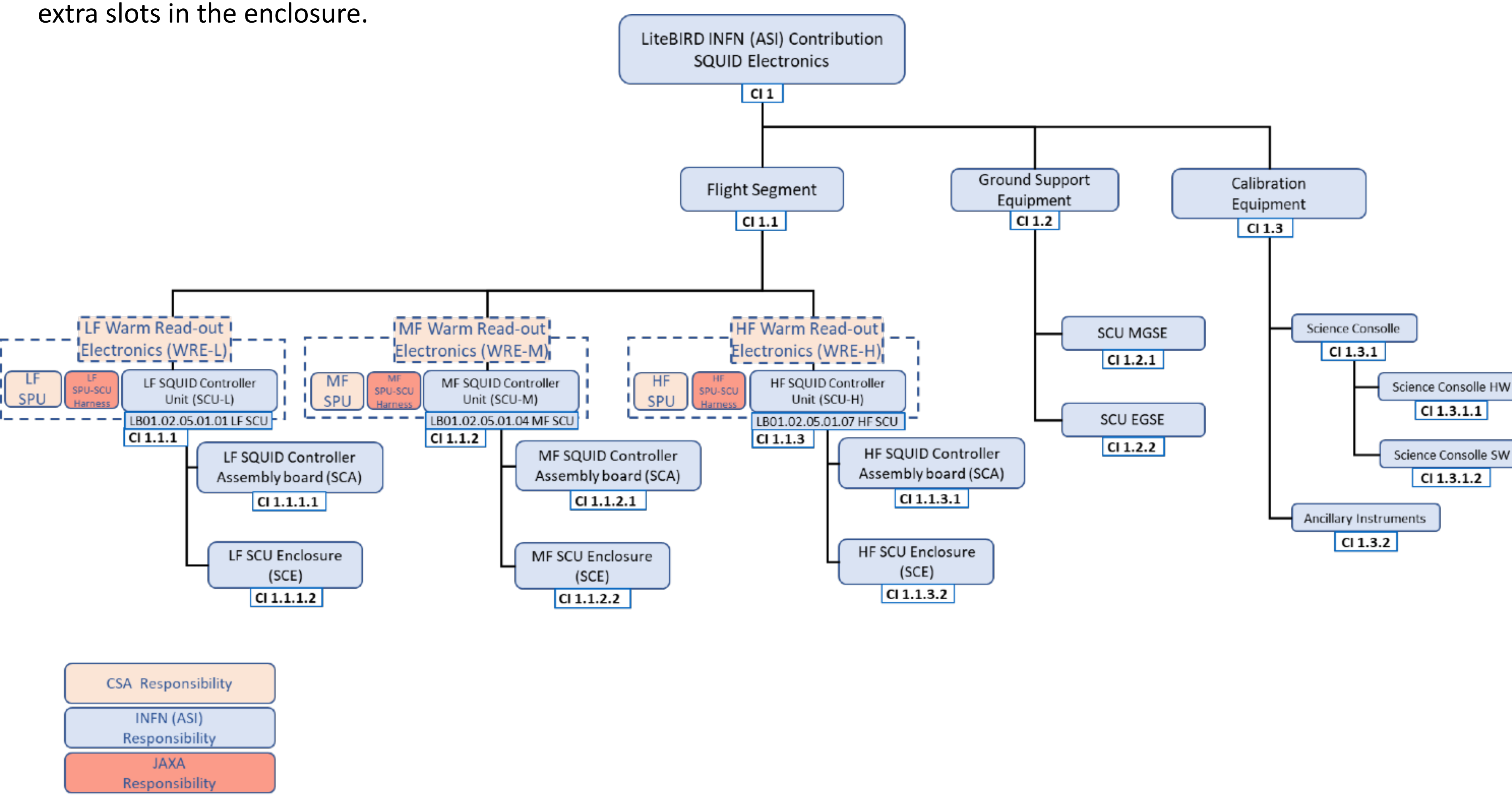
SCU product tree

Three SCUs will be delivered: SCU-L, SCU-M and SCU-H. The three units will be identical, except the fact that SCU-L will host only 6 operating boards, though having 8 slots.

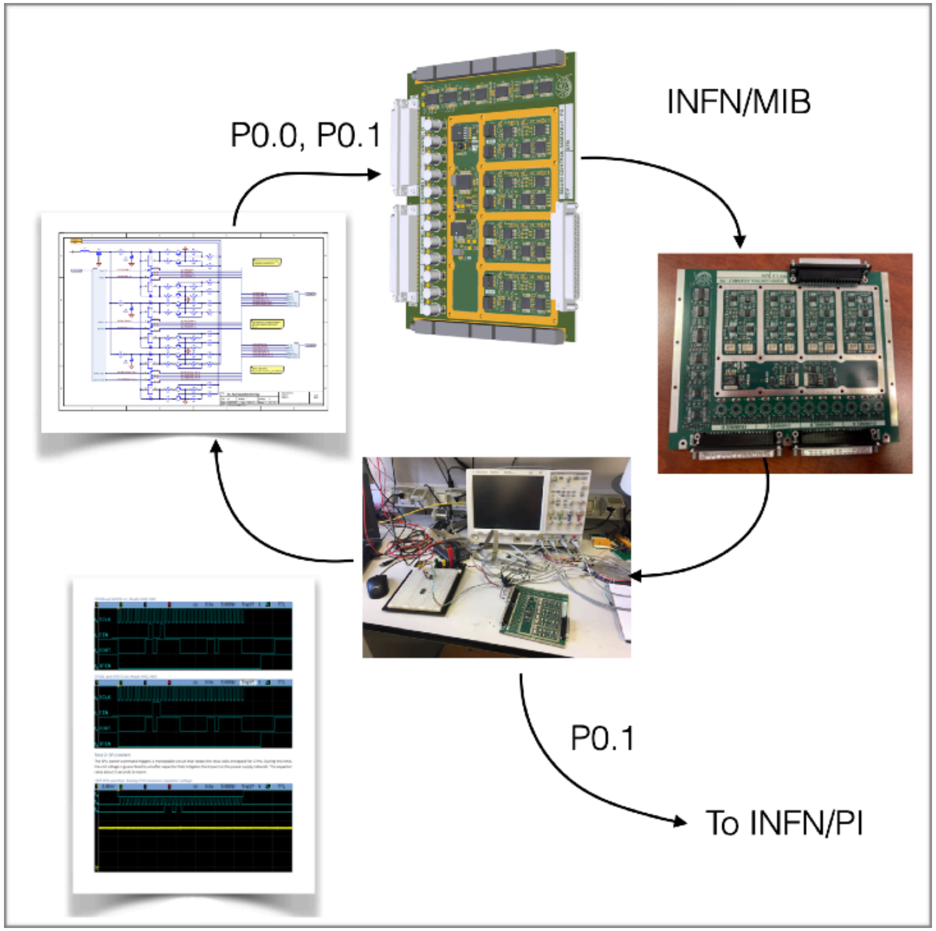
SCE has been designed to host 8 boards and the same enclosure will be used for all three SCUs to simplify the total cost including verification and qualification of the units. In case of SCU-L suitable dummy boards will occupy the 2 extra slots in the enclosure.

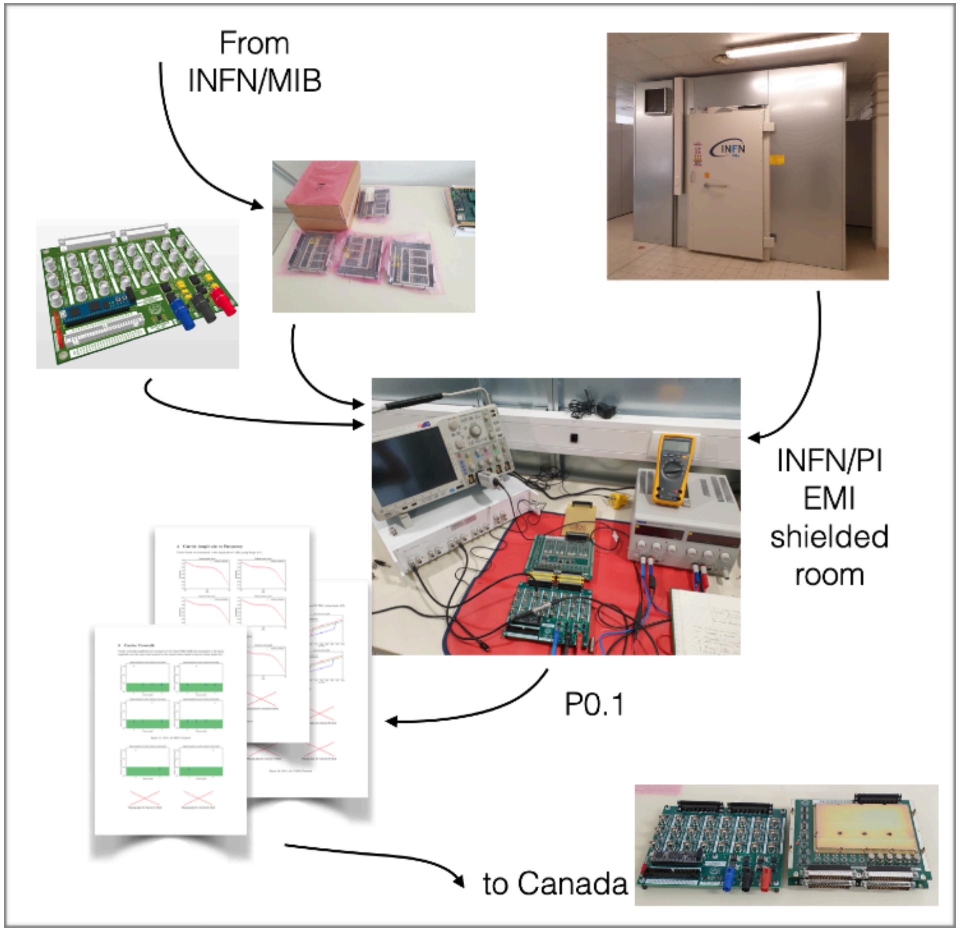


TRL Status

The electrical functional properties of the electronics board have been fully verified in a three stages:

- bench-top at INFN-MIB @ room temperature
- dedicated EMI-shielded test chamber at INFN-PI, at room temperature, using resistive/reactive networks as dummy loads.





TRL Status

We have completed a test campaign at McGill facilities to assess the performance of the SCA prototype model when used in a realistic setting, to control SQUID Array Amplifiers embedded in a FDM TES readout chain → TRL 4/5

Performed in July 2022 at McGill (Canada) by McGill and INFN personnel, some more tests ongoing in these days to verify some minor points

WRE coupling test results

In this test campaign, we have demonstrated that:

1. the interfaces between the SCA and McGill D/A Assembly work as expected in all the aspects: connector compatibility, communication (data and command I/O), low noise analog signal transfer/amplification to/from the SQUID.
2. the noise added by SCA is lower or equal to the one added by equivalent electronics based on COTS components (and without switching stage) developed by the McGill group for ground-based experiments.

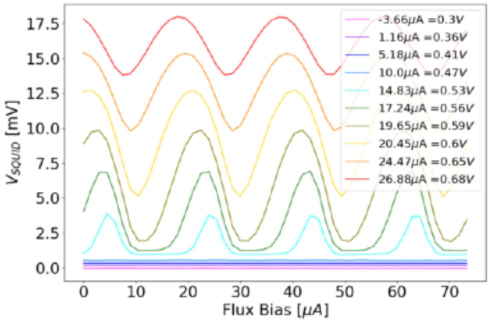


Figure 7 V-φ curves at different current biases applied

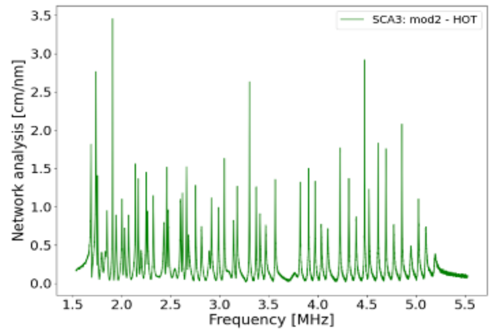
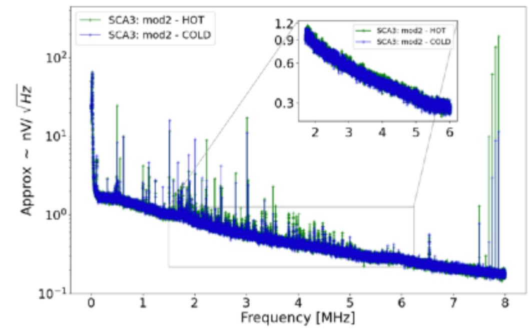


Figure 8. An example of network analysis taken with the full WRE chain (SCA+SPA)



→ The readiness level of the SCU is TRL4/5. For thermal and shielding functionalities, standard solutions will be adopted on the path towards TRL6, which is delineated in the following slides.

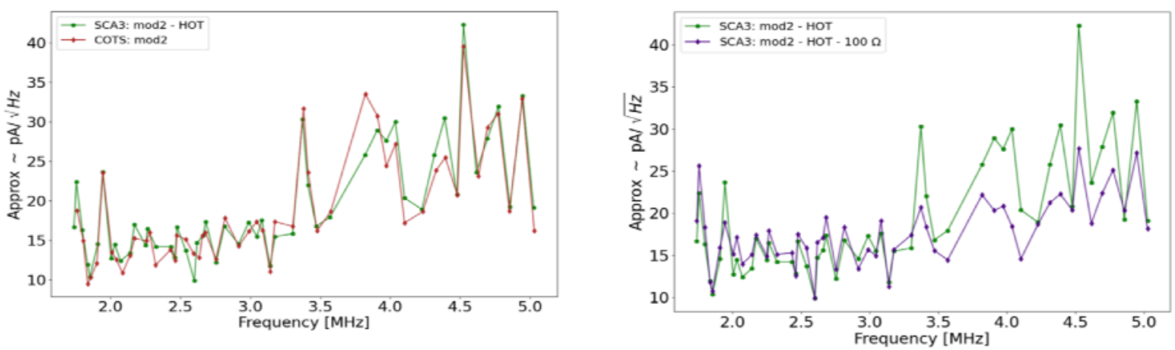


Figure 10. Noise at the SQUID input comparisons. Left: board SCA#3 vs SPT-3G board (COTS). Right: board SCA#3 vs the same board with a 100Ω resistor in order to disable a current sharing path at high frequency.

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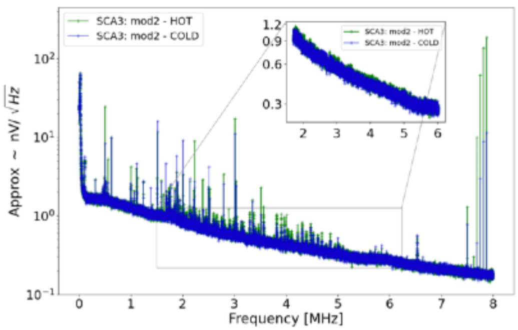
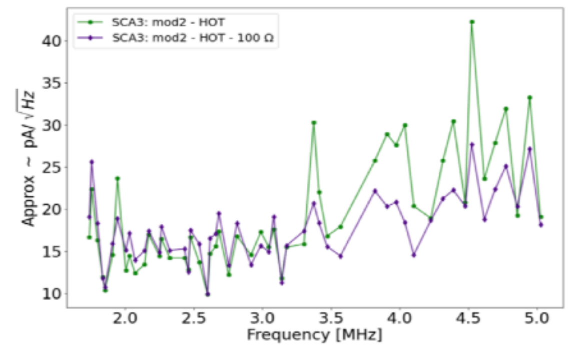
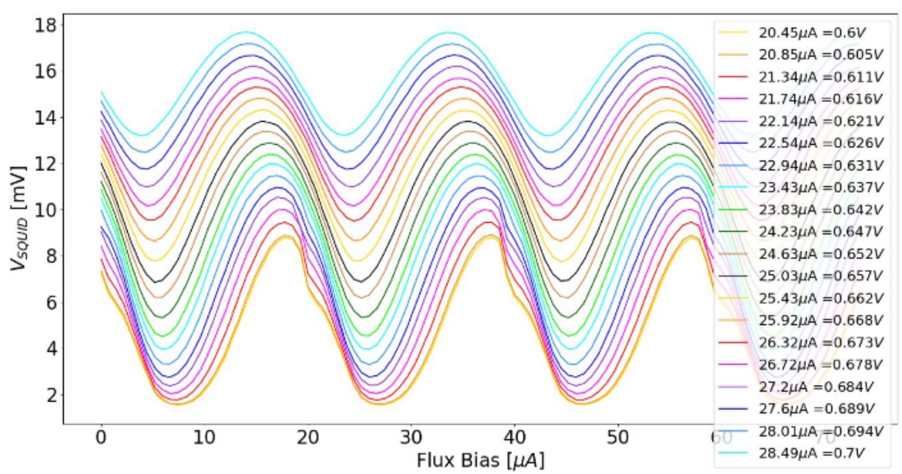






Data being taken right now

Model philosophy and verification

Proto-flight model/flight model (PFM/FM) approach will be used as model philosophy.

- One Engineering Model of SCU for performance validation at unit level
- Three Proto-Flight/Flight Models and Flight Spare of SCU

LiteBIRD SCU HW Matrix	BBM				EM		PFM/FM			Flight Spare	Total qty	
	GSE LFT	GSE MFT	GSE HFT	STM***	EM1**	EM2**	LFT	MFT	HFT		COTS ver	Flight Quality
SQUID Controller Assembly (SCA)	6 (+2dummies)	8	8	1 (+ 7dummies)	4	4	6 (+2dummies)	8	8	8*	29 (+11dummies)	30
SCU Enclosure (SCE)	1	1	1	1	1		1	1	1	1	5	4

* flight spare SCAs as baseline are 8 (4 deliverables as a minimum). The Flight Spare SCAs will be qualified at SCU level.
** EM1 is a set of 4 SCAs deliverable to CSA/JAXA for the integrated WRE/Instrument EM env test campaign
** EM2 is a separate not deliverable EM set of 4 SCAs
The 2 SCA EM sets will be tested at unit level using 1 EM SCE
*** STM is a not deliverable model

A set of BBM (three BBM SCUs and a STM SCU) will be used for the early verification/validation at sub-unit level (SCA).

Will provide sufficient information (proof of concept/model correlation) to enable the progression of the project to the next, more representative models.

The BBM will be manufactured with commercial components and the tests performed on this model will not be part of qualification, acceptance or validation tests. The tests will be used to verify the technology readiness at level 6.

Test matrix

The test matrix for the assumed model philosophy.

LiteBIRD SCU Test Matrix	BBM	EM	PFM (2)	FM (3)	FS (4)
Functional & Performance					
Functional	T	T	T	T	T
Performance	Tsca	T	T	T	T
Physical Properties					
Mass	T	T	T	T	T
CoG	A	A	A	A	A
MoI	A	A	A	A	A
Structural Test					
Vibration	T (1)	T	Tp	Ta	Ta/Tp
Shock		T(5)	Tp(5)	Ta(5)	Ta/Tp(5)
Acoustic	At Satellite level only				
Thermal Test TV/TB	T (1)	T	Tp	Ta	Ta/Tp
EMC/EMI		T	Tp	Ta	Ta/Tp
ESD		T(5)			

Legend	
T	Test
A	Verification by analysis
Tq	Test @ Qualification level
Tp	Test @ ProtoFlight level
Ta	Test @ Acceptance level
Tsca	Test at SCA level

(1) Test with a STM consisting of SCE BBM + 1 SCA BBM + SCA dummies
(2) The Protoflight specified tests are performed for the first PFM unit of the SCU (PFM#1)
(3) Acceptance level tests will be performed on subsequent 3 FMs
(4) The Flight Spare will be 1 of the 4 SCU PFMs/FMs, so it will be qualified at acceptance level as a minimum
(5) Test is TBC

Development Plan

The SCU preliminary master schedule until phase D is reported in the back-up slides.

We show here the key milestones and the main goals that have to be respected to ensure the milestone achievement.

The SCU key milestones dates have to be agreed on the basis of a consolidated schedule from JAXA/prime team.

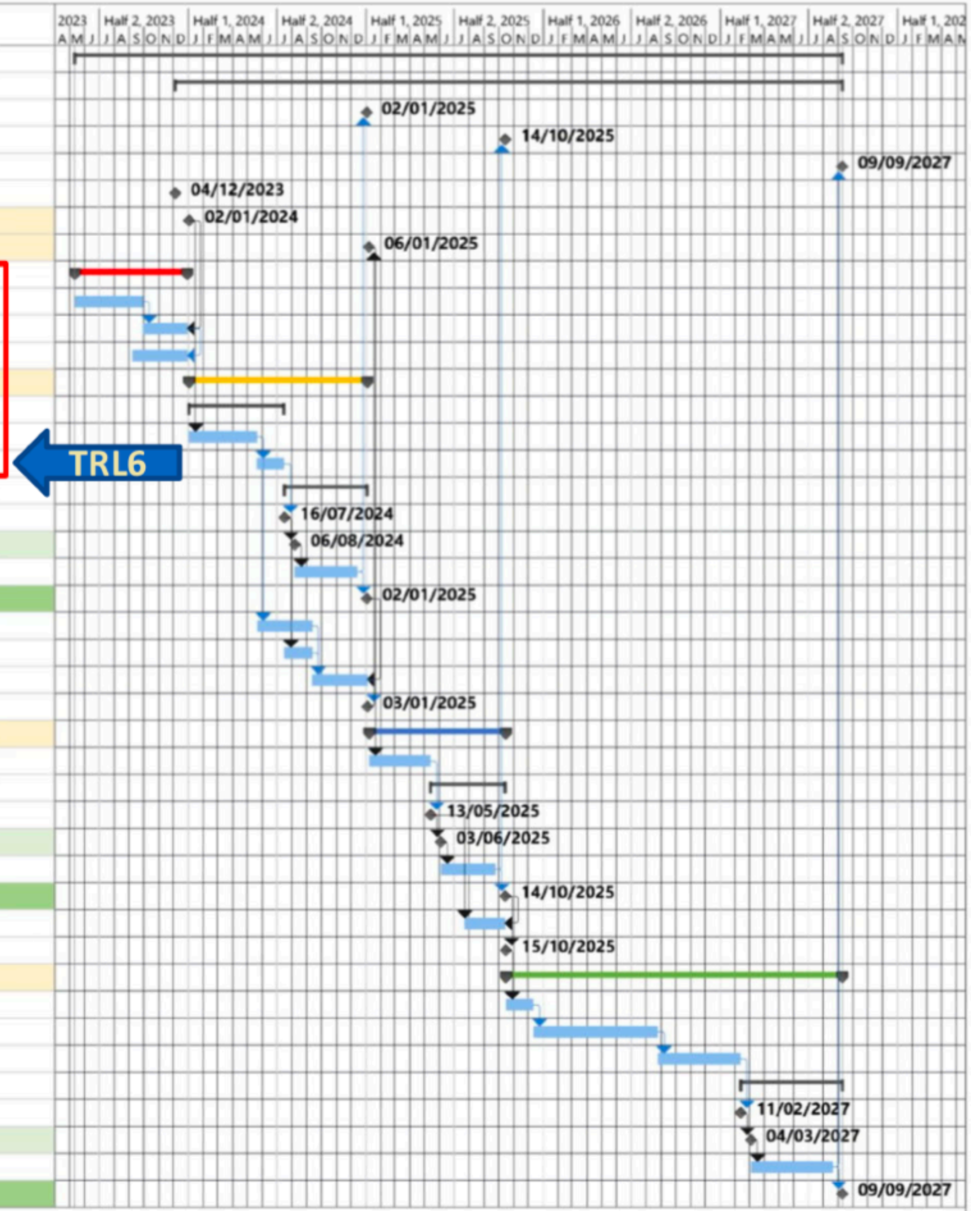
In this preliminary master schedule are considered the WRE delivery need dates provided by JAXA in Dec 2022.

Event or Milestone	Date
SCU Phase B KO	02/01/2024
SCU BBM TRB/DRB & handover to CSA	16/07/2024
SCU BBM LF/HF/MF DELIV to CSA	**06/08/2024**
WRE BBM LF/HF/MF DELIV to JAXA (Jan 2025)	**02/01/2025**
SCU PDR	03/01/2025
SCU Phase C/D KO	06/01/2025
SCU EM TRB/DRB & handover to CSA	13/05/2025
SCU EM LF/HF/MF DELIV to CSA	03/06/2025
WRE EM LF/HF/MF DELIV to JAXA (Oct 2025)	**14/10/2025**
SCU CDR	15/10/2025
SCU FM TRB/DRB & handover to CSA	11/02/2027
SCU FM LF/HF/MF DELIV to CSA	**04/03/2027**
WRE FM LF/HF/MF DELIV to JAXA (Sep 2027)	**09/09/2027**

JAXA updates (March 31 2023, Dotani): Japanese system companies (NEC and Melco) cannot accept an order from JAXA in FY2024 due to the conflict with their manufacturing plan/capability→ delay of the launch by a year or two (from January 2031). The start of phase B will also be delayed. JAXA will keep the schedule of SRR as much as possible → timing to fix the interfaces will not change.

Detailed schedule

ID	Task Name	Duration	Start	Finish
1	**LiteBIRD SCU Main Schedule**	**1119 days**	**12/05/23**	**09/09/27**
2	**SCU Events and Delivery Milestones**	**972 days**	**04/12/23**	**09/09/27**
3	**WRE BBM LF/HF/MF DELIV to JAXA (Jan 2025)**	0 days	02/01/25	02/01/25
4	**WRE EM LF/HF/MF DELIV to JAXA (Oct 2025)**	0 days	14/10/25	14/10/25
5	**WRE FM LF/HF/MF DELIV to JAXA (Sep 2027)**	0 days	09/09/27	09/09/27
6	MHFT-SCU Phase A2 Review (Dec 2023)	0 days	04/12/23	04/12/23
7	**SCU Phase B KO**	0 days	02/01/24	02/01/24
8	**SCU Phase C/D KO**	0 days	06/01/25	06/01/25
9	**SCU Phase Bridging (Phase A2 Completion)**	**164 days**	**12/05/23**	**29/12/23**
10	SCU LF/HF/MF BBM design, analyses	5 mons	12/05/23	28/09/23
11	SCU LF/HF/MF BBM Manufacturing	64 days	29/09/23	29/12/23
12	SCA GSE design & MAIT	4 mons	07/09/23	29/12/23
13	**LiteBIRD SCU Phase B**	**261 days**	**02/01/24**	**03/01/25**
14	**SCU BBM AIT & TRL6**	**140 days**	**02/01/24**	**15/07/24**
15	SCU LF/HF/MF BBM AIT	5 mons	02/01/24	20/05/24
16	SCU/SCA STM Vib + TV Tests (TRL6)	2 mons	21/05/24	15/07/24
17	**SCU BBM LF/HF/MF Units Delivery & WRE Integrated AIT**	**119 days**	**16/07/24**	**02/01/25**
18	SCU BBM TRB/DRB & handover to CSA	0 days	16/07/24	16/07/24
19	**SCU BBM LF/HF/MF DELIV to CSA**	0 days	06/08/24	06/08/24
20	WRE Integrated BBM AIT support	4.6 mons	07/08/24	12/12/24
21	**WRE BBM LF/HF/MF DELIV to JAXA**	0 days	02/01/25	02/01/25
22	SCU GSE design & MAIT	4 mons	21/05/24	10/09/24
23	SCU EM design, analyses	2 mons	17/07/24	10/09/24
24	SCU EM MAIT	4 mons	11/09/24	03/01/25
25	**SCU PDR**	0 days	03/01/25	03/01/25
26	**LiteBIRD SCU Phase C**	**202 days**	**07/01/25**	**15/10/25**
27	SCU EM Qualification Env Tests	4.5 mons	07/01/25	12/05/25
28	**SCU EM LF/HF/MF Units Delivery & WRE Integrated AIT**	**110 days**	**13/05/25**	**14/10/25**
29	SCU EM TRB/DRB & handover to CSA	0 days	13/05/25	13/05/25
30	SCU EM LF/HF/MF DELIV to CSA	0 days	03/06/25	03/06/25
31	WRE Integrated EM AIT support	4 mons	04/06/25	23/09/25
32	**WRE EM LF/HF/MF DELIV to JAXA**	0 days	14/10/25	14/10/25
33	SCU FM design and analyses	3 mons	23/07/25	14/10/25
34	**SCU CDR**	0 days	15/10/25	15/10/25
35	**LiteBIRD SCU Phase D**	**491 days**	**16/10/25**	**09/09/27**
36	SCU FM design and analyses refinement	2 mons	16/10/25	10/12/25
37	SCU FM MAIT	9 mons	11/12/25	24/08/26
38	SCU FM Protoflight/Acceptance tests	6 mons	25/08/26	10/02/27
39	**SCU FM LF/HF/MF Units and FS Unit Delivery & WRE Integrated AIT**	**150 days**	**11/02/27**	**09/09/27**
40	SCU FM TRB/DRB & handover to CSA	0 days	11/02/27	11/02/27
41	SCU FM LF/HF/MF DELIV to CSA	0 days	04/03/27	04/03/27
42	WRE Integrated FM AIT support	6 mons	05/03/27	19/08/27
43	**WRE FM LF/HF/MF DELIV. to JAXA**	0 days	09/09/27	09/09/27

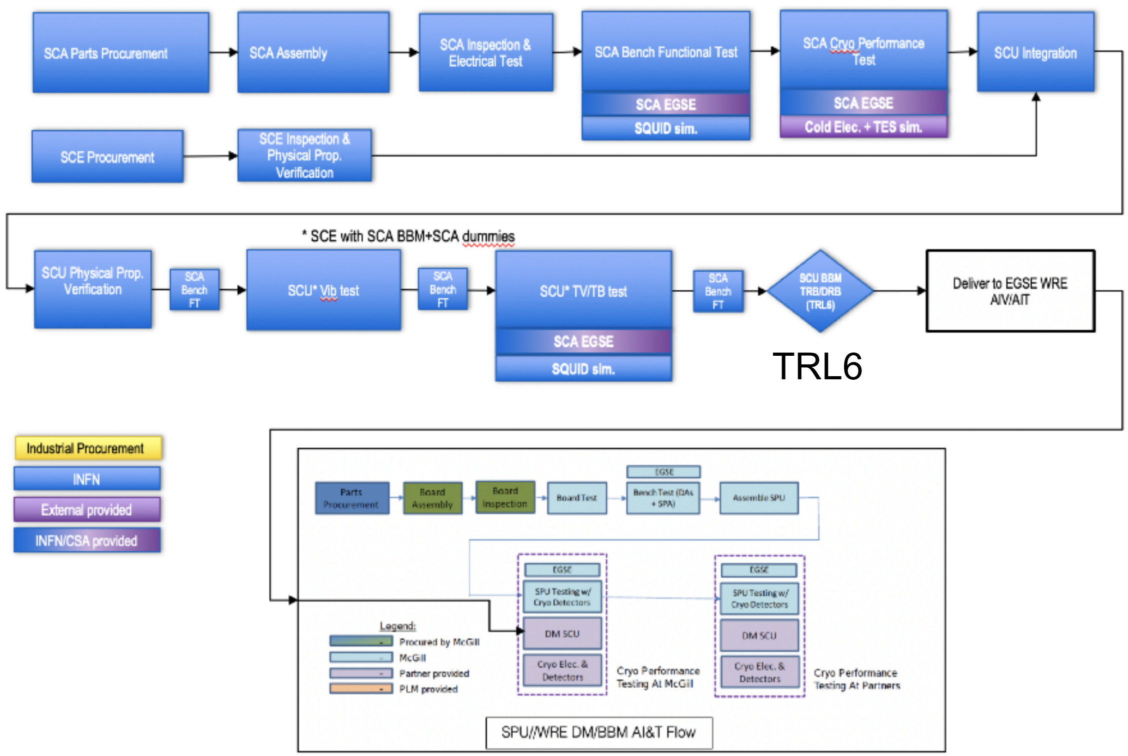


AIV Plan

The SCU AIV/AIT campaign is to demonstrate that:

- the SQUID Controller design at unit level is qualified at the environmental condition;
- the SCU is free from material and workmanship defects;
- the overall SQUID Controller (including procedures and resources) is able to fulfil the mission requirements, providing all the performances requirement during the mission period;
- the SCU verified in conjunction with the other WRE units and LiteBIRD Instruments work properly;
- the Final Model is delivered in due time;

As an example the AIV flow for the BBM shows the matching with CSA AIV flow



SCU AIV Plan

The AIV flow for EM and FM takes in consideration the procurement of the SCAs from industrial partners, while all subsequent activities will be carried out within INFN responsibility.

All the SCU PA/QA matters will be managed by INFN experienced PA personnel following ECSS-Q-ST standards.

The SCU PA/QA manager will act as focal point of the INFN SCU Team for all the PA matters and establish/maintain liaison with the LiteBIRD Italian collaboration (ASI), CNES, CSA and JAXA.

EM AIV

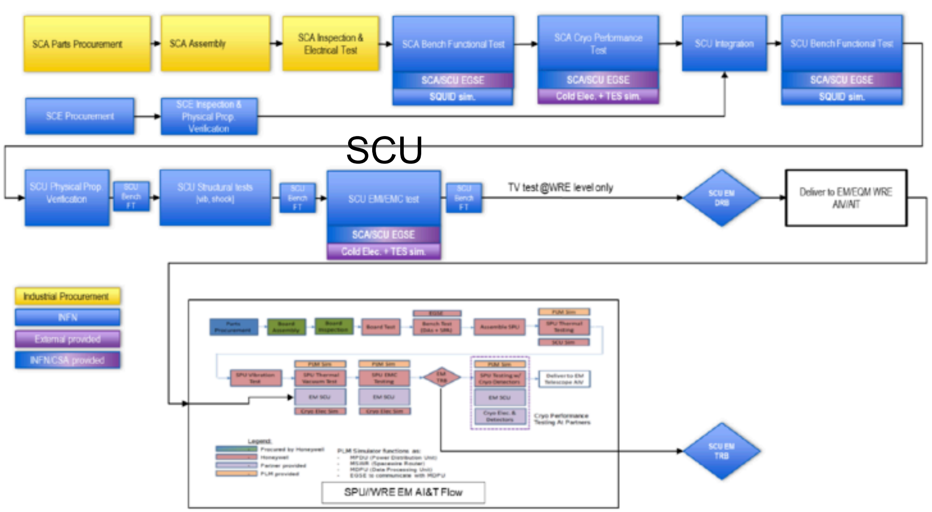


Figure 16. SCU EM alternative AIV Flow (TV test @WRE level only)

FM AIV

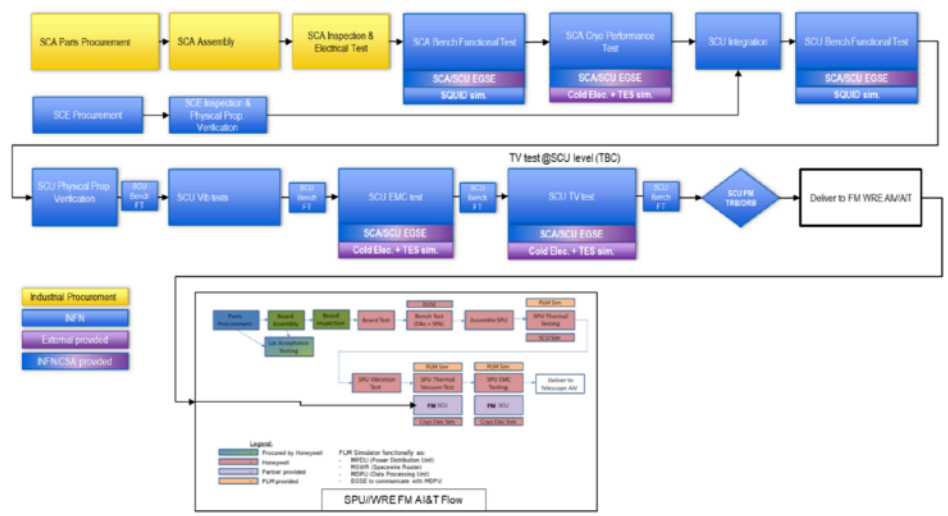
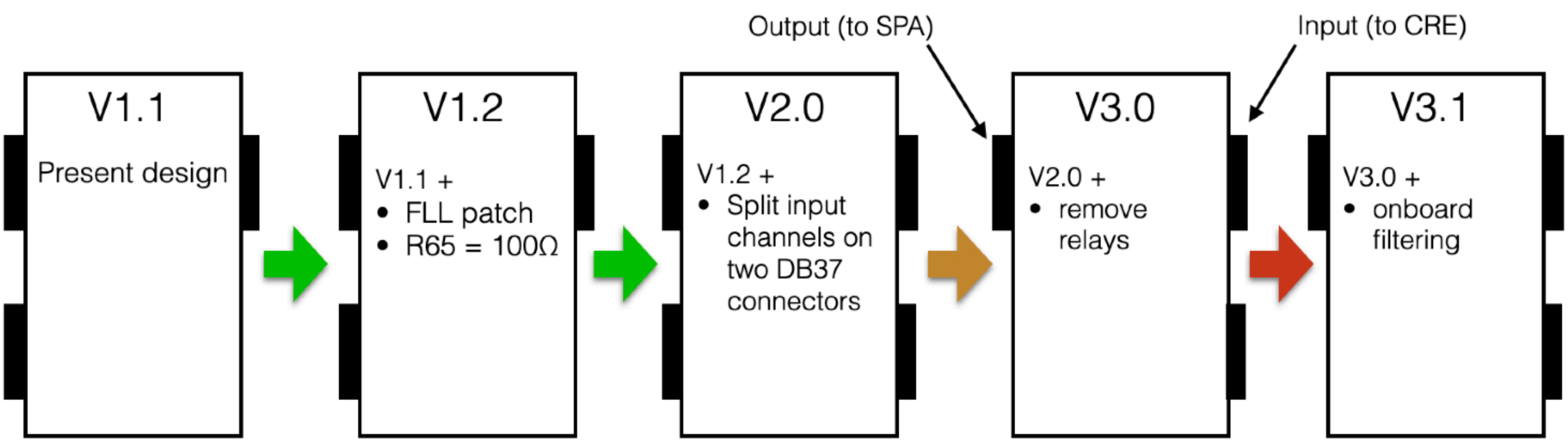


Figure 17. SCU FM AIV/AIT Flow (TV test @SCU level, TBC)

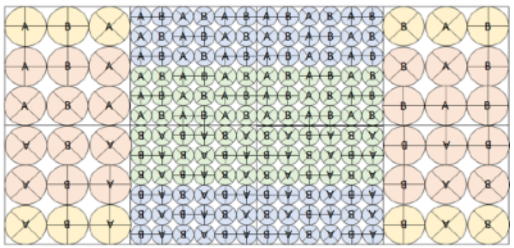
Open points (1)

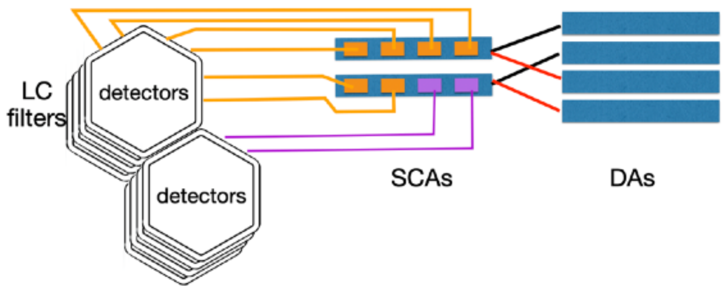
- Discussion on the redundancy policy
  - Functional redundancy instead of performance redundancy
  - Performance = guarantee that we are left with at least 90% of the detectors
  - Functional = allow to lose part of the detectors if we can compensate otherwise (e.g. increasing the observation time)
- Reduces the number of cold/hot spares in the SPUs
- Has implications on the design of the SCA since we need to remove the circuitery that allows the HOT/COLD switch
  - the design, somehow, simplifies
- A decision will be taken after the JAXA MDR (after summer)
- We are anticipating the design modifications to be compliant with the schedule.

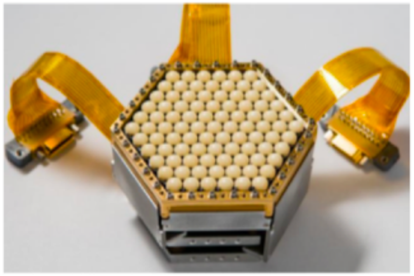


Open points (2)

- Identified some hardware modifications on the SCA boards
  - To match the modularity of the focal planes and independency of “pixels”



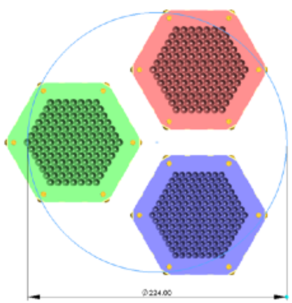




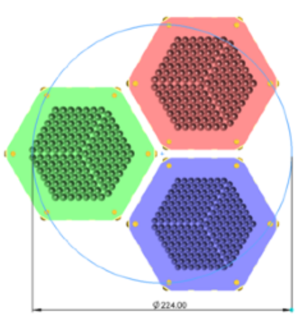
- Increase the number of pixels in HFT
  - Verify that it has no impact on the present readout design

Resource	Design Name	HF1 195/280 GHz	HF2 235/337 GHz	HF3 402 GHz	% Change from PTEP HF1/2/3
Pixel Count	PTEP	127	127	169	
	PPD1	147	147	192	+16/16/14%
	PPD2	162	162	264	+28/28/56%
	PPD3	162	162	330	+28/28/95%
Mux Factor	PTEP	62	62	62	
	PPD1	68	68	66	+10/10/6%
	PPD2	68	68	68	+10/10/10%
	PPD3	68	68	68	+10/10/10%
SQUID Count	PTEP	8	8	6	
	PPD1	9	9	6	+13/13/0%
	PPD2	10	10	8	+25/25/33%
	PPD3	10	10	10	+25/25/60%

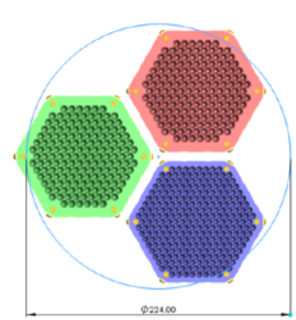
PTEP



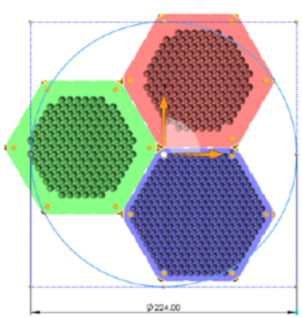
PPD1



PPD2

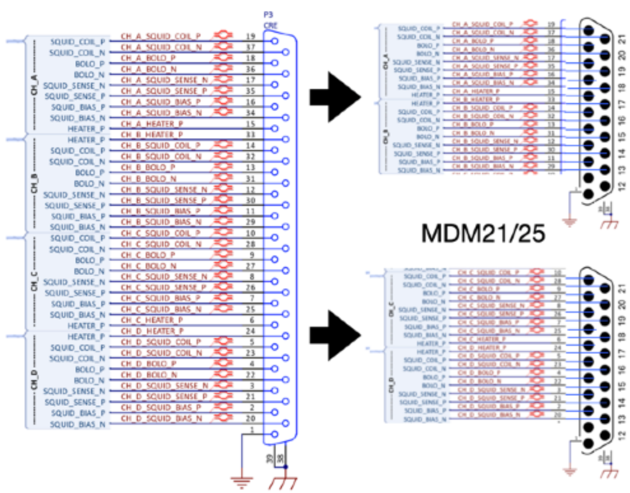


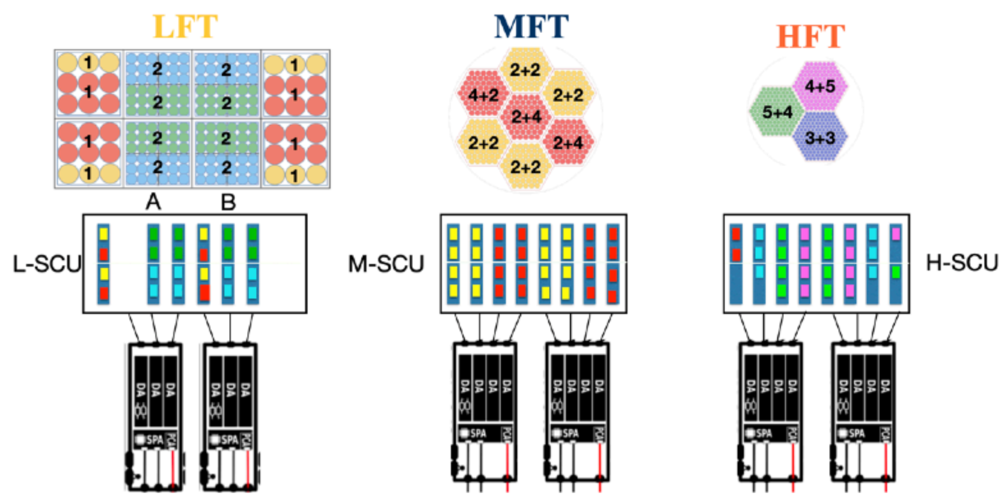
PPD3



Conclusion

- The SQUID Controller Units will be delivered under our responsibility
  - Excellent collaboration with McGill colleagues. Need to interact at "institutional" level
- The design (electrical-mechanical) is well advanced and subject to some decisions from the collaboration
  - Definition of the redundancy policy
  - Modularity of the connections with the focal planes
  - Exact placement on the payload
- TRL advancement is in sync with the schedule
- AIV plan has been envisaged and being sync'd with Canada
  - Test facilities being put in place for cryogenic tests / thermal-vacuum tests
  - Other test activities (cosmic rays, particle flux, etc.)
- We are ready for the end-of-year CNES review
  - Will manufacture three units by the end of the year. Ready to proceed towards phase-B!





SCU workshop LNF 24.5.2023

09:00	**Intro** **Speaker**: Giovanni Signorelli (Istituto Nazionale di Fisica Nucleare)	15m
09:15	**LiteBIRD Readout Chain** **Speaker**: Eugenia Di Giorgi (INFN Pisa)	20m
09:35	**SCU Electronics (design, versions, timeline)** **Speaker**: Andrea Passerini (MIB)	20m
09:55	**TASI Study status** **Speaker**: Mario Zannoni (Istituto Nazionale di Fisica Nucleare)	15m
10:10	**Analysis of McGill Data** **Speaker**: Giulia Conenna	25m
10:35	**SCU mechanics (design, simulations, models)** **Speaker**: Maurizio Massa (INFN Pisa)	20m
11:30	**SCU Tests and qualifications** **Speaker**: Andrea Tartari (Istituto Nazionale di Fisica Nucleare)	20m
11:50	**Schedule, model philosophy, AIV** **Speaker**: Michele Pinchera (Istituto Nazionale di Fisica Nucleare)	25m
12:15	**LNF Thermovacuum facility** **Speaker**: Luca Porcelli (Istituto Nazionale di Fisica Nucleare)	25m
14:30	**Cosmic ray effects and detector test on beamline** **Speakers**: Andrea Tartari (Istituto Nazionale di Fisica Nucleare), Stefano Della Torre (Istituto Nazionale di Fisica Nucleare)	20m
14:50	**Irradiation of LTC1668 at LNL** **Speaker**: Giovanni Signorelli (Istituto Nazionale di Fisica Nucleare)	15m
15:05	**Discussion session**	20m

End of slides

Status of Doc for Phase-A2 Review

The overall status of the WRE documentation is very good. Minor syncronizations may be needed following ongoing tests/design optimizations.

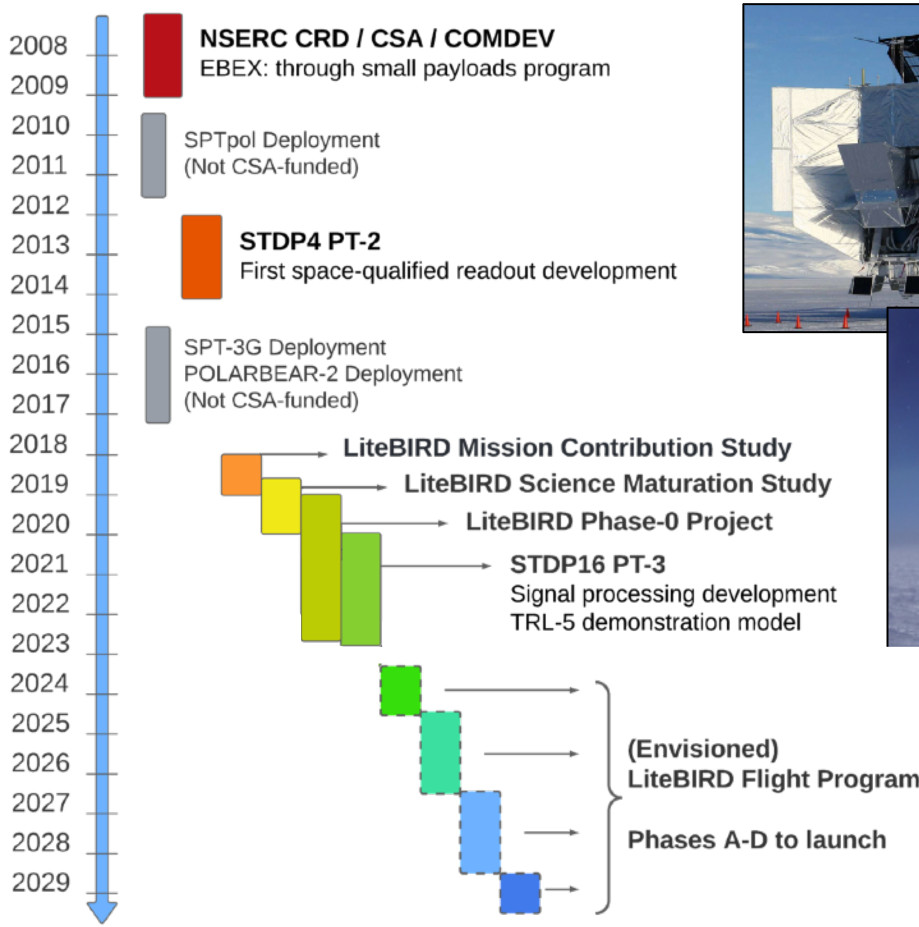
Sub-systems	Design Definition and Justification TRL achievement	Technical Budget (mass, thermal, electrical, data)	AIV Plan Only AIV flow for each model as given in 2021_11_18_MHFT_models&schedule.pptx	Development Plan (Models & Schedule)	Breadboard Test results	Requirements Specification
WRE (SPU)	OK	OK (SPU)	minor sync	minor sync	OK	minor sync
WRE (SCU)	OK	OK	minor sync	minor sync	Minor refinements	minor sync

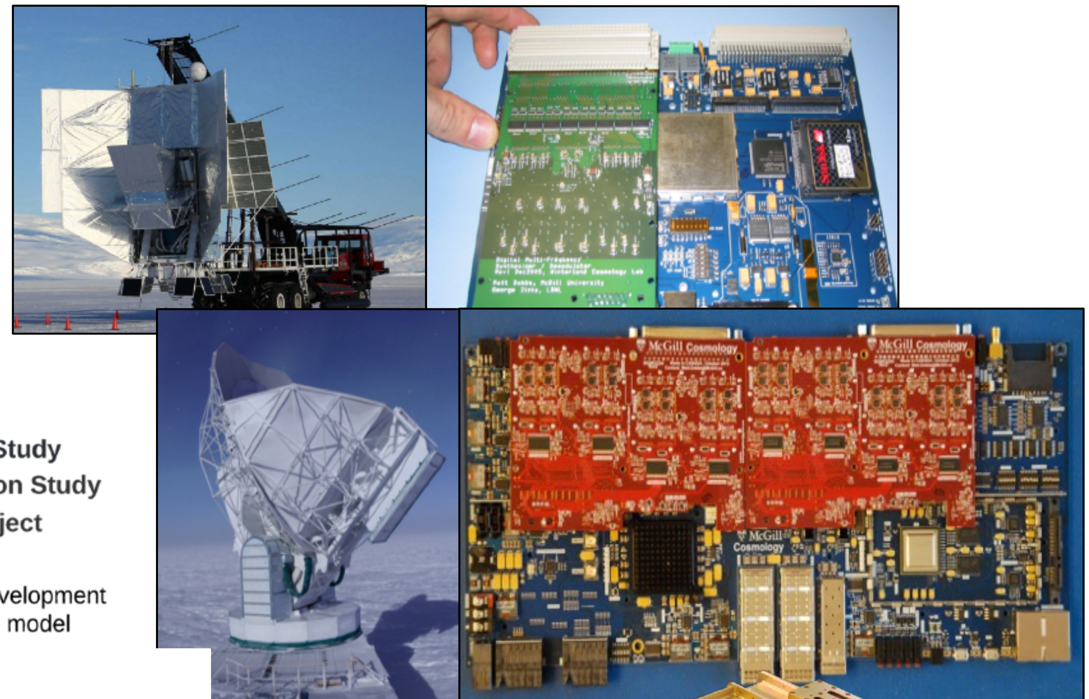
Delivered documentation for the KP:

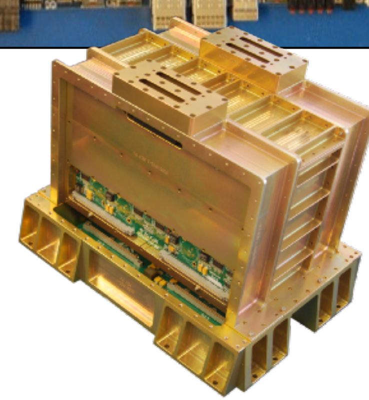
/Warm Readout Electronics			
	LBRD-DD-001-LiteBIRD-Warm-Readout-Design-Description v1.0	Mc Gill WRE Design	Final
	LBRD-RPT-002-Warm-Electronics-Development-Plan	Mc Gill WRE Dev Plan	Final
	LBRD-IRD-001-LiteBIRD-Warm-Readout-IRD v2.4	Mc Gill WRE IRD	Final
	LBRDSTDP RPT10 Honeywell Vibration and Thermal Cycling Tests (2021)	Mc Gill SPU TRL5 Verification: Vibration and Thermal cycling tests	Final
	LBRDSTDP RPT06 McGill TRL5 Verification Summary (2021)	Mc Gill SPU TRL5 Verification Summary	Final
	TF of SQUID Control Unit_V1_for_CNES_KP	Technical Feasibility for SQUID Control Unit	KP version
	RPR-LB20005_WRE_IRD_rev2.0_INFN-commented	WRE JAXA IRD	KP version
	List_of_JAXA-INFN-comments_to_RPR-LB20005_WRE_IRD_rev2.0_20230128	Comments to WRE JAXA IRD	KP version

Canadian Space Agency development of WRE/SPU

TRL-5 status is the product of long development effort



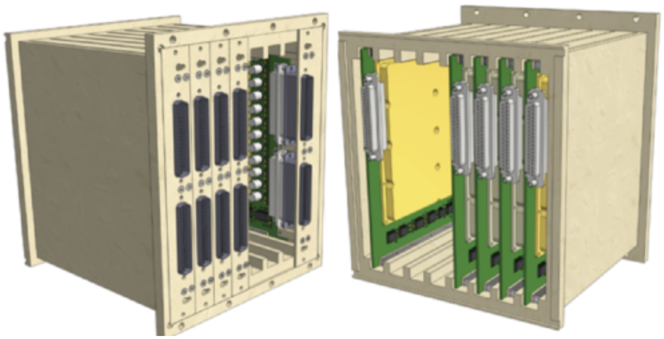




SCU Technical Budget

Mechanical and electrical budgets were evaluated by analysis and design and validated after the construction of a prototype enclosure + SCA breadboard, which is form-fit to the flight model.

Mass, form factor, volume and electrical power dissipation of our prototype model are within this subsystem allocated envelope.



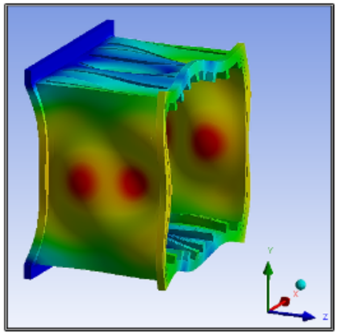
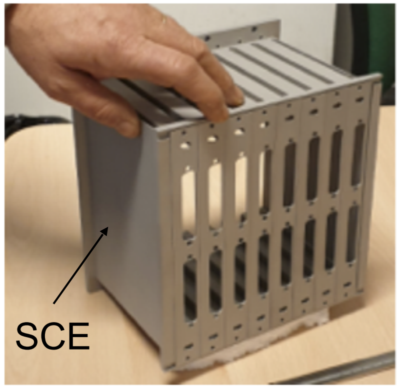
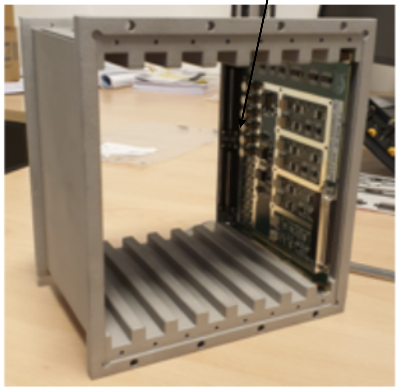


Figure 11 - Major Z mode (Mode 37), 4582,88 Hz

200mm×250mm×200mm.





Main Component	Component	Qty	Mass, CBE [kg]	Partial Mass, CBE [kg]	Main component Total mass, CBE [kg]	Contingency	Mass, MEV [kg]	Main Component Quantity	Total Mass, MEV [kg]
SCU-L	SCU Mechanics (Chassis, Frontal panel, Back Panel)	1	2	2	5	20%	6	1	6
	Boards	6+2	0.21	1.68					
	Card-locks	16	0.025	0.4					
	Emi Shield and EMI clamps	8	0.115	0.92					
SCU-M	SCU Mechanics (Chassis, Frontal panel, Back Panel)	1	2	2	5	20%	6	1	6
	Boards	8	0.21	1.68					
	Card-locks	16	0.025	0.4					
	Emi Shield and EMI clamps	8	0.115	0.92					
SCU-H	SCU Mechanics (Chassis, Frontal panel, Back Panel)	1	2	2	5	20%	6	1	6
	Boards	8	0.21	1.68					
	Card-locks	16	0.025	0.4					
	Emi Shield and EMI clamps	8	0.115	0.92					

Table 1 Mass budget

Component	# of boards	Dissipated power per board, CBE [W]	Total power to dissipate, CBE [W]	Contingency	Total Dissipated power, MEV [W]
SCU-L	6	1.65 (TBC)	9.9	20%	11.9 (TBC)
SCU-M	8	1.65 (TBC)	13.2	20%	15.9 (TBC)
SCU-H	8	1.65 (TBC)	13.2	20%	15.9 (TBC)
Total					43.6 (TBC)

Table 2 Thermal power budget

Component	# of boards	Electrical power per board, CBE [W]	Total power , CBE [W]	Contingency	Total Electrical power, MEV [W]
SCU-L	6	1.65	9.9	20%	11.9
SCU-M	8	1.65	13.2	20%	15.9
SCU-H	8	1.65	13.2	20%	15.9
Total					43.6

Table 3 Power budget