Front-end electronics
For FD2 X-Arapuca tests

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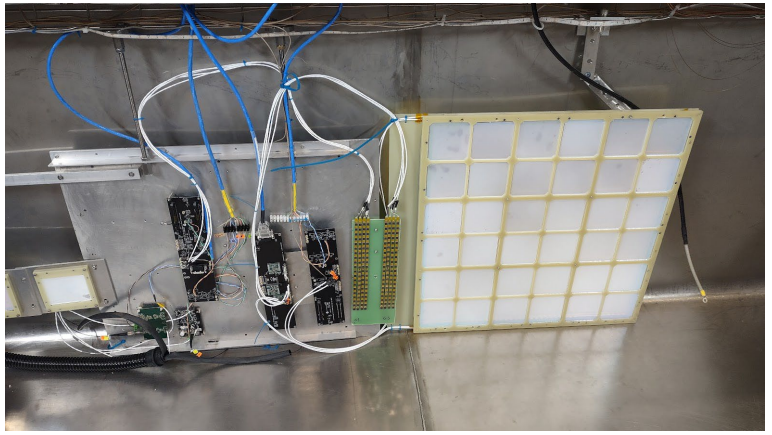
P. Carniti, C. Gotti, E. Cristaldo, G. Pessina, F. Terranova
INFN/Univ. Milano-Bicocca

Membrane cold electronics

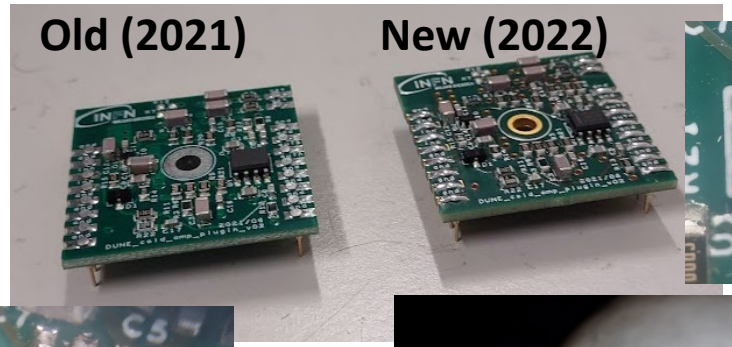


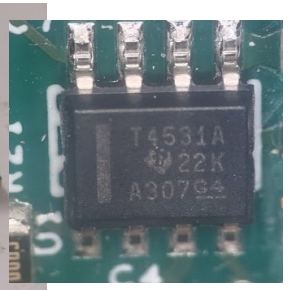
DMEM 1.0 4-channel motherboard designed at FNAL EDMS 2795424

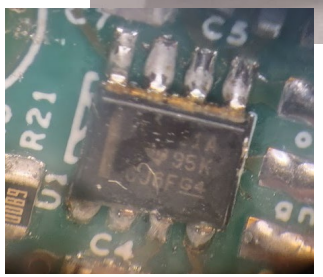
- **3@CERN** (in use), **7@MiB** (of which 2 in use)
- Changes w.r.t. EDMS schematic: Rf=1.2k instead of 2k (2 resistors per channel)
- Change propagated to all boards (except M1 M2 in module 0)

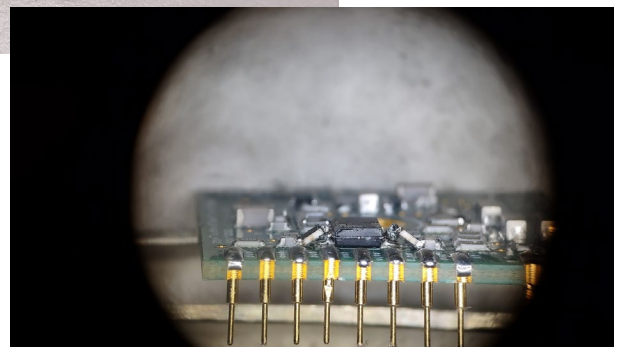
HD-style amplifiers: same as horizontal drift EDMS 2805804

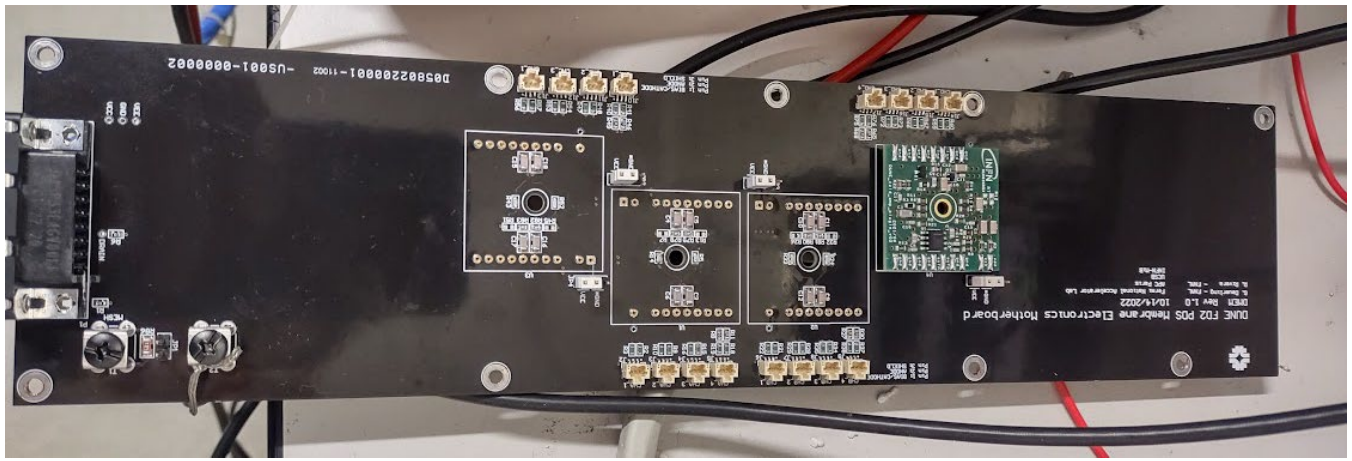
- **8(new)@MiB** (of which 4 in use), ≈**15(old)@CIEMAT**, a few(?)@CERN (not all in use)
- 50 ohm resistors must be added in series with the THS4531 outputs to prevent instabilities with large (>390 ohm) feedback resistors; likely not necessary with old amplifiers (old batch of THS4531)







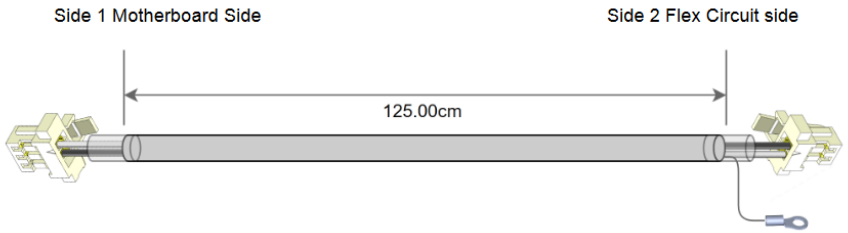




Cables

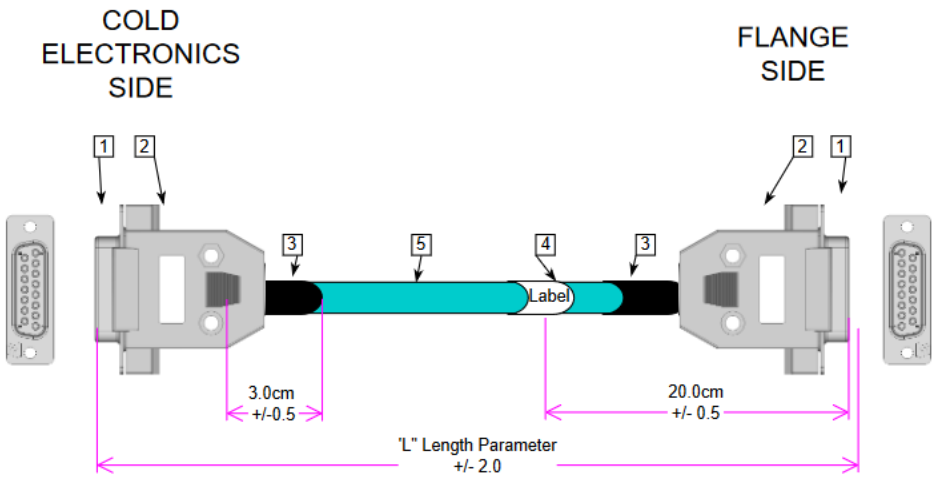
Between flex and DMEM: EDMS 2815448

- White «coaxial» cables (actually 2 conductors + shielding), about 1m long
- Made/ordered by FNAL
- Included in mounted Arapucas (?)



Between DMEM and warm: EDMS 2815464

- Blue superior essex cable (same as HD)
- DSUB15 connectors at both ends (differs from HD)
- Cold side: female/female
- Warm side: female/male

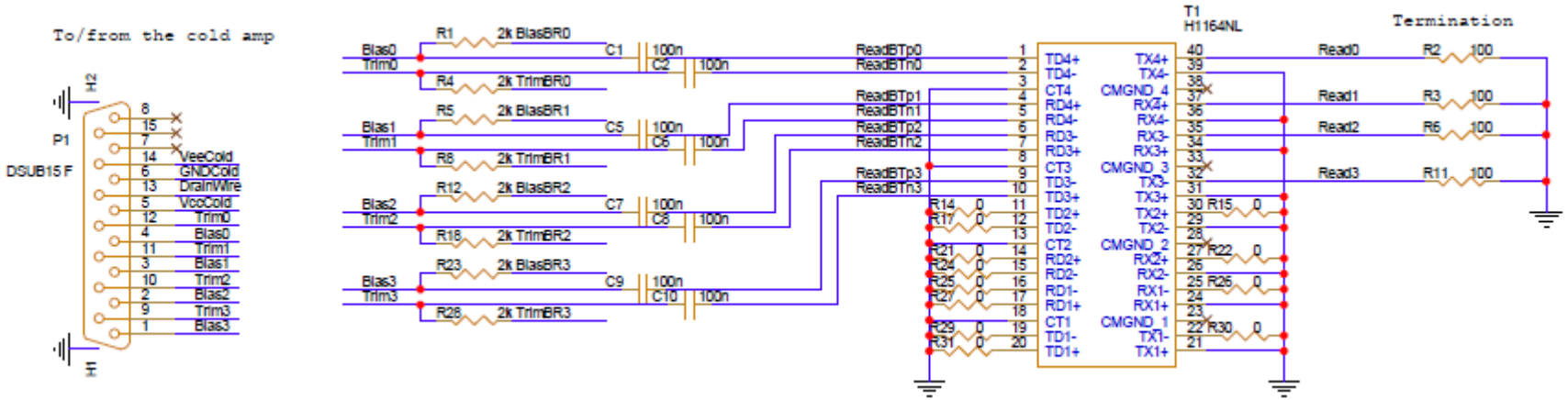


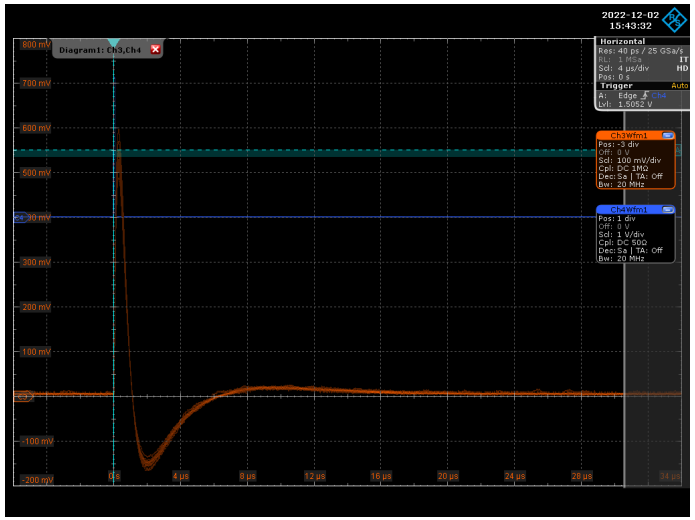
NIOBE-VD flange: EDMS 2802472

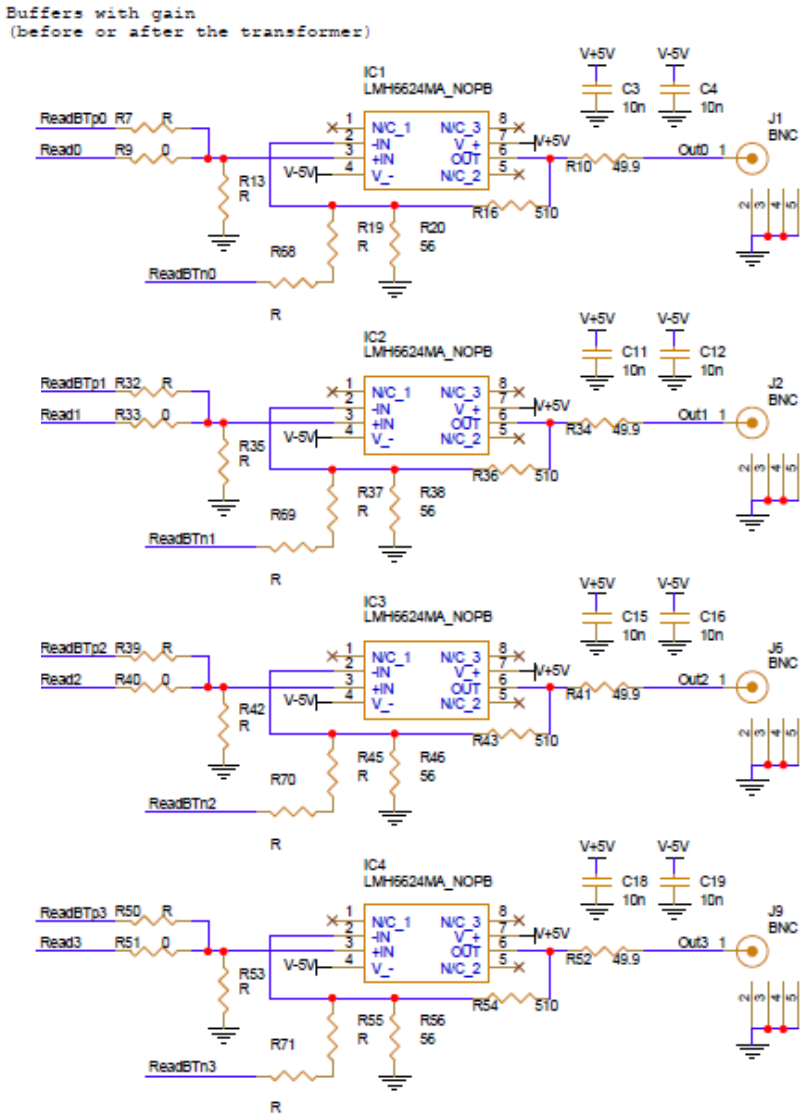
- Male DSUB15 connectors on both sides
- Designed by Jon Ameel (UMich), in use at CERN
- Don’t know if available for other labs

Warm second stage v1

- «Sold out» (a few boards in some labs, but we don't have anymore)
- Undershoot ≈25% mainly due to input transformer
- Same as unmodified DAPHNE V2A
- There are ways to reduce undershoot with the transformer, studied by Esteban, not applied here

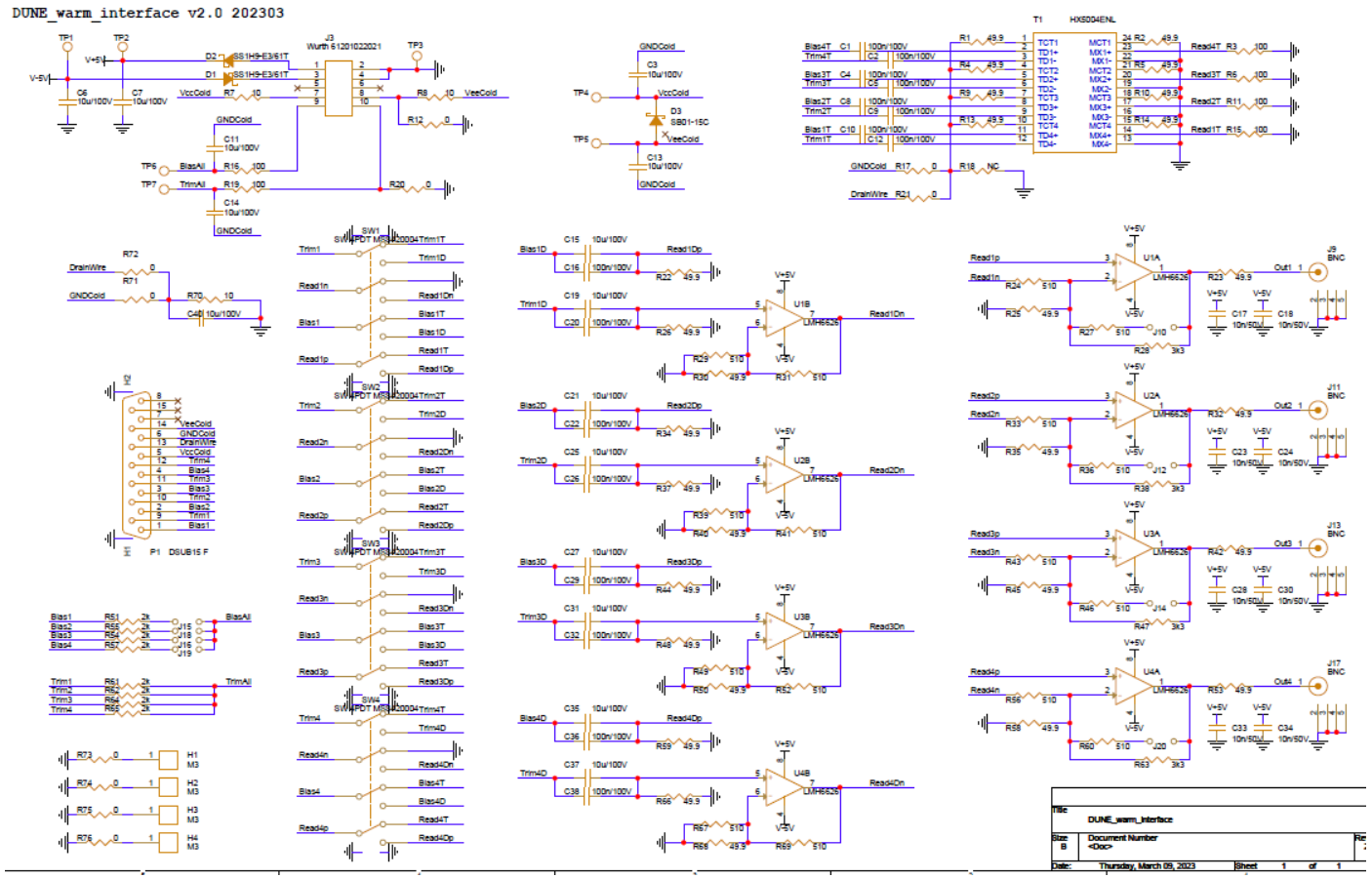


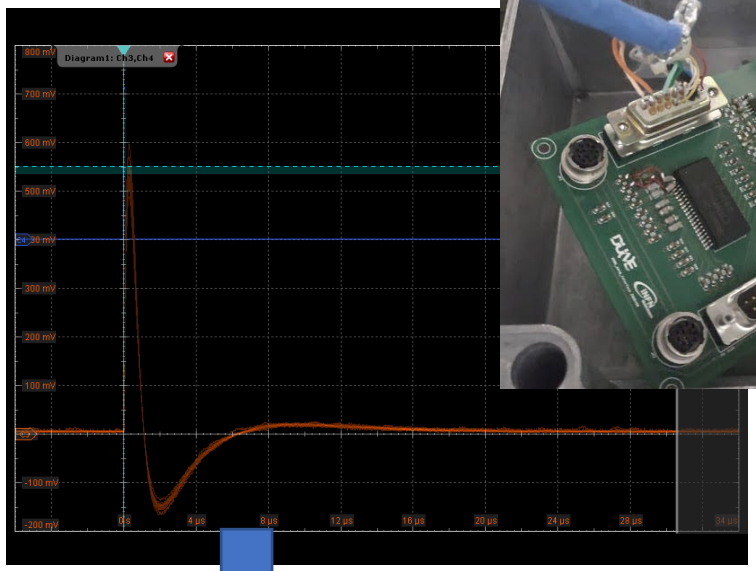


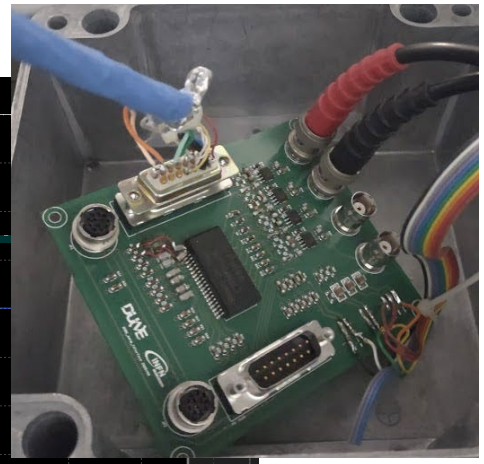


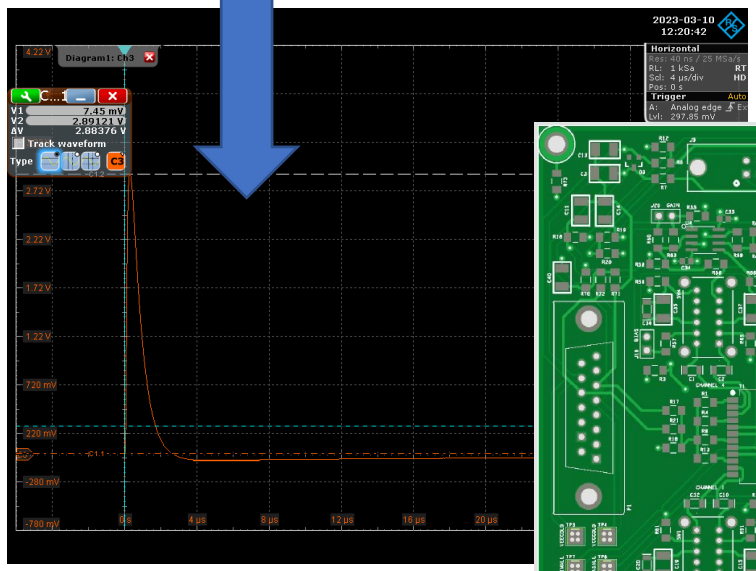
Warm second stage v2

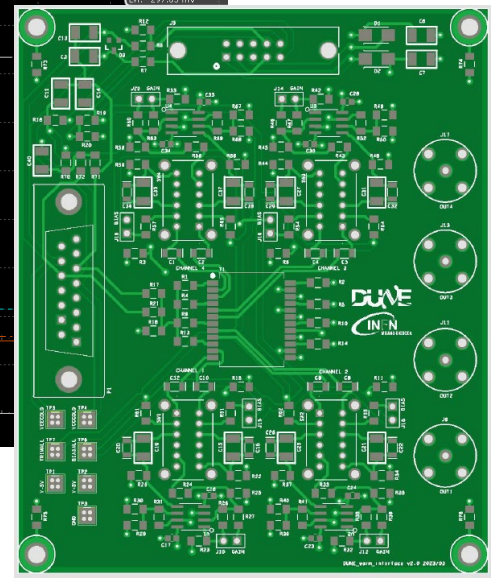
- 10 populated boards ordered, expected by mid may
- Two options:
  - Transformer as DAPHNE v3 (undershoot down to ≈8%)
  - Transformer bypassed, AC coupled w large caps, undershoot ≈3%





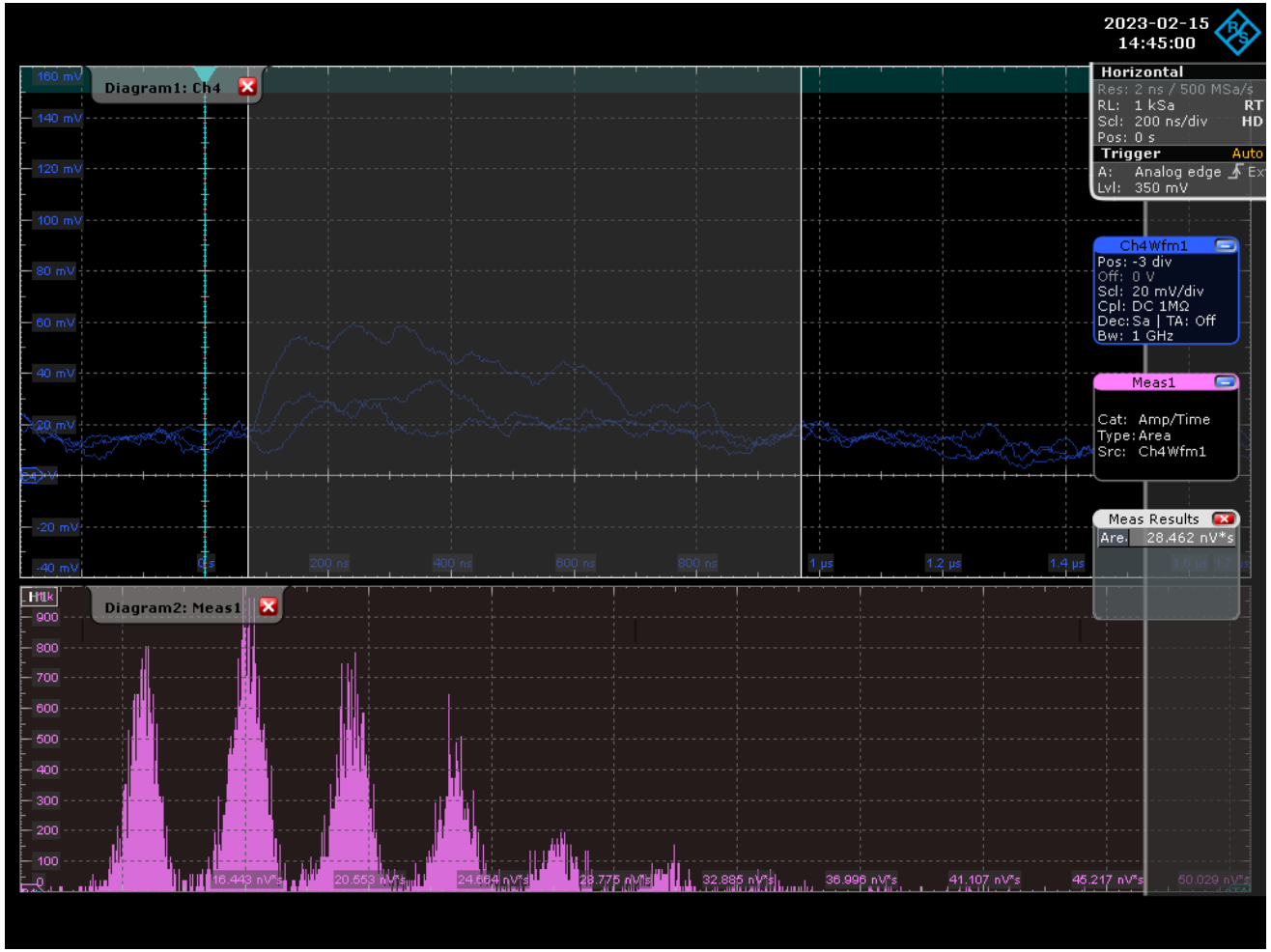






Expected performance

- S/N≈8 with HPK SiPMs at 45V in LN2 (+3Vov)



Lab instruments

- 0-60 V power supply for SiPM bias (current ≈ negligible; better if low noise)
- 3.3V power supply for the cold amplifier (current ≈ 1mA / cold amplifier)
- +5V/-5V supply for the warm amplifiers (current ≈ 100 mA for the warm second stage v2)
- Oscilloscope or digitizer
- Pulsed LED

Other readout options?

DAPHNE

- Needs effort to setup and operate
- Limited availability
- Less flexible than oscilloscope
- Makes sense only if one needs to acquire more than 4 channels at a time

Cathode electronics

- DCEM motherboard (several versions exist)
- Power over fiber (source+receiver)
- Signal over fiber (source+receiver)
- DCDC for SiPM bias voltage → fixed bias voltage (in most cases)