CLEOPATRA Review

Haspide WP2

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23/03/2023

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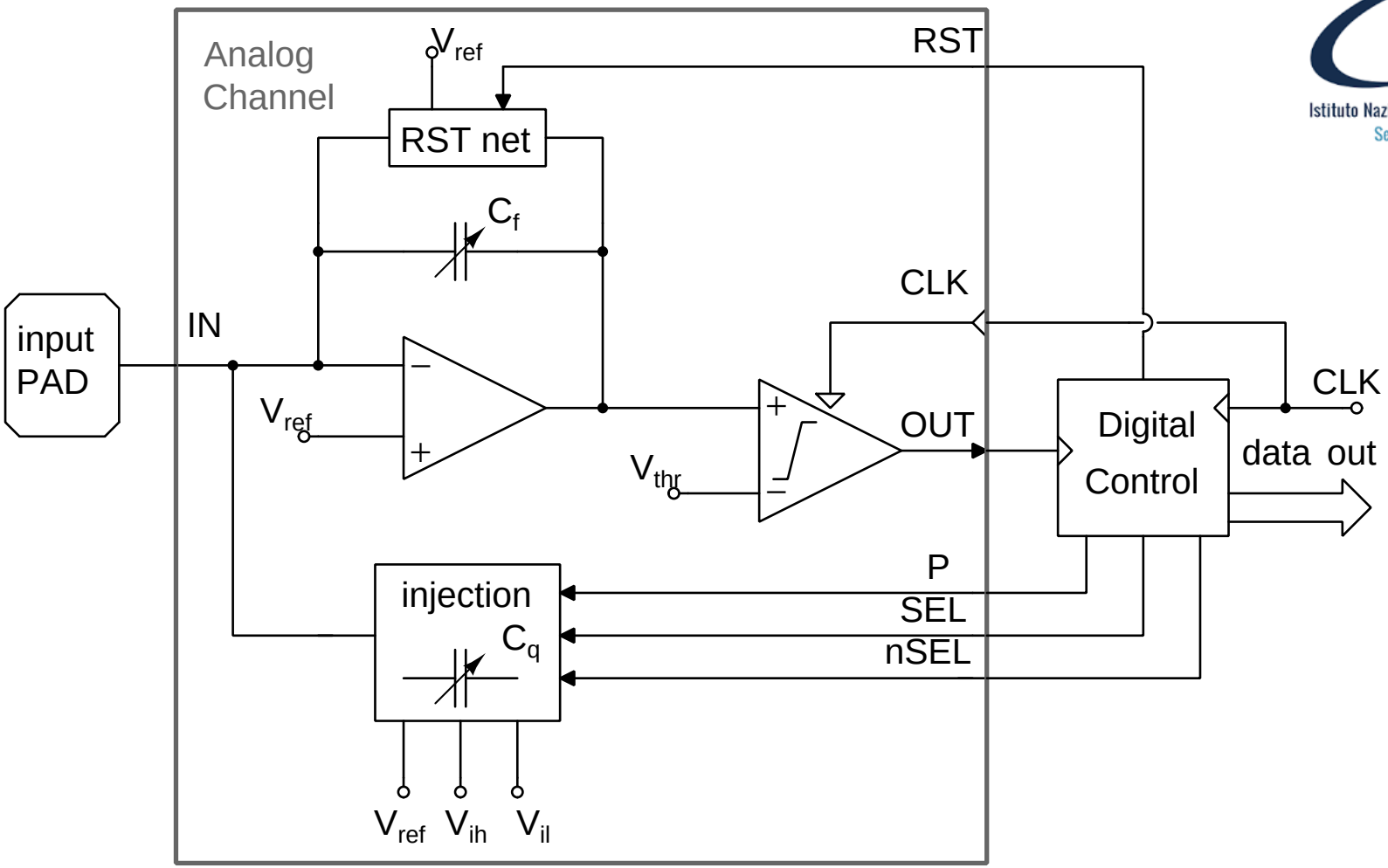
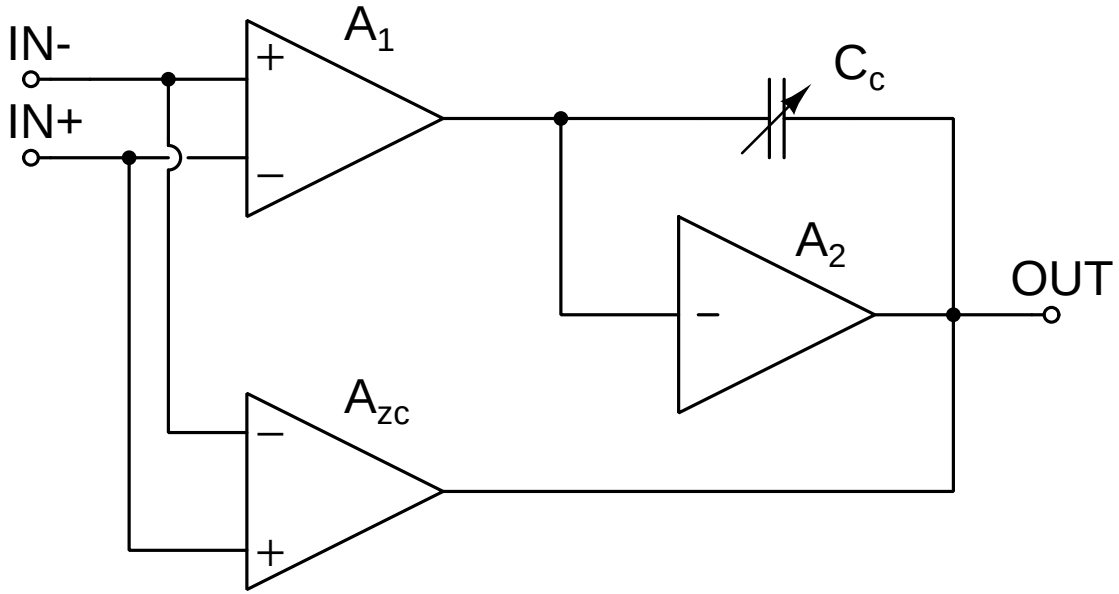
Architecture



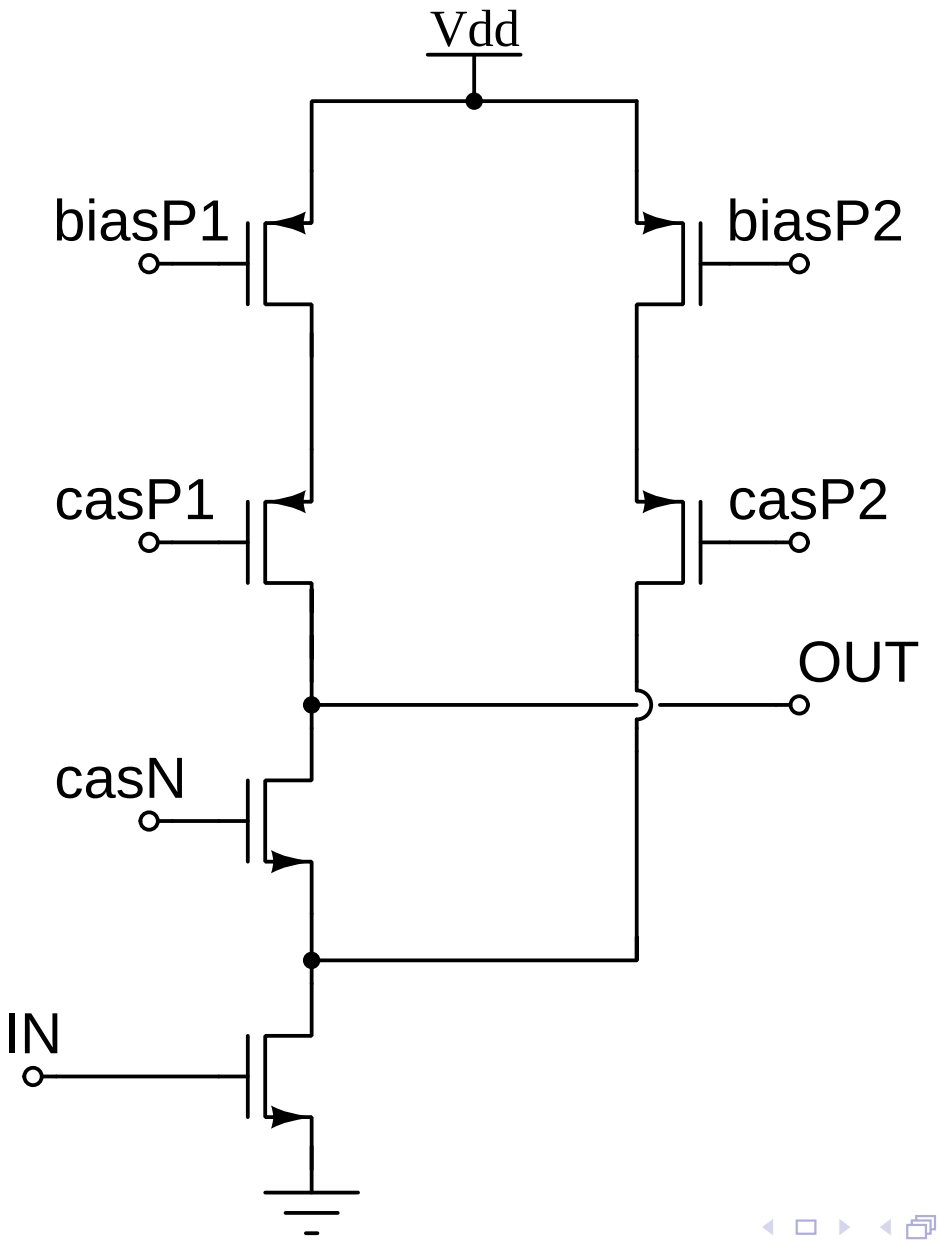
- 3 versioni del CSA.
- 1 solo discriminatore (!) (vedremo dopo).

Opamp with active feed-forward current compensation (ZC)

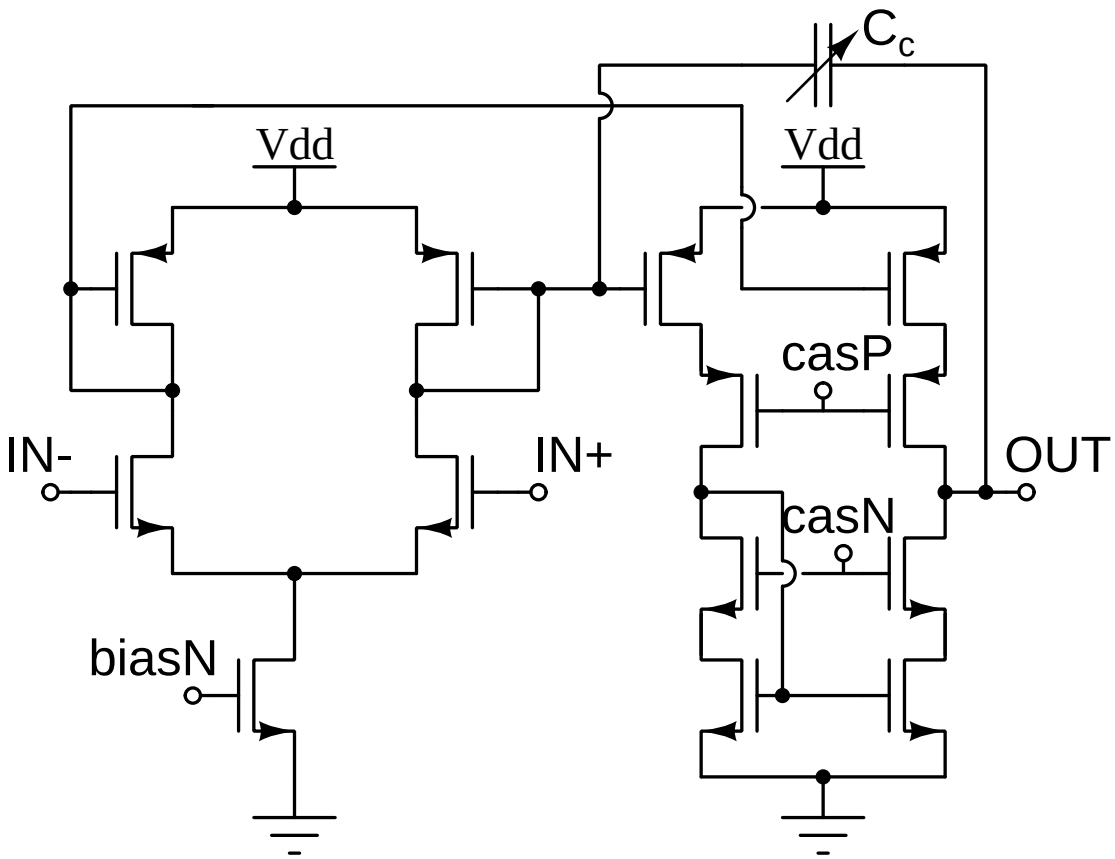


- Two stages.
- Output stage with split bias current to increase gain.
- ZC amplifier to compensate feedforward current and increase phase margin.
- Power $\rightarrow$ 97 µW.

Telescopic Cascode Amplifier with Split Bias Current

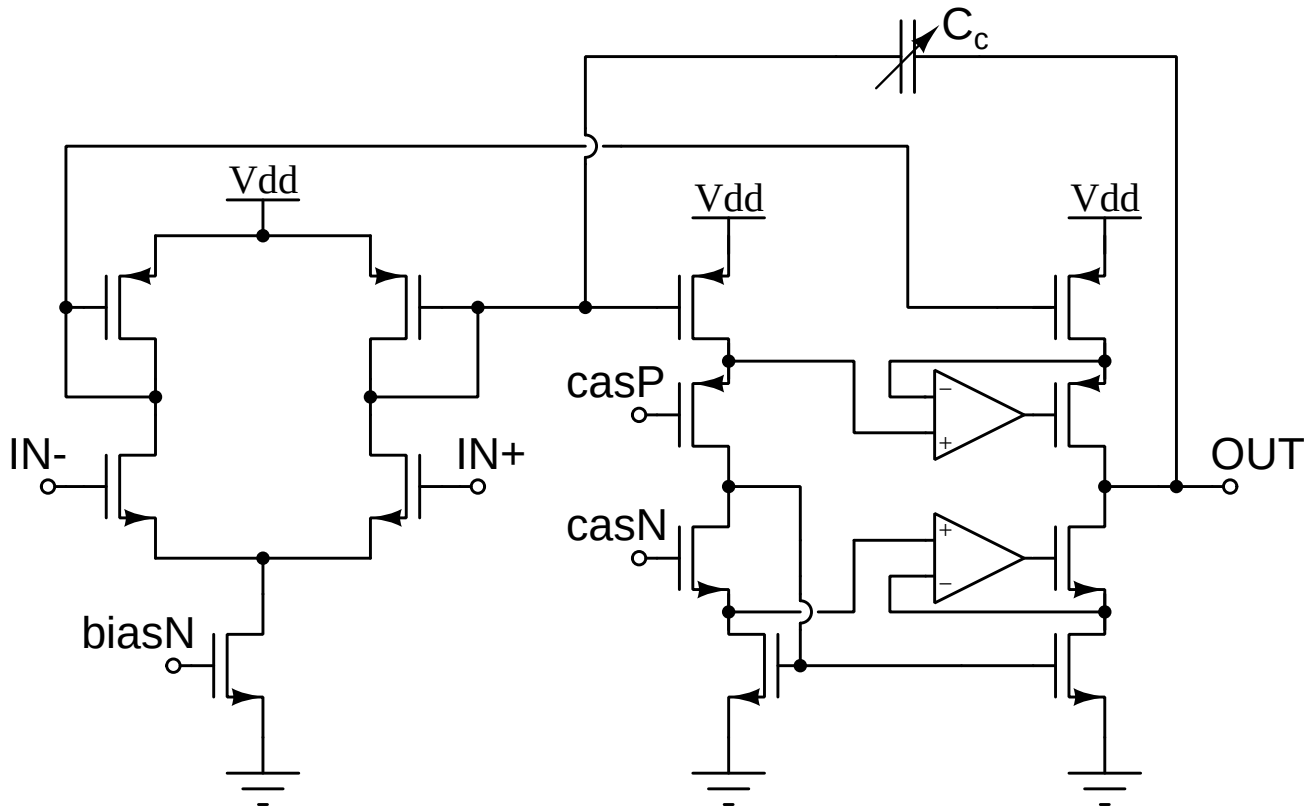


Two stage Opamp class AB (G)



- Two stages.
- Output stage cascoded.
- Lower gain higher band-width.
- Power $\rightarrow$ 30 µW.

Two stage Opamp class AB with Gain Boosting (GB)



- Two stages.
- Output stage cascoded.
- Gain Boosting $\rightarrow$ increases gain decreases band width
- Power $\rightarrow$ 90 µW.

Bode diagram Comparison

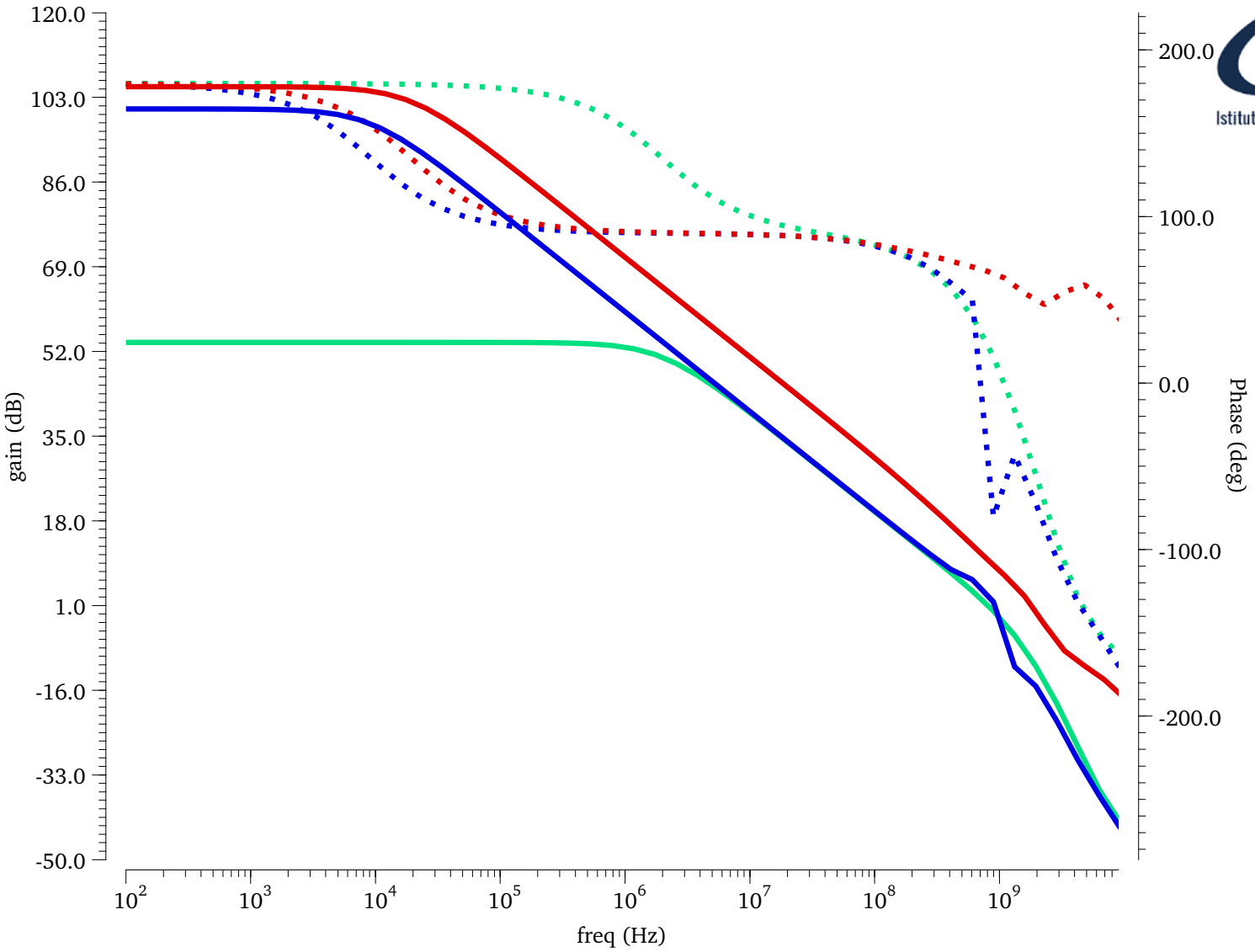


Figure: solid gain, dotted phaseZC G GB

BW and Phase Margin versus C_c

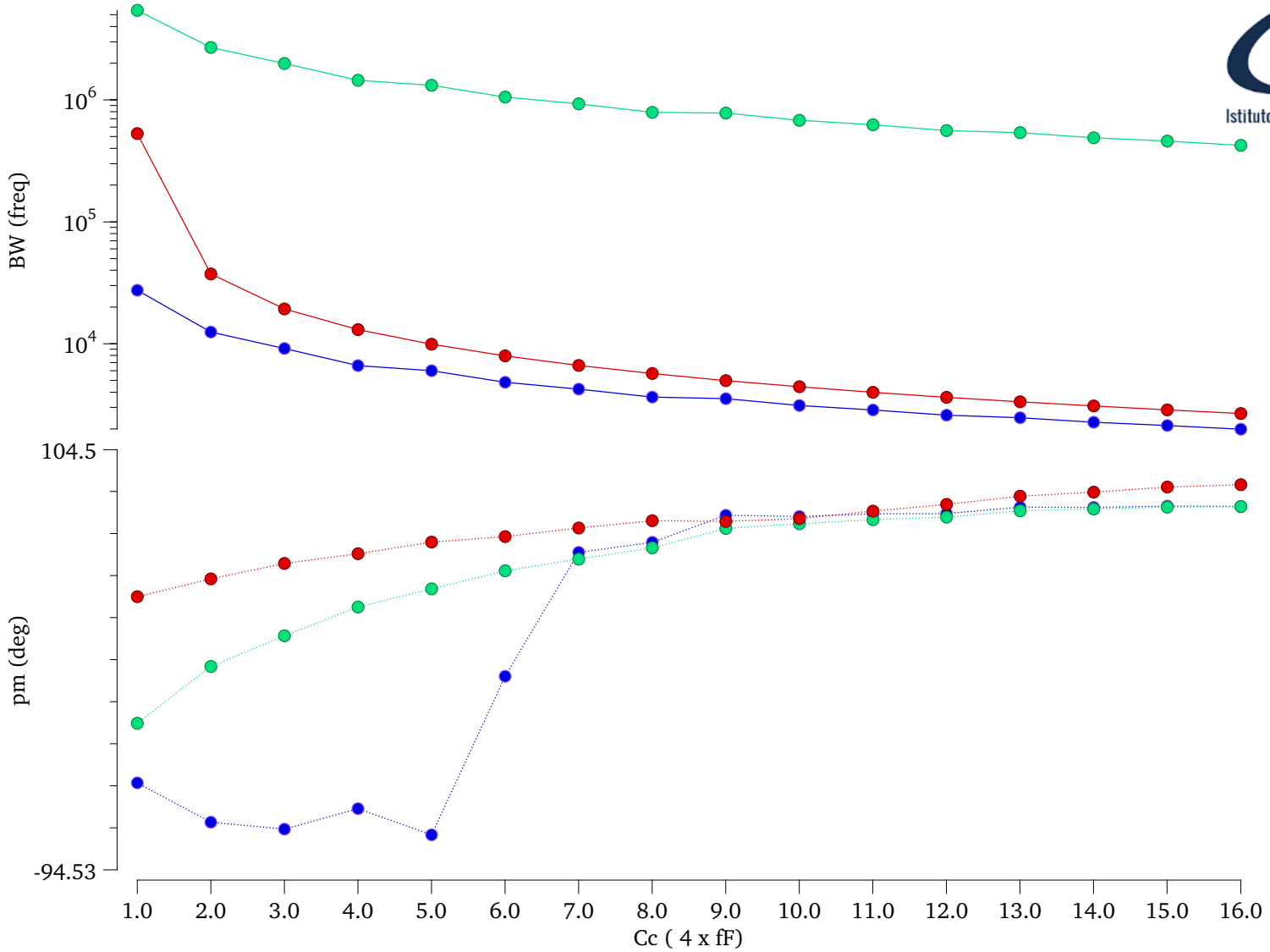
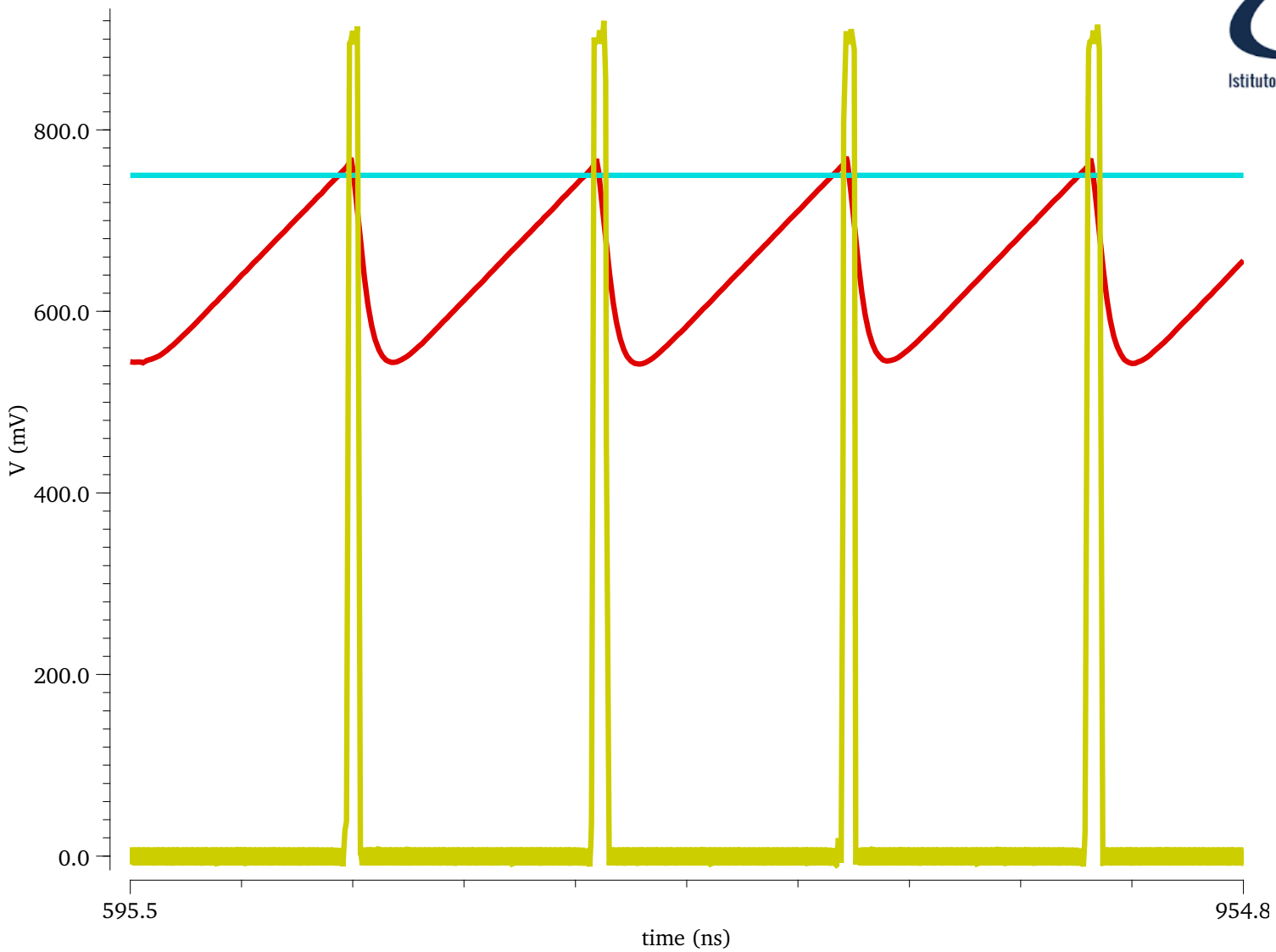


Figure: ZC G GB

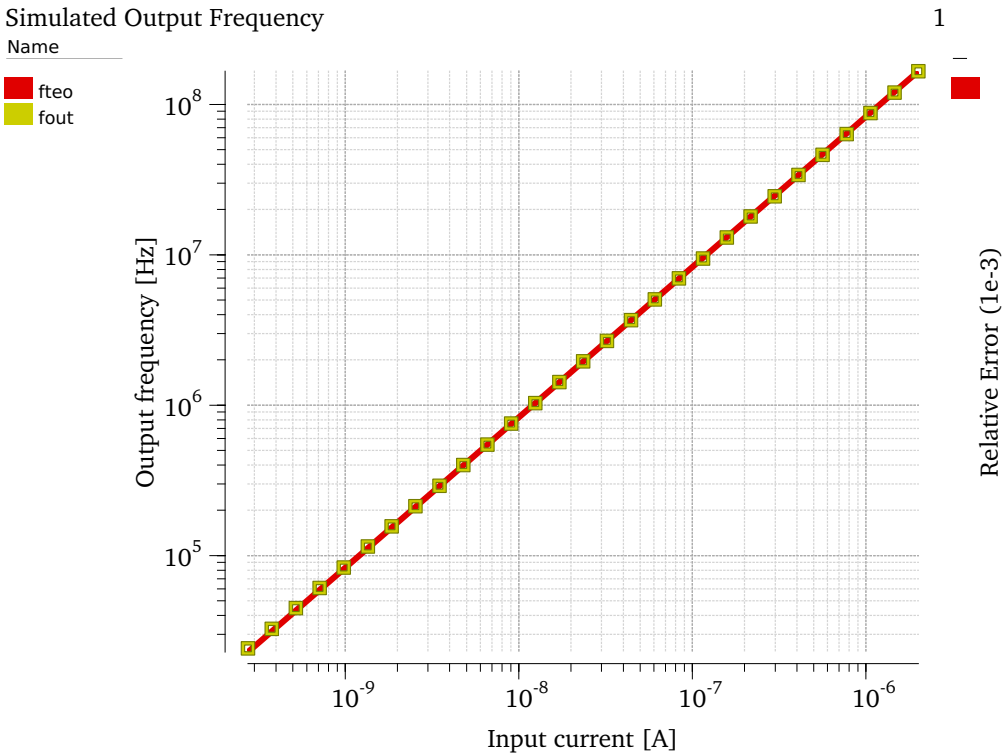
Programmable Capacitors

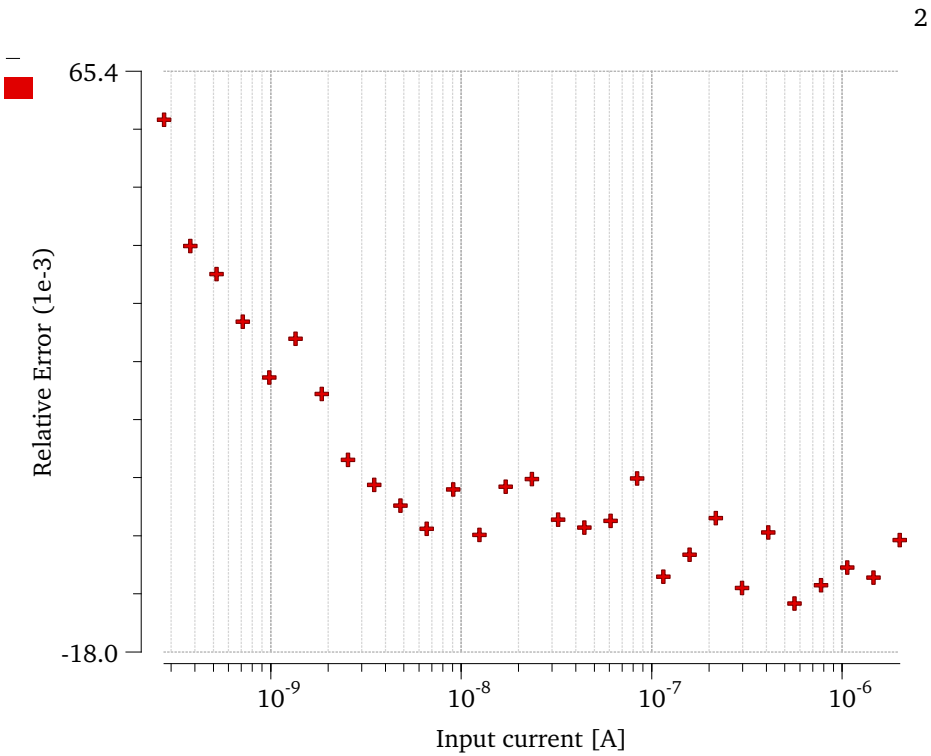
cap	nob	lsb	min	max
		fF	fF	fF
C_c	4	4	0	60
C_f	3	20	0	140
C_q	3	20	0	140

Operation Example



Simulated performance of ZC

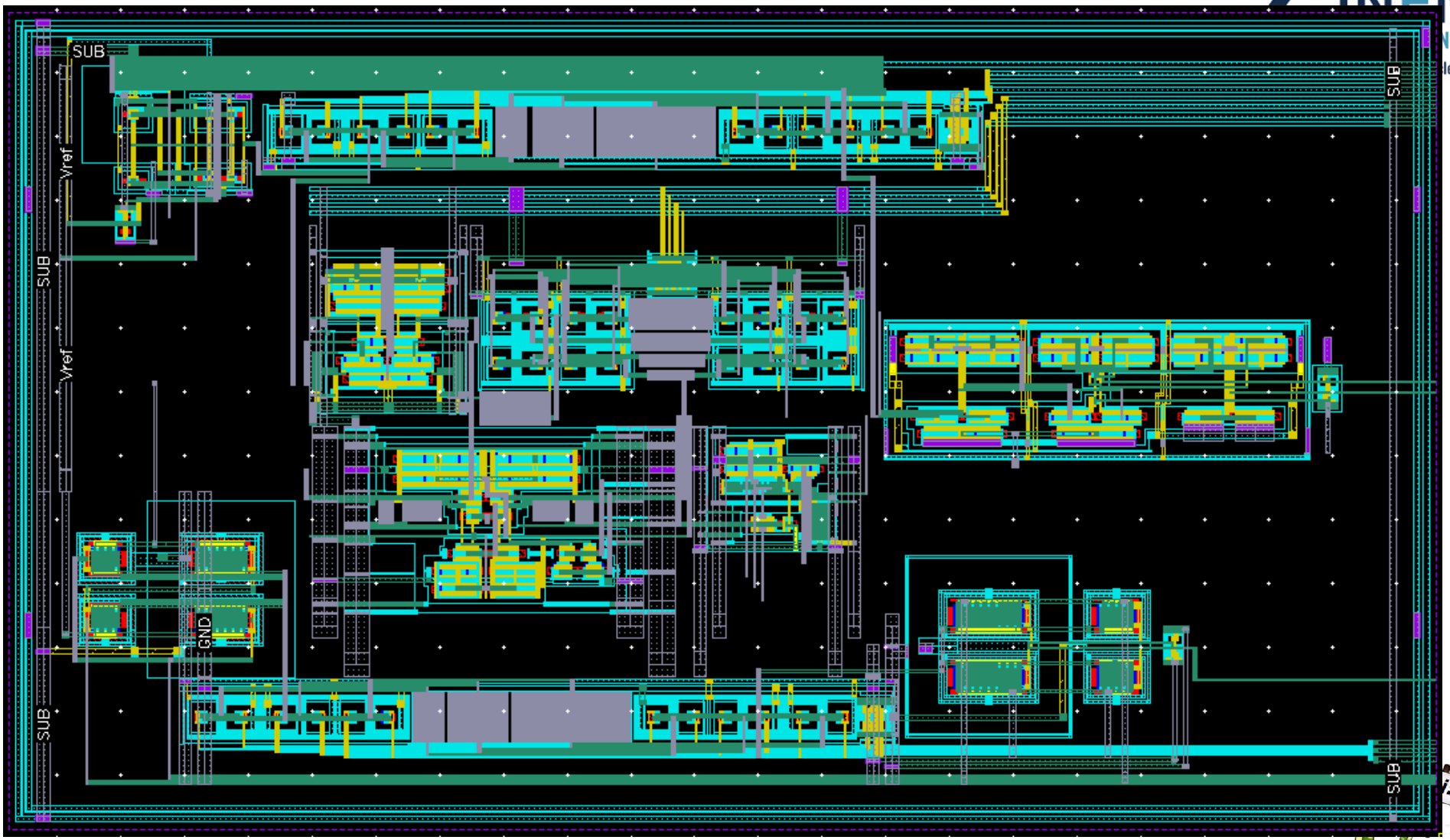




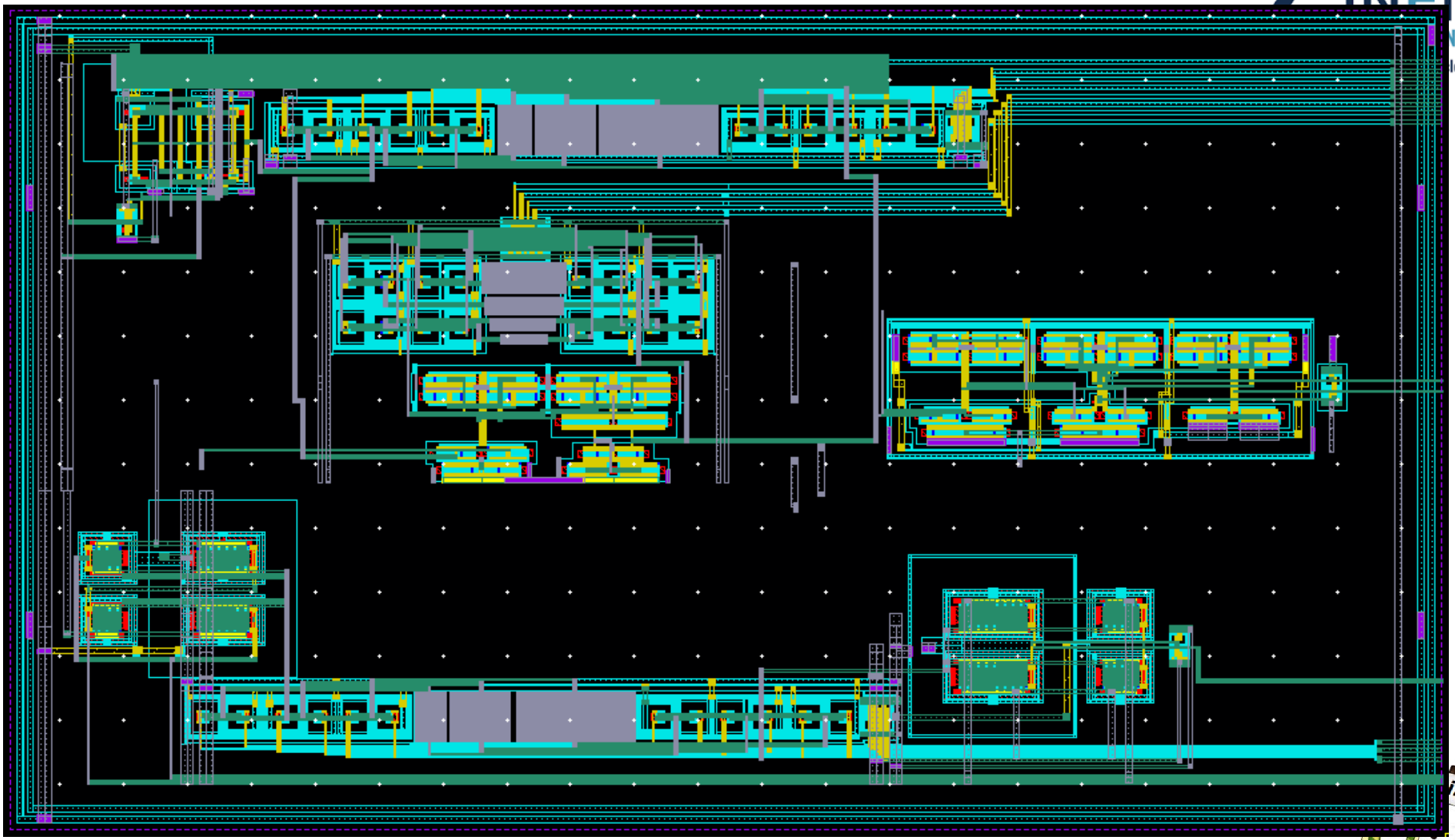
Generalita' Layout

- Area $\rightarrow$ 112 µm $\times$ 64 µm.
- M1 guard ring, Mpari verticali, Mdispari orizontali.
- Interconnessioni per accostamento N-S (tensioni esterne).
- Power in griglia M7-M8, 8 µm $\times$ 8 µm, grid 16 $\times$ 16.
- Inuput a sinistra M5.
- Destra: output M5, bias "privati" M5, controllo digitali (solo input) M3.

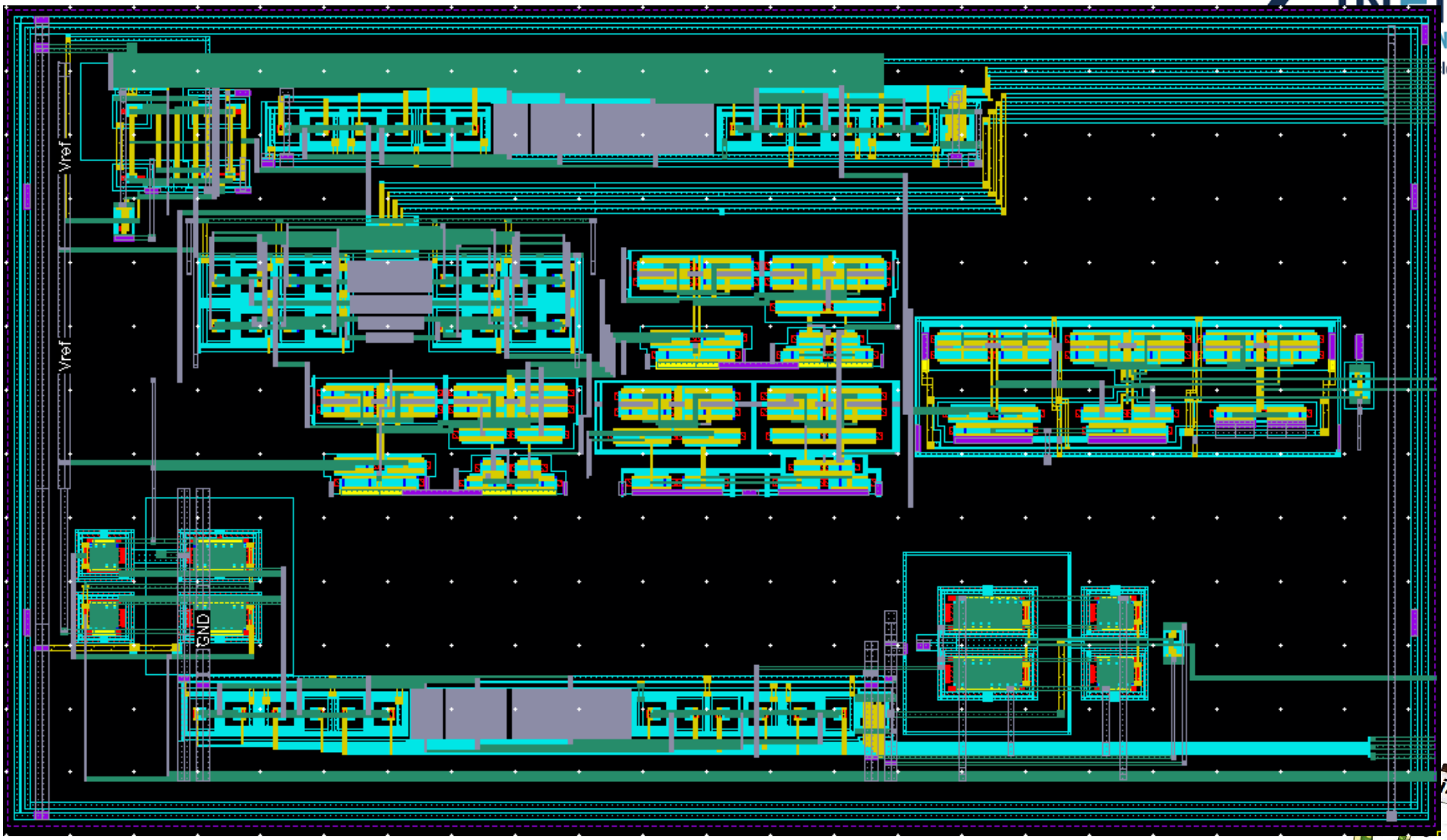
Layout of ZC



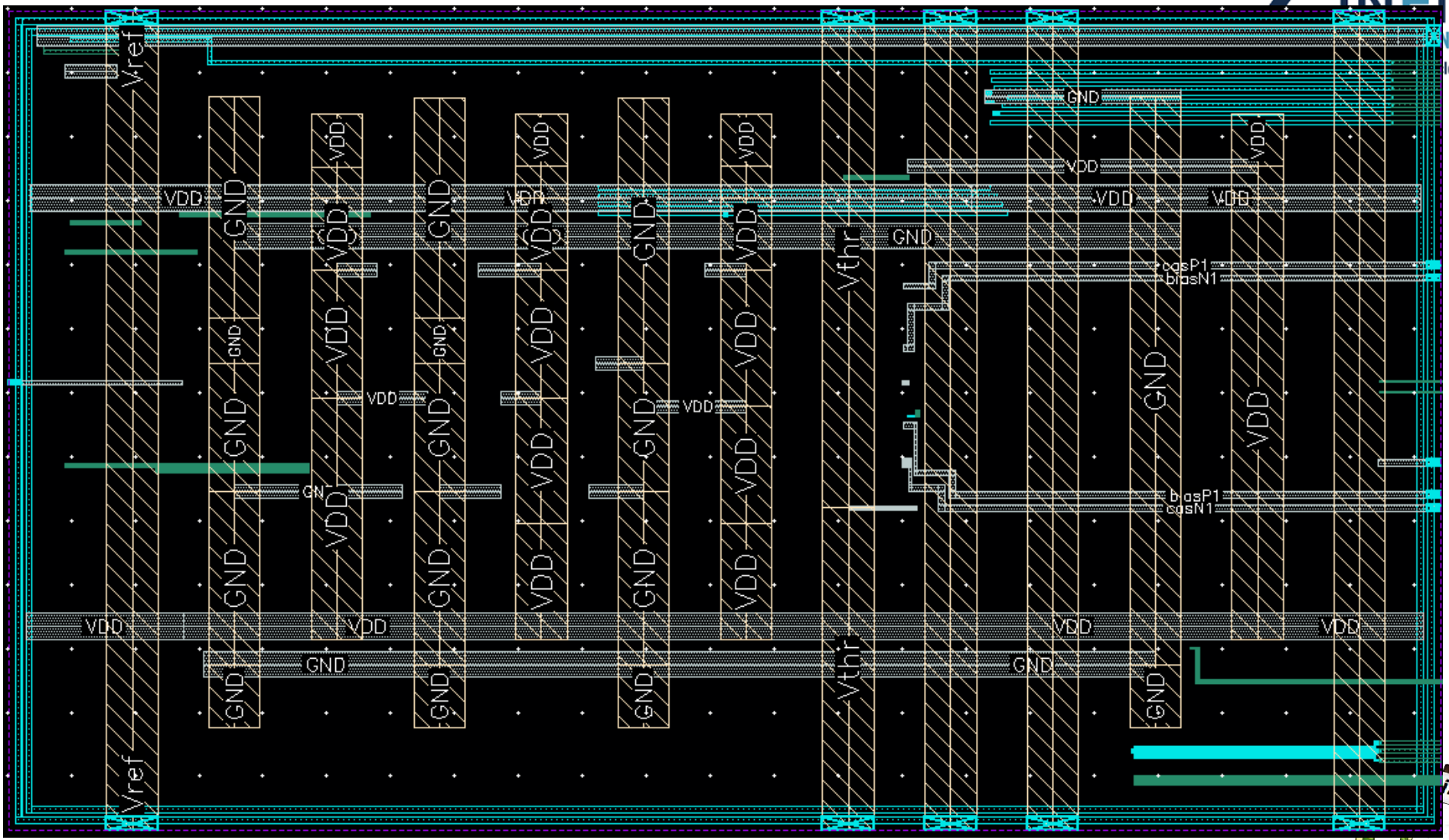
Layout of G



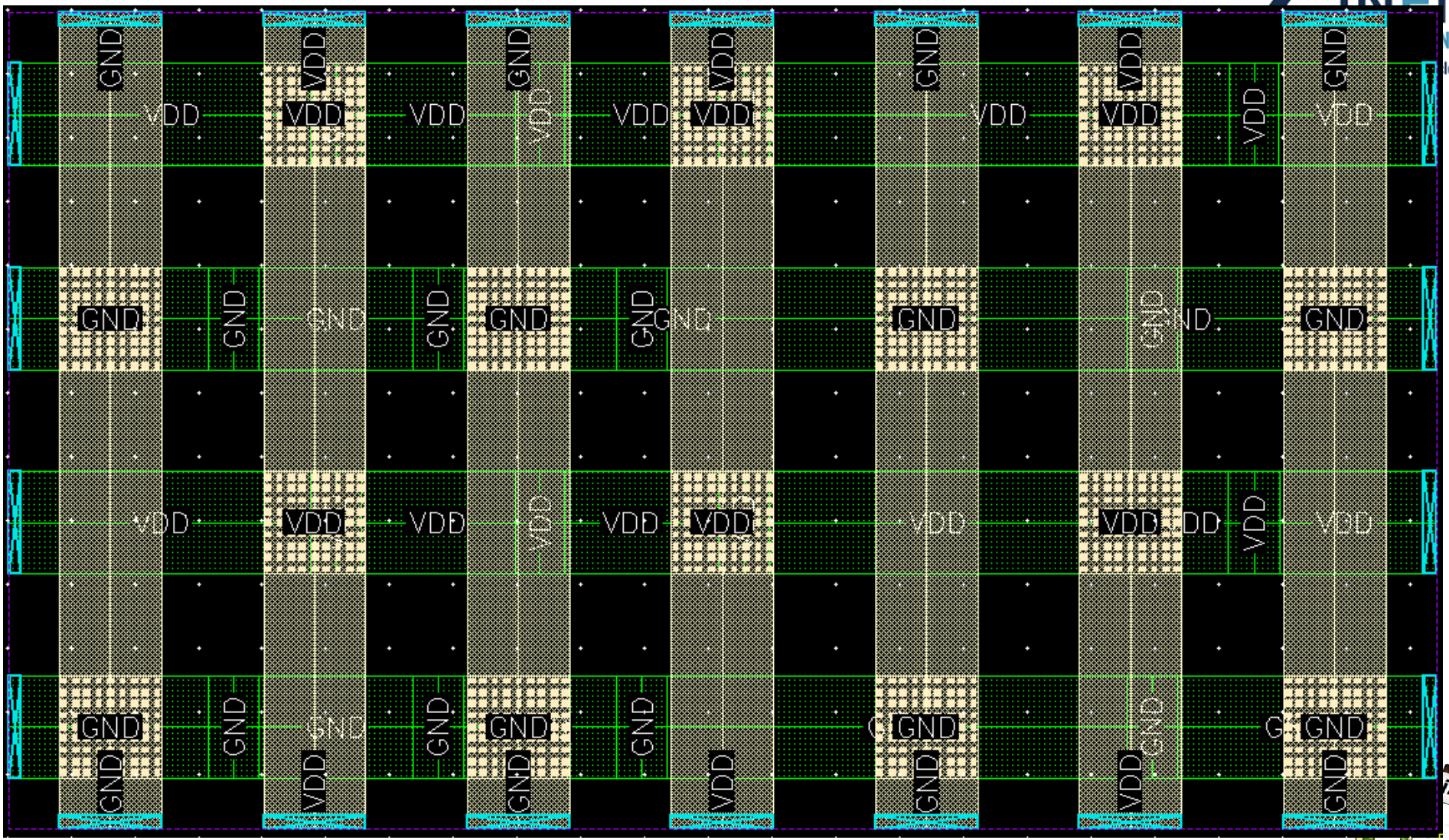
Layout of GB



Channel's Interface



Power Grid



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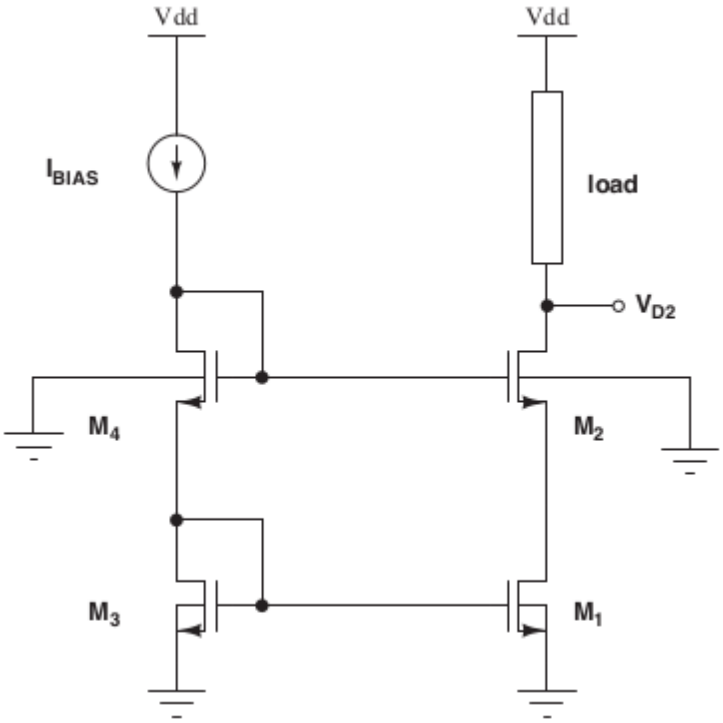
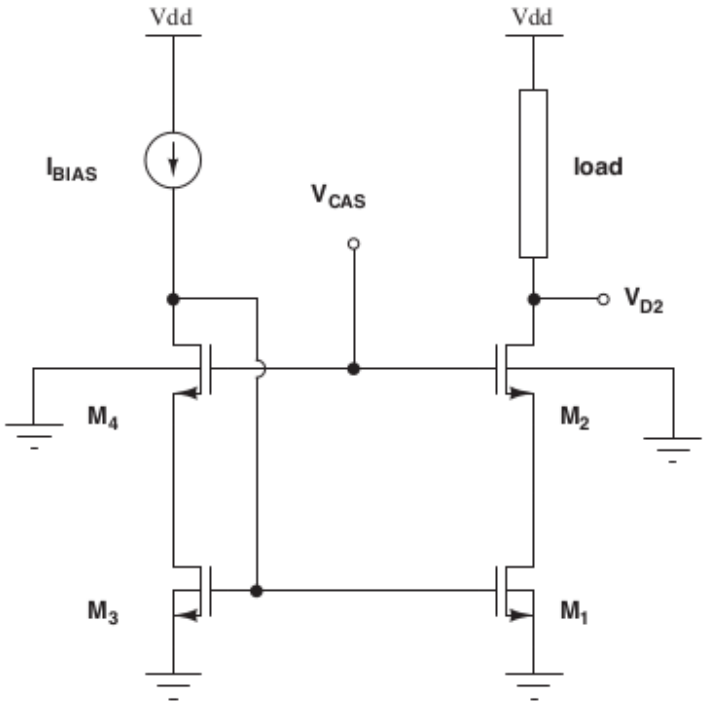
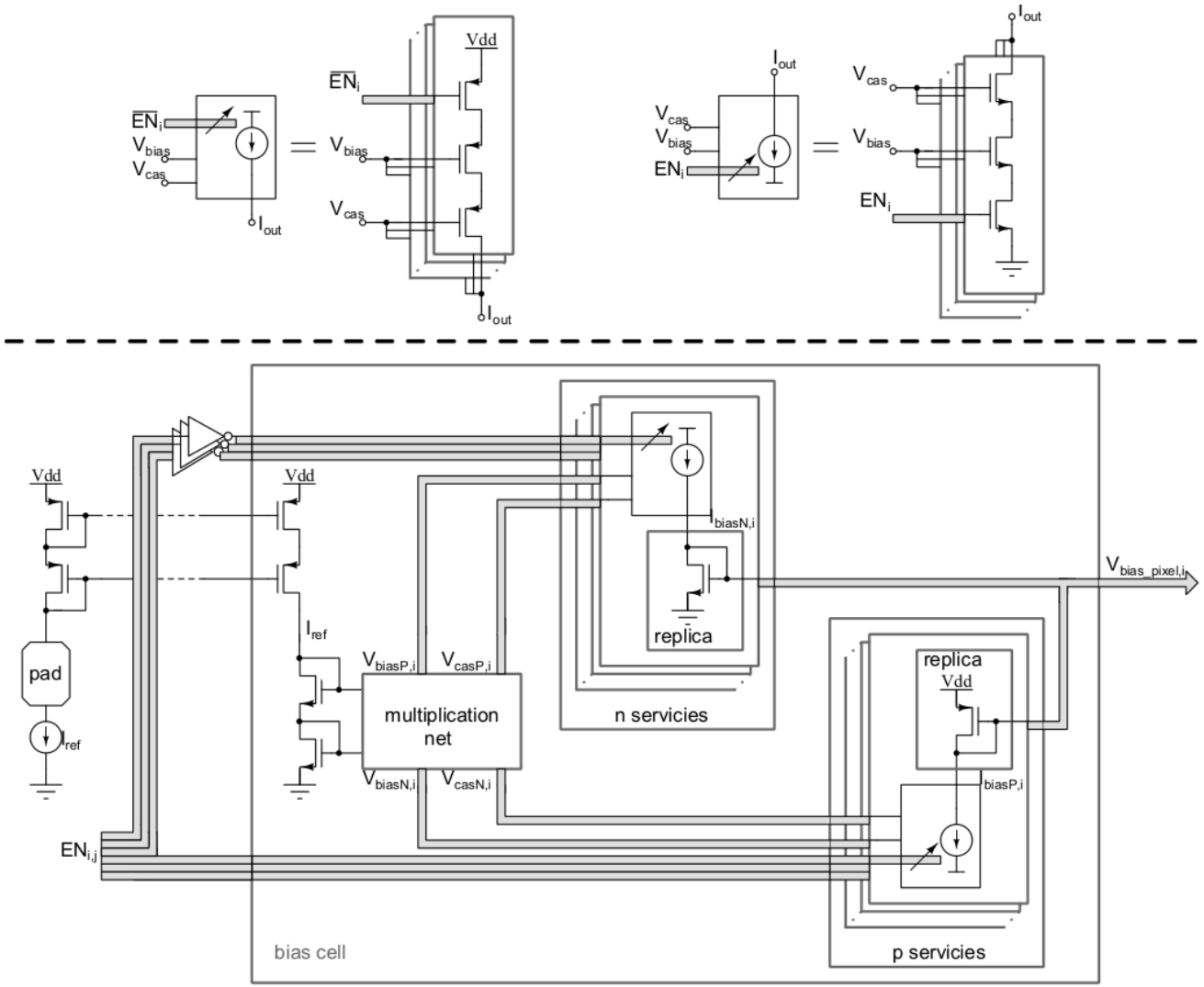
Generalita'





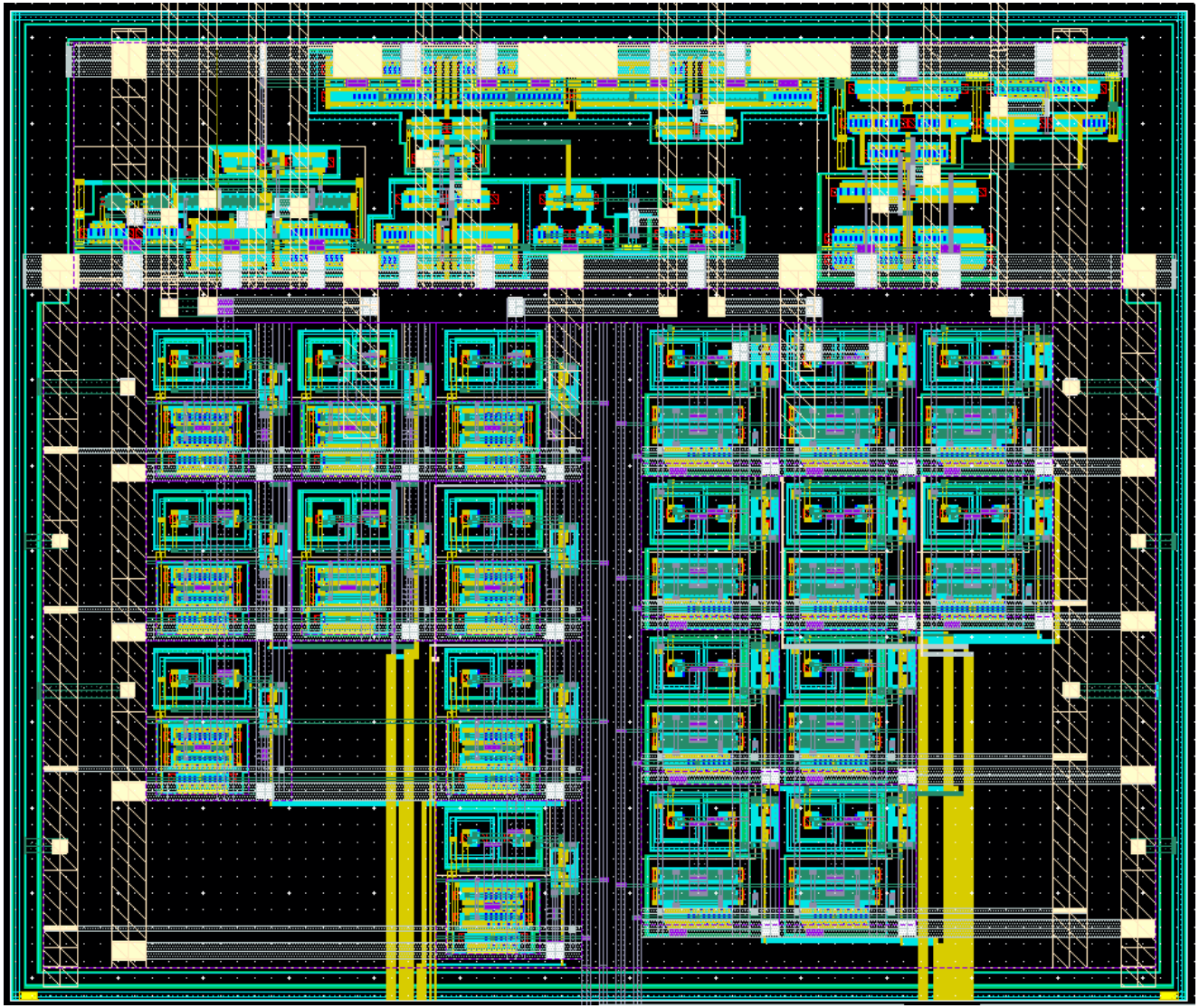
- Usati pre creare vbias e vcas.
- Entrambe le configurazioni migliorano l'accuratezza.
- Wide swing usato quando necessario.

Biasing per ZC

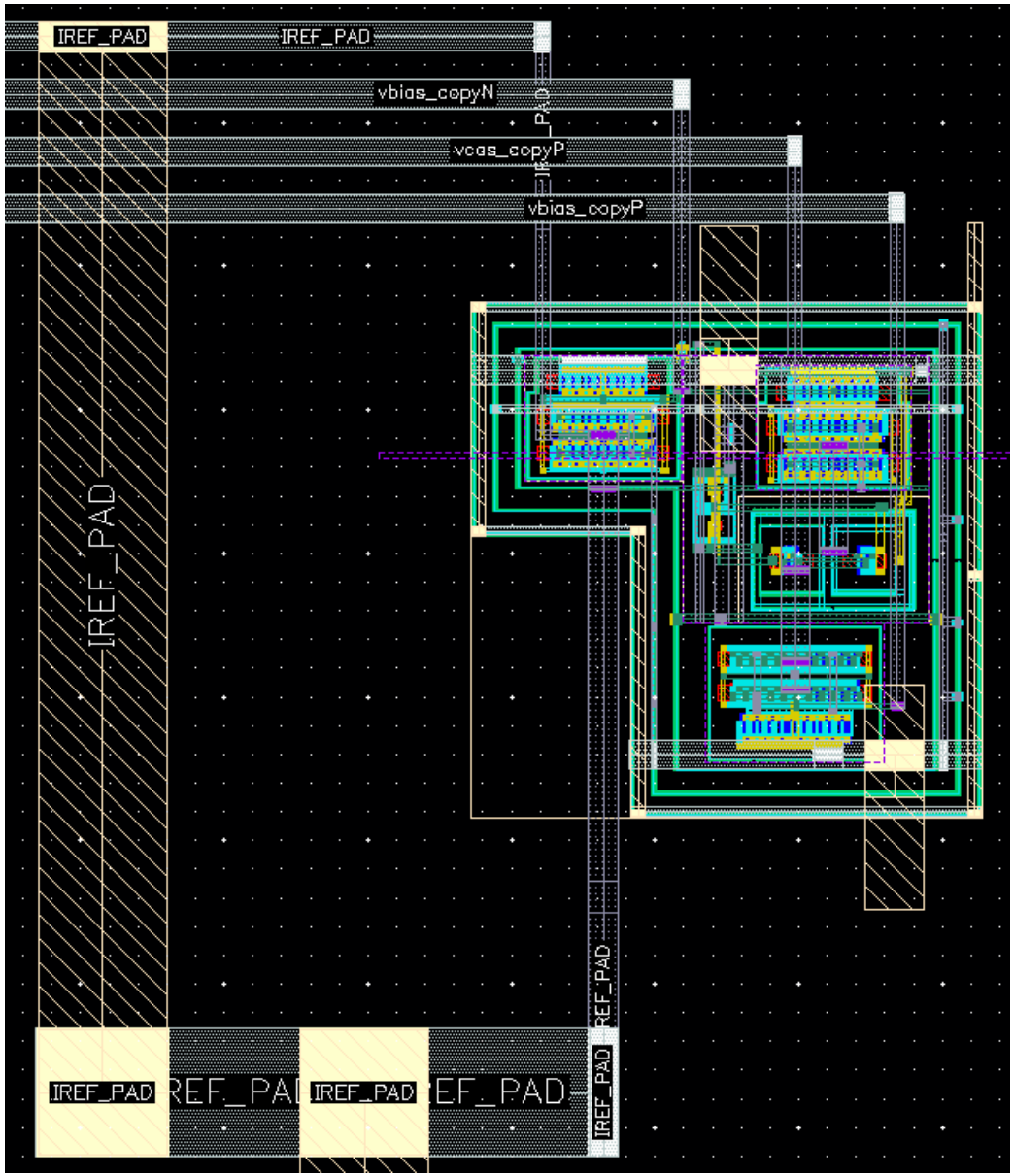


- (Questo e' quello di timespot): ci sono differenze (no-mult).

bias ZC



Iref Copy


IREF_PAD
IREF_PAD
vbias_copyN
vcas_copyP
vbias_copyP
IREF_PAD
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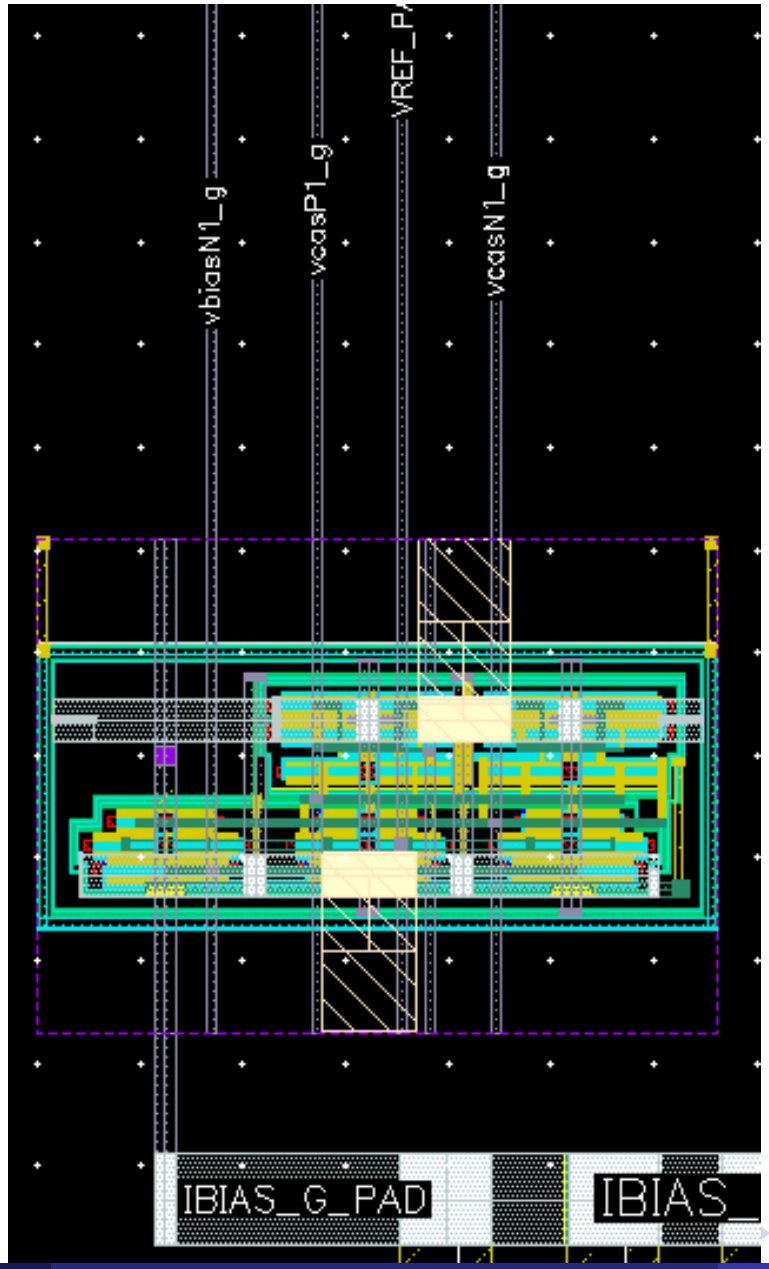
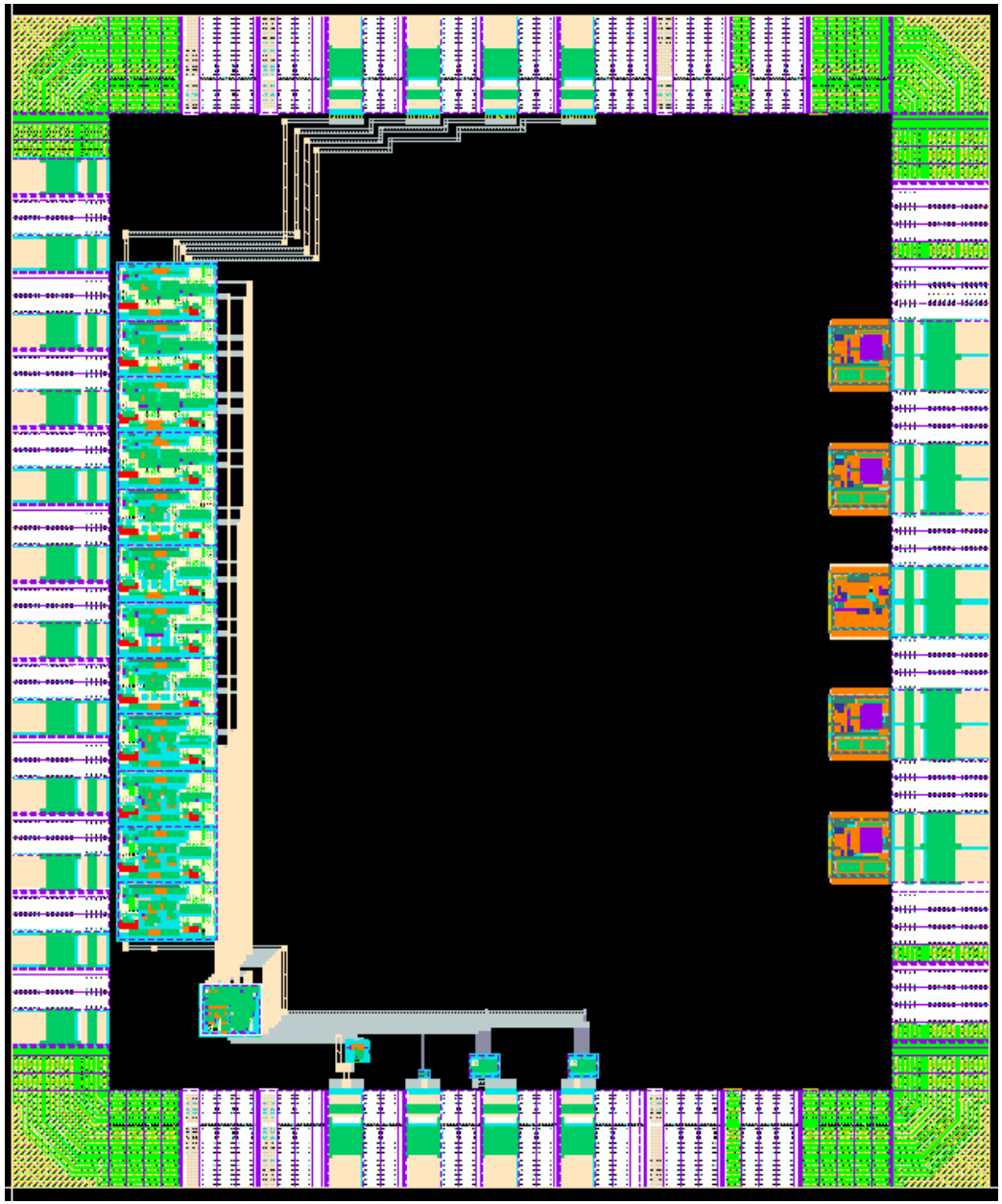
IREF_PAD

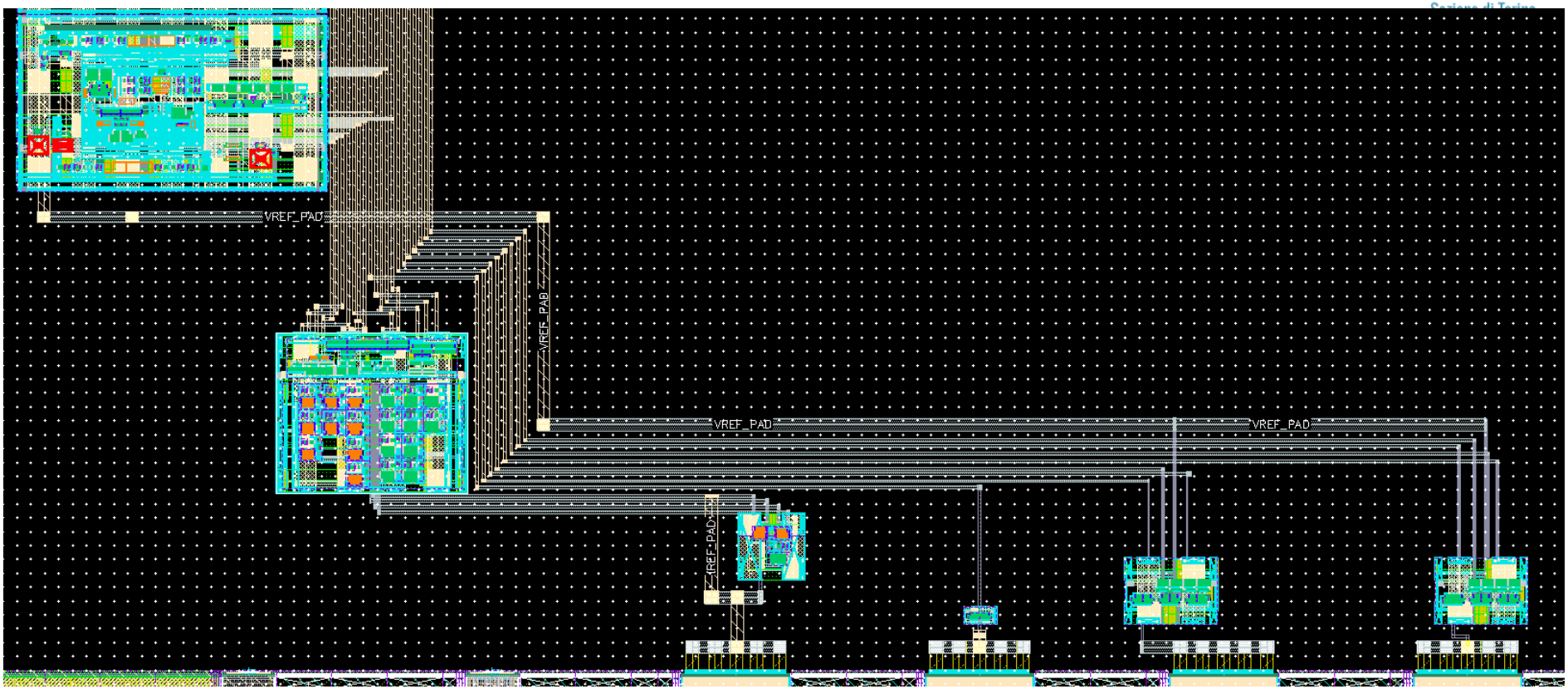
Bias G-GB



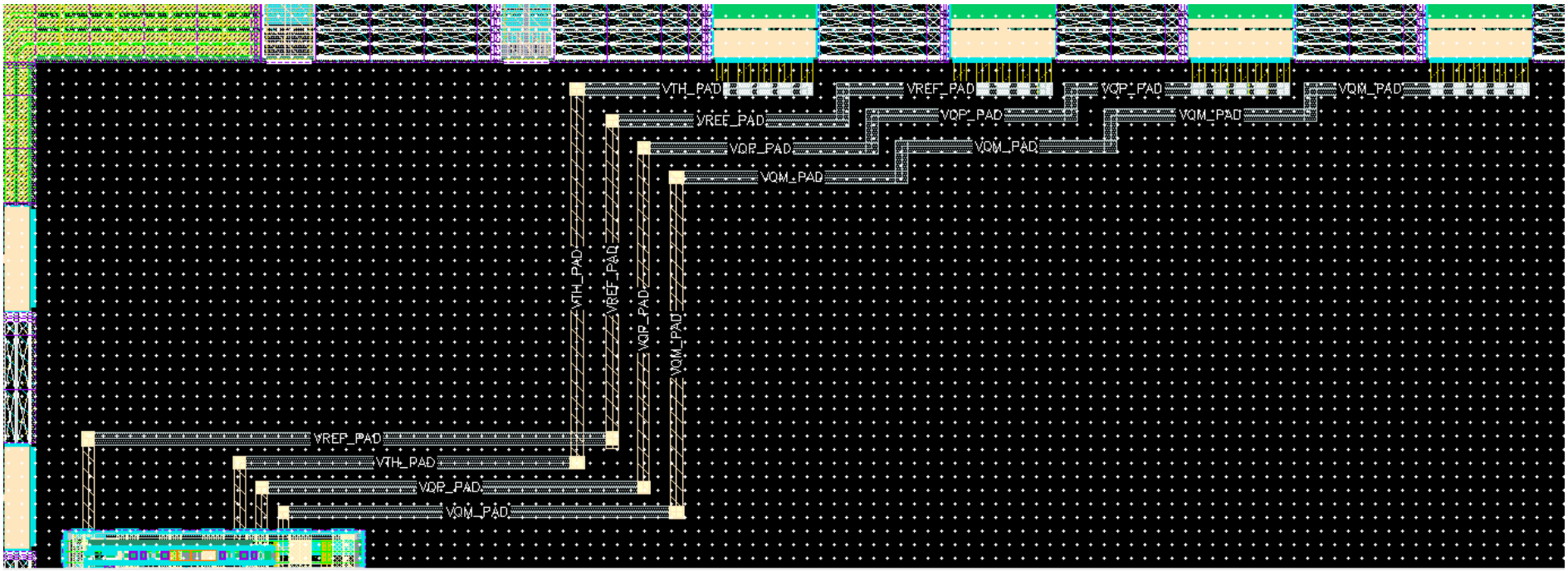
Interconnections



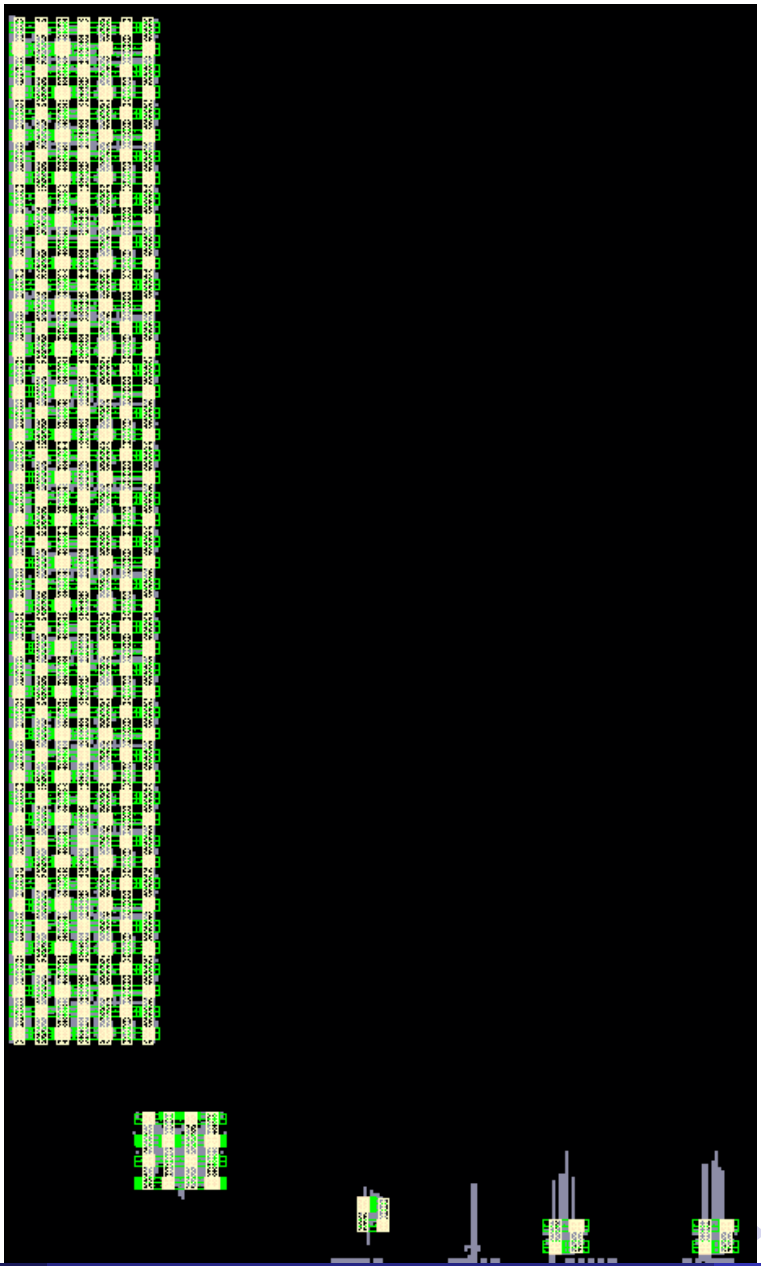
Bias connections



Voltage connections



Power grid



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Stato

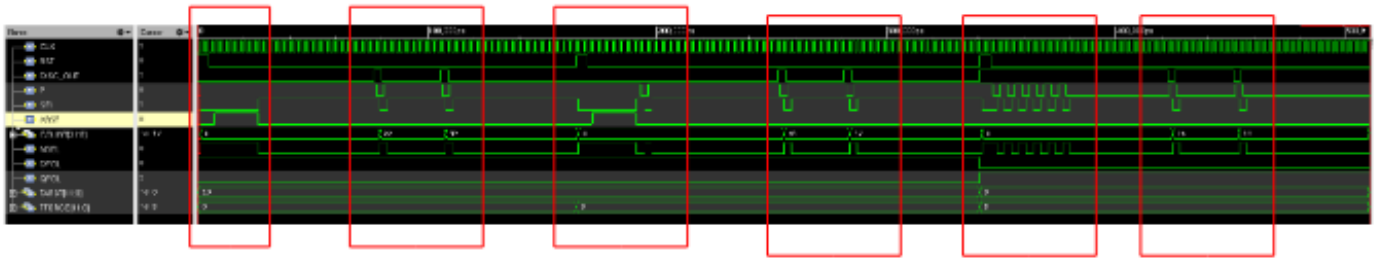
- RTL da terminare.
- Controllo con interfaccia seriale gia testata per scrivere i registri.
- Controllo del canale.
- Output con shift register: in idle parola di idle, dopo segnale di LATCH vengono salvate le uscite dei canali e trasmesse con header.

Registri necesari

nome	blocco	funzione	width	formato	N reg 12 bit	formato	direzione	moltiplicatore	indirizzo start	indirizzo end
b_CC	canale Analogico	cap compensazione in frequenza	3-0	dec	1	b_CC,b_CF,bCQ,UU	W	12	000 0100	000 1111
b_CF		cap di feedback	2-0	dec						
b_CQ		cap di iniezione	2-0	dec						
EN_a1	periferia Analogica	corrente stadio 1 (zc)	1-0	term	1	EN_a1,EN_a2,EN_a22,UUUUU	W	1	001 0000	001 0000
EN_a21		corrente stadio 2 ramo 1 (zc)	1-0	term						
EN_a22		corrente stadio 2 ramo 2 (zc)	2-0	term						
EN_zc		corrente totale stadio zc (zc)	7-0	term	1	EN_zc,ENzc2	W	1	001 0001	001 0001
EN_zc2		corrente stadio zc ramo 2 (zc)	3-0	term						
TARST	canale Digitale ?	durata reset analogico in numero di periodi	11-0	dec	1	TARST	W	12?	001 0010	001 1101
TFORCE		durata impulsi di carica per forzare il canale In numero di periodi	11-0	dec	1	TFORCE	W	12?	001 1110	010 1001
COUNT		conteggi in uscita?	31-0	dec	3	COUNT[31-20]	R	12	010 1010	011 0101
						COUNT[19-8]	R	12	011 0110	100 0001
						COUNT[7-0],UUUU	R	12	100 0010	100 1101
chEN[11-0]		enable del conteggio	11-0	bin	12	chEN[11-0]	W	1	100 1110	100 1110
chRST[11-0]		reset del singolo canale	11-0	bin	12	chRST[11-0]	W	1	100 1111	100 1111

- Molti possono essere messi in comune.
- L'output e' fatto con il meccanismo di cui sopra.

Controllo che ho usato nelle mixed signal



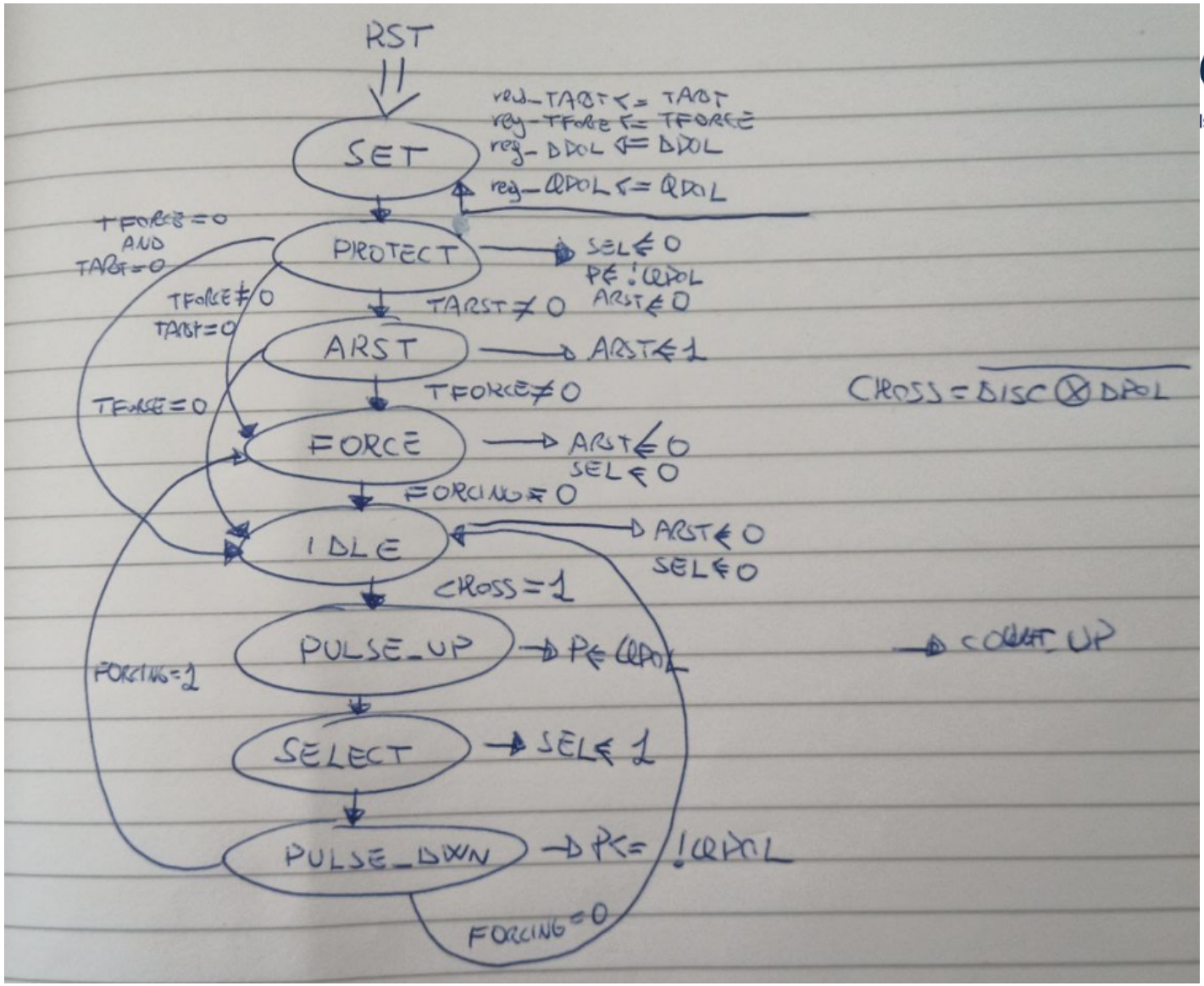
Segnali:

- CLK clock
- RST reset digitale del canale
- DISC_OUT: output del discriminatore
- P impulso per iniezione
- SEL, nSEL: selezionano il fronte da mandare al CSA (SEL=1)
- ARST: reset analogico (chiusura ad anello del CSA)
- COUNT: output (32 bit)
- DPOL: setta la polarita' del discriminatore (1: transizione 0→1)
- QPOL: setta la polaita' di P (0 : transizione 1→0)
- TFORCE, TARST: programmano la durata in multipli del clock delle forzatura e reset analogici

Programmazione: ogni volta che viene resettato il canale vengono letti dei registri esterni per settare I parametri. L'idea e' di avere il reset del canale in or con il global reset, in modo tale che all'accensione si leggano I dafault dei canali. Resettando il singolo canale si salvano I valori

Procedura: dopo il reset, si settano I parametri, poi si resetta l'analogico (opzionale), poi si forza il canale (opzionale), dopodiche' il canale e' attivo.

FSM del controllo



- scusate per questo schema analogico.

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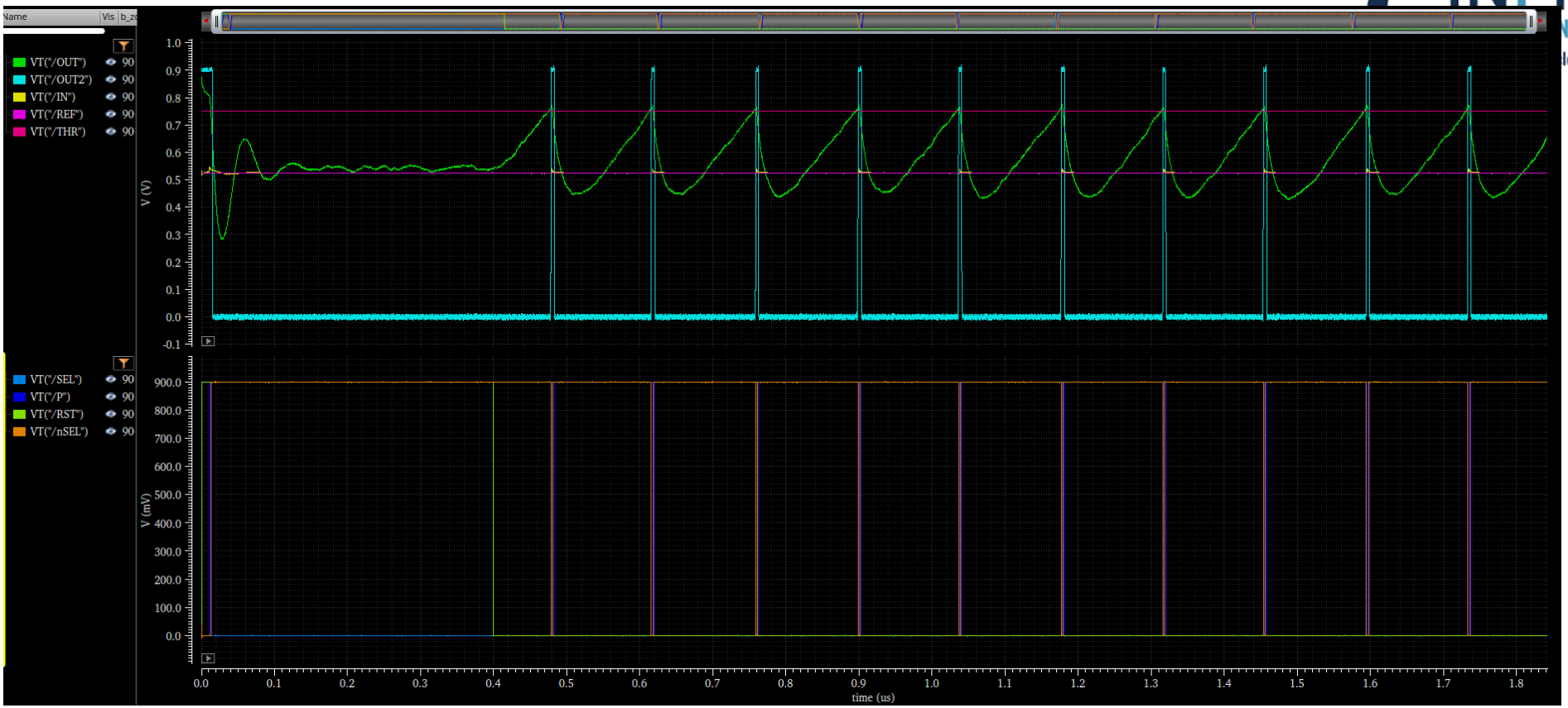
Stato

- Il sistema e' testato e funzionante, ma necessita' di simulazione piu' sistematiche (lunghe):
- Montecarlo di sistema(sigh).
- Esplorazione range basse correnti.
- Esplorazione configurazioni (non tutte: spazio delle configurazioni enorme).
- Estrarre performance verso corrente, capacita'.
- Vero Mixed signal.
- Le farei ad Aprile: devo trovare un set di casistiche limite rilevanti.

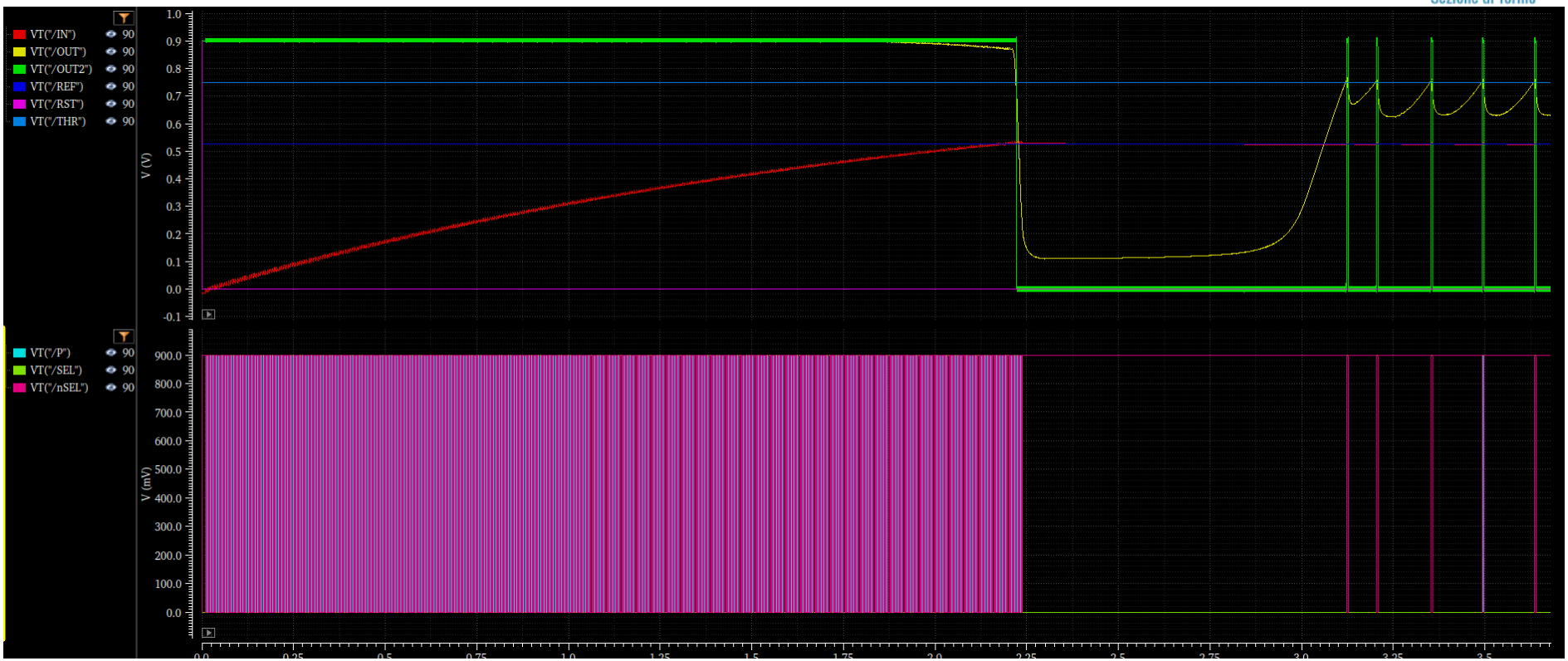
Simulazione tipica



- Iin 500n, clk 640M, fteo 1.143M, ferr 0.4%(con sistematico), fnoise $<$ 30G, Cin 3+10p (testato anche 30+50), Cprog al massimo.

Dettaglio discriminatore

Forzatura in carica



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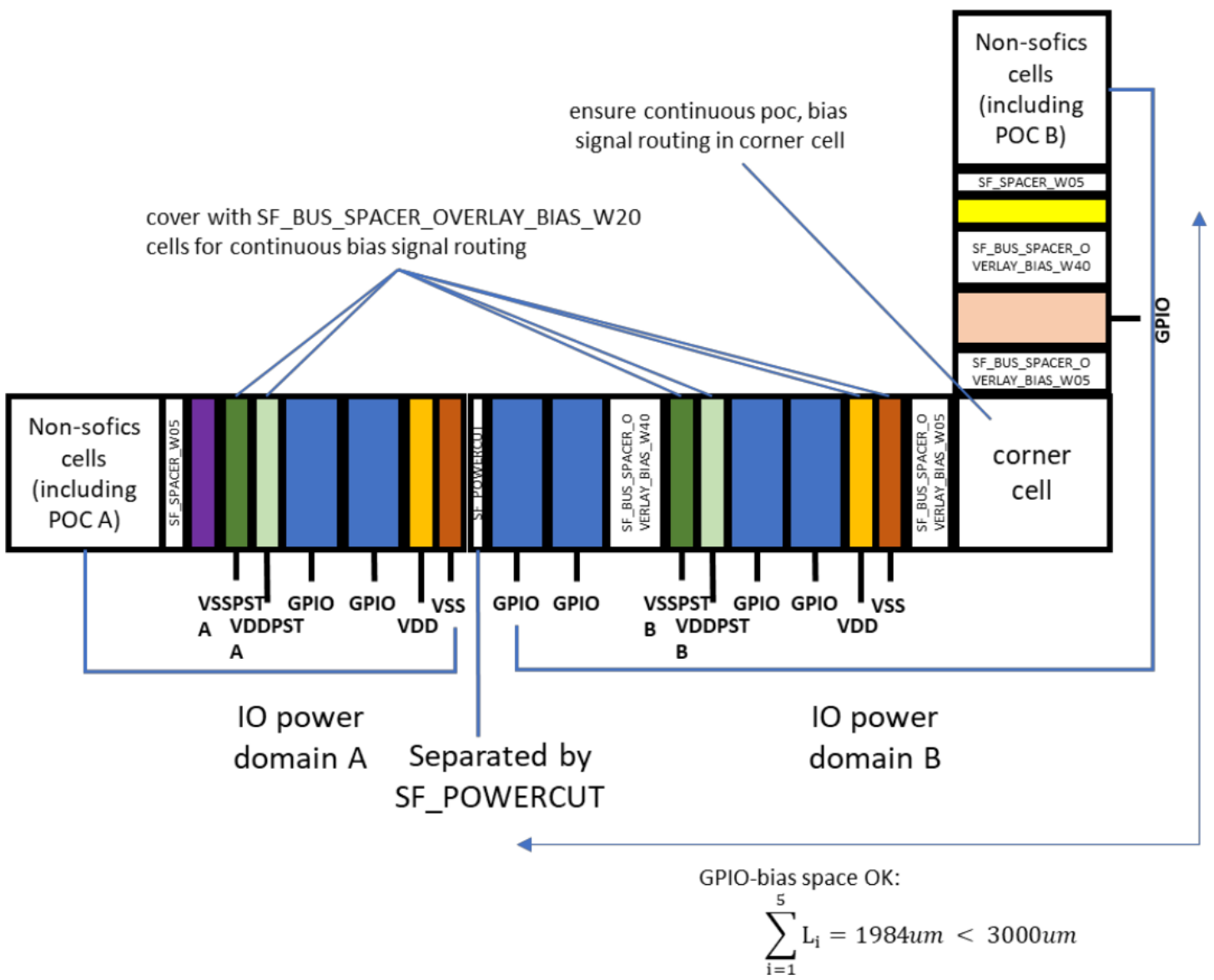
Stato

- Analogica $\rightarrow$ manca il power.
- Digitale $\rightarrow$ da ultimare i blocchi.
- Padframe $\rightarrow$ completo? Staggered? Da presentare a Barbara e Flori. Manca il seelring... (!)
- Utilizzati pad radtol (sofics).

Regole SF Digitale

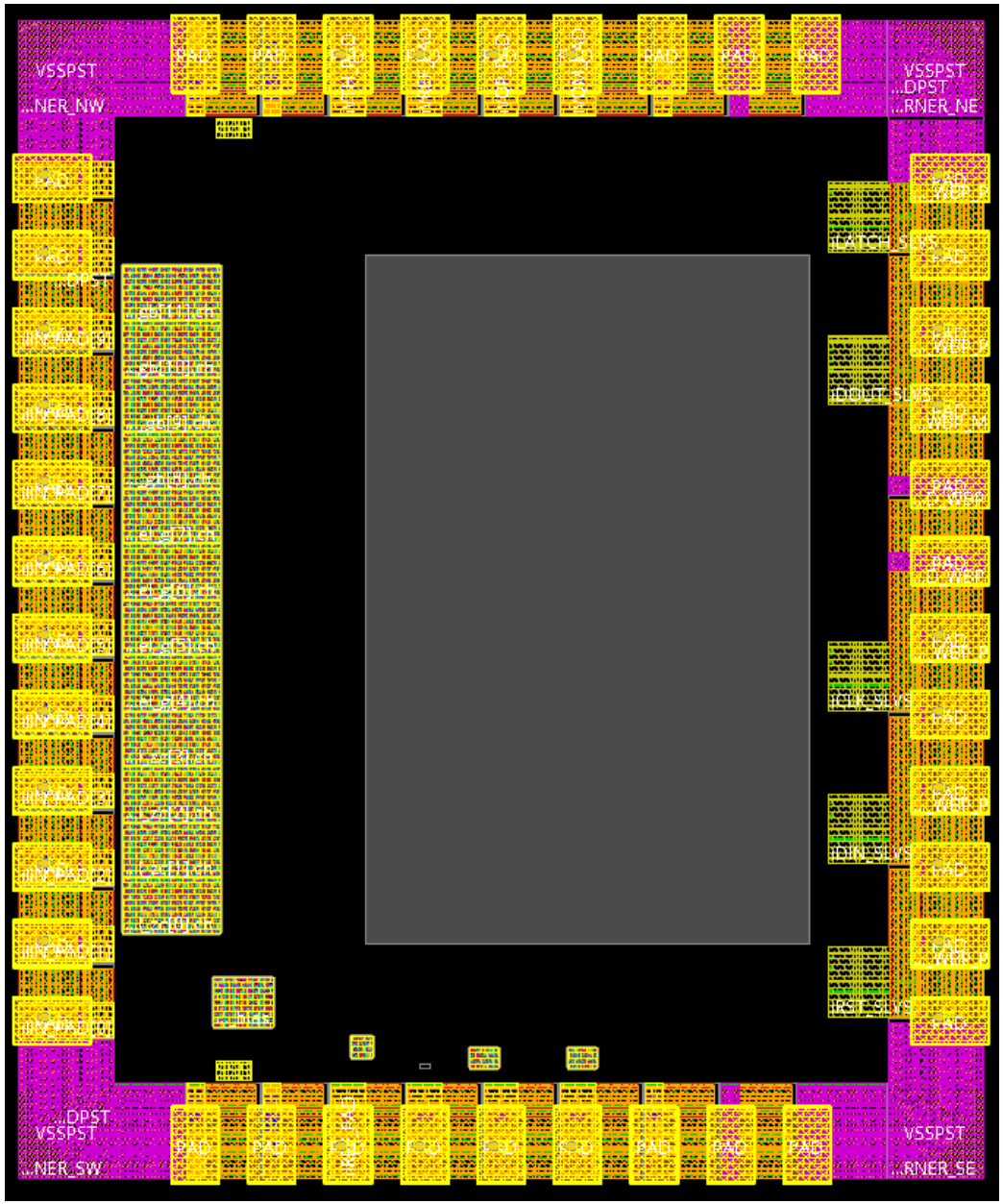
Multi power domain digital IO example



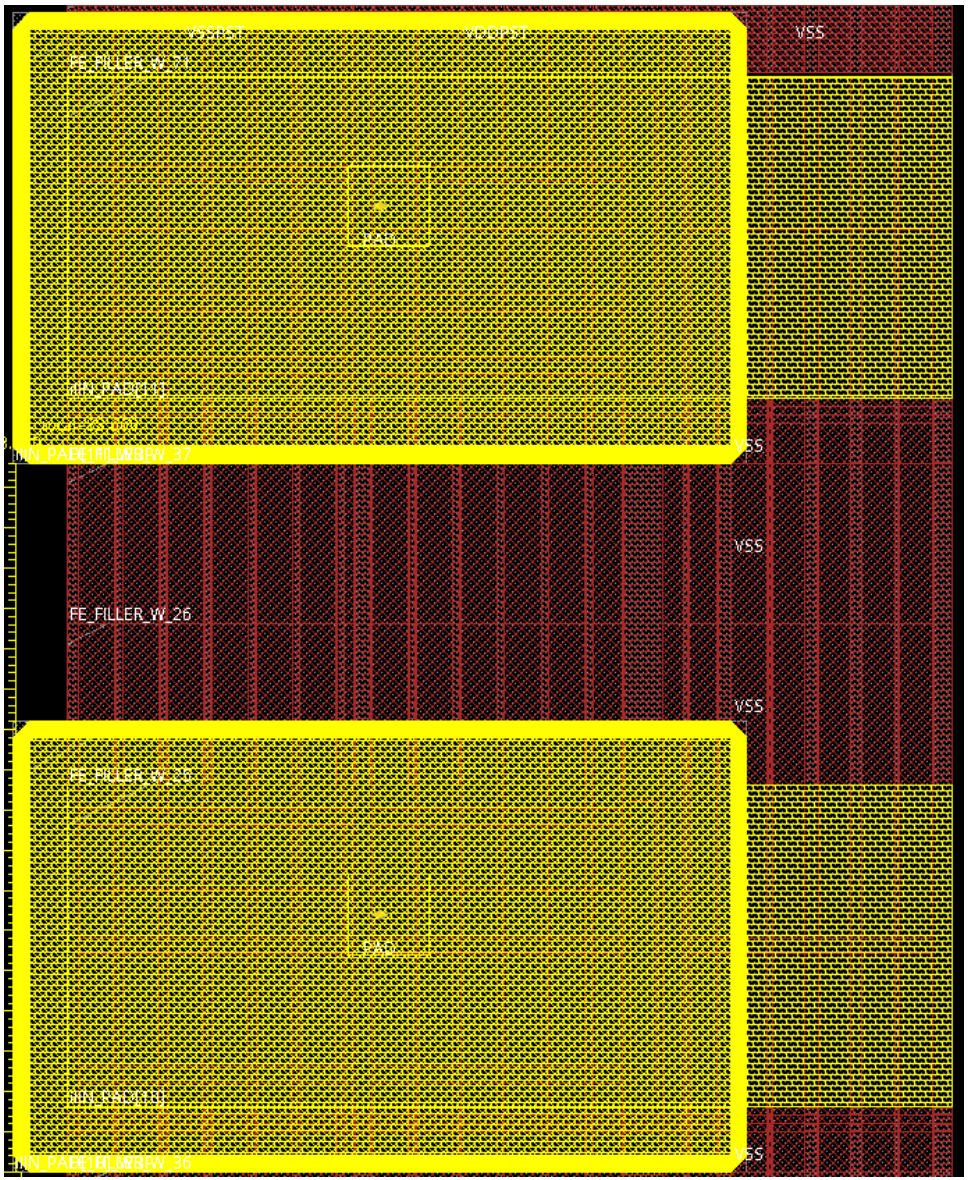
Esempio con PAD analogici

- Alimentazioni analogiche "NO-RAIL" $\rightarrow$ non serve interrompere il padframe.

Floorplan

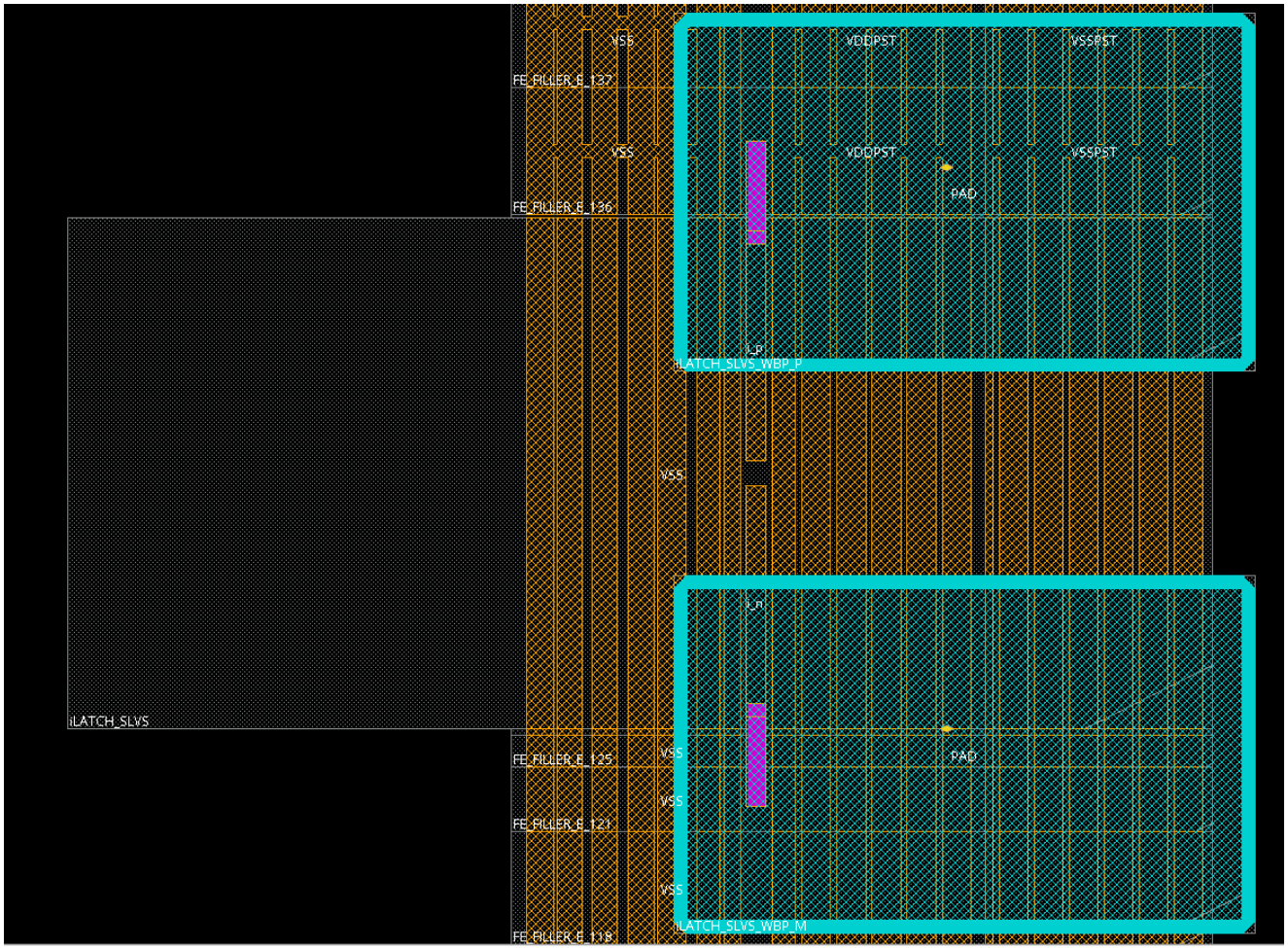

VSSPST
...NER_NW
VSSPST
...DPST
...RNER_NE
...DPST
VSSPST
...NER_SW
VSSPST
...RNER_SE

Pitch tra i PAD

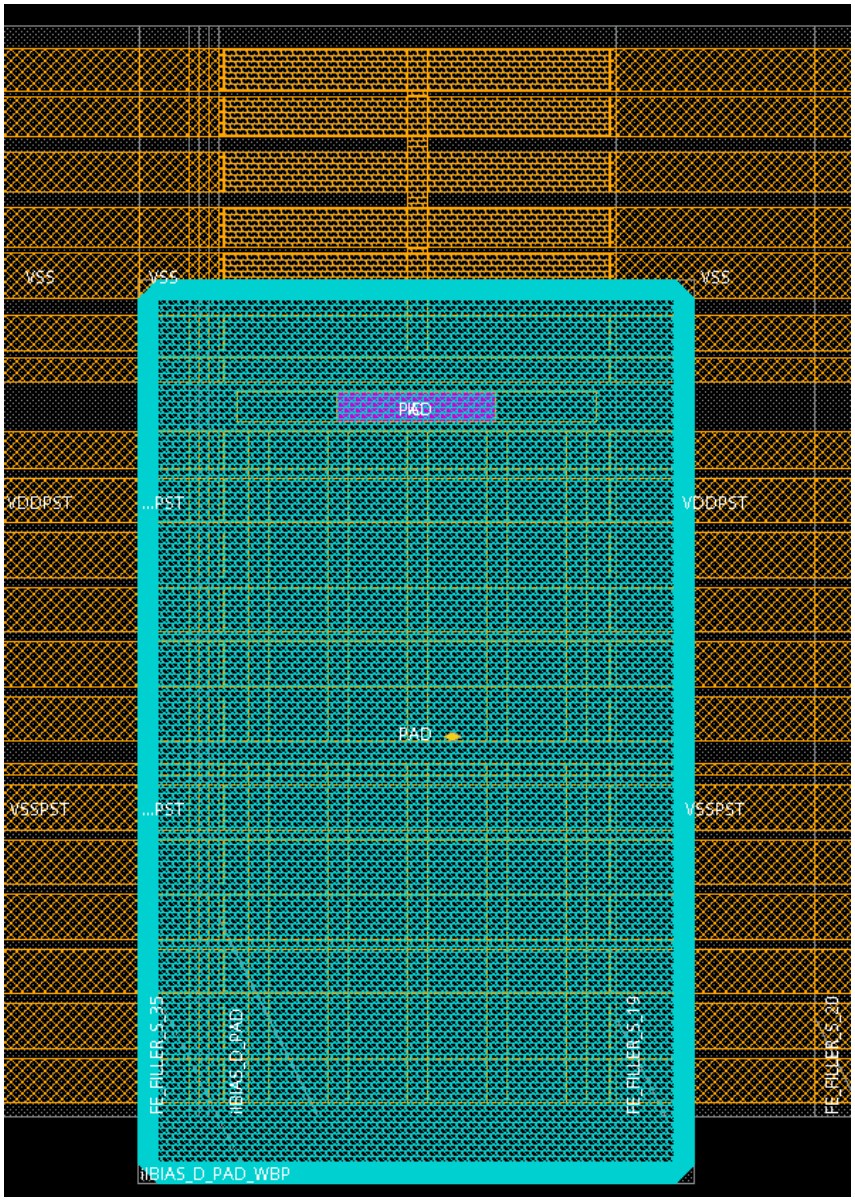


- pre-shrink: P 88 µm, W 56 µm, S 32 µm.
- Silicio: P 79.2 µm, W 50.04 µm, S 28.8 µm.

PAD SLVS


VSS
FE_FILLER_E_137
VDDPST
VSSPST
VSS
FE_FILLER_E_136
VDDPST
VSSPST
PAD
I_P
iLATCH_SLVS_WBP_P
VSS
I_P
iLATCH_SLVS
FE_FILLER_E_125
VSS
PAD
VSS
FE_FILLER_E_121
VSS
iLATCH_SLVS_WBP_M
FE_FILLER_E_118

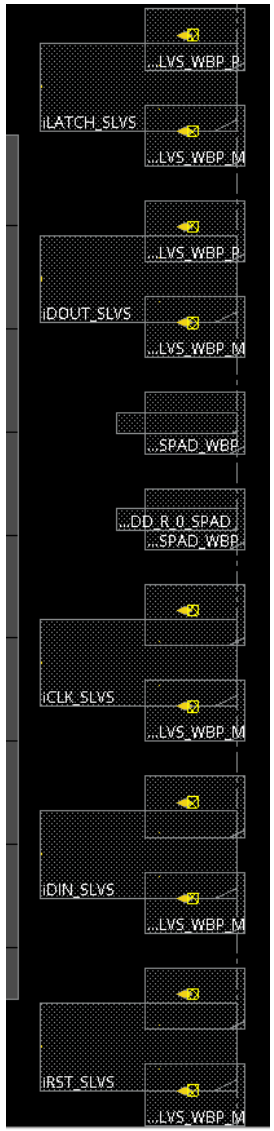
I PAD sporgono



- di 6.675u
- e manca il seal-ring.

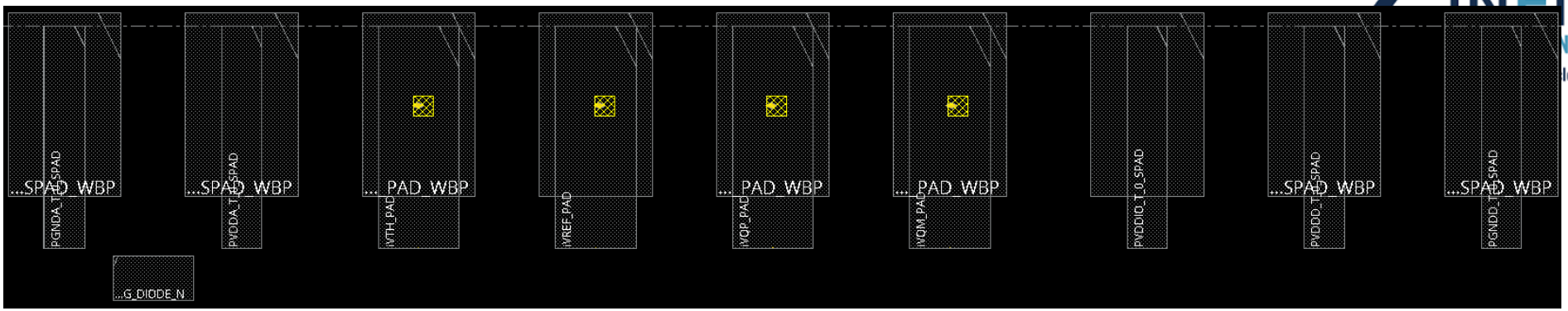
PADs Ovest e Est

- solo correnti di input.

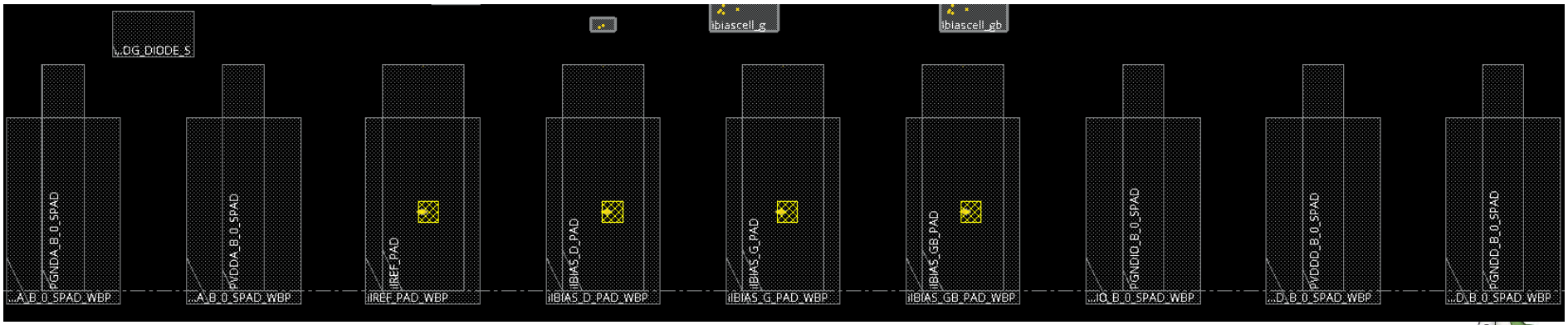


- Tutto il digitale e' qui ed e' differenziale.
- Al centro alimentazioni digitali.
- Centrali segnali critici/veloci/attivi (CLK,DOUT).

PADs Nord e Sud



- analog PWR-GND , tensioni esterne, VDDIO, digital PWR-GND



- analog PWR-GND , correnti di bias, GNDIO, digital PWR-GND

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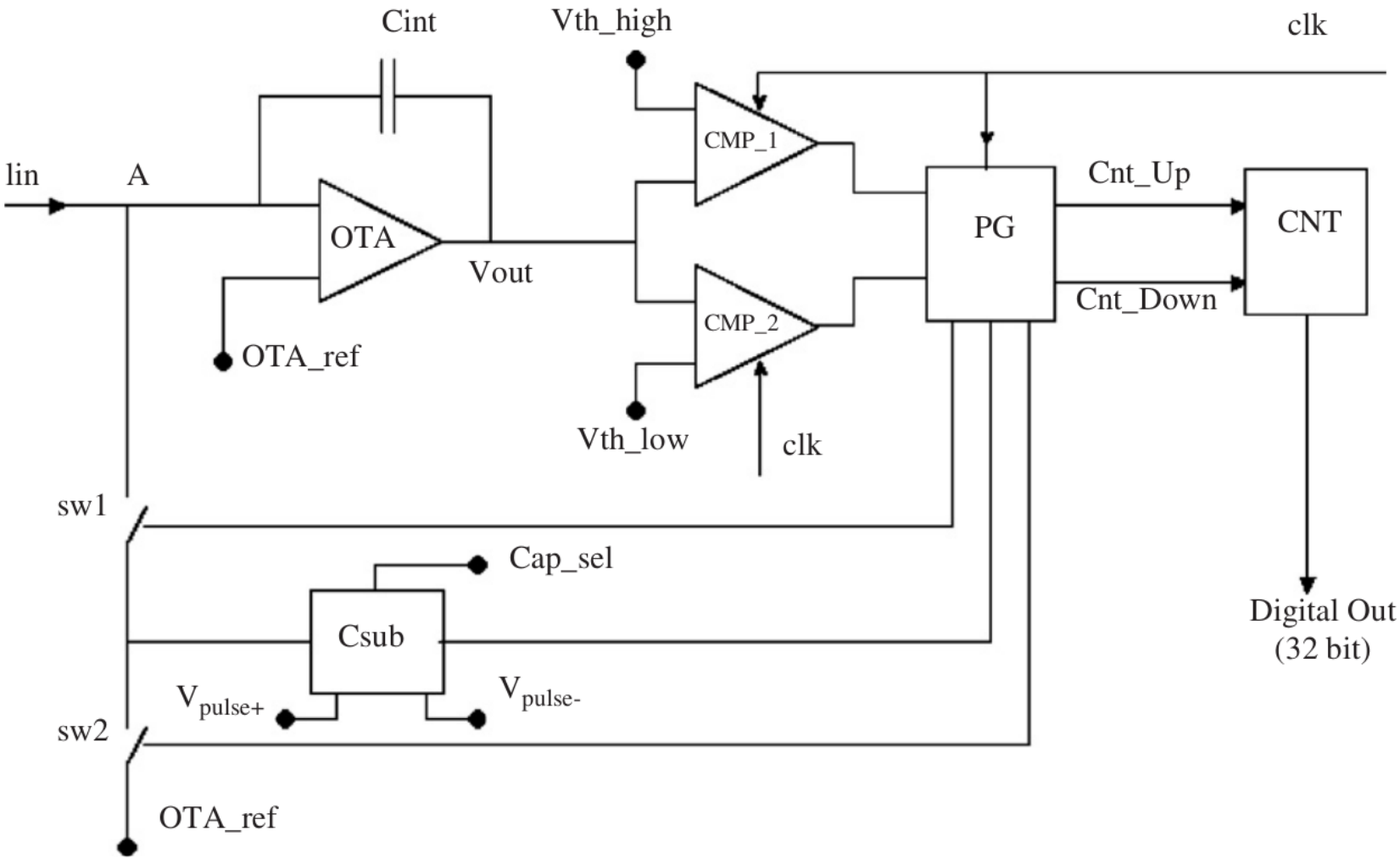
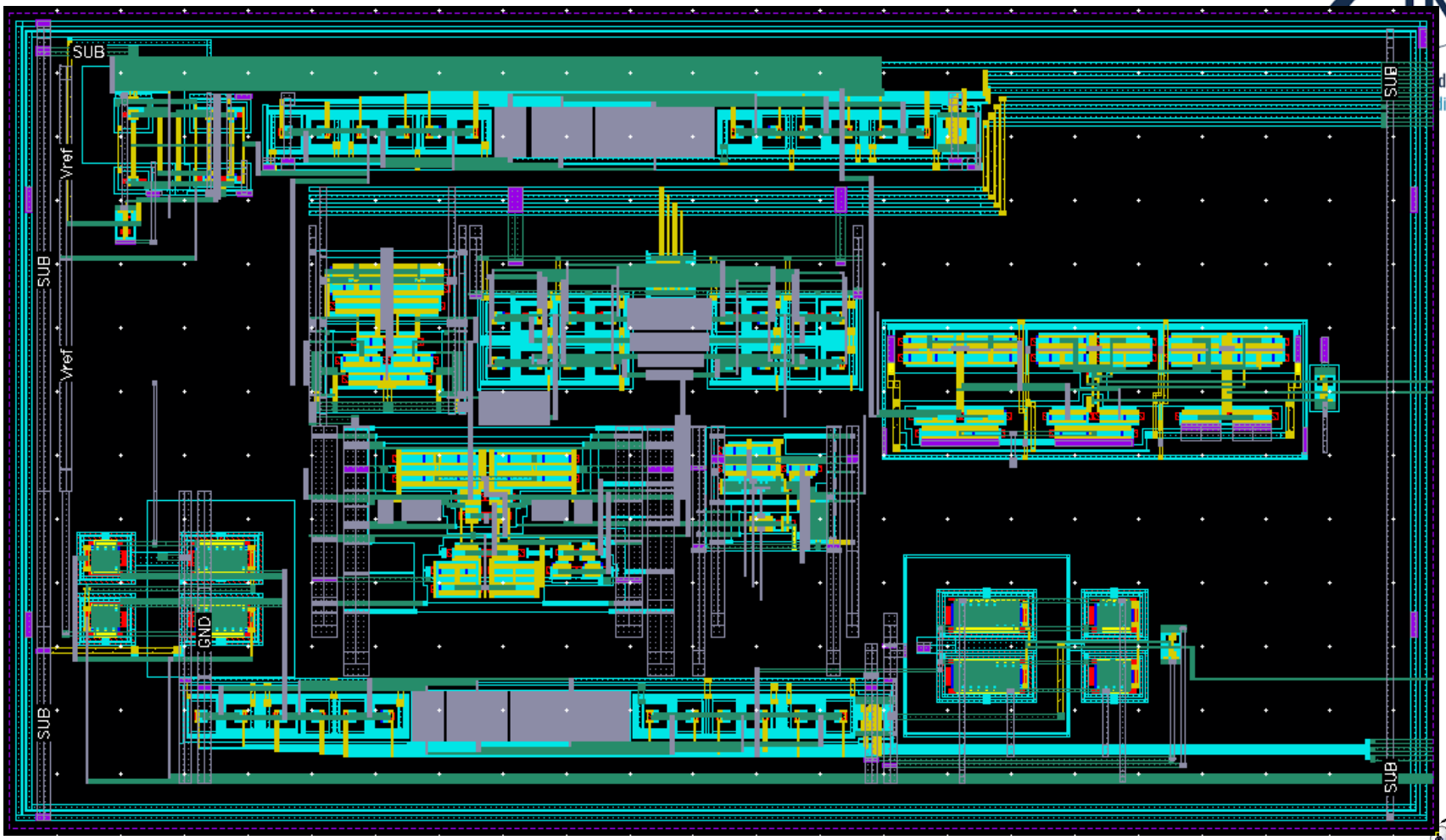
Prossimi Passi

- Aggiungere Decap su PWR-GND e tensioni.
- Stringere il PAD frame per seal-ring (pitch invariato)
- PAD staggered? da chiedere.
- Terminare un RTL totale.
- Integrare pwr e clock!.
- simulatione mista.
- verificare

Modifca: Aggiungere un discriminatore

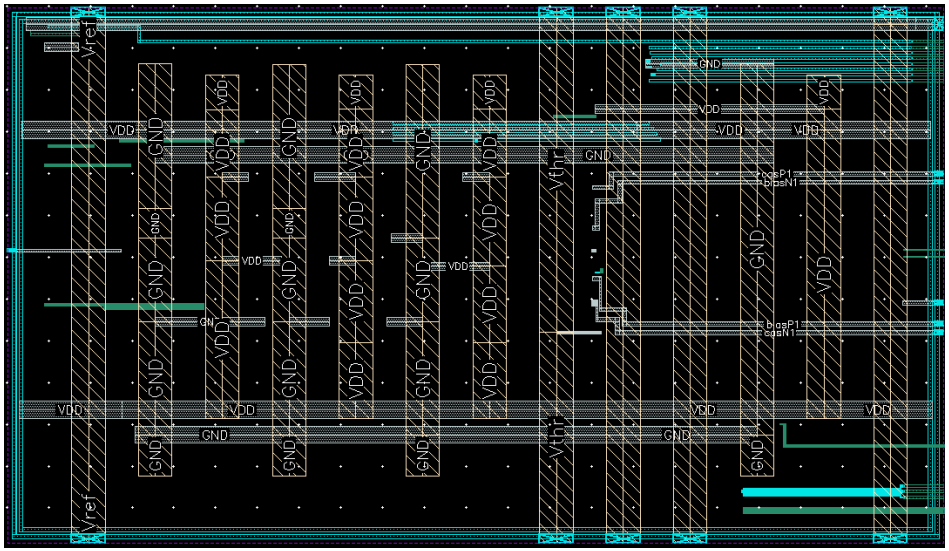


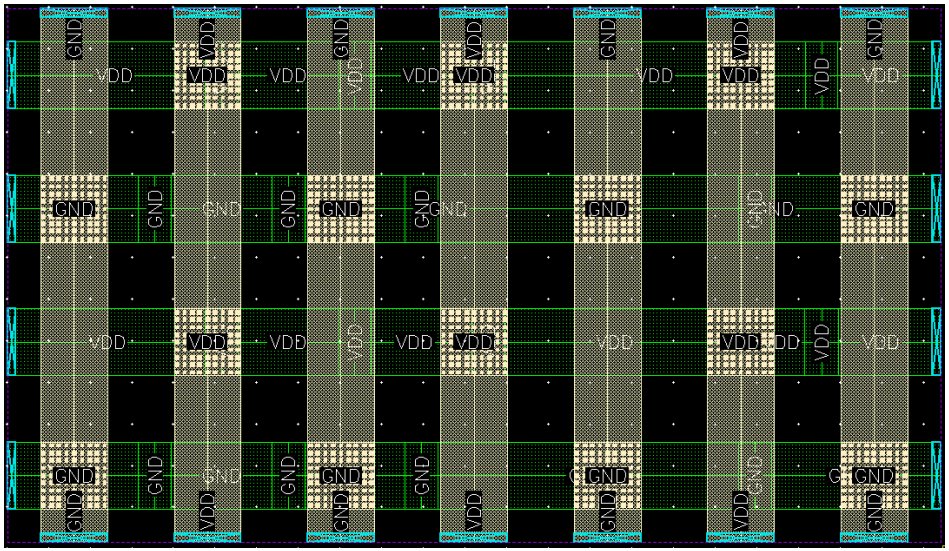
Dove?



- Sotto a quello esistente (che si sposta in alto).

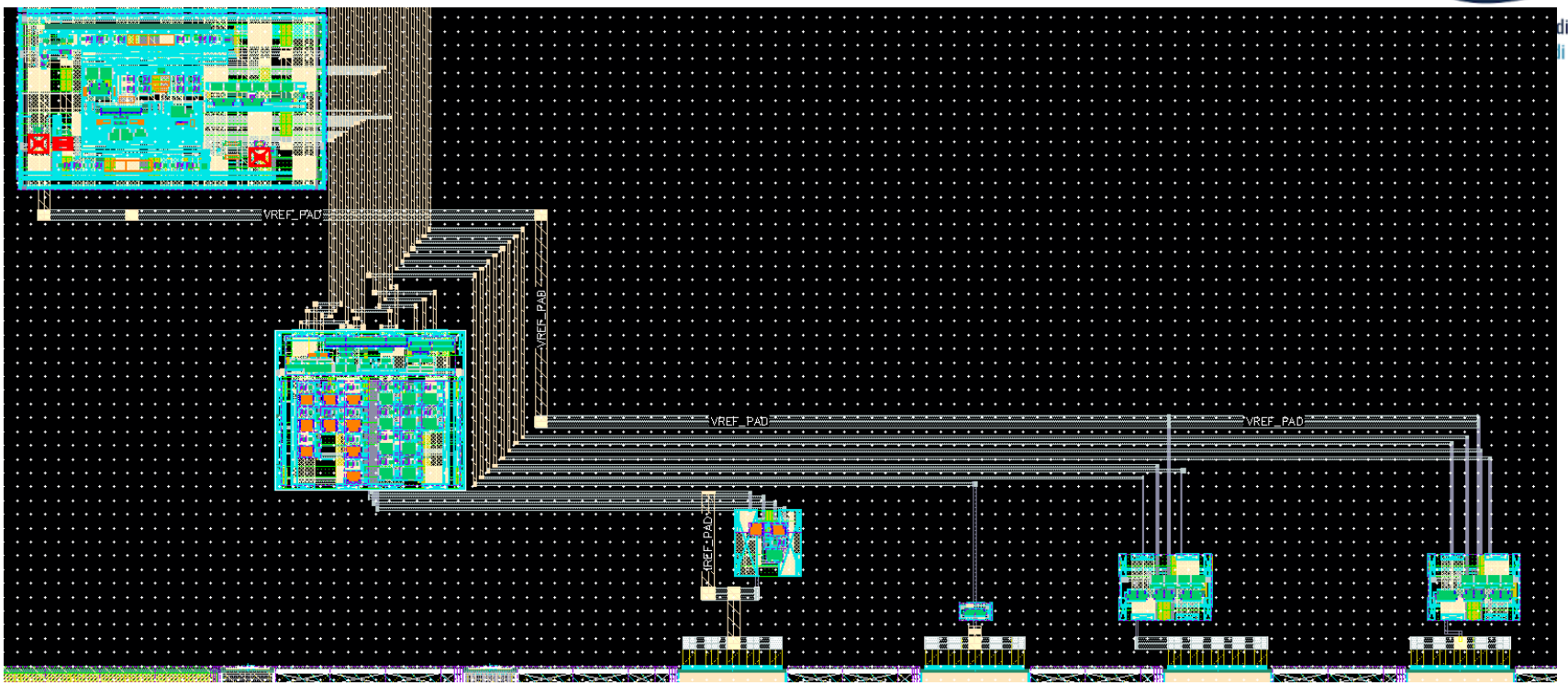
Come lo connetto?





- Mi serve una nuova Vth (sigh).
- Sposto le vare Vext a M7 (sigh sigh).
- Sposto la griglia da M7-M8 a M8-M9 (sigh sigh sigh).

Con che PAD?



- Condivido una cella di bias per G e GB (sono identiche).
- mi si libera un PAD a lato S.