Cryogenic high-speed transmitter and receiver circuits in advanced CMOS technology for quantum computing and technology

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Contents

Chapter 1

Introduction

This report presents the design of Scalable Low Voltage Signaling (SLVS) transmitter and receiver. The circuit works for IO supply of 1.8 V and core supply of 0.8 V. The target data rate of 2.56 Gbps is reached at room temperature. The designed is implemented in 22 nm FDSOI technology from Global Foundries.

1.1 LVDS standard

This design is based on the LVDS (Low Voltage Differential Signaling) standard proposed by IEEE in 1994 [5]. This standard was proposed with the aim of developing a layer of specifications which are technology independent, compatible with digital CMOS, optimized for communications between boards and scalable. The strategies adopted in this standard include:

- Low voltage swing, to minimize power dissipation and enable operation at very high-speed.
- Differential signaling, which is mandatory to obtain acceptable noise margins with low swings.
- Each receiver is assumed to provide its own termination resistors, in order to minimize board costs and to maximize clock rate.
- The ground potential difference between driver and receiver must be kept small by the system design.

These strategies offer some benefits. Firstly, the constant driver and link currents simplify the design.

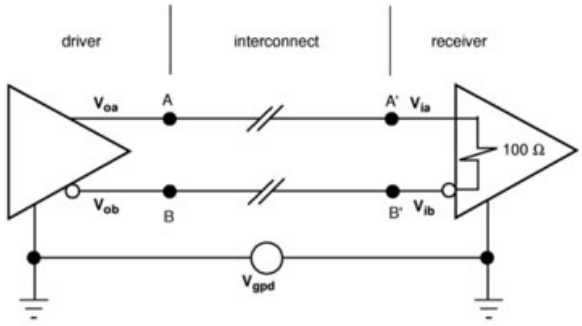

Figure 1.1: LVDS interface connected point-to-point. *Credits:* [5]

Then, the fact that induced noise and ground-bounce appear as a common-mode signals allows the use of a lower signal current and so the reduction of power consumption. The equal and opposite currents flowing in the transmission line create canceling electromagnetic fields, dramatically reducing the electromagnetic emissions. Finally, this circuit has a low susceptibility to externally generated noise.
LVDS drivers and receiver are usually connected point-to-point, as shown in Fig. 1.1. In this configuration, the LVDS interface achieves high data rate, while using little power. However, other configurations are possible.

Chapter 2

Transmission line

SLVS transmitter is a *current-mode* driver as opposed to the more common voltage-mode driver. It delivers a tunable current of $I = (500 + b_1 + 2b_2 + 4b_3)$ μA, which produces a differential voltage, ranging from 50 mV to 400 mV, across a 100 Ω termination resistance. These low signal swings reduce power consumption and together with differential signaling, which reduces noise coupling, allow for higher signaling rates.

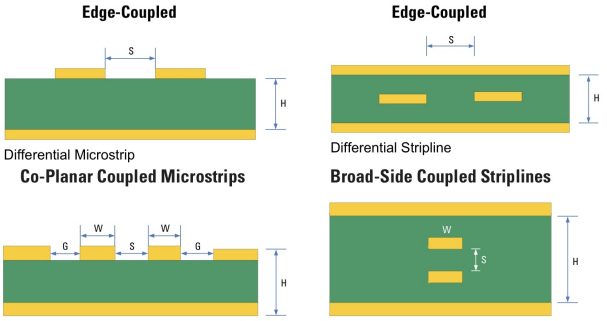

Figure 2.1: Possible pcb configurations. *Credits:* [7]

2.1 Differential signaling

Differential signaling [3] is a special case of two-wire signaling that involves the transmission of two complementary signals on equal and matched traces.
High speed differential wiring is often called balanced wiring. Twisted pair and quad configuration are the most common types balanced wiring.
High speed differential pcb traces must have:

- equal characteristic impedances;
- equal impedances to the surrounding reference system;
- equal propagation delay.

Most common trace configurations that meet these requirements are: differential edge-coupled microstrip and stripline, co-planar coupled microstrips and broad-side coupled striplines. These configuration are shown in Fig. 2.1.
A differential signaling system has a certain degree of immunity from other circuits that induce current in the reference structure. In fact, a differential receiver does not need the reference voltage to be the same everywhere, as long as the difference between the reference voltages is such that the received signal does not exceeds the common mode operating range of the receiver. Moreover, if the wires have equal coupling to the reference system, there is no current induced in the reference system. While, if the two impedances are not matched, a common-mode current flows in the reference system.
Either a weak-coupling approach or a precise-coupling approach can be used to reduce common-mode current. The first is used in twisted pairs and consists only in thickening the cable plastic jacket, to better isolate the conductors from the outside. The latter is used in pcb applications and consists in precisely balancing the coupling of each trace to ground; this is achieved using identical traces.

2.1.1 Termination resistance

The value of the termination resistance should be matched with the transmission line's characteristic impedance to reduce reflected signals that may increase data errors. The allowable reflection depends primarily upon noise margin, but generally matching the nominal characteristic impedance of the cable to ±10% of the termination resistance is sufficient [2]. Accordingly to EIA/TIA-644-A [10] and IEEE Std. 1596.3-1996 [5], the termination resistance is to be between 90 Ω and 132 Ω.
In this report, a 100 Ω termination resistance is used. This termination eliminates all differential mode signals' reflections but does not provide any termination for common mode signals. In fact, a single termination resistance drives zero current and acts as an open circuit with respect to a common mode signal. Note that it is important to eliminate both reflections because, once created at the receiver end, the common mode noise returns back to the driver; there, if it finds a low or high resistance, it starts bouncing back and forth between the receiver (open circuit) and the driver (low impedance). In particular circumstances, the common mode artifacts can superimpose, increasing common mode noise and radiated emission [3].
In literature, it is possible to find termination schemes that enable the elimination of reflections for both differential and common-mode signals. Most used one is $T-$termination (or split termination) [3], [9], [6]. In this scheme two resistance of half the differential impedance of the line are used, together with a capacitor (Fig. 2.2). The capacitance's value must be such that it looks like a short circuit for the AC component of the signal.
Adding a termination resistor at the transmitter end [1], [3] (LVDS Signaling section), helps reducing residual reflections of the differential mode, caused by crosstalk or imperfect termination. According to [10] and [5] the transmitter termination is to be between 40 and 140 Ω. However, this resistor would drain current from the transmission line, lowering the output. To obtain the same output the signal current must be increased, but this results in an increase in power consumption. That is why the second termination resistance is not used in this design.

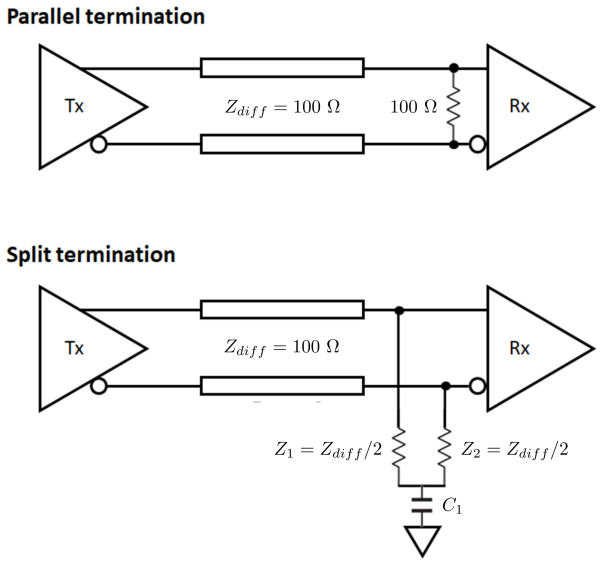

Figure 2.2: Single resistor termination (used in this design) and $T-$termination schemes.

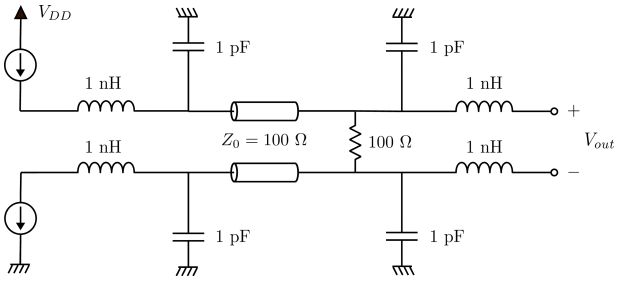

Figure 2.3: Transmission line testbench schematic.

2.2 Simulation results

Transmission line testbench schematic is represented in Fig. 2.3. A lossless transmission line with $Z_0 = 100\ \Omega$ was used to mimic the behavior of a 100 Ω (differential impedance) twisted pair. The transmission line is 0.1 m long and has a propagation velocity of $0.7c$. The 1 nH inductors and 1 pF capacitors were added to simulate wirebonds.
The transmission line was tested to determine its maximum operating frequency (aiming for a frequency higher than 2.56 Gbps). For this purpose,

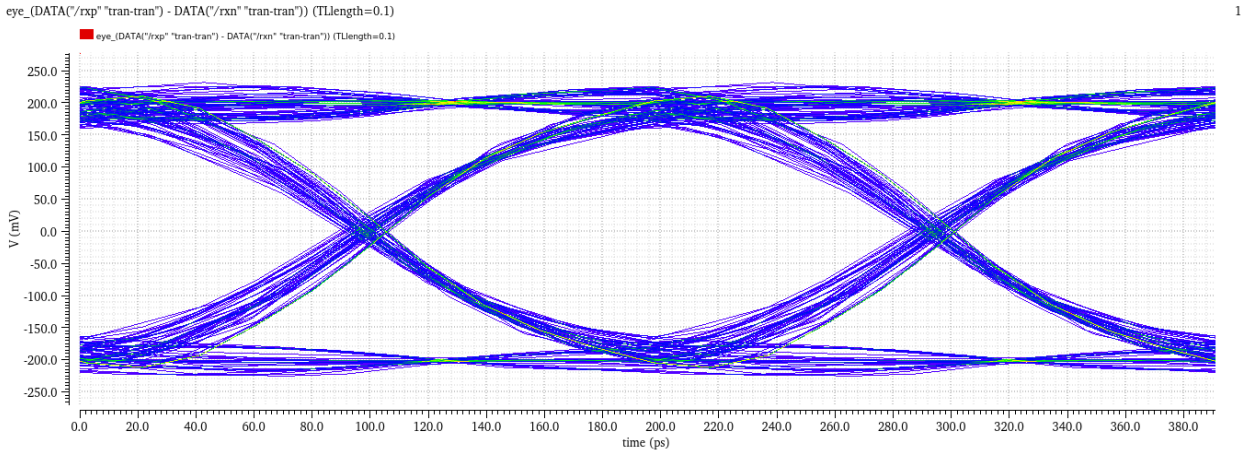

Figure 2.4: V_{out} eye-diagram at 2.56 Gbps.

eye's measurements were extracted from the output eye diagram (Fig. 2.4). Frequency was increased until eye's height dropped below half the ideal height (400 mV with a 4 mA signal current) or until jitter exceeded 5%. This setup met all constraints even at frequencies higher than 10.24 Gbps.

As a lossless line was used, all the imperfections in the eye diagram and the degradation of its measurements are attributable to impedance mismatch caused by wirebonds. When a real line is used, its characteristics should be the most determining factor in the overall system performance. The highest signaling rate would then be determined mainly by its length and other parameters [2].

Tests with a real line were not done due to the lack of time.

Chapter 3

Transmitter

The role of the transmitter is to produce a low and negative voltage at the two input terminals of the receiver if the input is a logic 0 and an always low but positive voltage if the input is a 1. To achieve this, a tunable current is made to flow downside up in the 100 Ω termination resistance with a logic 0 and upside down with a 1.
The transmitter block diagram is shown in Fig. 3.1. It is composed of a pre-driver which switches from $V_{DDL} = 0.8$ V to $V_{DD} = 1.8$ V and generates the core's input signals (V_{ip} and V_{in}), a voltage reference which creates a voltage V_{ref} of half the supply voltage, a bias circuit, which produces the two proper voltages (V_{pt} and V_{cmfbt}) needed to bias two current sources inside the core, and the core which steers the current in the termination resistance.

3.1 Core

The core is composed of a bridge and a Common Mode FeedBack circuit (Fig. 3.2). The bridge is what actually steers the current flowing in the termination resistance. The CMFB keeps the output common mode V_{cm} as close as possible to V_{ref} (half the supply voltage), acting on V_{nt}.

3.1.1 Bridge

The bridge circuit is represented in Fig. 3.3. The $p-$tail current is imposed by V_{pt}, coming from the bias circuit. The $n-$tail current, instead, is imposed by V_{nt} coming from the CMFB.
When the input is a 1 (Fig. 3.4), M_3 is an open cir-

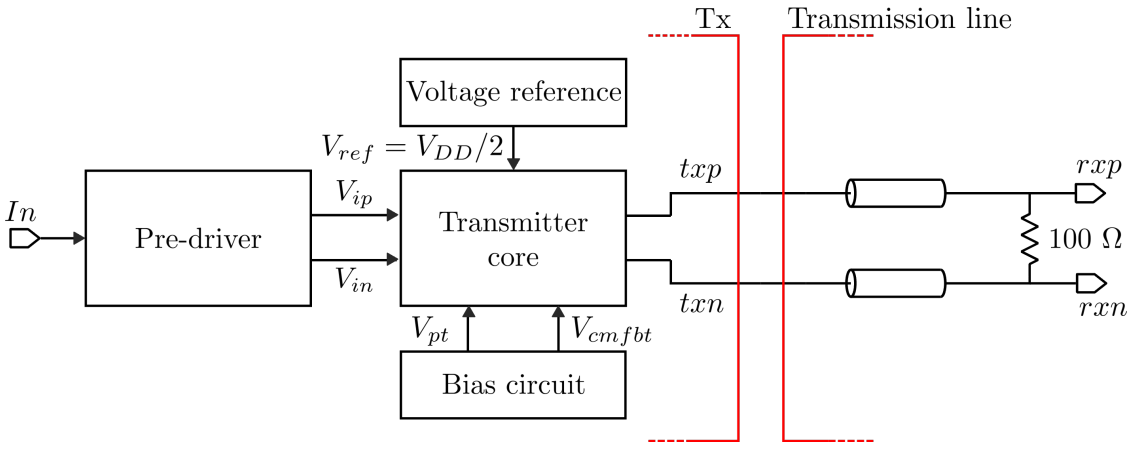

Figure 3.1: Transmitter block diagram.

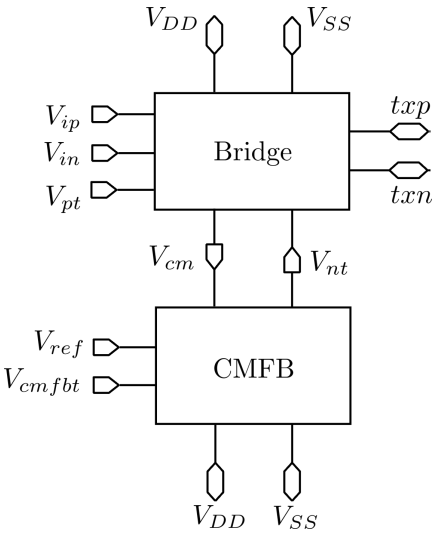

Figure 3.2: Core block diagram

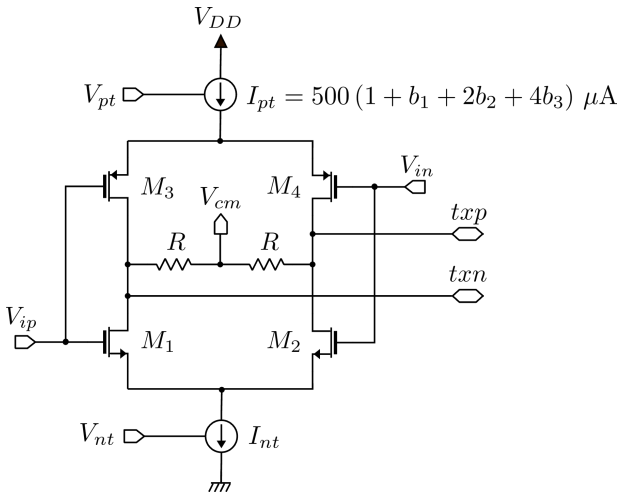

Figure 3.3: Bridge schematic

cuit, while M_1 is a closed circuit. On the opposite site, the inverted input is a 0, and so M_4 is a closed circuit and M_2 is an open circuit. In this way, the current flows upside down in the termination resistance, producing a positive output.
When the input is a 0 (Fig. 3.5), M_3 is a closed circuit and M_1 is an open circuit. The inverted input is a 1, M_4 is an open circuit and M_2 is a closed circuit. This time, the current flows downside up on the termination resistance, producing a negative output.
Signal current can be tuned with 3 control bits b_1, b_2 and b_3, in according to Tab. 3.1. The bits and their complements control six $p-$MOS switches to set I_{pt}. The BGP voltage of these switches is V_{SS}, so that they do not leak any current: with $BGP = -2.5$ V, their V_{tp} would have become positive and so they could have conducted some current even with a null V_{GS}. For the same reason, also the transistors that make up the $p-$tail mirror have $BGP = V_{SS}$.
The bits and their complements also control six $n-$MOS switches to set I_{nt}. The BGN voltage of these switches is again V_{SS}: with $BGN = 2.5$ V, their V_{tn} would have become negative and so they could have conducted some current even with a null V_{GS}. Instead, the transistors that make up the $n-$tail mirror have $BGN = 2.5$, as from simulations they did not seem to leak any current. So, leaving $BGN = 2.5$ V allows them to be made smaller.
Other two $p-$MOS switches and two $n-$MOS switches were added to the always-on branches of the $p-$tail and $n-$tail (which produce the 500 μA current). They are controlled by a tie-high and a tie-low circuit. This is necessary to make the layout more symmetrical.
The width of the switches $M_1, \ldots, M_4$ was increased until their R_{on} dropped below 25 Ω. To obtain equal R_{on}, $p-$MOS (M_3 and M_4) are larger than $n-$MOS (M_1 and M_2). In this way, even with $I_{pt} = 4$ mA:

$$\begin{aligned} &V_{DD} - V_{SS} = 1800 \text{ mV} = \\ &= |V_{DSpt}| + R^p_{on} I_{pt} + 400 \text{ mV} + R^n_{on} I_{pt} + V_{DSnt} = \\ &= 2V_{DSt} + 2R_{on} I_{pt} + 400 \text{ mV} = 2V_{DSt} + 600 \text{ mV} \end{aligned}$$

So, in the worst case, $V_{DSt} = \min\{V_{DSt}\} = 600$ mV. The BGP of M_3 and M_4 is -2.5 V. In fact:

$$V_{S3} = V_{S4} = V_{DD} - |V_{DSpt}| \leq 1.2 \text{ V}$$

where equality holds (approximately) with $I_{pt} = 4$ mA. So, when V_{G3} or V_{G4} is equal to V_{DD}, the corresponding V_{GS} would be greater then 600 mV. With $BGP = -2.5$ V, the threshold voltage of M_3 and M_4 becomes positive ($\simeq$ 200 mV). Anyway, having

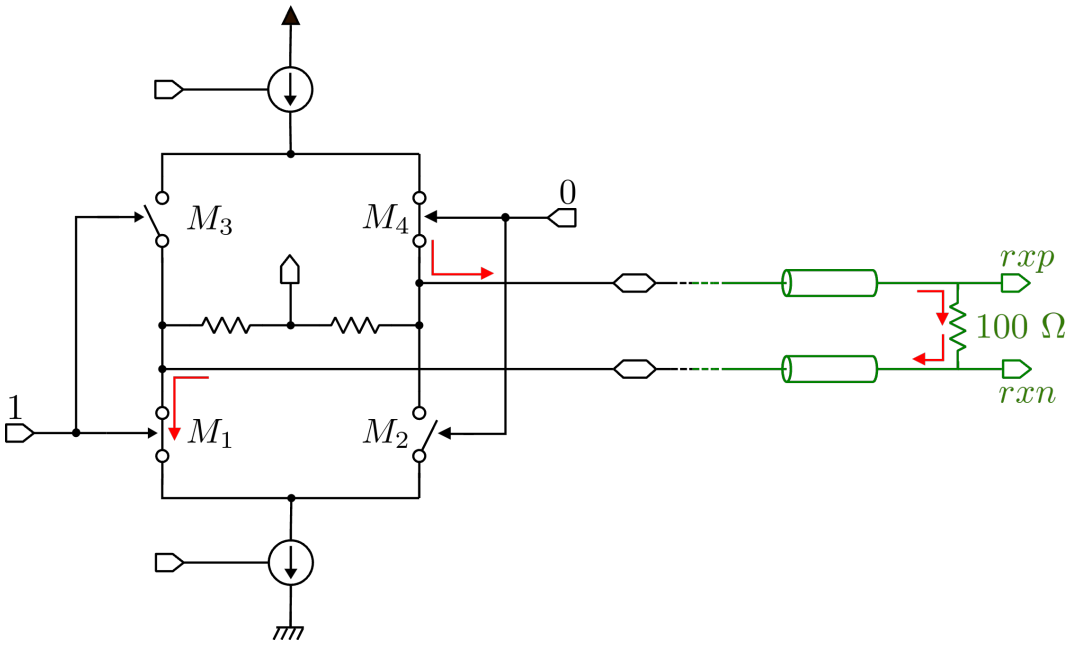

Figure 3.4: Simplified representation of the behavior of the bridge with a logic 1 as input

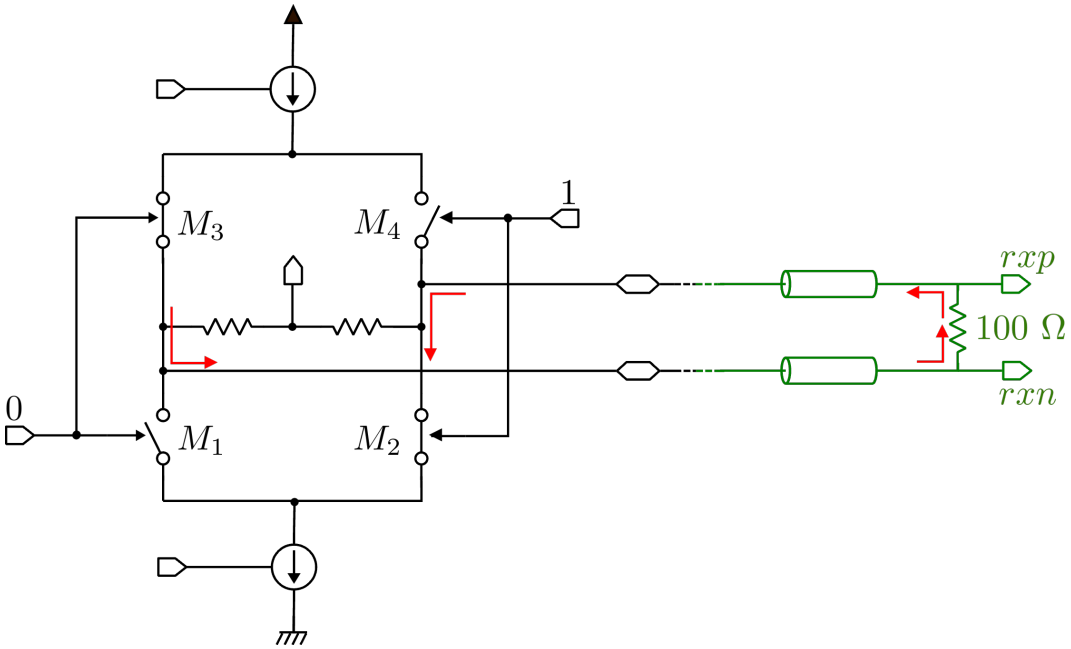

Figure 3.5: Simplified representation of the behavior of the bridge with a logic 0 as input

$\mathbf{b_1}$	$\mathbf{b_2}$	$\mathbf{b_3}$	$\mathbf{I_{pt}}$ (mA)	$\mathbf{V_{out}}$ (mV)
0	0	0	0.5	50
0	0	1	1	100
0	1	0	1.5	150
0	1	1	2	200
1	0	0	2.5	250
1	0	1	3	300
1	1	0	3.5	350
1	1	1	4	400

Table 3.1: I_{pt} and V_{out} values with all possible (b_1, b_2, b_3) combinations

$V_{GS} > V_{tp}$, these transistor would be off. So, setting their BGP to -2.5 V, allows them to be made smaller and to switch faster.
The same applies to M_1 and M_2: $V_{S1} = V_{S2} \geq 600$ mV. So, when V_{G1} or V_{G2} equals V_{SS}, the switch would have $V_{GS} \leq -600$ mV, which is lower than V_{tn} even with $BGN = 2.5$ V ($V_{tn}(BGN = 2.5\text{ V}) > -200$ mV).

3.1.2 CMFB

The CMFB circuit (Fig. 3.6) senses the bridge output common mode V_{cm} with two resistors R_{cm} and compares it with $V_{ref} = V_{DD}/2$. The value of R_{CM} is approximately 10 kΩ, so that they do not drain too much current from the transmission line. Then it acts on V_{nt} to adjust the current I_{nt}, such that:

- if V_{cm} is smaller than V_{ref}, I_{nt} is reduced and V_{cm} is increased to get it closer to V_{ref};
- if V_{cm} is bigger than V_{ref}, the circuit acts to increase I_{nt} and so decrease V_{cm}, again to get it closer to V_{ref}.

The resistance R_M and the capacitance C_M are used for stability compensation. Their values was chosen with the aid of the simulator, because hand calculations did not produce valid results.

3.1.3 Simulation results

The performance of the bridge were tested with a perfect voltage source driving it. The source produced a pseudo-random bit sequence at 2.56 Gbps. Bridge's output voltage when $I_{pt} = 400$ mA is represented in Fig. 3.7 together with the corresponding eye diagram. Common mode noise resonance was not observed, probably thanks to the inductors and the capacitances added to simulate wirebonds, which can act as a $\Pi-$termination for common mode signals.
The stability analysis of the CMFB is performed through an iprobe from *analogLib*. The probe was connected in the testbench schematic where the transmitter symbol is instantiated. A phase margin of 55° was reached with a resistor of 1.6 kΩ and a capacitance of 1 pF (Fig. 3.8). This is not an excellent phase margin, but is still decent. Of course a bigger capacitance would allow for bigger phase margins, but bode plots started exhibiting strange behaviors when the capacitance was increased to 2 pF.

3.2 Predriver

The predriver is made up of a level shifter and two inverter chains (Fig. 3.9).
One chain has an even number of inverters to produce the non-inverted input of the bridge. The other one has an odd number of inverters to produce the inverted input.
The level shifter transforms a low V_{DDL} of 0.8 V into an higher V_{DD} of 1.8 V, while leaving a null voltage unchanged.

3.2.1 Inverter chains

The two inverter chains were designed with the aim of minimizing power consumption, while keeping the outputs rise and fall times below a maximum value.
For this analysis a simplified switch-model of the inverter is used (see Fig. 3.10). In this way the gate transient behavior is determined by its output capacitance C_L and on-resistance R_n or R_p, depending on which transient we are considering.
The two propagation delays, t_{pHL} and t_{pLH}, are measured between the 50% transition point of the input

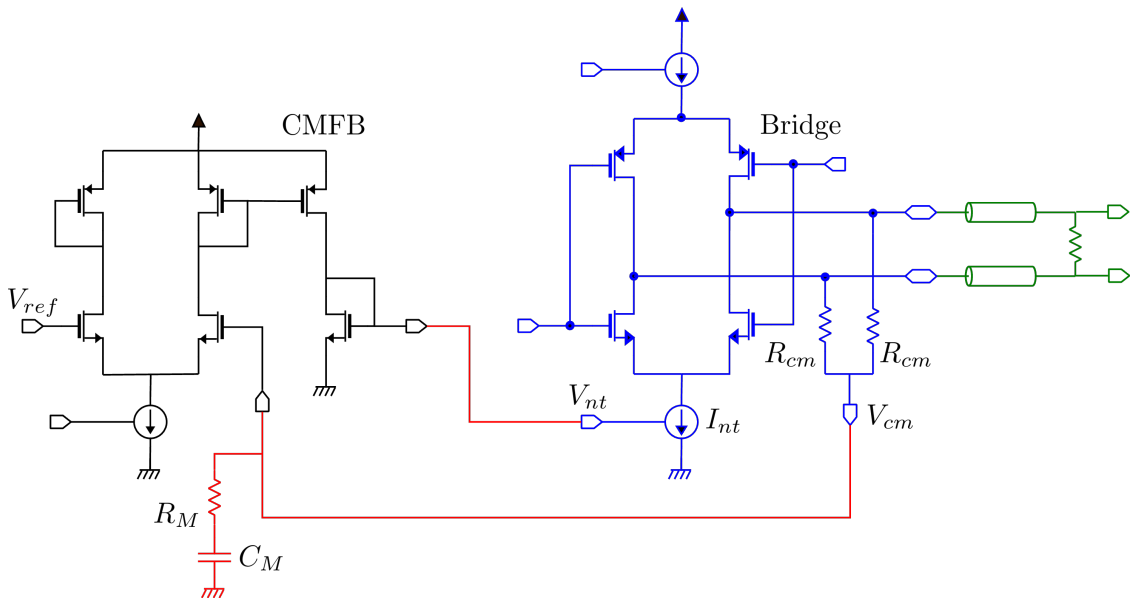

Figure 3.6: CMFB circuit

and output waveforms, as shown in Fig. 3.11. t_p is defined as the mean of the two:

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} \tag{3.1}$$

t_{pHL} is the propagation delay for an high to low transition, while t_{pLH} is for a low to high transition. This two response times are in general different, but can be made equal with a proper design. Although this may not be the best solution to minimize t_p [8], surely it creates an inverter with symmetrical VTC and simplifies the analysis a lot. Thus, all of the following inverters will be designed such that $t_{pHL} = t_{pLH} = t_p$. With these definitions and using the switch-model, it is possible to find simple expressions for t_{pHL} and t_{pLH}, when the inverter is driven by an ideal gate (with zero rise and fall times):

$$\begin{aligned} t_{pHL} &= \ln(2)\, R_n C_L \\ t_{pLH} &= \ln(2)\, R_p C_L \\ t_p &= \ln(2) \frac{R_n + R_p}{2} C_L \end{aligned} \tag{3.2}$$

as for a simple $RC-$network. From there, it becomes evident that achieving $t_{pHL} = t_{pLH}$ requires matching the two resistances: $R_n = R_p = R_{eq}$. Also t_{rise} and t_{fall} can be determined to be:

$$t_{rise} = t_{fall} = \ln(9)\, R_{eq} C_L \tag{3.3}$$

Unfortunately, both R_{eq} and C_L depend non-linearly on V_{out}, making an exact computation of t_p intractable. This problem can be overcome by replacing both with linear elements which values are the average of the resistance and capacitance over the interval of interest.
Calculations for R_n and R_p are found in Eq. (3.4). As $R_n = R_n((W/L)_n, BGN)$ and $R_p = R_p((W/L)_p, BGP)$, these four parameters (transistors' lengths are supposed to be: $L_n = L_p = L_{min}$) of the inverter must be chosen in such a way that $R_n = R_p = R_{eq}$.
For C_L refer to Fig. 3.13, where all the capacitances influencing the transient response of node V_{out} are shown. These capacitances can be gathered into a single capacitor C_L placed between V_{out} and ground. Note that C_{g1} and C_{g2} are also present. However, they do not influence V_{out} transient behavior and so are not depicted in the Figure. Following this

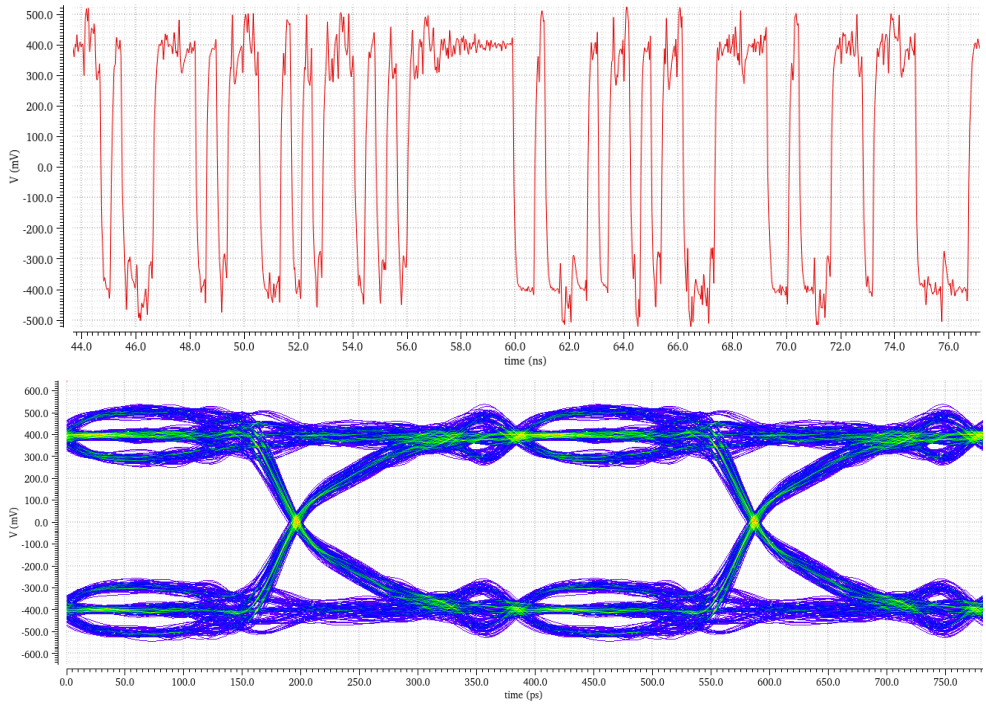

Figure 3.7: Output voltage of the bridge and corresponding eye diagram when $I_{pt} = 400$ mA

schematization, the load capacitance C_L can be broken into four major contributions:

1. Gate-Drain capacitance C_{gd12}, proportional to gate area (of the first inverter). Thanks to Miller effect, this floating capacitance can be replaced with two capacitances of value $2C_{gd12}$, one placed between V_{in} and ground (which does not influence V_{out}) and the other between V_{out} and ground.

2. Diffusion capacitances C_{db1} and C_{db2}, also proportional to gate area (of the first inverter). Together with the $2C_{gd12}$ output capacitance, they constitute the *intrinsic* or self-loading output capacitance of the first inverter.

3. Wiring capacitance C_w.

4. Gate capacitance of fanout C_{g3}, C_{g4} and $2C_{gd34}$ (although not represented), proportional to gate area (of the second inverter). Together with C_w, they constitute the *extrinsic* output capacitance of the first inverter.

Variations in the capacitances' values occurring during transitions will be ignored. So C_L can be written as:

$$C_L = C_{int} + C_{ext} \tag{3.5}$$

with C_{int} consisting of the diffusion capacitances of the NMOS and PMOS and of the gate-drain Miller capacitance (thus related to the first inverter's own gate area), and C_{ext} attributable to wiring and fanout. Ignoring C_w (as done for the rest of the discussion), even C_{ext} depends on the second inverter's gate area.
With this representation results found in Eq. (3.2)

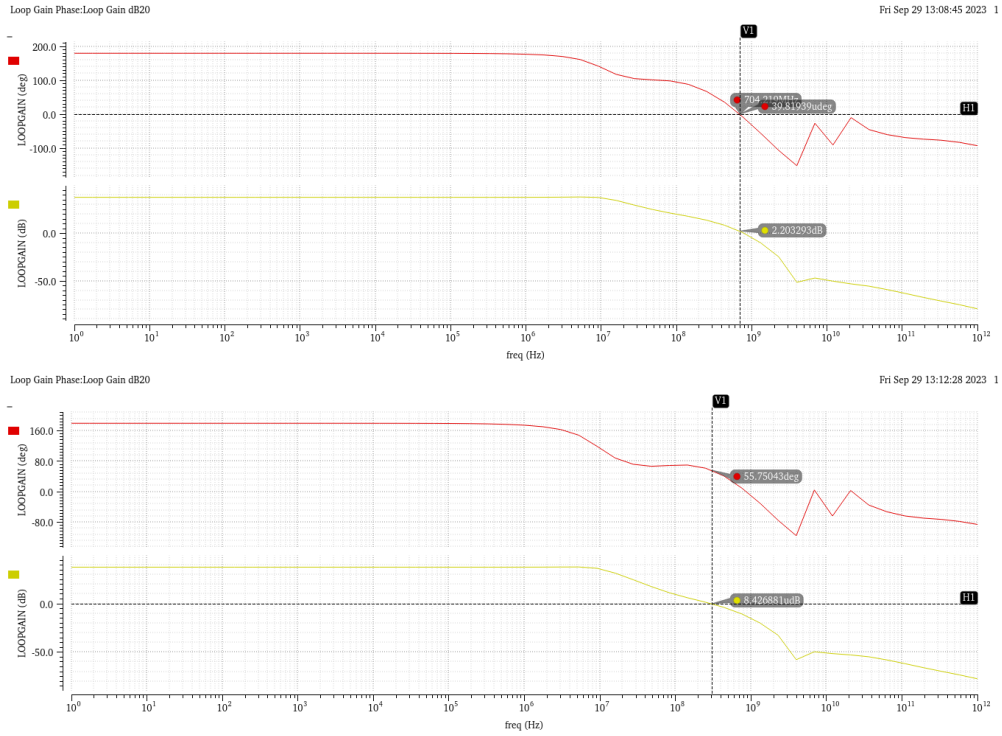

Figure 3.8: Core loop gain βA when non-compesated (1) and when compensated with $C_M = 1$ pF and $R_M = 1.6$ kΩ (2)

and (3.3) can be rewritten as:

$$t_p = \ln(2)\, R_{eq} C_{int} \left(1 + \frac{C_{ext}}{C_{int}}\right)$$
$$t_{rise} = t_{fall} = \ln(9)\, R_{eq} C_{int} \left(1 + \frac{C_{ext}}{C_{int}}\right) \tag{3.6}$$

Note that the first inverter also has an input capacitance, composed by the two gate capacitance C_{g1} and C_{g2} and the $2C_{gd12}$ Miller capacitance on the input side. Since all these components are proportional to the gate area of the first inverter, even its input ca-

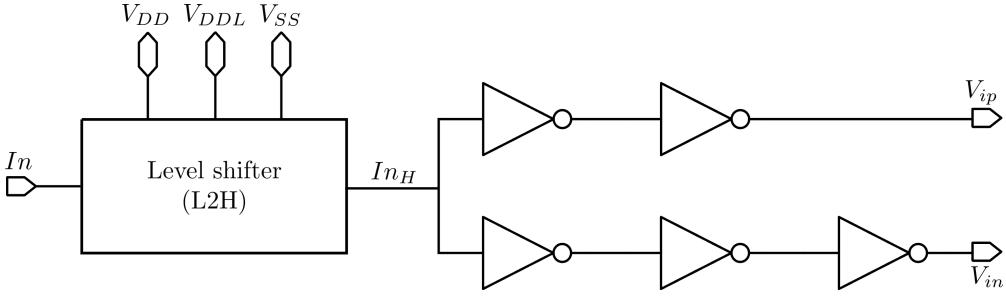

Figure 3.9: Predriver block diagram

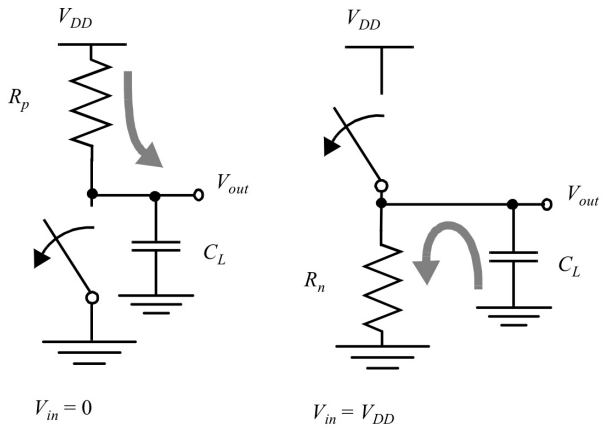

Figure 3.10: Switch model of static CMOS inverter. *Credits:* [8]

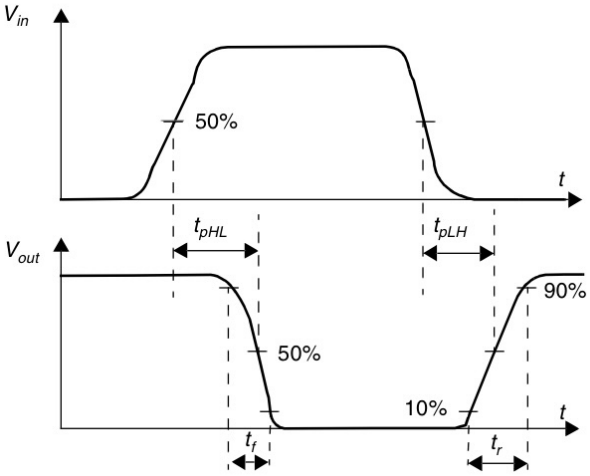

Figure 3.11: Propagation delays and rise and fall times for an inverting gate. *Credits:* [8]

pacitance, named C_g, is proportional to gate area, as well as its output capacitance C_{int}. This allows for writing:

$$C_{int} = \gamma C_g \tag{3.7}$$

Here γ is a proportionality factor, which only depends on the technology and is usually close to 1 for submicron processes. So t_p expression in Eq. (3.6) becomes:

$$\begin{aligned} t_p &= \ln(2)\, R_{eq} C_{int} \left(1 + \frac{C_{ext}}{\gamma C_g}\right) = \\ &= \ln(2)\, R_{eq} C_{int} \left(1 + \frac{f_{1,2}}{\gamma}\right) = \\ &= t_0(1 + \bar{f}_{1,2}) \end{aligned} \tag{3.8}$$

where $f_{1,2} = C_{ext}/C_g$ is the *effective fanout* of inverter 1 driving inverter 2, $\bar{f}_{1,2} = f_{1,2}/\gamma$ and t_0 is the propagation delay of the inverter when loaded only by its own intrinsic capacitance ($C_{ext} = 0$). Scaling both W_n and W_p of the first inverter by a factor S

$$W_n \longrightarrow SW_n, \quad W_p \longrightarrow SW_p$$

makes the equivalent resistance $S-$times smaller (I_{DSAT} at the denominator increases by a factor S) and the input and intrinsic capacitances $S-$times bigger (gate area increases by a factor S).

$$R_{eq} \rightarrow R_{eq}/S, \quad C_g \rightarrow SC_g, \quad C_{int} \rightarrow SC_{int}$$

When the inverter is scaled by S, t_p reduces to:

$$\begin{aligned} t_p &= \ln(2)\,(R_{eq}/S)(SC_{int}) \left(1 + \frac{C_{ext}}{\gamma SC_g}\right) = \\ &= t_0 \left(1 + \frac{\bar{f}_{1,2}}{S}\right) \end{aligned} \tag{3.9}$$

Eq. (3.9) leads to two significant conclusions:

1. t_0 is independent of the gates' sizes ($R_{eq} \propto 1/W$, $C_{int} \propto W$) and (if V_{DD} is fixed) depends only on BGN and BGP, by means of V_{tn} and V_{tp}.

2. Making S infinitely large produces the maximum performance gain.

The second conclusion is only true when the inverter is driven by an ideal driver. When the inverter is driven by a real gate, a large S would make C_g too big: first inverter's C_g would be the fanout extrinsic capacitance of its driving gate, slewing down its transient response. To take into account the charging

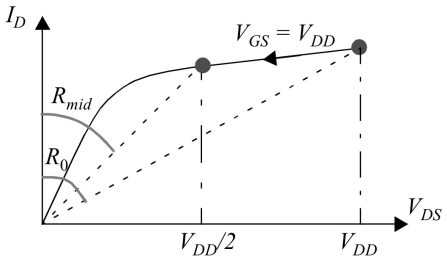

Figure 3.12: $I-V$ trajectory followed by the operating point of the NMOS of an inverter during a $H \to L$ transition. The instantaneous resistance is equal to v_{DS}/i_D and is visualized by the angle with respect to $y-$axis. *Credits:* [8]

$$R_n = \frac{-2}{V_{DD}} \int_{V_{DD}}^{V_{DD}/2} \frac{V}{I_{DSATn}(1+\lambda V)}\, dV \simeq \frac{3}{4}\frac{V_{DD}}{I_{DSATn}}\left(1 - \frac{7}{9}\lambda V_{DD}\right)$$

$$I_{DSATn} = k(V_{DSATn})\,\mu_n C_{ox}\frac{W_n}{L_n}\left[(V_{DD} - V_{tn})V_{DSATn} - \frac{V_{DSATn}^2}{2}\right]$$

$$k(V) = \frac{1}{1 + V/(\xi_c L_n)} \qquad V_{DSATn} = k(V_{DD} - V_{tn})\,(V_{DD} - V_{tn})$$

$$R_p = \frac{2}{V_{DD}} \int_{V_{DD}/2}^{V_{DD}} \frac{V}{I_{DSATp}(1+\lambda V)}\, dV \simeq \frac{3}{4}\frac{V_{DD}}{I_{DSATp}}\left(1 - \frac{7}{9}\lambda V_{DD}\right) \tag{3.4}$$

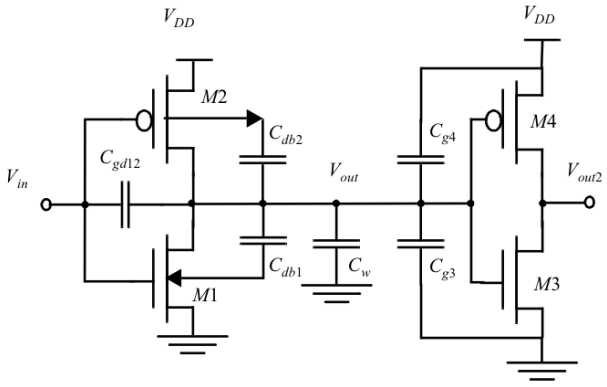

Figure 3.13: Parasitic capacitances influencing the transient of V_{out} in a cascaded inverter pair. *Credits:* [8]

effect of C_g on the driving gate, the following model can be used [4]:

$$t_{p,\text{inv1}} = t_{p,\text{inv1}}(\text{step}) + \eta t_{p,\text{driving gate}}(\text{step}) \tag{3.10}$$

where $t_p(\text{step})$ is the propagation delay of a gate for a perfect step input (e.g. the input produced by an ideal gate) and η is a proportionality factor. So $t_p(\text{step})$ is equal to t_p in Eq. 3.6.
According to this model, the propagation delay of the i inverter of a chain, driven by the $(i-1)$ inverter and driving the $(i+1)$, is:

$$t_{p,i} = t_{0,i}\left(1 + \bar{f}_{i,i+1}\right) + \eta t_{0,i-1}\left(1 + \bar{f}_{i-1,i}\right) \tag{3.11}$$

This model is in good agreement with simulation results and still allows for simple calculations. Simulations showed that even the rise and fall times depend almost linearly on the rise time of the driving gate, but far less than the propagation delay. Thus, to simplify the discussion, these variations of rise and fall times were not considered. In this way, t_{rise} and t_{fall} are linked to $t_p(\text{step})$ as shown in Eq. 3.6.
Theoretically $t_{0,i}$ and $t_{0,i-1}$ in Eq. (3.11) can be different:

- t_0 depends (to a first order) on 4 DOFs: W_n, W_p, BGN, BGP;
- setting $R_n = R_p$ leaves 3 DOFs (e.g. W_p/W_n, BGN, BGP);
- $R_{n,i} = R_{p,i}$ and $R_{n,i-1} = R_{p,i-1}$ can both be achieved, even with $(W_p/W_n)_i \neq (W_p/W_n)_{i-1}$, by choosing BGN_i, BGP_i and BGN_{i-1}, BGP_{i-1} appropriately;
- this can lead to $t_{0,i} \neq t_{0,i-1}$.

Allowing for differences in t_0 would require a computational demand far beyond the scope of this analysis. Therefore, another design constraint is introduced:

- BGN_{ref}, BGP_{ref}, $(W_p/W_n)_{ref}$ are chosen for a *reference inverter* in such a way that $R_{n,ref} = R_{p,ref}$;
- $W_{n,i}$ and $W_{p,i}$ of each inverter are scaled by an equal factor with respect to $W_{n,ref}$ and $W_{p,ref}$, while BGN_i and BGP_i are set equal to BGN_{ref} and BGP_{ref}.

Consequently, if

$$\left(\frac{R_p}{R_n}\right)_{ref}\left((W_p/W_n)_{ref},\ BGN_{ref},\quad BGP_{ref}\right) = 1$$

then

$$\left(\frac{R_p}{R_n}\right)_{i}\left((W_p/W_n)_{i},\ BGN_{i},\quad BGP_{i}\right) =$$

$$= \left(\frac{R_p}{R_n}\right)_{i}\left((W_p/W_n)_{ref},\ BGN_{ref},\quad BGP_{ref}\right) = 1$$

Now that the model has been fully described, it is time to focus on the LVDS predriver. It counts two inverter chains:

1. The first one, which inverters are labeled with i, is called the $I-$chain and contains M inverters, with M being and even number.
2. The second one, which inverters are labeled with j, is called the $J-$chain and contains N inverters, with N being and odd number.

Both the chains are driven by the level shifter, that ends with another inverter, called the $\omega-$inverter. This allows to use Eq. (3.11) for the propagation delays of the inverters ($i = 1$) and ($j = 1$). On the other side, the last inverters of both chains drive the gate capacitance of the bridge's switches. As the two $n-$switches and the two $p-$switches of the bridge are equal, it is possible to say that:

$$C_{ext,i=M} = C_{ext,j=N} = C_L \tag{3.12}$$

where C_L is known.
Applying Eq. (3.11) for all the inverters, the total

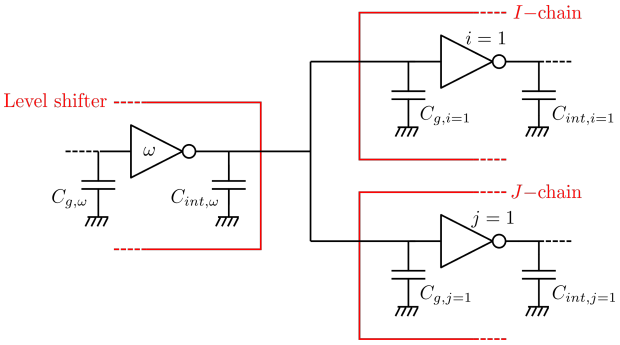

Figure 3.14: Inverter ω of level shifter driving first inverters of the $I-$chain and $J-$chain.

propagation delays of the chains are:

$$\begin{aligned} t_{ptotI} &= \eta t_0(1 + \bar{f}_{\omega,i=1} + \bar{f}_{\omega,j=1}) + \\ &+ (1+\eta)t_0 \sum_{i=1}^{M-1}(1 + \bar{f}_{i,i+1}) + \\ &+ t_0(1 + \bar{f}_{M,L}) \\ t_{ptotJ} &= \eta t_0(1 + \bar{f}_{\omega,i=1} + \bar{f}_{\omega,j=1}) + \\ &+ (1+\eta)t_0 \sum_{i=1}^{N-1}(1 + \bar{f}_{j,j+1}) + \\ &+ t_0(1 + \bar{f}_{N,L}) \end{aligned} \tag{3.13}$$

A fundamental design constraint is:

$$t_{ptotI} = t_{ptotJ} \tag{3.14}$$

If this constraint were not met, the duty cycle would be severely distorted.
Other design constraints are:

$$\begin{aligned} t_{rise}(V_{ip}) &= t_{fall}(V_{in}) < 50 \text{ ps} \\ t_{fall}(V_{ip}) &= t_{rise}(V_{in}) < 50 \text{ ps} \end{aligned} \tag{3.15}$$

As mentioned above, rise and fall times of an inverter are proportional to its t_p(step). If all t_0 are equal, t_p(step) depends only on f (effective fanout. See Eq. 3.6 and 3.8). So this constraints implies matching

$$C_{totI} = C_{g,i=1}\left\{(1+\gamma)\left[1+\sum_{i=1}^{M-1}\left(\prod_{k=1}^{i} f_{k,k+1}\right)\right]+\prod_{i=1}^{M} f_{k,k+1}\right\} \quad \text{with: } f_{M,M+1} = f_{M,L} \tag{3.19}$$

$$C_{totJ} = C_{g,j=1}\left\{(1+\gamma)\left[1+\sum_{j=1}^{N-1}\left(\prod_{k=1}^{j} f_{k,k+1}\right)\right]+\prod_{j=1}^{N} f_{k,k+1}\right\} \quad \text{with: } f_{N,N+1} = f_{N,L} \tag{3.20}$$

---

the effective fanouts of the last inverters of the two chains.

The power dissipation of an inverter can be attributed to three main contributions: dynamic power, direct path power and static power consumption.

Dynamic power

Dynamic power consumption of an inverter is due to charging and discharging its load capacitance (intrinsic and extrinsic). Each switching cycle, consisting of $L \to H$ and $H \to L$ transitions, drains the same amount of energy

$$E_{dyn} = C_L V_{DD}^2 \tag{3.16}$$

from the power supply. For a chain of L inverters with a final load capacitance C_L, each time the input completes a switching cycle, all the $2L+1$ capacitances (C_g and C_{int} for each inverter, plus C_L) are charged and discharged. If C_{tot} is defined to be the sum of all these capacitances, then the dynamic energy required by the chain during the switching cycle is

$$E_{dyn,\text{chain}} = C_{tot} V_{DD}^2 \tag{3.17}$$

Thus for the $I-$chain and the $J-$chain:

$$E_{dynI} = C_{totI} V_{DD}^2, \quad E_{dynJ} = C_{totJ} V_{DD}^2 \tag{3.18}$$

Full expression for C_{totI} and C_{totJ} are found in Eq. (3.19) and Eq. (3.20), were all capacitances have been related to $C_{g,i=1}$ and $C_{g,j=1}$ respectively (be aware that effective fanouts $f_{k,k+1}$ are used here). Note that, with a fixed V_{DD}, the only means to reduce E_{dyn} is acting on effective fanouts.

Direct path power

Due to the finite slope of the input signal, there is a short period of time during switching when both the $n-$MOS and the $p-$MOS of an inverter conduct. If the resulting current spikes can be modeled as triangles, the energy lost per switching period for this direct path between V_{DD} and ground is:

$$E_{dp} = t_{sc} V_{DD} I_{peak} \tag{3.21}$$

Here, t_{sc} is the time both transistors conduct. If t_{sw} is the $0\% \to 100\%$ transition time of the input (see Fig. , t_{sc} is approximately given by:

$$t_{sc} \simeq \frac{V_{DD}-2V_t}{V_{DD}} t_{sw} \simeq \frac{V_{DD}-2V_t}{V_{DD}} \frac{t_{r/f}}{0.8} \tag{3.22}$$

where $t_{r/f}$ is t_{rise} or t_{fall} depending on the transition. Increasing V_t reduces the voltage range $V_{DD}-2Vt$ in which both transistors are on, but also increases t_0 and therefore $t_{r/f}$. The contribution of V_t to E_{dp} is difficult to account for.
I_{peak} depends on the saturation current and on the ratio between the inverter's input and output slopes: direct path power consumption of a single inverter is minimized by making the output rise and fall times bigger than the input's ones. This produces only a local optimization as it causes short-circuit in the fanout gates. A rule of thumb for global optimization is to match rise and fall times of all inverters in a chain [11]. As mentioned before, rise and fall times of an inverter are proportional to its t_p(step), that (if all t_0 are equal) depends only on f (effective fanout. See Eq. 3.6 and 3.8). So this rule of thumb implies matching the effective fanouts of each gate.

Static power

Static power consumption is given by:

$$P_{stat} = I_{leak} V_{DD} \tag{3.23}$$

where I_{leak} is the subthreshold current of the transistors: MOS transistors can have a non-zero current even if their $|V_{GS}|$ is smaller than $|V_t|$. This current depends primarily on $|V_t|$:

$$I_{leak} \propto \frac{W}{L} e^{-\frac{|V_t|}{V_T}} \tag{3.24}$$

Thus, to offset static consumption, $|V_t|$ should be kept high. Nevertheless, increasing the threshold voltage with fixed V_{DD} significantly worsens performance (increases t_0). To solve trade-off between static power consumption and performance, V_{tn} and $|V_{tp}|$ should be chosen (tuning BGN and BGP) as high as possible, while still allowing to meet the rise and fall time specifications without using too big transistors (which worsen dynamic power consumption).

Simulations showed that the major contribution to power consumption is provided by dynamic power. The rule of thumb for reducing direct path power is also followed. So the dimensions of the inverters were chosen as small as possible and with matched fanouts. Unfortunately, if $t_{ptotI} = t_{ptotJ}$ is to be true, fanouts can not be all equal as $M \neq N$. Assuming that $N > M$ (this leads to the best solution), then put $N = L + K + 1$. All the M inverters in the $I-$chain have the same fanout, called f_0 ($\bar{f}_0 = f_0/\gamma$). In the $J-$chain, instead, L inverters have a founout f_1 and $K+1$ inverters have a founout f_0. As the $J-$chain as more inverters than the $I-$chain, f_1 must be smaller than f_0. Propagation delays expressed by Eq. 3.13 then become:

$$\begin{aligned} t_{ptotI} &= \eta t_0(1 + \bar{f}_{\omega,i=1} + \bar{f}_{\omega,j=1}) + \\ &+ (M-1)(1+\eta)t_0(1+\bar{f}_0) + \\ &+ t_0(1+\bar{f}_0) \\ t_{ptotJ} &= \eta t_0(1 + \bar{f}_{\omega,i=1} + \bar{f}_{\omega,j=1}) + \\ &+ L(1+\eta)t_0(1+\bar{f}_1) + \\ &+ K(1+\eta)t_0(1+\bar{f}_0) + \\ &+ t_0(1+\bar{f}_0) \end{aligned} \tag{3.25}$$

Imposing $t_{ptotI} = t_{ptotJ}$:

$$(M-1)(1+\bar{f}_0) = L(1+\bar{f}_1) + K(1+\bar{f}_0)$$

$$(M-1-K)(1+\bar{f}_0) = L(1+\bar{f}_1)$$

and using $K = N - 1 - L$:

$$[L-(N-M)](1+\bar{f}_0) = L(1+\bar{f}_1) \tag{3.26}$$

As $N > M$, $(N-M) > 0$ and $L > L-(N-M)$. So the previous equation is true only if $\bar{f}_1 < \bar{f}_0$ and $L > (N-M)$ (both sides are positive). To achieve the minimum C_{totJ}, the first L inverters of the chain should be the ones with a $\bar{f}_1$ fanout. This reduces dynamic power consumption.
With these assumptions Eq. 3.19 and 3.20 become Eq. 3.27 and 3.28. As C_L is a constant, what is relevant in Eq. 3.27 is:

$$\frac{C_{totI} - C_L}{(1+\gamma)C_L} = \frac{1}{f_0^M} \frac{f_0^M - 1}{f_0 - 1} = g_I(f_0, M) \tag{3.29}$$

As $g_I(f_0, M)$ decreases with f_0 and increases with M, in order to minimize g_I, the highest value of f_0 that allowed meeting the specifications in Eq. 3.15 ($f_0 = 3.3$) and the smallest admissible value for M were chosen ($M = 2$, $M = 0$ and $N = 1$ with $M > N$ do not work).

$$C_{totI} = C_{g,i=1}\left\{(1+\gamma)\left[1+\sum_{i=1}^{M-1} f_0^i\right]+f_0^M\right\} = C_{g,i=1}\left\{(1+\gamma)\left[1+\frac{f_0^M-1}{f_0-1}-1\right]+f_0^M\right\} =$$
$$= \frac{C_L}{f_0^M}\left\{(1+\gamma)\frac{f_0^M-1}{f_0-1}+f_0^M\right\} = C_L + (1+\gamma)\frac{C_L}{f_0^M}\frac{f_0^M-1}{f_0-1} \tag{3.27}$$

$$C_{totJ} = C_{g,j=1}\left\{(1+\gamma)\left[1+\sum_{i=1}^{L} f_1^i + f_1^L\sum_{j=1}^{(N-L)-1} f_0^j\right]+f_1^L f_0^{N-L}\right\} =$$
$$= \frac{C_L}{f_1^L f_0^{N-L}}\left\{(1+\gamma)\left[\frac{f_1^{L+1}-1}{f_1-1}+f_1^L\frac{f_0^{N-L}-f_0}{f_0-1}\right]+f_1^L f_0^{N-L}\right\} = \tag{3.28}$$
$$= C_L + (1+\gamma)\frac{C_L}{f_1^L f_0^{N-L}}\left[\frac{f_1^{L+1}-1}{f_1-1}+f_1^L\frac{f_0^{N-L}-f_0}{f_0-1}\right]$$

In the same way, what is relevant in Eq. 3.28 is:

$$\frac{C_{totJ}-C_L}{(1+\gamma)C_L} = \frac{C_L}{f_1^L f_0^{N-L}}\left[\frac{f_1^{L+1}-1}{f_1-1}+\right.$$
$$\left.+f_1^L\frac{f_0^{N-L}-f_0}{f_0-1}\right] = g_J(f_1,L,N) \tag{3.30}$$

as now f_0 is known. Then, from Eq. 3.26:

$$L = \frac{(N-M)(1+\bar{f}_0)}{\bar{f}_0-\bar{f}_1} = L(f_1,N)$$

When this expression is used in Eq. 3.30, it gives:

$$g_J(f_1,L,N) = g_J(f_1,N)$$

Now g_J can be minimized obtain $N=3$, $L=2$, and $f_1=0.95$ as best choices.

3.2.2 Level shifter

Level shifter schematic is represented in Fig. 3.15. Last inverter's dimensions are chosen as small as possible to reduce dynamic power. The same applies to the first inverter. The most critical part of this circuit is the DCVSL that performs the supply voltage shift. Focusing on the simpler circuit in Fig. 3.16, call C_3 (represented in the Fig.), C_2 and C_1 the capacitances between nodes $1,2,3$ and ground respectively. C_0 is not relevant as V_0 is driven by an ideal voltage source.

When V_0 undergoes a $0\to1$ transition, M_1 turns on and discharges C_2; V_2 starts decreasing and when it reaches $V_{DD}+V_{tp}$ M_3 turns on and charges C_3; so even V_3 undergoes a $0\to1$ transition.

When V_0 undergoes a $1\to0$ transition, V_1 has a $0\to1$; when V_2 reaches V_{tn} M_2 turns on and discharges C_3; so V_3 undergoes a $1\to0$ transition.

There is no need to perfectly match rise and fall times of V_3, as each of the following inverters would reduce the difference between the two. It is more important to match the propagation delay from V_0 to V_3.

Note that, during a $1\to0$ transition of V_0, M_1 is on until $V_0 > V_{tn}$. When M_1 turns off, it is possible that V_3 is still greater than $V_{DD}+V_{tp}$ and therefore that M_3 is still off. At this point V_2 is held only by the parasitic capacitance C_2. As V_2 is low, M_4 is on and a short circuit between V_{DD} and ground is present. When V_3 finally drops below $V_{DD}+V_{tp}$, M_3

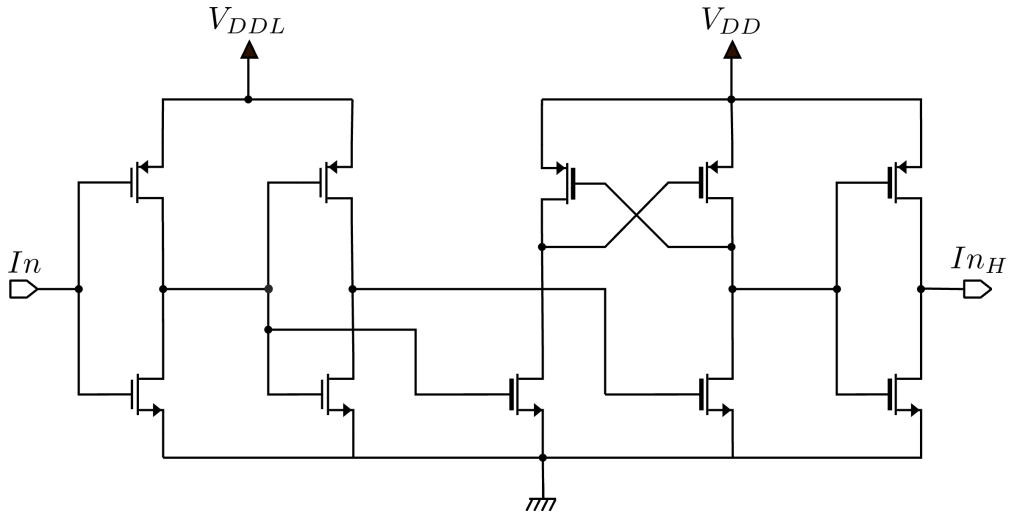

Figure 3.15: Level shifter schematic

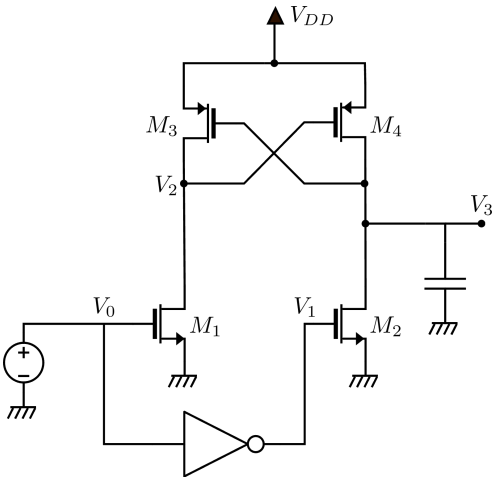

Figure 3.16: DCVSL in the level shifter

turns on but then it needs some time to charge C_2, increase V_2 and turn off M_4. It is vital that this V_2 transient ends in a bit period. In addition, the less it lasts the lower the direct path power lost when both M_2 and M_4 are on.
A direct path through M_1 and M_3 is also present during a $0 \rightarrow 1$ transition.
Transistors' dimensions were chosen with the aid of the simulator.

3.2.3 Simulation results

Level shifter's V_2 and V_3 are shown in Fig. 3.17. V_2 rise time does not appear as a problem. The difference between rise and fall times of V_3 is reduced by the inverters in the chains.
Predriver's outputs, V_{in} (sky blue) and V_{ip} (purple), are shown in Fig. 3.18. Design constraints expressed by Eq. 3.14 and 3.15 are almost perfectly met. Its power consumption is 2.3 mW, with 1 mW needed only for the core's input capacitance.

3.3 Conclusion

Transmitter's differential output is shown in Fig. 3.19 together with its corresponding eye diagram. Good measurements were extracted from the diagram:

Level 0 mean	−384.4 mV
Level 1 mean	388.9 mV
Eye height	586.2 mV
Eye width	372.4 ps
Rise time	78.49 ps
Fall time	78.15 ps

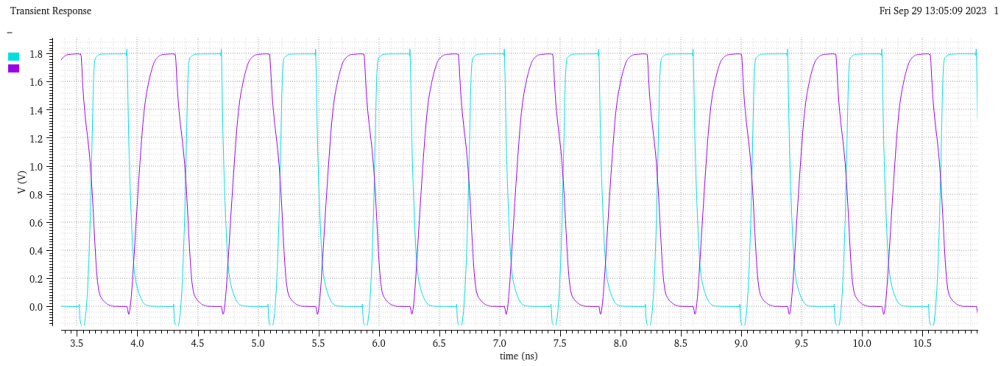

Figure 3.17: Level shifter's V_2 (sky blue) and V_3 (purple) at 2.56 Gbps

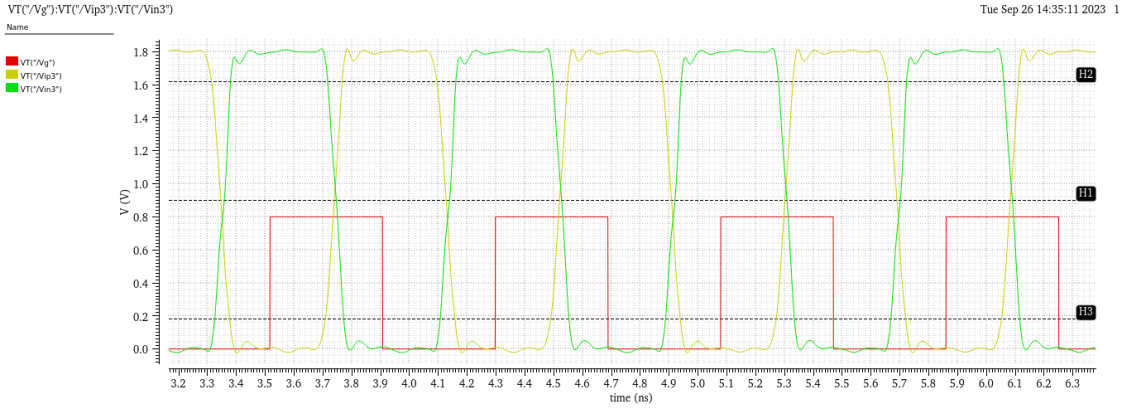

Figure 3.18: Predriver's outputs, V_{in} (green) and V_{ip} (yellow) at 2.56 Gbps

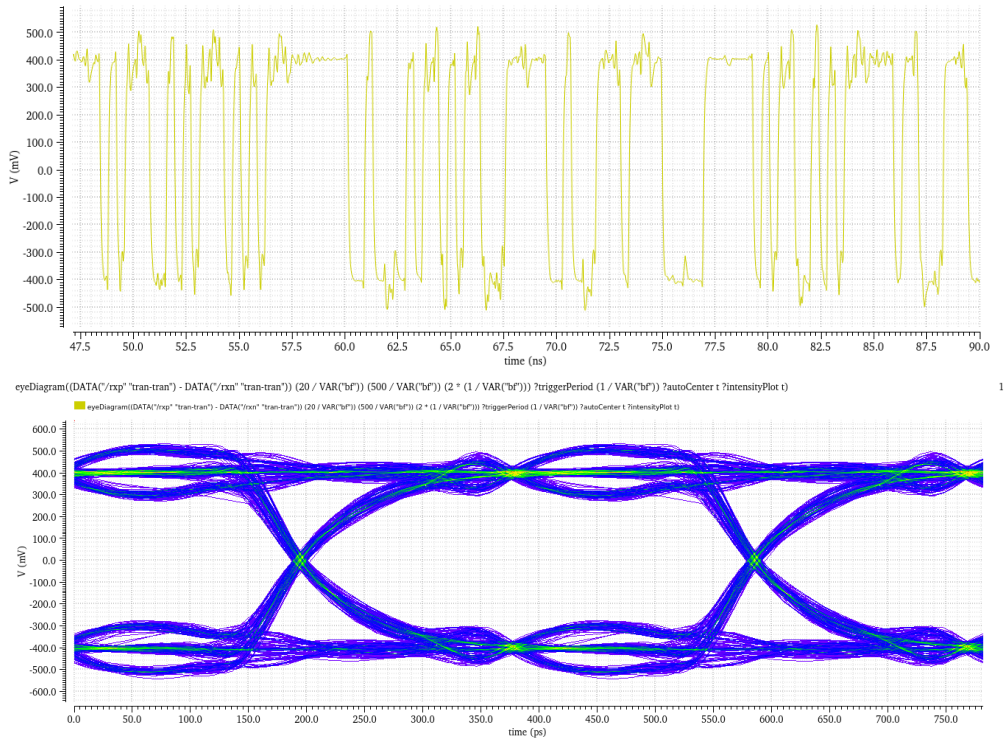

Figure 3.19: Transmitter's differential output at 2.56 Gbps with $I_{pt} = 4$ mA and its corresponding eye diagram

Chapter 4

Receiver

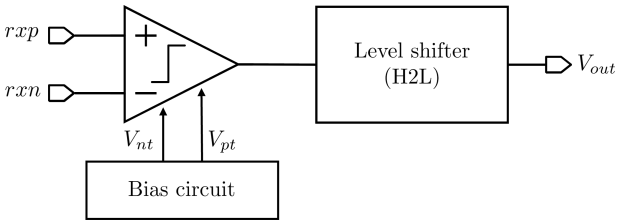

Figure 4.1: Receiver block diagram.

The receiver (Fig. 4.1) is composed by a comparator, its bias circuit and a level shifter, which switches from the higher supply voltage V_{DD} back to the lower one V_{DDL}.

4.1 Comparator

The comparator (Fig. 4.3) is composed of a differential pair and a decision circuit. The actual comparator design also has an $n-$input comparator, to widen the input's common mode range of variability.
Initially, the comparator was designed with hysteresis. However, it was immediately clear that, in order to obtain a switching threshold

$$V_H = \frac{I_t}{g_m}\frac{r-1}{r+1}, \quad r = \frac{\beta_C}{\beta_L} \tag{4.1}$$

lower than 50 mV (lowest possible receiver's input), the tail current I_t had to be too small to charge all the parasitic capacitances of the decision circuit. Therefore hysteresis was removed ($\beta_C = \beta_L$).
Now the comparator works well with a load capacitance of 30 fF, which is bigger then the level shifter's input capacitance.

4.2 Level shifter

The level shifter (Fig. 4.4) is a chain of 4 inverters. The first three are thick oxide inverters, while the last one is a thin oxide inverter. The first two work at a supply voltage of $V_{DD} = 1.8$ V, last two work at $V_{DDL} = 0.8$ V.
During an $H \to L$ transition of the third inverter's in-

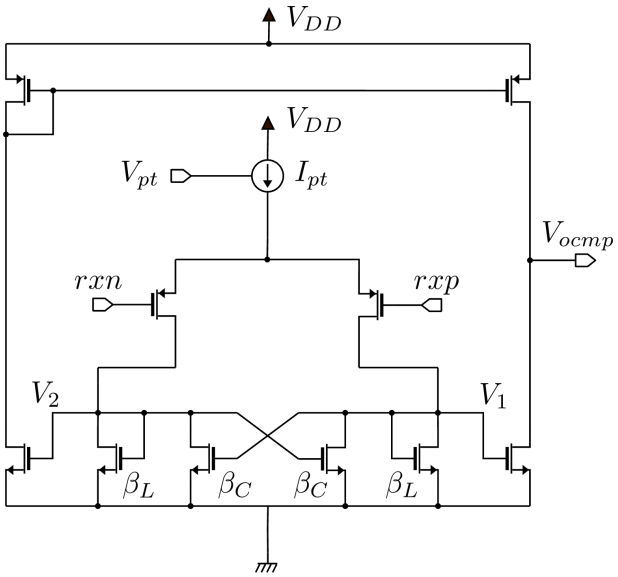

Figure 4.2: Schematic of the $p-$input comparator

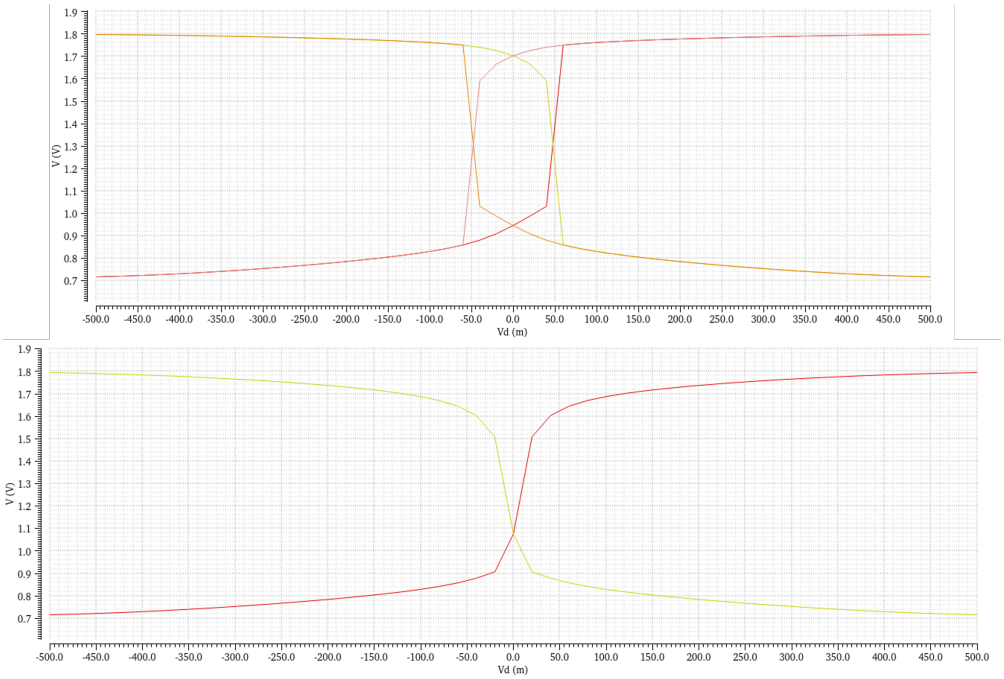

Figure 4.3: Outputs of the decision circuit of the $n-$input comparator as $V_{id} = rxp - rxn$ varies, with and without hysteresis

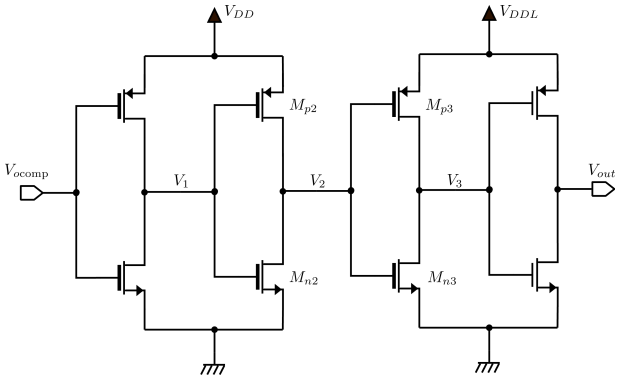

Figure 4.4: Level shifter schematic

put V_2, transistor M_{p3} will not start conducting until $V_2 < V_{DDL} + V_{tp}$. It takes V_{G3} some time to decrease from V_{DD} to $V_{DDL} + V_{tp}$. To reduce this delay and expedite the transition, M_{p3} has $BGP = -2.5$ V. In this way $V_{tp3} > 0$ and so $V_{DDL} + V_{tp3}$ is reached far earlier. In addition to that, M_{n2} is made larger than how it should be, to further speed up the transition. On the contrary, a $L \rightarrow H$ transition does not represent a problem, as M_{n3} will start conduction as soon as V_2 reaches V_{tn}.

4.3 Conclusion

Performance of the receiver was tested with all possible differential input values, at 2.56 Gbps. Resulting receiver's output with $V_{id} = 50$ mV and a 50 fF load capacitance is represented in Fig. 4.5.
Whole circuit's performance was also tested with a pseudo-random bit sequence as transmitter's input (2.56 Gbps). Circuit's output and the corresponding eye diagram are shown in Fig. 4.6.

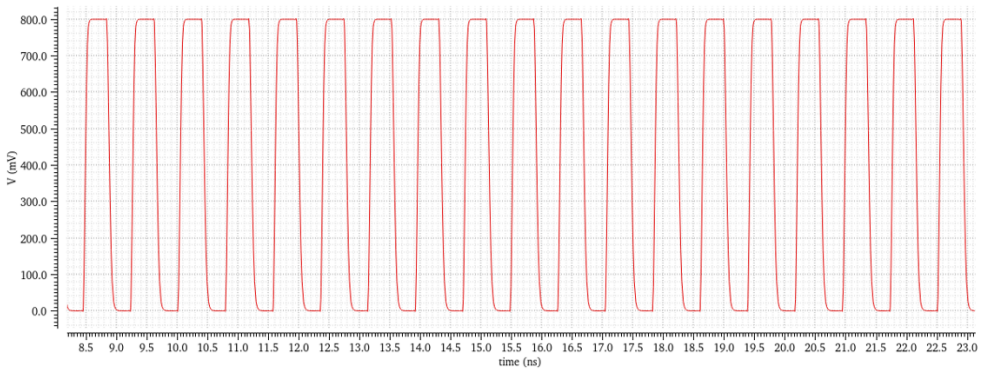

Figure 4.5: Output of the receiver at 2.56 Gbps with $V_{id} = 50$ mV and $C_L = 50$ fF

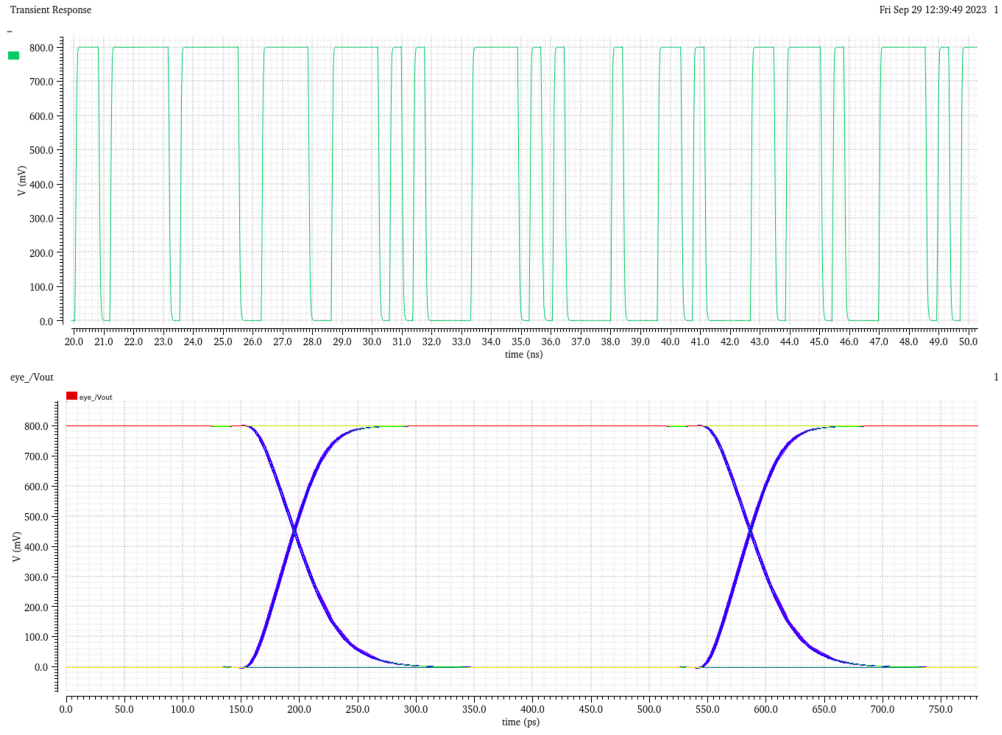

Figure 4.6: Output of the whole circuit, with a pseudo-random bit sequence as input (2.56 Gbps) and $C_L = 50$ fF, and its eye diagram

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