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Design of the cooling system of the Mu2e electromagnetic calorimeter at Fermi National Accelerator Laboratory

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Introduzione

Il mio lavoro di Tesi è consistito nel progetto del sistema di raffreddamento dell'elettronica del calorimetro elettromagnetico dell'esperimento Mu2e attualmente in costruzione presso il Fermi National Accelerator Laboratory. L'obiettivo dell'esperimento è la ricerca della conversione coerente di un muone in elettrone senza la produzione di neutrini nel campo di un nucleo di alluminio. L'osservazione di questo processo fisico dimostrerebbe l'evidenza di fisica oltre il Modello Standard. Si prevede che l'esperimento possa iniziare la presa dati nell'anno 2020. In vari casi, per la *beamline*, i magneti ed i rivelatori, si stanno prendendo in considerazione più soluzioni tecniche, con più opzioni disponibili. Questo accade anche per il calorimetro elettromagnetico, in particolare per la scelta del cristallo e del fotosensore, che ha avuto conseguenze anche sul mio lavoro. Il calorimetro è stato progettato e verrà costruito da una collaborazione di diversi enti, quali l'Istituto Nazionale di Fisica Nucleare, il California Institute of Technology e il Fermilab. Si tratta di un'ampia collaborazione che coinvolge molti gruppi di ingegneri e fisici. Il mio primo obiettivo è stato di raccogliere tutte le informazioni tecniche necessarie per capire i vincoli esterni, fissati dalle caratteristiche dell'area sperimentale, dalle caratteristiche tecniche dell'elettronica del calorimetro che determina le prestazioni richieste al sistema di refrigerazione, e da quelle fissate dal gruppo che si occupa dell'integrazione del calorimetro nell'esperimento. Per fare ciò sono stato per otto mesi, da Marzo 2015 ad Ottobre 2015, in continuo contatto con i ricercatori e i tecnologi dell'INFN di Pisa, dell'INFN di Frascati e di Fermilab. Inoltre ho vinto una borsa di studio dell'Universities Research Association per condurre il mio lavoro di Tesi a Fermilab da Agosto a Settembre 2015.

Nel Capitolo 1 sono spiegati l'obiettivo e la tecnica sperimentale di Mu2e. È inoltre fornita una descrizione del complesso dell'acceleratore del Fermilab e dell'apparato sperimentale di Mu2e. È data infine una breve descrizione del tracciatore di Mu2e, del calorimetro, dello schermo dei raggi cosmici e del sistema di acquisizione dati. Il Capitolo 2 mostra le specifiche tecniche del calorimetro elettromagnetico, entrando nel dettaglio del progetto meccanico ed elettronico, inclusi i fotosensori, l'elettronica di front-end e le schede custom che provvedono alla digitalizzazione dei segnali prodotti dai fotosensori.

Il Capitolo 3 descrive il progetto del raffreddamento dell'elettronica del calorimetro, che include il raffreddamento dei fotosensori e delle schede di *front-end*, fatto con un disco di alluminio che fornisce sia il supporto meccanico che il raffreddamento; e dei *waveform digitizer*, che è fatto estraendo il calore dissipato tramite i *crate*, che forniscono il supporto meccanico, con del fluido refrigerante. Successivamente è presentata una spiegazione più nel dettaglio del sistema di refrigerazione del *crate* e una relativa analisi termica.

Il Capitolo 4 fornisce un progetto schematico della distribuzione del fluido refrigerante attraverso l'intero calorimetro. Il progetto prende in considerazione i vincoli che derivano dal fatto che il tracciatore e il calorimetro condividono lo stesso sistema di refrigerazione.

Il Capitolo 5 descrive il processo di produzione e di assemblaggio del *crate* che contiene la *interface board* e il *waveform digitizer*, nonchè la produzione della serpentina.

Il Capitolo 6 fornisce una descrizione preliminare delle misure necessarie di degasaggio e termiche per testare i componenti scelti per il circuito di raffreddamento. L'obiettivo dei test termici è di verificare che la massima temperatura raggiunta da ogni componente elettronico non eccede il massimo valore riportato nelle specifiche tecniche.

Il Capitolo 7 riporta le conclusioni e i propositi per i futuri sviluppi del mio lavoro.

Nelle Appendici ci sono tutti i disegni tecnici dei componenti progettati (A) e i data-sheet dei componenti usati (B).

Introduction

My work has been the design of the cooling system of the electronics of the Mu2e electromagnetic calorimeter at Fermi National Accelerator Laboratory. The goal of the Mu2e experiment is to search for the neutrino-less coherent conversion of a muon to an electron in the field of an aluminum nucleus, a physics process which would be the evidence of the existence of physics beyond the Standard Model. The experiment is currently in construction and is expected to begin commissioning in the year 2020. Many technical solutions for the experimental apparatus, for the beamlines, magnets, and detectors, are still under study, with more than one option available in several cases. This is the case also of the electromagnetic calorimeter, which is being designed and is going to be constructed by a collaboration among the Italian Istituto Nazionale di Fisica Nucleare, the California Institute of Technology, and Fermilab. It is a wide collaboration with many groups of physicists and engineers involved. I have been in continuous contact with the INFN-Pisa, INFN-Frascati and the Fermilab groups during the 8 months, from March 2015 to October 2015, I have dedicated to my Thesis. I was also awarded a 2month scholarship of the Universities Research Association to visit Fermilab in August and September 2015.

In the Chapter 1 the Mu2e goal and the experimental technique are reviewed. A description of the Fermilab accelerator complex and of the Mu2e experimental apparatus is provided. A brief description of the Mu2e tracker, calorimeter, cosmic ray veto and data acquisition system is given.

Chapter 2 reviews the technical specifications of the electromagnetic calorimeter, with a more accurate description of the mechanical design and of the electronics, including photo-sensors, front-end electronics and custom boards which performs digitization of the signals produced by the photo-sensors.

Chapter 3 describes the project of the calorimeter electronics cooling system, which includes the cooling of the photo-sensors and front-end boards implemented via an aluminum plate which provides mechanical support and cooling, and the cooling of the waveform digitizer boards, which is made by extracting the dissipated power from the aluminum crates, which provide the mechanical support, with a cooling fluid. A detailed description of the crate cooling system and a thermal analysis are provided.

Chapter 4 provides a schematic design of the distribution of the cooling fluid throughout the entire calorimeter. This project takes into consideration the constraints deriving from the fact that the tracker and the calorimeter share the same cooling system.

Chapter 5 describes the manufactoring and assembly of the crate which contains the interface and waveform digitizer boards and the production of the coil.

Chapter 6 provides a preliminary description of the outgassing and thermal measurements required to test the components chosen for the cooling circuit. The goal of the thermal tests is to verify that the maximum temperature reached by each electronic component does not exceed the maximum values reported in the specifications.

Chapter 7 reports the conclusions and prospects for future developments of my work.

In the Appendix there are all the technical drawings of the designed components (A) and the data-sheets of the used components (B).

Chapter 1

The Mu2e goal and experimental technique

The Standard Model of particle physics provides an excellent interpretation of experimental data. The model has been tested in many ways and to high precision in the last decades and it has proven to provide an excellent description of physics phenomena at energies. The fundamental constituents of matter are quarks and leptons, which are arranged in three "families", or "generations", and completely differ in the phenomenology of their interactions. According to the experimental evidence, the muon decays to an electron and a muon neutrino and an electron anti-neutrino pair ($\mu^- \rightarrow e^- + \bar{\nu}_e + \nu_\mu$) with a branching fraction of approximately 100%. In some rare cases, in addition to these decay products, other particles with a net charge of zero are produced (e.g. a photon, or an electron-positron pair). Searches for Lepton Flavor Changing Neutral current effects, as the decay process $\mu \rightarrow e + \gamma$, have, so far, yielded null results. This is expected within the framework of the Standard Model which predict a probability $< 10^{-54}$ for this decay process (Fig. 1.1).



Figure 1.1: Feynman diagram for the charged lepton flavor violating muon decay $\mu \rightarrow e + \gamma$.

Although the Standard Model has been very well tested, it is probably and incomplete theory. Several extensions of the Model include Charged Lepton Flavor Violation (CLFV) processes which allow the neutrino-less muon decay



Figure 1.2: Feynman diagram of a muon conversion into an electron in a nucleus field, according to Standard Model extensions which include Charged Lepton Flavor Violation process.

to an electron, with rates within the reach of the next generation experiments. Mu2e has been designed and is now being constructed to search for the neutrino-less muon conversion to an electron in the field of an aluminum nucleus (Fig. 1.2). The experimental signature of this process is a single mono energetic electron with the energy of approximately the muon rest mass, 104.97 MeV. Simulations show the Mu2e sensitivity allows to observe this process if it has a probability above 10^{-17} . In case no event is observed the limit on the probability of this process can be set at 10^{-17} which is an improvement of four order of magnitude over current experiments.

1.1 The Fermilab accelerator complex

Fermilab is located about 50 km west of Chicago, Illinois. It is a US Department of Energy Laboratory and has been operated by the Universities Research Association (URA) since its founding, in 1967 [1]. The name "Fermilab" was given to the laboratory in 1974 in honor of Nobel Prize-winning italian physicist Enrico Fermi [2]. Fig. 1.3 shows an aerial view of the laboratory, which has played a major role in the field of high energy physics for the last forty years. Among its scientific achievements, we can mention the discovery of three of the four particles of the third generation of the Standard Model: the bottom quark (May- June 1977), the top quark (February 1995) and the tau neutrino (July 2000) [1].

1.1.1 The chain of accelerators

Fermilab accelerator complex is made of several stages schematically shown is Fig. 1.4. The first stage is provided by a **Cockcroft-Walton generator**, which turns hydrogen gas into H-ions by flowing it into a container lined with molybdenum electrodes: a matchbox-sized, oval-shaped cathode and a surrounding anode, separated by 1 mm and held in place by glass ceramic insulators. A magnetron is used to generate a plasma to form H^- ions near



Figure 1.3: Aerial view of Fermi National Accelerator Laboratory. The 3.2 km circumference Main Injector tunnel is visible in the foreground, the Tevatron tunnel is visible in the background. The High Rise is in the top left corner. The Tevatron has been the most "powerful" particle accelerator for many years before the turning on of the Large Hadron Collider (LHC) at CERN in Geneva.

the metal surface. A 750 keV electrostatic field is applied by the Cockcroft-Walton generator, and the ions are accelerated out of the container. The second stage is a **Linear Accelerator** (or Linac), which accelerates particles to 400 MeV, or about 70% of the speed of light. Right before entering the next accelerator, the H-ions pass through a carbon foil, which strips off the electrons thus producing a H^+ ions (i.e. protons) beam. The third stage is the **Booster ring**. The Booster ring is a 468 m circumference circular accelerator that uses magnets to bend beams of protons in a circular path. The protons coming from the Linac travel around the Booster about 20,000 times in 33 ms so that they repeatedly experience electric fields. With each revolution the protons pick up more energy, and leave the Booster with the energy of 8 GeV. The **Main Injector** is the next link in the accelerator chain. Completed in 1999, it has become Fermilab's "particle switchvard" with four functions: (1) accelerating protons from 8 GeV to 150 GeV; (2)delivering protons for antiproton production; (3) accelerating antiprotons, produced by the Antiproton Source, to 150 GeV; (4) injecting protons and antiprotons into the Tevatron. The **Tevatron** has been the most powerful particle accelerator in the world for many years, and ceased operations on September 30, 2011, while the operations of the Large Hadron Collider (LHC) at CERN was ramping up. The Tevatron has been decommissioned, but the reminder of the complex of accelerator is now being used to support the ongoing Fermilab research program, which includes Mu2e, g-2 and neutrino experiments.



Figure 1.4: Schematic drawing of the Fermilab accelerator components used for the Tevatron collider operations which were ended on September 30, 2011. [3].

1.2 The Mu2e experimental apparatus

The Mu2e apparatus has been extensively documented in the Conceptual Design Report and Technical Design Report [5],[4]. The layout of the muon beam line and the detector system are based on the MECO design and are sketched in Fig. 1.5. The major feature of the muon beam line is the Superconducting Solenoid Magnet System. The inner bore of the solenoids is evacuated to 10^{-4} Torr in order to limit backgrounds from muons that interact with gas particles. The Solenoid Magnet System can be schematically divided in 3 major sub-systems:

• Production Solenoid (PS)

- Transport Solenoid (TS)
- Detector Solenoid (DS)



Figure 1.5: The Mu2e apparatus. The proton beam enters from the right at the junction between the Production Solenoid and the Transport Solenoid and strikes the production target. The cosmic ray veto system, which surrounds the Detector Solenoid, and the muon stopping monitor are not shown in this scheme.

1.2.1 Production Solenoid

The primary 8 GeV proton beam enters the Production Solenoid and strikes the production target located in an axial magnetic field, which decreases from 5 T to 2.5 T along the beam line. The target is a radiatively cooled tungsten target, 16 cm long and 12.6 mm in diameter. A massive concrete shield surrounding the Production Solenoid absorbs secondaries from the production target. Back-scattered muons are captured by the Production Solenoid and transported through the S-bend Transport Solenoid to the stopping target.

1.2.2 Transport Solenoid

The function of the Transport Solenoid is to transport 10^{11} muons per second to be stopped in the secondary target located in the Detector Solenoid. This beam line includes the collimators and anti-proton stopping window in the Transport Solenoid, proton and neutron absorbers, beam stop, and vacuum system. The Transport Solenoid filters the particle flux producing a momentum (< 0.08 GeV/c) and charge-selected muon beam, with a good reduction of the contamination from e^{\pm} , μ^+ , π^{\pm} , p and \bar{p} during the detector live-time.

1.2.3 Detector Solenoid

The upstream section of the Detector Solenoid contains the muon stopping target and has a graded magnetic field, which nearly doubles the acceptance for conversion electrons and rejects certain backgrounds. The downstream section of the Detector Solenoid is occupied by the tracker and the electromagnetic calorimeter. This region has a relatively uniform magnetic field. Conversion electrons, produced in the stopping target are captured by the magnetic field within the Detector Solenoid. Then, they are transported through the tracker, which provides a precision measurement of the momentum. The conversion electrons hit the electromagnetic calorimeter, which performs an independent measurement of the electron energy and time of impact. The baseline aluminum target has a mass of 159 g in 17×0.02 cm thick disks (Fig. 1.6). The disks are positioned parallel and at 50 mm each other. They are centered on the Solenoid Magnet axis with each face perpendicular to it. Their radii range from 8.30 cm at the upstream end to 6.53 cm at the downstream end. The target support wires are made as thin as



Figure 1.6: The Mu2e stopping target. It is made of 17 aluminum disks, 0.2 mm thick, spaced 5.0 cm apart along the Detector Solenoid axis. The disks radius decreases from 8.3 cm upstream to 6.53 cm downstream.

possible to minimize the number of stopped muons in them. If muons stop in the wires at a significant distance from the solenoid axis, then low energy electrons produced in the muon decay could fall into the acceptance of the tracker and cause an undesired low energy background.

1.2.4 Mu2e Detectors

The Mu2e tracker and electromagnetic calorimeter are placed inside the volume of the Detector Solenoid. For the tracker the Mu2e collaboration has decided to use a design similar to the one developed by the MECO collaboration (Fig. 1.7). The tracker resides in a uniform 1 T magnetic field and is kept in a 10^{-4} Torr vacuum to reduce the interaction of particles with gas to a negligible level. This detector measures the parameters of the helical trajectories of the electrons with high efficiency and high resolution. Since multiple scattering in the tracker increases the uncertainty on the helix parameter measurements, the mechanical structure of the detector is made extremely light. A further source of uncertainty is due to pattern recognition errors. This effect may produce high energy tails in the resolution function. The tracker is made of straw drift tubes. It is called T-tracker because the straws are transverse to the axis of the Detector Solenoid. The basic detector element is made of a 20 μ m sense wire inside a straw tube filled with gas. The straws are 5 mm diameter tubes made of 15 μ m thick metallized Mylar. The tracker has $\sim 20,000$ straws arranged into 18 measurement stations across a \sim 3 m length. Planes consist of two layers of straws, to improve efficiency and help overcome the classic "left-right" ambiguity. A 1 mm gap between straws allows for manufacturing tolerance and expansion due to gas pressure. A ring at large radius, outside the active detector region, supports the straws. Each straw has preamps and time to digital converter on both sides, for the measurement of the signal arrival time, and uses also analog to digital converters for the measurement of the total integrated charge which provides useful information for particle identification. The tracker is designed so that only electrons with energy greater than about 53 MeV can be observed. They represent a fraction of about 3% of the total flux of electrons from muon decays-in-orbit. Since momentum resolution is crucial to suppress several critical backgrounds, the tracker is required to have a resolution better than 180 keV.

The Mu2e calorimeter provides additional energy, position, and timing information on tracks that have been reconstructed by the tracker. The calorimeter and the tracker use different technologies and physical processes to perform their measurements, so the sources of error from the two systems are not correlated. This helps to reduce backgrounds and gives a cross check to verify the quality of signal events. The calorimeter operates in vacuum and in a magnetic field of 1 Tesla. It must handle a large flux of particles, mostly low energy background of protons, neutrons and gamma rays produced by muon captures in the stopping target. It must deal with a large flux of electrons from muons decaying in the atomic orbit in the aluminum stopping



Figure 1.7: tracker layout. The top panel displays the 18 station tracking system. The bottom panel shows a cross-sectional view of the tracker. Only electrons with energies greater than 53 MeV are reconstructed. Electrons with lower energy spiral in the uninstrumented central region.

target and other particles during beam injection. A more detailed description of the calorimeter is reported in Chapter 2.

1.2.5 Cosmic ray shield

Cosmic ray muons can interact with the detector material and produce backgrounds to the search of the muon conversion signal. These backgrounds can be reduced by passive and active shields. The cosmic ray shield surrounds the entire volume occupied by the Detector Solenoid. The idea is to place it about 20' underground. The cosmic ray background rate will be monitored between beam spills and when the beam is off. This allows a direct measurement of the background level. The background rate will be measured as soon as the detector and detector solenoid are in place.

1.2.6 Trigger and DAQ

The Mu2e detectors include the Trigger and Data Acquisition (TDAQ) subsystems, which provide hardware and software for recording the digitized data from the detectors. These data are delivered to online and offline processors for analysis. The TDAQ also synchronizes and controls the detector operation. In a streaming mode, the off-detector bandwidth requirement for the DAQ is estimated to be approximately 100 GBytes/sec. The TDAQ has the function to combine information from all detector data sources and apply filters (triggers) to reduce this rate by a factor of several thousand before data can be delivered to offline storage.



Figure 1.8: Map view of the Mu2e experimental area.

Chapter 2

The Mu2e electromagnetic calorimeter

The Mu2e detectors have been designed to reject backgrounds to a level consistent with a single event sensitivity for $\mu \rightarrow e$ conversion of the order of 10^{-17} . The electromagnetic calorimeter is a vital link in the chain of background defenses. A background of particular concern is due to false tracks arising from pattern recognition errors that result from the high rates of hits expected in the tracker. The accidental hits can combine with, or obscure, hits from lower energy particles, and erroneously create a trajectory consistent with a higher energy conversion electron which may mimic the muon conversion signal. Thus the primary function of the Mu2e calorimeter is to provide a redundant set of measurements that complement the information from the tracker and provide sufficient information to reject backgrounds due to track reconstruction errors.

2.1 Conceptual detector design

Electrons produced in the decay of the muons stopped in the target follow helical trajectories in the solenoidal magnetic field and hit the front faces of the calorimeter crystals. The maximum energy of the electrons is in the 100 MeV range. In this energy regime a total absorption calorimeter employing a homogeneous continuous medium is required to meet the Mu2e resolution requirements. The sensitive material could be either a liquid, such as xenon, or a scintillating crystal. The Mu2e collaboration has chosen the scintillating crystal technology. Several types of crystals have been considered including: barium fluoride (BaF₂) and cesium iodide (CsI). The baseline design uses an array of BaF₂ crystals arranged in two annular disks. An alternative design uses the less expensive CsI crystals. At the moment of writing this Thesis the technological choice has not been made yet and is expected for December 2015. Fig. 2.1 shows a schematic view of the detector. Photodetectors, electronics and services are mounted on the rear face of the disks and are not visible in Fig. 2.1. Each crystal is read out by two large-area APDs; solid-state photo-detectors are required because the calorimeter operates in a 1 T magnetic field. Front-end electronics is mounted on the rear side of each disk, while voltage distribution, slow controls and electronic boards for data acquisition are mounted in 24 crates placed externally to the disks. A laser flasher system provides light to each crystal for relative calibration and monitoring purposes. A circulating liquid radioactive source system provides absolute calibration and allows to determinate the absolute energy scale. The crystals are supported by an aluminum structure which can be moved along the beam line on horizontal rails. The detector components are described in more detail in the following Sections.

2.2 Technical specifications

The primary function of the calorimeter is to provide energy, position and timing information to confirm that particle trajectories reconstructed by the tracker are well measured and are not just the result of a spurious combination of hits. Moreover, the calorimeter provides information to the trigger for online selection of data. This leads to the following requirements [5]:

- An energy resolution of 5% at 100 MeV to confirm the electron momentum measurement performed by tracker;
- a timing resolution better than 0.5 ns to ensure that energy deposits in the calorimeter are in time with events reconstructed in the tracker;
- a position resolution better than 1 cm to allow a comparison of the position of the energy deposit to the extrapolated trajectory of the reconstructed track;
- the calorimeter should provide additional information useful for particle identification that can be combined with the information from the tracker to improve the muon/electron separation;
- the calorimeter should provide a trigger, either in hardware, or in software, or in firmware, that could be used to identify events with significant energy deposits;



Figure 2.1: CAD model of the Mu2e calorimeter. The two annular disks of crystals coupled to the readout electronic are shown in violet; The 24 custom crates which host the boards for voltage distribution, slow controls and photo-sensor signals digitization are shown in gray; the cryostat walls, which surround the detector are shown in yellow.

• the calorimeter must operate in the hostile, high-rate Mu2e environment and must maintain its functionality for radiation exposures up to 20 Gy/crystal/year and for a neutron flux equivalent to $10^{11} n_{1MeVeq}/\text{cm}^2$.

2.3 Mechanical design

The two calorimeter disks are placed inside the detector solenoid (Fig. 2.1). Each disk has an inner radius of 351 mm, an outer radius of 660 mm, and is made of of 910 trapezoidal crystals. The crystals are 200 mm long with a square base and a side length of 30.7 mm. Each crystal is wrapped with 8 layers of 25 μ m thick PTFE (Teflon) reflective film to maximize light transport within the crystal and minimize cross-talk among crystals [6].

Each disk is supported by two coaxial cylinders. The inner cylinder is made of carbon fiber in order to minimize the amount of the passive material in the region where spiraling electrons are concentrated. The outer cylinder can be as robust as required to support the load of the crystals and is made of aluminum. Each disk has two cover plates. The plate facing the beam is made of low radiation length material to minimize the electron energy deposit in order to preserve the electron energy measurement. It has been designed to allow also the calibration source. The back plate supports the photosensors, the front-end electronics and cooling pipes and is made of aluminum. It has been designed to allow access to the electronic and crystals.

The mechanical properties of the crystals are critical for this type of configuration. A Finite Element Model, using the crystal properties as input, has been used to optimize this design. The boundary conditions of this layout have been fixed and the structural analysis has been used to verify the displacements and deformations of the components.

The front-end electronics boards are located at the back of each disk. The electronic boards necessary to provide the power to the photo-sensor and to digitize the photo-sensor signals are distributed in 12 crates per disk. Each crate houses 10 sets of boards.

In order to gain as much room as possible between the disks, when servicing of the crystals or the front-end electronics is required, the crates are placed at the outermost region of each disk. One crucial function is to provide heat dissipation for the electronic boards. This is a critical function since the calorimeter operates in vacuum and electronic power is dissipated primarily through thermal conduction. To this purpose the front-end electronics boards are placed in thermal contact with the supporting back plate where a cooling pipe is routed. The calorimeter cooling system will be connected to the same cooling circuit used by the tracking system.

2.4 Calorimeter electronics

The Mu2e calorimeter is a very complex detector and we can tentatively divide the entire electronics equipment in three main subsystems:

- photo-sensors and front-end boards;
- interface boards;
- waveform digitizer boards.

The photo-sensors and the front-end boards are placed behind the crystals and are integrated with the main mechanical structure which provides also heat dissipation. The other boards require a dedicated support structure and are placed in crates placed around the disks (Fig. 2.2).



Figure 2.2: CAD model of one disk of the Mu2e calorimeter.

2.4.1 Photo-sensors and front-end electronics

The interaction between the electron and the crystal generates photons which continue their path through the crystal towards the photo-sensors. Every crystal has on its back side the photo-sensors which convert light into electrical signals. There are 2 photo-sensors per crystal, electrically connected to one front-end board. The reason for doubling the photo-sensors is to provide more robust measurements and to not loose data if one photo-sensor fails during data taking. The total resulting number of photo-sensors is 1820 per disk.

The front-end electronics for the calorimeter readout consists of two discrete and independent chips (Amp-HV) placed on one unique front-end board



Figure 2.3: Crystal, photo-sensor and front-end board CAD model.

electrically connected to the back of the photo-sensor pins (Fig. 2.3 and Fig. 2.4). The two chips provide both the amplification stage and a local linear regulation for the photo-sensor bias voltage. Groups of 16 Amp-HV chips are controlled by one dedicated ARM controller that distributes the low voltage and the high voltage reference values, while setting and reading back the locally regulated voltages. The ARM controller is placed on the Interface board. The Amp-HV is a multi-layer double-sided discrete component board that carries out the two tasks of amplifying the signal and providing a locally regulated bias voltage, thus significantly reducing the noise loop-area. The two functions are independently executed in a single chip layer, named the Amp and HV sides, respectively. The development of the Amp-HV board has



Figure 2.4: Front and rear view of one Amp-HV prototype.

been done by the Laboratori Nazionali di Frascati (LNF) Electrical Design

Department. The required characteristics of the preamplifier are:

- high amplification with low noise;
- fast signal rise and fall times for good time resolution and pileup rejection;
- low detection threshold at the MeV level;
- functional in a rate environment of 200 kHz/channel;
- low power consumption.

2.4.2 Interface board

The interface board function provides the primary high voltage to the photosensors and a 16-bit linear regulation of the applied voltage. The board is equipped with a commercial high-voltage regulator, one ARM controller which drives a set of ADC and DAC placed on the front-end boards and used to adjust the applied voltage to the photo-sensors in the range between 250 V and 500 V. The accuracy of the voltage regulation is 16 bit and communication between the interface board and the front-end electronics board is performed with the I2C protocol. The ARM controller also receives data from temperature measurement devices placed on the front-end boards. The interface board is equipped with an ethernet interface for external communication. The total dissipated power from the board is 2 watt. A prototype of the board is shown in Fig. 2.5.

2.4.3 Waveform Digitizer

The fast analog signals generated by the photo-sensors and amplified by the front-end electronics are digitized and transmitted to the data acquisition by the Waveform Digitizer boards. Since the signals are fast, a fast digitization with good resolution is necessary. A 12-bit sampling at 250 MHz is required. The board digitizes analog data, serializes it and sends it upstream to the data acquisition system using fiber optic transceivers. The board performs also some digital signal processing operations, suppressing data below threshold as well as providing the mean charge and time for each channel by means of running averages. The fundamental components used on the board are analog to digital converters, which perform the digitization of the analog signals received from the front-end electronics, DC-DC converters, to generate the voltages required to power the board components from the voltage



Figure 2.5: Front and rear view of one Amp-HV prototype.

received from the external power supplies, and one FPGA, which is necessary to process and transmit the digitized data to the external data acquisition stream through optical links. The design of the Waveform Digitizer prototype is now being finalized. More details relative to the board and relevant to the thermal analysis are given in Chapter 3.

Chapter 3

Design of the calorimeter electronics cooling system

The design of the calorimeter cooling system has been an iterative process which has required a continuous interaction with several research groups, in Italy and US, responsible of the design of the many electronic components used on the detector. This has been rather complicated also because some projects exist only at a conceptual level. Moreover, space and resources necessary for the calorimeter cooling and other services inside the cryostat have to be shared with the tracker. A significant part of my work has been interacting with the research groups, physicists and engineers, involved in the tracker and calorimeter design, and with the group responsible for the detectors integration, to develop a commonly acceptable solution.

The entire electronic apparatus of the calorimeter can be divided in two main subsystems, which can be ideally separated for the different functions and locations. The first subsystem is placed on the back side of the crystal disks. It contains the photo-sensors and the front-end electronics. The design of its cooling system is still preliminary and is briefly described in Section 3.7. The second subsystem is located on the radial external side of the calorimeter. It contains the waveform digitizers and the interface boards. The position of the two systems is clearly visible in Fig. 2.1. I have been mostly involved in the design of the cooling of the waveform digitizer and interface boards. In this case most technical choices relative to the design of the boards have already been finalized and it has been possible to make a detailed project. As far as the photo-sensors and front-end electronics, some technical choices have not been taken yet, mostly due to the uncertainty on the use of BaF_2 or CsI crystals which require different photo-sensors. This does not allow to make a detailed project yet. One student from the University Guglielmo Marconi in Rome is currently working on this topic for his Master Thesis in

Mechanical Engineering. He is expected to graduate in the year 2016.

3.1 Design constraints

The goal of my project has been developing a solution acceptable both to the group responsible for the integration of the tracker and for the group responsible of the integration of the calorimeter. This included making sure that all the services would fit in the limited space available inside the cryostat. Interacting with the integration group has been necessary and useful to the progress and the development of the project. The most important constraints have been relative to available spaces (Fig. 3.1) and the operating conditions of the coolant fluid. The refrigerating system is included in the cryostat and has to leave sufficient space for the other services, including cables and vacuum pumping. These constraints will be discussed in more detail in the next Chapters. The primary function of the cooling system is to keep the temperature of all the electronic components below the critical value which may reduce the reliability expected life and even cause irreversible damage. All the electronics components are placed inside the cryostat in vacuum at 10^{-4} torr, and at the average constant temperature of 25°C. In our case, the main mechanism to remove the electronic heating power is the conduction and through the coolant fluid. This is due to the fact that irradiation is a negligible effect respect to conduction, given the relatively low temperatures of the electronic components.

3.2 Waveform Digitizer and Interface boards Layout

In collaboration with the INFN electronic engineers I developed a solution for the cooling of the Waveform Digitizer and the Interface board.

3.2.1 Waveform Digitizer board

The components of the Waveform Digitizer with maximum power dissipation are:

- 1 Field Programmable Gate Array (FPGA);
- 2 DC-DC converters;
- 8 Analog to Digital Converter (ADC).



Figure 3.1: Schematic view of the calorimeter dimensions and of the services, tracker and calorimeter cables and cooling pipes.

We have verified that the resistors and capacitors dissipation is negligible.

We have chosen the FPGA FC1152 of *Microsemi* (B.1 - Fig. 3.2a). It processes all the data received from the photo-sensors and is the most complex component of the board. According to the data-sheet, the maximum junction temperature should be below 100°C. Since the exact amount of dissipated power by the FPGA depends on the number of operations it performs per unit of time, and the firmware has not been finalized yet, we have taken a conservative upper limit of 5 W as power dissipation. This value will be verified once the firmware has been completed and implemented on the device.

We have chosen the DC-DC converter LTM8033 of *Linear Technology* (B.2 - Fig. 3.2b). The function of the DC-DC converter is to transform the voltage received from the external power supply to the values required by the components used on the board. We have chosen a non-standard DC-DC converter with no iron-magnetic nucleus. This has been a necessary choice, since the Waveform Digitizer is placed in a 1 Tesla magnetic field, which would immediately saturate the field inside the iron nucleus of a standard DC-DC converter. Due to the absence of the iron-magnetic nucleus, the component has a much lower efficiency than a standard device. This implies

a larger power dissipation compared to a device equipped with iron-magnetic nucleus. The estimate of the dissipated power is 3 W, according to the data-sheet. The critical junction temperature is 125°C.

We have chosen the AD9230 of Analog Device (B.3 - Fig. 3.2c). It converts analog signals received from the front-end boards into digital signals which are further processed by the FPGA and then transmitted to the DAQ system. Its power consumption is 470 mW per unit. Its critical junction temperature is 85°C.



Figure 3.2: The main components used on the Waveform Digitizer are FPGA, DC-DC converters and ADCs.

In similar projects, the components are frequently cooled using a copper thick layer inside or at the bottom of the printed circuit board. This copper layer is in thermal contact with the components placed on the upper face through thermal vias (Fig. 3.3). In some cases, components have also dedicated pins for heat dissipation which are soldered to this layer. At the sides of the board the thermal layer emerges and is placed in thermal contact with the board lockers. In our case, some components are incompatible with this technical solution. The FPGA and the DC-DCs are ball grid array (BGA) components. This does not allow to cool them down from the bottom. A further problem is that the ADCs have the thermal pin connected to the analog ground. To avoid noise problems, we decided not to connect this pin with the thermal ground layer. For these reasons we decided to use an external plate placed in contact with all the electrical components which require cooling from the top side of the board. The design of the external plate is described in detail in the Section 3.3.2.

The proposed layout of the Waveform Digitizer board is shown in Fig. 3.4a. The placement of the components has been made after performing a preliminary thermal simulation. Our first decision has been to have a symmetric board. The idea has been to build a symmetric crate and to cool boards from both sides. In order to make the best use of the cooling



Figure 3.3: Thermal vias. A cross view of thermal vias in a PCB for heat dissipation of the electrical components.

components from both sides, we have chosen a symmetric placement of the components on the board.

We have chosen to spread the components on the board to achieve a better heat distribution and to have a simple routing of the electronic connections on the internal layers of the printed circuit board. There are several electronic constraints to follow. The most important ones are spacing of the connectors, spacing of the blocking system and routing of the connection lines to the ADCs. For the first two constraints, a sufficient amount of space all around the board has been left. For the last one, all the connections among ADCs and the FPGA must have the same physical length, to guarantee the same propagation time of the signals along all the lines.

As far as the board size is concerned (Fig. 3.4b), we have chosen the 6U Standard Euroboard (160 mm x 230 mm). The size of the board grants enough space to place all the components and to route all the lines safely. Due to the limited space available in the cryostat, and to have a more efficient cooling, boards are rotated by 90°. While the Euroboards usually have the connections on the longer side, and the lockers on the shorter sides, in our case longer sides are used to lock the board in the proper position and to extract heat, while the shorter sides are used for electrical connections. The design has been conducted in close collaboration with the electronic engineers of INFN of Pisa.

3.2.2 Interface board

The main components of the Interface board are:

• the ARM controller;



(a) Conceptual CAD model of the Waveform Digitizer board





Figure 3.4: Schematic representation of the Waveform Digitizer layout.

- the DACs.
- the ADCs.

These components have no particular problem in the connection with the board from a thermal point of view. They can be cooled by the copper ground layer inside the printed circuit board. Since the Interface board has an estimated power dissipation of the order of 2 W, we have decided to do not worry about them, and to focus on the refrigeration of the Waveform Digitizer boards. Each Interface board is placed side by side to one Waveform Digitizer. We have taken into account the power generated by the Interface boards, but we haven't accurately verified the temperatures of their components since a simplified simulation shows they are we are below the limits.

3.3 The Waveform Digitizer cooling system

The cooling system of the Waveform Digitizer boards consists of several parts connected in order to create a thermal bridge with an adequate overall thermal resistance. The whole system has been designed in order to be easily mounted and dismounted in occasion of the scheduled shut downs for maintenance.

Fig. 3.5 shows the Waveform Digitizer board. The assembled board is inserted into the crate which provides the mechanical support and the cooling through the fluid which flows through the pipes soldered to the crate walls (Fig. 3.6).

These are the main components of the thermal circuit:

- thermal pads;
- aluminum plate;
- cardlocks;
- crate;
- pipe.

It is important to notice that connections are made in vacuum condition and the thermal contact resistance can be significant. So contact thermal resistances between materials taken into account in our calculation and possibly measured experimentally.

3.3.1 Thermal pads

The function of the thermal pads is to create a stable thermal contact between the electronic components and the aluminum plate (Fig. 3.7). The pads are


Figure 3.5: Exploded view of the Waveform Digitizer board and the parts of the thermal bridge.

sized properly to fit over each component and to provide a good thermal conductivity. The planarity of the electrical components is not guaranteed, due to the soldering process to mount them. Also the dimensional tolerance of the aluminum plate cannot assure a good planarity of the surfaces which should be in contact with the electronic components. The optimal thermal contact between the electrical components and the aluminum plate is not guaranteed. In vacuum a contact not adequate between two objects implies a very high thermal resistance at the interface.

Using these pads compensates for possible misalignments between surfaces. The requirements for the pads are:

- low hardness;
- low thermal resistance;
- very low out gassing;
- high radiation hardness.

We have chosen the pad $ASKER \ C \ 8 \ 1 \ mm$ thick of the CPSS Series of RoHSCompliant. It adequately satisfies the requested characteristics (B.4). It is very soft, it has a 8 value in the ASKER C hardness scale ¹ (Fig. 3.8).

¹Asker C is a measuring device used to measure hardness with a durometer (a spring



Figure 3.6: View of the crate with the soldered pipe used for the cooling fluid flow.

The thermal conductivity of the pad is 2 W/m K. The thermal resistance depends on the dimension of pads. The thermal resistances of the pads for each component are summarized in Table 3.1.

	FPGA	DC-DC	ADC
Size $[mm \times mm]$	35×35	15×11	8×8
Thermal resistance $[K/W]$	0.41	3.03	7.81

Table 3.1: Thermal resistances of pads used for the FPGA, the DC-DC converter and the ADC.

The pads are made of a silicon-free material and no siloxane outgassing is expected. This means they can be used in vacuum with a very limited release of molecules. Unfortunately, we have no quantitative data about

hardness scale) as stipulated in SRIS0101 (SRIS: Society of Rubber Industry [Japan] Standards). When a 20 is listed for Asker C in a physical properties chart, this indicates that the value measured with the Asker C hardness scale is 20. In contrast to a needle penetration test or cone penetration test, larger numbers indicate a harder material.



Figure 3.7: Example of thermal pad used to improve the thermal contact between the electrical components and the aluminum plate.



Figure 3.8: Asker hardness scale with some examples.

outgassing properties and radiation hardness. Pads of the same material family have been used in vacuum conditions with good results, so we expect a similar behavior in our case. This will be verified experimentally with the first assembled prototype.

3.3.2 Aluminum plate

As we have anticipated, the electrical connections between the components and the internal metal layers do not allow to dissipate the thermal power with an adequate thermal gradient. The board substrate has a very low thermal conductivity $(0.29 \div 0.343 W/m K$ through-plane and $0.81 \div 1.059 W/m K$ in-plane). Hence an auxiliary external high conductive plate is required. Since the dimensions of the components and the height from the printed circuit changes from component to component, the solution is a formed aluminum plate shaped properly to be in contact with each electrical components (Fig. 3.9). We also decided to form the plate to have some threaded feet in order to connect the plate with the board and to link them into an unique body (Fig. 3.10 e Fig. 3.11).

The shape of the plate leaves space for the connectors both in the front



Figure 3.9: CAD model of the aluminum plate used as a thermal bridge between the board and the crate walls.

and rear sides of the board. There is 0.5 mm left in height for pads housing between the plate and the components, to be sure pads are squeezed and in a good thermal contact. There are through holes in the left and right sides of the board to let the cardlock be screwed with both the Waveform Digitizer board and the plate. The technical drawing is reported in Appendix A. The material chosen for the plate should obviously be a good thermal conductor. It should be easy to form, light and, obviously, cheap. We have considered two possible options: aluminum and copper. They have quite similar thermal conductance for a comparable mass. If they have the same weight, their thermal conductivity is almost equal. The advantage of copper would be a thinner plate. We have chosen aluminum to be homogeneous with the rest of the structure. Although they will work under vacuum condition, they have to be manipulated before, and they can oxidize and increase the contact thermal resistivity. Moreover, they have to be connected with cardlocks, that are made of aluminum, and by choosing the same material any chance of electro-galvanic erosion is prevented.

We have chosen the alloy aluminum of series 1100-O with an elongation of 20%. We have used Ansys Workbench for the thermal analysis. After some preliminary considerations and a simplified calculations, we have decided to use a 3 mm thick aluminum plate. This choice has been made for a technical reason: we want to produce these plates without expensive procedures like a



Figure 3.10: View of the aluminum plate section. The shape of the plate in order to be at the proper height is visible.



Figure 3.11: Section view of the aluminum plate with components and the board. Section and the components are labeled.

mold die, but having a limited thermal drop. We have found this thickness is a good compromise. In the steady state thermal analysis, surfaces in contact with cardlocks have been considered at homogeneous temperature. They are close to the pipes with the cooling fluid, that can be assumed to have constant characteristics during the refrigeration of a single board. This approximation has been done to have a simpler model. The heat sources are thermal fluxes located in areas where the electrical components are placed. Irradiation from the external surfaces has been neglected, so the whole body has an adiabatic constraint. The resulting temperature distribution is shown in Fig. 3.12. Fig. 3.13 shows the result of the z-axis heat flux. We can imagine a fictitious parallel thermal resistances for the three types of electrical components, as shown in Fig. 3.14, whose values are collected in Table 3.2. This will be useful in Section 3.6.

In the real case a limited fraction of heat is going to propagate through the printed circuit board. This effect can have only a positive effect to reduce the



Figure 3.12: Temperature distribution on a 3 mm thick aluminum plate.



Figure 3.13: Z-axis heat flux distribution of the 3 mm thick aluminum plate.

thermal gradient. By neglecting this effect in the simulation we have made a conservative assumption.

	FPGA	DC-DC	ADC
$\Delta T_{max} \ [^{\circ}C]$	4.76	4.68	2.84
Thermal resistance $[K/W]$	1.90	1.56	6.04

Table 3.2: Temperature drops and thermal resistances of the aluminum plate for single components.



Figure 3.14: Analogy of the plate temperature drop with an electrical circuit.

3.3.3 The cardlocks

We have decided to use one cardlock for each side of the board. The lock the waveform digitizer board and the aluminum plate in the right position and transfer heat to the crate (Fig. 3.15). Cardlocks are used to secure a printed circuit board in a crate as well to transfer heat to their housing (crate). They allow an easy mount and dismount operation and they are made by a series of separated blocks held together by a proper screw system. They have a taper side that allows expanding when the connecting screw system has been tighten.

We have chosen a cardlock made of five trapezoidal shaped blocks (one fixed and four mobile). Which slip on a unique and fixed rail. When they are axially compressed by screwing a bolt, they enlarge in the transversal direction (Fig. 3.16).

We have chosen the cardlock Series 265 of Calmark, which is 210 mm long. The data sheet is reported in Appendix B.5. We have made this choice for several reasons. First of all, the dimensions are the best option for our geometry given the required thickness and length. It has a higher working pressure and it leads to a better thermal contact with the crate. It has



Figure 3.15: Positioning of cardlocks on the Waveform Digitizer.



Figure 3.16: Cardlock mechanism. When the cardlock is axially compressed by screwing a bolt, it enlarges in the transverse direction.

good thermal properties and it is qualified for vacuum. Nevertheless, the producer does not guarantee the value of its thermal resistance in vacuum. The datasheet reports only an approximate estimate which corresponds to an increase of 40% with respect to the operational condition at the atmospheric pressure. To estimate the temperature drop between the cardlock sides I have used the chart suggested by the producer (Appendix B.5). Considering a total pair length of 17 inches, and using the 4°C in/W curve, the estimated thermal resistance of one cardlock has been estimated 0.6°C/W. If we increase this value by 40% the estimated thermal resistance increases to 0.9°C/W.

Since the cardlock is used in vacuum, also the temperature drop of the interface has to be taken into account. The idea is to fix the cardlock to the plate with a thermal glue that can operate in this condition and has good thermal properties. We have no reason to dismount a cardlock from the aluminum plate, and there are many types of glues that could satisfy these requirements. For example, $3M^{TM}$ Thermally Conductive Epoxy Adhesive TC-2707 is an epoxy glue with a thermal conductivity value of 0.72 W/m K. Assuming a layer 0.1 mm thick of such glue, we have estimated a thermal resistance of 0.15 K/W. If we need to decrease this thermal resistance, we can use more expensive glues, made of aluminum-nitride, that have a thermal conductivity up to 2.5 W/m K

This cannot be done on the other side of the cardlock which is in direct contact with the aluminum of the crate. In vacuum the temperature drop between two surfaces depends on several features: the materials, the roughness, how the surfaces have been machined, the contact pressure, the hardness of the materials and the heat flow direction. It is a very complicated problem, there are several theories and models, and they require a lot of information. The level of detail of the current analysis and design does not require this level of accuracy. So a simplified analysis has been performed and only the materials and the pressure are taken into account [7]. Assuming a connection between aluminum and a pressure of 2360 kN/m^2 on a surface of 660 mm^2 , the thermal resistance has been estimated $0.1 \div 0.3 K/W$.

3.4 The aluminum crate

The 240 Waveform Digitizer and Interface boards are placed in 24 crates. The function of the crate is to store and to cool the boards.

Because of space limitations in the cryostat, we could not adapt any commercial crate to our case and we have been forced to design a custom crate. In this way there are no limits imposed by producers. Furthermore, it can be partially built at the INFN workshop. During the design, the machining possibilities of the INFN workshop have been considered. INFN laboratories have several 3-axis CNC machines, and the solution is to build a crate made of four aluminum sheets, fastened together by screws, and machined on both sides. In Fig. 3.17 and 3.18 a CAD model of the crate has been reported.

The crate should be as compact as possible and have good thermal transmission properties. During the design we have made every possible effort to save as much space as possible by reducing the size of each component. To improve thermal transmission we have decided to solder the refrigerating pipe to the opposite side of the aluminum sheet where the boards are connected. The thermal resistance between the pipe and the boards is very low. Thickness of the sheet and steps used to support the boards are sufficient to have a good heat distribution, and to have a better usage of the pipe sur-



Figure 3.17: CAD model of the crate.

face. We have chosen the alloy aluminum of series 5083-O. It is an alloy with magnesium (up to 4.5%) which can be easily welded. Each hole has to pass through in order to not have any pocket of air that would increase the outgassing rate. Some small steps have been designed to simplify the mounting process and to have reference surfaces for the assembly (Fig. 3.19).

The pipe is made of three parts: two of them are welded to the crate sides, and they have the shape of a coil; they are connected together by a third segment of pipe, brazed successively (Fig. 3.20). It is shaped to allow an easy insertion of boards after welding.

The outer and the inner diameter of the pipe are respectively 5 mm and 4 mm. The material is Al1100-O. The coil has been designed to be brazed on the surface of the aluminum plate, but actually it is possible to weld it. Due to the reduced thickness of the pipe, welding may be complicated.

The design of the coil has been made to have a good temperature distribution and to set similar temperature boundary conditions for all the boards. This is an advantage for electronic purposes, because all the boards function approximately at the same temperature. We have used Ansys Workbench (a FEM software) to perform the simulation and we have achieved a configuration which sets the difference of boundary temperature of the boards below $1^{\circ}C$. The boundary condition of the FEM model has been adiabatic surfaces,



Figure 3.18: CAD model of the crate with sizes.

a fixed temperature of $0^{\circ}C$ in the inner side of the pipe and a flux of 7.5 W for the Waveform Digitizer boards and 1 W for the Interface boards. We assumed a thermal conductivity of 222 W/m K for the Al1100-O, 121 W/m K for the Al5883-O, and 100 W/m K for the brazing.

The thermal resistance of the crate side and the pipe welded to it is $0.23 \ K/W$. If the total inert gas welding process is chosen, the thermal resistance decreases.

Pipes have to be compatible to an internal pressure of 2.5 MPa. According to the Article D-2 (AD-201) [8] the minimum required thickness of the pipe with a given internal pressure is:

$$t = \frac{PR}{S - 0.5P} = 0.07 \ mm$$

Where P is the internal pressure (2.5 MPa), R is the internal radius (2 mm) and S is the membrane stress intensity limit and is taken from tables of design stress intensity values in Subpart 1 of part D of [9] (69 MPa).



Figure 3.19: Detail of the step for helping the assembling process.



Figure 3.20: Detail of the pipes connection on a crate.

3.5 The refrigerant fluid

We have chosen Suva 410A (technical data are reported in the Appendix B.6) at the temperature of $25^{\circ}C$ in boiling conditions. The reason is that the refrigerating system is shared between the tracker and the calorimeter. The tracker group has already designed the mechanics of the detector and they use this refrigerant for two reasons: they want to work at room temperature, for mechanical-thermal reason of the tracker structure; the storage vessel



Figure 3.21: FEM simulation of the temperature distribution on the side plate of crate. We have reported the temperature difference between the pipe temperature, that has been set to $0^{\circ}C$ as reference point, and the contact surfaces of the boards. The two columns with the higher temperature are the contact surfaces with the Waveform Digitizer boards. As expected the contact surfaces with the Interface boards do not reach high temperature.

(which also serves as the heat exchanger) and pumps are recycled from the CDF experiment, a previous Fermilab experiment, which used SUVA410a for the cooling of the Central Outer Tracker. This will save approximately 30.000 \$.

We have taken into account the temperature drop at the boundary layer inside the pipe. Since the fluid inside the tubes is boiling, the estimate of the heat transfer coefficient is hard. We have pipes which run both horizontally and vertically, and SUVA410a quality changes with the position along the circuit. In order to have a conservative estimate of the temperature drop a film coefficient value for SUVA410a in a fluid state has to be taken into account. The film coefficient value (as the flow regime) is usually a function of the quality of the fluid, as shown in Fig. 3.22.

Since we have decided to maintain an approximate quality of 0.2 at the end of the refrigerating path (as explained in Chapter 4), we can assume the film coefficient would be similar to that the SUVA410a has in a fluid state [10]. The average velocity of the fluid inside the pipe is approximately 2 m/s (as explained in Chapter 4), so the flow rate is $25 \text{ cm}^3/s$. The resulting



Figure 3.22: Qualitative variation of the heat transfer coefficient and flow regime as a function of quality for internal flow boiling in a horizontal tube. Reproduced from Carey (1992).

Reynolds number is approximately

$$Re = \frac{\rho u \Phi}{\mu} = 71000$$

where ρ is the Suva density in liquid state at 25°C, u is the average velocity in the pipe, Φ is the inner diameter and μ is the viscosity of SUVA410a in the liquid state at 25°C. Given the estimated Reynold number, the fluid is in a turbulent flow.

The resulting Prandtl value in this condition is approximately

$$Pr = \frac{c\mu}{k} = 2.49$$

where c is the specific heat [J/kg K], and k is the thermal conductivity [W/m K] of the liquid SUVA410a at 25°C. This value of Prandtl implies that the momentum diffusivity dominates in confront of the thermal diffusivity. To evaluate the film coefficient we have estimated the Nusselt number

$$Nu = 0.023 Re^{0.8} Pr^{0.3} = 236$$

where we have used the Dittus-Boelter relation for turbulent flow. The resulting heat transfer coefficient is

$$h = \frac{Nuk}{\Phi} = 5230 \frac{W}{mK}$$

By considering an approximate area which exchanges heat of

$$\Phi \times L = 1000 \ mm^2$$

where L is the length of a branch of the pipe which cools just one board, the resulting thermal resistance of the film is approximately $0.2 \ K/W$.

3.6 Thermal analysis

We have determined all the thermal resistances of the heat path from the pipe to the electronic components placed on the Waveform Digitizer. Table 3.3 reports all the estimated thermal resistances and the estimated temperature drops.

Component	Symbol	[K/W]	[W]	$\Delta T [^{\circ}C]$
FPGA Package	$R_{FPGA Tj}$	14.4	2.5	36
DCDC Package	$R_{DCDC Tj}$	16.7	3	50
ADC Package	$R_{ADC Tj}$	2.90	0.5	1.4
FPGA Pad	$R_{FPGA Pad}$	0.41	2.5	1
DCDC Pad	$R_{DCDC Pad}$	4.27	3	9.1
ADC Pad	RADC Pad	3.03	0.5	3.7
FPGA plate	$R_{FPGA\ Al}$	1.90	2.5	5
DCDC plate	$R_{DCDC Al}$	1.56	3	4.7
ADC plate	$R_{ADC Al}$	6.04	0.5	2.9
Glue	R_{glue}	0.154	7.5	1
Cardlock	R_{CLock}	0.90	7.5	7
Interface	R_{gap}	0.25	7.5	2
Crate	R_{Crate}	0.23	7.5	2
Boundary layer	$R_{B \ layer}$	0.19	7.5	1

Table 3.3: Thermal resistances and temperature drops for all the elements of the thermal circuit.

The equivalent electrical circuit for half of the crate with boards is shown in Fig. 3.23.



Figure 3.23: Equivalent electrical circuit to the thermal circuit made of the Waveform Digitizer and the aluminum crate.

We have summed all the temperature drops determined for each component. Starting from the temperature of $25^{\circ}C$ of the cooling fluid as lower temperature, the maximum temperature is reached on the junctions inside the electrical components. For the FPGA, the temperature is $79^{\circ}C$, for the DC-DC it is $101^{\circ}C$ and for the ADC it is $45^{\circ}C$. Table 3.4 summarizes the temperature values and the security factors. The security factor has been calculated as the maximum temperature tolerable for the component, divided by the achieved temperature.

Component	$T_{max} \ [^{\circ}C]$	$T_{ac} [^{\circ}C]$	SF
FPGA	100	79	1.26
DCDC	125	101	1.23
ADC	85	45	1.87

Table 3.4: Estimated temperature on the junctions of the electrical components used on the Waveform Digitizer and their safety factors.

The most critical components are the FPGA and the DC-DC converter. They have a safety factor of $\simeq 25\%$, which means the temperature can exceed our estimate of 25% before the component reaches its critical temperature. These results are the outcome of calculations, estimates and simulation and provide useful information to understand what can be done to improve the power dissipation. Further experimental analysis is required to validate these results. However, as the histograms in Fig. 3.24 show, the most important temperature contribution is given by the package of the components. Sadly this thermal resistance cannot be modified because it is an intrinsic characteristic of each component. We have also to keep in mind the cardlocks thermal resistance value is highly variable. For this reason further tests are going to be arranged to test the performance of this component.

The safety factor can be improved by decreasing the operating tempera-

ture of the SUVA410a. It has a temperature of $25^{\circ}C$, but if we could decrease this value, with a lamination at the beginning of the pipes that point to the calorimeter, we would easily improve the safety factor. To do that we showed insert in the cooling system, just before the cryostat, a lamination valve we can set to decrease the temperature in the pipe, and check if the pumps supply the required higher pressure.

3.7 Design of the photo-sensors and front-end electronics cooling system

This part of the project has not reached the same level of maturity as the part relative to the waveform digitizer and interface boards cooling because the Mu2e Project has not chosen between the BaF_2 and CsI crystals yet. The two crystals require different photo-sensors which have different requirements in terms of operational voltage and temperature. While BaF₂ requires solarblind APDs which use high voltage and need a low temperature to limit the electronic noise, CsI uses more standard SiPM with looser thermal requirements. Some mechanical and thermal simulations have been performed by a mechanical engineering student of the University Guglielmo Marconi in Rome for his Master Thesis which he is going to defend in spring 2016. The current configuration includes the following: number of crystals per disk (910), the number of photo-sensors per crystal (2), and the number of front-end boards per crystal (1). In the worst case scenario, the total estimated power dissipated by two photo-sensors with the front-end board is 350 mW. The idea for the cooling is to insert the front-end board in a brass box (Fig. 3.25). All the 910 boxes are inserted in an aluminum backplate which provides a mechanical support to all the readout electronics and a thermal bridge to extract the dissipated power.

To remove the heat from the housing box of the front-end boards, an aluminum backplate connected to the outer and the inner cylinder of the calorimeter has been designed. Its function is also to be a mechanical stiffening element for the whole calorimeter. It consist of a 25 mm thick cylindric plate, it is divided in four quarters and fastened to the outer calorimeter cylinder (Fig. 3.26). It has 910 squared holes where the photo-sensors can be inserted. All the holes are placed to let the photo-sensor precisely face to the crystals.

An important complication for the cooling of the front-end boards is that the electronic characteristics of the photo-sensor are widely influenced by their temperatures. Since their measurements are strongly modified by the



Figure 3.24: Temperature drops caused by the individual parts of the thermal circuit per each electrical component: FPGA (top-left), DC-DC (top-right), ADC (bottom-left).



Figure 3.25: FEM steady state thermal simulation of a front-end board inserted inside its housing box.

temperature, they should be virtually at the same and constant temperature. To do that, an engraved pipe system has been designed, with a path that is highly distributed between all the holes (Fig. 3.27). In this way the plate can reach a quite uniform temperature and permit to have the same thermal constraints to all the front-end boards. Some simulations have been performed to verify this solution (Fig. 3.28).

Moreover, due to their particular electrical behavior, they have an efficiency value that is better at lower temperature. Hence the necessity to cool the photo-sensors. Some solutions are being studied in this months, waiting the technical decision to continue the efforts.

The cooling fluid for the cooling of the front-end boards is the SUVA410a, and it is the same for the whole detector. At the moment the piping system is connected in parallel for the front-end boards, the crates and the tracker. This means that the inlet flow has to be sized to take care of the back plate refrigeration too, but it will not change the external constraint for the refrigeration fluid of the crates, that is better explained in the Chapter 4.



Figure 3.26: Calorimeter disk view with the aluminum backplate and some front-end boards for example.



Figure 3.27: Detail of the actual pipe path on the aluminum back plate.



Figure 3.28: FEM steady state thermal simulation of the temperature distribution in the aluminum back plate with the actual pipe path.

Chapter 4

Integration of the calorimeter cooling system

In this Chapter we provide a schematic design of the distribution system of the refrigerant fluid throughout the entire calorimeter cooling circuit. This project has been made taking into consideration all the constraints deriving from the fact that the calorimeter and the tracker share the same cooling system. My primary goal has been developing quickly a satisfactory solution for both detectors in order to proceed rapidly with the technical drawings and then with the construction and assembly of a prototype for the experimental tests. We expect to receive sufficient information from the tests of the prototype to finalize the entire project.

4.1 Distribution of the cooling pipes along the calorimeter disks

The first step has been designing the connections of the cooling channels between consecutive crates. Obviously the simplest solution would be to connect the 24 crates in parallel directly to the cooling fluid supply. This implies there would not be any connection between consecutive crates. This would provide the best possible control of the fluid flow with the minimum pressure drop in the pipes. This is not possible because the number of pipes through the Instrumentation Feedthrough Bulkhead, would be too large. It would be possible for the calorimeter to tap off 24 individual lines from a single supply header, but the issue is that control and regulation of those individual line would need to be inside the DS warm bore (and thus in the magnetic field) and it is very complicated. The Instrumentation Feedthrough Bulkhead function is to seal the cryostat, to minimize the air leaks from outside into the internal volume of the solenoid. During shut downs, we want a relatively simple access to the detectors. So the pass through elements have to satisfy the requirement to operate with a relative pressure of 1 atm with no leaks. On the other hand, it would be unreasonable to connect all the crates in series, since this would generate an excessive pressure drop along the small pipe. The fluid should be pushed with high pressure and the lamination would generate a large change of temperature in the boiling condition. In addition, it would be more complicated to test the system, since it would be hard to identify a single malfunctioning section. Due to the shape of the pipe, the most significant contributions to the pressure drop are the concentrate pressure drops caused by turns and junctions. If we take into calculation the pipes connected to a single crate, we have to consider a pipe length of approximately 7 m. The distributed pressure drop can be easily estimate with the Darcy-Weisbach formula:

$$\Delta p = f \cdot \frac{L}{\Phi} \cdot \frac{\rho u^2}{2}$$

where Δp is the pressure drop [Pa], L is the length of the pipe [m], Φ is its internal diameter [m], ρ is the density of the fluid [kg/m³], u is the average velocity of the fluid [m/s] and f is the Fanning factor, whose value can be estimated with the Blasius correlation for turbulent flow:

$$f = 0.079 Re^{0.25}$$

where Re is the Reynold number. The order of magnitude of this drop is around 10^{-2} bar which is negligible if compared to the concentrated drops. For each crate the pipe has 18 bends of 180 degrees and 14 bends of 90 degrees. The concentrate drop pressure is:

$$\Delta p = \sum_{i=1}^{n} K_i \frac{1}{2} \rho u^2$$

where K_i is 1.1 for the 90 degrees bends and 1.4 for 180 degrees bends. The order of magnitude of this pressure drop is 1 bar. In our case we do not have only a liquid fluid flow, but a boiling mixture of liquid and vapor. Since we decided not to exceed the quality of 0.2 in the output pipe, we considered a fluid made of liquid and vapor proportional with the quality. This means the velocities of liquid and vapor are approximately equal. Given the low quality this exemplification is not so wrong. We probably have bubbly flow, with bubbles velocity equal to the liquid fluid. If the quality increases too much, the annular flow prevails and this approximation is no longer satisfied.

We have estimated a value of density and viscosity of the two-phase mixture. This is the Homogeneous model ([10]):

$$\rho_{TP} = \left(\frac{x}{\rho_v} + \frac{1-x}{\rho_l}\right)^{-1}$$
$$\mu_{TP} = \left(\frac{x}{\mu_v} + \frac{1-x}{\mu_l}\right)^{-1}$$

where factors with TP are referred to the two-phase mixture and x is the vapor fraction (quality). The Reynolds and the Fanning factor are respectively:

$$Re_{TP} = \frac{GD}{\mu_{TP}}$$
$$f = 0.079 Re_{TP}^{0.25}$$

The drop pressure is given by the further correlation:

$$\frac{dP}{dz} = \frac{2f_{TP}G^2}{\rho TPD}$$

where dP/dz is the pressure drop per length of the pipe unit. Although fluid heating is a distributed process along the pipe, we made the simplified assumption that the fluid temperature is constant along the pipe of one single crate. The fluid temperature is increased in one step only at the exit of the crate. This procedure is iterated for all the crates. We have an estimate of 16 W dissipated for each board which provides a total power of 160 W dissipated in one crate. This power flows from the crate to the cooling fluid. By taking into account the flow rate, we have estimated the enthalpy extracted with the two-phase mixture. Using the software RefProp, we have estimated the thermal state per each step, and so refreshing all data. The result is the diagram reported in Fig. 4.1 which shows the transformation of the fluid during the cooling of three crates. The data of the calculated point are showed in Table 4.1 (for all the values calculated, see AppendixC).

11	Temperature	Pressure	Density	Enthalpy	Entropy	Quality
Ŧ	$[^{\circ}C]$	[MPa]	$[kg/m^3]$	[kJ/kg]	[kJ/kg K]	[kg/kg]
1	25,0	$1,\!657$	1059	239,9	1,137	$0,\!00$
2	23,5	1,592	620,4	$245,\!9$	$1,\!157$	$0,\!044$
3	20,7	1,477	343,2	256,4	1,194	0,12
4	16,5	1,313	193,7	271,5	1,248	0,22

Table 4.1: Calculated state points of SUVA410A.



Figure 4.1: Transformation of the fluid through the pipe of three crates. This is an enlargement of the enthalpy-pressure characteristic diagram of the SUVA410a fluid. The three dotted line represent the fluid transformation for each crate.

We have observed that after the refrigeration of two crates the quality raises above 0.2. Moreover, the temperature decreases excessively and boards would be in different conditions. For these reasons we have decided to connect just two crates in a row. This choice reduces the number of pipes that have to pass through the Instrumentation Feedthrough Bulkhead, even if not much. Fig. 4.2 and 4.3 show a possible configuration of the pipes and the connections among the crates. This part of the design has not been finalized yet. Groups have to discuss if this setting does not obstruct further operations of maintenance or cable routing.

We decided to have a unique inlet pipe among the Instrumentation Feedthrough Bulkhead with an internal diameter of 14 mm which grants a fluid velocity of approximately 1 m/s (the purple pipes in Fig.s 4.2 and 4.3). It arrives near the left foot of the calorimeter, it travels circumferentially next to the aluminum backplate and close to the crates, and it distributes the SUVA410a to the crates. From the main inlet pipe, one single pipe branches off per each pair of crates. After the pipe is driven above the crates again and it travels circumferentially close to the inlet pipe, until it reaches the right calorimeter foot, where all the outlet pipes are grouped and are led to the beam stop plate. In this configuration we have 1 inlet pipe with an external diameter



Figure 4.2: Back side view of the pair of crates connected in series.

of 16 mm and 6 outlet pipes with an external diameter of 5 mm per disk. We have to add the pipes for the refrigerating of the aluminum back plate and the front-end electronics. However the idea is to keep the pipe lines disconnected inside the cryostat, to test independently each single circuit with having no control devices inside the magnetic field. Once the pipes and the cables that have to pass through the Instrumentation Feedthrough Bulkhead have been defined, a design of their arrangement can be done.

4.2 System characteristics

The distribution system of the cooling fluid has to satisfy some additional technical requests. First of all we want to be able to move the two disks along the rails. When the cryostat is opened during shut downs, the Instrumentation Feedthrough Bulkhead is unbolted from the warm bore, and moved away at the end of the rail system; the two calorimeter disks and the tracker are pulled out with the Instrumentation Feedthrough Bulkhead outside the cryostat. They are all linked together in order to have a single train. This



Figure 4.3: Angular view of the pair of crates connected in series.

means that the relative distances between the Instrumentation Feedthrough Bulkhead and the calorimeter disks are fixed (Fig. 4.4).





In this way the distance between the calorimeter disks is fixed to 350 mm (Fig. 4.5). The operator who has to work on front-end boards and on the



Figure 4.5: Side view of the calorimeter disks.

waveform digitizer boards has a very limited amount of space available. A possible option to have more space is to allow an independent movement of the two disks. Allowing for this movement poses at least two problems:

- the cables and the pipes that connect the calorimeter to the Instrumentation Feedthrough Bulkhead plate have to allow for this movement;
- to create the train system, some beams are placed to connect the calorimeter disks, the beam stop and the tracker (not represented in Fig. 4.5). These beams have to be removable easily during dismounting process to avoid any risk for the structure.

The former can be solved with longer cables and pipes with low stiffness. This can be achieved with omega shaped pipes, or rubber flexible pipes that can be used in vacuum environment and with high pressure. However the calorimeter integration group strongly disfavor moving any element of the train relative to others.

The system should also have a control system for the Suva flow. The idea is to connect a digital fluxometer and a servo valve to each outlet pipe. In this way we can control the flow inside the pipes and have a feedback about the heating process inside the cryostat. This is not so easy because of the space to space limitations. We have reported below two possible solutions:

- placing all this equipment behind the backplate. In this way we can rejoin all the pipes together after the control system and have only one inlet and one outlet pipe for the whole detector. The problem is that in such place there is a high magnetic field, so all the instrumentation has to be magnetic hard or shielded in some way. Moreover, since the Instrumentation Feedthrough Bulkhead moves, all the equipment has to move with it;
- placing the control instrumentations in the pump room. We can use standard equipment because we are far from the magnetic field, but there is not very big space there, and we have to drive all the pipes in the pump room, that is in the upper floor. Moreover, the path of the pipes is shown in Fig. 4.6. The red segment is removed when the cryostat has to be dismounted in order to create space where to move the train. If this solution is chosen, there will be a group of at least 18 pipes, long about 10 m, that have to be mounted and dismounted every shut down. This is a very unpleasant option, and should be avoided if at all possible.



Figure 4.6: Map view of the distribution refrigerant fluid pipes.

Both the hypotheses have been evaluated. As things stand at the moment, the system components and a simplified layout of the cooling system are shown in Fig. 4.7

The refrigerant is at saturated condition and stored in a pressure vessel, which also houses a single heat exchanger rated at the maximum capacity of the detector. This heat exchanger transfers heat from the chilled water supply of the building. It also has additional valves making it capable of using a stand-alone chiller connected in either series or parallel with the



Figure 4.7: System components and simplified layout of the tracker and calorimeter cooling systems. [11]

buildings water supply (not shown in Fig. 4.7). The refrigerant then travels downwards into one of two 1.5 HP pumps. The first one is the main pump, the second one is a backup pump which automatically activates in the event of failure of the main pump. The sub-cooled/saturated liquid is pumped through stainless steel piping roughly 25 m to the area which houses the Mu2e tracker and calorimeter. Just outside the vacuum penetrations a phase separator is employed to assure no vapor is supplied to the detector. The cooling system is equipped with an array of instruments to measure pressure, flow rate, temperature, refrigerant level, and many other process variables. These variables are read by a programmable logic controller which controls the various pieces of equipment to ensure a stable temperature that matches the set point. All process readings are recorded and archived for future recall, or they can be read in real time. Any changes to the temperature set point is done through an easy to use touch-screen controller.

Chapter 5

Manufacturing and assembly of the crate

5.1 Manufacturing of the crate components

5.1.1 The aluminum plate

The 3 mm thick aluminum plate is going to be produced by an external manufacturing factory. These are the most relevant production phases:

- machining process of cropping the right size of the plate and the other machining operations;
- forming the plate;
- polishing the surfaces.

The machining process consists of cropping an aluminum rectangle 250 mm wide and 180 mm high from a 3 mm thick aluminum sheet, and boring the holes (Fig. 5.1). This can be done in the INFN workshop since it requires a CN Cartesian milling machine. The procedure consists of:

- drilling bores, with the plate locked by clamps on its sides;
- cropping the edges, with the plate locked by screws inserted in holes previously machined.

The forming phase will necessarily be commissioned to an external factory, since the required press machine is not available at the INFN workshop. The plate has to be formed and bent to its final shape, with its side bends and the formed feet. The technical drawing is reported in the Appendix A.



Figure 5.1: Starting aluminum plate and contour of the plane plate.

The polishing phase consists of a machining process of refining the surfaces of the areas of the plate that are in thermal contact with the other components, since the thermal conductivity contact value is higher when the surface have a good surface quality.

Another possible solution to make the process faster is to obtain the cropped and drilled plate by precision blanking process. Finally the realization of the threads by tapping. The whole process shall be done by the same bending factory. Since the number of plates we have to build is only 240, they will be quite expensive per plate because the cost of blanking spreads over relatively few plates. However a proposal to a factory will be delivered to have a comprehension of how much they cost with this alternative making process. Having a faster backup solution can be useful if something does not proceed as planned.

5.1.2 The crate sides

The crate sides can be manufactured by 3 Axis CN machines of INFN workshop. The row material is an aluminum sheet 25 mm thick for the lateral sides and a 10 mm thick aluminum sheet for the upper and lower sides. The single parts and assembly technical drawings are reported in Appendix A.

5.1.3 The aluminum pipe

The raw material for the coil mounted on each side is an aluminum pipe with an external diameter of 5 mm and 3.5 m long. I have designed a bending mask (Fig. 5.2) made of three main components.



Figure 5.2: Bending mask design to manufacture the coil.

- the base;
- the bending pegs;
- the bending blocks.

The straight pipe is laid down on the base, and kept in position by some sawhorse to prevent from bending. The first step is to lock the pipe with the two bending pegs and leave a distance of 400 mm from a pipe extremity (Fig.5.3).

The operator inserts the bending pegs in the counter-bores, which are references for their positioning, and locks them with the bolts (Fig. 5.4). Then he winds up the right side of the pipe around the peg for 185 degrees, which include 5 degrees of over bending. The pegs are designed to not flatten the pipe. The result of this operation is visible in Fig. 5.5a.

The operator continues making the remaining in plane bends, inserting each time a new bending peg. The result of this operation is shown in Fig. 5.5b. The right extremity of the pipe has been half-bent in order to avoid any interference with the bending procedure.



Figure 5.3: Starting condition of the bending procedure.



Figure 5.4: Sectioned detail of the bending peg.

Given the pipe length, the operator has to turn the base for the bending procedure. To this purpose he has to work on a smooth table which lets him to turn the base of the bending mask with no inconvenience. At this point the operator has to make the first out of the plane. He has to fix the first block on the pipe. The block has two dowel pins to refer itself on the plate, and it is locked by two bolts. After that, the operator bends the extremity in the proper groove (Fig. 5.6a). Bending grooves are designed in order to not flatten the pipe. They also allow an over bending of 10 degrees to make the pipe straight after the curves. Then he inserts the stop and locks it with



Figure 5.5: In plane pipe bending process.

two bolts. He can now make the second bend (Fig. 5.6b).



Figure 5.6: Sectioned detail of the first bending block.

After the first terminal bend, the operator has to remove the block he has just set, and to move on to the second terminal bend. He ends bending the extremity he has left before, and locks the pipe with another terminal block (block 1) as shown in Fig. 5.7. The block has two dowel pins as a reference on the plate, and it is locked by two bolts. After that, the operator bends the extremity in the proper groove. Then he mounts another block (block 2), which is referred by one dowel pin and lies on the block one side, and he locks it with one bolt. He can now make the second extremity bending following the engraved groove.

At this point he can dismount everything. The result of the whole bending process is reported in Fig. 5.8.

The last operation is the cutting and enlarging the extremities. He has to cut 8 mm after the bend, and enlarge the internal diameter of the pipe to



Figure 5.7: Sectioned detail of the terminal bending blocks.



Figure 5.8: Final result of the bending process.

5 mm, for the junction with the other pipes.

The other segments of the coil are manufactured with other bending masks, but since their design is not final yet, the bending masks haven't been designed and their design is postponed when a more precise model of the calorimeter is available.
5.2 Assembly of the crate

Since new development of the structure design and of the services location are expected in future, the goal of this Section is to provide a preliminary plan of the assembly.

The electronic mounting process will obviously follow the structural mounting process, so we have considered the whole structure will be already built when the electronic components have to be mounted. At the moment the mounting process of the electronics is organized in the following steps:

- mounting the crates off the calorimeter site;
- connecting the crates above the calorimeter disks;
- joining the pipes by welding that connect crates between themselves;
- connecting the cooling fluid distribution pipes with the backplate and the crates;
- inserting all the waveform digitizer boards and interface boards, previously equipped with the aluminum plate and the cardocks;
- connecting the front-end boards with the backplate and the crystals;
- routing all the connections between the boards and with the DAQ.

The crate is mounted into a first part, that consists of soldering the pipe to the crate sides, and the second part, that includes the assembly of the crate and the connection of the coils of the two sides between themselves. The former part can be done in Italy at the INFN, while the latter is done at Fermilab, because it doesn't requires particularly precautions. In this way the shipment will be easier.

The crate base has been designed having several through holes in order to be linked to the calorimeter outer cylinder by bolts (Fig. 5.9).

We need some supports where to lay the crates, and the easier way is to create an aluminum support to fasten to the outer cylinder by bolts. Since the space available radially inside the cryostat is limited, to have the smallest supports, they are connected by a couple of screw to the cylinder, but they have through holes just at the crate base holes because there is not enough space to let the screws grasp to the supports (Fig. 5.10). The bolts grasp directly to the cylinder, and the supports are used to create a planar surface where to lay the crates.

Another possibility is to build these supports and then to weld them to the calorimeter outer cylinder, and then to machine properly the cylinder to create tapped holes.



Figure 5.9: Detail of the crate base with holes for fastening it to the calorimeter outer cylinder.



Figure 5.10: Detail of the crate fixed to the calorimeter outer cylinder.

Chapter 6 Design of experimental tests

The Mu2e experiment is very complex and expensive and each component we use has to be accurately tested, to made sure it does not have any failure during data taking. Reliability is crucial, since any access to the detector is going to be limited to a few weeks per year. In our case, we want to perform outgassing and thermal tests of all the component before beginning the production. For the cooling system, we need to measure the thermal resistance of the components, the estimated maximum temperature of the electronic components and the pressure drops of the cooling fluid in the pipes. The INFN facilities allow to test the small and medium size components i.e. the electronic boards, the aluminum plate, the cardlocks and the crates. Given the larger size of the pumps and the cooling distributor system, these can only be tested at Fermilab experimental facilities. I developed a preliminary project of the experimental machine INFN is going to use to perform the local tests.

6.1 Outgassing measurements

We need to determinate the outgassing rate of the materials we use in a 10^{-4} torr $(1.3 \cdot 10^{-7} \text{ bar})$ vacuum environment. We can perform several useful tests. One uses the weight loss method, that is regulated by ASTM E595 and ECSS-Q-ST-70-02. It is commonly used for high outgassing rate materials, namely organics. In our case it can be a useful test for the electrical components, the pads and the thermal glues. We briefly outline the steps of a possible outgassing test:

• the samples are submitted to pre-conditioning (24 hours at 25°C and 55% rH) to allow moisture uptake;

- during the vacuum test (25°C and 10⁻⁴ torr for 24 hours) the outgassing behavior is determined by measuring the weight of the samples before and after thermal treatment;
- samples are also weighted after a post-conditioning (24 hours at 25°C and 55% rH) allowing recovery of lost moisture.

Then the sample is weighted out with a precision balance. We expect to determine the following parameters from the outgassing test:

- TML (Total Mass Loss): Total mass loss relative to the initial sample mass;
- RML (Recovered Mass Loss): Mass loss after water absorption during post-conditioning (relative to initial sample mass);
- CVCM (Collected Volatile Condensable Material): mass gain of collectors relative to initial sample mass.

The qualitative mass evolution with time is shown in Fig. 6.1.



Figure 6.1: Qualitative mass evolution of a specimen during a weight loss method outgassing test.

The sample sizes are 8 mm x 8 mm x 10 mm maximum and 3 samples per material are required for statistical evaluation. The weight of each sample has to be between 100 mg and 300 mg.

To perform this test we need a small vacuum chamber, that can achieve 10^{-4} torr, and a balance with a tolerance of at least 10^{-4} g and a DAQ. If a

mass spectrometer is available, the characterization of the type of outgassing gases is possible.

An alternative test uses the throughput method. This method is commonly used when upper limits of outgassing rate are needed and the sample is very large. We can use this test for the outgassing measurement of the full mounted crate with all the boards installed. The idea is to apply the desired pressure with a vacuum pump in a vacuum chamber, to turn off the pump and to read the pressure value as a function of time. The pressure inside the chamber increases due to the outgassing and the leaks. The parameter provided by this test is the slope of the curve pressure vs time (Fig. 6.2) which represents the outgassing rate.



Figure 6.2: Qualitative pressure evolution with time of a specimen during a throughput method outgassing test.

To perform this test a vacuum chamber bigger than the crate ($\geq 500 \times 600 \times 300 \text{ mm}$) is necessary with a high vacuum gauge and a DAQ. All these measurements are very time-consuming. Each measurement can require up to 3 days of measuring time, to which the setup time be added.

6.2 Thermal measurements

The goal of these tests is to determine the thermal resistance of the components, and the maximum temperature achieved on the boards. To evaluate the thermal resistances, we need a thermostatic vacuum chamber, big enough to include the components and the instrumentation. The specimen has to be kept in position with no thermal contacts except for the surfaces we want the heat to pass trough. We also need some heating devices as resistors that can create the appropriate heat flux and some temperature sensors. These could be some cheap resistance temperature detectors (RTDs) like a PT100, or a more complex visual system as thermo-graphic camera and a DAQ. These tests provide precious information relative to the thermal behavior of the components, for examples the cardlock, the thermal pads and the aluminum plate. To calculate the thermal contact resistance we need to know before the resistance of the elements that are in contact singularly, and then measure the temperature drop when they are connected together, and calculate the contact thermal resistance by difference. To determine the temperature reached on the electronic components on the boards, we need to build an entire crate completely filled with dummy boards. Given the cost of real boards we accept to simulate the thermal behavior with dummy boards filled with resistors to simulate the component power dissipation. We also need a system to supply the cooling fluid in the proper thermodynamical conditions. This requires a pumping system for the SUVA410a up to 2.5 MPa of pressure, a chiller that can refrigerate the SUVA410a to 25°C, a valve lamination system to set the quality of the fluid and a pressure gauge to visualize the quality by reading the pressure or a temperature sensor to do that by reading the temperature, a flow meter to characterize the piping channel, a phase separator, more than the thermostatic vacuum chamber, the temperature sensors and the DAQ. In Fig. 6.3 a CAD sketch model of the specimen support is shown. With the instrumentation required for the temperature tests, we are able to



Figure 6.3: CAD sketch model of the specimen support for thermal and temperature measurements.

perform the pressure drop tests too. If we adjust the experimental machine with an inlet and outlet pressure gauges for measuring the pressure at the beginning and at the and of the pipe, we are able to calculate the pressure drop inside the coil.

Chapter 7 Conclusions

My work has been the design of the cooling system for the electronics of the Mu2e electromagnetic calorimeter at Fermi National Accelerator Laboratory. The goal of the Mu2e experiment is to search for the neutrino-less coherent conversion of a muon to an electron in the field of an aluminum nucleus, a physics process which would be the evidence of physics beyond the Standard Model. The experiment is currently in construction and is expected to begin commissioning in the year 2020. Many technical solutions for the experimental apparatus, for the beamlines, magnets, and detectors, are still under study, with more than one option available in several cases. This is the case also of the electromagnetic calorimeter, which is being designed and is going to be constructed by a collaboration among the Italian Istituto Nazionale di Fisica Nucleare, the California Institute of Technology, and Fermilab. It is a wide collaboration with many groups of physicists and engineers involved.

My first task has been collecting the technical information necessary to understand the external constraints deriving from the characteristics of the experimental area, the technical characteristics of the calorimeter electronics which pose the performance requests on the cooling system. I have been in continuous contact with the INFN-Pisa, INFN-Frascati and the Fermilab groups during the 8 months, from March 2015 to October 2015, I have dedicated to my Thesis. I was also awarded a 2-month scholarship by the Universities Research Association to visit Fermilab in August and September 2015.

The main problem of cooling the Mu2e calorimeter electronics is that the detector is installed inside the Mu2e cryostat which is evacuated at the pressure to 10^{-4} torr. This is necessary to reduce the interactions of beam particles and muon decay products with gas, since this may produce undesired signals in the Mu2e detector which may mimic the backgrounds searched by the experiment. In this condition, the power generated by electronics boards

has to be dissipated through conduction.

The entire electronics apparatus of the calorimeter can be divided in two main subsystems, which can be ideally separated for the different functions and location. The first subsystem is located on the back side of the crystal disks. It contains the photo-sensors, which collect the scintillation light produced in the crystals, and the Front-end electronics, which receive and amplify the electric signals from the photo-sensors and transmit these signals to the Waveform Digitizers. There is a total number of 1820 photo-sensors and a total number of 910 Front-end electronics boards for each calorimeter disk. The second subsystem is radially located on the external side of the calorimeter. It contains the Waveform Digitizers, which receive the data from the Front-end electronics and perform a digitization of the signals which are transmitted to the data acquisition system of the experiment, and the Interface boards, which provide the voltage to the Front-end and the photosensors and drive the voltage regulation to the photo-sensors. This is a crucial function, since the photo-detectors performance depends on the voltage, which has to be accurately regulated and monitored. There is a total of 120 Waveform Digitizer and Interface boards for each calorimeter disks which are hosted in 12 crates per disk.

For both subsystems the cooling system is integrated in the mechanical support structure and uses the cooling fluid SUVA410a. The cooling circuit used for the calorimeter is actually part of a larger system which performs the cooling also of the tracker. Both the tracker and the calorimeter receive and use SUVA410A at $25^{\circ}C$.

The photo-sensors and the Front-end boards are mechanically supported by an aluminum backplate, which is also a stiffening element of the entire calorimeter mechanical structure. The Front-end boards are thermally connected to the aluminum plate with metal surfaces and the plate is refrigerated by a pipe engraved in the plate itself. This provides a homogeneous temperature on the plate and keeps the photo-sensors and the Front-end boards approximately at the same temperature throughout the entire calorimeter disk. The design of this part of the cooling system is part of the Master Thesis of a Mechanical Engineering of a student of the Università Guglielmo Marconi in Rome. Each Interface board is paired to a Waveform Digitizer. Ten of these pairs of boards are placed in one crate. Given the total of 120 required pairs of boards for 1 disk, 12 crates are necessary for each disk. The 12 crates are placed externally to the disk in the radial direction. The crate function is to provide a mechanical support for the boards, but also a thermal path to extract the power dissipated by the electronics components. We must make sure the temperature of each component do not exceed the limit specified in the specification.

For the Interface board, which has a total power dissipation of 2 watt, and the Waveform Digitizer, which has a power dissipation of 15 watts, we use slightly different technical solution. For the interface boards, power is extracted through an metal layer internal to the printed circuit board and mechanically connected to the crate walls. This simpler solution cannot be used on the more complex Waveform Digitizer board and in this case we have decided to add an external aluminum plate on the top of the printed circuit board placed in thermal contact with the electronic components (FPGA, DC-DC converters, ADC) with larger power dissipation. The aluminum plate is locked to the printed circuit board and to the crate with a set of cardlocks which provide adequate thermal conductance and are easy to mount. I have performed a detailed thermal analysis of all the crate components, I have estimated all the thermal resistances and the temperature of all the components. I have verified that my design provides an adequate cooling of all the electronic components. I have also worked on the design of the cooling fluid distribution system, with a project of the entire pipe circuit from the external pumps and chiller, to the calorimeter crates.

Part of my Thesis has been dedicated to optimize the placement of the crates inside the cryostat. This has been a critical decision which has required the interaction with independent groups, the group involved in the distribution of the services (i.e. electric cables and cooling pipes) to the tracker and the calorimeter and the group responsible of vacuum creation and maintenance inside the cryostat. Although not completely final, my project has been taken as a solid and complete plan which may still evolve.

I have also worked to develop possible manufacturing solutions to build the crate, the welded coil, and the aluminum plate which covers the Waveform Digitizer. I concluded my work with the design of the tests necessary to verify the thermal and outgassing performance of the components and of the entire cooling system. These tests are going to be performed at INFN-Pisa in the next few months.

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Appendix A Technical drawings



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Appendix B

Data-sheets

B.1 FPGA





Note: Dimensions are in millimeters. Refer to the "FC1152 Package Mechanical Drawing Dimensions" section on page 70 for the dimensions.

Supported Devices					
SmartFusion2 (M2S150)	IGLOO2 (M2GL150)				

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FC1152 Package Mechanical Drawing Dimensions

JEDEC Equivalent	FC1152 (page 69) Min. Nom. Max.			
Dimension				
A	2.34	2.62	2.90	
A1	0.40	0.50	0.60	
A2		0.8		
aaa		0.20		
b	0.50	0.64	0.70	
ccc		0.25		
D	34.85	35.00	35.15	
D1	33.00 BSC			
D2	29.00 REF			
D3		27.00 REF		
E	34.85	35.00	35.15	
E1	33.00 BSC			
E2	29.00 REF			
E3	27.00 REF			
e	1.00 BSC			
eee	0.25			
fff	0.10			

Notes: 1. All dimensions are in millimeters. 2. BSC = Basic spacing between centers.

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2 – SmartFusion2 DC and Switching Characteristics

General Specifications

Operating Conditions

Table 2-1 • Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units	Notes
TJ	Junction temperature	Commercial	0	25	85	°C	
	Junction temperature	Industrial	-40	25	100	°C	
VDD	DC core supply voltage		1.14	1.2	1.26	V	
VPP	Power supply for charge pumps (for	2.5 V range	2.375	2.5	2.625	V	
	normal opeartion and programming)	3.3 V range	3.15	3.3	3.45	V	
PLLx_VDDA	Analog power supply for PLL0 to	2.5 V range	2.375	2.5	2.625	V	
	PLL5	3.3 V range	3.15	3.3	3.45	V	
PLL_PCIE_x_VDDA	Auxiliary power supply voltage by	2.5 V range	2.375	2.5	2.625	V	
	core to macro	3.3 V range	3.15	3.3	3.45	V	
PLL_MDDR_VDDA	Analog power supply for PLL	2.5 V range	2.375	2.5	2.625	V	
	MDDR	3.3 V range	3.15	3.3	3.45	V	
PLL_FDDR_VDDA	Analog power supply for PLL FDDR	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
PCIExVDD	PCIe/PCS power supply		1.14	1.2	1.26	V	
PCIExVDDIO[L/R]	Tx/Rx analog I/O voltage supply		1.14	1.2	1.26	V	
PCIExVDDPLL[L/R]	Anlog power supply for SERDES PL	L of PCIe	2.375	2.5	2.625	V	
VDDIx	1.2 V DC supply voltage		1.14	1.2	1.26	V	
	1.5 V DC supply voltage	1.425	1.5	1.575	V		
	1.8 V DC supply voltage		1.71	1.8	1.89	V	
	2.5 V DC supply voltage		2.375	2.5	2.625	V	
	3.3 V DC supply voltage		3.15	3.3	3.45	V	
	LVDS differential I/O		2.375	2.5	3.45	V	
	B-LVDS, M-LVDS, Mini-LVDS, RSDS	6 differential I/O	2.375	2.5	2.625	V	
	LVPECL differential I/O		3.15	3.3	3.45	V	
VREFx	Reference voltage supply for FDDR MDDR (bank 5)	0.49 * VDDI0	0.5 * VDDI0	0.51 * VDDI0	V		
VCCENVM	Embedded nonvolatile memory	2.5 V range	2.375	2.5	2.625	V	
	supply	3.3 V range	3.15	3.3	3.45	V	

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SmartFusion2 DC and Switching Characteristics

Product Grade	Storage Temperature	Programming Temperature	Element	Grade Programming Cycles	Retention
Commercial	Min. T _J = 0°C Max. T _J = 85°C	Min. T _J = 0°C Max. T _J = 85°C	FPGA	500	20 years
		Min. T _J = 0°C	Embedded Flash	< 1,000	20 years
	Max. T _J = 85°C			< 10,000	10 years
Industrial	Min. T _J = –40°C Max. T _J = 100°C	Min. T _J = 0°C Max. T _J = 85°C	FPGA	500	20 years
		Min. T _J = –40°C	Embedded Flash	< 1,000	20 years
		Max. T _J = 100°C		< 10,000	10 years

Table 2-2 • FPGA and Embedded Flash Programming, Storage and Operating Limits

Power Supply Sequencing and Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every SmartFusion2 SoC FPGA. These circuits ensure easy transition from powered-off state to powered-up state of the device. The SmartFusion2 system controller is responsible for systematic power-on reset whenever the device is powered on or reset. All the I/Os are held in a high-impedance state by the system controller until all power supplies are at their required levels and the system controller has completed the reset sequence. The power-on reset circuitry in SmartFusion2 devices requires the VDD supply to ramp at a predefined rate. Four ramp rate options are available during design generation: 50 µs, 100 µs, 1 ms, and 100 ms.

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Revision 0



SmartFusion2 System-on-Chip FPGAs

Thermal Characteristics

Introduction

The temperature variable in the SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. Eq 1 through Eq 3 give the relationship between thermal resistance, temperature gradient, and power.

 θ_{JC}

$$\theta_{\mathsf{J}\mathsf{A}} = \frac{\mathsf{T}_{\mathsf{J}} - \theta_{\mathsf{A}}}{\mathsf{P}}$$

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

$$= \frac{T_J - T_C}{P}$$

EQ 3

where

- θ_{JA} = Junction-to-air thermal resistance
- θ_{JB} = Junction-to-board thermal resistance
- θ_{JC} = Junction-to-case thermal resistance
- T_J = Junction temperature
- T_A = Ambient temperature
- T_B = Board temperature (measured 1.0 mm away from the
- package edge)
- T_C = Case temperature
- P = Total power dissipated by the device

Table 2-3 • Package Thermal Resistance

	θ_{JA}					
Product	Still Air	1.0 m/s	2.5 m/s	^θ јс	θ _{JB}	Units
M2S050T-FG896	14.7	12.5	10.9	7.2	4.9	°C/W

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SmartFusion2 DC and Switching Characteristics

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another. The maximum power dissipation allowed is calculated using EQ 4.

Maximum Power Allowed =
$$\frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100°C. EQ 5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2S050T-FG896 package at commercial temperature and in still air, where

 θ_{JA} = 14.7°C/W (taken from Table 2-3 on page 2-3). $T_A = 85^{\circ}C$

Maximum Power Allowed =
$$\frac{100^{\circ}C - 85^{\circ}C}{14.7^{\circ}C/W}$$
 = 1.088 W

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

2-4

Revision 0

B.2 DC-DC Converter



FEATURES

- Complete Step-Down Switch Mode Power Supply
- Wide Input Voltage Range: 3.6V to 36V
- 3A Output Current
- 0.8V to 24V Output Voltage
- EN55022 Class B Compliant
- Current Share Multiple LTM8033 Regulators for More Than 3A Output
- Selectable Switching Frequency: 200kHz to 2.4MHz
- Current Mode Control
- SnPb or RoHS Compliant Finish
- Programmable Soft-Start
- Compact Package (11.25mm × 15mm × 4.32mm) Surface Mount LGA and (11.25mm × 15mm × 4.92mm) BGA Packages

APPLICATIONS

- Automotive Battery Regulation
- Power for Portable Products
- Distributed Supply Regulation
- Industrial Supplies
- Wall Transformer Regulation

TYPICAL APPLICATION





EMI Performance

8033fb

TECHNOLOGY

For more information www.linear.com/LTM8033

LTM8033

Ultralow Noise EMC 36V_{IN}, 3A DC/DC µModule Regulator

DESCRIPTION

The LTM®8033 is an electromagnetic compatible (EMC) 36V, 3A DC/DC μ Module® buck converter designed to meet the radiated emissions requirements of EN55022. Conducted emission requirements can be met by adding standard filter components. Included in the package are the switching controller, power switches, inductor, filters and all support components. Operating over an input voltage range of 3.6V to 36V, the LTM8033 supports an output voltage range of 0.8V to 24V, and a switching frequency range of 200kHz to 2.4MHz, each set by a single resistor. Only the bulk input and output filter capacitors are needed to finish the design.

The LTM8033 is packaged in a compact (11.25mm \times 15mm \times 4.32mm) overmolded land grid array (LGA) and ball grid array (BGA) package suitable for automated assembly by standard surface mount equipment. The LTM8033 is available with SnPb (BGA) or RoHS compliant terminal finish.

ABSOLUTE MAXIMUM RATINGS (Note 1)

VIN, FIN, RUN/SS Voltage	36V
ADJ, RT, SHARE Voltage	6V
V _{OUT} , AUX	25V
PGOOD, SYNC	30V

BIAS	25V
Maximum Junction Temperature (Note 2)	125°C
Solder Temperature	245°C

PIN CONFIGURATION



ORDER INFORMATION

		PART MARKING*		PACKAGE	MSI	TEMPERATURE BANGE
PART NUMBER	PAD OR BALL FINISH	DEVICE	FINISH CODE	TYPE	RATING	(Note 2)
LTM8033EV#PBF	Au (RoHS)	LTM8033V	e4	LGA	3	-40°C to 125°C
LTM8033IV#PBF	Au (RoHS)	LTM8033V	e4	LGA	3	-40°C to 125°C
LTM8033MPV#PBF	Au (RoHS)	LTM8033V	e4	LGA	3	-55°C to 125°C
LTM8033EY#PBF	SAC305 (RoHS)	LTM8033Y	e1	BGA	3	-40°C to 125°C
LTM8033IY#PBF	SAC305 (RoHS)	LTM8033Y	e1	BGA	3	-40°C to 125°C
LTM8033IY	SnPb (63/67)	LTM8033Y	eO	BGA	3	-40°C to 125°C
LTM8033MPY#PBF	SAC305 (RoHS)	LTM8033Y	e1	BGA	3	-55°C to 125°C
LTM8033MPY	SnPb (63/67)	LTM8033Y	eO	BGA	3	-55°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

 Terminal Finish Part Marking: www.linear.com/leadfree Recommended LGA and BGA PCB Assembly and Manufacturing

Procedures: www.linear.com/umodule/pcbassembly

 LGA and BGA Package and Tray Drawings: www.linear.com/packaging

2

For more information www.linear.com/LTM8033



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Antimum Input VoltageImm <th>PARAMETER</th> <th>CONDITIONS</th> <th></th> <th>MIN</th> <th>түр</th> <th>ΜΔΧ</th> <th>UNITS</th>	PARAMETER	CONDITIONS		MIN	түр	ΜΔΧ	UNITS
Minimum mut voltageDA < lour < 3A. RADJ Open, Vin < 24V	Minimum Input Voltage			min		3.6	V
Output Do VoltageOA < 1001 < 3A, RAD (John, VIII) < 24VO.3VIIOutput DC Current $V_{IN} = 24V$ 03//Quiescent Current into V _{IN} RUWSS = 0.2V Not Switching0.011//Quiescent Current into BIASRUN/SS = 0.2V Not Switching0.010.011Quiescent Current into BIASRUN/SS = 0.2V Not Switching0.010.5//Quiescent Current into BIASRUN/SS = 0.2V Not Switching0.010.5//Quiescent Current into BIASRUN/SS = 0.2V Not Switching0.010.5//Line Regulation5.5V Not Switching05//Line Regulation0.4 < lour < 3A, VIN = 24V		$0.4 \leq l_{\text{sum}} \leq 2.4 \text{ Bys} \cdot 0.0000 \text{ V/m} = 2.4 \text{ V/m}$			0.0	3.0	v
Output DC Current $V_{IN} = 24V$ 034Quiescent Current into V_{IN} RUN/SS = 0.2V Not Switching0.011 μ/μ 30BIAS = 0/V, Not Switching0.01150 μ/μ Quiescent Current into BIASRUN/SS = 0.2V Not Switching0.010.5 μ/μ Line Regulation5.5V < $V_{IN} < 36V$ 0.3%Load Regulation0 A < lour < 3A, $V_{IN} = 24V$ 0.4%Output RMS Voltage Ripple $V_{IN} = 24V, 0A < lour < 3A$ 5m/wSwitching Frequency $R_T = 45.3k$ 780kHzVoltage at ADJ Pin Φ 2 μ/μ Minimum BIAS Voltage for Proper Operation $RUN/SS = 2.5V$ 510RUN/SS = 2.5V 5 10 μ/μ MUN/SS Pin CurrentRUN/SS = 2.5V510RUN/SS Pin CurrentRUN/SS = 2.5V510RUN/SS Input Liew Voltage0.2VPGOOD Threshold (at ADJ) V_{OUT} Rising730m/WPGOOD Sink CurrentPGOOD = .4V200735 μ/μ SYNC Input Low Threshold $f_{SYNC} = 550$ KHz0.5VSYNC Input High Threshold $f_{SYNC} = 550$ KHz0.7VSYNC Cov0.1 μ/μ GookHz Anrowband Conducted Emissions24V_{IN} 3.3V_{OUT} lour = 3A, 5\mu/H LISN89dBp/MGook Runced Conducted Emissions69dBp/M	Output Do Voltage	$OA < I_{OUT} < SA, R_{ADJ} OPEN, VIN = 24V$ $OA < I_{OUT} < SA, R_{ADJ} = 16.5k, V_{IN} = 32V$			24		v
Quiescent Current into V_{IN} RUN/SS = 0.2V Not Switching0.011 M/A μ/A BIAS = 0V, Not SwitchingQuiescent Current into BIASRUN/SS = 0.2V 	Output DC Current	V _{IN} = 24V		0		3	A
Not Switching BIAS = 0V, Not Switching 30 60 $\mu\mu$ Quiescent Current into BIASRUWSS = 0.2V Not Switching BIAS = 0V, Not Switching 0.01 0.5 $\mu\mu$ Line Regulation $5.5V < V_{IN} < 36V$ 0.3 9% Load Regulation $0A < I_{0UT} < 3A, V_{IN} = 24V$ 0.4 9% Output RMS Voltage Ripple $V_{IN} = 24V, 0A < I_{0UT} < 3A$ 5 mV Voltage tADJ Pin $F_T = 45.3k$ 780 kHz Current Out of ADJ PinADJ = $1V, V_{0UT} = 0V$ 2 $\mu\mu$ RUWSS Input High Voltage 0.25 0.2 0.2 RUWSS Input High Voltage 0.25 0.2 0.2 PGOOD Threshold (at ADJ) V_{0UT} Rising 730 mV PGOOD Sink CurrentPGOOD = $0.4V$ 200 735 $\mu\mu$ SYNC Input Low Threshold $f_{SYNC} = 550 KHz$ 0.5 0.7 V_V SYNC Bias CurrentSYNC = $0V$ 0.1 $\mu\mu$ SOkHz Narrowband Conducted Emissions $24V_{IN}, 3.3V_{0UT}, I_{0UT} = 3A, 5\mu$ 89 $dB\mu$ GokHz Narrowband Conducted Emissions $24V_{IN}, 3.3V_{0UT}, I_{0UT} = 3A, 5\mu$ 69 $dB\mu$	Quiescent Current into VIN	RUN/SS = 0.2V			0.01	1	μA
Bits = 0V, Not Switching100130 μ Quiescent Current into BIASRUN/SS = 0.2V Not Switching0.010.5 μ BIAS = 0V, Not Switching05 μ BIAS = 0V, Not Switching05 μ Line Regulation5.5V < V _{IN} < 36V		Not Switching			30	60	μA
Collected unrent hito birksNot Switching0.3 $\mu \mu$ Not Switching05 $\mu \mu$ BIAS = 0V, Not Switching0.30Line Regulation0.4 < lour	Quiescent Current into PIAS				0.01	0.5	μA
BIAS = 0V, Not Switching05 μ ALine Regulation5.5V < V _{IN} < 36V	Quescent current into biAS	Not Switching			75	120	μΑ μΑ
Line Regulation $5.5V < V_{IN} < 36V$ 0.3 $\%$ Load Regulation $0A < I_{0UT} < 3A, V_{IN} = 24V$ 0.4 $\%$ Output RMS Voltage Ripple $V_{IN} = 24V, 0A < I_{0UT} < 3A$ 5 mVSwitching Frequency $R_T = 45.3k$ 780 kH_2 Voltage at ADJ Pin \bullet 775 790 805 mVCurrent Out of ADJ PinADJ = 1V, V_{OUT} = 0V 2 μA Minimum BIAS Voltage for Proper Operation 2 2.8 V RUN/SS Pin CurrentRUN/SS = 2.5V 5 10 μA RUN/SS Input High Voltage 2.5 V 0.2 V PGODD Threshold (at ADJ) V_{0UT} Rising 730 mV P PGODD Leakage CurrentPGOOD = 0.4V 200 735 μA SYNC Input Low Threshold $f_{SYNC} = 550 KHz$ 0.5 0.7 V SYNC Input Low Threshold $f_{SYNC} = 550 KHz$ 0.7 V 0.7 V SYNC Bias CurrentSYNC = 0V 0.1 μA 0.6 0.7 V SYNC Bias CurrentSYNC = 0V 0.1 μA 0.6 0.7 0.7 0.7		BIAS = 0V, Not Switching			0	5	μΑ
Load Regulation $0A < I_{DUT} < 3A, V_{IN} = 24V$ 0.4 $\%$ Output RMS Voltage Ripple $V_{IN} = 24V, 0A < I_{OUT} < 3A$ 5 mVSwitching Frequency $R_T = 45.3k$ 780 kHzVoltage at ADJ Pin \bullet 775 790 805 mVCurrent Out of ADJ PinADJ = 1V, V _{OUT} = 0V 2 μ AMinimum BIAS Voltage for Proper Operation 2 2.8 V RUN/SS Pin CurrentRUN/SS = 2.5V 5 10 μ ARUN/SS Input High Voltage 2.5 V 0.2 V PGODD Threshold (at ADJ) V_{OUT} Rising 730 mVPGODD Leakage CurrentPGOOD = $30V$, RUN/SS = $0V$ 0.1 1 μ APGODD Sink CurrentPGOOD = $0.4V$ 200 735 μ ASYNC Input Low Threshold $f_{SYNC} = 550$ KHz 0.5 0.7 V SYNC Input High Threshold $f_{SYNC} = 550$ KHz 0.1 μ ASYNC Input Low Threshold $f_{SYNC} = 550$ KHz 0.1 μ ASYNC Input Low Threshold $f_{SYNC} = 50$ KHz 0.7 V SYNC Input Low Threshold $f_{SYNC} = 50$ KHz 0.1 μ ASONKL Narrowband Conducted Emissions $24V_{IN}, 3.3V_{OUT}, I_{OUT} = 3A, 5\mu$ H LISN 89 $dB\mu$ U	Line Regulation	5.5V < V _{IN} < 36V			0.3		%
Output RMS Voltage Ripple $V_{IN} = 24V, 0A < I_{OUT} < 3A$ 5mNSwitching Frequency $R_T = 45.3k$ 780kHzVoltage at ADJ Pin•775790805mNCurrent Out of ADJ PinADJ = 1V, V _{OUT} = 0V2 μA Minimum BIAS Voltage for Proper Operation22.8 V RUN/SS Pin CurrentRUN/SS = 2.5V510 μA RUN/SS Input High Voltage2.5VRUN/SS Input Low Voltage0.2 V PGODD Threshold (at ADJ) V_{OUT} Rising730mVPGODD Leakage CurrentPGOOD = 30V, RUN/SS = 0V0.11 μA PGODD Sink CurrentPGOOD = 0.4V200735 μA SYNC Input Low Threshold $f_{SYNC} = 550$ KHz0.5VVSYNC Input High Threshold $f_{SYNC} = 550$ KHz0.7VSYNC Bias CurrentSYNC = 0V0.1 μA SONKL Narrowband Conducted Emissions24V _{IN} , 3.3V _{OUT} , I _{OUT} = 3A, 5µH LISN89dBpV	Load Regulation	$0A < I_{OUT} < 3A, V_{IN} = 24V$			0.4		%
Switching Frequency R _T = 45.3k 780 kHz Voltage at ADJ Pin • 775 790 805 mV Current Out of ADJ Pin ADJ = 1V, V _{OUT} = 0V 2 µA Minimum BIAS Voltage for Proper Operation 2 2.8 VV RUN/SS Pin Current RUN/SS = 2.5V 5 10 µA RUN/SS Input High Voltage 2.5 VV 0.2 VV RUN/SS Input Low Voltage 0.2 0.2 VV VV PGODD Threshold (at ADJ) V _{OUT} Rising 730 mV PGODD Leakage Current PGODD = 30V, RUN/SS = 0V 0.1 1 µA PGODD Sink Current PGODD = 0.4V 200 735 µA SYNC Input Low Threshold f _{SYNC} = 550kHz 0.5 VV VV SYNC Input High Threshold f _{SYNC} = 550kHz 0.7 VV VV SYNC Input High Threshold f _{SYNC} = 550kHz 0.1 µA PA SOWLA Narrowband Conducted Emissions 24V _{IN} , 3.3V _{OUT} , I _{OUT} = 3A, 5µH LISN 89	Output RMS Voltage Ripple	$V_{IN} = 24V$, $OA < I_{OUT} < 3A$			5		mV
Voltage at ADJ Pin • 775 790 805 mV Current Out of ADJ Pin ADJ = 1V, V _{OUT} = 0V 2 µA Minimum BIAS Voltage for Proper Operation 2 2.8 V RUN/SS Pin Current RUN/SS = 2.5V 5 10 µA RUN/SS Input High Voltage 2.5 V 0.2 V RUN/SS Input Low Voltage 0.2 0.2 V V PGODD Threshold (at ADJ) V _{OUT} Rising 730 mV PGODD Leakage Current PGODD = 30V, RUN/SS = 0V 0.1 1 µA PGODD Leakage Current PGODD = 0.4V 200 735 µA SYNC Input Low Threshold f _{SYNC} = 550kHz 0.5 V V SYNC Input High Threshold f _{SYNC} = 550kHz 0.7 V V SYNC Iss Current SYNC = 0V 0.1 µA 4 SYNC Input High Threshold f _{SYNC} = 550kHz 0.7 V V SYNC Bias Current SYNC = 0V 0.1 µA 4	Switching Frequency	R _T = 45.3k			780		kHz
Current Out of ADJ Pin ADJ = 1V, V _{OUT} = 0V 2 µ/4 Minimum BIAS Voltage for Proper Operation 2 2.8 V RUN/SS Pin Current RUN/SS = 2.5V 5 10 µ/4 RUN/SS Input High Voltage 2.5 V V 0.2 V RUN/SS Input Low Voltage 0.2 V 0.2 V PGODD Threshold (at ADJ) V _{OUT} Rising 730 mV PGODD Leakage Current PGOOD = 30V, RUN/SS = 0V 0.1 1 µ/4 PGODD Sink Current PGODD = 0.4V 200 735 µ/4 SYNC Input Low Threshold f _{SYNC} = 550kHz 0.5 V SYNC Input High Threshold f _{SYNC} = 550kHz 0.7 V SYNC Input High Threshold f _{SYNC} = 0V 0.1 µ/4 SONKIZ Narrowband Conducted Emissions 24V _{IN} , 3.3V _{OUT} , I _{OUT} = 3A, 5µH LISN 89 dBµ/4	Voltage at ADJ Pin		•	775	790	805	mV
Minimum BIAS Voltage for Proper Operation 2 2.8 V RUN/SS Pin Current RUN/SS = 2.5V 5 10 µA RUN/SS Input High Voltage 2.5 V 0.2 V RUN/SS Input Low Voltage 0.2 V 0.2 V PGODD Threshold (at ADJ) V _{OUT} Rising 730 mV PGODD Leakage Current PGOOD = 30V, RUN/SS = 0V 0.1 1 µA PGODD Leakage Current PGODD = 0.4V 200 735 µA SYNC Input Low Threshold f _{SYNC} = 550kHz 0.5 V SYNC Input High Threshold f _{SYNC} = 550kHz 0.7 V SYNC Bias Current SYNC = 0V 0.1 µA 500kHz Narrowband Conducted Emissions 24V _{IN} , 3.3V _{OUT} , I _{OUT} = 3A, 5µH LISN 89 dBµV	Current Out of ADJ Pin	$ADJ = 1V, V_{OUT} = 0V$			2		μA
RUN/SS Pin Current RUN/SS = 2.5V 5 10 µ/k RUN/SS Input High Voltage 2.5 V RUN/SS Input Low Voltage 0.2 V PGODD Threshold (at ADJ) V _{OUT} Rising 730 mV PGODD Threshold (at ADJ) V _{OUT} Rising 730 mV PGODD Leakage Current PGOOD = 30V, RUN/SS = 0V 0.1 1 µ/k PGODD Leakage Current PGOOD = 0.4V 200 735 µ/k SYNC Input Low Threshold f _{SYNC} = 550kHz 0.5 V SYNC Input High Threshold f _{SYNC} = 550kHz 0.7 V SYNC Bias Current SYNC = 0V 0.1 µ/k SONKIZ Narrowband Conducted Emissions 24V _{IN} , 3.3V _{OUT} , I _{OUT} = 3A, 5µH LISN 89 dBµ/V	Minimum BIAS Voltage for Proper Operation				2	2.8	V
RUN/SS Input High Voltage 2.5 V RUN/SS Input Low Voltage 0.2 V PGODD Threshold (at ADJ) V _{OUT} Rising 730 mV PGODD Threshold (at ADJ) V _{OUT} Rising 730 mV PGODD Leakage Current PGODD = 30V, RUN/SS = 0V 0.1 1 µA PGODD Leakage Current PGODD = 0.4V 200 735 µA SYNC Input Low Threshold f _{SYNC} = 550kHz 0.5 V SYNC Input High Threshold f _{SYNC} = 550kHz 0.7 V SYNC Bias Current SYNC = 0V 0.1 µA 500kHz Narrowband Conducted Emissions 24V _{IN} , 3.3V _{OUT} , I _{OUT} = 3A, 5µH LISN 89 dBµV	RUN/SS Pin Current	RUN/SS = 2.5V			5	10	μA
RUN/SS Input Low Voltage 0.2 V PGODD Threshold (at ADJ) V _{OUT} Rising 730 mV PGODD Threshold (at ADJ) V _{OUT} Rising 730 mV PGODD Leakage Current PGODD = 30V, RUN/SS = 0V 0.1 1 µA PGODD Sink Current PGODD = 0.4V 200 735 µA SYNC Input Low Threshold f _{SYNC} = 550kHz 0.5 V SYNC Input High Threshold f _{SYNC} = 550kHz 0.7 V SYNC Bias Current SYNC = 0V 0.1 µA 500kHz Narrowband Conducted Emissions 24V _{IN} , 3.3V _{OUT} , I _{OUT} = 3A, 5µH LISN 89 dBµV	RUN/SS Input High Voltage			2.5			V
PGODD Threshold (at ADJ) V _{OUT} Rising 730 mV PGODD Leakage Current PGODD = 30V, RUN/SS = 0V 0.1 1 μ/k PGODD Leakage Current PGODD = 0.4V 200 735 μ/k PGODD Sink Current PGODD = 0.4V 200 735 μ/k SYNC Input Low Threshold f _{SYNC} = 550kHz 0.5 V SYNC Input High Threshold f _{SYNC} = 550kHz 0.7 V SYNC Bias Current SYNC = 0V 0.1 μ/k SO0kHz Narrowband Conducted Emissions 24V _{IN} , 3.3V _{OUT} , I _{OUT} = 3A, 5μH LISN 89 dBµ/V	RUN/SS Input Low Voltage					0.2	V
PGODD Leakage Current PGODD = 30V, RUN/SS = 0V 0.1 1 µ/k PGODD Sink Current PGODD = 0.4V 200 735 µ/k SYNC Input Low Threshold f _{SYNC} = 550kHz 0.5 V SYNC Input High Threshold f _{SYNC} = 550kHz 0.7 V SYNC Bias Current SYNC = 0V 0.1 µ/k 500kHz Narrowband Conducted Emissions 24V _{IN} , 3.3V _{OUT} , I _{OUT} = 3A, 5µH LISN 89 dBµ/v 69 dBµ/v 69 dBµ/v	PGOOD Threshold (at ADJ)	V _{OUT} Rising			730		mV
PGODD Sink Current PGODD = 0.4V 200 735 μ A SYNC Input Low Threshold f _{SYNC} = 550kHz 0.5 V SYNC Input High Threshold f _{SYNC} = 550kHz 0.7 V SYNC Bias Current SYNC = 0V 0.1 μ A 500kHz Narrowband Conducted Emissions 24V _{IN} , 3.3V _{OUT} , I _{OUT} = 3A, 5µH LISN 89 dBµV 69 dBµV 69 dBµV	PGOOD Leakage Current	PGOOD = 30V, RUN/SS = 0V			0.1	1	μA
SYNC Input Low Threshold f _{SYNC} = 550kHz 0.5 V SYNC Input High Threshold f _{SYNC} = 550kHz 0.7 V SYNC Bias Current SYNC = 0V 0.1 µA 500kHz Narrowband Conducted Emissions 24V _{IN} , 3.3V _{OUT} , I _{OUT} = 3A, 5µH LISN 89 dBµV MHz Narrowband Conducted Emissions 69 dBµV	PGOOD Sink Current	PG00D = 0.4V		200	735		μA
SYNC Input High Threshold f _{SYNC} = 550kHz 0.7 V SYNC Bias Current SYNC = 0V 0.1 µA 500kHz Narrowband Conducted Emissions 24V _{IN} , 3.3V _{OUT} , I _{OUT} = 3A, 5µH LISN 89 dBµV 1MHz Narrowband Conducted Emissions 69 dBµV	SYNC Input Low Threshold	f _{SYNC} = 550kHz		0.5			V
SYNC Bias Current SYNC = 0V 0.1 µ/F 500kHz Narrowband Conducted Emissions 24V _{IN} , 3.3V _{OUT} , I _{OUT} = 3A, 5µH LISN 89 dBµV 1MHz Narrowband Conducted Emissions 69 dBµV	SYNC Input High Threshold	f _{SYNC} = 550kHz				0.7	V
500kHz Narrowband Conducted Emissions 24V _{IN} , 3.3V _{OUT} , I _{OUT} = 3A, 5µH LISN 89 dBµV	SYNC Bias Current	SYNC = 0V			0.1		μA
1MHz Narrowhand Conducted Emissions 69 dR/M	500kHz Narrowband Conducted Emissions	24V _{IN} , 3.3V _{OUT} , I _{OUT} = 3A, 5µH LISN			89		dBµV
10112 10110 Wolard Conducto Emissiono	1MHz Narrowband Conducted Emissions				69		dBµV
3MHz Narrowband Conducted Emissions 51 dBµV	3MHz Narrowband Conducted Emissions	1			51		dBµV

ELECTRICAL CHARACTERISTICS The • denotes the specifications which apply over the full operating

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM8033E is guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8033I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM8033MP is guaranteed to meet specifications over the full –55°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.



For more information www.linear.com/LTM8033



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.





For more information www.linear.com/LTM8033



REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
Α	04/14	Add BGA package option	1, 2, 22, 24
В	09/14	BGA ball A1 was missing, corrected	2
		Changed quiescent current V_{IN} and BIAS from 20 μA and 50 μA to 30 μA and 75 $\mu\text{A},$ respectively	13



Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.



B.3 ADC



12-Bit, 170 MSPS/210 MSPS/250 MSPS, 1.8 V Analog-to-Digital Converter

AD9230

FEATURES

SNR = 64.9 dBFS @ fin up to 70 MHz @ 250 MSPS ENOB of 10.4 @ fin up to 70 MHz @ 250 MSPS (-1.0 dBFS) SFDR = -79 dBc @ f_{IN} up to 70 MHz @ 250 MSPS (-1.0 dBFS) Excellent linearity DNL = ±0.3 LSB typical

INL = ±0.5 LSB typical

LVDS at 250 MSPS (ANSI-644 levels)

700 MHz full power analog bandwidth

On-chip reference, no external decoupling required Integrated input buffer and track-and-hold

Low power dissipation

434 mW @ 250 MSPS—LVDS SDR mode 400 mW @ 250 MSPS—LVDS DDR mode

Programmable input voltage range 1.0 V to 1.5 V, 1.25 V nominal 1.8 V analog and digital supply operation

Selectable output data format (offset binary, twos complement, Gray code)

Clock duty cycle stabilizer

Integrated data capture clock

APPLICATIONS

Wireless and wired broadband communications Cable reverse path **Communications test equipment** Radar and satellite subsystems Power amplifier linearization

GENERAL DESCRIPTION

The AD9230 is a 12-bit monolithic sampling analog-to-digital converter optimized for high performance, low power, and ease of use. The product operates at up to a 250 MSPS conversion rate and is optimized for outstanding dynamic performance in wideband carrier and broadband systems. All necessary functions, including a track-and-hold (T/H) and voltage reference, are included on the chip to provide a complete signal conversion solution.

The ADC requires a 1.8 V analog voltage supply and a differential clock for full performance operation. The digital outputs are LVDS (ANSI-644) compatible and support either twos complement, offset binary format, or Gray code. A data clock output is available for proper output data timing.

Fabricated on an advanced CMOS process, the AD9230 is available in a 56-lead LFCSP, specified over the industrial temperature range (-40°C to +85°C).

Rev. 0 Information furnishe responsibility is assu FIGU. JU Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use, Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. d trademarks are the property of their resp ks and rec



PRODUCT HIGHLIGHTS

- 1. High Performance-Maintains 64.9 dBFS SNR @ 250 MSPS with a 70 MHz input.
- Low Power-Consumes only 434 mW @ 250 MSPS.
- 3. Ease of Use-LVDS output data and output clock signal allow interface to current FPGA technology. The on-chip reference and sample and hold provide flexibility in system design. Use of a single 1.8 V supply simplifies system power supply design.
- Serial Port Control-Standard serial port interface supports various product functions, such as data formatting, disabling the clock duty cycle stabilizer, power-down, gain adjust, and output test pattern generation.
- Pin-Compatible Family-10-bit pin-compatible family 5. offered as AD9211.

 One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.

 Tel: 781.329.4700
 www.analog.com

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AD9230

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
ELECTRICAL	
AVDD to AGND	-0.3 V to +2.0 V
DRVDD to DRGND	-0.3 V to +2.0 V
AGND to DRGND	–0.3 V to +0.3 V
AVDD to DRVDD	-2.0 V to +2.0 V
D0+/D0– through D13+/D13– to DRGND	-0.3 V to DRVDD + 0.3 V
DCO to DRGND	-0.3 V to DRVDD + 0.3 V
OR to DGND	-0.3 V to DRVDD + 0.3 V
CLK+ to AGND	–0.3 V to +3.9 V
CLK- to AGND	–0.3 V to +3.9 V
VIN+ to AGND	-0.3 V to AVDD + 0.2 V
VIN- to AGND	-0.3 V to AVDD + 0.2 V
SDIO/DCS to DGND	-0.3 V to DRVDD + 0.3 V
PDWN to AGND	–0.3 V to +3.9 V
CSB to AGND	–0.3 V to +3.9 V
SCLK/DFS to AGND	–0.3 V to +3.9 V
ENVIRONMENTAL	
Storage Temperature Range	-65°C to +125°C
Operating Temperature Range	-40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 6.

Package Type	θ _{JA}	θις	Unit
56-Lead LFCSP (CP-48-3)	30.4	2.9	°C/W

Typical θ_{JA} and θ_{JC} are specified for a 4-layer board in still air. Airflow increases heat dissipation, effectively reducing θ_{JA} . In addition, metal in direct contact with the package leads from metal traces, and through holes, ground, and power planes reduces the θ_{JA} .

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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AD9230

OUTLINE DIMENSIONS



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9230BCPZ-1701	-40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-56-2
AD9230BCPZ-2101	-40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-56-2
AD9230BCPZ-2501	-40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-56-2
AD9230-170EBZ1		LVDS Evaluation Board with AD9230BCPZ-170	
AD9230-210EBZ1		LVDS Evaluation Board with AD9230BCPZ-210	
AD9230-250EBZ1		LVDS Evaluation Board with AD9230BCPZ-250	

¹ Z = Pb-free part.

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B.4 Thermal Pad





B.5 Cardlock

CALMARK Product Selection Guide

Card-Lo	k								
Product Series	3 or 5 pc.	Actuation	Profile Width (nominal) x Relaxed Height (max)	Profile Height Expanded (min)	Length (min)	Approximate Clamping Force ² N(lbs)	Recommended Torque Setting N-cm (in-lbs)	DSCC	DSCC CID
223	5	Screw	5.72 (.225) x 6.86 (.270)	8.26 (.325)	121.9 (4.80)	tbd	limited		
224	5	Screw	5.33 (.210) x 7.24 (.285)	8.64 (.340)	121.9 (4.80)	tbd	limited		
225	3	Screw	5.72 (.225) x 6.86 (.270)	8.26 (.325)	54.61 (2.15)	489 (110)	68 (6)	84103	59590
E225	3	Screw	5.72 (.225) x 6.86 (.270)	8.26 (.325)	71.12 (2.80)	489 (110)	68 (6)		
L225	3	Lever	5.72 (.225) x 6.86 (.270)	8.26 (.325)	54.61 (2.15)	533 (120)	N/A		
226	5	Screw	5.72 (.225) x 6.86 (.270)	8.26 (.325)	121.92 (4.80)	800 (180)	68 (6)	89064	59789
230	3	Screw	5.59 (.220) x 5.72 (.225)	6.99 (.275)	54.61 (2.15)	489 (110)	68 (6)	84103	59590
231	5	Screw	5.59 (.220) x 5.72 (.225)	6.99 (.275)	121.92 (4.80)	800 (180)	68 (6)	89064	59789
235	3	Screw	5.84 (.230) x 7.32 (.288)	8.64 (.340)	71.12 (2.80)	445 (100)	68 (6)		
236	5	Screw	5.84 (.230) x 7.32 (.288)	8.64 (.340)	147.32 (5.80)	800 (180)	68 (6)		
240	3	Screw	6.10 (.240) x 4.57 (.180)	5.59 (.220)	54.61 (2.15)	489 (110)	68 (6)	84103	59590
245	3	Screw	6.60 (.245) x 6.86 (.270)	8.26 (.325)	54.61 (2.15)	622 (140)	113 (10)		59590
250	3	Screw	9.53 (.375) x 9.78 (.385)	11.94 (.470)	63.50 (2.50)	1111 (250)	227 (20)		59590
255	3	Screw	12.70 (.500) x 11.68 (.460)	15.24 (.600)	54.61 (2.15)	1778 (400)	351 (31)		59590
260	5	Screw	6.35 (.250) x 6.26 (.270)	8.26 (.325)	54.61 (2.15)	1778 (400)	68 (6)	89024	
261	3	Screw	6.35 (.250) x 6.26 (.270)	8.26 (.325)	54.61 (2.15)	667 (150)	68 (6)		59789
L260	5	Lever	6.35 (.250) x 6.26 (.270)	8.26 (.325)	54.61 (2.15)	556 (125)	N/A		59789
LE260	5	Lever	6.35 (.250) x 6.26 (.270)	8.26 (.325)	54.61 (2.15)	556 (125)	N/A		59789
263	5	Screw	6.35 (.250) x 7.44 (.293)	8.89 (.350)	54.61 (2.15)	1778 (400)	68 (6)		
264	3	Screw	6.35 (.250) x 7.44 (.293)	8.89 (.350)	54.61 (2.15)	667 (150)	68 (6)		59789
265	5	Screw	5.72 (.225) x 5.84 (.230)	7.37 (.290)	54.61 (2.15)	1556 (350)	68 (6)		
266	3	Screw	5.72 (.225) x 5.84 (.230)	7.37 (.290)	54.61 (2.15)	600 (135)	68 (6)		
267	5	Screw	6.35 (.250) x 5.00 (.197)	5.99 (.236)	54.61 (2.15)	1556 (350)	68 (6)		
280	5	Screw	9.27 (.365) x 9.65 (.380)	11.68 (.460)	60.96 (2.40)	3334 (750)	227 (20)		59789
281	3	Screw	9.27 (.365) x 9.65 (.380)	11.68 (.460)	60.96 (2.40)	1245 (280)	227 (20)		
						1			

Channel	-Lok						
Product Series	3 or 5 pc.	Actuation	Width x Height (max)	Board Thickness	Length ¹ (min)	Approximate Clamping Force-N (lbs)	Recommended Torque Setting N-cm (in-lbs)
227	3	Screw	12.57 (.495) to 8.89 (.350)	1.14 (.045) to 2.62 (.103)	76.20 (3.00)	489 (110)	68 (6)
228	5	Screw	12.57 (.495) to 8.89 (.350)	1.14 (.045) to 2.62 (.103)	101.6 (4.00)	801 (180)	68 (6)

Retainers & 0	Card Guides					
Product Series	Material	Conductive	Application	Board Thickness	Length ¹ (min)	UL rating
125/126	CR	Yes	Sheet Metal	1.6 (.063) & 2.4 (.094)	31.75 (1.25) to 311.15 (12.25)	N/A
165/166	BeCu	Yes	Sheet Metal	1.6 (.063) & 2.4 (.094)	31.75 (1.25) to 311.15 (12.25)	N/A
NW125/NW126	CR	Yes	Cold Wall	N/A	31.75 (1.25) to 311.15 (12.25)	N/A
NW165/NW166	BeCu	Yes	Cold Wall	N/A	31.75 (1.25) to 311.15 (12.25)	N/A
120	Nylon	No	Sheet Metal	1.6 (.063) & 2.4 (.094)	101.60(4.00),152.40(6.00),177.8(7.00),215.90(8.50),241.30(9.50)	V-2 (V-0 available)
C120	Polycarbonate	Yes	Sheet Metal	1.6 (.063) & 2.4 (.094)	101.60(4.00),152.40(6.00),177.8(7.00),215.90(8.50),241.30(9.50)	V-2 (V-0 available)

Plastic E	xtractors & Inse	erter-Extr	actors			Metal E	xtractor	s & Insert	er-Extracto	ors
Product Series	Material	Function ⁴	Mechanical Advantage	Board Thickness	UL Rating	Product Series	Material	Function ^₄	Mechanical Advantage	Board Thickness
107	Glass-filled Nylon	I & E	4.5:1	1.6 (.063) & 2.4 (.094)	V-0	107-35	AI	I & E	5.5:1	1.6 (.063), 2.4 (.094) & 3.2 (.125)
107-10	Glass-filled Nylon	1 & E	3.3:1	1.6 (.063) & 2.4 (.094)	V-0	107-50	AI	1 & E	4.5:1	1.6 (.063), 2.4 (.094) & 3.2 (.125)
107-20	Glass-filled Nylon	I, E & L	4.5:1	1.6 (.063) & 2.4 (.094)	V-2 (V-0 available)	107-51	AI	I & E	3.3:1	1.6 (.063), 2.4 (.094) & 3.2 (.125)
107-30	Glass-filled Nylon	1 & E	5.5:1	1.6 (.063)	V-0	107.55	A1	105	9.0.1	1.6 (.063), 2.4 (.094) &
107-40-3	Glass-filled Nylon	1.& F	4.5-1	1.6 (.063) &	V-0	10/-55	~	TOLL	0.0.1	3.2 (.125)
107 10 5	ciass mice rigion	142		2.4 to 3.2 (.094 to .125)		107-73	AI	I, E & L	4.2:1	1.6 (.063), 2.4 (.094) &
	Glass-filled Nylon			1.6 (.063),	V-0 (Inserter-					3.2 (.125)
107-70	Latch - Nylon	I, E & L	4.5:1	2.4 (0.94) & 3.2 (.125)	Extractor) V-2 (Latch)	107-75	AI	I, E & L	7.0:1	1.6 (.063), 2.4 (.094) & 3.2 (.125)
						109	Al or CR	E	4.5:1	1.6 (.063), 2.4 (.094) & 3.2 (.125)

1-Other assembly lengths available upon request. 2-Clamping forces based on Chemical Film Option – Other finishes and options will yield different results 3-101 available in 1.6 (.063) only 4-Function: E=Extract 1=Insert 1=Latch or Lock 5-Dinits are metic (inch)

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CALMARK Series 265 - "Card-Lok" Retainer (Cold Plate)



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Series 265 - "Card-Lok" Retainer (Cold Plate) CALMARK 4.57 (.180) **OPTION PREFIX** × 5.8 (.23) Detail "V" 1 REF 1 (227) Provides visual lock indication. OPTION SUFFIX Detail "L" Detail "L" Provides prevailing torque for resistance to lossening from shock and vibration. Adds 22 N-cm (2 in-lbs) torque to assembly. See application data on previous sheet. Detail "K" Prevents the unintentional disassem-bly of screw from front wedge. Lock element per MIL-F-18240 applied to thread of screw 2.38 (.094) Hex Socket Cap Per ANSI/ ASME B18.3 Center hole location "E" option only M2 ±.13(.005) → Ó E O 5.84 (.230) max. M = Assembly Length 48.26 (1.90) ± .13 (.005) - 4.6 (.18) REF 20.32 (.800) - 7.6 (.30) max 7.37 (.290) min H O -Units: mm (in.) Unless otherwise specified $xx \pm .25$, $x \pm .5$ ($xxx \pm .010$, $xx \pm .02$) Note: Each piece has a toler specified: of ± .010 lard. Extr added with "E" option Part Number Code Example: Part Number Code Series 265 Card-Lok Five Piece M265-4.80H <u>3.80</u> E H L K Series 265 Card-Lok five piece 121.9 (4.80) long with M2.5 hex drive, gold chemical M V A 265 -Prefix options film finish and standard rivet hole mounting Metric Screw Head M2.5 Hex Drive _____ Standard Screw Head 3/32 Hex Drive ____ [blank] FINISH TABLE Code Visual Indicator _____ No Visual Indicator _ [blank] <u>Letter</u> Finish No Visual Indicator ______ Black Anodize _____ or choose from Finish Table __ Chemical Film per Mil-DTL-5541 Class 1A, Type 1, Gold [blank] see table Chemical Film per Mil-DTL-5541 Class 3, Type II, Clear Black Anodize per Mil-A-8625 Type II, Class 2 "R" Suffix options Assembly length in inches. Standard lengths range from 71.12 (280), 96.52 (3.80) and 121.9 (4.80). Other lengths available upon request Additional Center Mounting Hole "A" "HA" "EN" length.xx

[blank]

H see table

[blank]

[blank]

Code

"H"

None

None_____ Captive Screw None _____

Mounting Options - through mounting holes_ or choose from Mounting Option Table _____ Lock Element _____ None

Hard Black Anodize per Mil-A-8625 Type III, Class 2 Electroless Nickel per Mil-C-26074 Class 4, Grade B, Bright MOUNTING METHOD TABLE Letter Method

Ø1.73/1.85 (.068/.073) dia. through holes countersink 100° X 1.52 (.060) deep 0-80 tapped hole "T0" "T2" "TM2" "TM2.5" 2-56 tapped hole M2 x 0.40 tapped hole M2.5 x 0.45 tapped hole

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CALMARK^{*} Clamping Force Data - Card-Loks

The clamping outputs indicated in the table below are the results of averaged data. Within each series numerous Card-Loks of various lengths, finishes, and configurations were cycle tested. The accumulated data verified the following:

- Clamping output is not dependent on length
- Clamping output is greatly affected by choice of finish
- Clamping output is greatly improved when washers are used

Customized Card-Lok variations for specific applications are available on request

		Torque		Clampin	g Force	
Series	Screw	Setting N-cm (in-lbs)	Chem Film Finish N (lbs)	Chem Film Finish With Washers N (lbs)	Black Anodize N (lbs)	Black Anodize With Washers N (Ibs)
223	4-40	N/A	Consult factory	Consult factory	Consult factory	Consult factory
224	4-40	N/A	Consult factory	Consult factory	Consult factory	Consult factory
225	4-40	68 (6)	445 (100)	778 (175)	1223 (275)	1423 (320)
E225	4-40	68 (6)	445 (100)	778 (175)	1223 (275)	1423 (320)
L225	4-40	N/A	N/A	N/A	533 (120)	N/A
226	4-40	68 (6)	801 (180)	1402 (315)	2224 (500)	2755 (615)
227	4-40	68 (6)	N/A	778 (175)	N/A	1423 (320)
228	4-40	68 (6)	N/A	1402 (315)	N/A	2775 (615)
230	4-40	68 (6)	489 (110)	890 (200)	3334 (300)	1512 (340)
231	4-40	68 (6)	801 (180)	1402 (315)	2224 (500)	2755 (615)
235	M3	68 (6)	445 (100)	N/A	1223 (275)	N/A
236	M3	68 (6)	801 (150)	N/A	2224 (500)	N/A
240	4-40	68 (6)	489 (110)	623 (140)	1446 (325)	1490 (335)
245	6-32	110 (10)	623 (140)	1023 (230)	1779 (400)	1779 (400)
250	8-32	220 (20)	1112 (250)	1779 (400)	2958 (665)	3114 (700)
255	10-32	350 (31)	1779 (400)	2669 (600)	3336 (750)	3670 (825)
260	4-40	68 (6)	N/A	1779 (400)	N/A	2224 (500)
261	4-40	68 (6)	N/A	667 (150)	N/A	1223 (275)
L260	4-40	N/A	N/A	N/A	556 (125)*	N/A
LE260	4-40	N/A	N/A	N/A	556 (125)*	N/A
263	4-40	68 (6)	N/A	1779 (400)	N/A	2224 (500)
264	4-40	68 (6)	N/A	667 (150)	N/A	1223 (275)
265	4-40	68 (6)	N/A	1557 (350)	N/A	2113 (475)
266	4-40	68 (6)	N/A	600 (135)	N/A	801 (180)
267	4-40	68 (6)	N/A	1557 (350)	N/A	2113 (475)
280	8-32	220 (20)	N/A	3336 (750)	N/A	4003 (900)
281	8-32	220 (20)	N/A	1245 (280)	N/A	2224 (500)

* Finish is dry film lube over black anodize

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Thermal Resistance - Card-Loks CALMARK

Testing performed by numerous users of Calmark's Series 225 and similar size Card-Loks (approx. 6.35 [.25] high) has shown that the thermal resistance across the interface of a card which is clamped to a cold plate will usually fall within the range of 2° to 4° C inch/watt. Three piece Card-Loks of shorter lengths will usually provide results close to the 2, while longer Card-Loks (over 6 inches) may fall closer to the 4. These thermal resistance numbers apply when testing is performed at or near sea level. When the same testing is performed at high altitude or near vacuum conditions the results can be significantly affected. Increases of from 10 to 40 percent would not be unusual, especially with the longer three piece Card-Loks.

Five piece Card-Loks, such as the Series 260 or 265, with their greater and more evenly distributed clamping force, will greatly reduce these potential gradients.

. The following chart provides an easy method of estimating the temperature rise across the interface (junction) of the card and cold plate when thermal conductivity is the only means of heat transfer considered (heat loss due to radiation and convection minimized).



Example: A card using a pair of 127mm (5.00 inch) long Card-Loks is clamped to a pair of cold plates and is dissipating 50 watts of power: Total length of Card-Loks is 254 (10), [127 (5) x 2] Junction resistance is shown as between 0.2° and 0.4°C/W

Therefore, at their junction, card temperature will rise between 10° and 20°C above the cold plate. [0.2°C/W x 50(W) = 10°C]

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B.6 SUVA 410A

General Toperty	, information, but one	5444 4070, Dui 0		
Physical Property	Unit	Suva [®] 407C (R-407C)	Suva [⊛] 410A (R-410A)	HCFC-22
Molecular Weight, avg.	g/mol	86.20	72.58	86.47
Vapor Pressure at	kPa abs	1174.1	1652.9	1043.1
25°C (77°F)	psia	170.29	239.73	151.40
Boiling Point (1 atm)	°C	-43.56	-51.53	-40.80
	°F	-46.40	-60.76	-41.40
Critical Temperature	°C	86.74	72.13	96.24
	°F	188.13	161.83	205.24
Critical Pressure	kPa abs	4619.10	4926.1	4980.71
	psia	669.95	714.5	722.39
Critical Density	kg/m³	527.30	488.90	524.21
	Ib/ft³	32.92	30.52	32.73
Liquid Density at	kg/m³	1134.0	1062.4	1194.68
25°C (77°F)	Ib/ft³	70.80	66.32	74.53
Density, Satd. Vapor at 25°C (77°F)	kg/m³	41.98	65.92	44.21
	Ib/ft³	2.62	4.12	2.76
Specific Heat, Liquid at 25°C (77°F)	kJ/kg⋅K	1.54	1.84	1.24
	Btu/lb⊦°F	0.367	0.440	0.296
Specific Heat, Vapor at 25°C (77°F) (1 atm)	kJ/kg∙K	0.830	0.832	0.685
	Btu/lb⊦°F	0.198	0.199	0.157
Vapor Pressure of Satd.	kPa abs	1173.4	1652.9	1043.1
Liquid at 25°C (77°F)	psia	170.3	239.73	151.4
Heat of Vaporization	kJ/kg	245.1	276.2	233.5
at Normal Boiling Point	Btu/Ib	105.4	118.8	100.4
Thermal Conductivity at 25°C (77°F)	\A// 1/	0.0010	0.000/	0.0040
Liquia	W/m⋅ĸ Btu/hr⋅ft⋅°F	0.0819	0.0886	0.0849
Vapor (1 atm)	W/m⋅K	0.01314	0.01339	0.01074
	Btu/hr⋅ft⋅°F	0.00758	0.00772	0.00621
Viscosity at 25°C (77°F) Liquid Vapor (1 atm)	Pa∙s Pa∙s	$\begin{array}{c} 1.60 \times 10^{-4} \\ 1.23 \times 10^{-5} \end{array}$	$1.20 imes 10^{-4}$ $1.27 imes 10^{-5}$	1.59×10^{-4} 1.30×10^{-5}
Flammability Limit in Air (1	atm) vol%	none	none	none
Ozone Depletion Potential	CFC-11 = 1.0	0	0	0.05
Halocarbon Global Warming Potential	CFC-11 = 1.0	0.38	0.46	0.34
Global Warming Potential	CO ₂ = 1.0 (100-yr ITH)	1600	1890	1700
TSCA Inventory Status	Included	yes	yes	yes
Inhalation Exposure Limit*	ppm (8- and 12-hr TWA)	1000	1000	1000

	Table 3	
General Property Infor	mation, DuPont™ Suva® 407C, D	DuPont [™] Suva [®] 410A, and HCFC-22

* The exposure limit is calculated based on the DuPont Acceptable Exposure Limit (AEL) for each component of the refrigerant blend. AEL is an airborne exposure limit established by DuPont that specifies time-weighted average concentrations to which nearly all workers may be repeatedly exposed without adverse effects during an 8- or 12-hr workday and a 40-hr work week.



Figure 4. Pressure-Enthalpy Diagram for DuPont[™] Suva[®] 410A (SI Units)

Appendix C Calculations

Potenza	×	M	160	5,000			•				
Densità vapore	٩_v	kg/m^3	65,92	100 4,000							
Densità liquido	٩- ١-	kg/m^3	1062,4	а 3,000							
Calore specifico	U	J/kg K	1840	,000 5 Snue							
Viscosità vapore	μ_V	Pa s	1,27E-05	برة 1,000							
Viscosità liquido	Ę	Pa s	1,20E-04	0,000	,						
Conducibilità termica	<u>×</u>	W/m K	0,0886		0T'0 50'0 00'0	57'0 07'0 51'0	0*'0 55'0				
Prandtl	Pr	/	2,492))	Quality))				
Potenza per Board	M	N	16								
Salto entalpico	Δh kJ/kg		5,992	10,521	15,051	19,580	24,109	28,638	33,167	37,696	42,225
Diametro int	Q	ε	4,00E-03								
Portata	ŋ	m^3/s	2,51E-05	4,41E-05	6,31E-05	8,21E-05	1,01E-04	1,20E-04	1,39E-04	1,58E-04	1,77E-04
Portata massica	Σ	kg/s	0,02670								
Velocità	>	m/s	2,00	3,51	5,02	6,53	8,05	9,56	11,07	12,58	14,09
Reynolds	Re		70827								
Nusselt	Nu		235,91								
Film coefficient	ч	W/m K	5225								
Lunghezza condotto	_	ε	0,25								
Salto termico nel film	ΔT	×	3,1								
quality	×		0,00	0,05	0,10	0,15	0,20	0,25	0,30	0,35	0,40
density two phase	P_tp	kg/m^3	1062	605	423	325	264	222	192	169	151
viscosity two phase	μ_tp	Pa s	1,20E-04	8,44E-05	6,50E-05	5,29E-05	4,46E-05	3,86E-05	3,39E-05	3,03E-05	2,74E-05
Reynolds two phase	Re_tp		70827	100747	130667	160587	190507	220427	250347	280267	310187
Fannor two phase	f_tp		0,00484	0,00443	0,00416	0,00395	0,00378	0,00365	0,00353	0,00343	0,00335
Pressure drop per length	ΔP/L	Pa/m	2572	4136	5544	6850	8081	9256	10384	11474	12530
number of crate	#crate		1	1	1	1	1	1	1	1	1
Length of the pipe	_		7,00	7,00	7,00	7,00	7,00	7,00	7,00	7,00	7,00
Distribuited pressure drop	ΔP_distr	bar	0,018	0,029	0,039	0,048	0,057	0,065	0,073	0,080	0,088
concentrated coeff	×		1,4	1,4	1,4	1,4	1,4	1,4	1,4	1,4	1,4
number of concentration	# k /cr		22	22	22	22	22	22	22	22	22
Concentrated pressure drop	ΔP_conc	bar	0,654	1,149	1,644	2,138	2,633	3,128	3,622	4,117	4,612