



ATLAS

THE UNIVERSITY OF CHICAGO



FTK

Fast Track Trigger for ATLAS

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FTK purposes overview

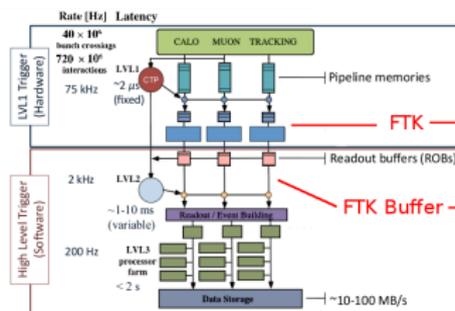
The motivation: precise SM & BSM measurements

- ▶ event selection with large number of **pile-up** events



- ▶ calorimetry isolation not sufficient at higher luminosity

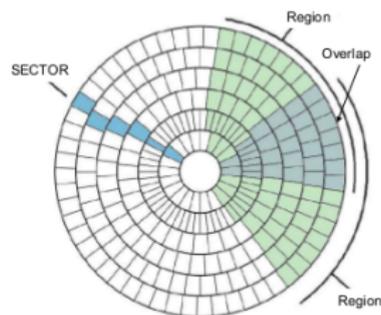
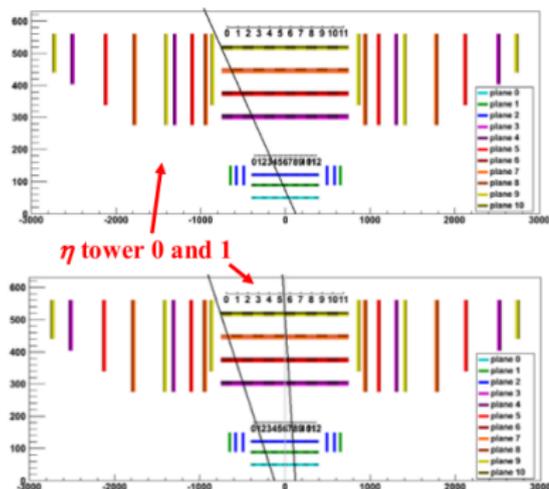
⇒ use tracking information to select particles from primary vertex



FTK is an highly parallel tracking system:

- ▶ global tracking in the ATLAS silicon detector: $p_T > 1 \text{ GeV}$
- ▶ use full LVL1 trigger output rate → high quality tracks for HLT

FTK architecture overview



- ▶ inner detector structure mapped in 64 overlapping η - ϕ towers
- ▶ 1 tower: Data Formatter DF + 2 parallel processing units \rightarrow 2x (AM board + AUX board)
- ▶ DF: hits clustering + data mapping in 11 logical layers

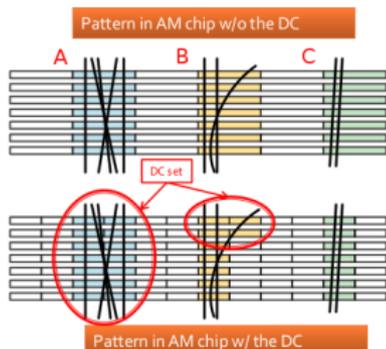
Don't Care feature

The AM chip can use 2 precisions at the same time, balancing the effect:

- ▶ fine resolution patterns (**TSP patterns**) \Rightarrow lower fake rate but more AM space required
- ▶ coarse resolution patterns (**AM patterns**) \Rightarrow less AM space required but greater output bandwidth



- ▶ TSP patterns generated and grouped in AM patterns \Rightarrow **tree structure**



DC allows to change the SS resolution in a dynamic way:

- ▶ **A**: wide roads save pattern space;
- ▶ **B,C**: reduce fake using narrower SSs in some or all layers

Multiple DC bits AM bank configurations

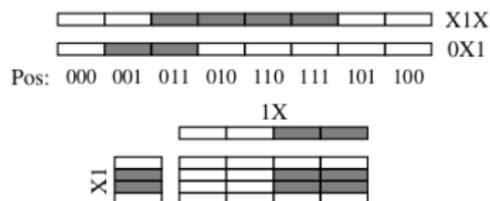
AM bank generation from TSP bank (fine resolution patterns bank):

- ▶ ΔSS_{TSP} = SS size for TSP bank = maximum precision
- ▶ $\Delta SS_{AM} = \Delta SS_{TSP} \times 2^{N_{DC}} =$ SS size for AM bank
- ▶ N_{DC} = number of DC bits = number of TSP SSs in one AM SSs

⇒ TSP bank configurations: 24x20x36 & 15x16x36

- ▶ 24x36 (15x36) = 2-dim pixel superstrip dimension in number of silicon channels
- ▶ 20 (16) = 1-dim SCT superstrip dimension

(position bits encoded with Gray Code) →



⇒ AM bank configurations: $(N_{DC}(pixel_X), N_{DC}(pixel_Y), N_{DC}(SCT))$

- ▶ (1,0) - 1
- ▶ (0,1) - 1
- ▶ (1,1) - 1
- ▶ (1,2) - 1
- ▶ (2,1) - 1
- ▶ (1,0) - 2
- ▶ (0,1) - 2
- ▶ (1,1) - 2
- ▶ (1,2) - 2
- ▶ (2,1) - 2

Multiple DC bits study - datasets

► **Efficiency** study:

⇒ 100k single muon events

► **AM size + Efficiency** study:

TSP = 24x20x36

⇒ 1500 $Z \rightarrow \mu\mu$ events

⇒ 46 pileup events

⇒ $\sqrt{s} = 14$ TeV, luminosity 2×10^{34}

TSP = 15x16x36

⇒ 1500 WH events

⇒ 71 pileup events

⇒ $\sqrt{s} = 14$ TeV, luminosity 3×10^{34}

⇒ 7 Layer architecture

⇒ 8 $\eta - \phi$ overlapping regions → 1 region considered: barrel only

⇒ 16 sub-regions per each region

⇒ 8 Layer architecture

⇒ 64 $\eta - \phi$ overlapping towers → 12 regions considered: (barrel + endcap)

⇒ 4 sub-regions per each region

Hardware constraints

- ▶ **#AM patterns**: capacity of the AM board
 - 2 AM boards per tower
 - 4 LAMB per AM board
 - 32 AM chips per LAMB
 - 80k patterns per chip

⇒ **20.48M AM patterns per tower**
- ▶ **#Roads**: output rate towards AUX card
 - 1 AM board connected with the AUX card with 16 links 2 Gbps
 - maximum rate: 500 roads/event per link
 - maximum rate: 8 kroads/event per board

⇒ **16 kroads/event per tower**
- ▶ **#Fits**: average number of fits sustainable by the TF
 - goal: 1 track in 1 ns
 - time to fit 10000 combinations per TF
 - 40 kfits/board

⇒ **80 kfits per tower**

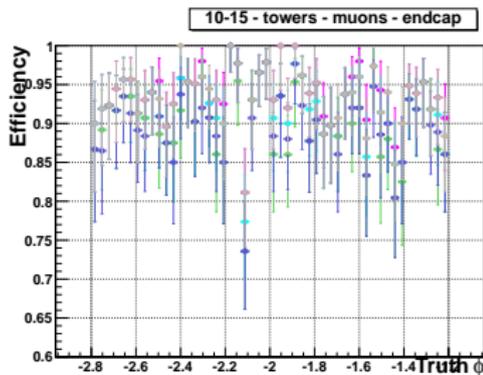
Color Legend

- ▶ **magenta** → 30xDC_SCTx144 → (1,2) - DC_SCT
- ▶ **lightgray** → 60xDC_SCTx72 → (2,1) - DC_SCT
- ▶ **cyan** → 30xDC_SCTx72 → (1,1) - DC_SCT
- ▶ **green** → 30xDC_SCTx36 → (1,0) - DC_SCT
- ▶ **blue** → 15xDC_SCTx36 → (0,1) - DC_SCT

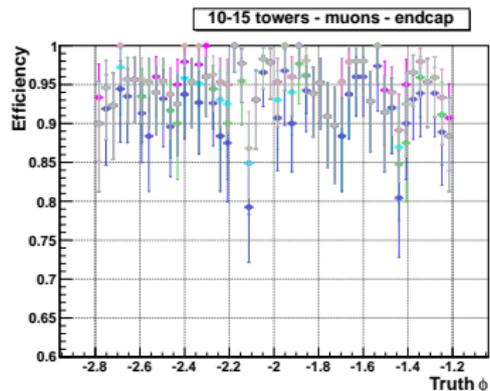
Efficiency vs ϕ - single μ - endcap & barrel

Endcap

1 DC bits SCT

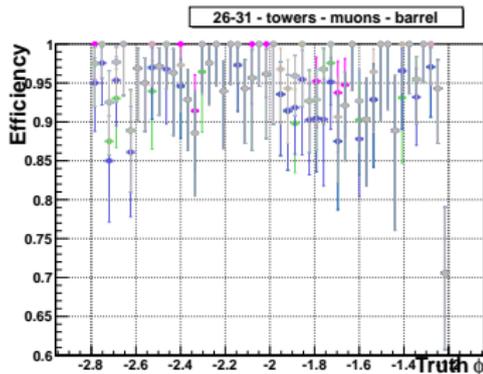


2 DC bits SCT

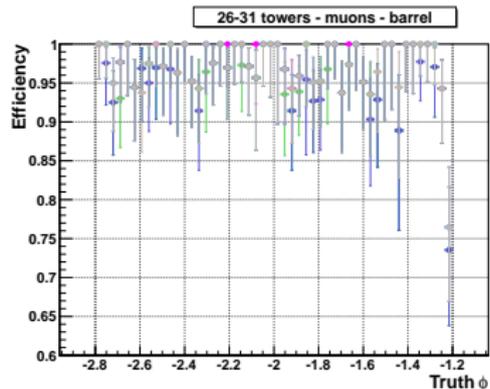


Barrel

1 DC bits SCT



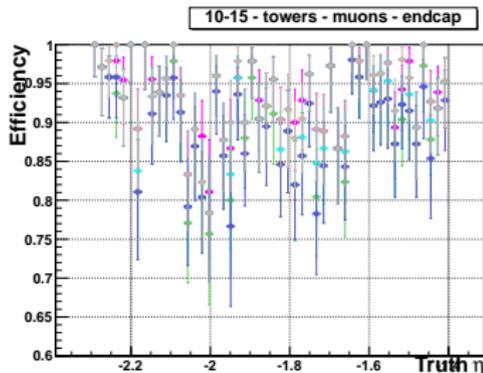
2 DC bits SCT



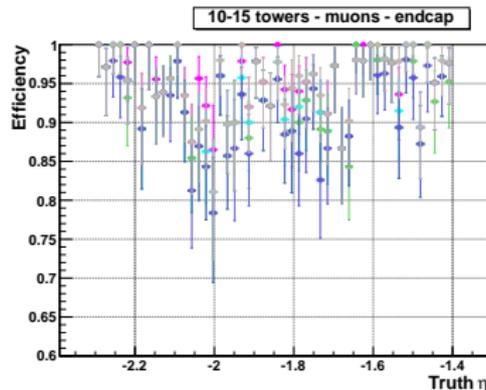
Efficiency vs η - single μ - endcap & barrel

Endcap

1 DC bits SCT

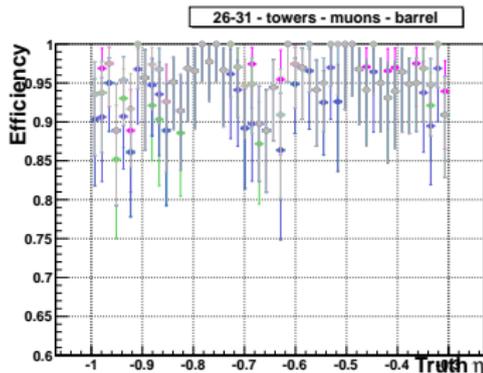


2 DC bits SCT

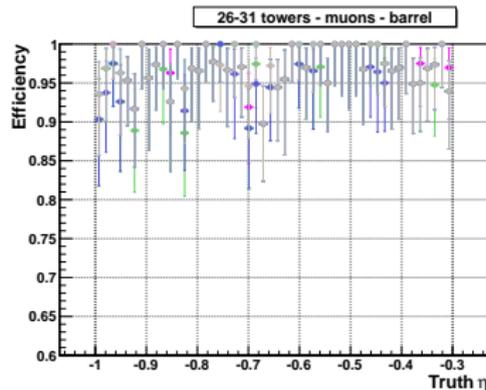


Barrel

1 DC bits SCT



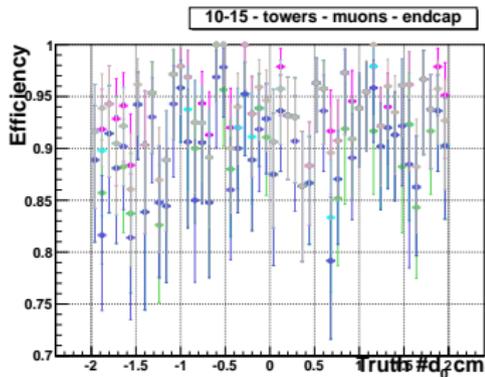
2 DC bits SCT



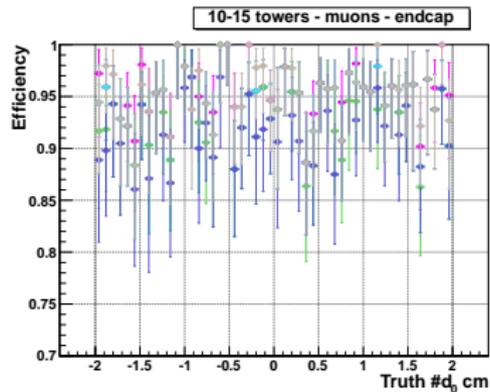
Efficiency vs d_0 - single μ - endcap & barrel

Endcap

1 DC bits SCT

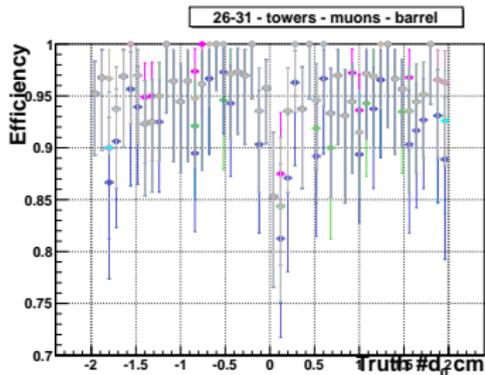


2 DC bits SCT

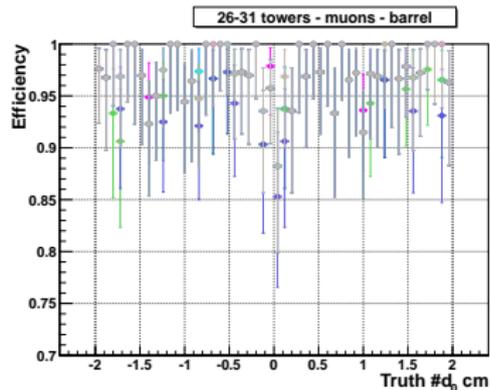


Barrel

1 DC bits SCT



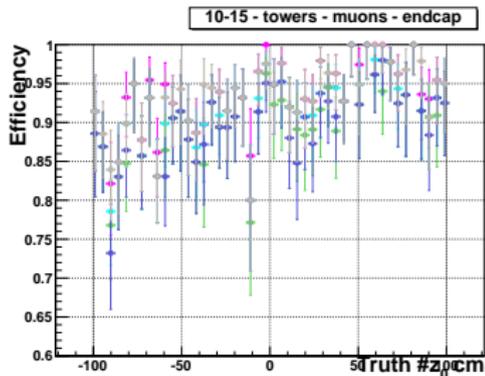
2 DC bits SCT



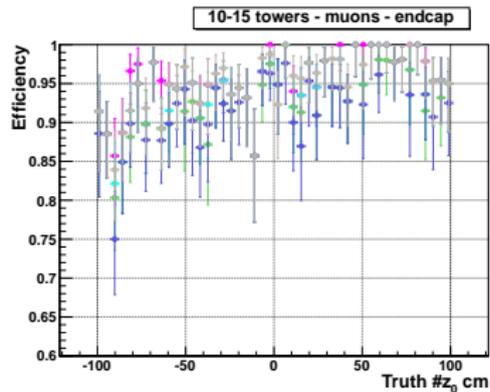
Efficiency vs z_0 - single μ - endcap & barrel

Endcap

1 DC bits SCT

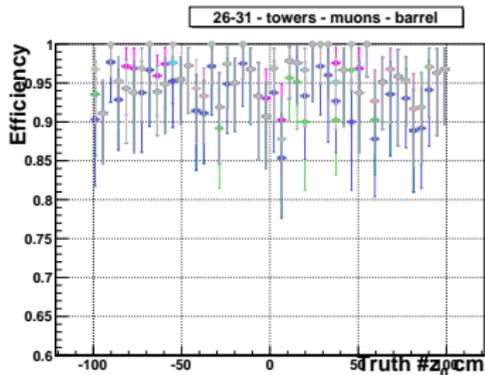


2 DC bits SCT

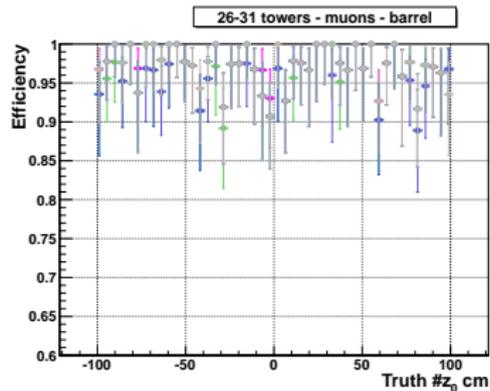


Barrel

1 DC bits SCT



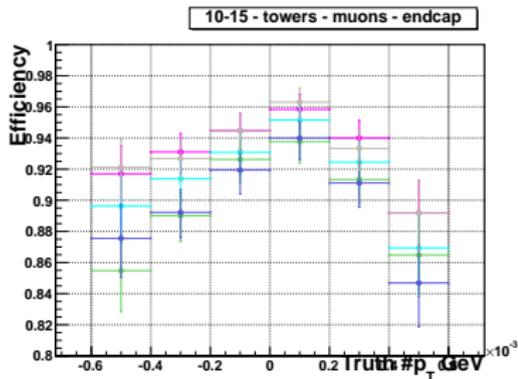
2 DC bits SCT



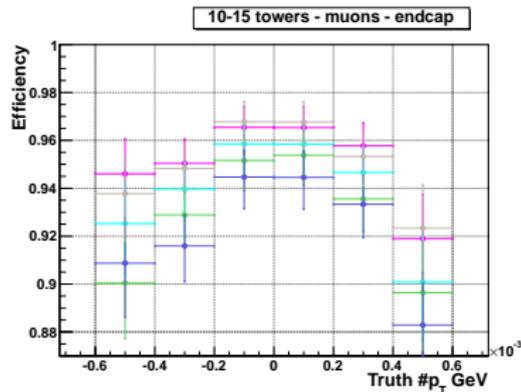
Efficiency vs p_T - single μ - endcap & barrel

Endcap

1 DC bits SCT

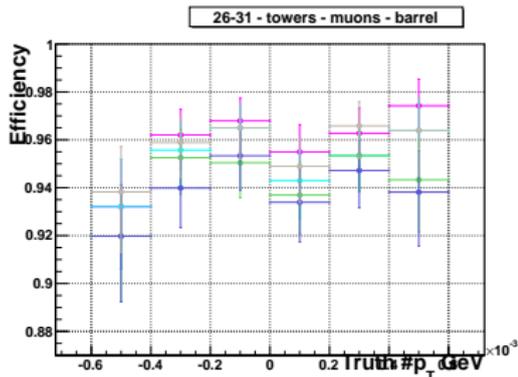


2 DC bits SCT

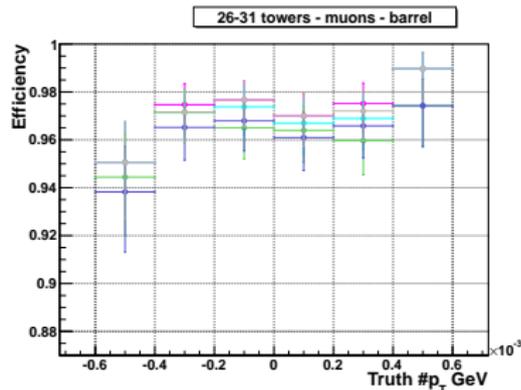


Barrel

1 DC bits SCT



2 DC bits SCT



Results with 8 layers geometry in 26-31 towers - barrel

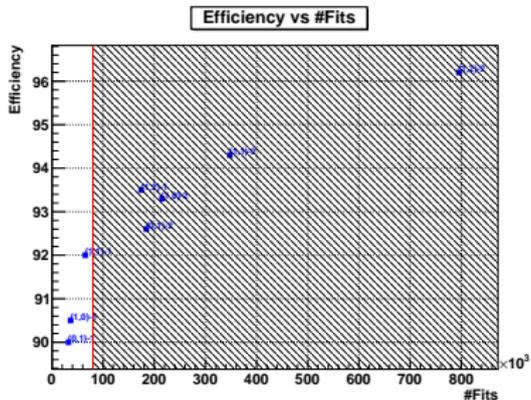
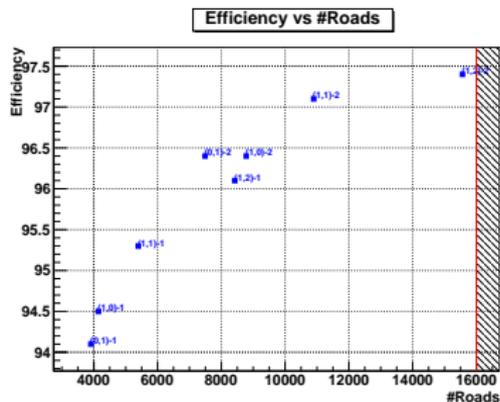
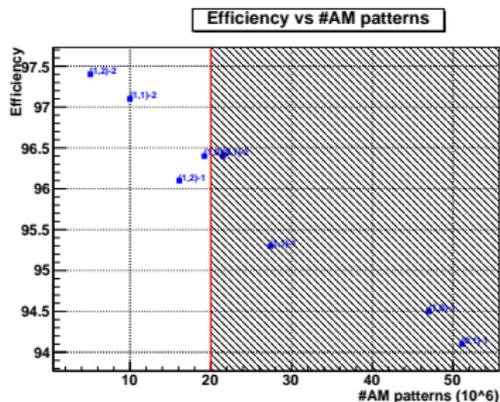
26-31 towers:

DC bits	# TSP .10 ⁶	# AM .10 ⁶	Efficiency	$\langle N \rangle$ Roads/evt	$\langle N \rangle$ Fits/evt .10 ³	$\langle N \rangle$ Tracks/evt
(0,1)-1	120	51	94.1 %	3909	22	50
(1,0)-1	120	47	94.5 %	4147	25	51
(1,1)-1	120	27	95.3 %	5395	47	53
(1,2)-1	120	16	96.1 %	8423	150	57
(2,1)-1	120	16	95.8 %	6783	116	48
(0,1)-2	120	21	96.4 %	7490	87	55
(1,0)-2	120	19	96.4 %	8781	118	57
(1,1)-2	120	10	97.1 %	10898	208	56
(1,2)-2	120	5	97.4 %	15562	585	59
(2,1)-2	120	5	97.25 %

- #AM patterns, #Tracks, Roads and Fits evaluated only in tower 26

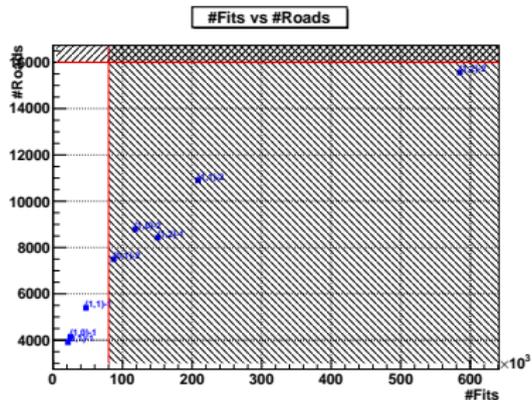
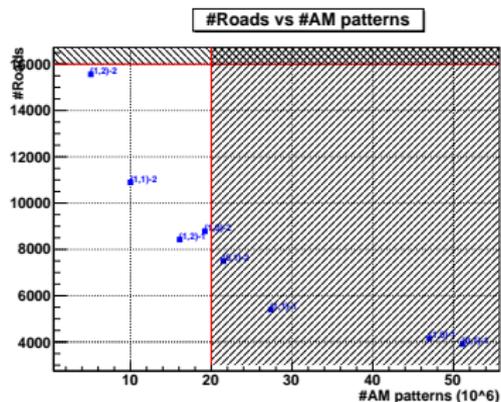
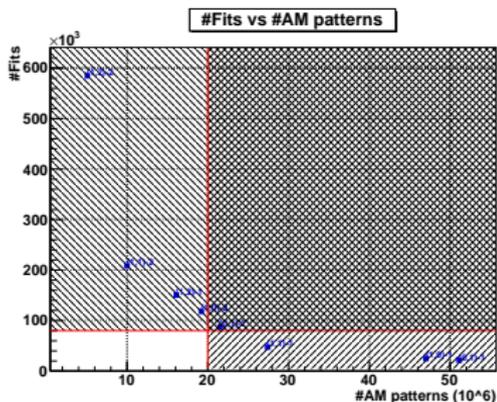
Results with 8 layers geometry - AM bank comparison

Barrel - towers 26 → 31:



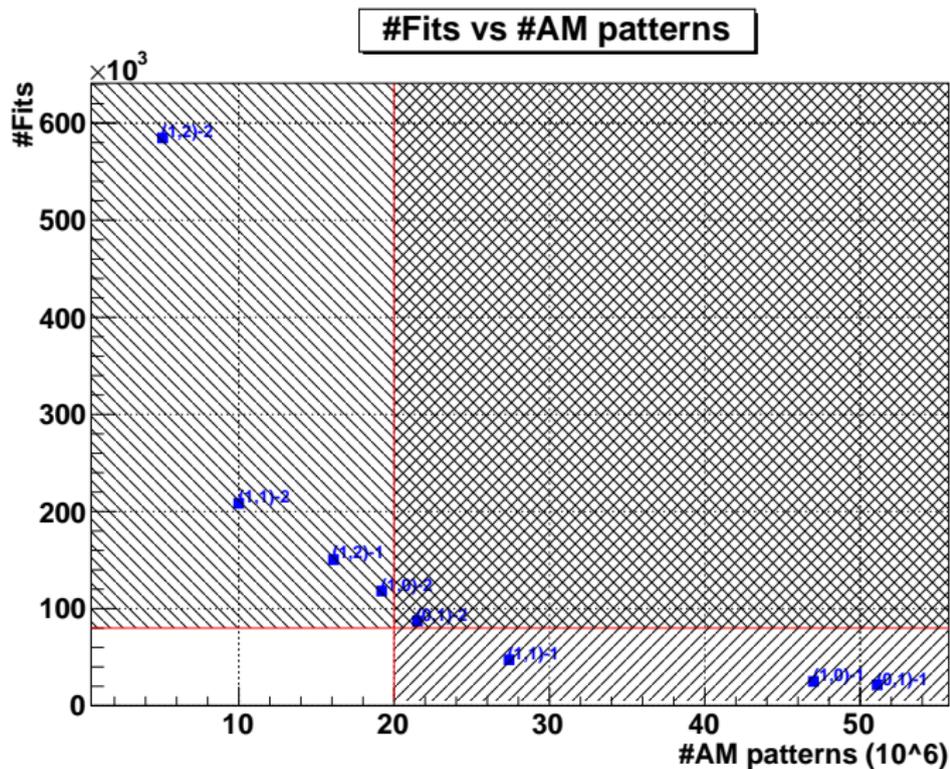
Results with 8 layers geometry - AM bank comparison

Barrel - towers 26 \rightarrow 31:



Results with 8 layers geometry - AM bank comparison

Barrel - towers 26 → 31:



Constraining #AM patterns

⇒ #AM patterns per tower = 20×10^6

Barrel:

- ▶ ↑ Efficiency = 95.3 % ⇒ 95.0 %
- ▶ ↓ #Fits = 47×10^3 ⇒ 38×10^3
- ▶ ↓ #Roads/event = 5395 ⇒ 4415
- ▶ ↓ #AM patterns = 27×10^6 ⇒ 20×10^6
(5M AM patterns per sub-region)

⇒ AM bank with DC configuration (1,1) - 1 within the acceptable region

Results with 8 layers geometry - #AM patterns constrained

Barrel - towers 26 \rightarrow 31:

