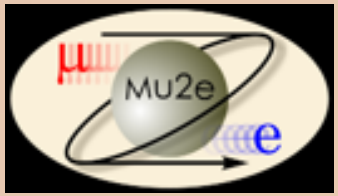


FPGA-BASED DIGITIZER FOR MU2E

September 24, 2014 : Final Review

Summer Student : Martina Benvenuti

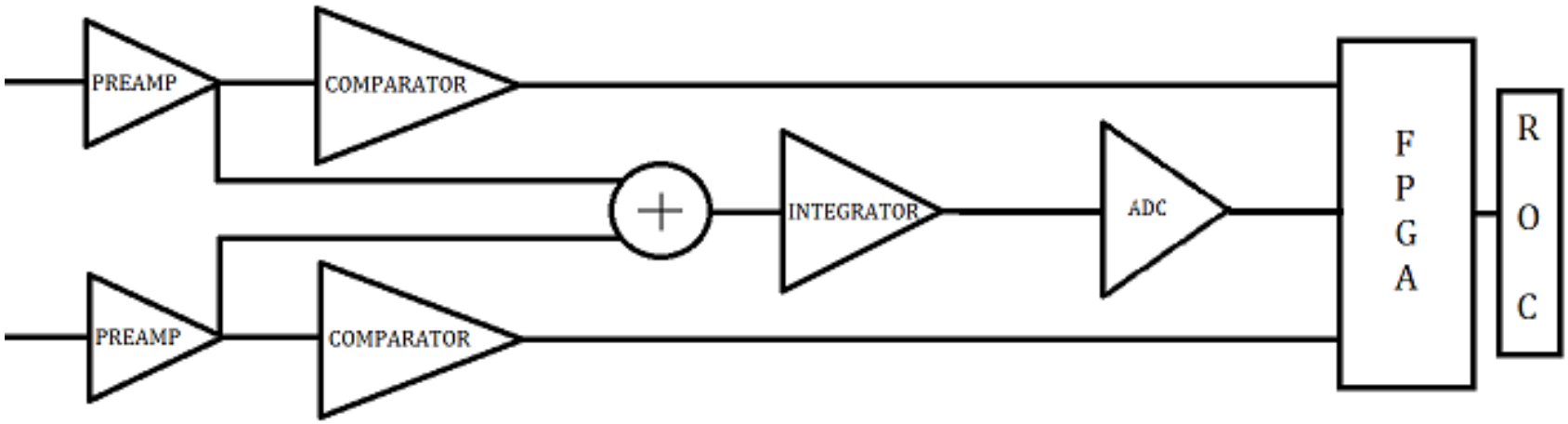
Supervisor: Vadim Rusu

OUTLINE

- Introduction : Starting From The Mid Term Review
- New Goals
- Simplify The TDC Channel
- Modified Design To Be Debugged And Fitted In The FPGA
- New Logic Design : Fitting And Testing
- What Is Left, Acknowledgements

THE WHOLE SYSTEM

Data Acquisition System



NEXT STEPS

- ✓ Write a C script to get future changes easier to be tested;
- ✓ Post Layout Simulation to include paracitic delays and see how the system is really working;
- ✓ Modify the TDC channel bundle to make it smarter and simplier;
- ✓ Achieve the best performance on the Altera FPGA and then move and fit the new design into the Microsemi IGLOO2.

GOALS

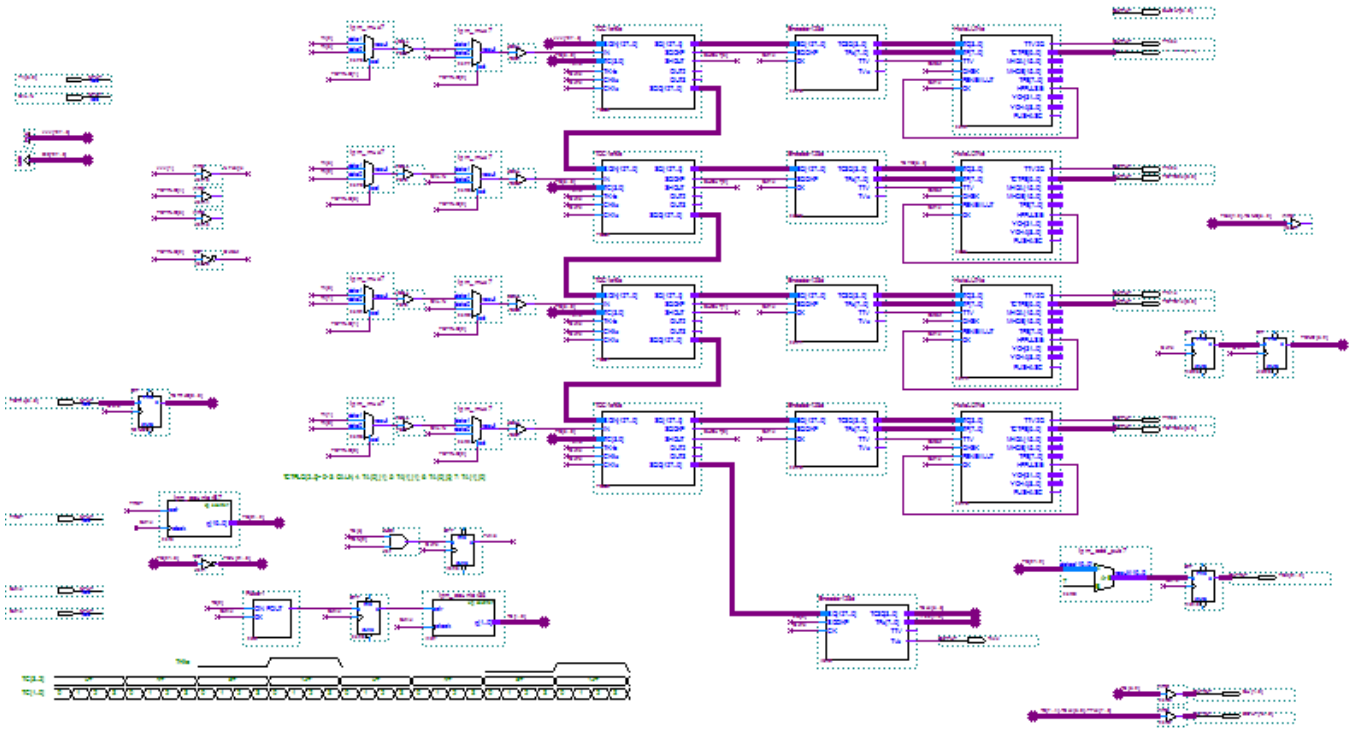
What Had To Be Done/ I Have Done

- Simplify The TDC Channel
- Modify The Hardware And Create New Entities
- Try To Fit The Design
- Join Gabriele's Logic For The FER Entity
- Try To Fit The New/Definitive Design

TDC CHANNEL

Old Stuff

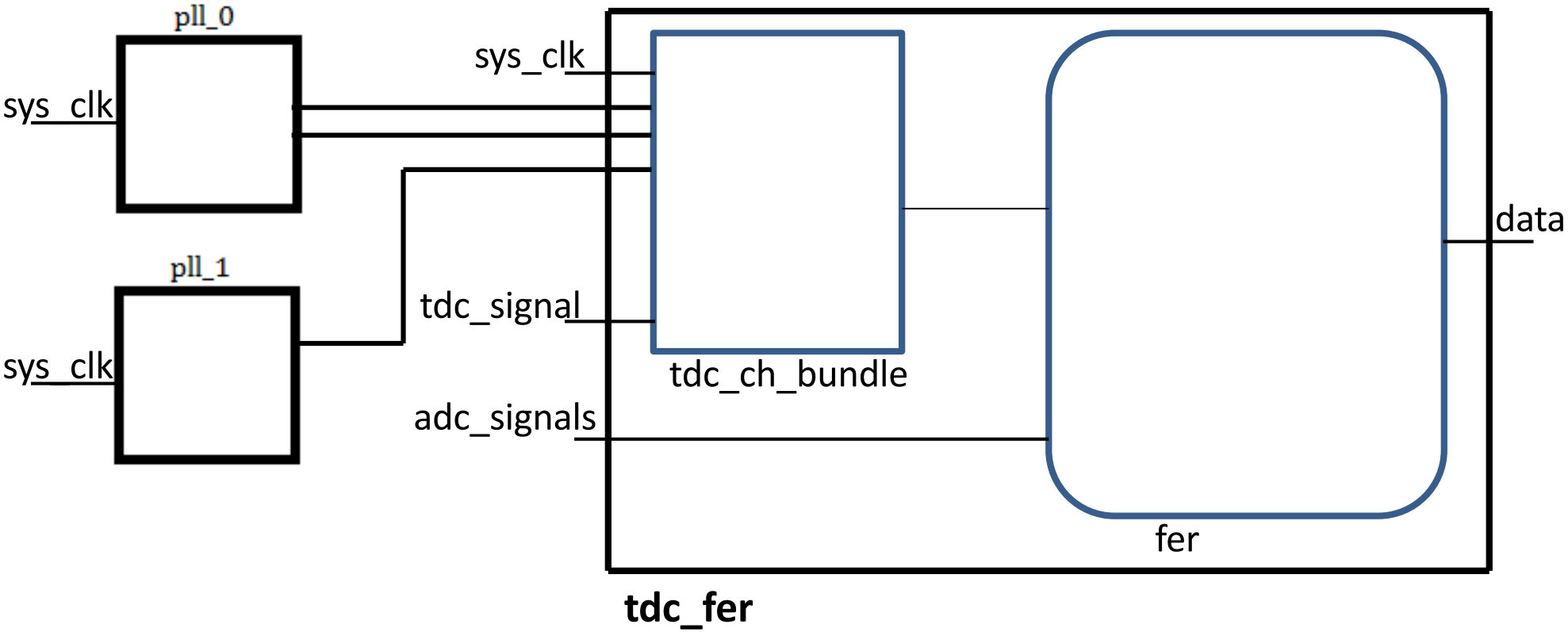
tdc_ch_bundle



- Get Rid Of Unused Signals/Pins
- Take Out From The Tdc-entity The Two Plls
- From Two Coupled Channel To A Single One
- Create A New Entity Linking The New Tdc With Its Own Fer

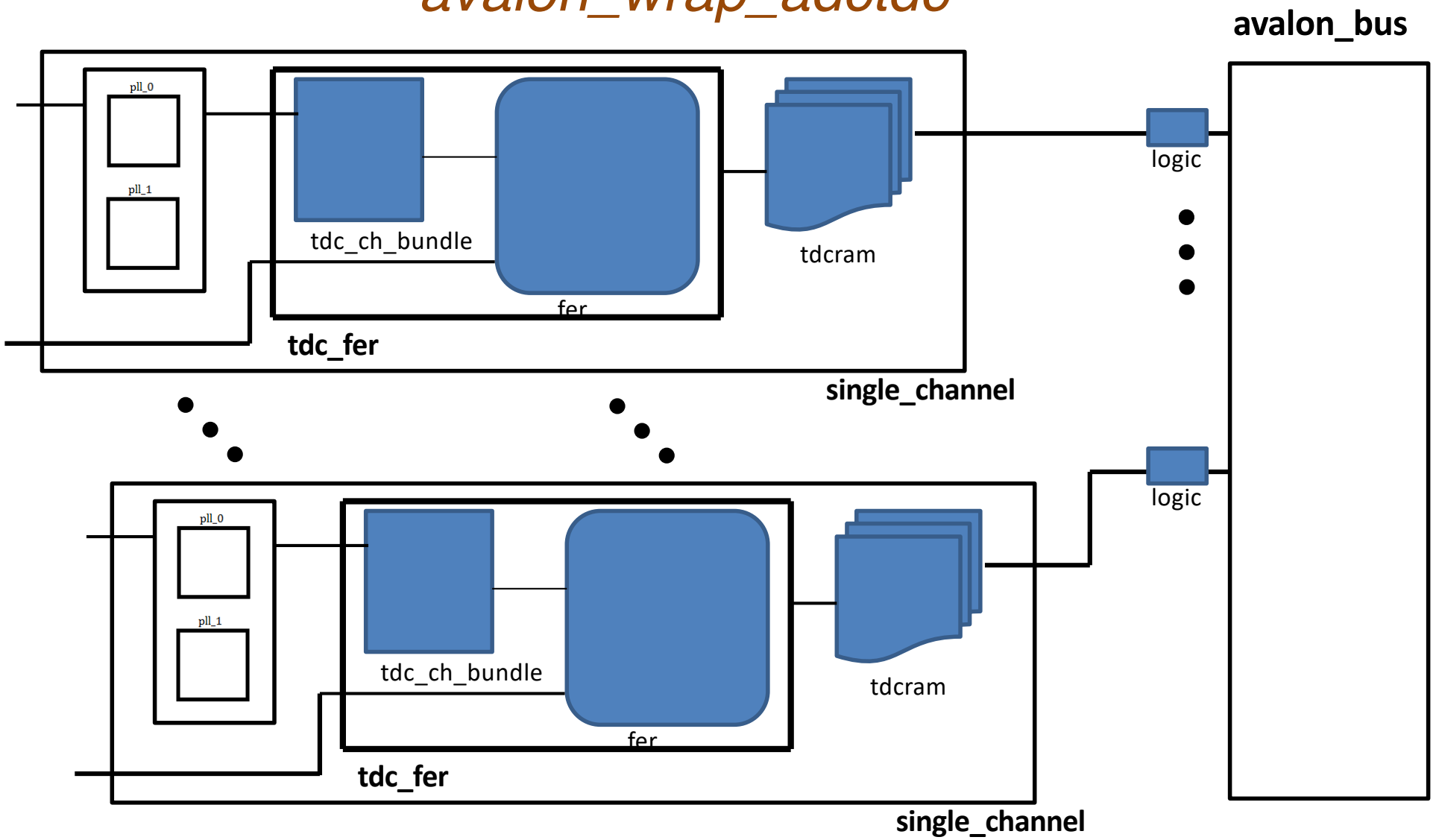
TDC CHANNEL

TDC_FER



MAIN BLOCK

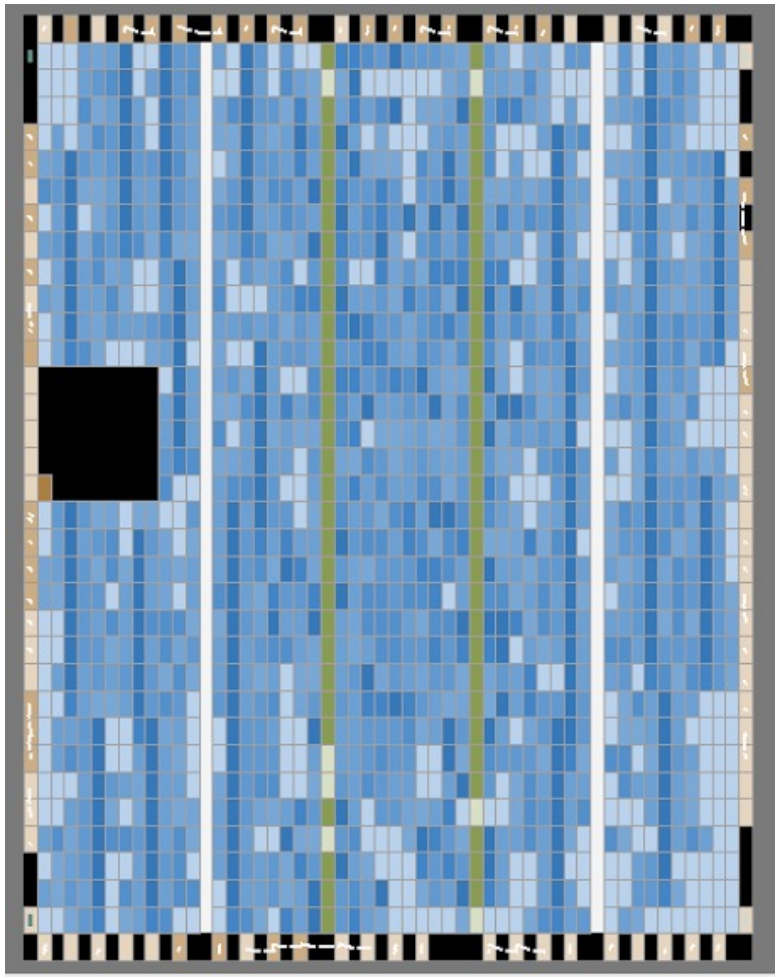
avalon_wrap_adctdc



MAIN BLOCK

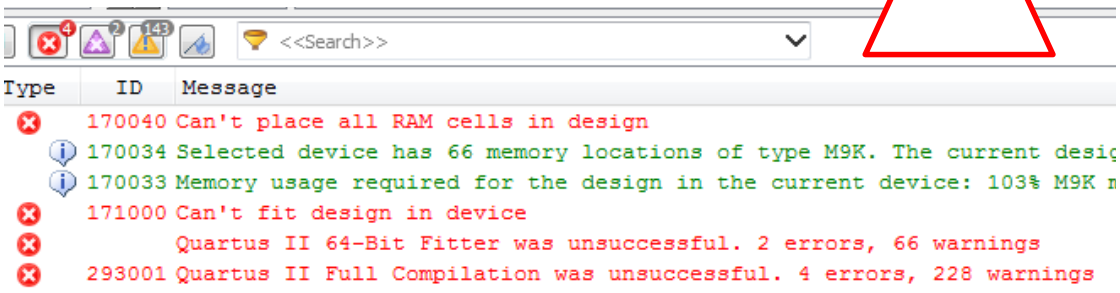
Fitting

12 channels



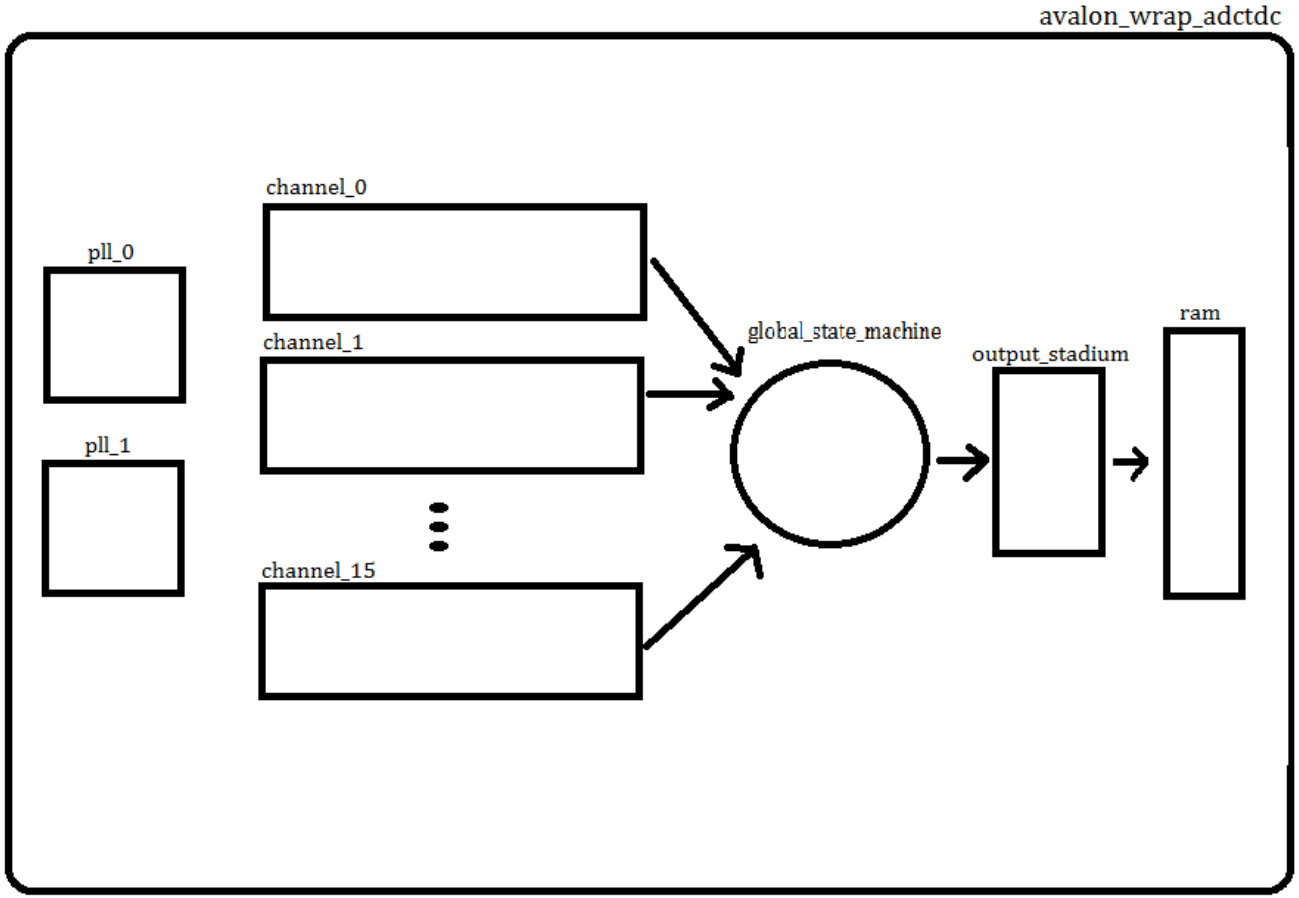
16 channels

Flow Summary	
Flow Status	Flow Failed - Wed Sep 10 13:00:35 2014
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	testnios
Top-level Entity Name	testnios
Family	Cyclone III
Device	EP3C25F324C8
Timing Models	Final
Total logic elements	22,180 / 24,624 (90 %)
Total combinational functions	20,053 / 24,624 (81 %)
Dedicated logic registers	12,274 / 24,624 (50 %)
Total registers	12274
Total pins	76 / 216 (35 %)
Total virtual pins	0
Total memory bits	340,032 / 608,256 (56 %)
Embedded Multiplier 9-bit elements	0 / 132 (0 %)
Total PLLs	2 / 4 (50 %)



MAIN BLOCK

New Design



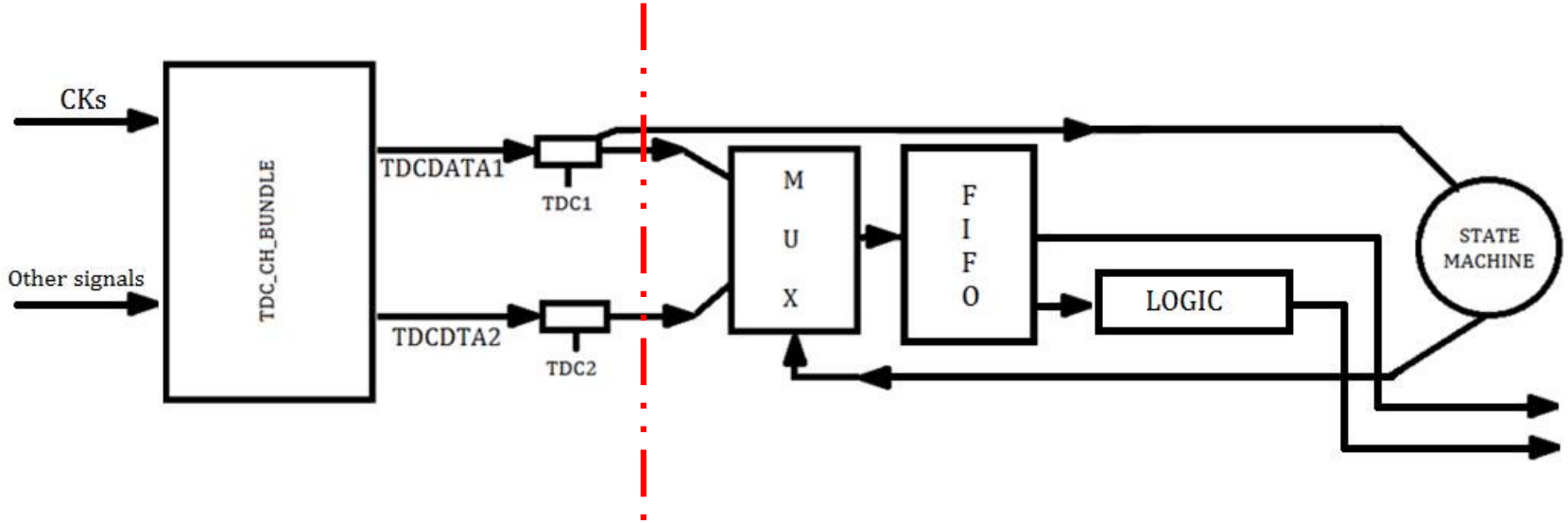
✓ Better In Sending Data To The ROC

- FIFO (Inside The Output_stadium) Is Easier Than Ram To Be Managed
- The Use Of Fifo Guarantees More Independence Among Channels

✓ Slimmer

CHANNELS

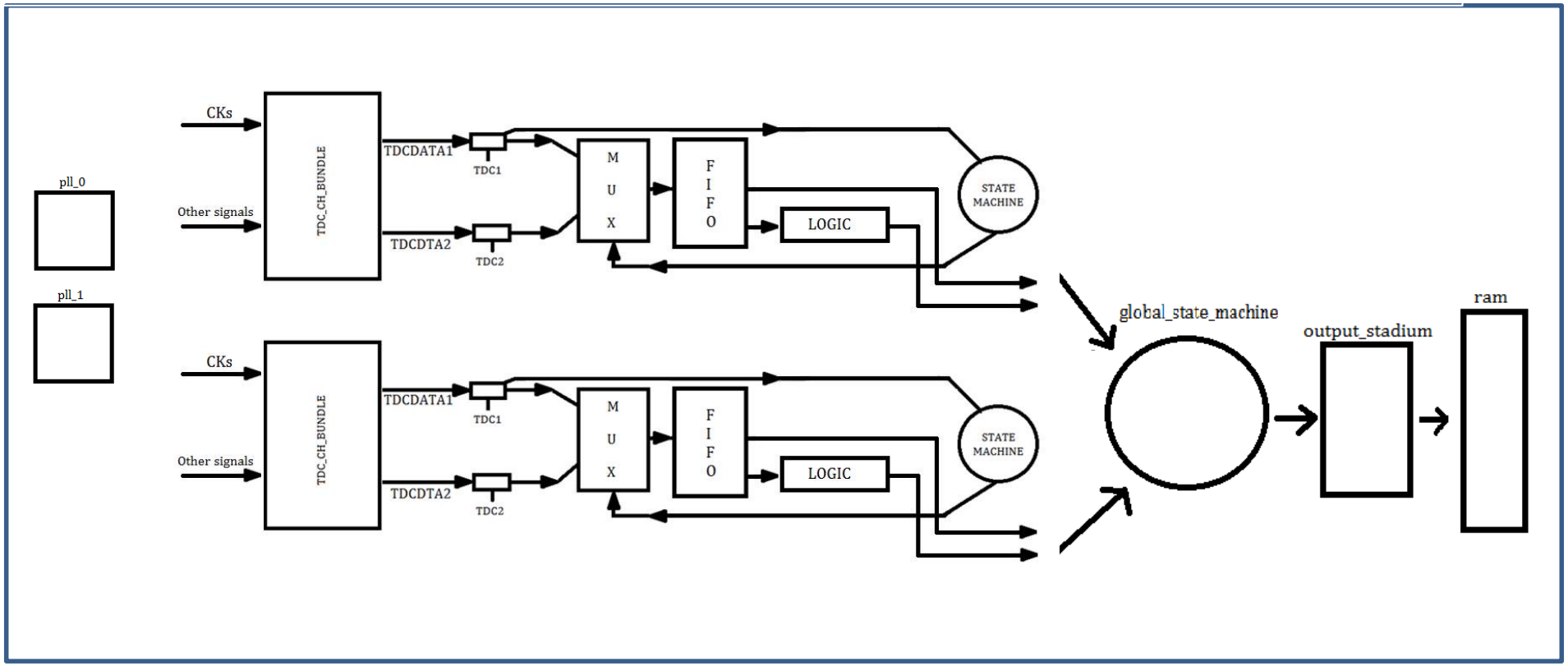
The New Channel Structure – Joining Our Projects



- New TDC Channel
- New Logic For The FER Entity

MAIN BLOCK

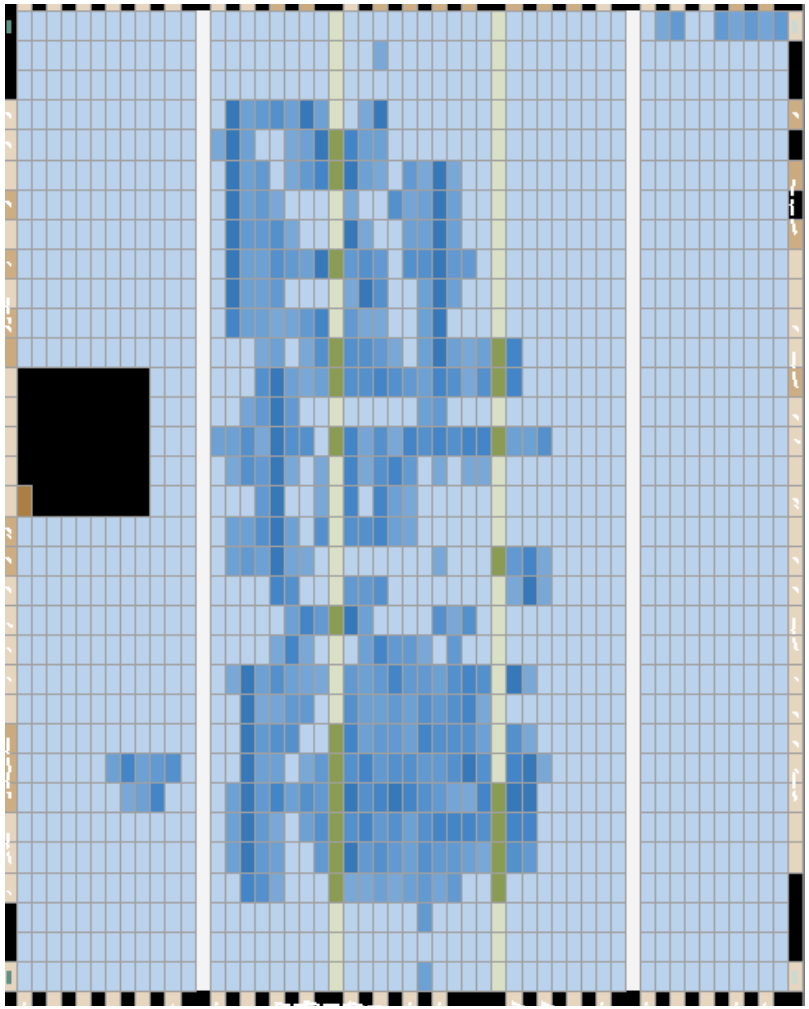
The New avalon_wrap_adctdc : 2 Channels



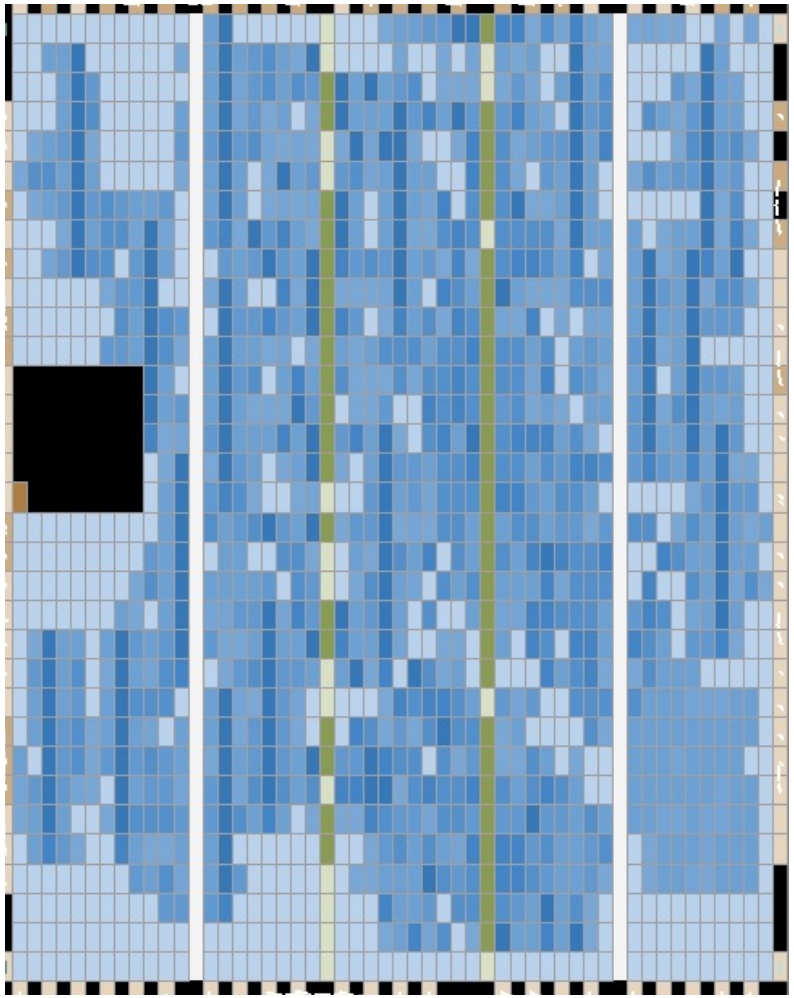
THE WHOLE SYSTEM

Chip Planners

2 channels



8 channels



WHAT IS LEFT

Future Works On The Digitizer

- Modify the gobal_state_machine to let it suitable for 16 channels and fit the whole design into the FPGA;
- Looking for the ROC : then join the projects;
- Achieve the best performance on the Altera FPGA and then move and fit the new design into the Microsemi IGLOO2.

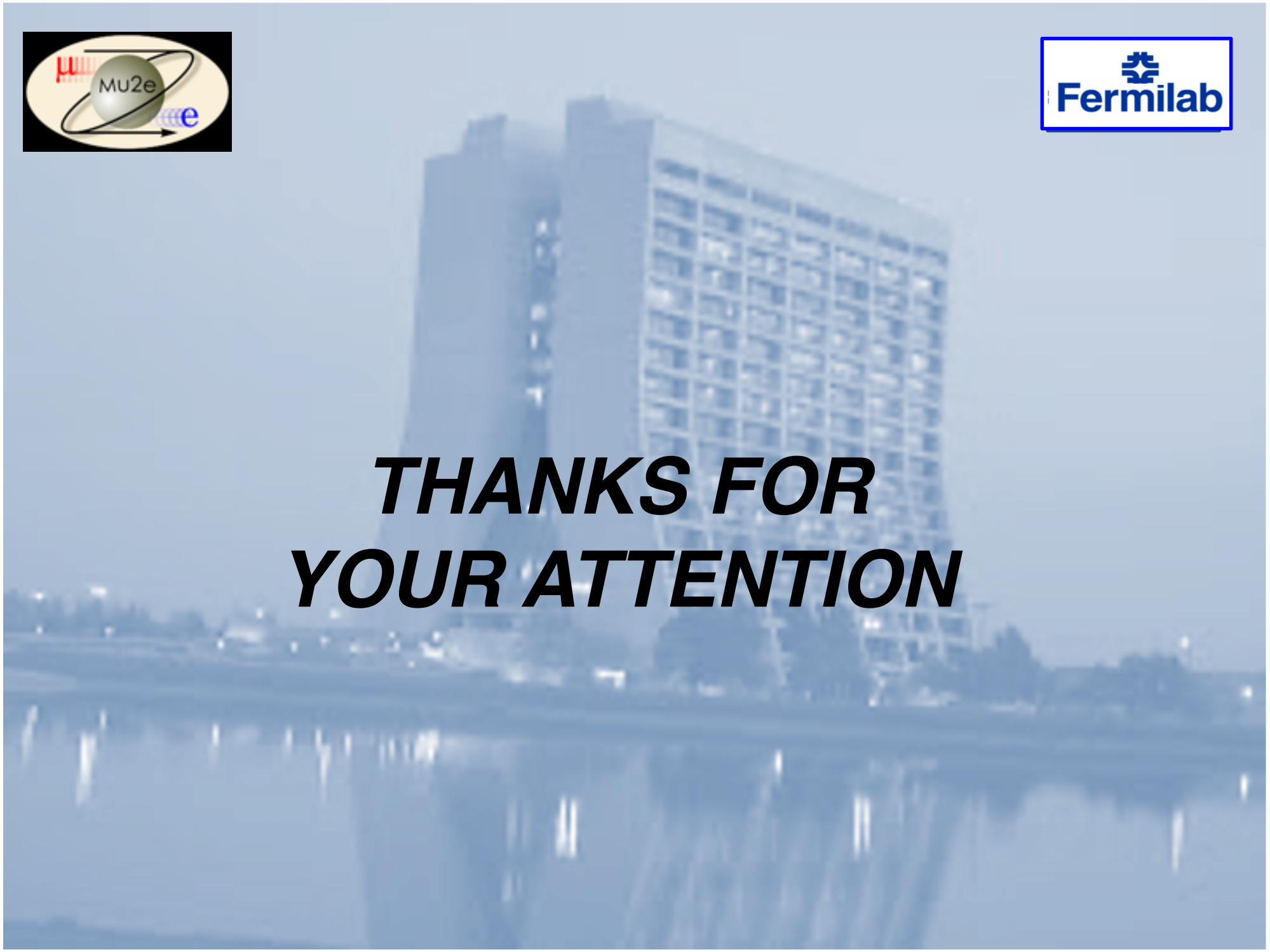
ACKNOWLEDGEMENTS

Thank you!

Vadim: my supervisor, who has provided me an unvaluable support me during my two months of work at Fermilab. With his teaching he has contributed to my personal and professional growth.

Gabriele: who collaborated with me in the whole working project. We are now not only good collegues but also very good friends.

Each summer students and professors: who shared with me this unforgettable experience.


THANKS FOR
YOUR ATTENTION