VIPIC: a 3D Read Out Chip at the Fermilab Test Beam Facility

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Outline

- Silicon tracking telescope
- CAPTAN Data Acquisition (DAQ)
- Software architecture
- VIPIC architecture
- Results

Radiation Hard detectors

Radiation-hard tracking detectors are being developed for the Large Hadron Collider (LHC) experiments to withstand the increased radiation expected from the High-Luminosity LHC (HL-LHC) upgrade.

The detectors currently in use in the innermost barrel layer of the CMS pixel tracker will receive fluences up to the order of $10^{15} n_{eq}/cm^2$ dose in their lifetime.

After the HL-LHC upgrade, the new detectors in this layer are estimated up to receive 20 times more $(2x10^{16} n_{eq}/cm^2)$ this amount!

Sensors: Pixels vs Strips





Pixels:

- Low resolution (cell size is 100x150 µm²)
- Small coverage area (1.6x1.6 cm²)
- Strips:
 High resolution (60 µm pitch)
 Big coverage area (4x4 cm²)

Telescope



CAPTAN

Compact And Programmable daTa Acquisition Node

- Flexible boards designed of data acquisition
- FPGA based
- Distributed architecture
- Independent nodes
- Easy access via Gigabit ethernet



Board Interface

- The architecture used is the Xilinx MicroBlaze soft core
- Ethernet packets are exchanged by UDP protocol to achieve high bandwidth efficiency
- All data and commands are encoded as 32 bit words

DAQ architecture



XDAQ

- XDAQ is an open source project to provide a simple, consistent and integrated distributed programming environment for Data Acquisition
- Developed at CERN and extensively used in CMS
- The framework builds upon industrial standards, open protocols and libraries



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Final Review

VIPIC

- New 3D technology Read Out Chip (ROC) developed by Gregory Deptuch's group at Fermilab
- Originally designed for high timing resolution
 X-ray Photon Correlation Spectroscopy
- We are developing the Firmware and Software to test this ROC in the test beam.

Time issue



The strips have an internal time stamp counter The VIPIC do not, the time stamp is added by the CAPTAN when the data is sent out

Timing issues

- Input clock half of the 54 MHz of the accelerator
- 48-bit Time Stamp Counter
- Each hit has only an 8 bits counter
- Strips and VIPIC share the same clock and trigger events

The actual timestamp is reconstructed offline merging the 48 bit counter with the 8 bits of the hit

Read Out Latency: VIPIC vs strips



difference between the trigger event and the hit

difference between the trigger event and the hit

The VIPIC has a wider read out latency variance than the strips

Preliminary results

2D efficiency distribution Dut0



- The inefficiency is likely due to the DAQ
- Thanks to this study a new improved version will be implemented for the next test beam run

Preliminary results



My other tasks

- I improved the configuration and made it more flexible with the introduction of JSON
- I prepared the software interface for the digital version of CMS ROC (PSI46Dig)
- I fixed minor bugs in the PxSuite software

Thanks for your attention