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Managed by Fermi Research Alliance, LLC for the U.S. Department of Energy Office of Science

CMS L1 Silicon-based Tracking Trigger
Evaluation of Virtex-7 and Kintex UltraScale FPGA

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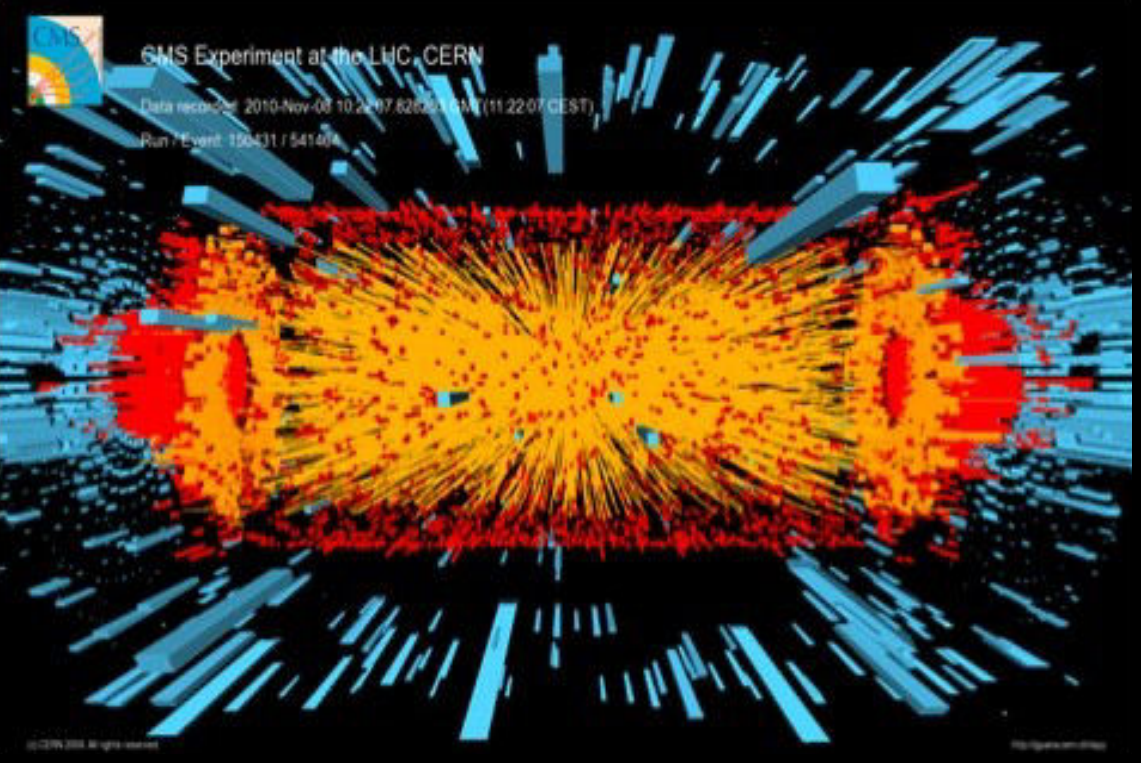
Supervisor: Ted Liu

Italian Summer Students Final Reports

September 25th 2015



CMS Experiment at the LHC CERN

CMS L1 Tracking Trigger:

Will need to reconstruct charged particle trajectories for every beam crossing.

Few numbers:

- 40 million beam crossings per second, one every 25 ns
- Bandwidth required to transfer up to 100 Tb/s

The challenges

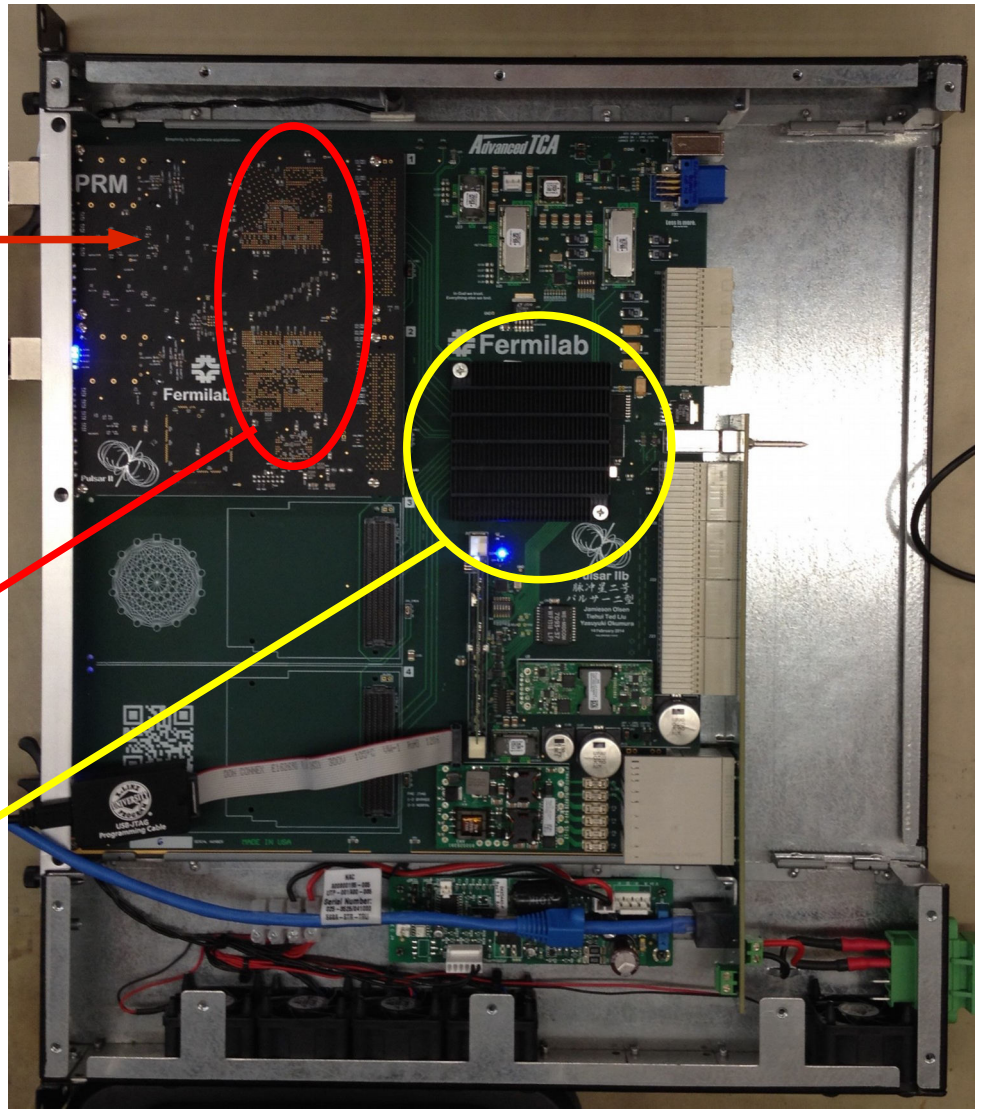
- **Compute-intensive**
  - Massively parallel computation involving *very large number* of processing elements;
- **Communication-intensive**
  - *High-speed transfer of data* among processing elements;
- **Data-intensive**
  - High-speed manipulation of *very large quantities of data.*

Pulsar IIb

PRM Mezzanine Card

#2 Kintex UltraScale

Virtex-7



XILINX FPGAs

Focus on:

- Data transfer evaluation: **IBERT** Test
  ---> *High speed data transfer* & serial link
- **BlockRAM** features study
  ---> *Huge data storage and quick access*

GTH Transceivers

GTH Transceivers

VC709 board provides acces to 22 GTH Transceivers:

- #8 PCI Express x8 endpoint edge connector
- #10 FMC HPC connector
- #4 SFP+ connectors

GTH are grouped by four in Quads;

Through SFP connectors we have access to **Quad 113**.

Integrated Bit Error Ratio Test

Integrated Bit Error Ratio Test (IBERT) core for 7 series FPGA GTX transceivers is designed for evaluating and monitoring the GTX transceivers.

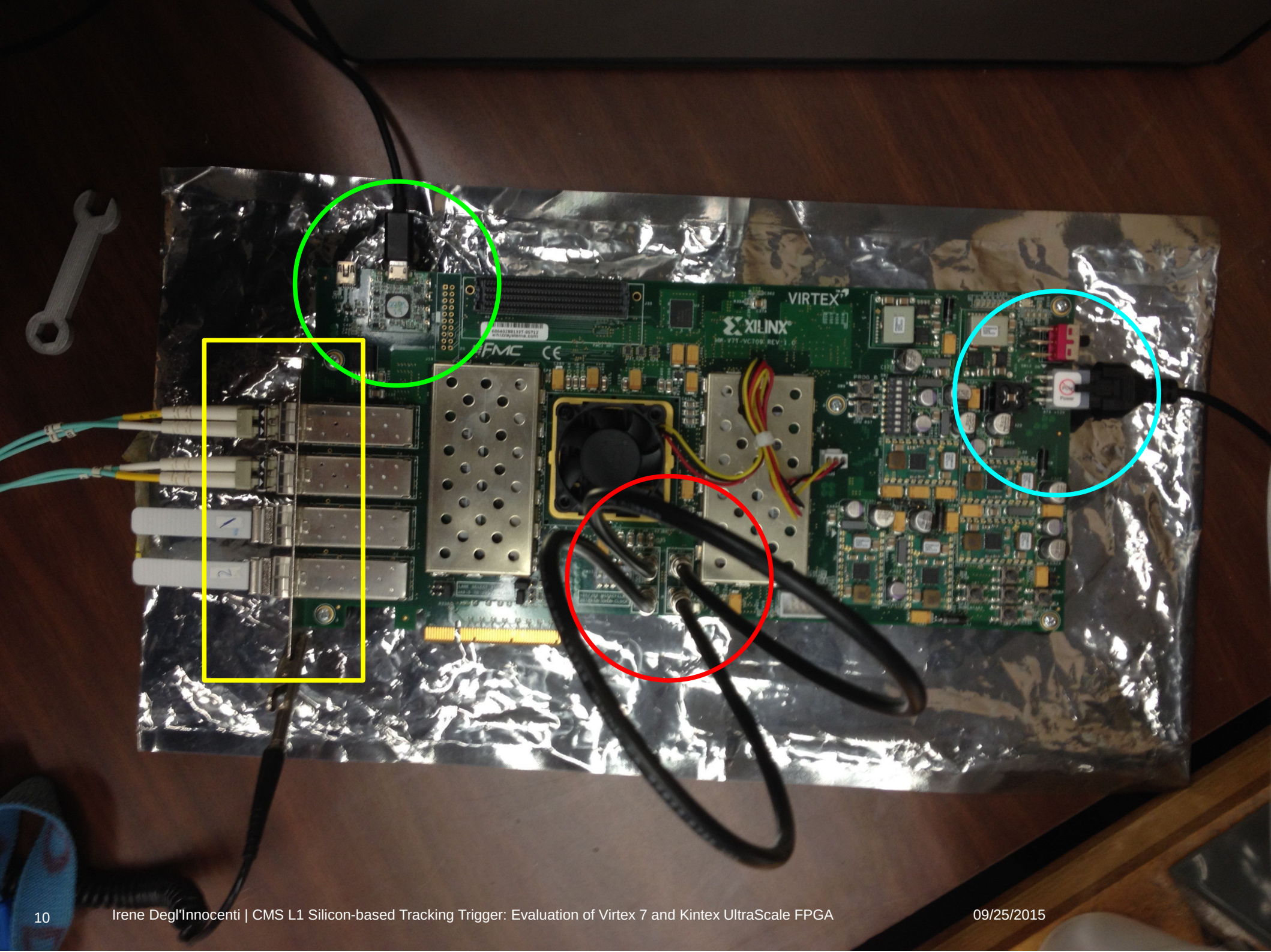
This core includes pattern generators and checkers that are implemented in FPGA logic, and access to ports and the dynamic reconfiguration port attributes of the GTX transceivers.

Communication logic is also included to allow the design to be run time accessible through JTAG.

How to program VC709: IBERT test

VIVADO™ → The development environment

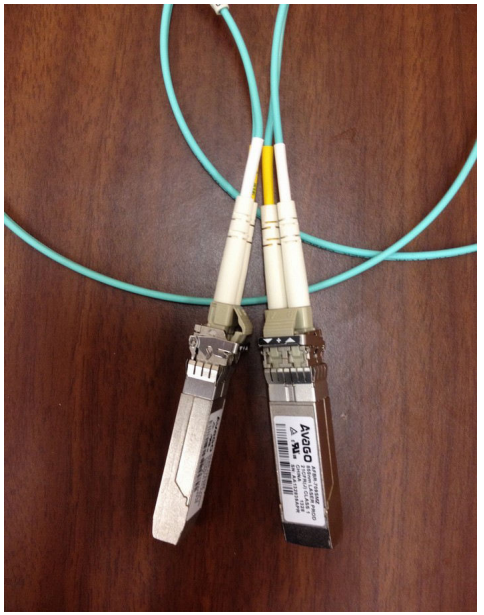
The guide provided by Xilinx →


VIRTEX
XILINX
FMC

Connections: optical cables and loopback

Prismian O.C.
2F 50/125 OM2 BB

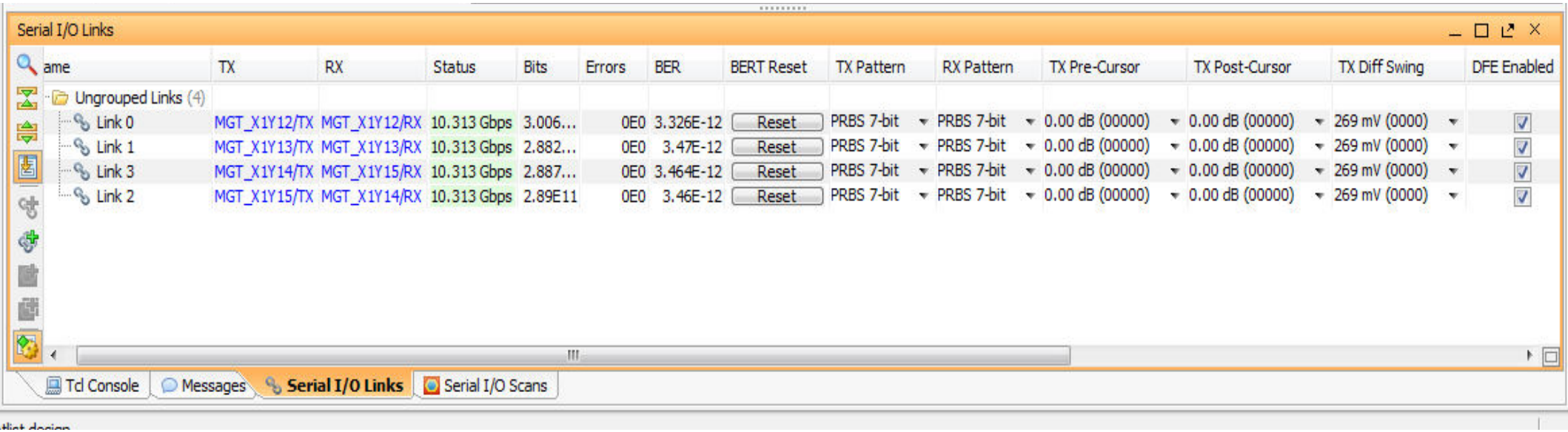
AFL Telecommunications
1-800-AFL_FIBER 50/125



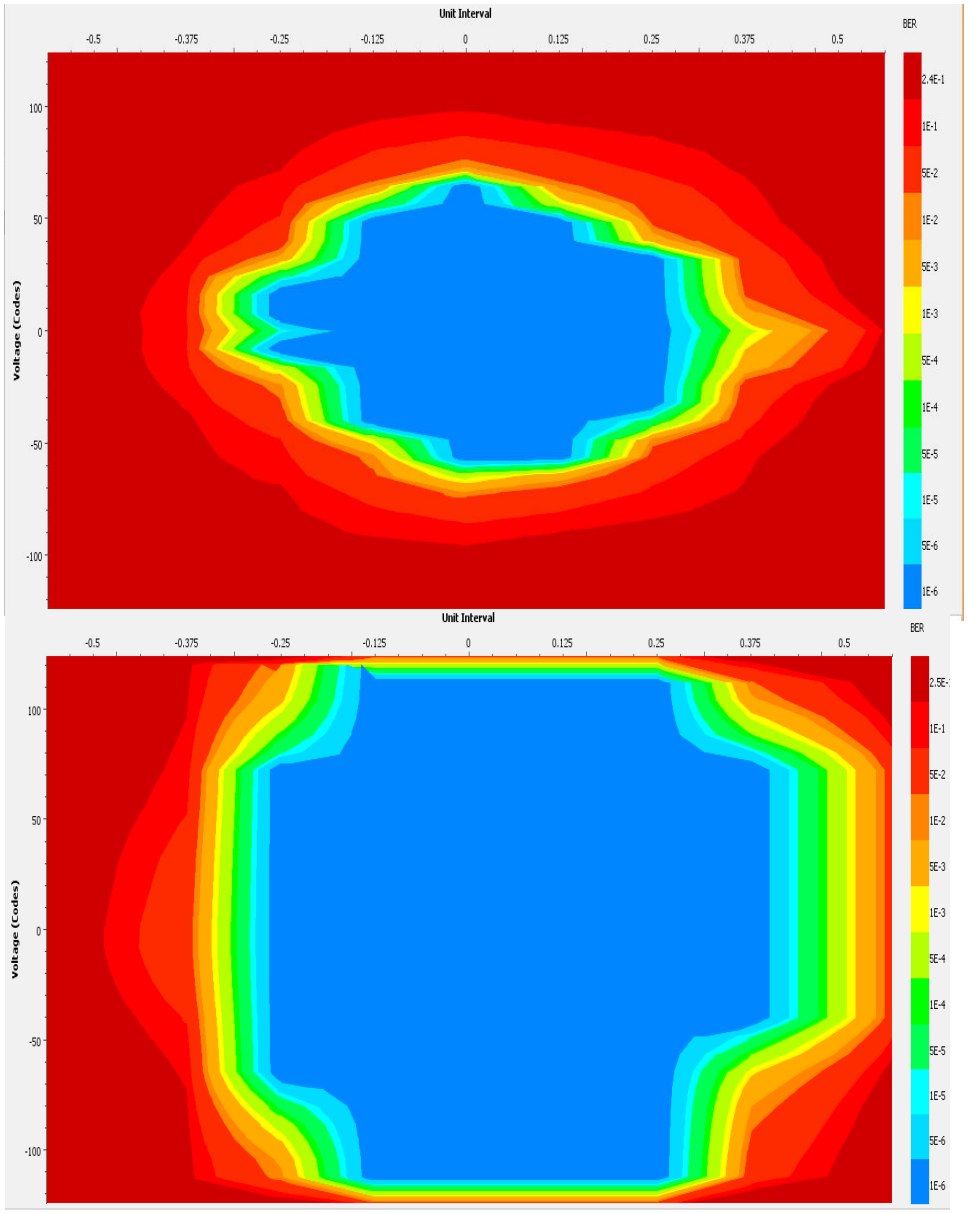
AMPHENOL CABLES
LSZH 04/13 0942M

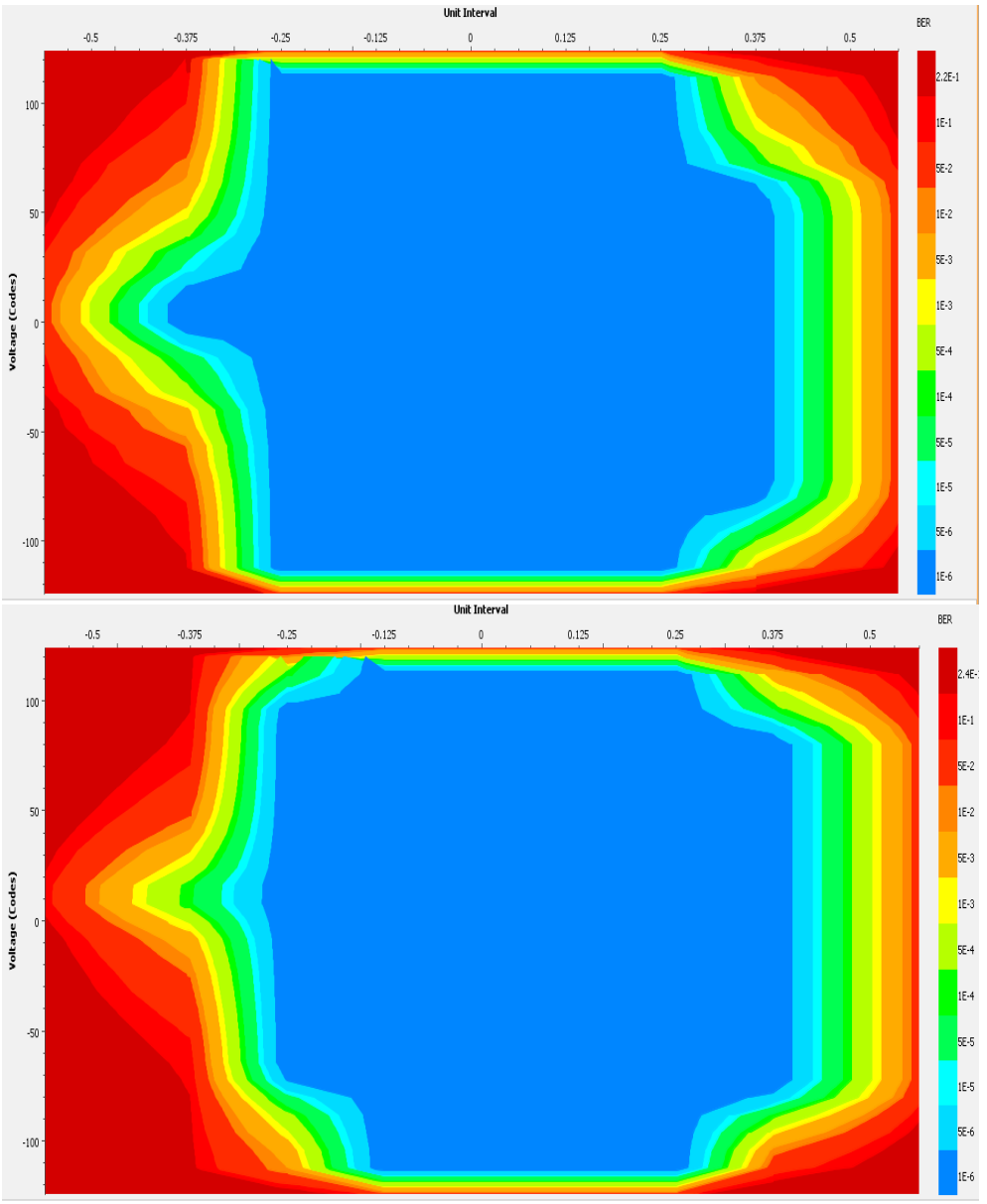
ELPEUS TECHNOLOGY
SFPP LB

Serial I/O Links Monitor



The statistical eye





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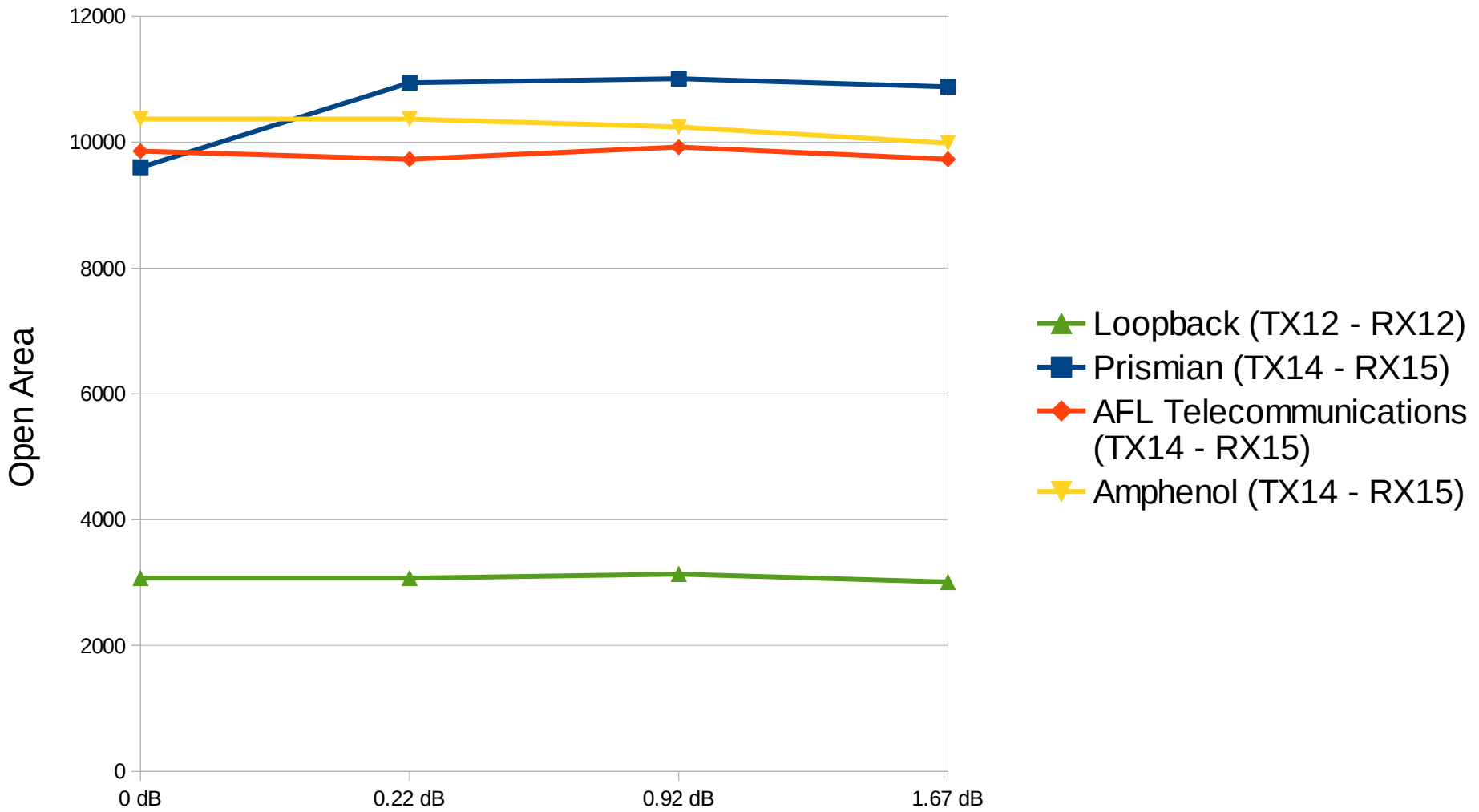
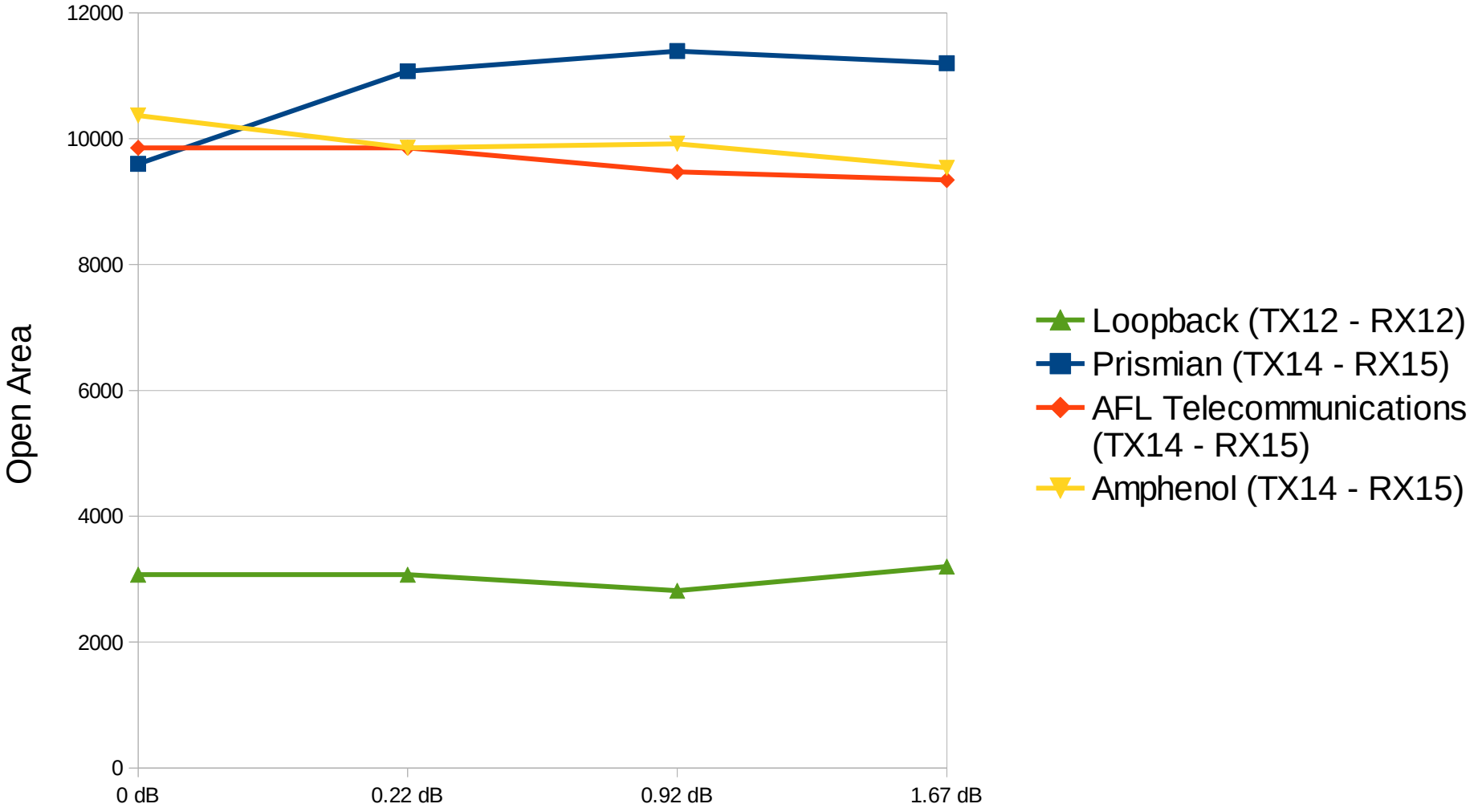
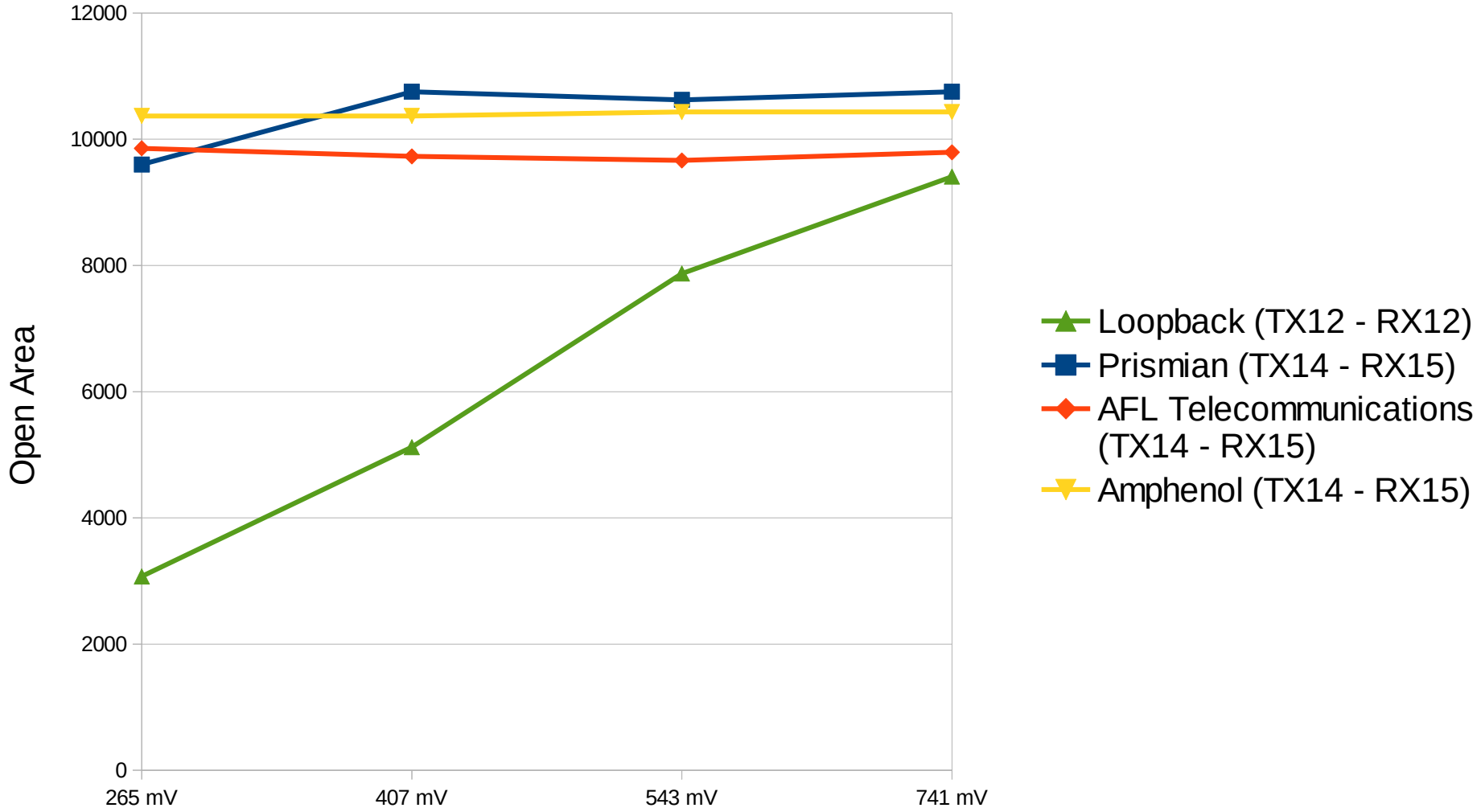
TX Pre Cursor



TX Post Cursor

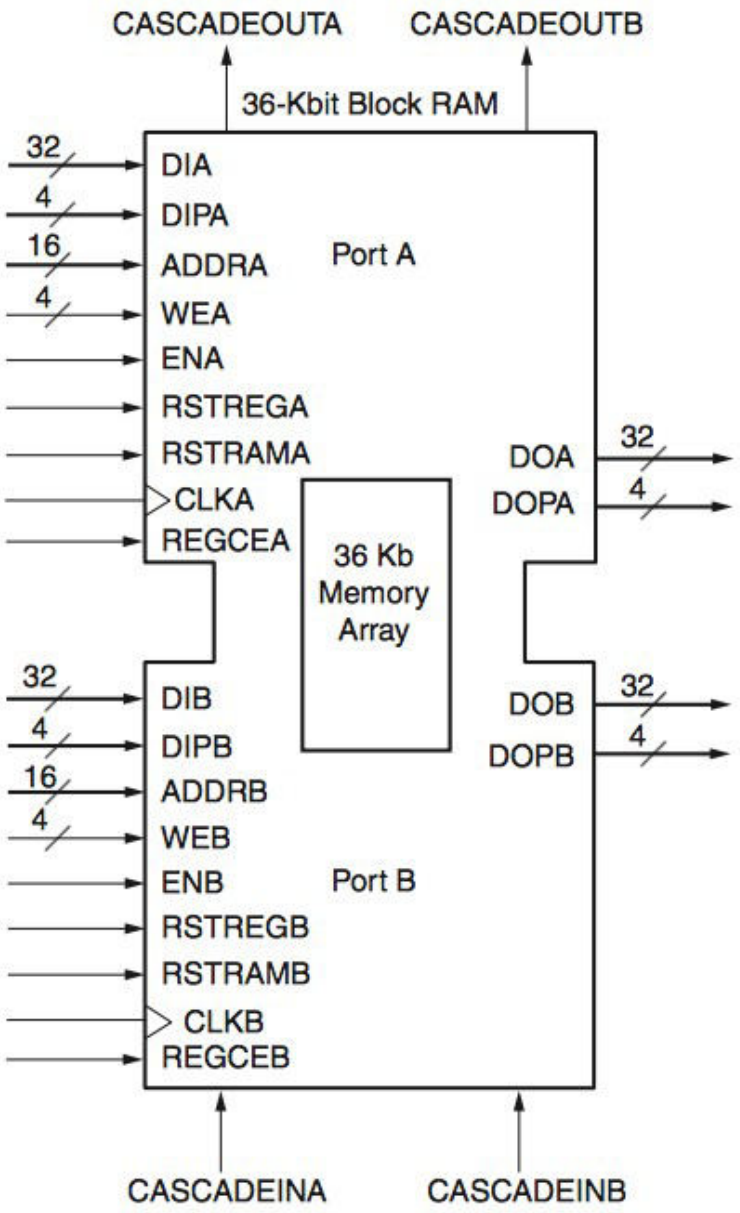


TX Differential Swing



BlockRAM

Block RAM in Virtex-7 FPGA



They are used for:

→ data storage or buffering

→ state machines or FIFO buffers

→ shift registers, LUT, or ROMs.

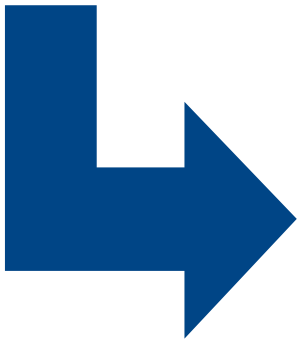
Main features:

- stores up to 36 Kbits
- two independent 18 Kb RAMs or single 36Kb RAM
- Write and Read are synchronous operations;
- the two ports are symmetrical and totally independent.

Virtex 7 - XC7VX690T

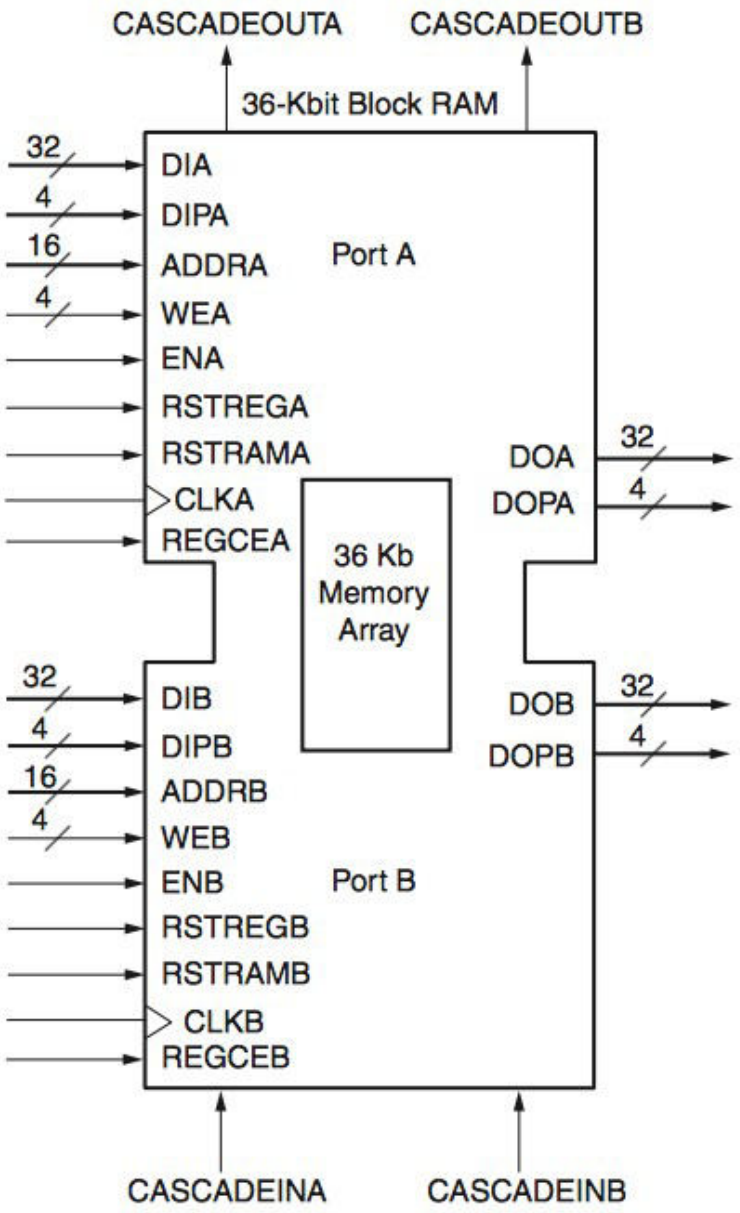
Columns per device: 15

36Kb Block RAM blocks per column: 100



1470 36Kb Block RAM blocks

Possible configurations: TDP



True Dual Port Mode:

→ Ports A and B are completely indipendent, they only share data.

→ Clocks can be different

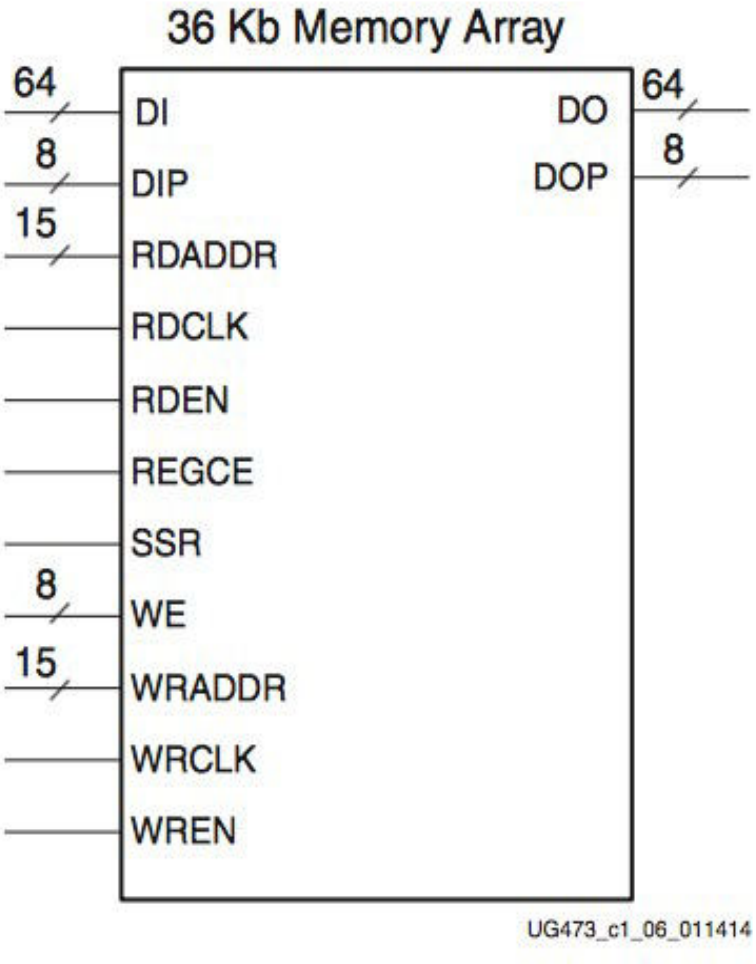
→ Data can be written to and be read from both ports

→ Maximum Bit Width: 36

ATTENTION: avoid conflict!

Accessing the same memory location from both ports could produce invalid output.

Possible configurations: SDP



Simple Dual Port Mode:

→ Port A is designated as the READ port

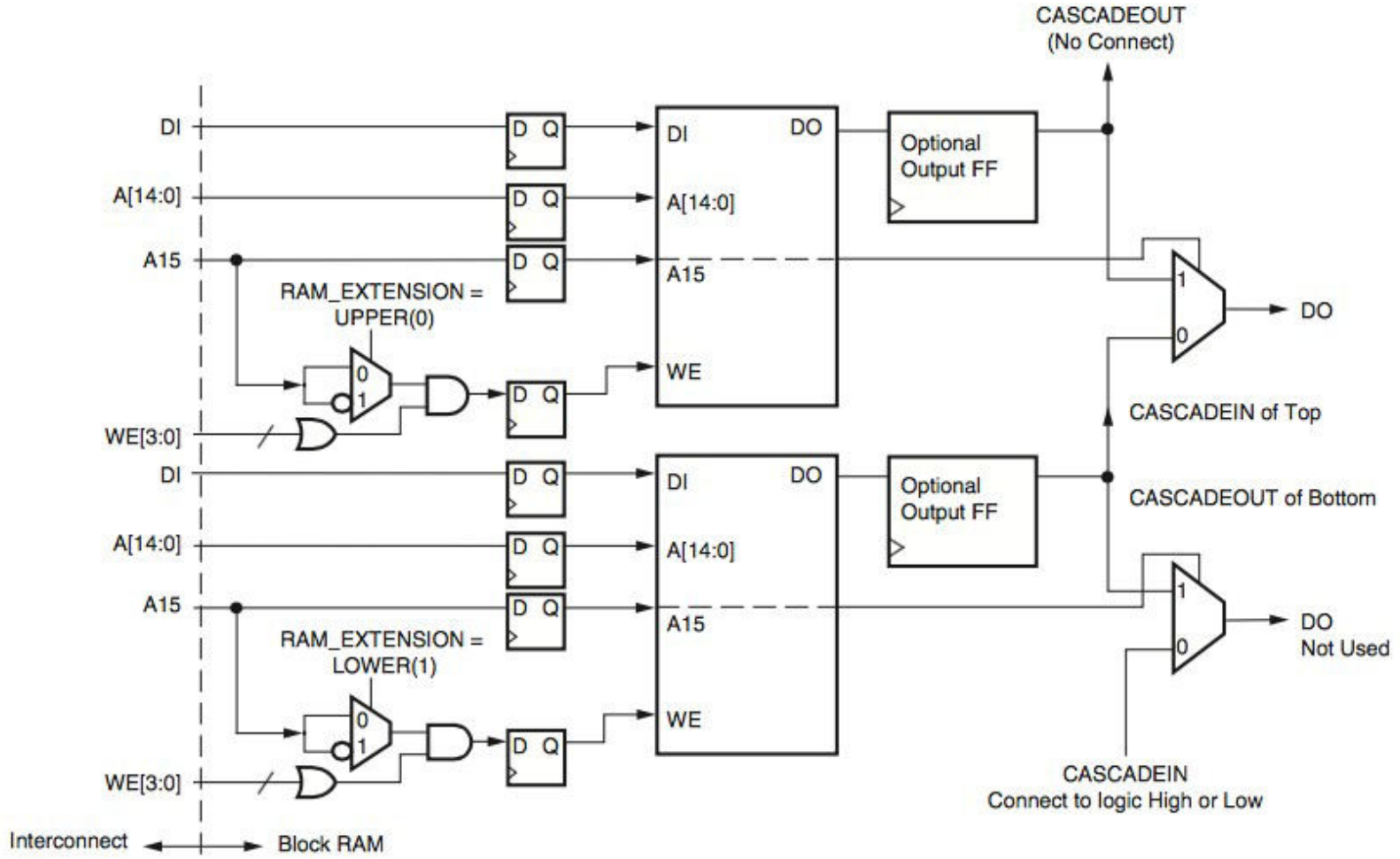
→ Port B is designated as the WRITE port

→ Maximum Bit Width: 72

→ One port width is fixed x64 or x72

Collision: when the read and write port access the same data location at the same time.

Possible configurations: Cascadable



Two adiacent 32K x 1 RAMs can be combined to form one 64K x 1 RAM

Write Modes

- WRITE_FIRST: outputs the newly written data onto the output bus.
- READ_FIRST: outputs the previuosly store data while the new one is being written.
- NO_CHANGE: maintains the output previuosly generated by a read operation.

→ Byte-Wide Write Enable: allows writing 8 bit portions of incoming data

Waveform Simulation

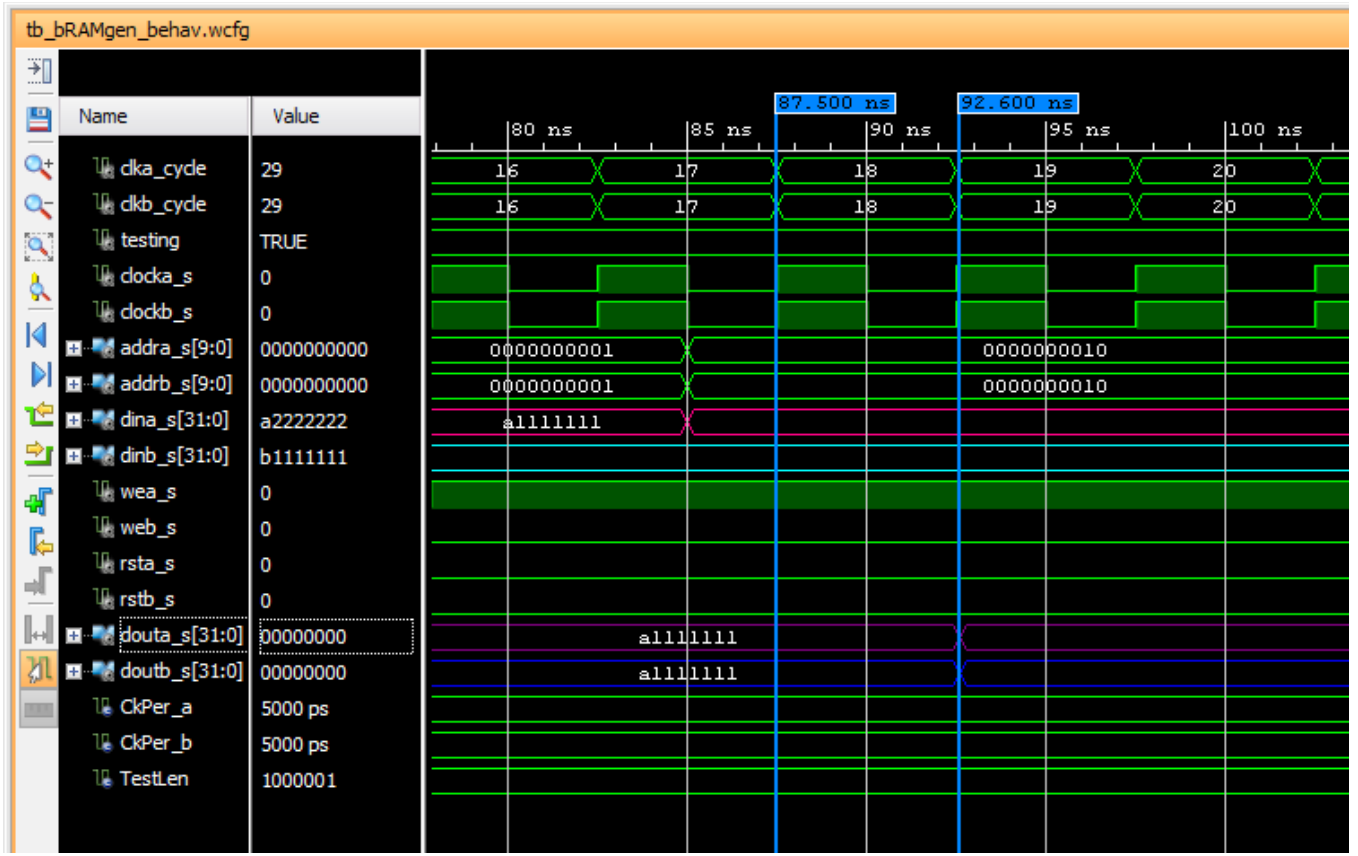
VHDL Entity bRAM created using the MACRO

Parameters:

- Block RAM size: 18Kb – 36Kb
- Optional output registers: enabled – not enabled
- Data Width: 16 bits – 32 bits
- Write Mode: WRITE_FIRST – READ_FIRST
- Clock frequency: 200 Mhz – 400 Mhz

Example: port A R/W, port B R/O

BRAM size 36Kb, data width 32 bits, output register enabled, WRITE_FIRST, clock 200 MHz



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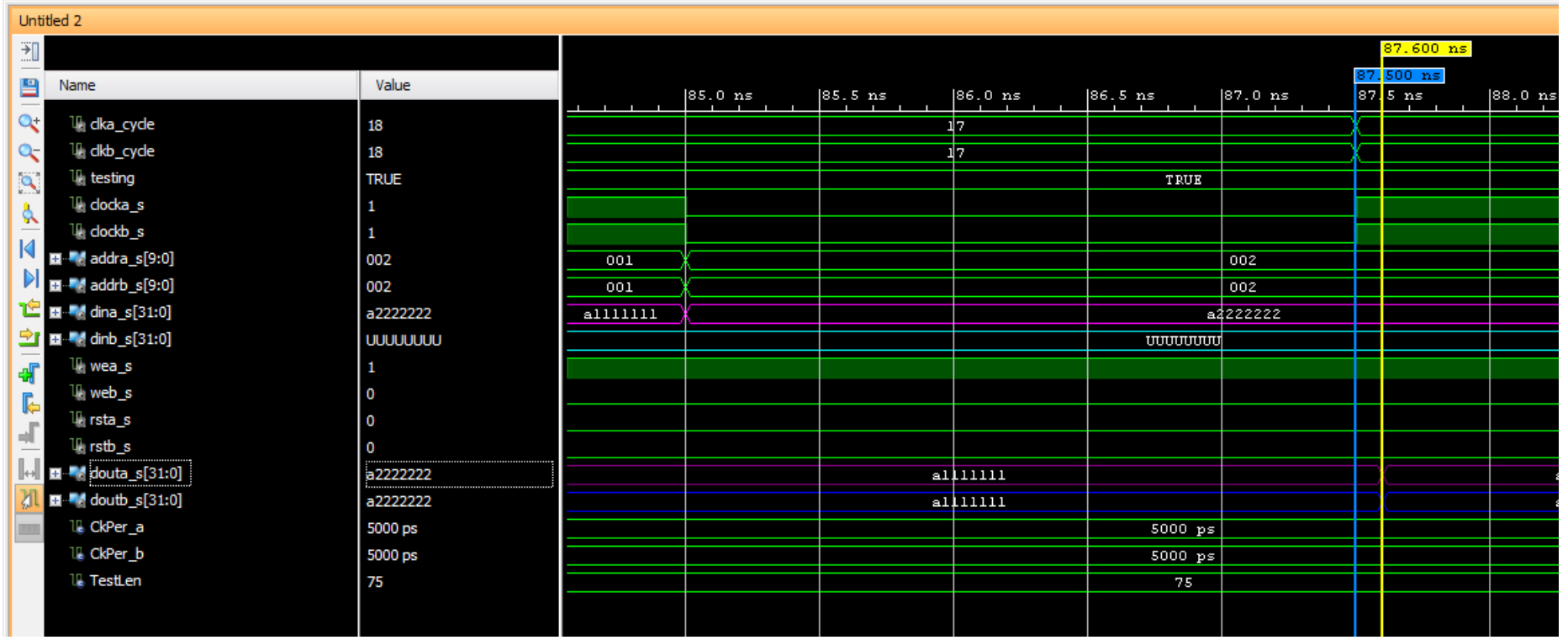
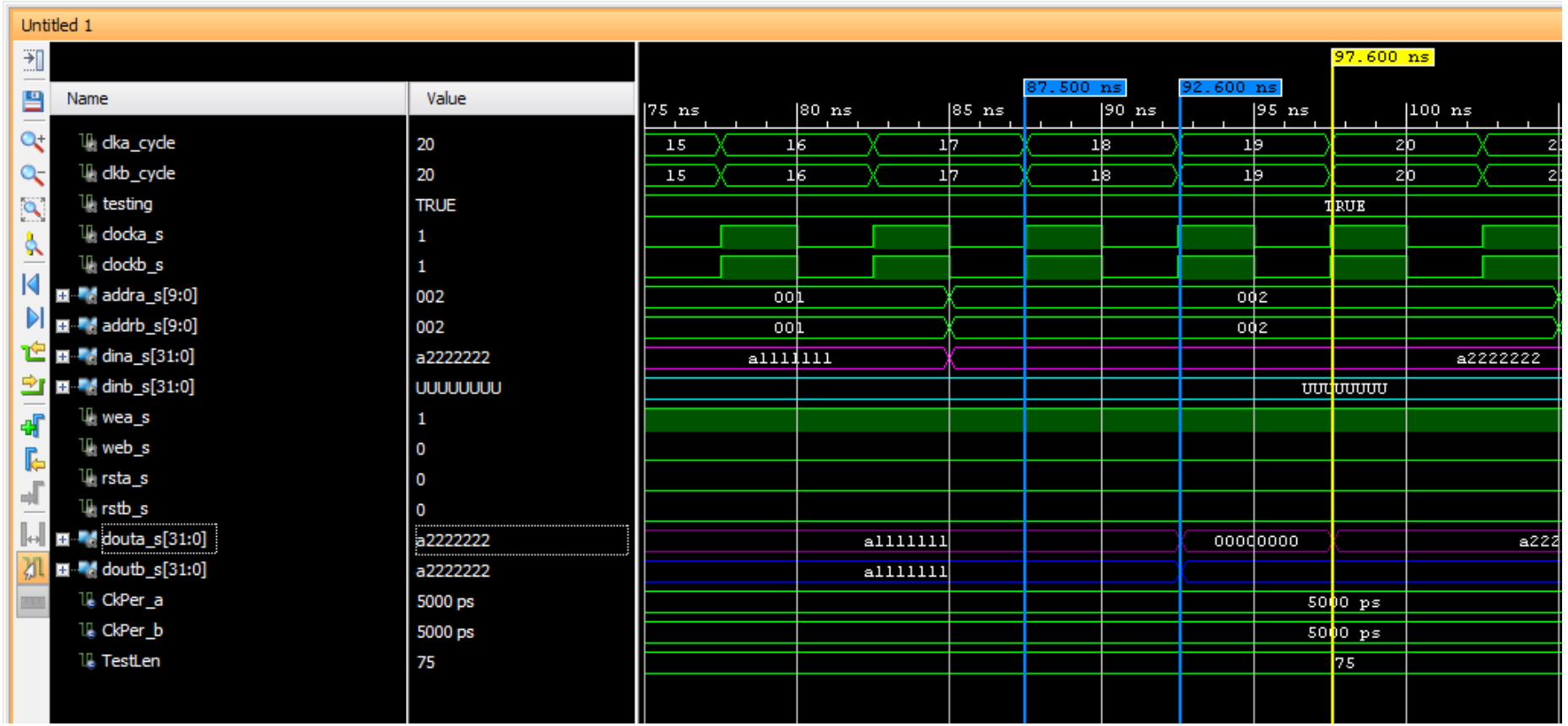
Example: port A R/W, port B R/O

BRAM size 36Kb, data width 32 bits, output register **not** enabled, WRITE_FIRST, clock 200 MHz



Example: port A R/W, port B R/O

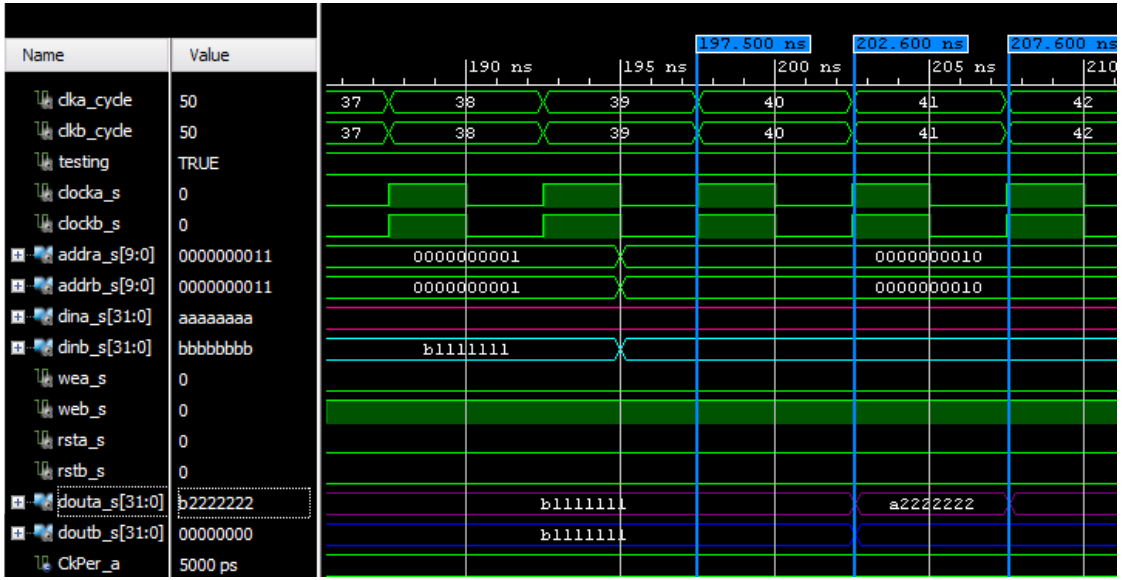
BRAM size 36Kb, data width 32 bits, output register enabled, **READ_FIRST**, clock 200 MHz

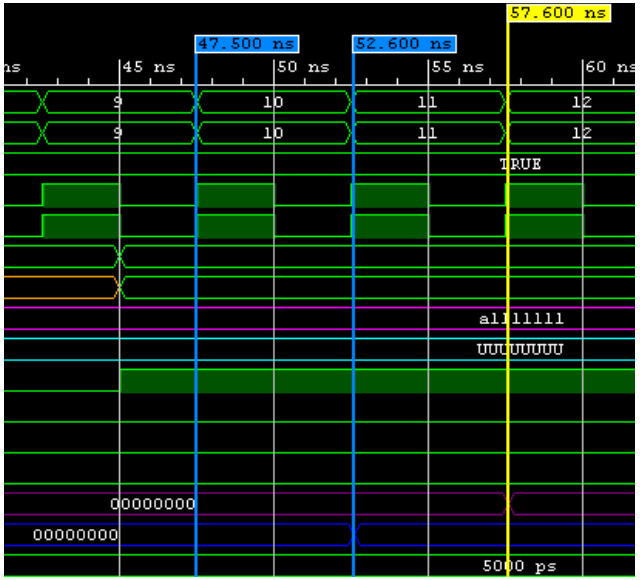


Observations

- The clockedge-to-output delay is modeled 0.1 ns

- When WE_A is low, port A outputs the previuosly store data while the new one is being written.
- When WE_B is low, port B outputs the newly written data onto the output bus.





Block RAM in Kintex UltraScale

Main changes from 7 Series FPGA:

- SDP memory supports NO_CHANGE mode
- New data cascading scheme (more than x2 block RAMs)
- Address enable added
- Dynamic Sleep mode preserving data content

Waveform Simulation

VHDL Entity bRAM created using the IP block RAM generator

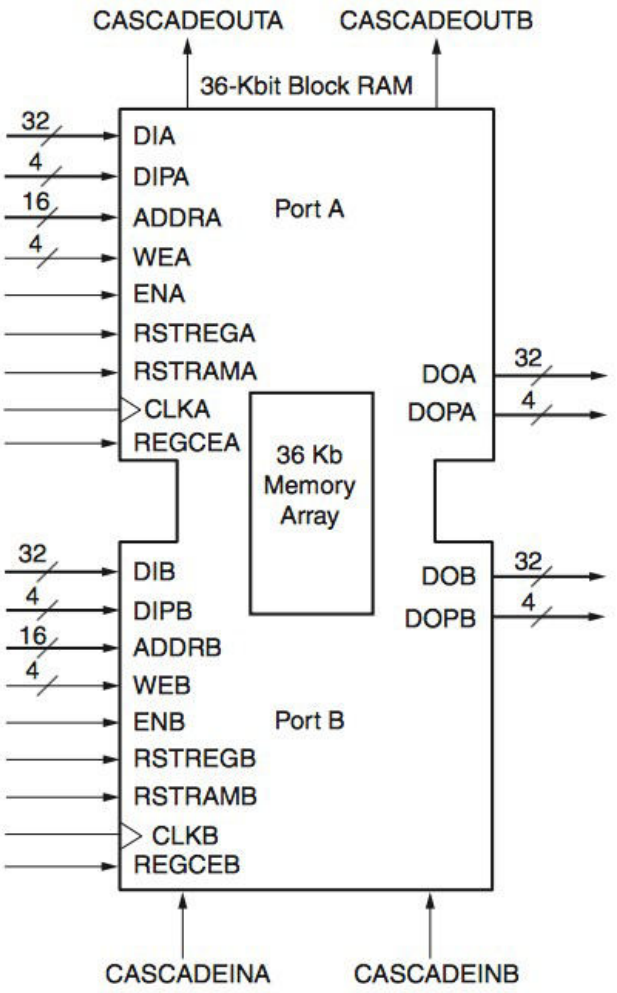
Different modes:

- TDP
- CASCADE – Single Port
- SDP + ECC

TDP (True Dual Port) Mode

	Port A	Port B
Write Width	18	36
Read Width	36	9
Write Depth	1024	512
Read Depth	512	2048
Operating Mode	WRITE_FIRST	READ_FIRST
Output Register	Enabled	Enabled
Reset Priority	Clock Enable	Set-Reset
Address Width	10	11

# 36K BRAMs	1
Read Latency	2 clock cycles



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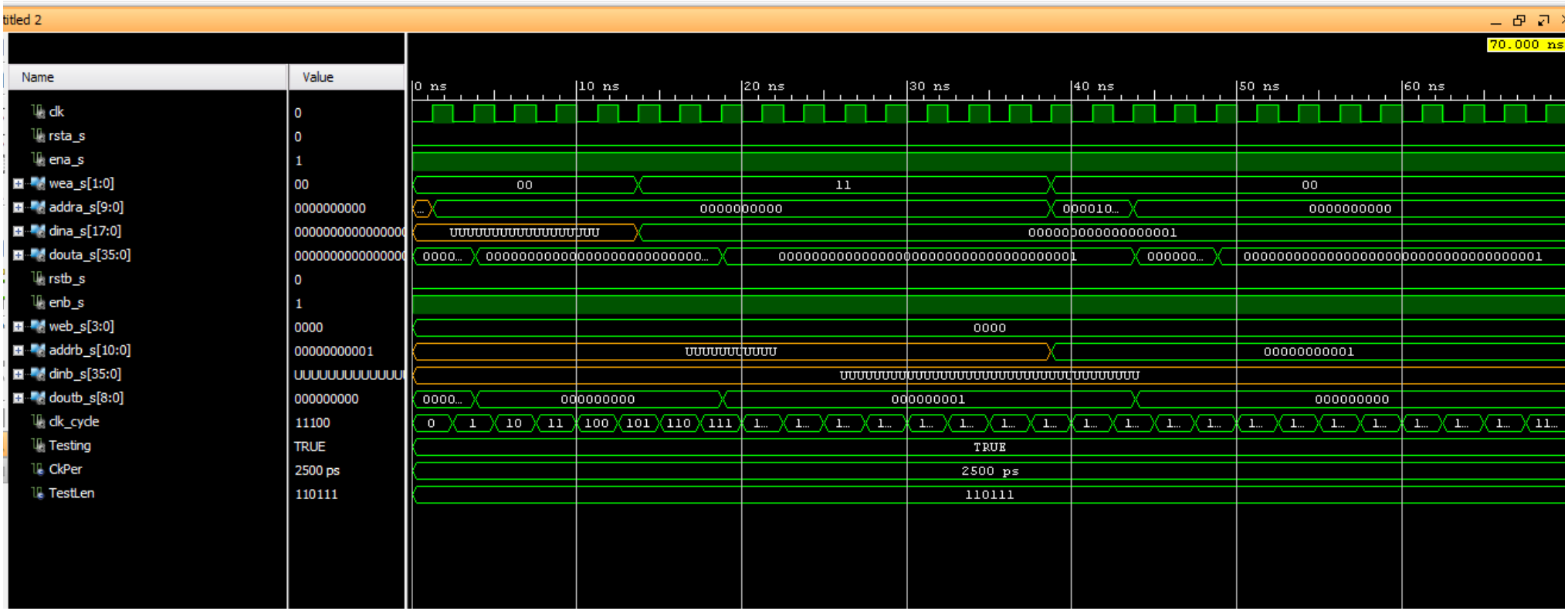
TDP (True Dual Port) Mode



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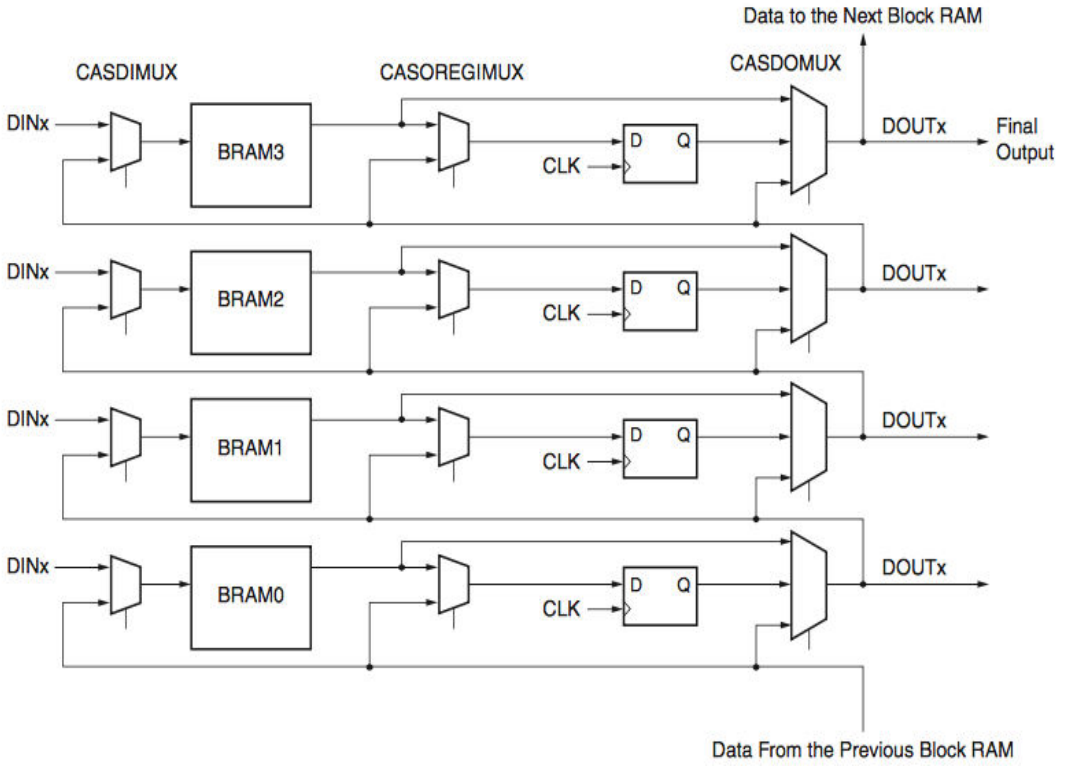
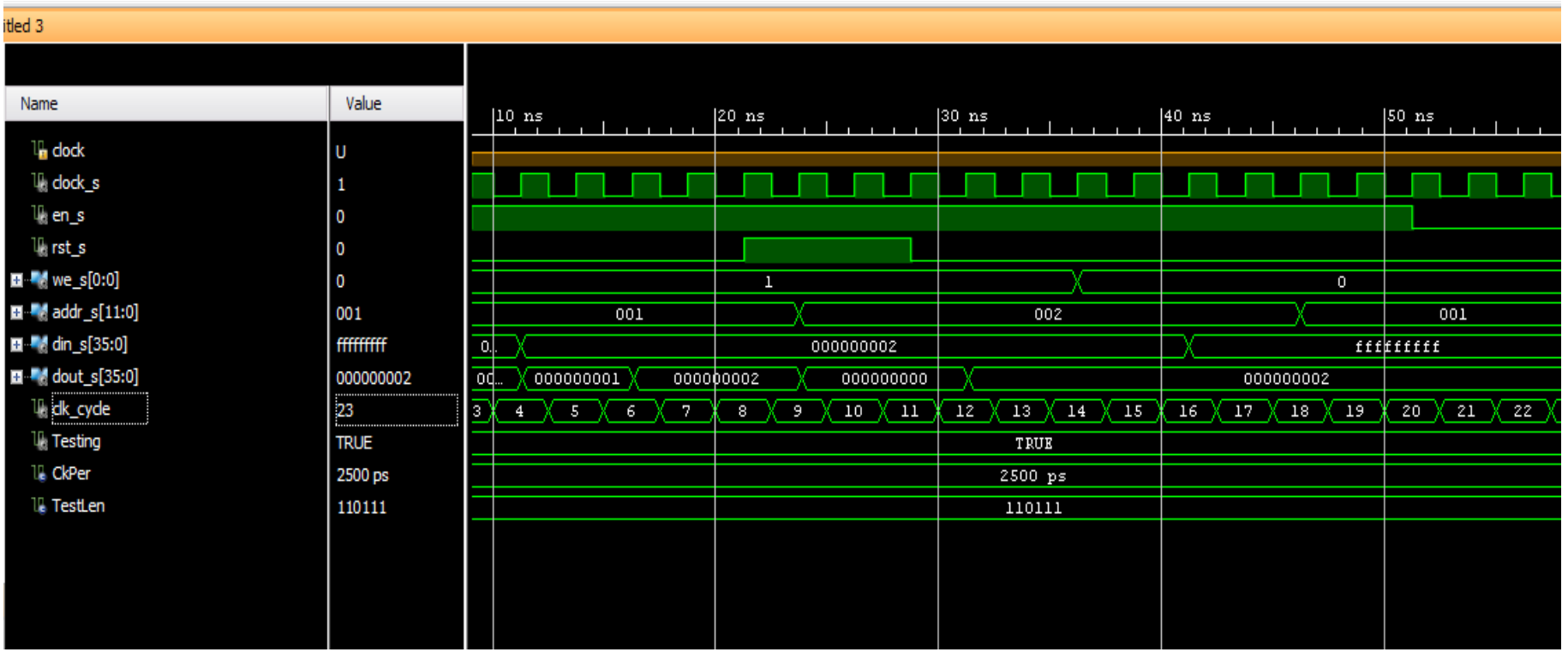
Cascade Mode – Single Port A

	Port A
Write Width	36
Read Width	36
Write Depth	4096
Read Depth	4096
Operating Mode	WRITE_FIRST
Output Register	Enabled
Reset Priority	Set - Reset
Address Width	12

# 36K BRAMs	4
Read Latency	2 clock cycles



Cascade Mode – Single Port A



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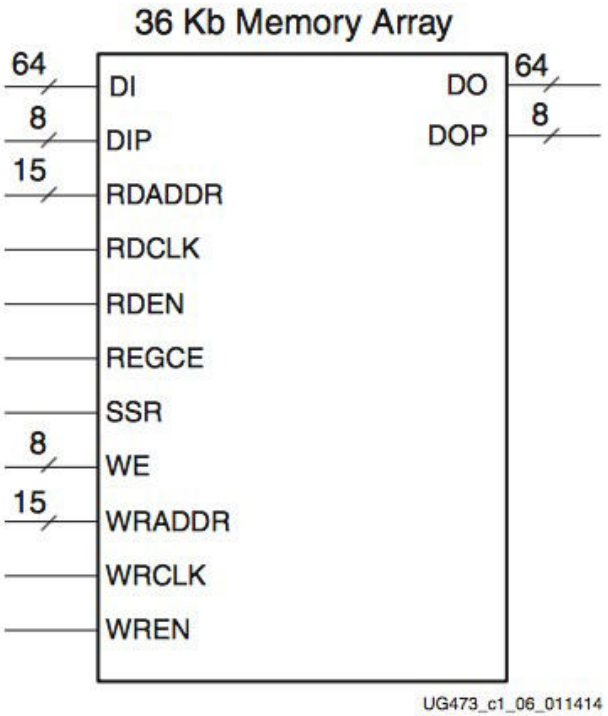
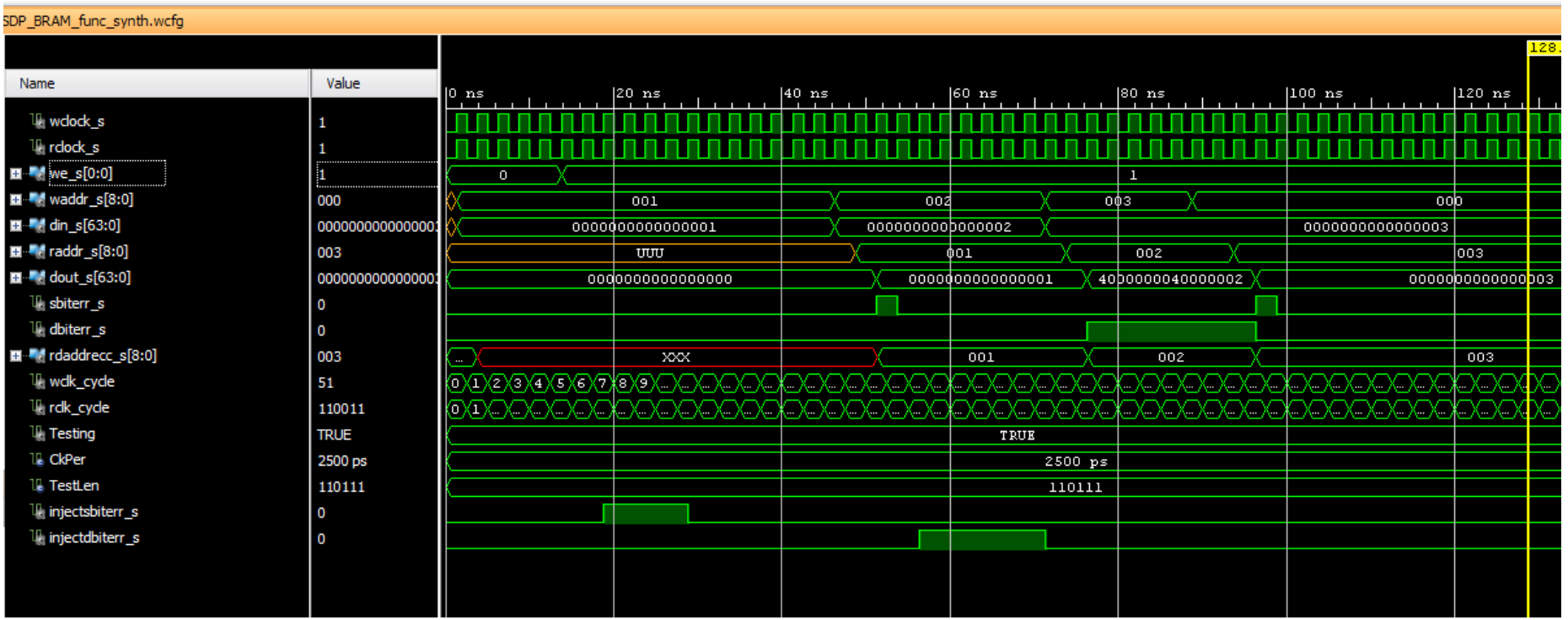
SDP (Simple Dual Port) Mode + ECC

	Port A (W)	Port B (R)
Write Width	64	~
Read Width	~	64
Write Depth	512	~
Read Depth	~	512
Operating Mode	WRITE_FIRST	~
Output Register	~	Enabled
Reset Priority	~	~
Address Width	9	9

# 36K BRAMs	1
Read Latency	2 clock cycles



SDP (Simple Dual Port) Mode



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ECC – Hamming code error correction

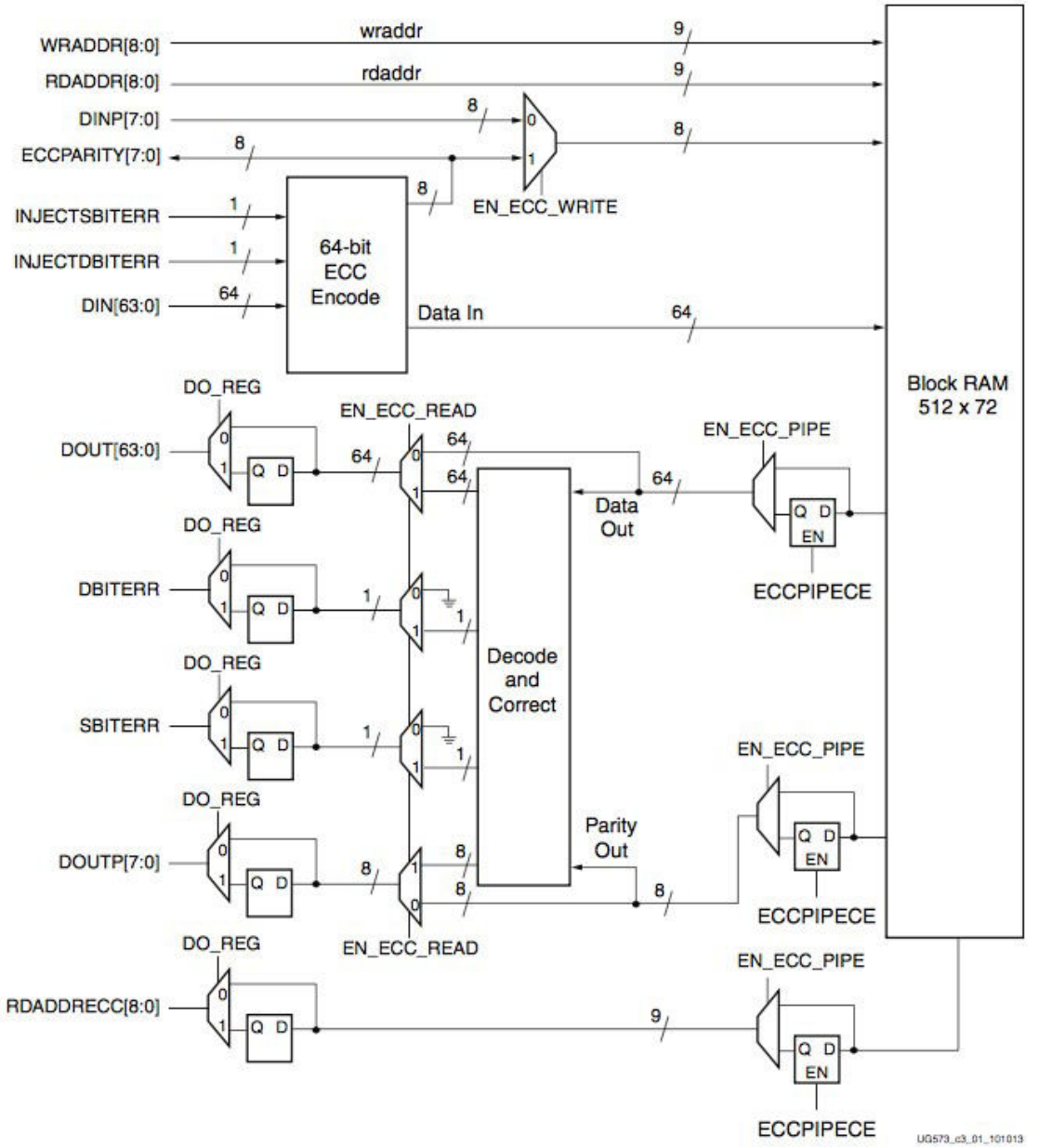
Built-in Hamming code error correction option makes possible to detect up to two-bit errors or correct one-bit errors.

- Simple Dual-Port memory
- 64 word width RAM
- Encoder / Decoder

Top-level view of the ECC Architecture

Modes:

- Standard mode
- Decoder-only mode
- Encoder-only mode
- SBITERR and DBITERR status bits
- Pipeline mode to improve maximum frequency ------>(more latency)



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Summing up

Technical evaluation of Xilinx FPGAs features can help in the future development of Pulsar II b to better achieve the high performance required:

- GTH tranceivers → *High band width*
- Block RAMs → *Huge storage data*

THANK YOU FOR YOUR ATTENTION!