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Tesi di laurea magistrale

Design and preliminary tests of the cooling system of the Mu2e electromagnetic calorimeter at Fermilab

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A nonno Piero

Abstract

Chapter 1 reports a brief description of the Mu2e physics motivation and experimental technique, a description of the Fermilab chain of accelerators and of the Mu2e experimental apparatus, including the magnetic apparatus and the detectors

Chapter 2 provides a detailed description of the Mu2e electromagnetic calorimeter, the technical specifications, the mechanics and the electronics, including the photo-sensors, the front-end electronics, and the data acquisition, power and monitoring electronics.

Chapter 3 describes my research activity, the design of the cooling system of the calorimeter electronics. Since this is a complex project, my work has been focussed on the cooling of the data acquisition electronics hosted in the DAQ crates.

Chapter 4 reports on the problem of the thermal interfaces in vacuum and the estimates of the thermal contact conductance of the relevant interfaces present in the DAQ crate thermal circuit.

Chapter 5 describes the simulation and the thermal analysis of the DAQ crates and boards, which I have performed with Ansys.

Chapter 6 reports the design of the thermal-vacuum tests required to qualify the components used in the cooling systems for vacuum operation and to perform experimental tests of the thermal simulation of the DAQ crates and boards.

Chapter 7 describes the procedures we have developed for the DAQ crates assembly and integration in the Mu2e experimental area

Chapter 8 reports the conclusions and prospects for a future development of my work .

The Appendix reports all the technical drawings of the designed components (A) and the data-sheets of the used components (D).

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Introduction

The physics motivation of the Mu2e experiment at Fermilab is the search for the neutrino-less coherent conversion of a muon to an electron in the field of an aluminum nucleus, a physics process which would be an unambiguous evidence of the existence of physics beyond the Standard Model. The experiment is currently in construction and is expected to begin data taking in the year 2020. The electromagnetic calorimeter is being designed and is going to be constructed by a collaboration among the Istituto Nazionale di Fisica Nucleare, the California Institute of Technology, and Fermilab. It is a wide collaboration which involves many groups of physicists and engineers. I have worked with the INFN Pisa, INFN-Frascati and the Fermilab groups, and I have participated to a of a lot of meetings, where I have presented the progress of my work.
The Aerospace Engineering Department of the University of Pisa and INFN have collaborated for many years on several international research projects in high energy and nuclear physics, including the Compact Muon Solenoid (CMS) and A Thoroidal LHC ApparatuS (ATLAS) at Cern, the Collider Detector at Fermilab (CDF), and Mu2e at Fermilab.
My Master Thesis research project has been the design of the cooling system of the Mu2e electromagnetic calorimeter and the development of the integration procedures in the Mu2e experimental area. I have also verified that my design provides an adequate cooling of all the electronic components for a reliable operation in vacuum. I have concluded my work with the design of the necessary tests to qualify the entire system for operation in vacuum.

Chapter 1

The Mu2e physics motivation and experimental technique

The Standard Model of particle physics provides an excellent interpretation of experimental data which has been tested to high precision and in a wide energy range [1] [2]. According to the model, the fundamental constituents of matter are quarks and leptons. Quarks combine to form composite particles called hadrons, the most stable of which are protons and neutrons, the components of atomic nuclei. Leptons exist in two main classes: charged leptons, also known as the electron-like leptons, and neutral leptons, better known as neutrinos. Charged leptons can combine with other particles to form various composite particles such as atoms. Neutrinos rarely interact with anything and are consequently rarely observed. The best known of all charged leptons is the electron. Quarks and leptons are respectively classified in three "families" or "generations", and show completely different interactions and phenomenology. Quarks are subject to strong, as well as weak and electromagnetic interactions, leptons are not subject to strong interactions. Among the three lepton families, the first generation is the electronic leptons, comprising the electron and the electron neutrino, the second is the muonic leptons, comprising the muon and the muon neutrino, and the third is the tauonic leptons, comprising the tau and the tau neutrino. The electron is a stable particle, the muon and the tau are unstable. The muon decays to a muon neutrino, an electron and an electron anti-neutrino ($\mu^- \rightarrow e^-\bar{\nu}_e\nu_\mu$) with a branching fraction of approximately 100 %. In some rarer cases, in addition to these decay products, other particles with zero net charge may be produced (e.g. a photon, or an electron-positron pair). Searches for Charged Lepton Flavor Violating processes, such as the decay $\mu \rightarrow e\gamma$, have, so far, yielded null results. This is expected within the Standard Model which predicts a probability $< 10^{-50}$ for these phenomena (Fig. 1.1).
With the current level of experimental precision, such effects are obviously well beyond our experimental reach.

Although the Standard Model has been accurately tested, it is probably and incomplete theory. Several extensions of the model include Charged Lepton Flavor Violating (CLFV) processes and allow for the neutrino-less muon

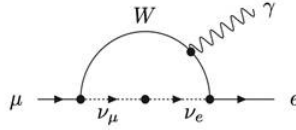


Figure 1.1: Feynman diagram for the Charged Lepton Flavor Violating muon decay $\mu \to e\gamma$.

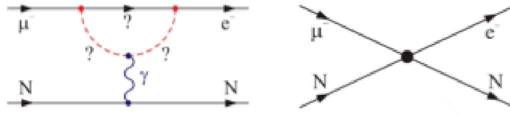


Figure 1.2: Feynman diagrams for the coherent muon conversion to electron in the electric field of a nucleus, according to Standard Model extensions which include Charged Lepton Flavor Violating processes.

conversion to an electron, in the electric field of a nucleus with rates within the reach of the next generation experiments, including Mu2e.
Mu2e has been designed and is now being constructed at Fermi National Accelerator Laboratory to search for the neutrino-less muon conversion to an electron in the field of an aluminum nucleus (Fig. 1.2). The beginning of Mu2e data taking is planned for the year 2020. The experimental signature of this process is a single mono-energetic electron with the energy of approximately the muon rest mass, 104.97 MeV. The simulation shows the Mu2e sensitivity allows to observe this process if it has a probability above 10^{-17}. In case no event is observed the limit on the probability of this process can be set at 10^{-17} which is an improvement of four orders of magnitude over current experimental limits.

1.1 The Fermilab accelerator complex

Fermilab is located about 50 km west of Chicago, Illinois. It is a US Department of Energy Laboratory and has been operated by the Universities Research Association (URA) since its founding, in 1967 [10]. Since 2007 it is operated by the Fermilab Research Alliance (FRA) a partnership of the University of Chicago and the University Research Association. The name Fermilab was given to the laboratory in 1974 in honor of the Nobel Prize-winning italian physicist Enrico Fermi [11]. Fig. 1.3 shows an aerial view of the laboratory, which has played a major role in the field of high energy physics for the last forty years. Among its scientific achievements, we can mention the discovery of three of the four particles of the third generation of the Standard Model: the bottom quark (May-June 1977), the top quark (February 1995) and the tau neutrino (July 2000) [10].

Figure 1.3: Aerial view of the Fermi National Accelerator Laboratory. The 3.2 km circumference Main Injector tunnel is visible in the foreground, the Tevatron tunnel is visible in the background. The Mu2e facility is located next to the High Rise. The Tevatron has been the most "powerful" particle accelerator for many years before the turning on of the Large Hadron Collider (LHC) at CERN in Geneva.

1.1.1 The chain of accelerators

The Fermilab accelerator complex is made of several stages. The first stage is a **Cockcroft-Walton generator**, which turns hydrogen gas into H-ions by flowing it into a container lined with molybdenum electrodes: a matchbox-sized, oval-shaped cathode and a surrounding anode, separated by 1 mm and held in place by glass ceramic insulators. A magnetron is used to generate a plasma to form H^- ions near the metal surface. A 750 keV electrostatic field is applied by the Cockcroft-Walton generator, and the ions are accelerated out of the container. The second stage is a **Linear Accelerator** (or Linac), which accelerates particles to 400 MeV, or about 70% of the speed of light. Right before entering the next accelerator, the H-ions pass through a carbon foil, which strips off the electrons thus producing a H^+ ions (i.e. protons) beam. The third stage is the **Booster ring**. The Booster ring is a 468 m circumference circular accelerator that uses magnets to bend beams of protons in a circular path. The protons coming from the Linac travel around the Booster about 20,000 times in 33 ms so that they repeatedly experience electric fields. With each revolution the protons pick up more energy, and leave the Booster with the energy of 8 GeV. Protons are injected into the **Recycler Ring** where they circulate while they are re-bounded by a 2.5 MHz frequency system. The reformatted bunches are transported to the delivery ring where they are slow extracted to the Mu2e detector through a new external beamline (1.4).

Figure 1.4: Layout of the Mu2e facility (lower right) relative to the accelerator complex that provides the proton beam to the detector. Protons are transported from the Booster through the MI-8 beamline to the Recycler Ring where they circulate while they are re-bunched by a 2.5 MHz RF system. The reformatted bunches are kicked into the P1 line and transported to the Delivery Ring where they are slow extracted to the Mu2e detector through a new external beamline. [12].

1.2 The Mu2e experimental apparatus

The Mu2e apparatus has been extensively documented in the Conceptual Design Report and Technical Design Report [14],[13]. The layout of the muon beam line and the detector system are based on the MECO design and are sketched in Fig. 1.5. The major feature of the muon beam line is the Superconducting Solenoid Magnet System. The inner bore of the solenoids is evacuated to 10^{-4} Torr in order to limit any background from muons that interact with gas particles. The Solenoid Magnet System can be schematically divided in 3 major sub-systems:

- Production Solenoid (PS)
- Transport Solenoid (TS)
- Detector Solenoid (DS)

We will give a brief description of the three elements of the Solenoid Magnet System in the next sub-sections.

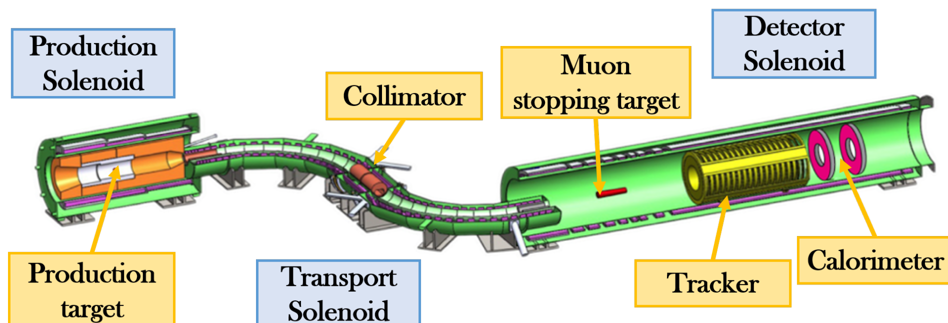


Figure 1.5: The Mu2e apparatus. The proton beam enters from the right at the junction between the Production Solenoid and the Transport Solenoid and strikes the production target. The cosmic ray veto system, which surrounds the Detector Solenoid, and the muon stopping monitor are not shown in this scheme.

1.2.1 Production Solenoid

The primary 8 GeV proton beam enters the Production Solenoid and strikes the production target located in an axial magnetic field, which decreases from 5 T to 2.5 T along the beam line. The target is a radiatively cooled tungsten target, 16 cm long and 12.6 mm in diameter. A massive concrete shield surrounding the Production Solenoid absorbs secondaries from the production target. Back-scattered muons are captured by the Production Solenoid and transported through the S-bend Transport Solenoid to the stopping target.

1.2.2 Transport Solenoid

The function of the Transport Solenoid is to transport 10^{11} muons per second to be stopped in the secondary target located in the Detector Solenoid. This beam line includes the collimators and anti-proton stopping window in the Transport Solenoid, proton and neutron absorbers, beam stop, and vacuum system. The Transport Solenoid filters the particle flux producing a momentum ($<$ 0.08 GeV/c) and charge-selected muon beam, with a good reduction of the contamination from $e^{\pm}, \mu^{+}, \pi^{\pm}, p$ and $\bar{p}$ during the detector live-time.

1.2.3 Detector Solenoid

The upstream section of the Detector Solenoid contains the muon stopping target and has a graded magnetic field, which nearly doubles the acceptance for conversion electrons and rejects certain backgrounds. The baseline aluminum target is made of 17 $\times$ 0.02 cm thick disks (Fig. 1.6). The disks are positioned parallel to each other and at the relative distance of 50 mm. The disks are centered on the Solenoid Magnet axis with each face perpendicular to it. Their radii range from 8.30 cm at the upstream end to 6.53 cm at the downstream end. The target support wires are made as thin as possible to minimize the

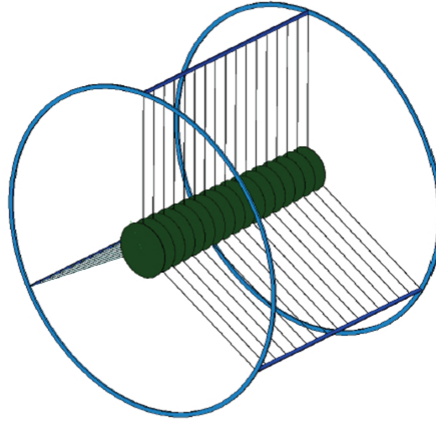


Figure 1.6: The Mu2e stopping target. It is made of 17 aluminum disks, 0.2 mm thick, spaced 5.0 cm apart along the Detector Solenoid axis. The disks radii decrease from 8.3 cm at the upstream end to 6.53 cm at the downstream end.

probability that muons may interact and stop . If muons stop in the wires at a significant distance from the solenoid axis, then low energy electrons produced in the muon decay could fall into the acceptance of the tracker and cause an undesired low energy background.The downstream section of the Detector Solenoid is occupied by the tracker and the electromagnetic calorimeter. This region has a relatively uniform magnetic field. Conversion electrons, produced in the stopping target are captured by the magnetic field within the Detector Solenoid. Then, they are transported through the tracker, which provides a precision measurement of the momentum. The conversion electrons hit the electromagnetic calorimeter, which performs an independent measurement of the electron energy and time of impact.

1.2.4 Mu2e Detectors

The Mu2e tracker and electromagnetic calorimeter are placed inside the volume of the Detector Solenoid. The Mu2e collaboration has decided to use a tracker design similar to the one developed by the MECO collaboration (Fig. 1.7). The tracker resides in a uniform 1 T solenoidal magnetic field and is kept in a 10^{-4} Torr vacuum to reduce the interaction of particles with gas to a negligible level.

This detector reconstructs particle tracks with high efficiency and measures the parameters of the helical trajectories with high resolution. Since multiple scattering in the tracker determines the resolution on the measurement of the helix parameters, the mechanical structure of the detector has to be extremely light. A further source of uncertainty is due to pattern recognition errors. This effect may produce high energy tails in the resolution function. The tracker is made of straw drift tubes and is called T-tracker because the straws are transverse to the axis of the Detector Solenoid. The basic detector element is made of a 20 μm sense wire inside a straw tube filled with gas. The straws are 5 mm diameter tubes made of 15 μm thick metallized Mylar. The tracker has ∼20,000 straws arranged into 18 measurement stations across the ∼3 m tracker length. Planes consist of two layers of straws, to improve efficiency and help overcome the classic "left-right" ambiguity. A 1 mm gap between straws allows for manufacturing tolerance and expansion due to gas pressure. A ring at large radius, outside the active detector region, supports the straws. Each straw has one preamplifier and one time to digital converter on both sides, to measure the signal arrival time on both sides, and uses also analog to digital converters for the measurement of the total integrated charge which provides useful information for particle identification. The tracker is designed so that only electrons with energy greater than approximately 53 MeV can be observed. They are approximately only 3% of the total flux of electrons from muon decays-in-orbit. Since momentum resolution is crucial to suppress several critical backgrounds, the tracker is required to have a momentum resolution better than 180 keV.

The Mu2e calorimeter provides additional energy, position, and timing information for particles that have been reconstructed by the tracker. The calorimeter and the tracker use different physical processes and technologies to perform their measurements, so the sources of error from the two systems are not correlated. This helps to reduce backgrounds and gives a cross check to verify the quality of signal events. The calorimeter operates in the same solenoidal 1 T magnetic field and 10^{-4} Torr vacuum as the tracker. It handles a large flux of particles, mostly low energy background of protons, neutrons and gamma rays produced by muon captures in the stopping target. It also handles a large flux of electrons from muons decaying in the atomic orbit in the aluminum stopping target and other particles during beam injection. A more detailed description of the calorimeter is reported in Chapter 2.

1.2.5 Cosmic ray shield

Cosmic ray muons can interact with the detector material and produce backgrounds to the search of the muon conversion signal. These backgrounds can be reduced by passive and active shields.The cosmic ray shield surrounds the entire volume occupied by the Detector Solenoid. The cosmic ray background rate will be monitored between beam spills and when the beam is off. This allows a direct measurement of the background level. The background rate will be measured as soon as the detector and detector solenoid are in place.

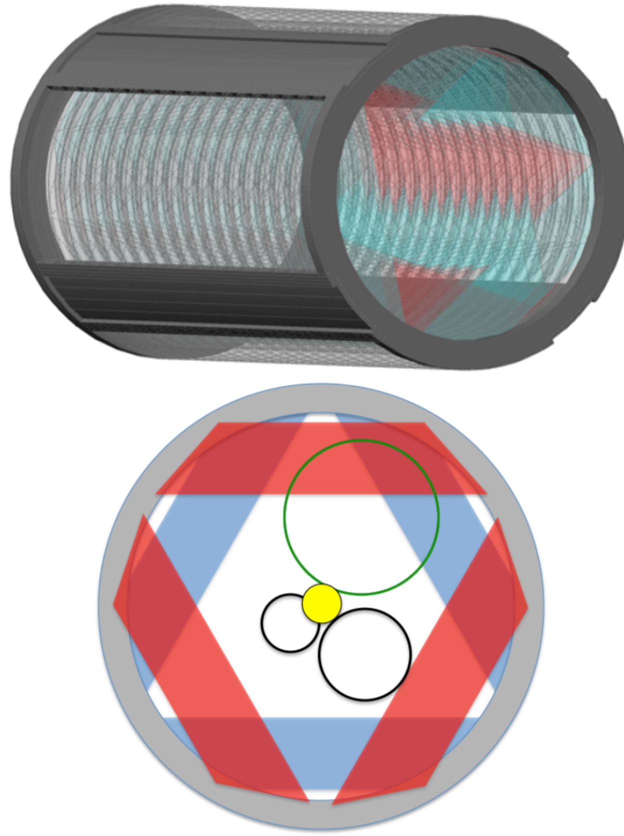


Figure 1.7: Mu2e tracker layout. The top panel displays the 18 station tracking system. The bottom panel shows a cross-sectional view of the tracker. Only electrons with energies greater than 53 MeV are reconstructed. Electrons with lower energy spiral in the uninstrumented central region.

1.2.6 Trigger and Data Acquisition

The Mu2e detectors include the Trigger and Data Acquisition (TDAQ) subsystems, which provide hardware and software to record the digitized data from the detectors. These data are delivered to online and offline processors for further analysis. The TDAQ also synchronizes and controls the detector operations. In a streaming mode, the off-detector bandwidth requirement for the DAQ is estimated to be approximately 100 GBytes/sec. The TDAQ combines information from all detector data sources and applies filters (triggers) to reduce this rate by a factor of several thousand before data can be delivered to offline storage.

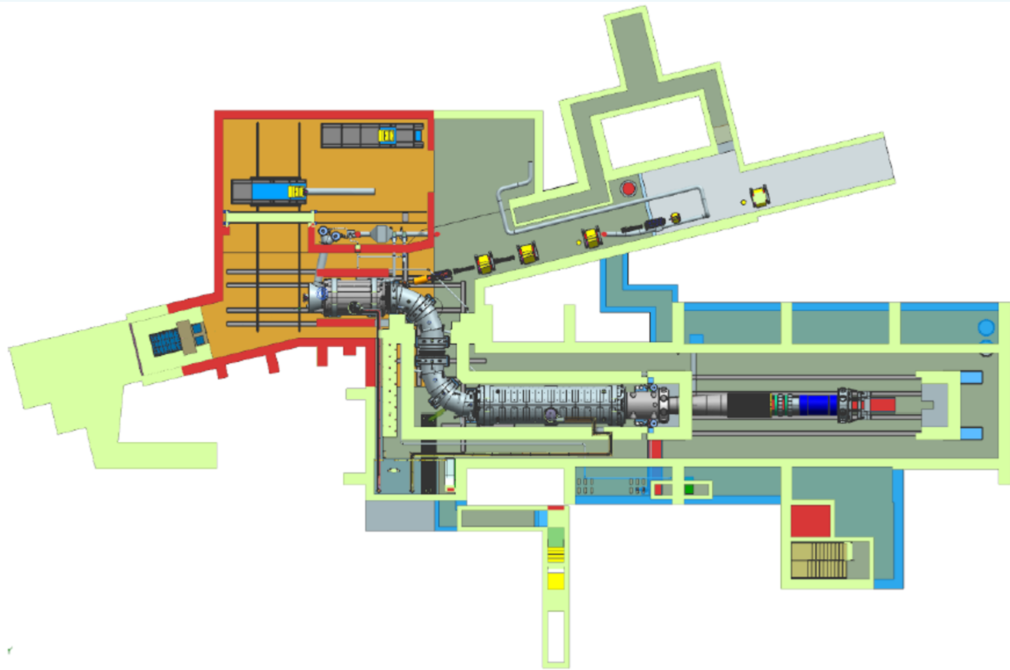


Figure 1.8: Map view of the Mu2e experimental area.

Chapter 2

The Mu2e electromagnetic calorimeter

The Mu2e detectors have been designed to reject backgrounds to a level consistent with a single event sensitivity for the $\mu \to e$ conversion of the order of 10^{-17}. The electromagnetic calorimeter is a vital link in the chain of background defenses. A background of particular concern is due to false tracks arising from pattern recognition errors that result from the high rate of hits in the tracker. Accidental hits may combine with hits from lower energy particles and erroneously create a trajectory consistent with a higher energy electron which may mimic the muon conversion signal. Thus the primary function of the Mu2e calorimeter is to provide a redundant set of measurements to complement the information from the tracker and provide sufficient information to reject backgrounds due to track reconstruction errors.

2.1 Conceptual detector design

Electrons produced in the decay of the muons stopped in the aluminum target follow helical trajectories in the solenoidal magnetic field and hit the front faces of the calorimeter crystals with a maximum energy in the 100 MeV range. In this energy regime a total absorption calorimeter employing a homogeneous continuous medium is required to meet the Mu2e energy and time resolution requirements. The sensitive material could be either a liquid, such as xenon, or a scintillating crystal. The Mu2e collaboration has chosen the scintillating crystal technology. Several types of crystals have been considered, including barium fluoride (BaF_2) and cesium iodide (CsI). The baseline design uses an array of less expensive CsI crystals arranged in two annular disks. Fig. 2.1 shows a schematic view of the detector. Photodetectors, front-end electronics and services are mounted on the rear face of the disks and are not visible. Each crystal is read out by two large-area solid-state photo-detectors (SiPM) which are necessarily preferred to standard photo-multipliers because the calorimeter operates in a 1 T magnetic field. While front-end electronics is mounted on the rear side of each disk, voltage distribution, slow control and data acquisition boards are hosted in 22 crates placed externally to the disks. A laser flasher

system provides light to each crystal for relative calibration and monitoring purposes. A circulating liquid radioactive source system provides absolute calibration and allows to determine the absolute energy scale. The crystals are supported by an aluminum structure which can be moved along the beam line on horizontal rails. The detector components are described in more detail in the following Sections.

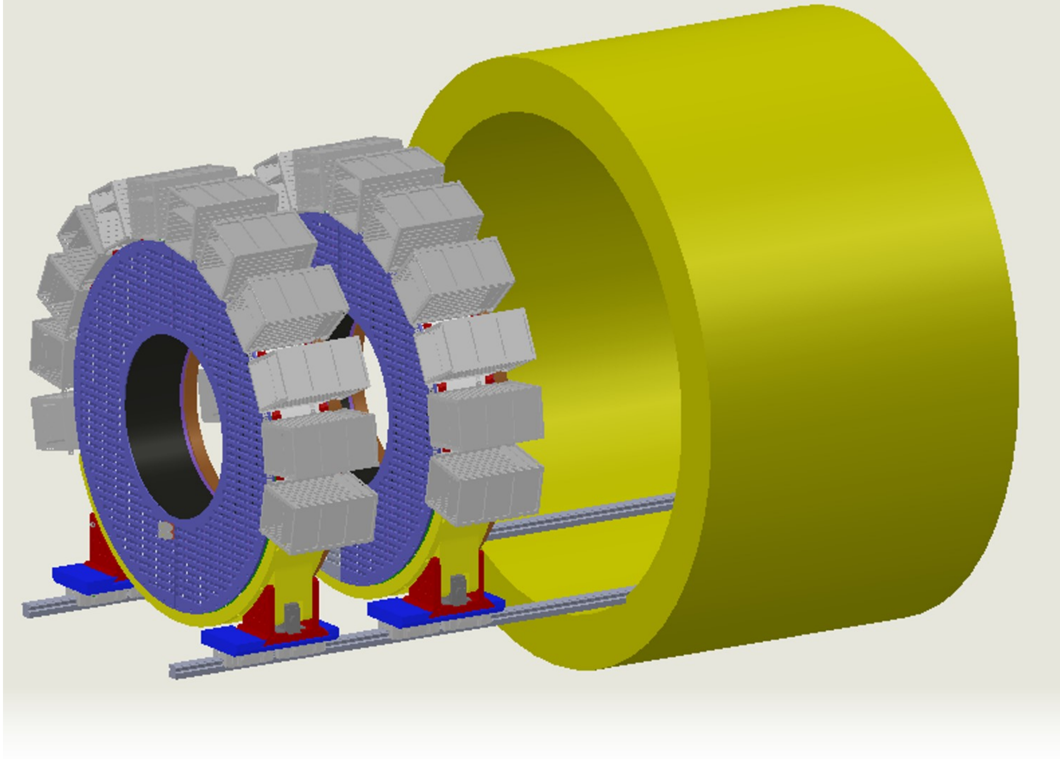


Figure 2.1: CAD model of the Mu2e electromagnetic calorimeter. The two annular disks of crystals are shown in violet; The 22 custom crates which host the boards for voltage distribution, slow controls and data acquisition are shown in grey; The calorimeter can be moved along the beamline on a horizontal rail. The cryostat walls, which surround the detector are shown in yellow.

2.2 Technical specifications

The primary function of the electromagnetic calorimeter is to measure electron energy, position and timing to confirm that particle trajectories reconstructed by the tracker are well measured and are not just the result of a spurious combination of hits. Moreover, the calorimeter provides information to the trigger for the online data selection of data. This leads to the following technical specifications [14]:

- Energy resolution of 5% at 100 MeV to confirm the electron momentum measurement performed by the tracker;

- timing resolution better than 0.5 ns to ensure that energy deposits in the calorimeter are in time with hits reconstructed in the tracker;
- position resolution better than 1 cm to allow a comparison of the position of the energy deposits to the extrapolated trajectories of the reconstructed tracks;
- the calorimeter should provide additional information useful for particle identification that can be combined with the information from the tracker to improve the muon/electron separation;
- the calorimeter should provide a trigger, either in hardware, or in software, or in firmware, that could be used to identify and select events with significant energy deposits;
- the calorimeter must operate in the hostile, high-rate, Mu2e environment and must maintain its functionality intact for radiation exposures up to 20 Gy/crystal/year and for a neutron flux equivalent to 10^{11} n_{1MeVeq}/cm^2.

2.3 Calorimeter mechanics

The two calorimeter disks are placed inside the detector solenoid (Fig. 2.1). Each disk has an inner radius of 374 mm, an outer radius of 660 mm, and is made of of 674 staggered trapezoidal crystals. The crystals are 200 mm long with a square base and a side length of 34 mm. Each crystal is wrapped with 8 layers of 25 μm thick PTFE (Teflon) reflective film to maximize light transport within the crystal and minimize cross-talk among crystals [15].
Each disk is supported by two coaxial cylinders. The inner cylinder is made of carbon fiber in order to minimize the amount of passive material in the region where spiraling electrons are mostly concentrated. The outer cylinder can be as robust as required to support the crystals load and is made of aluminum. Each disk has two cover plates. The plate facing the beam is made of low radiation length material to minimize the electron energy deposit in order to preserve the electron energy measurement. It has been designed to accomodate also the calibration source. The back plate supports the photosensors, the front-end electronics and cooling pipes and is made of plastic material. It has been designed to allow access to the front-end electronics and crystals [9]. The electronic boards which provide the power to the photo-sensors and perform digitization of the photo-sensors signals are distributed in 11 crates per disk (Fig. 2.1). Each crate houses 8 sets of boards.
In order to gain as much space as possible between the disks and allow for an easier access to the front-end electronics, we have chosen to place the crates on the external side of the disks. One crucial function of the mechanical structure is to provide adequate heat dissipation for the photo-sensors readout electronics and the electronic boards used for data acquisition, power and monitoring. This is a critical function since the calorimeter operates in vacuum and the

electronic power has to be dissipated primarily through thermal conduction. To this purpose the electronics is placed in thermal contact with structures where cooling pipes are routed. The calorimeter cooling system has its own cooling station, composed of a vacuum pump and chiller placed externally to the cryostat, designed by INFN engineers.

2.4 Calorimeter electronics

The entire calorimeter electronic system can be divided in two main subsystems, which can be ideally separated for the different functions and locations. The first subsystem is placed on the back side of the crystal disks. It contains the photo-sensors and the front-end electronics. The second subsystem is made of the electronic boards which perform the digitization of the analog signals received from the front-end electronics and provide power and monitoring to the front-end electronics. This subsystem is located on the radial external side of the calorimeter. The boards are placed in the data acquisition (DAQ) crates clearly visible in Fig. 2.1. The cooling system of the front-end electronics and of the data acquisition, power and monitoring electronics are partially independent and have been designed independently. In this Thesis we have mainly developed the cooling system of the data acquisition power and monitoring boards.

2.4.1 Photo-sensors and front-end electronics

The interaction between the electron and the crystal generates photons which diffuse through the crystal towards the photo-sensors. Every crystal has on its back side the photo-sensors which convert light into electrical signals. There are two photo-sensors per crystal electrically connected to one front-end board. The reason for having two photo-sensors per crystal is to provide a more robust measurement and to not loose data if one photo-sensor fails during data taking. The total resulting number of photo-sensors is 1348 per disk.

The front-end electronics for the calorimeter readout consists of two discrete and independent chips (Amp-HV) placed on one unique front-end board electrically connected to the back of the photo-sensor pins (Fig. 2.3 and Fig. 2.4). The two chips provide both amplification and a local linear regulation to the photo-sensor bias voltage. Groups of 16 Amp-HV chips are controlled by one dedicated ARM controller placed on one interface board placed in the DAQ crate that distributes low voltage and high voltage reference values, and sets and reads back the locally regulated voltages. The Amp-HV is a multilayer double-sided discrete component board that performs out the two tasks of amplifying the signal and providing a locally regulated bias voltage, and significantly reduces the noise loop-area. The two functions are independently executed in a single chip layer, named the Amp and HV sides, respectively. The development of the Amp-HV board has been done by the INFN Laboratori Nazionali di Frascati (LNF) Electronic Design Department. The required characteristics of the preamplifier are:

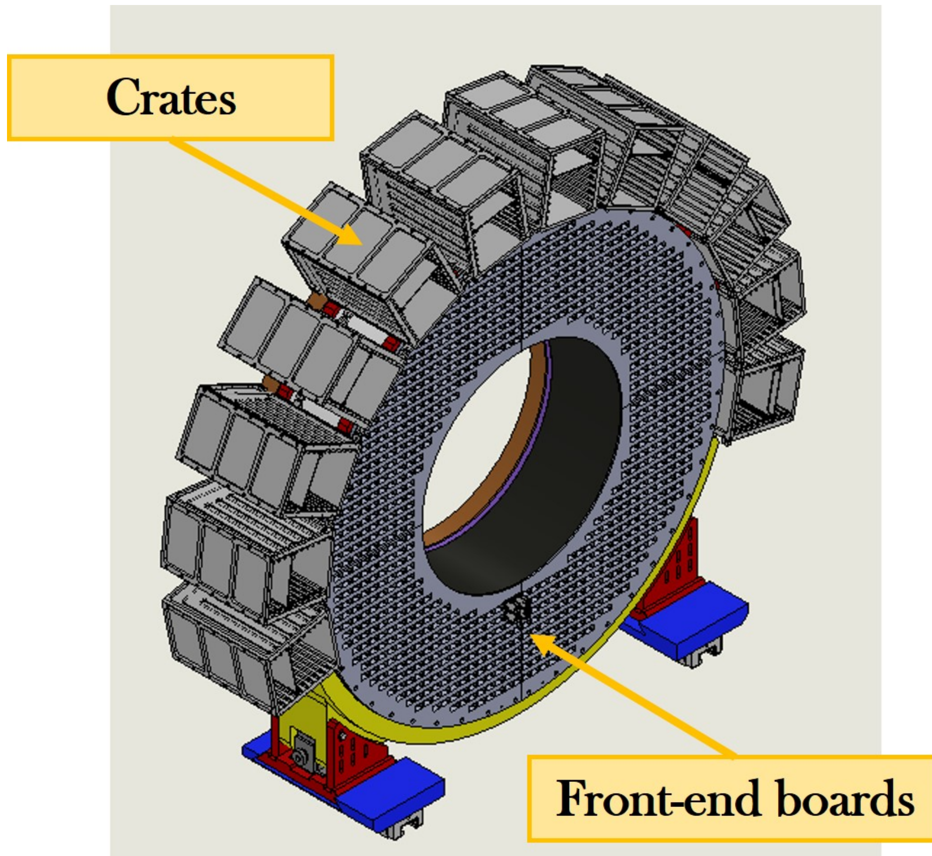


Figure 2.2: CAD model of one disk of the Mu2e calorimeter. All the cables which connect the boards hosted in the crates to the front-end electronics are not shown.

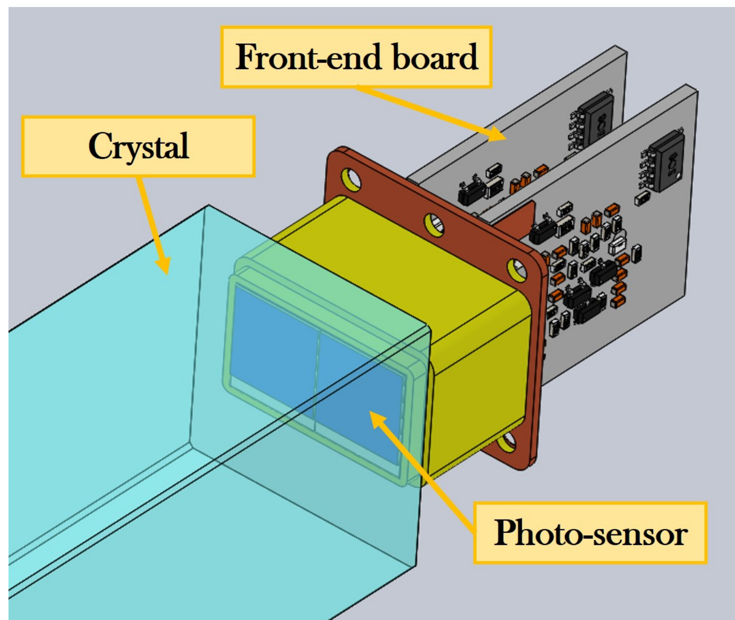


Figure 2.3: CAD model of one crystal, photo-sensor and front-end board.

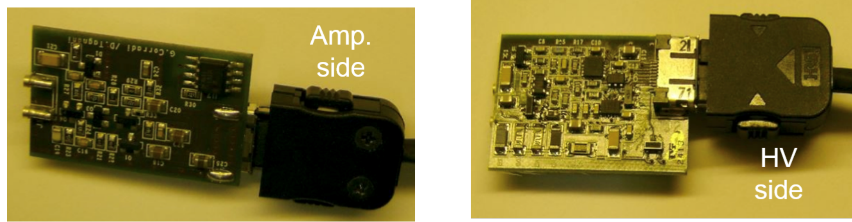


Figure 2.4: Front and rear view of one Amp-HV prototype.

- high amplification with low noise;
- fast signal rise and fall times for good time resolution and pileup rejection;
- low detection threshold at the MeV level;
- functional in a rate environment of 200 kHz/channel;
- low power consumption.

2.4.2 Data acquisition, power and monitoring electronics

The analog signals produced by the front-end electronics are transmitted to data acquisition boards hosted in the DAQ crates which are positioned on the external surface of the disks. Since the main function of the data acquisition boards is to digitize and transmit the analog signals to the global Mu2e data acquisition, these boards are named "waveform digitizers". Additional boards are necessary to provide and distribute power to the front-end boards, and to monitor the photo-sensor and front-end electronics performance. These boards are named "interface boards". There is an equal number of waveform digitizers and interface boards. Each DAQ crate hosts 7 waveform digitizers and 7 interface boards placed one next to the other. We will not describe in detail the functions of these boards, we will only list the components with significant power dissipation.
The waveform digitizer uses:

- 1 Field Programmable Gate Array (FPGA) We have chosen the FPGA FC1152 of *Microsemi* (Fig. 2.5a). It is the most complex component of the board and it processes all the analog data received from the photo-sensors. According to the data-sheet, the maximum junction temperature should be below 100°C. Since the exact amount of dissipated power depends on the number of operations the FPGA performs per unit of time, we have taken a conservative upper limit of the power dissipation at 5 W. This estimate will be verified once the firmware has been completed and implemented on the device.
- 2 DC-DC converters. The function of the DC-DC converter is to transform the voltage received from the external power supply to the values

required by the components used on the board. We have chosen a non-standard DC-DC converter with no iron-magnetic nucleus LTM8033 of *Linear Technology* (Fig. 2.5b). This has been a necessary choice, since the waveform digitizer is placed in a 1 T magnetic field, which would immediately saturate the field inside the iron nucleus of a standard DC-DC converter. Due to the absence of the iron-magnetic nucleus, this converter has a much lower efficiency than a standard device. This requires a larger power dissipation compared to a device equipped with iron-magnetic nucleus. The estimate of the dissipated power by 1 DC-DC converter is 3 W according to the data-sheet. The critical junction temperature is 125°C.

- 8 Analog to Digital Converter (ADC). The ADC converts analog signals received from the front-end boards into digital signals which are further processed by the FPGA and then transmitted to the DAQ system. We have chosen the AD9230 of *Analog Device* (Fig. 2.5c) with a relative power consumption of 470 mW per unit. The critical junction temperature is 85°C.

We have verified that the resistors and capacitors power dissipation is negligible. The total power dissipated by one waveform digitizer board is 15 W. We currently have only a conceptual design of the interface board and the choice of the components has not been finalized yet. With the current design the interface board uses:

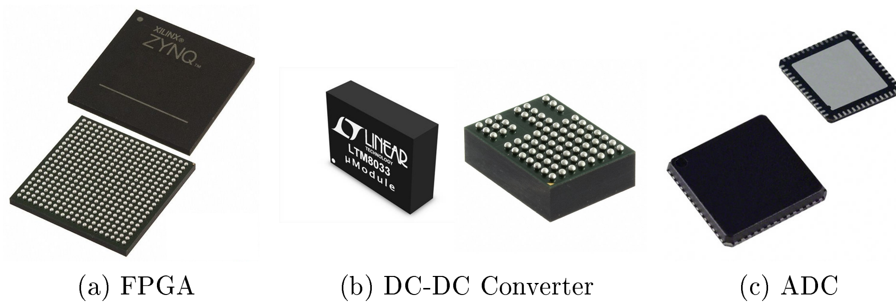
- One voltage regulator which transforms the 28 V received from the power supplies placed outside the cryostat to the 8 V used by the front-end electronics board. We expect the voltage regulator should provide approximately 1 A. A conservative estimate of the dissipated power is 10 W.

- One ARM Controller and I2C drivers which monitor the performance of the front-end electronics. We estimate a dissipated power of approximately 1 W

The total power dissipated by one interface board is approximately 11 W. Each DAQ crate hosts 7 waveform digitizers and 7 interface boards. The total dissipated power by one DAQ crate is approximately 180 W.

2.4.3 Possible options for electronic boards cooling

The first problem encountered in designing the cooling system of the electronics components has been choosing the technique to extract the power locally from the boards. There are several options and in similar projects the components are frequently cooled using a copper layer inside or at the bottom of the printed circuit board. This copper layer is in thermal contact with the electronics placed on the upper face through thermal vias (Fig. 2.6) and with some external heat sink. In some cases, the components have also dedicated pins



(a) FPGA (b) DC-DC Converter (c) ADC

Figure 2.5: The main components used on the waveform digitizer board are 1 FPGA, 2 DC-DC converters and 8 ADCs.

for heat dissipation soldered to this layer. At the board sides the copper layer emerges and is placed in thermal contact with the board lockers. In

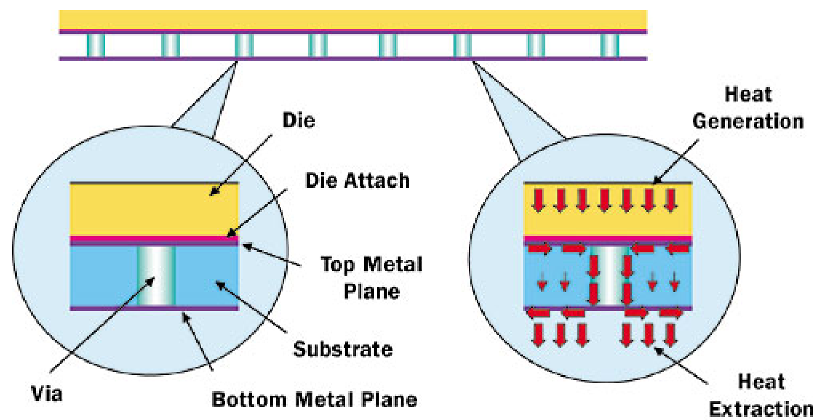
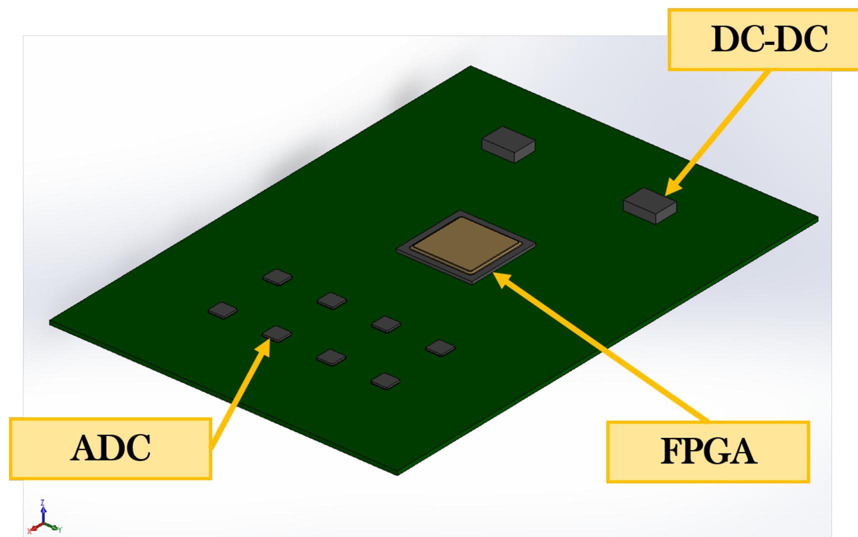
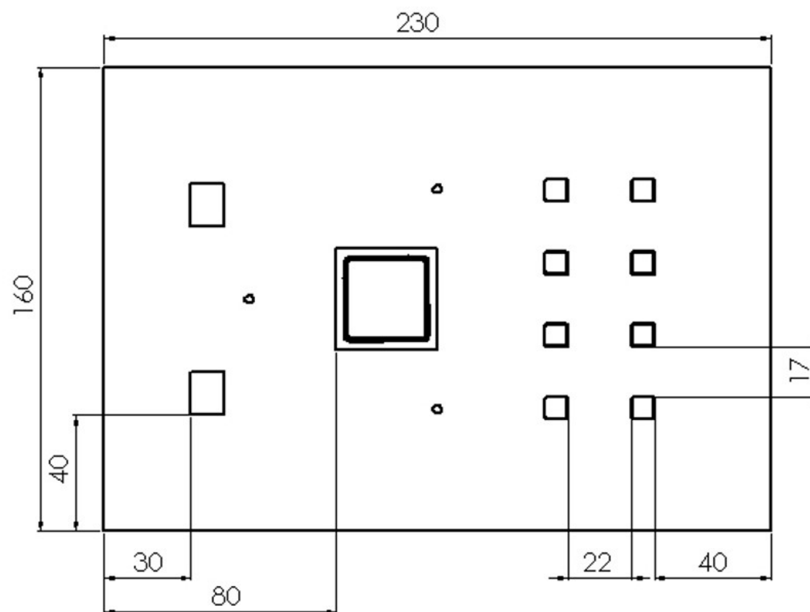


Figure 2.6: Thermal vias. A cross view of thermal vias in a PCB for heat dissipation of the electrical components.

our case, some components are incompatible with this technical solution. The FPGA and the DC-DC converters are ball grid array (BGA) components. This does not allow to cool them from the bottom. A further problem is that the ADCs have the thermal pins connected to the analog ground. To avoid electronic noise problems, we decided not to connect these pins to the the thermal ground layer. We decided to use an external thermally conductive plate placed in contact with all the electrical components which require cooling from the top side of the board. A schematic layout of the waveform digitizer board is shown in Fig. 2.7a. The placement of the components has been chosen after performing a preliminary thermal simulation. The idea has been to build a symmetric crate and to cool boards from the two sides mechanically connected to the crate walls. In order to make the best use of the cooling system, we have chosen a symmetric placement of the components on the board. A schematic layout of the interface board is shown in Figure 2.8. It is just a conceptual sketch, since the final design of this board has not been completed yet. We have chosen to spread the components on the board as much as possible to have a more uniform heat distribution and to have a simple



(a) Conceptual CAD model of the waveform digitizer board.



(b) Upper view with main quotes

Figure 2.7: Schematic waveform digitizer layout.

routing of the electronic connections on the internal layers of the printed circuit board. There are several electronic constraints to follow. The most important ones are connectors and blocking system spacing of the blocking system routing of the connection lines to the ADCs. For the first two constraints, a sufficient amount of space all around the board has been left. For the second one, all the connections among ADCs and the FPGA must have the same physical length, to guarantee the same propagation time of the signals along all the lines.
For the mechanical standard of the waveform digitizer (Fig. 2.7b) we have

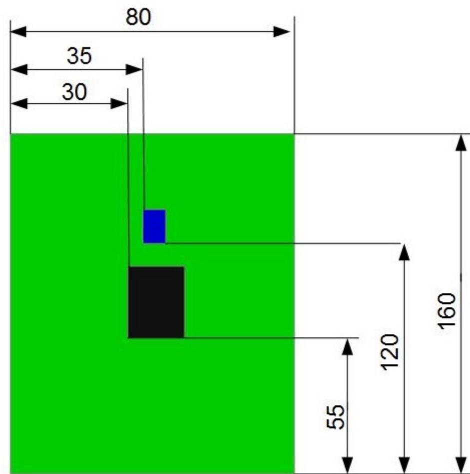


Figure 2.8: Conceptual layout of the interface board. We have reported only the voltage regulator and the ARM controller. More details about this board are not available.

chosen the 6U Standard Euroboard (160 mm x 230 mm). The size of the board grants enough space to place all the components and to route all the lines safely. Due to the limited space available in the cryostat, and to have a more efficient cooling, boards are rotated by 90°. While the Euroboards usually have the connections on the longer side, and the lockers on the shorter sides, in our case the longer sides are used to lock the boards in the proper position and to extract heat, while the shorter sides are used for the electrical connections. The design has been made in close collaboration with the INFN Pisa electronic engineers. Figure 2.8 reports a conceptual design of the interface board, which provides power to and monitors the performance of the front-end electronics. Although the choice of the components has not been defined yet, we know a custom voltage regulator and an ARM controller will be the components with the largest power consumption. Our idea is to use the same technique as for the waveform digitizer for the cooling of this board. Power will be extracted with a thermally conductive plate placed in contact with the electronic components from the top and connected to the crate walls with two cardlocks.

Chapter 3

Design of the calorimeter electronics cooling system

The design of the calorimeter cooling system has been an iterative process which has required a continuous interaction with several research groups. Italy and US are in charge of the design of the electronic components used in the detector. This design has been rather complicated also because space and resources necessary for the calorimeter cooling and services inside the cryostat are shared with other detectors, like the tracker.
The entire calorimeter electronics is divided in two main subsystems, with different functions and locations. The first subsystem is placed on the back side of the crystal disks and contains the photo-sensors and the front-end electronics. The second subsystem is located on the radial external side of the calorimeter. It contains the data acquisition, power and monitor boards. The main function of the data acquisition boards is to digitize the analog signals received from the crystals front-end electronics and transfers these data to the Mu2e data acquisition for permanent storage. These data contain the information relative to the energy and time of impact of the electrons on the calorimeter. For this reason these boards are called "waveform digitizers" in the following. The main function of the power and monitor boards is to provide the power to the front end electronics and monitor the system performance. For this reason these boards are called "interface boards" in the following. Each waveform digitizer is paired to one interface boards. They are hosted in the DAQ crates positioned on the external side of the calorimeter disks, as shown in Fig. 2.1. I have designed the entire hydraulic system external to the calorimeter, including the choice of the chiller and pumps, the manifolds which distribute the cooling fluid to the 22 DAQ crates hosting the waveform digitizers and interface boards, the DAQ crates, and the thermal circuit to extract the electronic power from the boards.

3.1 Design constraints

My Thesis has provided an acceptable solution to the groups responsible of the integration of the tracker and of the electromagnetic calorimeter. I have

verified that all the services will fit in the limited space available inside the cryostat. This work has been possible thanks to a constant interaction with the integration groups, fundamental to the progress and the development of the project. The most stringent constraints have been the available spaces (Fig. 3.1) and the operational conditions of the coolant fluid. The refrigerating system is located inside the cryostat and has to leave sufficient space to the other services, including cables and vacuum pumping. The main function of the cooling system is to keep the temperature of all the electronic components below the critical values, since temperatures above these values would cause irreversible damage and reduce the reliability and the expected lifetime of the components. For all the electronic components placed inside the cryostat, at the vacuum level of 10^{-4}torr, all the dissipated power has to be removed by conduction through a cooling fluid.
In all our calculations heat transfer due to thermal irradiation has been neglected with respect to the forced convection. This approximation is justified by comparing the temperatures and sizes of the radiating surfaces to the parameter which determine the amount of power transferred by conduction, i.e. forced film coefficient and heat transfer areas.

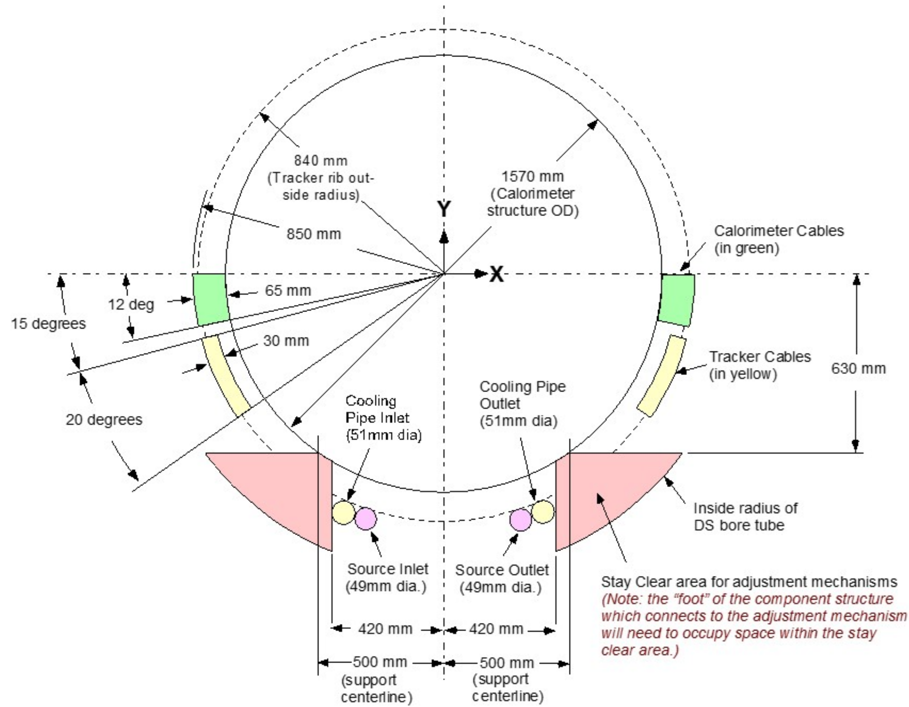


Figure 3.1: Schematic view of the calorimeter dimensions and of the services, of the calorimeter cables and cooling pipes.

3.2 Photosensors and front-end electronics

The main problem of the front-end electronics cooling system is that the maximum operational temperature of the SiPM should be approximately $0°C$.

Figures 3.2 and 3.3 show a preliminary design of the front-end electronics cooling system, made of a structure of pipes in thermal contact with the copper mechanical structure which supports SiPM and the boards. We have estimated that with the limited power dissipated by the electronic components, a flux of cooling fluid at -5 ° C allows to keep the SiPM at the operational temperature of 0°C. The design of the cooling system of the front-end electronics is the topic of a Master Thesis of a student in Aeronautical Engineering at the University of Pisa. The conclusion of this project is expected for autumn 2016.

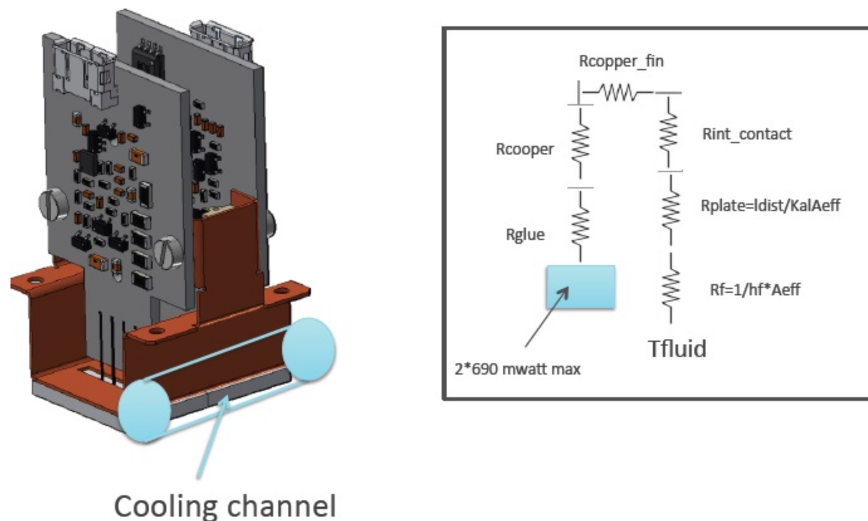


Figure 3.2: (Left) Schematic design of the SiPM, front-end boards and mechanical supports; (Right) Schematic view of the equivalent thermal circuit of the SiPM and front-end electronics.

3.3 Data acquisition and interface boards

Each DAQ crate hosts 7 pairs of waveform digitizer and interface boards and one board dedicated to the clock distribution. Fig. 3.5 shows a view of one crate. The main electronic components installed on the waveform digitizer are:

- 1 FPGA, 5 W;
- 2 DC-DC converter 2x3 W;
- 8 ADC, 8x0.5 W.

These are the main components of the thermal circuit:

- thermal pads (Figure 3.6). They are necessary in order to guarantee a good thermal contact between the electronic components and the aluminum plate. It would be possible to press the plate to the package

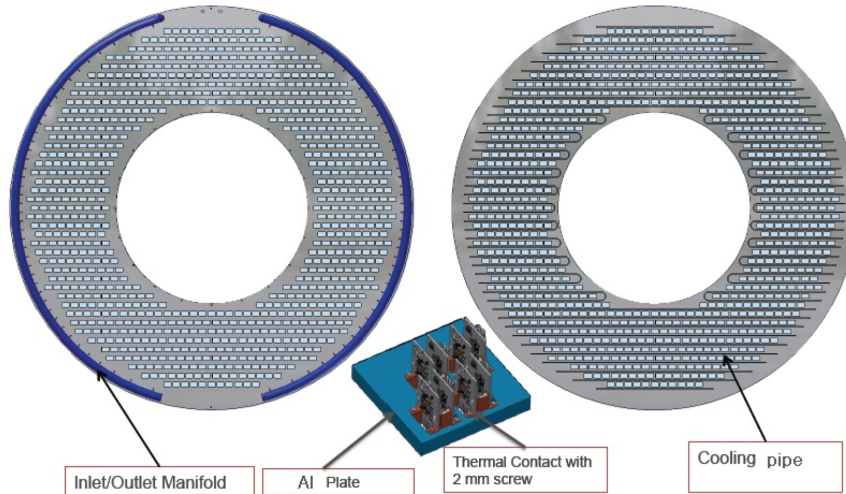


Figure 3.3: Schematic design of the front-end plate which provides the mechanical support to the front-end electronics boards. A structure of cooling pipes is routed in the space available in the front-end plate and is placed in contact with the copper mechanical supports of the front-end boards.

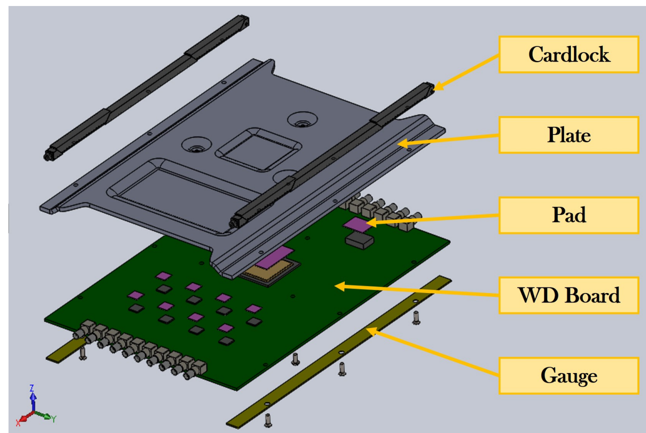


Figure 3.4: View of the waveform digitizer board. Heat is produced by electronic electronics and is dissipated through thermal path, composed of thermal pads, an aluminum plate, glue, cardlocks, the DAQ crate walls and the cooling pipe.

mechanically, but it would be more complicated.
The main requirements of the thermal pads are low outgassing and low thermal resistance, properties that are verified by Ultra-soft ASKER C 8 silicone free thermal pads.

- aluminum plate. This component is shaped in order to push down on the electronic components (Fig. 3.7) and has the function of heat sink ;
- cardlocks (Figure 3.8). To hold the waveform digitizer and the interface boards into the DAQ crate we have used a set of cardlocks. They have good thermal properties and they are qualified for vacuum. A descrip-

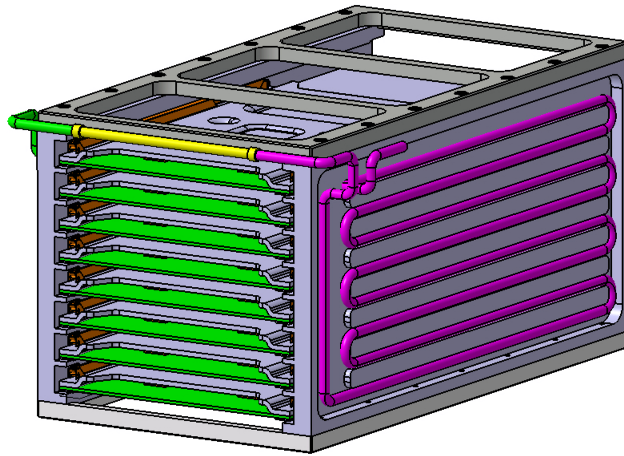


Figure 3.5: View of the DAQ crate with the 7 waveform digitizer and interface boards and one clock distribution board. Power is produced by the electronic components and removed by the cooling fluid flowing inside the pipe. Heat is extracted by conduction through the thermal circuit composed of the thermal pads, the aluminum plate, the cardlocks, the crate walls and the cooling fluid flowing into the pipe.

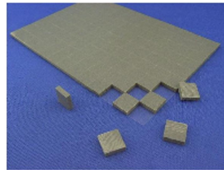


Figure 3.6: Ultra-soft ASKER C 8 silicone free thermal pads.

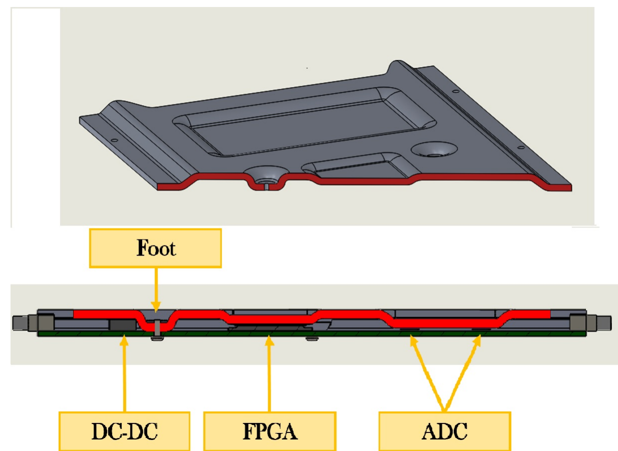


Figure 3.7: Section of the aluminum plate ([9]).

tion of the cardlock mounting and dismounting procedure is reported in Chapter 7 ;

- DAQ crate wall. The space constraints inside the cryostat have forced

Figure 3.8: View of Calamark cardlock series 265.

to us to design a customized DAQ crate. The cooling pipe is brazed on the external surface of this component

- cooling pipe. Its shape satisfies the space constraint and guarantees the integration of the crates with the cooling line. Figure 3.9 shows the cooling pipe housed inside the crate wall. The procedure to determine the pipe size is reported in Chapter 3. ;

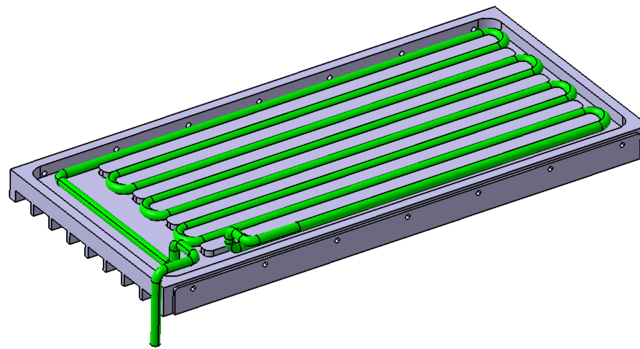


Figure 3.9: View of the one DAQ crate wall and of the cooling pipe.

A well known problem of thermal conduction in vacuum is due to the thermal interfaces, i.e. thermal contact resistances between adjacent surfaces which may be significantly increased with respect to the atmospheric pressure conditions. For this reason we have performed an accurate study in vacuum of all the interfaces present in the thermal circuit. This study is reported in Chapter 4. The main electronic components used in the interface board are:

- 1 ARM controller, with a power dissipation of 0.5 W;
- 1 voltage regulator, with a power dissipation 10 W.

At the moment of writing this Thesis the design of the interface board exists only at a conceptual level and the choice of the electronic components has not been finalized yet. This does not allow to perform a detailed design of the cooling system of this board, but we plan to use a similar technique as for the waveform digitizer board, with an aluminum plate and cardlocks.
The total power dissipated by one waveform digitizer and one interface board

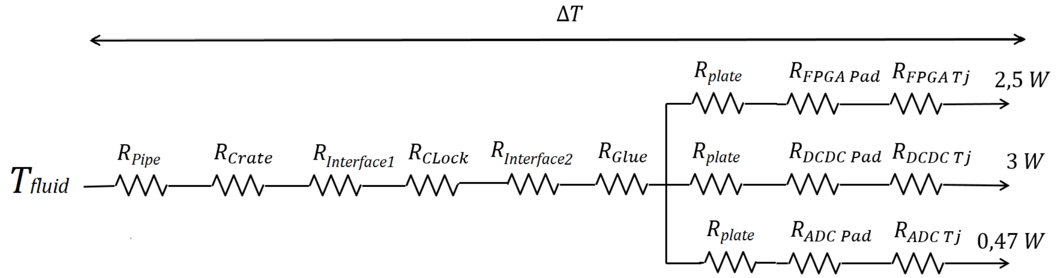


Figure 3.10: Simplified view of the thermal circuit which extracts the dissipated power from the electronic components of the waveform digitizer board.

is approximately 25.5 W. Since there are 7 waveform digitizers and 7 interface boards in one DAQ crate, the total power dissipated in one crate is approximately 180 W. We have neglected the power dissipated by the clock distribution board, since we know it is extremely limited.

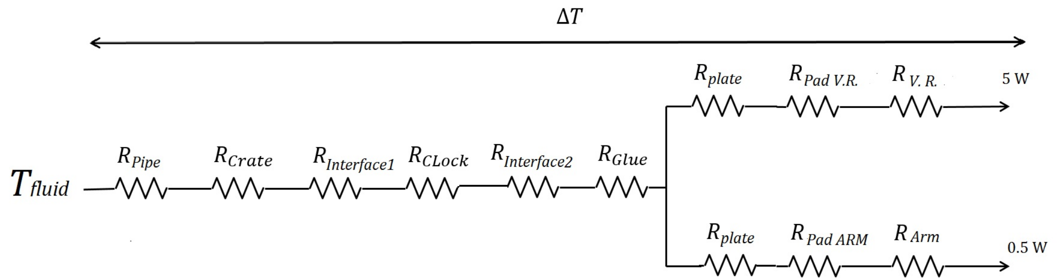


Figure 3.11: Simplified view of the thermal circuit which extracts the dissipated power from the electronic components of the interface board.

3.3.1 Choice of the cooling fluid

We have performed a detailed study of the properties of the several commercially available refrigerant fluids.
For our choice we have taken into account the following parameters:

- cost;

- corrosion properties;
- required pumping power;
- thermal properties.

Several cooling fluids can be used between 0 and -10 $°C$. Water unfortunately cannot be used. We have chosen a 35% monopropylene glycol aqueous solution, which has excellent thermal properties and a limited cost. Table 3.1 reports a summary of the cooling fluid thermal properties.

Table 3.1: Properties for 35% monopropylene glycol aqueous solution.

Property	**Value**
Density $\left[\frac{kg}{m^3}\right]$	1038
Specific heat $\left[\frac{J}{kg \cdot K}\right]$	3767
Dynamic viscosity $[Pa \cdot s]$	0.003588
Thermal conductivity $\left[\frac{W}{m \cdot K}\right]$	0.432
Freezing point	[-17 ° C]

3.3.2 Dimensioning the cooling pipe

Each crate hosts 7 pairs of waveform digitizer and interface boards. A conservative estimate of the total power dissipated in one crate is approximately 180 W but we prefer to add a safety factor of 1.5 in our calculations and we dimension the cooling pipe for a dissipation of 270 W.
Extracting the dissipated power from the crate with a cooling fluid is a forced convection problem, where the internal diameter of the pipe is the unknown variable. We have used an iterative approach, in order to optimize pipe dimensions, fluid dynamics properties of the fluid and thermal requirements.
Let us call $\dot{m}$ the mass flow rate, C_P the specific heat capacity of the 35% monopropylene glycol and $\triangle T$ the temperature difference between the output and the input fluid. We have to verify that:

$$Q_{Tot} = \dot{m} \cdot C_P \cdot \triangle T = 270\ W \tag{3.1}$$

This equation has ∞^2 solutions, which depend on the possible choices of $\dot{m}$ and $\triangle T$.
We have chosen to fix the upper limit of the thermal drop $\triangle T \leq 3°C$. Under this condition, we can assume that along each straight portion of the pipeline (which approximately corresponds to one board side) the temperature is constant. After the optimization of these parameters we have decided to fix the thermal drop $\triangle T \approx 2.25°C$ therefore

$$\dot{m} = \frac{Q_{Tot}}{C_P \cdot \triangle T} \approx 0,04\ \frac{kg}{s} \tag{3.2}$$

Pipe dimensions have been defined by the continuity equation.

$$\dot{m} = \rho \cdot U \cdot A = \rho \cdot U \cdot \frac{\pi d^2}{4} \tag{3.3}$$

We have chosen an average velocity of the fluid inside the pipe of approximately 3 m/s. This value guarantees an adequate Reynolds number (≥ 3000) and allows to have a fully developed turbulent flow. We also know that the Reynolds number should not be too high because pressure losses depend significantly on the average fluid velocity. Equation 3.3, allows to estimate the internal diameter of the pipeline:

$$d = 4\ mm$$

The Reynolds number is estimated with the following equation:

$$Re = \frac{\rho U d}{\mu} \approx 3615$$

where ρ is the Ethylene Glycol density in liquid state at the temperature of $-5°C$, U is the average velocity of the fluid in the pipe, d is the inner diameter and μ is the viscosity of the fluid in the liquid state at $-5°C$. Given the estimated Reynolds number, we can assume a fully developed turbolent flow.
The resulting Prandtl number is:

$$Pr = \frac{c\mu}{k} \approx 23$$

where c is the specific heat [J/kg K], and k is the thermal conductivity [W/m K] of the fluid at $-5°C$.
The resulting Nusselt number:

$$Nu = 0.023 Re^{0.8} Pr^{0.3} \approx 236$$

We can estimate the value of the *film coefficient* using Dittus-Boelter equation for turbulent flow.
The resulting heat transfer coefficient is

$$h = \frac{Nuk}{\Phi} \approx 4751\ \frac{W}{mK}$$

3.4 Estimate of the pressure losses along the circuit

In order to characterize the hydraulic plant and select the specifications of the cooling pumps, we have estimated the pressure losses in the circuit brazed to the DAQ crate walls. In Section 3.6 we will also estimate the pressure losses in the dividing manifold.
The change of the static pressure for an incompressible flow through a pipe can be expressed by the equation:

$$p_1 - p_2 = \frac{1}{2}\rho(U_1^2 - U_2^2) + \frac{1}{2}\rho U^2 K + \rho g (z_2 - z_1) \tag{3.4}$$

where

- p is the static pressure
- ρ is the fluid density
- U is the average fluid velocity
- K is the irreversible loss coefficient
- g is the gravitational acceleration
- z is the elevation

Since $z_1 = z_2$ the hydrostatic component can be neglected. For a steady incompressible flow through a pipeline, the loss coefficient K can be expressed as a function of the Reynolds number and geometry (surface roughness, area change, bend radius etc.) of the component:

$$K = F(Re, geometry) \tag{3.5}$$

Since there are no area changes along the line:

$$\rho \cdot A \cdot U_1 = \rho \cdot A \cdot U_2 \tag{3.6}$$

and $U_1 = U_2 = U$, therefore equation 3.4 can be written as follows:

$$\Delta P = \frac{1}{2} \cdot \rho \cdot U^2 \cdot K = \frac{1}{2} \cdot \rho \cdot U^2 \cdot \frac{fL}{d} \tag{3.7}$$

where three new parameters, f, L, d, have been introduced. The dimensionless friction factor for turbolent flow f is a function of $f = F(Re, \epsilon/d)$ where ϵ/d is the pipe relative roughness.
L is the distance along the pipe span separating the two points where ΔP is evaluated and d is the hydraulic diameter (of course, in our case, d is the inner pipe diameter).
The total pressure loss ΔP is the sum of the losses due to the pipe spans upstream and downstream the bend, and the localized pressure losses due to the bends, as shown in equation 3.8

$$\triangle P = \underbrace{\rho \cdot f \cdot \frac{L}{d} \cdot \frac{U^2}{2}}_{Pressure\ loss\ along\ pipe} + \underbrace{\sum_{bends} \rho \cdot K_c \cdot \frac{U^2}{2}}_{Localized\ pressure\ loss} \tag{3.8}$$

3.4.1 The friction factor

The friction factor f for turbolent flow can be analytically estimated using the *Colebrook-White* correlation:

$$\frac{1}{f^{1/2}} = 1.74 - 2log_{10}\left(\frac{2\epsilon}{d} + \frac{18.7}{f^{1/2}Re}\right) \tag{3.9}$$

and the solution of this transcendental equation is plotted on Moody's diagram, Figure 3.12

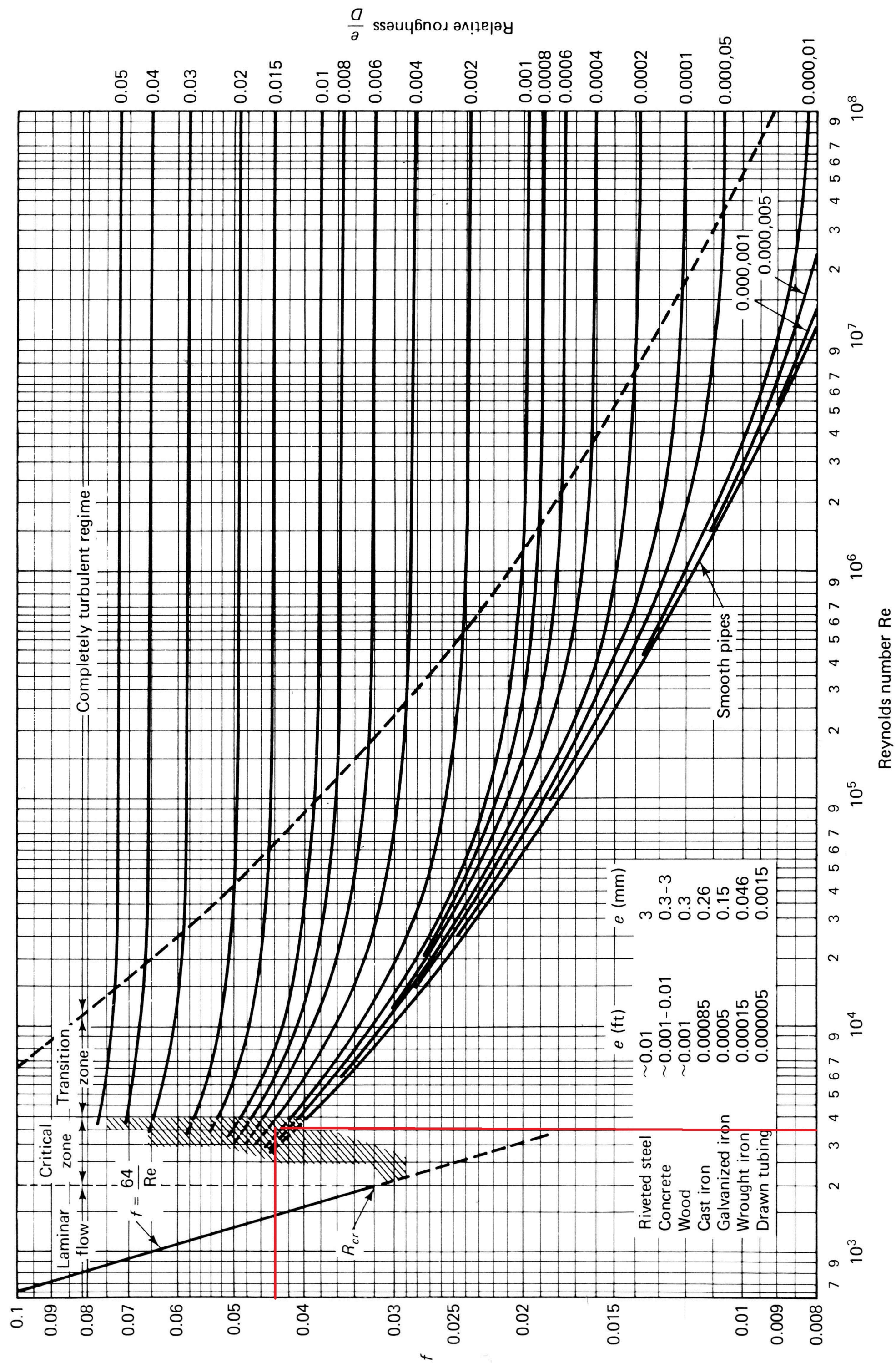


Figure 3.12: Moody's diagram. On the x-axis is reported the Reynolds number, on the y-axis is reported the friction factor.

However, to estimate the friction factor as a function of each parameter, a simplified approximate equation 3.10 has been used

$$f = \left[1.14 - 2 \cdot log\left(\frac{\epsilon}{d} + \frac{21.25}{Re^{0.9}}\right)\right]^{-2} \approx 0.042 \tag{3.10}$$

We have verified that equation 3.10 is within 0.4% of the *Colebrook-White* correlation. According to the experimental evidence [3] the value of the equivalent surface roughness set in equation 3.10 is:

$$\epsilon \approx 0.006\ mm$$

3.4.2 Distributed pressure losses

As shown in equation 3.8, this term for relatively long pipes can be calculated as follows:

$$\triangle P = \rho \cdot f \cdot \frac{L}{d} \cdot \frac{U^2}{2} \approx 2.85\ bar \tag{3.11}$$

Where L is the pipeline length for a crate and d is the inner diameter.

3.4.3 Localized pressure losses

The localized pressure losses have been estimated using the equation:

$$\sum_{bends,180} \rho \cdot K_{c,180} \cdot \frac{U^2}{2} \approx 0.35\ bar \tag{3.12}$$

where $K_{c,180} = 0.44$ is the dimensionless loss coefficient for 180° bends [3].

$$\sum_{bends,90} \rho \cdot K_{c,90} \cdot \frac{U^2}{2} \approx 0.2\ bar \tag{3.13}$$

where $K_{c,90} = 0.35$ is the dimensionless loss coefficient for 90° bends [3].
The total pressure drop expressed by equation 3.8 is

$$\Delta P \approx 3.40\ bar$$

for one crate.

3.5 Experimental measurement of the pressure losses

In order to test the predictions of the analytical model described in the previous Section, we have measured the pressure losses in one crate circuit at the INFN Pisa laboratory.
We have measured the pressure drop of *Monopropylene glycol* between the inlet and outlet of the pipeline using two static pressure sensors. Measurements have been performed at the temperature of -5 ° C, at fixed values of the flow rate. The prototype of the DAQ crate has been connected to the experimental apparatus by two VCR swagelock (Fig. 3.14).

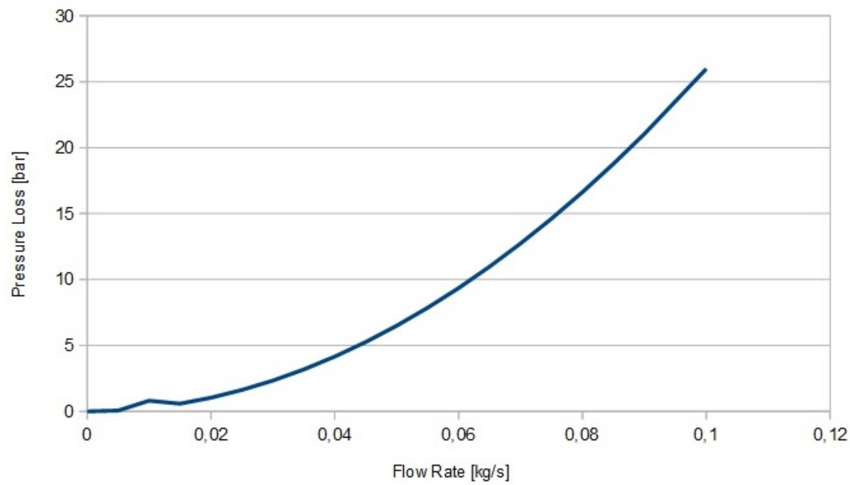


Figure 3.13: Analytical estimate of the pressure losses as a function of flow rate. The pressure loss (bar) is reported on the y-axis, the flow rate (kg/s) is reported on the x-axis.

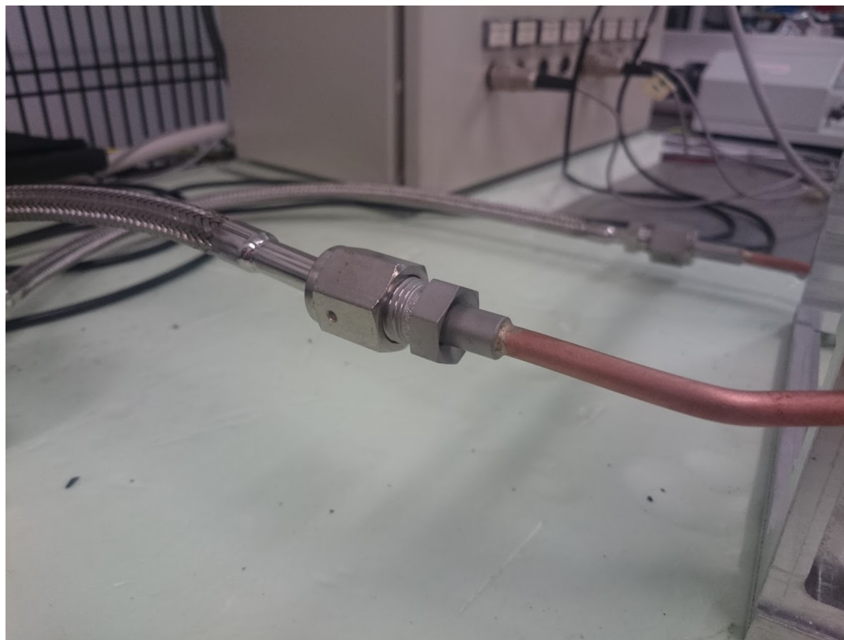


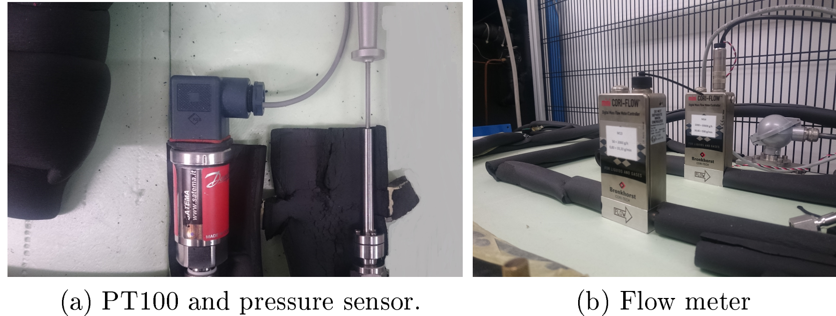
Figure 3.14: Connection between the DAQ crate and the hydraulic system.

3.5.1 Experimental setup

The goal of the experimental test is to measure the pressure drop between the inlet and outlet of one single crate, in order to confirm the values of the pressure losses estimated with the analytical model. The tests have been performed at the INFN Pisa laboratory using the prototype built by the INFN Pisa workshop. We have used the following sensors to perform the measurements:

- *Danfoss* pressure transmitter **AKS 33**. This sensor is optimized for refrigeration plant (Fig. 3.15a);

- *PT100* temperature sensor
- *SATEMA ACM 300* flow meter Figure 3.15b.



(a) PT100 and pressure sensor. (b) Flow meter

Figure 3.15: Instrumentation used for the tests.

Signals have been acquired by *SENECA Z-4RTD2* and *SENECA Z-4AI* modules and sent to a CPU *Telemecanique*.
The transmission of the data from the CPU to a PC has been performed through a serial port RS232. Data have been analyzed and plotted using the software *Movicon11*. Figure 3.16 shows the schematic experimental setup used to perform these tests.

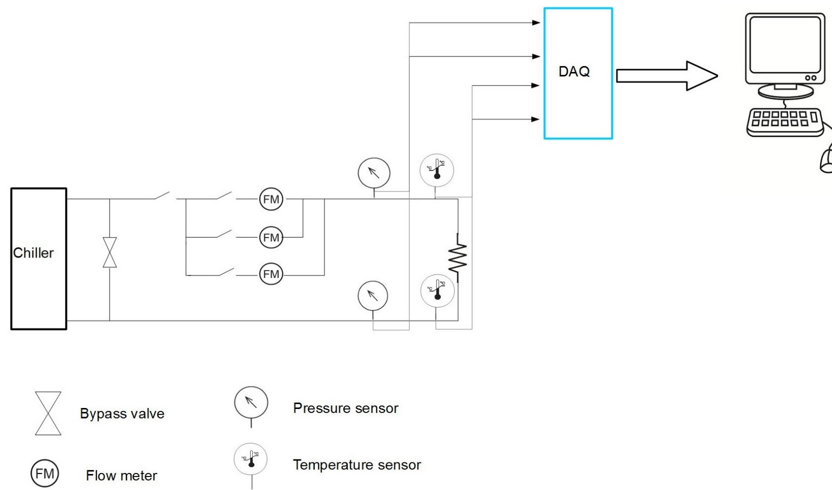


Figure 3.16: Experimental setup for the measurement of the pressure losses.

Best fit equation is a second order polynomial and can be written as follows:

$$\Delta P(G) = 0.32G^2 + 0.65G \tag{3.14}$$

Since we are going to work at fixed flow rate of 2.4 kg/min, the experimental pressure loss is

$$\Delta P = 3.28 \pm 0.1 \; bar$$

This can be compared to the analytical estimate of the pressure losses

$$\Delta P \approx 3.40\ bar$$

Figure 3.17 reports the measured data with a fit to a quadratic form. The

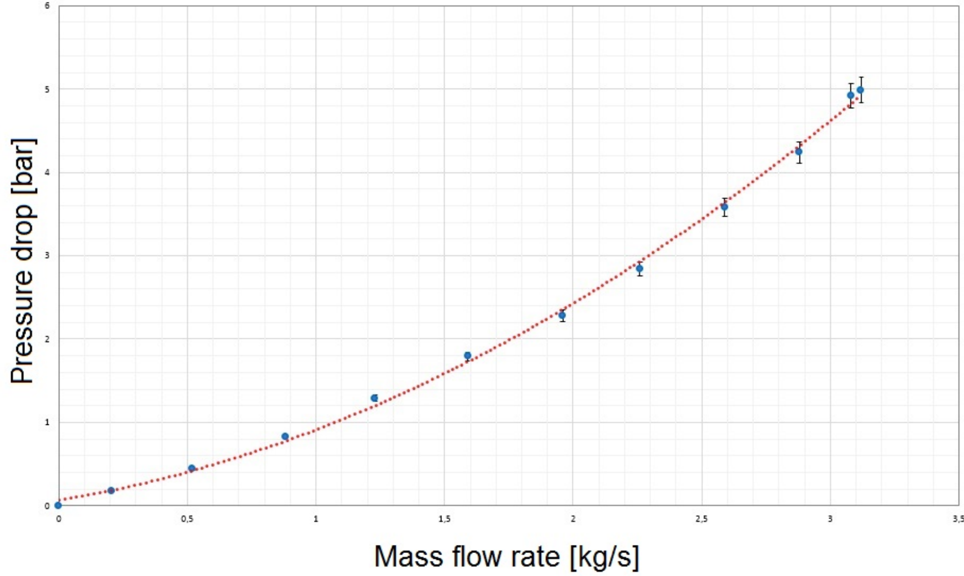


Figure 3.17: Best fit of the measured pressure losses as a function of flow rate for one crate.

fractional discrepancy between the analytical model and experimental model is about 2.4 %. We are convinced that the analytical model for pressure losses for each crate has been confirmed and can be used in order to estimate the global pressure losses which we need to design the hydraulic plant.

3.6 Design of the dividing manifold

The cooling fluid flowing through the 11 DAQ crates installed on each calorimeter disk is provided and received by two dividing manifolds positioned on the external surface of the calorimeter disk.
After an accurate study of the fluid parameter we have chosen the internal diameter of the stainless steel main pipe $D_{manifold} = 1'' \approx 25.4\ mm$

The function of the dividing manifold is to guarantee a uniform flow of the cooling fluid into the branches at the approximately constant average velocity of the cooling fluid, u_b.
Assuming that the pressure losses along main pipe are negligible ($(A/A_b)^2 \gg 1$) with respect to the localized pressure losses, the pressure loss before and after each branch is the same. For this reason, the flow velocity into each branch is constant. As it has been explained before we want an average fluid

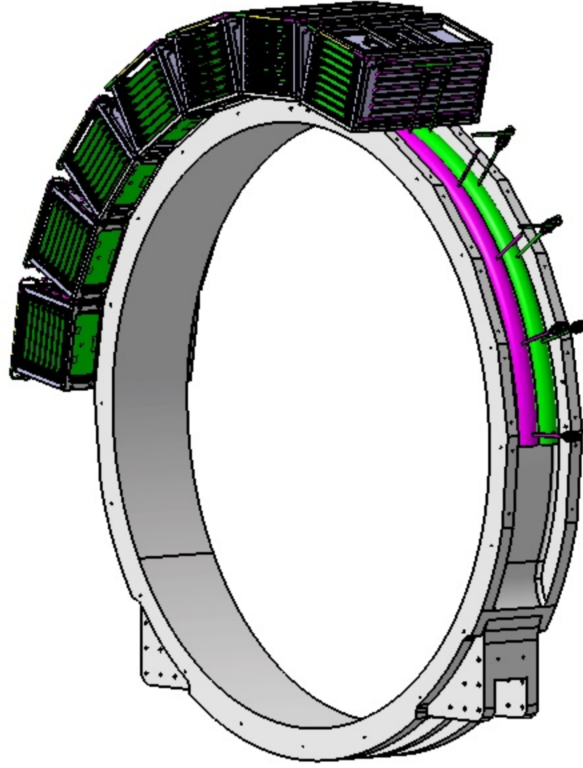


Figure 3.18: Architecture of the dividing manifold which provide and receive the cooling fluid of the 11 DAQ crates.

velocity of approximately 3 m/s, so the problem is reduced to determining the velocity at the entrance of the main pipe by using the continuity equation.

$$U = u_b \cdot \frac{d}{D_{manifold}} \sqrt{11} \approx 1.5 \; m/s \tag{3.15}$$

3.6.1 Estimate of the pressure losses

For the dividing manifold, let us consider a generic branch. Neglecting the pressure losses along the pipe, we can write:

$$p_i - p_j = \frac{1}{2} \rho u_b^2 K_{i,j} - \frac{1}{2} \rho \left(U_i - U_j\right)^2 \approx 0,4 \; bar \tag{3.16}$$

where:

- p_i is the static pressure before the branch;
- p_j is the static pressure after the branch;
- u_b is the velocity into the branch, as already said it has been fixed at 3 m/s;

- $U_i - U_j$ is the velocity variation before and after the branch. For the continuity equation, and neglecting pressure losses along pipe this value is constant for each branch;

- $K_{i,j}$ is the loss coefficient. We have assumed $K_{i,j} = 0,5$ in agreement with the experimental correlation [3].

The INFN mechanical workshop is now working on the fabrication of the one prototype of the designed dividing manifold to perform an experimental verification of the estimated pressure losses.

3.7 Technical specification of the cooling station

INFN is responsible also of the design of the cooling station which provides the refrigerant fluid for the cooling of the entire calorimeter. Requirements for the cooling line are reported in the Table 3.2.

Technical specification	
Cooling fluid	35% monopropylene glycol
Fluid temperature	-5 $°C$
Flow rate	2,4 kg/s
Velocity of entrance in dividing manifold	1,54 m/s
Global pressure losses	5 bar

Table 3.2: Technical specification and parameters of the cooling fluid.

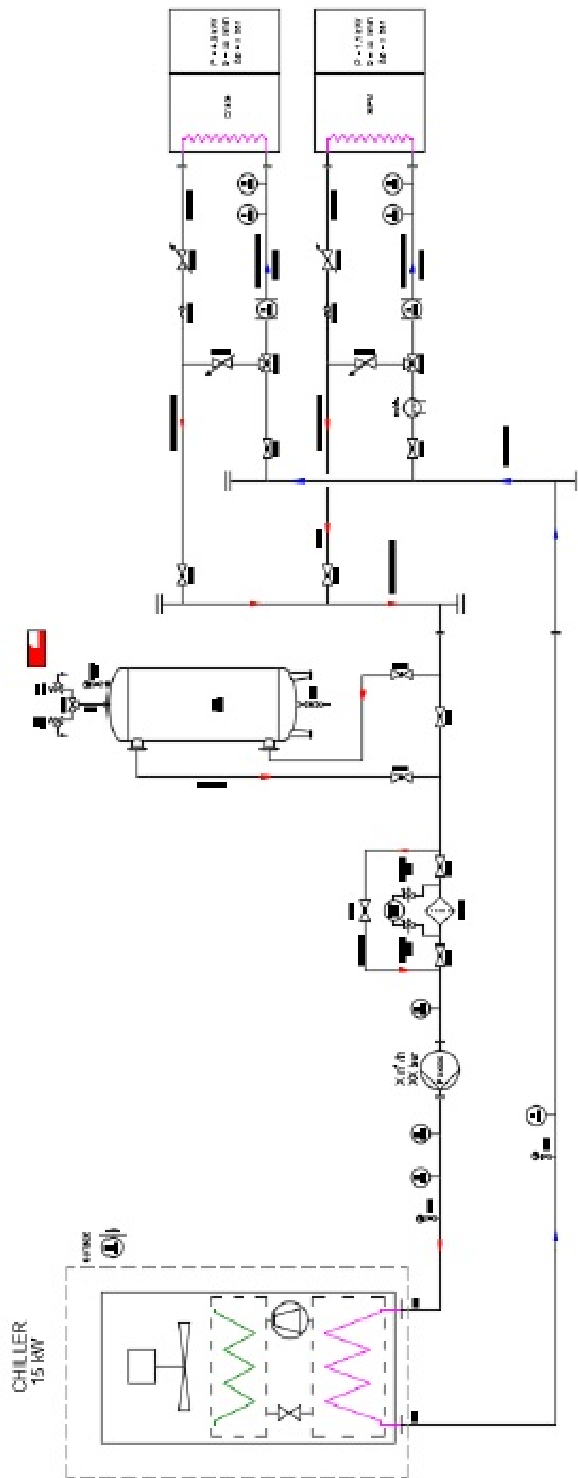


Figure 3.19: Conceptual design of the calorimeter cooling station.

Chapter 4

The problem of thermal interfaces in vacuum

In a thermal circuit operating in vacuum the heat flow through the interfaces between all the components of the circuit has to be carefully checked. This is extremely important, since the interface between two components represents an additional resistance to the heat flow, and consequently an additional thermal drop that has to be estimated and taken into account. In this Chapter we will describe the analytical model used to estimate the thermal resistances between all the surfaces placed in contact in the electronic boards and DAQ crate thermal circuit. Heat transfer per unit area through two surfaces placed in contact is given by the combination of three terms.

- Conduction through contact spots, Q_c;
- Convection in the interstital areas, Q_g;
- Irradiation Q_i

The heat flux can be written as:

$$Q = Q_g + Q_c + Q_i \tag{4.1}$$

The *Thermal Contact Resistance* is defined as follows:

$$TCR = R = \frac{\Delta T}{Q \cdot A_a} = \frac{1}{h \cdot A_a} \tag{4.2}$$

where

$$h = h_g + h_c + h_i = \frac{Q}{A_a \cdot \Delta T} \tag{4.3}$$

h is called *Thermal Contact Conductance.*
In our case, since we are operating in a vacuum, we can neglect the contribution due to convection Q_g. Given the limited temperatures, radiation can also be neglected with respect to conduction, so equation 4.3 can be approximated as:

$$h = h_c = \frac{Q_c}{A_a \cdot \Delta T} \tag{4.4}$$

Despite of this simplification of the equation 4.4, an accurate estimate of the thermal contact conductance is very difficult because it depends on a lot of parameters.
Thermal conduction through interfaces occurs through contact spots, and clearly it is hard to evaluate the number and size of the contact spots, and consequently A_a. Several analytical models have been developed to solve this problem in vacuum, and the related correlation will be used to estimate the order of magnitude of the *thermal contact conduction*. The main question is related to modelling the asperities deformation once they are brought in contact.
We will take into account only nominally flat surfaces placed in contact in a vacuum under the condition of no radiation. Under this hypotesis, the heat flow across the joint will be distributed among the contact spots with different sizes.

4.1 Basic equations

Let us consider the generic contact point i. One can assume that this contact point is circular with a radius a_i, so for each contact we can write [7]:

$$Q_i = 2ka_i\Delta T_c \cdot \frac{1}{\psi_i} \tag{4.5}$$

where:

- k is the harmonic mean thermal conductivity, expressed by the relationship:

$$k = \frac{2(k_1k_2)}{k_1 + k_2} \tag{4.6}$$

  where k_1 and k_2 are the thermal conductivity of the material 1 e 2 brought in contact.

- ΔT_c is the temperature drop across the interface. For geometrically similar contact, we can assume a constant temperature drop for each contact i.

- ψ_i is a *geometrical factor*. The analytical estimate of this parameter has been object of research for several authors, and it can be expressed as follows:

$$\psi_i = \left(1 - \frac{a_i}{b_i}\right)^{1.5} \tag{4.7}$$

  where b_i is the radius of the adiabatic cylinder and a_i the radius of the spot.

Heat flow per **apparent** unit of area can be expressed from 4.5 as:

$$\frac{Q}{A_a} = \frac{\sum_i Q_i}{A_a} = 2k\Delta T_c \sum \frac{a_i/A_a}{\psi_i} \tag{4.8}$$

Neglecting the variation of ψ_i from contact to contact compared with variation in a_i, equation 4.8 can be rewritten:

$$\frac{Q}{A_a} \approx \frac{2k\Delta T_c}{\psi} \cdot \sum \frac{a_i}{A_a} \tag{4.9}$$

Moreover if we define an average radius of contact spot a_m, such that

$$\sum_{i=1}^{n} a_i = na_m$$

eq. 4.9 is transformed as:

$$\frac{Q}{A_a} \approx \frac{2k\Delta T_c}{\psi} \cdot \frac{na_m}{A_a} \tag{4.10}$$

The question is how one can obtain the value of n, a_m and A_a, in other words how to estimate the number and the size of the contact spots. This analysis is based on the model suggested by Kimura [8]. To do this, some important assumptions regarding asperity deformation are necessary.
Hypotheses:

- The heights and slopes of the surface profile are randomly distributed;
- There is no correlation between the probability density of the height and the probability density of the slopes.

Under these assumptions, one can define $z = f(x, y)$ as the profile height function, above the $x - y$ plane, defined as follows:

$$\int\int_A zdxdy = 0$$

where A is the nominal areas of contact.
It means that the $x - y$ plane is located at the mean height of the profile. We can also define the profile slopes in x and y direction as:

$$z_x = \frac{\partial z}{\partial x}$$

and in the same way

$$z_y = \frac{\partial z}{\partial y}$$

Let $w(z)$ be the *probability density function.* If we define ϵ as the average clearance at a given pressure P, the ratio between the real area of contact A_r and the nominal area of contact A can be expressed as follows:

$$\frac{A_r}{A} = prob(z > \epsilon) = \int_{\epsilon}^{\infty} w(z)dz \tag{4.11}$$

Our goal is to estimate the number of spots n_x, for unit length of surface

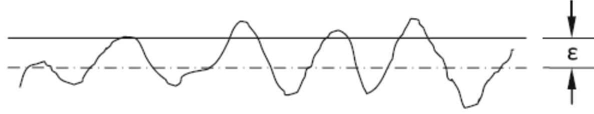


Figure 4.1: The average clearance of a cross section of x-y plane

profile parallel to the x-axis (with reference at figure 4.2), located above ϵ limit. Of course, similarly, the number of spots located above ϵ limit referred to y direction will be called n_y.
Let $w(z, z_x)dzdz_x$ be the joint probability that $z \in [z + dz]; z_x \in [z_x + dz_x]$.
The expected number of crossing per unit lenght dx, at $z = \epsilon$ is given by relation:

$$\frac{w(\epsilon, z_x)dzdz_x}{dx} = |z_x|w(\epsilon, z_x)dz_x \tag{4.12}$$

Of course, z_x can assume any value at $z = \epsilon$, because crossing does not depend on the slope of the profile. Therefore we can estimate the number of crossing per unit length as follows:

$$2n_x = \int_{-\infty}^{+\infty} |z_x|w(\epsilon, z_x)dz_x \tag{4.13}$$

This expression consider both crossing with positive and negative slope. Moreover there is no correlation between $w(z)$ and $w(z_x)$, so equation 4.13 can be finally written:

$$n_x = \frac{1}{2}w(\epsilon) \int_{-\infty}^{+\infty} |z_x|w(z_x)dz_x \tag{4.14}$$

In the same way we can estimate the number of crossing in y-direction

$$n_y = \frac{1}{2}w(\epsilon) \int_{-\infty}^{+\infty} |z_y|w(z_y)dz_y \tag{4.15}$$

Introducing the average length of contact spots, l_x and $l_y$in the x and y

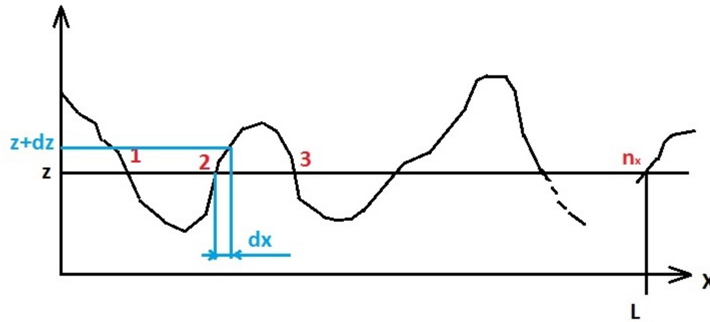


Figure 4.2: The average clearance of a cross section of x-y plane

directions spot such that:

$$L_x n_x = L_y n_y = \int_{\epsilon}^{\infty} w(z)dz = \frac{A_r}{A} \tag{4.16}$$

Let S be the mean area of contact spots, so a non dimensional shape form

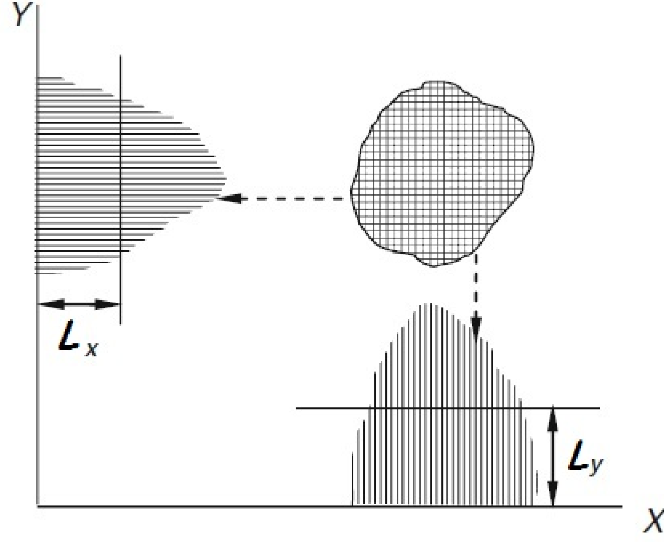


Figure 4.3: Mean lengths of contact spots

can be introduced

$$g = \frac{S}{L_x L_y} \tag{4.17}$$

The shape factor for a circular contact spot is equal to $4/\pi$
Now let n the number of contact spot per unit of area such that

$$nS = \frac{A_r}{A}$$

considering equation 4.16 and 4.17, we can write:

$$n = \frac{A}{A_r}\frac{1}{g}n_x n_y \tag{4.18}$$

Substituting equations 4.14 and 4.15 into equation 4.18 finally the total number of spot per area can be found:

$$n = \frac{1}{4g} \cdot \frac{A}{A_r}\left[w(\epsilon)\right]^2 \cdot \int_{-\infty}^{+\infty} |z_x| w(z_x) dz_x \int_{-\infty}^{+\infty} |z_y| w(z_y) dz_y \tag{4.19}$$

and consequently

$$S = \frac{4g \cdot \left(\frac{A_r}{A}\right)^2}{\left[w(\epsilon)\right]^2 \cdot \int_{-\infty}^{+\infty} |z_x| w(z_x) dz_x \int_{-\infty}^{+\infty} |z_y| w(z_y) dz_y} \tag{4.20}$$

4.1.1 Gaussian distribution of surface peaks and slopes

The distribution of peaks is assumed Gaussian (distribution acceptable in accordance with experimental observation).

In this model, surfaces are described by the standard deviation σ and the average of the absolute value of the slope ($tan(\theta)$).
Under this assumption we can write:

$$w(z) = \frac{1}{\sqrt{2\pi\sigma}} exp\Big(-\frac{z^2}{2\sigma^2}\Big) \tag{4.21}$$

A similar expression can be written for $w(z_x)$ and $w(z_y)$ replacing σ with σ_x and σ_y respectively for the profile slopes.
The average clearance can be found by equation 4.2 using this probability density.

$$\epsilon = \sigma\sqrt{2} erfc^{-1}\Big(\frac{2A_r}{A}\Big) \tag{4.22}$$

where

$$erfc(x) = 1 - erf(x) = \frac{2}{\sqrt{\pi}} \int_x^{+\infty} e^{-t^2} dt$$

and it's called complementary error function.
From equations 4.19 4.20 we obtain:

$$n = \Big(\frac{1}{4\pi^2 g}\Big)\Big(\frac{\sigma_x\sigma_y}{\sigma^2}\Big) \cdot \Big(\frac{A}{A_r}\Big) exp\Big[-2\Big\{erfc^{-1}\Big(\frac{2A_r}{A}\Big)\Big\}^2\Big] \tag{4.23}$$

$$S = (4\pi^2 g)\Big(\frac{\sigma^2}{\sigma_x\sigma_y}\Big)\Big(\frac{A_r}{A}\Big)^2 exp\Big[2\Big\{erfc^{-1}\Big(\frac{2A_r}{A}\Big)\Big\}^2\Big] \tag{4.24}$$

We can define the equivalent standard deviation of profile heights and of profile slopes:

$$\sigma_e^2 = \sigma_1^2 + \sigma_2^2 \tag{4.25}$$

where subscript 1 is refereed to one side of contact and subscript 2 to the second one.
The equivalent roughness can be written as:

$$\sigma_e = \sqrt{\sigma_1^2 + \sigma_2^2} \tag{4.26}$$

It's important to note that no observation about deformation analysis have been done.
Let Ψ be the *index of plasticity* defined by Mikic (1974) as follows:

$$\Psi = \Big(\frac{E'}{H}\Big) tan\theta \tag{4.27}$$

Mikic demonstrated that plastic deformation occurs when $\Psi > 1$. The last step is to determine the ratio A_r/A. Let P and H [MPa] be the mechanical pressure of contact and microhardness of softer material respectively. For fully plastic deformation one can assume:

$$A_r H = PA$$

We are now able to find an analytical expression for the thermal contact conductance. Considering a circular contact spot, such that the shape factor $g = 4/\pi$, $S = \pi a_m^2$, from equation 4.20 one can write:

$$a_m = 4\frac{\sigma}{tan\theta} \cdot \Big(\frac{A_r}{A}\Big) exp\Big[\Big\{erfc^{-1}\Big(\frac{2A_r}{A}\Big)\Big\}^2\Big] \tag{4.28}$$

and from equation 4.19

$$n = \Big(\frac{1}{16\pi}\Big)\Big(\frac{tan\theta}{\sigma}\Big)^2\Big(\frac{A}{A_r}\Big) exp\Big[-2\Big\{erfc^{-1}\Big(\frac{2A_r}{A}\Big)\Big\}^2\Big] \tag{4.29}$$

Finally it is possible to evaluate the quantity:

$$na_m = \Big(\frac{1}{4\pi}\Big)\Big(\frac{tan\theta}{\sigma}\Big) exp\Big[-2\Big\{-erfc^{-1}\Big(\frac{2A_r}{A}\Big)\Big\}^2\Big] \tag{4.30}$$

Replacing this quantity into equation 4.9, considering definition 4.4 the analytical expression of thermal contact conductance can be written as:

$$h_c = \Big(\frac{1}{2\pi}\Big)\Big(\frac{tan\theta}{\sigma}\Big)\Big(\frac{k}{A_r\psi}\Big) exp[-X] \tag{4.31}$$

where, under the assumption of fully plastic deformation

$$X = \Big\{erfc^{-1}\Big(\frac{2P}{H}\Big)\Big\}^2$$

This is a theoretical expression for the thermal contact conduction in a vacuum. In order to estimate this parameter we have used similar empirical results based on this theory and suggested by several authors. Empirical correlations are described in the following paragraph.

4.1.2 Empirical correlation for the estimate of the thermal contact conductance

Every relation is related to fully plastic deformation of metals in contact and is based on the hypothesis described in the previous section.

- Tien model (1968) [7]

$$h_c^{Tien} = 0.55k\frac{tan\theta}{\sigma}\Big(\frac{P}{H}\Big)^{0.85} \tag{4.32}$$

- Mikic model (1974) [6]

$$h_c^{Mikic} = 1.13k\frac{tan\theta}{\sigma}\Big(\frac{P}{H}\Big)^{0.94} \tag{4.33}$$

- Cooper, Mikic, Yovanovich model (1969) [5]

$$h_c^{c,m,y} = 1.45k\frac{tan\theta}{\sigma}\Big(\frac{P}{H}\Big)^{0.985} \tag{4.34}$$

- Yovanovich model (1982) [7]

$$h_c^{Yovanovich} = 1.25k\frac{tan\theta}{\sigma}\Big(\frac{P}{H}\Big)^{0.95} \tag{4.35}$$

4.2 Study of the interfaces in the DAQ crate thermal circuit

We have studied the two interfaces of the DAQ thermal circuit where we expect a significant thermal drop. We have estimated the thermal contact conductance and we have used the estimated values for the simulation of the thermal circuit. The first interface is between the cardlock and the crate wall, while the second one is between the internal surfaces of the cardlock, see Figure 4.4. Where possible, we plan to apply a film of glue or thermal pad between the surfaces placed in contact in order to guarantee an optimal thermal contact. Of course, once a film of glue or a thermal pad has been inserted between two metal surfaces, the model of the thermal contact conductance cannot be used, and the thermal drop between the two surfaces can only be estimated using the thermal properties of the glue or of the pad provided by the technical datasheets.

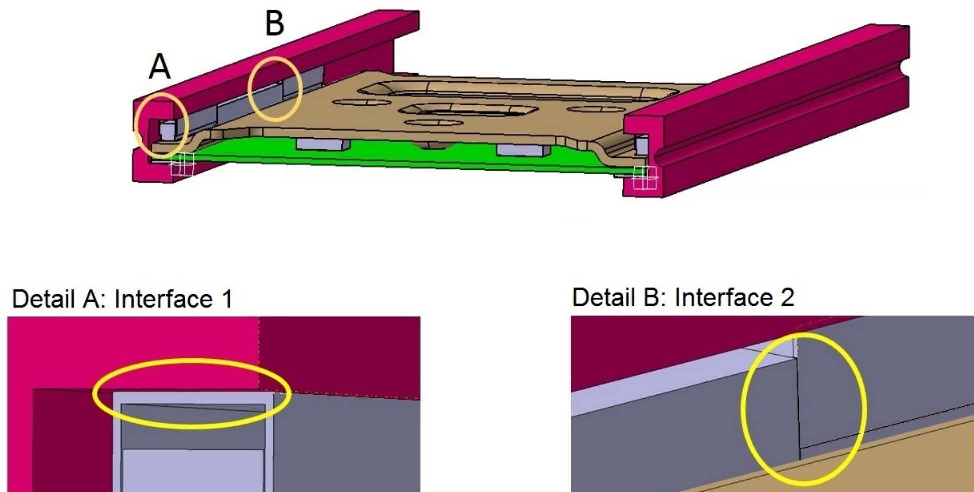


Figure 4.4: Design of the most relevant thermal interfaces in the DAQ crate thermal circuit.

4.2.1 Estimate of the thermal contact conductance between the cardlock and the crate wall

Table 4.2 reports the material properties we have used to estimate the thermal contact conductance between the cardlock and the crate wall.

The plasticity index has been estimated using equation 4.27, in which:

Table 4.1: Properties of materials.

	Cardlock	**Crate**
Material	Stainless Steel grade 304	Aluminum
Thermal conductivity, $k_{1,2}[W/(mK)]$	16.2	218
Hardness, $H, [MPa]$	1800	1400
Modulus of elasticity, $E_{1,2}[MPa]$	190000	70000
Poisson's modulus	0.27	0.33
Roughness, $r_{1,2}, [\mu m]$	0.8	0.8
Slope, $tan\theta_{1,2}$	0.03	0.03

$$E' = 2\Big[\frac{1-\upsilon_1^2}{E_1} + \frac{1-\upsilon_2^2}{E_2}\Big] \approx 57000\ MPa$$

where E' is the equivalent elastic modulus, υ_i the Poisson modulus and is H the hardness of the softer material. Under this condition, $\Psi \approx 1,75$ therefore for the Mikic assumption the problem can be considered totally plastic.
The thermal conductivity as a function of the mechanical contact pressure has been plotted using the correlations described in the previous Section.

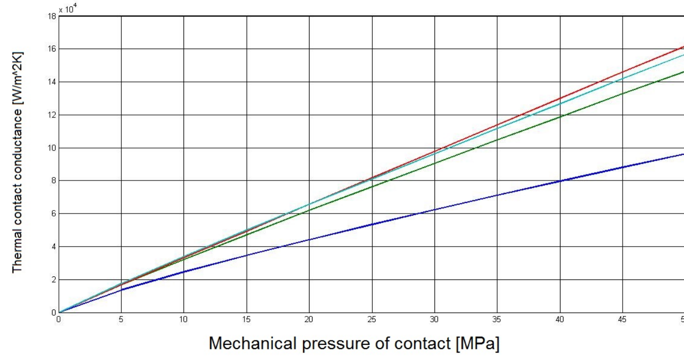


Figure 4.5: Thermal contact conductance (y-axis) vs mechanical pressure of contact(x-axis). The blue curve has been determined with the Tien model, the green curve has been determined with the Mikic model, the pale blue curve has been determined with the Yovanovich model, and the red curve has been determined with the Cooper, Mikic and Yovanovich model.

Under reasonable assumption we have estimated a minimum value of the mechanical contact pressure.
It is approximately $1,1MPa$ and it is reached with a cardlock tightening torque minimum of 30 $N \cdot cm$. This is an important constraint that must be verified during the crate assembly. Lower values of the torque would imply lower contact pressure values and clearly a higher thermal contact resistance which would imply a more significant thermal drop (see Figure 5.12).
The minimum value of thermal contact conductance in this condition, estimated using Tien model (the most conservative correlation) is:

$$h_c^{Card-Crate} \approx 4100W/m^2K$$

.

4.2.2 Estimate of the thermal contact conductance between the internal surfaces of the cardlock

We have studied the thermal contact conductance between the internal surfaces of the cardlock. According to the datasheet, the internal contact pressure has been evaluated for a minimum value of the torque.
In this case using Tien model we have obtained the following value of the thermal contact conductance

$$h_c^{Card-Card} \approx 40000\ W/m^2K$$

Table 4.2: Thermal conductivities used for the thermal simulation

	Cardlock side 1	**Cardlock side 2**
Material	Stainless Steel grade 304	Stainless Steel grade 304
Thermal conductivity, $k_{1,2}[W/(mK)]$	16.2	16.2
Hardness, $H, [MPa]$	1800	1800
Modulus of elasticity, $E_{1,2}[MPa]$	190000	190000
Poisson's modulus	0.27	0.27
Roughness, $r_{1,2}, [\mu m]$	0.8	0.8
Slope, $tan\theta_{1,2}$	0.03	0.03

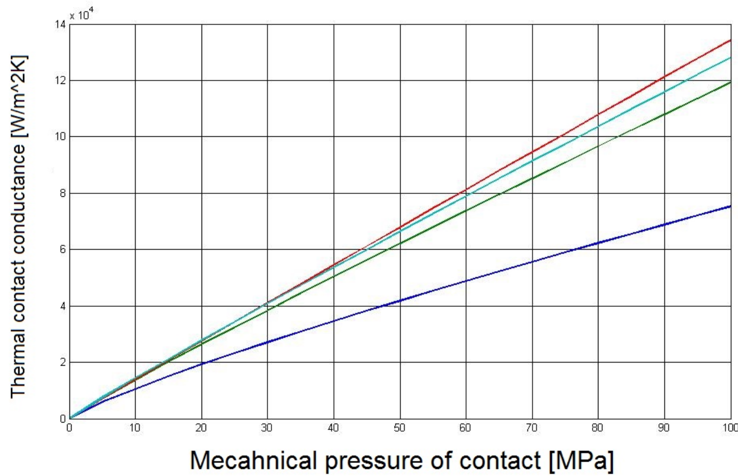


Figure 4.6: Thermal contact conductance (y-axis) vs mechanical pressure of contact(x-axis). The blue curve has been determined with the Tien model, the green curve has been determined with the Mikic model, the pale blue curve has been determined with the Yovanovich model, and the red curve has been determined with the Cooper, Mikic and Yovanovich model.

Chapter 5

DAQ crate and boards thermal analysis

In this Chapter we describe the thermal analysis we have performed on the waveform digitizer and interface boards and on the DAQ crates which host these boards. Since the reliability and lifetime of the electronics components depends on the temperature of operation, we have to make sure that the cooling system allows to keep a stable local temperature well below the critical temperature of each component.

5.1 3D CAD model of the boards

To reduce the computing time required for the simulation and the thermal analysis of the boards, we have used a simplified CAD model. Holes, geometrical details and connections, which are useless to estimate the field of temperature have been excluded during the geometry cleanup. On the other hand contacts and electronic parts have been carefully modeled. The 3D CAD is shown in Figure 5.1. The thermal properties of each component relevant for the thermal analysis have been reported in Table 5.1. The thermal properties

Table 5.1: Thermal conductivities used for the simulation of the thermal circuit.

Part	**Material**	**Thermal conductivity** $[\frac{W}{m \cdot K}]$
Plate	Aluminum	237.5
Cardlock	Stainless Steel grade 304	16.2
Thermal Pad	silicon	2
Thickness	Aluminum	237.5
FR4 board (x-y plane)	FR-4	0.9
FR4 board (along z axis)	FR-4	0.3

of the electronic components have been estimated using the overall thermal resistance reported in the datasheets. We have limited the thermal analysis to 1 single board. With the limited temperature variation of the cooling fluid flowing in the DAQ crate circuit, we can impose the same boundary condition

in terms of temperature to all the 7 waveform digitizer and interface boards hosted in the DAQ crate. For the thermal analysis, all the board pairs are consequently identical.

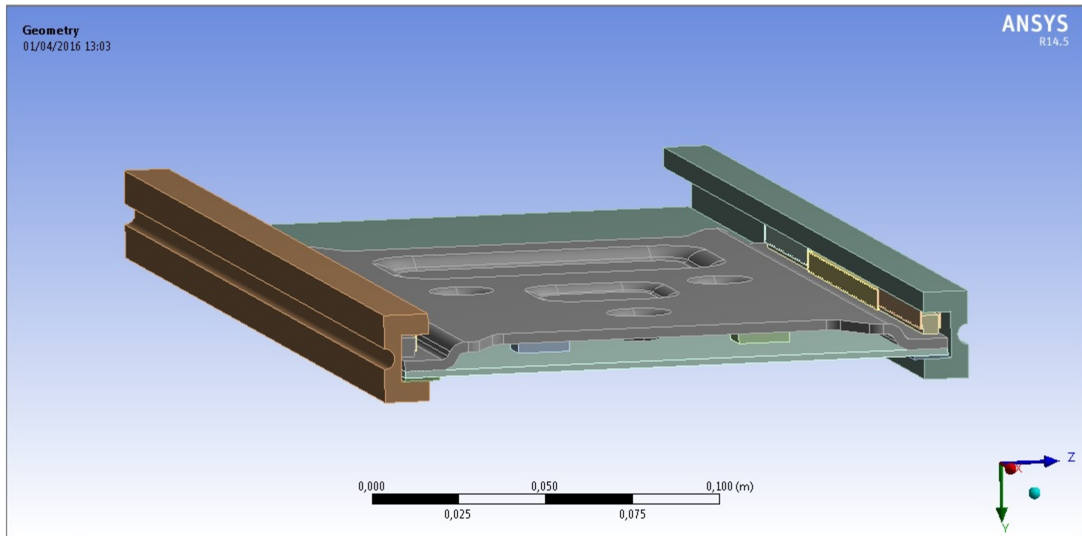


Figure 5.1: 3D model used for thermal simulation.

5.1.1 Input values and boundary condition

As mentioned in Chapter 2 the approximate values of the power dissipated by the electronic components of the waveform digitizer are:

- FPGA: 5 W;
- DCDC: 3 W;
- ADC: 0.5 W.

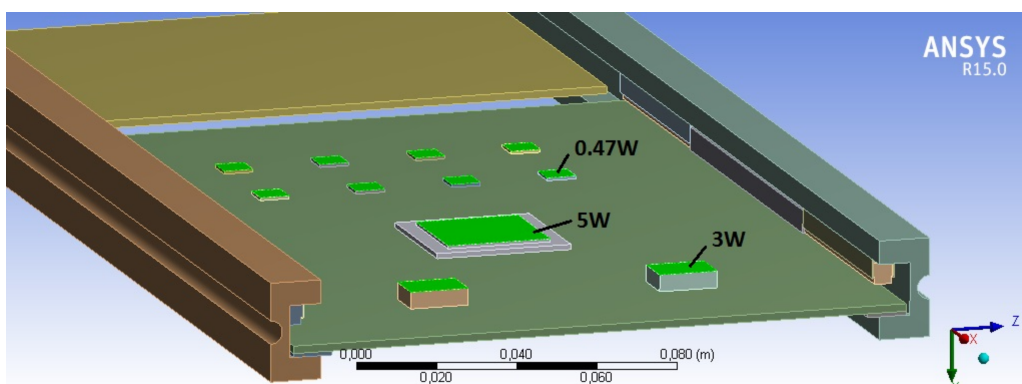


Figure 5.2: Approximate distribution of the electronic components on the waveform digitizer and approximate power dissipated by each component.

We have assumed a sufficient cooling fluid flux to impose a boundary condition on each board side at the average temperature of the cooling fluid.
As reported in Chapter 3, the properties of glycol ethylene are:

- Operating temperature: -5 $^{\circ}C$;
- Film coefficient: $\sim$ 4200 W/m^2K;

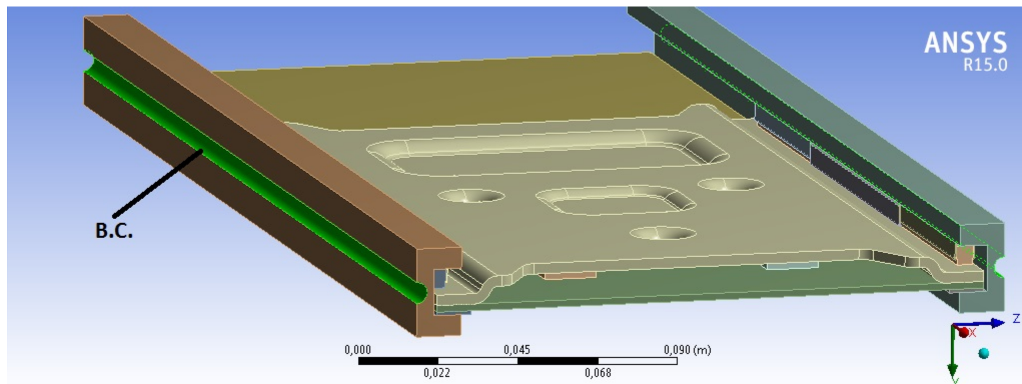


Figure 5.3: Model of boundary conditions used in the thermal analysis of the waveform digitizer.

In the commercial code used for the thermal simulation we have inserted the value of the *thermal contact conductance* estimated on the basis of the analytical model reported in Chapter 4. Note that in this thermal analysis we have assumed a conservative value of tightening torque $T = 30\ N \cdot cm$, the lowest acceptable value.

5.2 Results of the thermal simulation

Figures 5.4, 5.5, 5.6, 5.7, 5.8 report the fields of temperature in the several electronic components of the waveform digitizer, in the aluminum plate, in the cardlocks and in the DAQ crate walls.

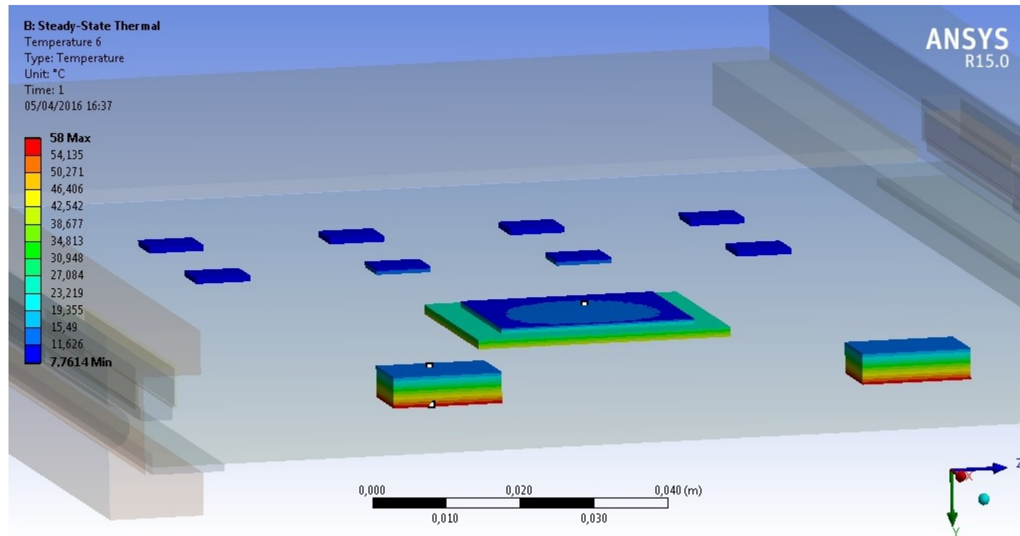


Figure 5.4: Field of temperature inside the electronic components of the waveform digitizer.

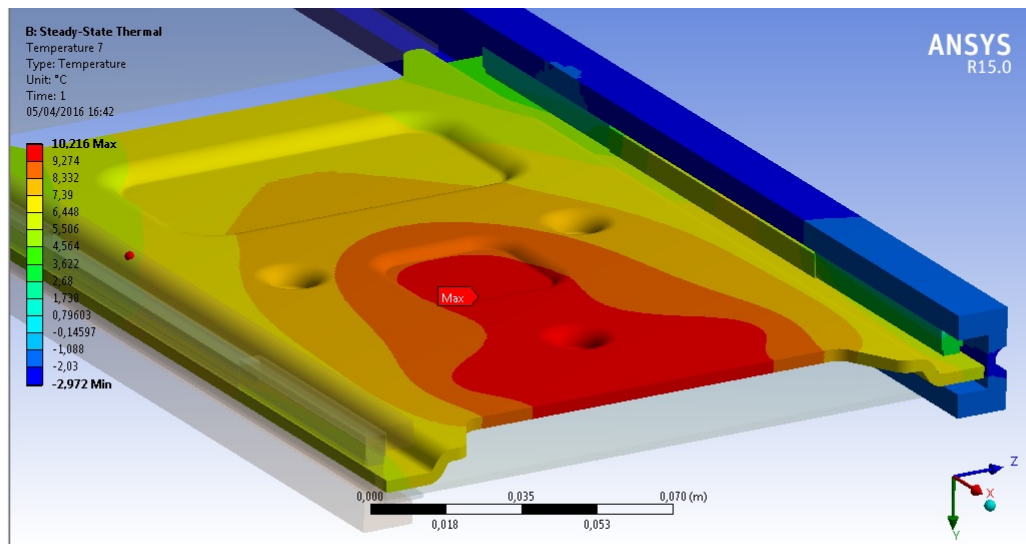


Figure 5.5: Field of temperature in the aluminum plate, cardlock and crate.

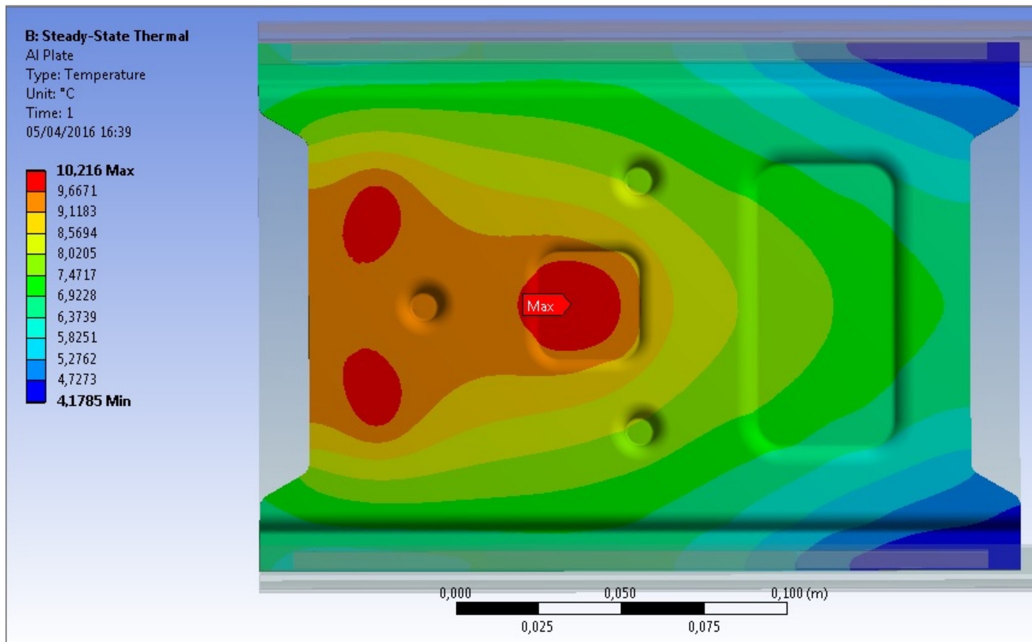


Figure 5.6: Field of temperature in the aluminum plate.

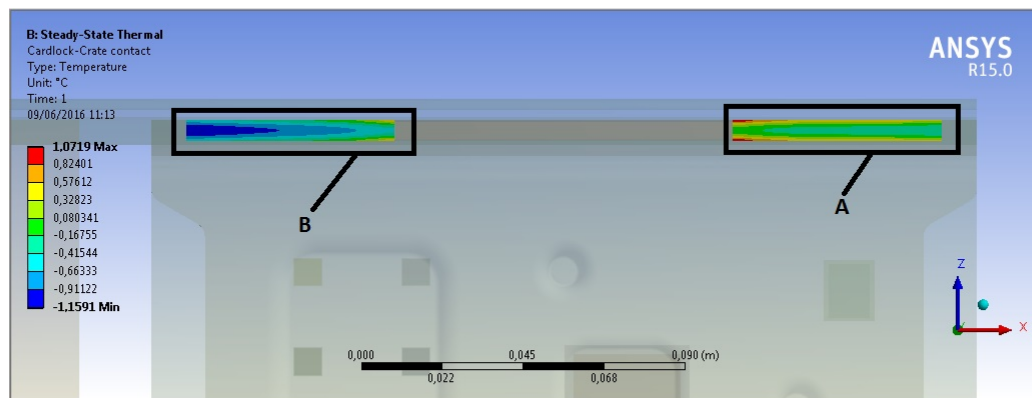


Figure 5.7: Temperature of the cardlock part in contact with the crate wall.

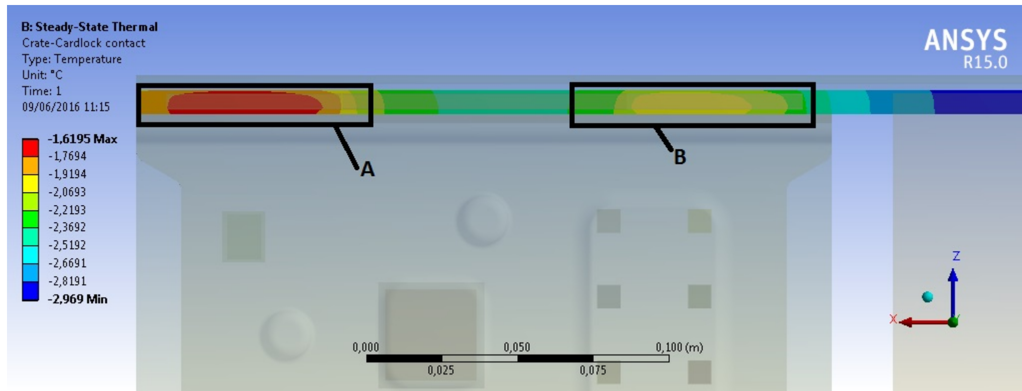


Figure 5.8: Temperature of crate wall part in contact with the cardlock.

We have also performed a preliminary thermal analysis of the interface board. Since we only have a conceptual design of this board, we have only approximately estimated an order of magnitude of the temperature of the external surface of the voltage regulator which is the component with the largest power dissipation.
We have used the same thermal model in this board as for the waveform digitizer board, with the expected power dissipation for the voltage regulator of 10 W. The field of temperature for the voltage regulator is reported in Figure 5.9.

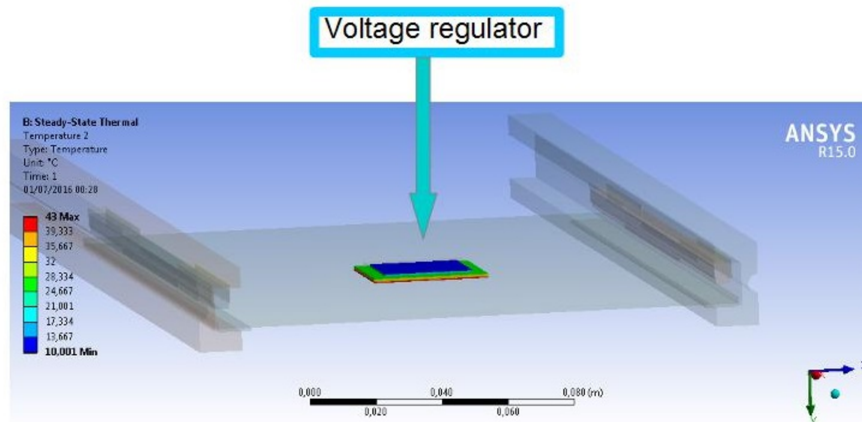


Figure 5.9: Field of temperature for the voltage regulator.

Once we have obtained the field of temperature by the Finite Element Analysis, we have estimated the thermal resistances of each component and we have compared the temperature of each junction inside the electronic component their maximum allowed temperature.
The thermal resistance is refereed to the equivalent thermal circuit of the waveform digitizer (Fig. 5.10).

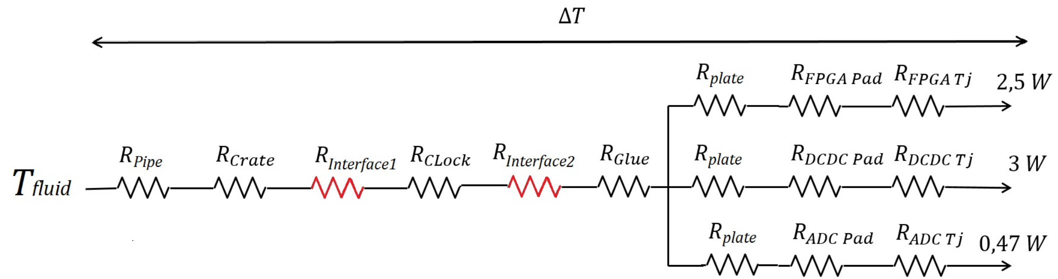


Figure 5.10: Equivalent thermal circuit of the waveform digitizer board.

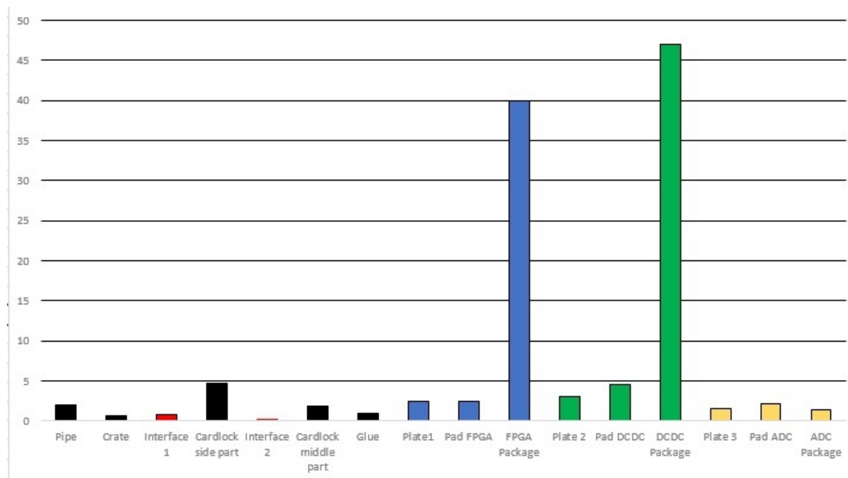


Figure 5.11: Estimated thermal drops related to the 1D simplified model reported in Figure5.10.

Table 5.2 reports the estimated temperatures of each electronic component.

This analysis shows that the operational conditions of the waveform digitizer are not critical, in fact the safety factors are higher than two. We expect similar conclusion also for the interface board.
Further experimental measurements will be necessary to validate this result, however in order to reduce the thermal drops along the chain of thermal resistances we have to minimize the thermal contact resistance. Figure 5.12 shows the dependence of the temperature drop at the interface between the cardlock and the DAQ crate wall as function of the cardlock tightening torque. The upper limit is fixed by the torque value which corresponds to a thermal drop lower than 1 $°C$. The upper limit is a cardlock mechanical limit given by

Board	Component	T_{max} [$°C$]	T_{ac} [$°C$]	SF
waveform digitizer	FPGA	100	44	2.27
waveform digitizer	DCDC	125	58	2.15
waveform digitizer	ADC	85	11	7.72
interface	Voltage regulator (interface board)	-	43	-

Table 5.2: Estimated temperature on the junctions of the electrical components used on the waveform digitizer and interface board with an estimate of the safety factors. We currently do not know the critical temperature of the voltage regulator since this component has not been designed yet.

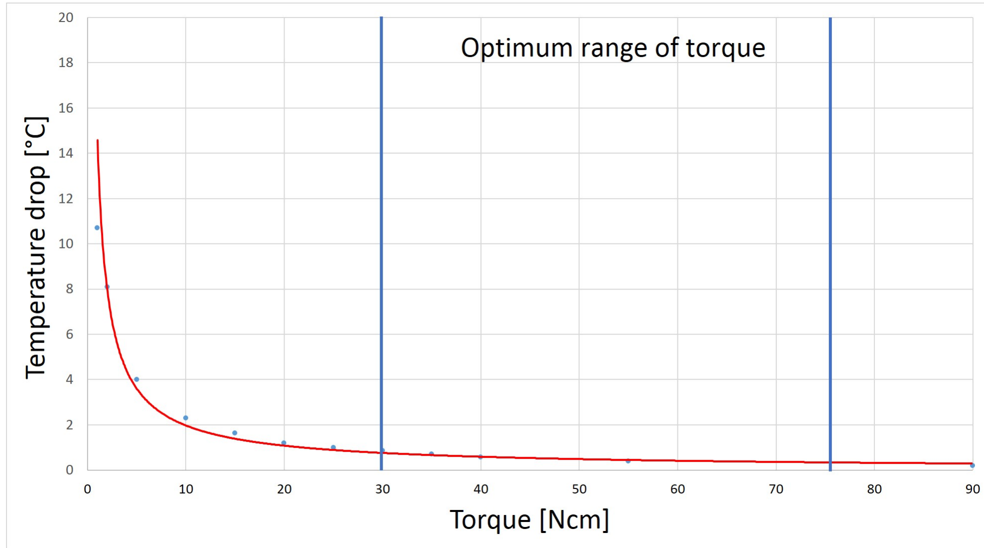


Figure 5.12: Average thermal drop in the interface 1, as function of the torque. This figure shows how the temperature drop increases due to a wrong installation of the boards.

datasheet.
The recommended torque is around 60 $N \cdot cm$, which implies a thermal drop on the interface one of $\approx 0.4°C$. All the remaining contributions to the thermal drops (resistances in black) depend only on the material and the geometry.
For this reason, as we will see in the Chapter 7, some important precautions during the assembly process will have to be taken.

As additional comment to the thermal analysis of the interface board note that this estimate of the voltage regulator temperature is very preliminary, since we don't know the technical specification of this component.

Chapter 6

Thermal-vacuum tests design

Each component of the Mu2e experiment has to be tested and qualified for operations in vacuum. Also reliability is crucial, since any access to the detector is going to be limited to a few weeks per year. Our goal is to perform outgassing and thermal tests of every component used in the electromagnetic calorimeter. We want to measure the thermal resistance of the components and the maximum temperature reached by the electronic components during operation. In this way we can also validate the finite element model we have used for the thermal analysis. In this Chapter we will describe the thermal-vacuum tests we plan to perform at the INFN Pisa laboratory.

6.1 Outgassing measurements

We have to measure the outgassing rate of the materials which will be used in the vacuum environment of 10^{-4} Torr (High vacuum level) expected in the Mu2e cryostat. We plan to perform several tests. The standard test is the total mass loss, which is commonly used for high outgassing rate materials and is regulated by ASTM E595 and ECSS-Q-ST-70-02 and can be a used for the electrical components, the thermal pads and the thermal glues. The ASTM regulation gives the exact procedure to perform this test. The main steps are [9]:

- the models are submitted to pre-conditioning (24 hours at 25°C and 55% rH) to allow moisture uptake;
- during the vacuum test (25°C and 10^{-4} torr for 24 hours) the outgassing rate is estimated by the measurement of the weight of the model before and after thermal treatment;
- samples are also weighted after a post-conditioning (24 hours at 25°C and 55% rH) allowing recovery of lost moisture.

Then the sample is weighted with a precision balance. This test allows to measure:

- TML (Total Mass Loss): Total mass loss relative to the initial sample mass;

- RML (Recovered Mass Loss): Mass loss after water absorption during post-conditioning (relative to initial sample mass);
- CVCM (Collected Volatile Condensable Material): mass gain of collectors relative to initial sample mass.

The qualitative mass evolution with time is shown in Fig. 6.1.

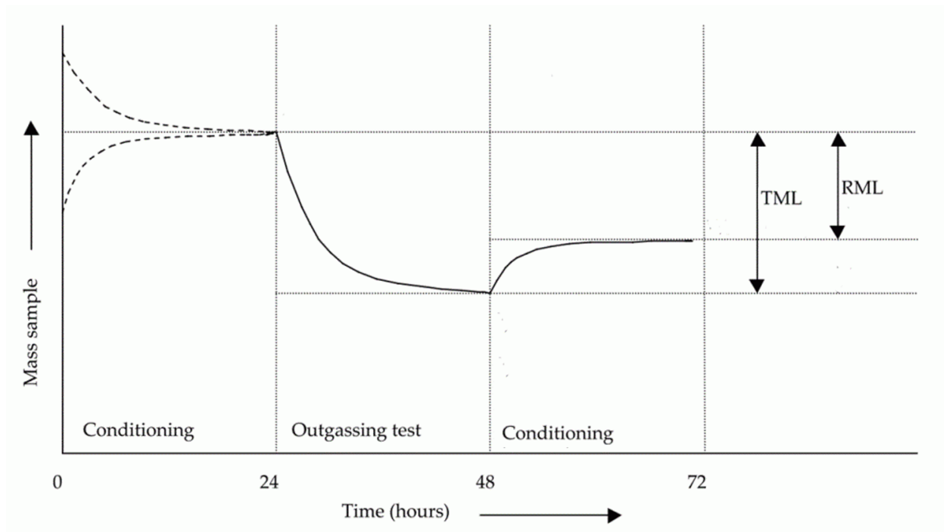


Figure 6.1: Qualitative mass evolution of a specimen during a weight loss outgassing test.

This test can be performed at the INFN Pisa laboratory where a small vacuum chamber is available. An alternative test uses the throughput method. This method is commonly used when upper limits of outgassing rate are needed and the sample is very large. We can use this test for the outgassing measurement of the full mounted crate with all the boards installed. The idea is to apply the desired pressure with a vacuum pump in a vacuum chamber, to turn off the pump and to read the pressure value as a function of time. The pressure inside the chamber increases due to the outgassing and the leaks. The parameter provided by this test is the slope of the curve pressure as a function of time (Fig. 6.2) which represents the outgassing rate [9].

To perform this test a vacuum chamber which can contain the crate ($\geq 500 \times 600 \times 300$ mm) with a high vacuum gauge and a data acquisition system are necessary. All these measurements are very time-consuming. Each measurement can require up to 3 days of measuring time, to which the setup time has to be added. Also in this case, the necessary instrumentation is available at the INFN Pisa laboratory, and we plan to perform these tests in the next few months.

6.2 Thermal-vacuum tests of the DAQ crate

The thermal-vacuum tests are extremely useful to validate the entire thermal simulation and, in particular, to check the thermal behavior of all the compo-

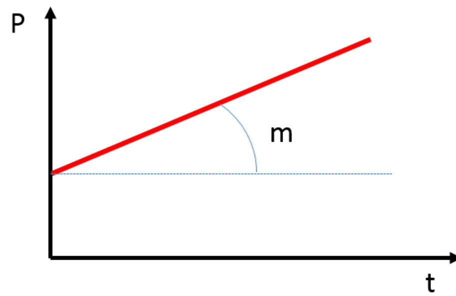


Figure 6.2: Qualitative pressure evolution with time of a specimen during a throughput method outgassing test [9].

nents, including the cardlocks, the thermal pads, and the analytical estimates of the thermal contact resistances. We can perform these measurements at the INFN Pisa laboratory where a thermostatic vacuum chamber sufficiently large to contain the components and the instrumentation (Figure 6.7) is available.

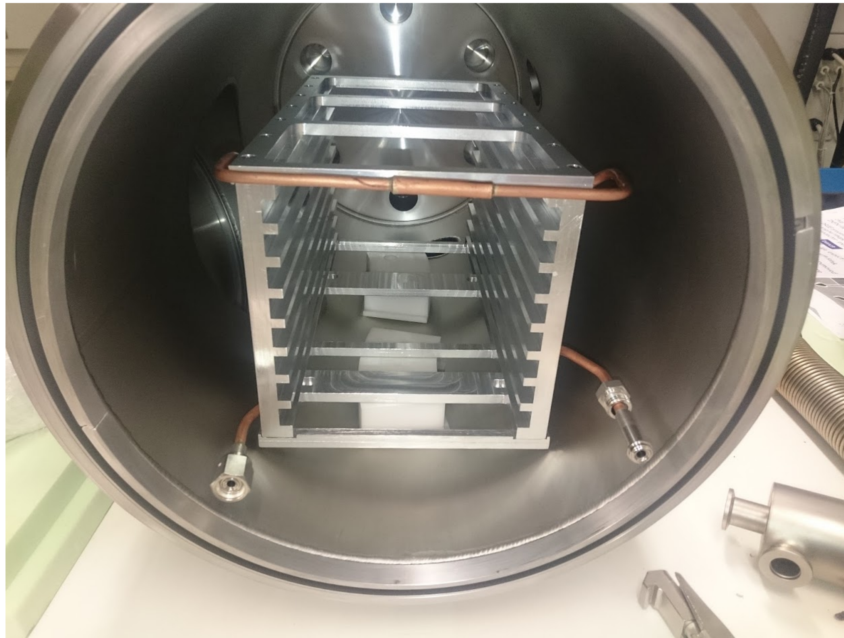


Figure 6.3: Vacuum chamber with the prototype DAQ crate at the INFN Pisa laboratories. This chamber will be used to perform all the thermal-vacuum tests of the DAQ crate components.

The DAQ crate prototype has to be kept in position with no thermal contacts with the structure and the vacuum chamber. Given the cost and the time to completely design and assemble a first waveform digitizer prototype, we have designed a dummy board equipped with resistors which reproduces the power dissipation of the FPGA, DCDC converter and ADCs.
The ADC power dissipation is simulated with a primary electrical circuit powered at a 10 V and a series of electrical resistances with a value of 3 Ohm. FPGA and DCDCs power dissipation is reproduced with a secondary electri-

cal line powered at 8 V and a series of resistances of value 5 Ohm and 3 Ohm respectively (Figure 6.5).

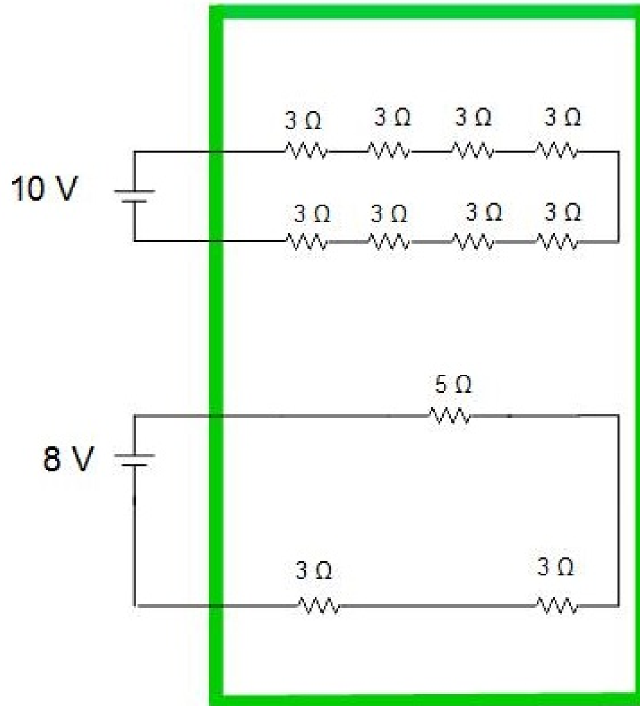


Figure 6.4: Layout of the board used for the thermal tests of the dummy waveform digitizer board. The eight top 3 Ohm resistances simulate the eight ADCs, the central 5 Ohm resistance simulates the FPGA, and the two bottom 3 Ohm resistances simulate the two DC-DC converters.

The resistances have been chosen to simulate the package in terms of size and dimensions. We have used *PWR263S-35 Series power resistor* Bourns Inc. To measure the temperature of the electronic components, we can use a PT100 probe, or alternatively a visual system as thermo-graphic camera and a DAQ. This dummy board will be inserted inside the prototype DAQ crate in the vacuum chamber and the cooling pipe will be connected to the chiller with an appropriate vacuum feedthrough. INFN Pisa laboratory has also a pumping system to supply the glycol ethylene cooling fluid in the proper thermodynamical conditions and the necessary instrumentation to regulate all the flow parameters, such as the flow rate, temperature and pressure. The pumping system has been described in Chapter 3.

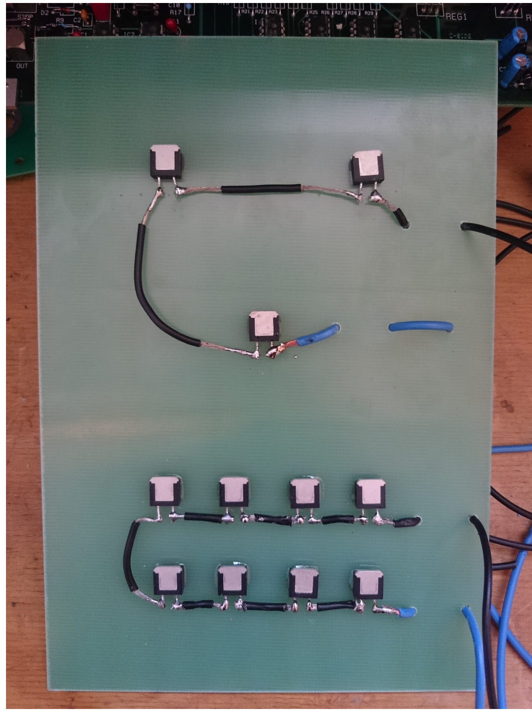


Figure 6.5: Dummy waveform digitizer board assembled to the thermal tests. The two top 3 Ohm resistances simulate the two DC-DC converters, the central 5 Ohm resistance simulates the FPGA, and the eight bottom 3 Ohm resistances simulate the eight ADCs.

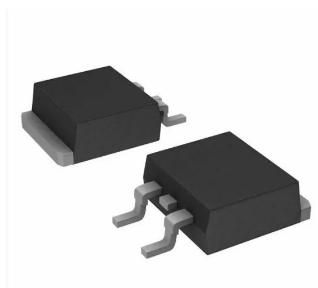


Figure 6.6: Power resistors used for the thermal test of the dummy waveform digitizer board.

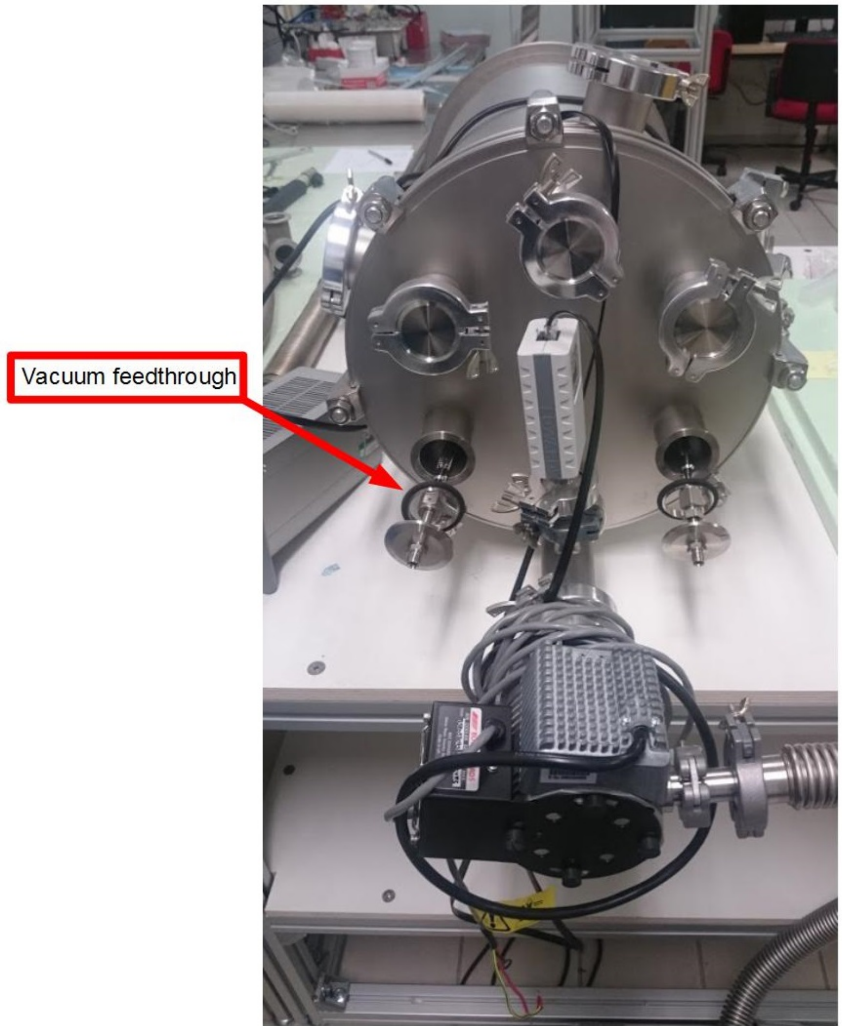


Figure 6.7: Vacuum chamber used for the thermal-vacuum tests at the INFN Pisa laboratory.

Chapter 7

Procedures for the DAQ crates integration

The DAQ crates will be assembled at the Fermilab Mechanical workshop and then integrated on the calorimeter disks. In this Chapter we will describe a possible 4-step assembly and integration procedure:

- DAQ crates assembly;
- Integration of the DAQ crates and of the cooling system on the calorimeter;
- Connection of the DAQ crate cooling circuit to the dividing manifolds;
- Integration of the waveform digitizer and interface boards in the DAQ crates.

In this Chapter we will give a brief description of this assembly and integration procedure.

7.1 DAQ crate assembly and integration

The DAQ crate is made of four machined walls which will be assembled with a set of screws.

The shape of the cooling pipe is optimized in order to satisfy all the space constraints. The installation of the cooling pipes on the DAQ crates will be done before integrating the crates on the calorimeter disks. The procedure is done in three steps:

1. Brazing the cooling pipe on one DAQ crate wall (Fig. 7.2) ;
2. Brazing the cooling pipe on the opposite DAQ crate wall (Fig. 7.3);
3. Connecting the two cooling pipes on the two opposite walls by brazing a pipe (Fig. 7.4).

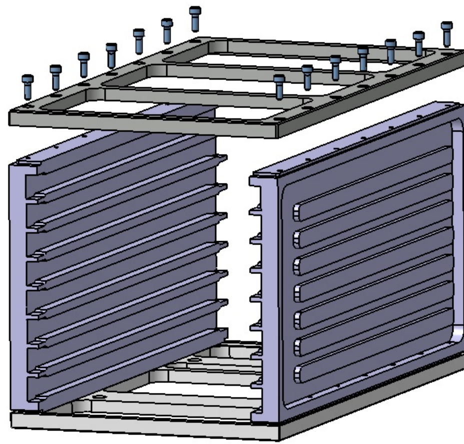


Figure 7.1: Assembly of the four machined walls to make the DAQ crate

We have chosen an **AlSi12** alloy of *STELLA Welding Alloys*. It is a aluminum-silicon brazing alloy with good thermal properties and qualified for operation in vacuum since it is cadmium and zinc free.

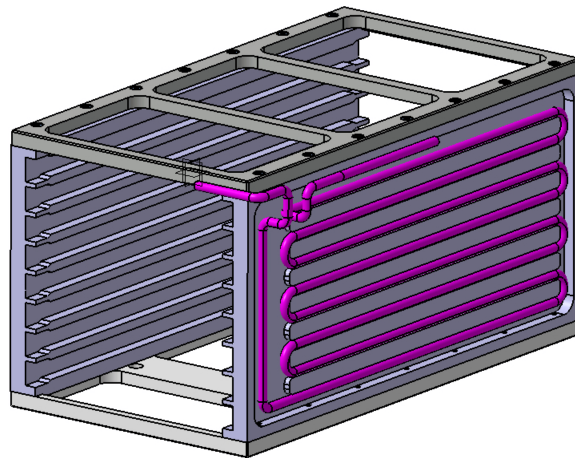


Figure 7.2: Cooling pipe integration step 1: the cooling pipe is brazed on one DAQ crate wall.

7.2 Cooling circuit integration

We have several options to fix the cooling pipe to the DAQ crate walls, by flame, induction, as well as furnace. Our preference is to use induction.
To connect crate pipes to the dividing manifolds we plan to use VCR Metal Gasket Face Seal Fittings. This is a stainless steel connector designed for vacuum operations. The preliminary operation before integrating the cooling

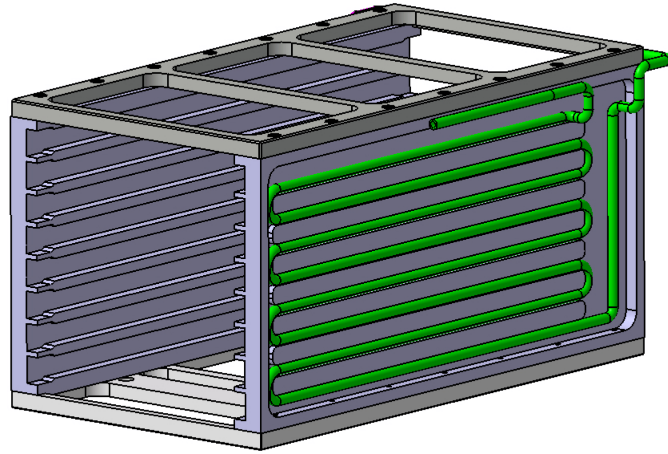


Figure 7.3: Cooling pipe integration step 2: the cooling pipe is brazed on the opposite DAQ crate wall.

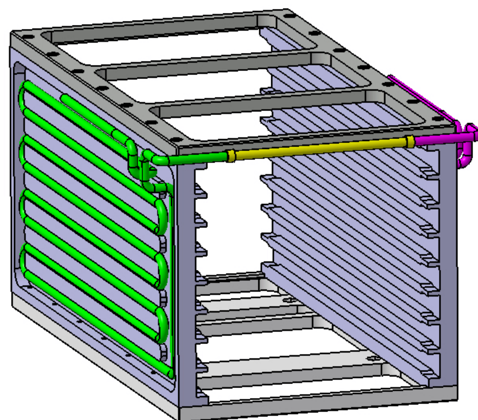


Figure 7.4: Cooling pipe integration step 3: the cooling pipes brazed on the two opposite DAQ crate walls are connected with a pipe.

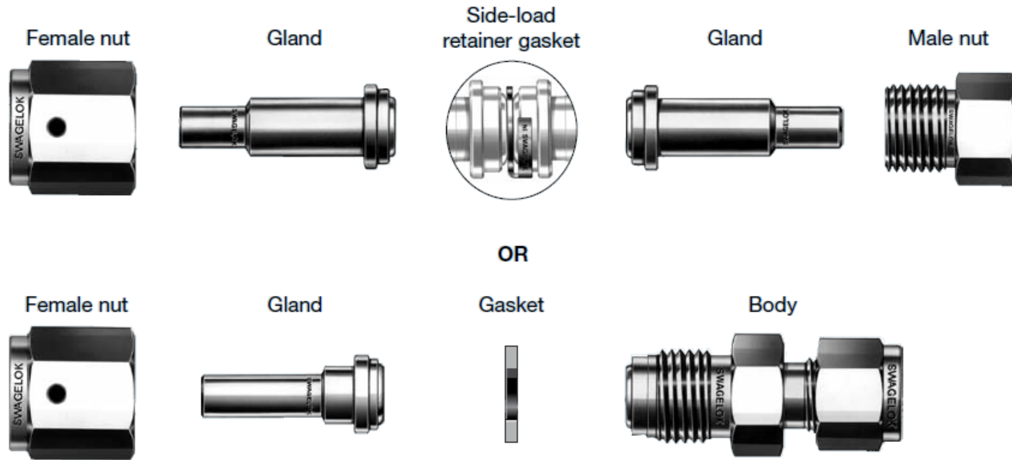


Figure 7.5: Section of VCR swagelock connector.

system on the calorimeter is to braze the female part of the VCR swagelock on the dividing manifold branches and the male part of the VCR swagelock on the cooling pipe (Figure 7.6).

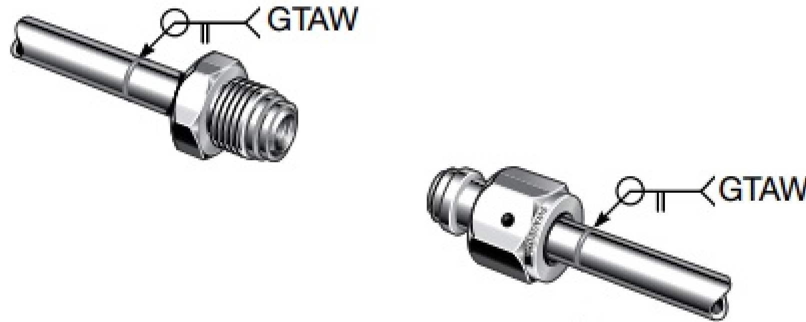


Figure 7.6: Brazing process of the VCR on the pipes.

Once the male part of the VCR swagelock is brazed, the dividing manifold is ready for installation, Figure 7.11. The integration of the cooling system has been designed in order to minimize the number of modifications on the calorimeter outer ring, which represents our mechanical interface.
In order to fix the dividing manifold to the structure we have decided to install three supports, bolted to the outer ring.

Finally the DAQ crates can be installed on the external side of the electromagnetic calorimeter disks. It is important to notice that the DAQ crate plate in contact with the outer ring, is made of peek material. Peek is a plastic material qualified for vacuum and has a very low outgassing rate and adequate thermal insulating properties (0.25 W/mK). The bottom peek plate will have

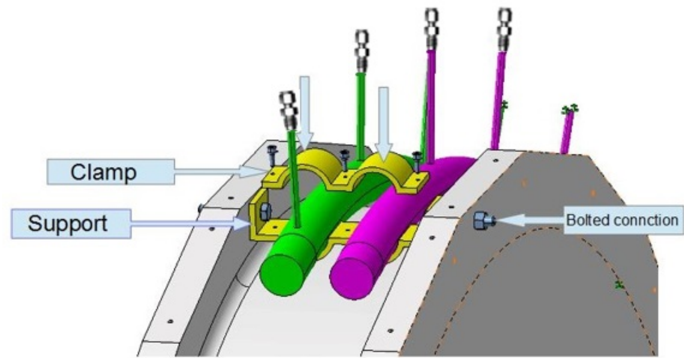


Figure 7.7: Installation of the dividing manifolds on the calorimeter disk.

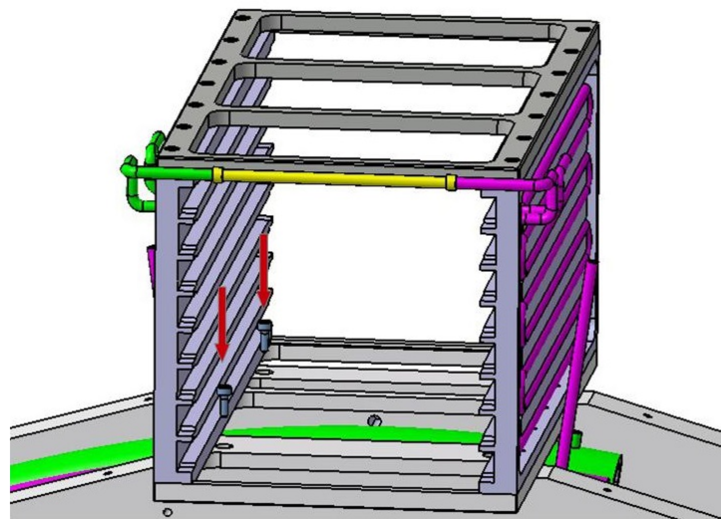


Figure 7.8: Connection of the DAQ crate on the external ring.

to be placed on the external surface of the outer ring and connected by the screws (Fig. 7.8). In appendix B is reported the verification of the bolt connection. The operator has to start with the most external crate and place the baseplate on the mechanical mounting holes by a screw mechanism, in order to connect the cooling pipe to the dividing manifold.

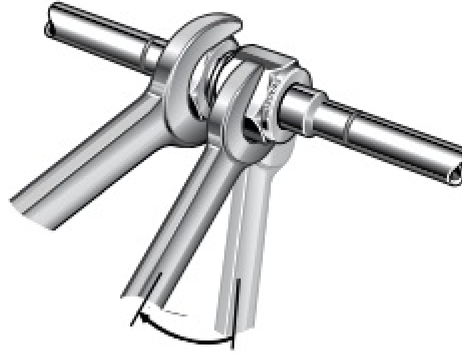


Figure 7.9: Connection of the DAQ cooling pipe to the dividing manifold.

7.3 Boards integration in the DAQ crate

Cardlocks are used to fix the waveform digitizer and the interface boards to the DAQ crate walls. The mechanism is very simple, cardlocks are made of a series of separated blocks, mantained in contact by a screw system which allows easy mounting and dismounting. We have decided to use cardlocks because they are suitable regarding pressure of contact and they have very good thermal properties. The cardlock datasheet is reported in appendix D.5.

The first operation is to fix the cardlock on the waveform digitizer. It is very important for the proper working of the system to follow the instruction step by step:

1. Clean the aluminum plate surface and apply a film of epoxy glue;

2. Position the cardlock over the glue film and hold it with the three position screw;

3. Insert the waveform digitizer into the crate and clamp the cardlock with a torque value $T \geq 60N \cdot cm$.

Since we expect there is no reason to dismount the cardlock from the aluminum plate, the connection among these two components will be made with a thermal glue that guarantee a good contact and thermal properties.
A lot of commercially available glues satisfy our requirements, but after a long comparison we have chosen the $3M^{TM}$ Thermally Conductive Epoxy adhesive TC-2707. This is an epoxy glue with a thermal conductivity value of $0.72W/mK$ and the main reason for this choice is that this is not an expansive

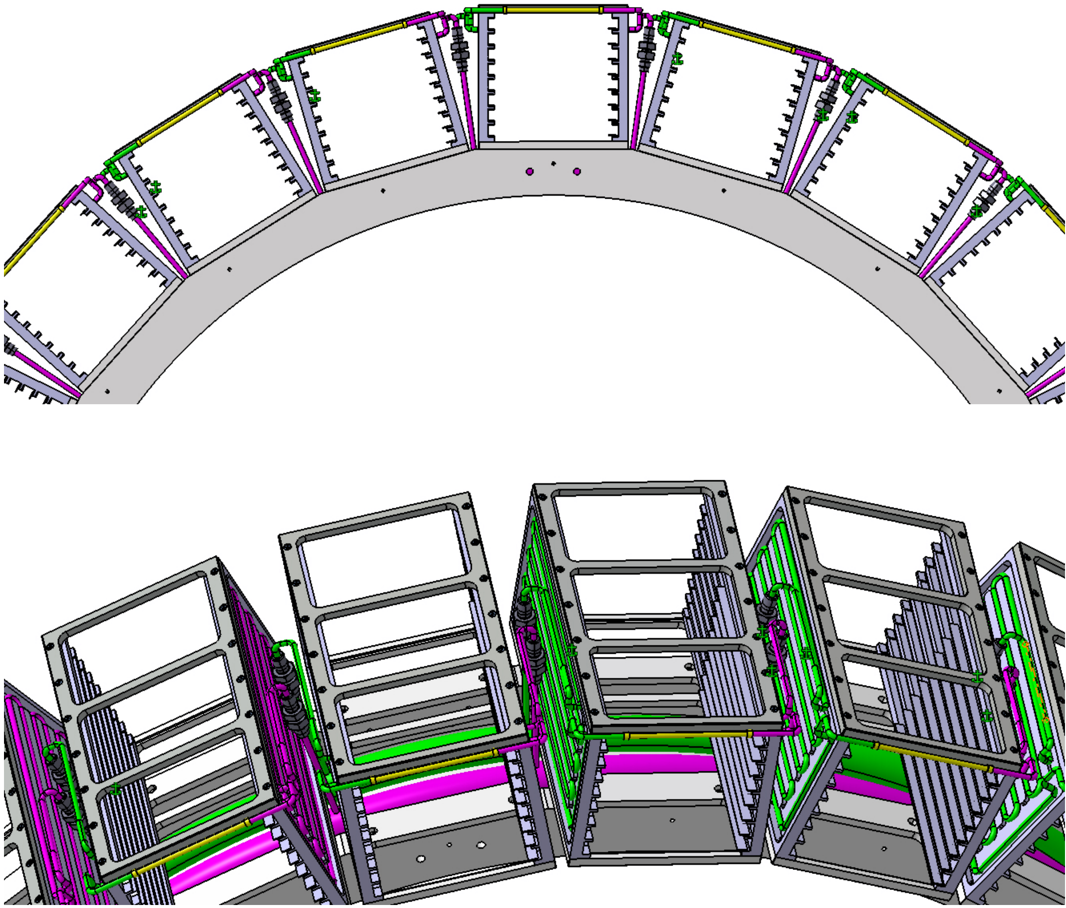


Figure 7.10: Views of the DAQ crates integrated with the cooling system

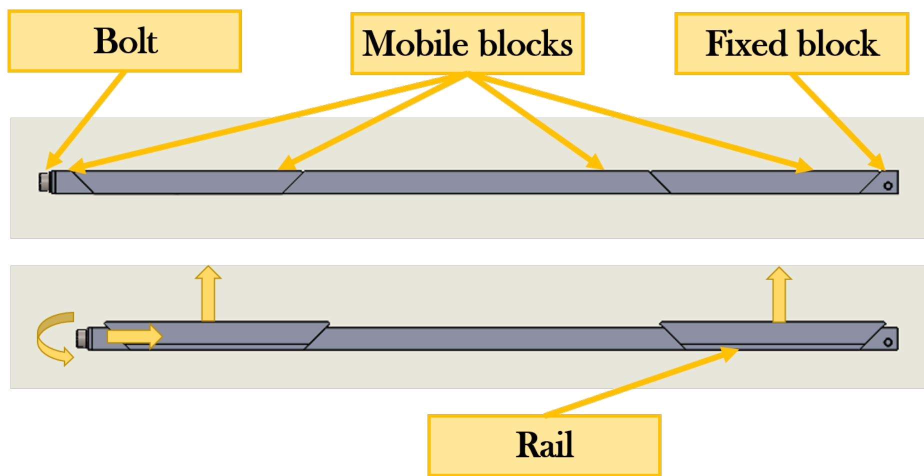


Figure 7.11: Cardlock mechanism

glue and the estimated thermal drop estimated in this condition is acceptable. If we assume a precautionary glue layer of 0.1 mm the relative thermal resistance is about $0.15K/W$.

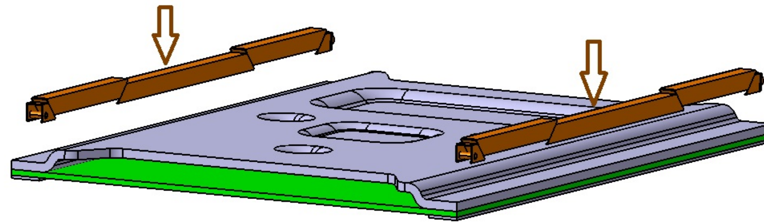


Figure 7.12: Positioning of the cardlocks over the glue film.

Once the cardlock is inserted into the crate, a minimum value of torque of $\approx 60N \cdot cm$ must be guaranteed.
This constraint should minimize thermal drops on the surfaces in contact, and it has been chosen after an accurate estimate of the thermal contact conductance (see Chapter 4). The cardlock datasheet reports only thermal properties measured at atmospheric pressure, so an accurate study of contact pressure as a function of the mechanical torque has been performed.

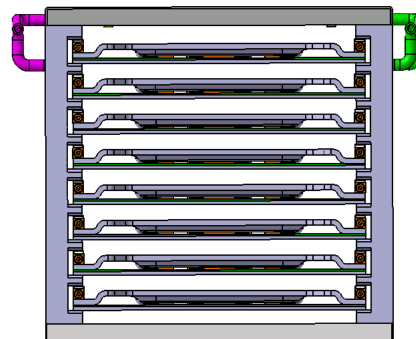


Figure 7.13: Insertion of the waveform digitizer and interface boards into DAQ crate slot. Note that the layout of the interface board has not been finalized yet, we strongly recommend an integration by cardlocks.

Since thermal contact conductance depends on roughness, an high precision of machine process is required for the fins (surface in contact with cardlock). We need $0.8\mu m$ level of roughness that can be reached by a milling process. More details for the manufacturing are explained in the technical drawings.

The design of the interface board has not been entirely finalized yet. Since the layout of the DAQ crates cooling system is completed, the interface board will have to be fixed to the same DAQ crate slots with cardlocks as the wavefmor digitizer boards.

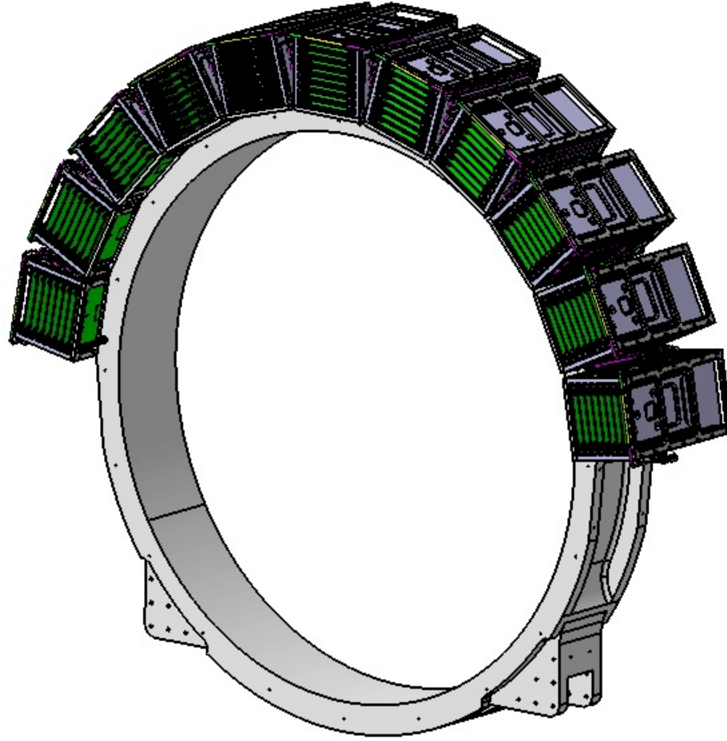


Figure 7.14: Completed view of the aluminum disk with the fully assembled DAQ cooling system.

Chapter 8

Conclusions

The physics motivation of the Mu2e experiment at Fermilab is the search for the neutrino-less coherent conversion of a muon to an electron in the electric field of an aluminum nucleus, a physics process which would be an unambiguous evidence of the existence of physics beyond the Standard Model. The experiment is currently in construction and is expected to begin data taking in the year 2020. The electromagnetic calorimeter is designed and is going to be constructed by a collaboration among the Italian Istituto Nazionale di Fisica Nucleare, the California Institute of Technology, and Fermilab. It is a wide collaboration which involves many groups of physicists and engineers. I have worked with the INFN Pisa, INFN-Frascati and the Fermilab groups, and I have taken part to a of a lot of meetings to present the progress of my work.
My research project has been the design of the cooling system of the Mu2e electromagnetic calorimeter and the development of the integration procedures of the system in the experimental area. The challenge of the calorimeter cooling is that the detector is installed inside the Mu2e cryostat which is evacuated at the pressure of 10^{-4} Torr. This is required to reduce the interactions of beam particles and muon decay products with gas, since this may produce undesired signals in the Mu2e detectors, which may mimic the conversion electron signal searched by the experiment. In this condition, the power generated by the electronic components can only be dissipated through conduction. The entire calorimeter electronics is divided in two main subsystems, with different functions and locations. The first subsystem is placed on the back side of the crystal disks and contains the photo-sensors and the front-end electronics. The second subsystem is located on the radial external side of the calorimeter. I have mainly worked on the design and on the thermal analysis of the DAQ crates and boards. It contains the data acquisition, power and monitor boards. The main function of the data acquisition boards is to digitize the analog signals received from the crystals front-end electronics and transfer these data to the Mu2e data acquisition for permanent storage. For this reason they are called "waveform digitizer" boards.The main function of the power and monitor boards is to provide the power to the front-end electronics and monitor the system performance. For this reason they are called "interface boards". I have designed the cooling system of the DAQ crates which host

the waveform digitizer and interface boards. This is a crucial project, since the reliability and performance of all electronic components depend critically on the local temperature. There is a total of 77 waveform digitizers and 77 interface boards per calorimeter disk, hosted in 11 DAQ crates per disk. The DAQ crates are placed externally to the disk in the radial direction. The crate function is to provide a mechanical support to the boards, but also a thermal path to extract the power dissipated by the electronics components with a cooling fluid flowing in pipes brazed on the DAQ crate walls.
The calorimeter cooling system is independent from the rest of the experimental apparatus and the cooling station used for the calorimeter is being designed by INFN mechanical engineers. The cooling fluid is a 35 % monopropylene glycol aqueous solution. Starting from an existing conceptual layout of the cooling system, my research project has been to define completely the architecture of the DAQ crates cooling system, its integration on the electromagnetic calorimeter and to perform and plan several thermal-vacuum tests in order to verify the performances of the entire cooling system.
The goal of the first part of my Thesis has been to develop the mechanical drawings of the DAQ crate (Fig. 8.1) and the bending template of the cooling pipe built at INFN mechanical workshop (Fig. 8.3). I have been responsible

Figure 8.1: DAQ crate wall during the manufacturing process.

to build the copper cooling pipe and to assemble the components (Fig. 8.3). I have also performed the thermal analysis of the electronic components installed on the waveform digitizer and interface board and I have verified that the cooling system is able to keep the maximum temperature of these components under their critical value. To do this I have used Ansys steady state thermal.
Thanks to a strong collaboration with INFN mechanical workshop and VCS S.r.l., we have built the first prototype of the DAQ crate. The INFN mechanical workshop has built the DAQ crate walls, while VCS has provided the cooling pipe with the VCR connection, and has been responsible of the brazing

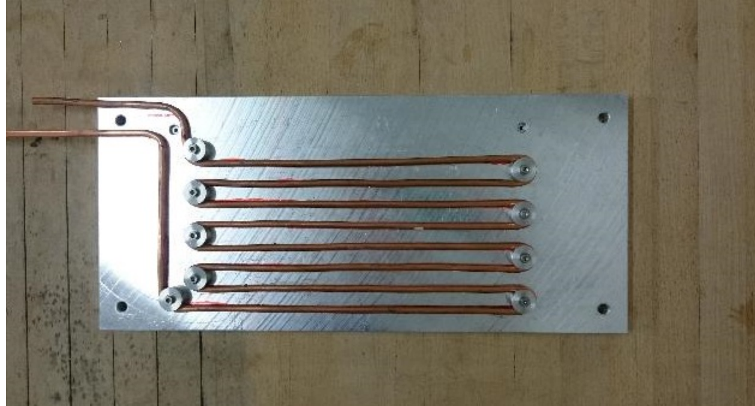


Figure 8.2: Cooling pipe built at INFN mechanical workshop.

processes.
The goal of the second part of my Thesis has been to integrate the cooling system with the rest of the structure, and to perform and plan several tests. For the hydraulic tests I have experimentally verified the prediction of the an-

Figure 8.3: DAQ crate during hydraulic test.

alytical model and I have verified that my design provides an adequate cooling of all the electronic components.
I concluded my work with the design of the necessary tests to verify the thermal and outgassing performance of the components and of the entire cooling system. These tests are going to be performed at INFN Pisa in the next few months.
A mock up of the electromagnetic calorimeter is currently under construction and will be assembled at INFN National Laboratory in Frascati where a prototype of the aluminum outer ring has already been built (Fig. 8.4). Future extensions of the work described in this Thesis include the integration of the prototype DAQ crate designed and built at INFN Pisa on the mock-up disk

Figure 8.4: Prototype of the aluminum outer ring of the electromagnetic calorimeter at the INFN National Laboratory in Frascati.

built at INFN Frascati.

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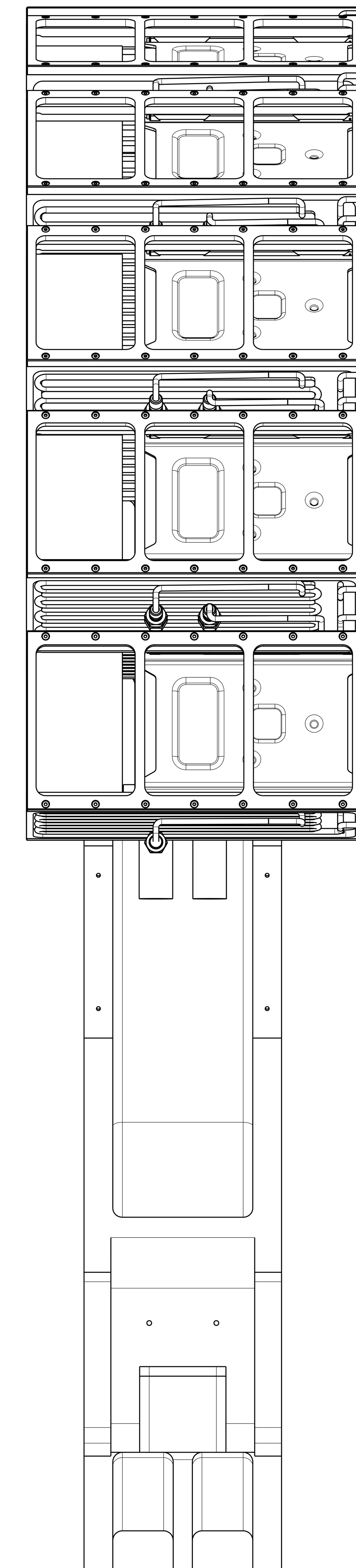
Appendix A

Technical drawings

4 5 3 1 2

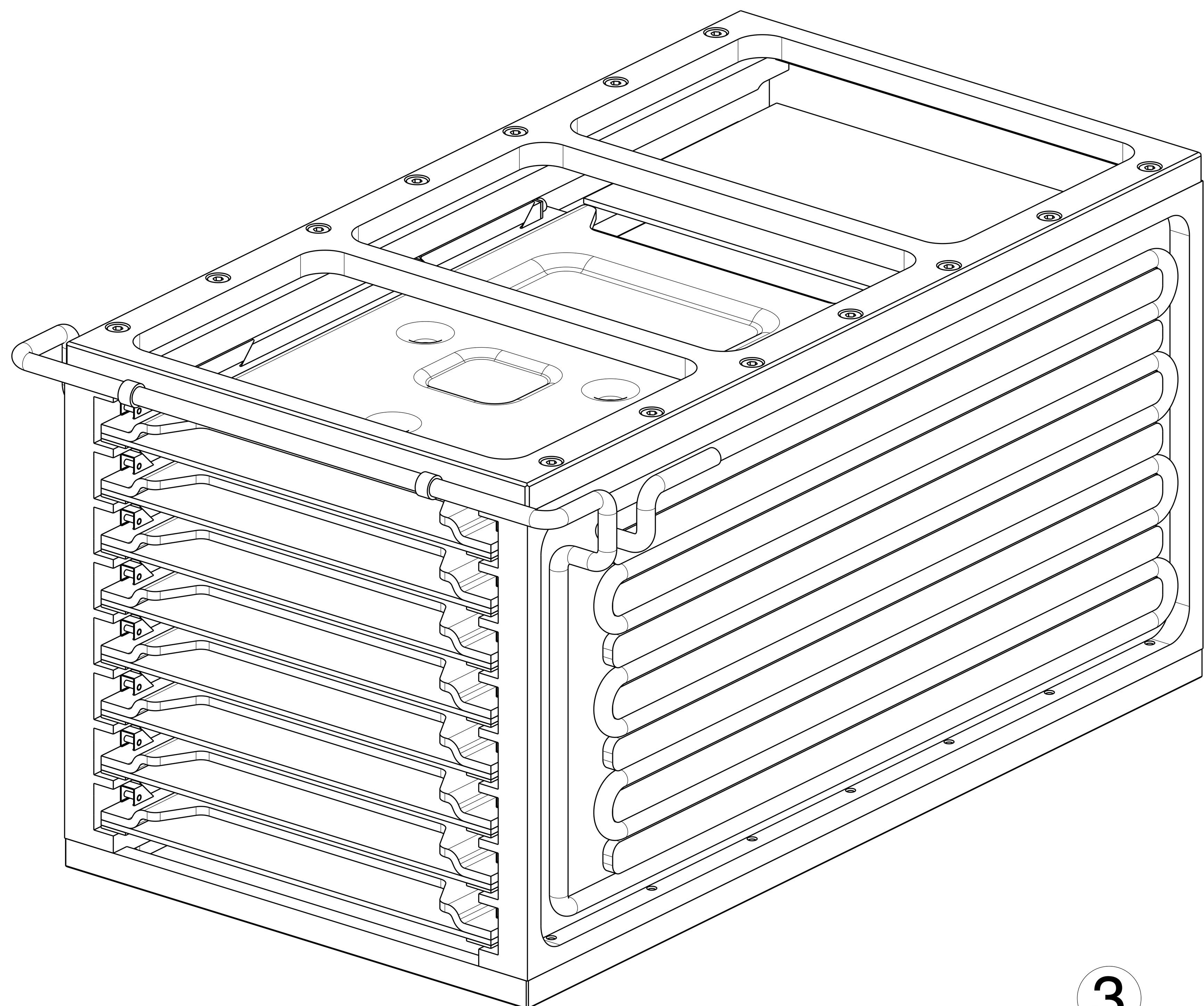
Vista frontale
Scala: 1:3



Pos.	Gruppo	Quantità
5	DAQ crates	11
4	Connettore VCR	22
3	Collettore	2
2	Supporto	3
1	Outer Ring	1

UNIVERSITA' DI PISA
INFN sez.ne di PISA

Denominazione:		Materiale:
Complessivo: DAQ crates		Foglio 1 di 1
Gruppo: Mu2e Project		Scala 1:1
Sottogruppo: Mu2e Calorimeter		Data 07/04/2016
TOLLERANZE GENERALI DI LAVORAZIONE	Misto	Disegnatore Gianmarco Ducci
	Appr.	Supervisor Ing. Fabrizio Raffaelli



Vista isometrica
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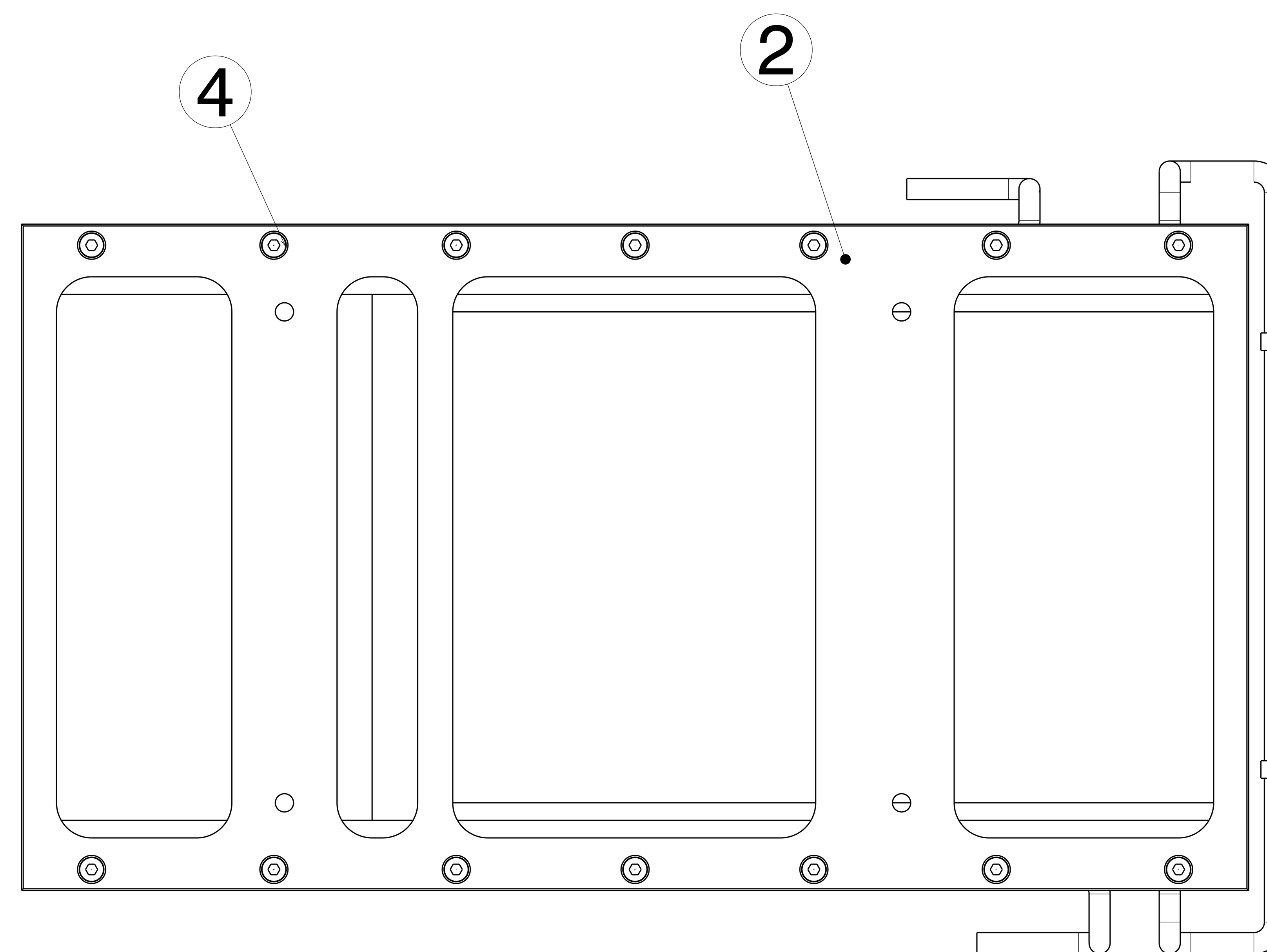

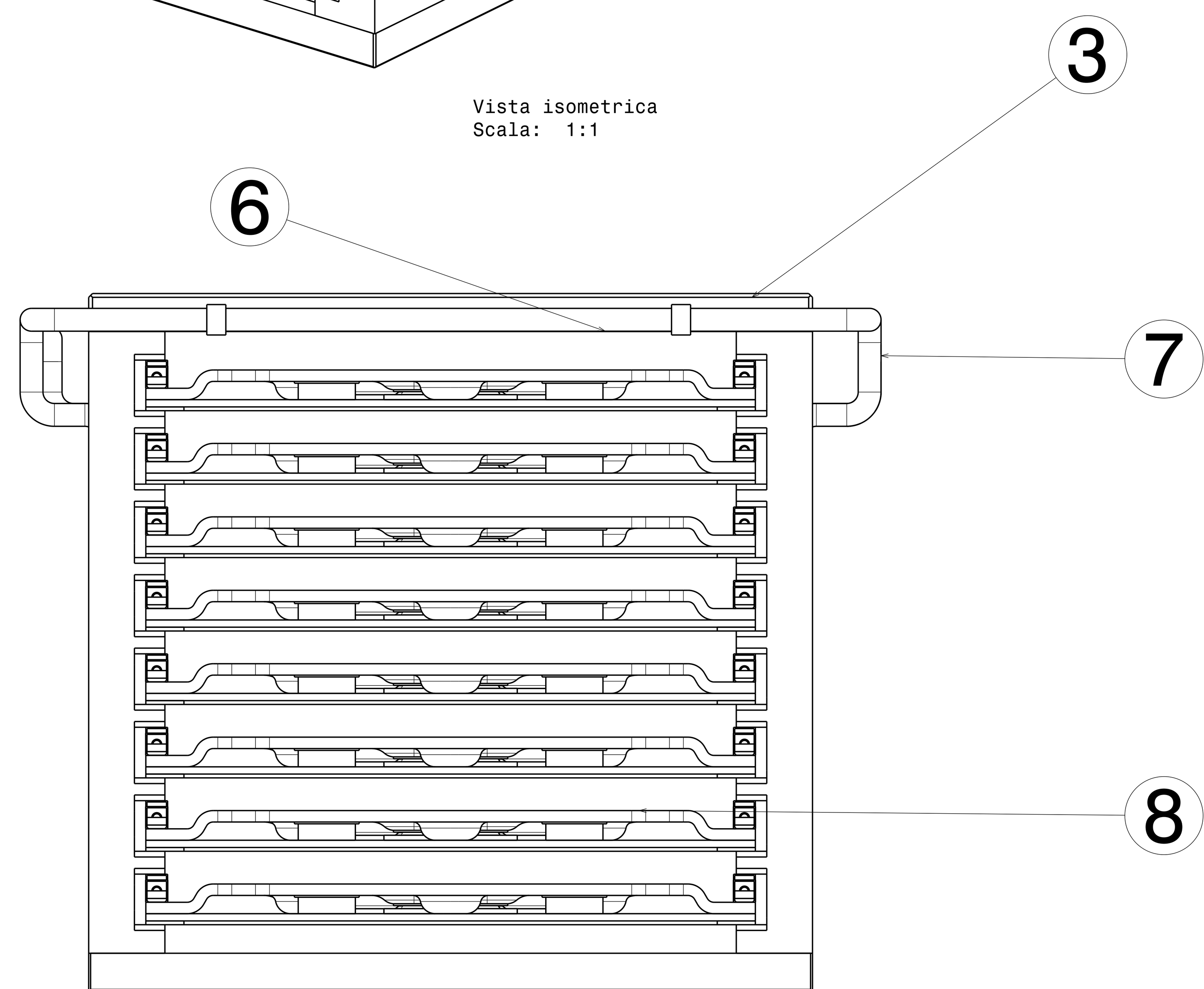

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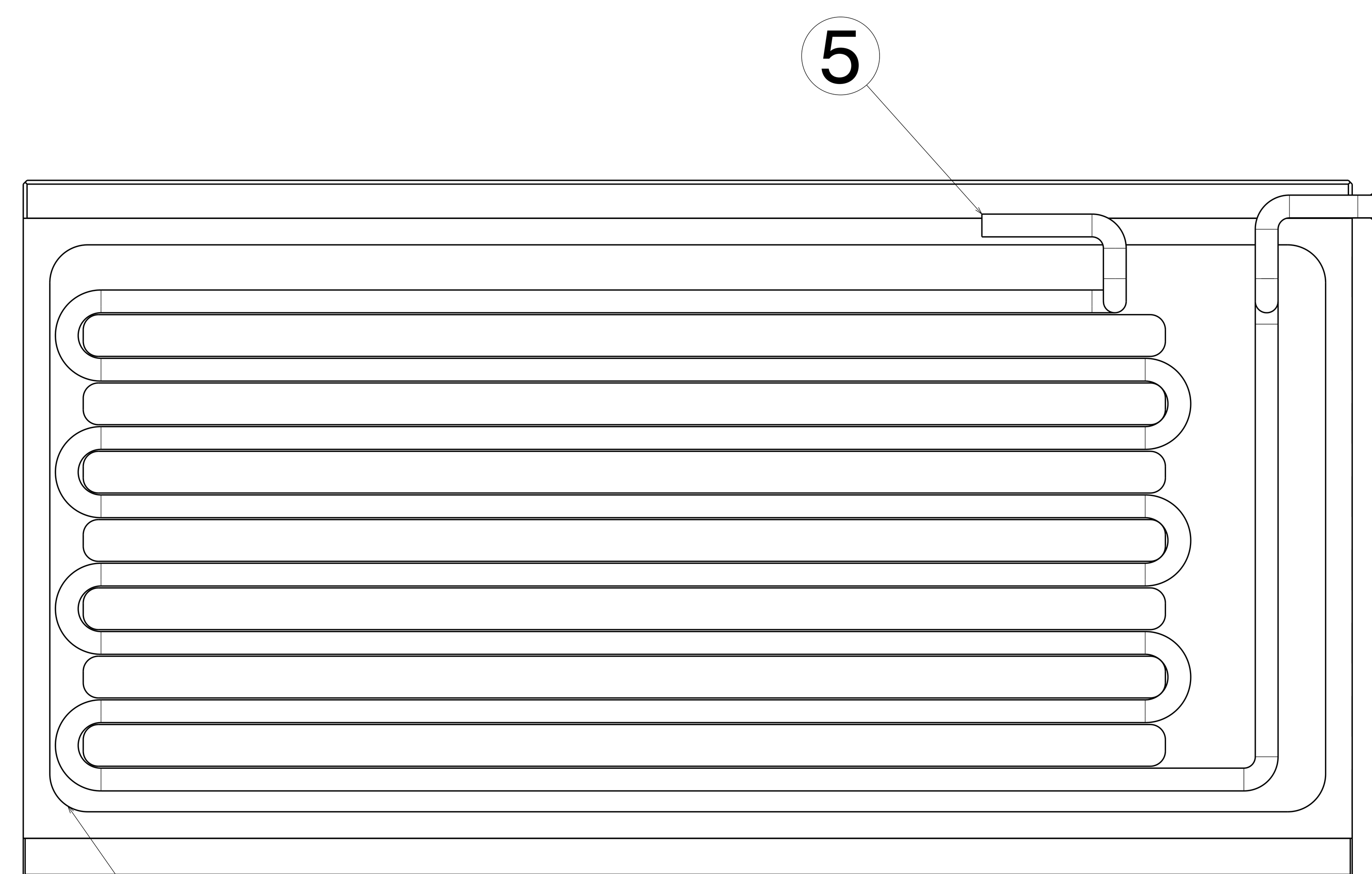
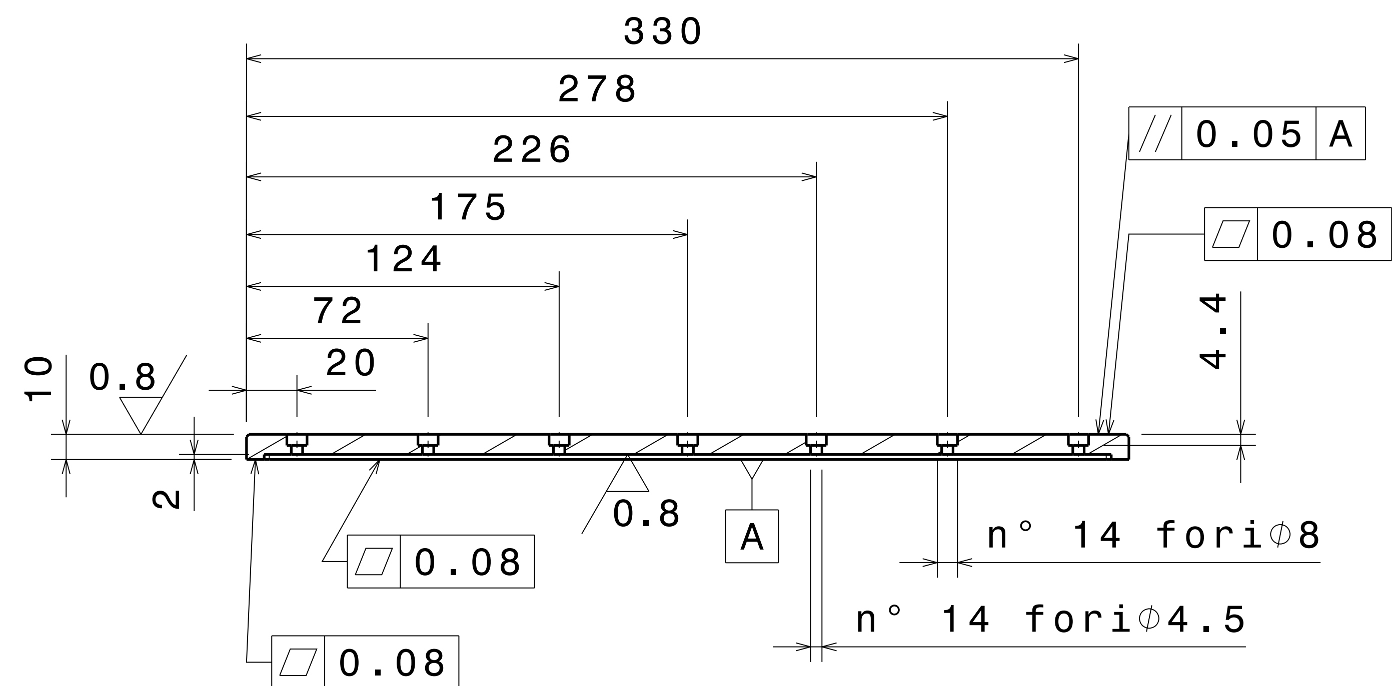


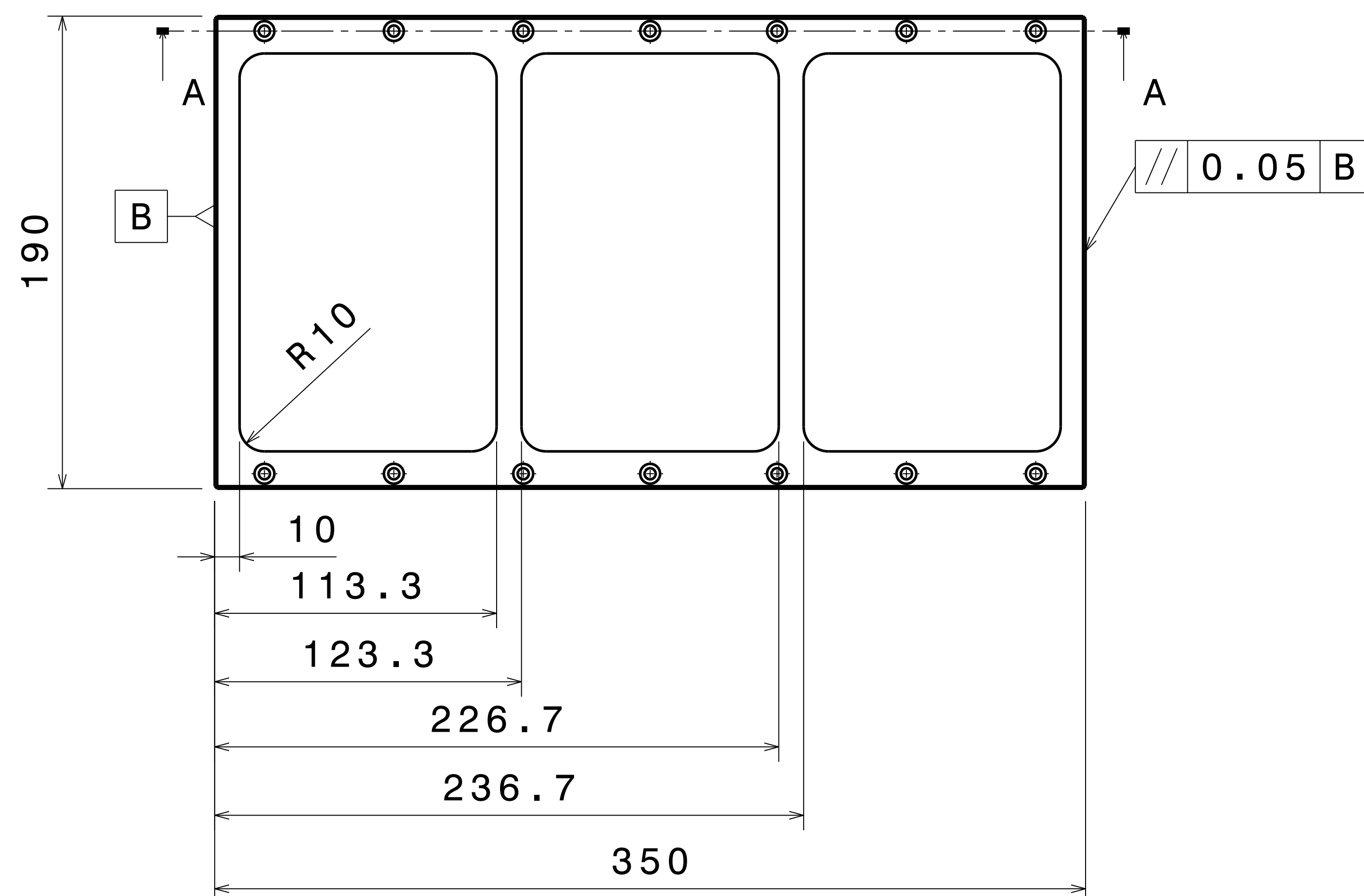
Vista da sinistra
Scala: 1:1

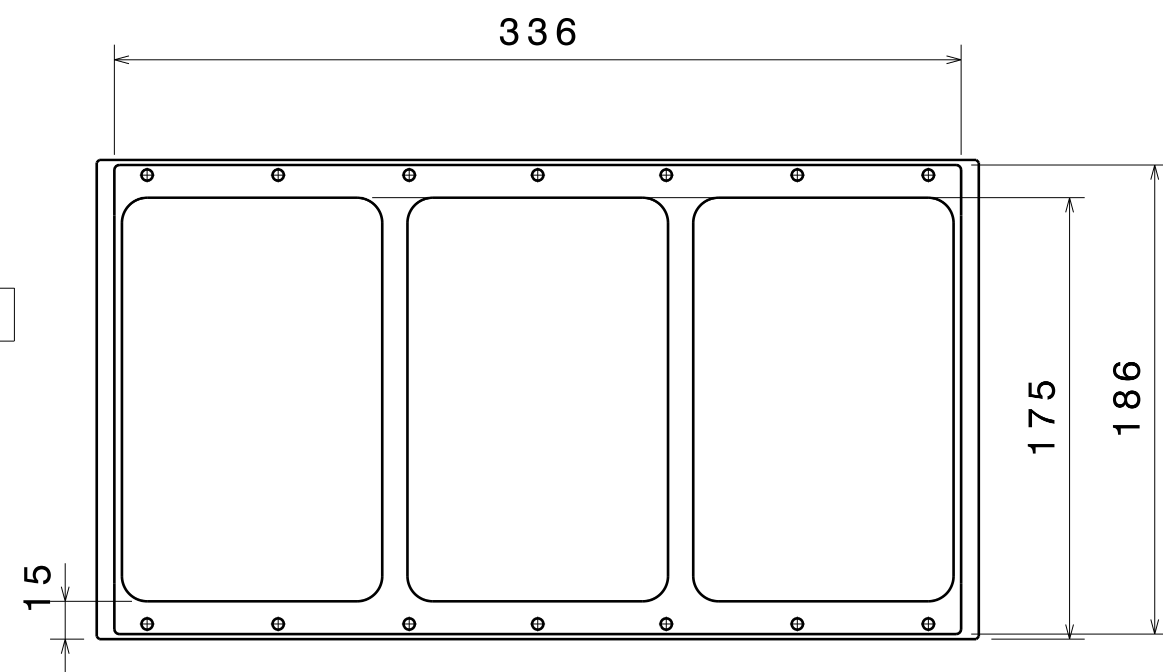
Pos.	Denominazione	Num.	Materiale
8	Waveform digitizer	8	
7	Serpentina lato 2	1	Cu-DHP R220
6	Connessione	1	Cu DHP R220
5	Serpentina lato 1	1	Cu-DHP R220
4	Vite UNI 5931 M4x60	28	
3	Create top	1	Al1100-O
2	Crate bottom	1	Peek
1	Crate side	2	Al1100-O

UNIVERSITA' DI PISA
INFN sez.ne di PISA

Denominazione: Pareti laterali	Materiale: Alluminio
Complessivo: Crate	Foglio 1 di 1
Gruppo: Mu2e Project	Scala 1:1
Sottogruppo: Mu2e Calorimeter	Data 07/04/2016
TOLLERANZE GENERALI DI LAVORAZIONE / Grado di precisione medio — Misto	Disegnatore Gianmarco Ducci
Appr.	Supervisor Ing. Fabrizio Raffaelli







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COMPLESSIVO	Denominaz. Mu2e calorimeter		FOGLIO 1 di 1
GRUPPO	Denominaz.: Crate		SCALA 1:3
SOTTOGRUPPO	Denominaz.:		DATA 10/07/2016
TOLLER. GENER. DI LAVORAZIONE	TRATT. TERMICI	Sostituisce il	Dis. Gianmarco Ducci
		Sostituito dal	App. Fabrizio Raffaelli

Sezione A-A

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n° 4 fori Φ6.2

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A

B

R10

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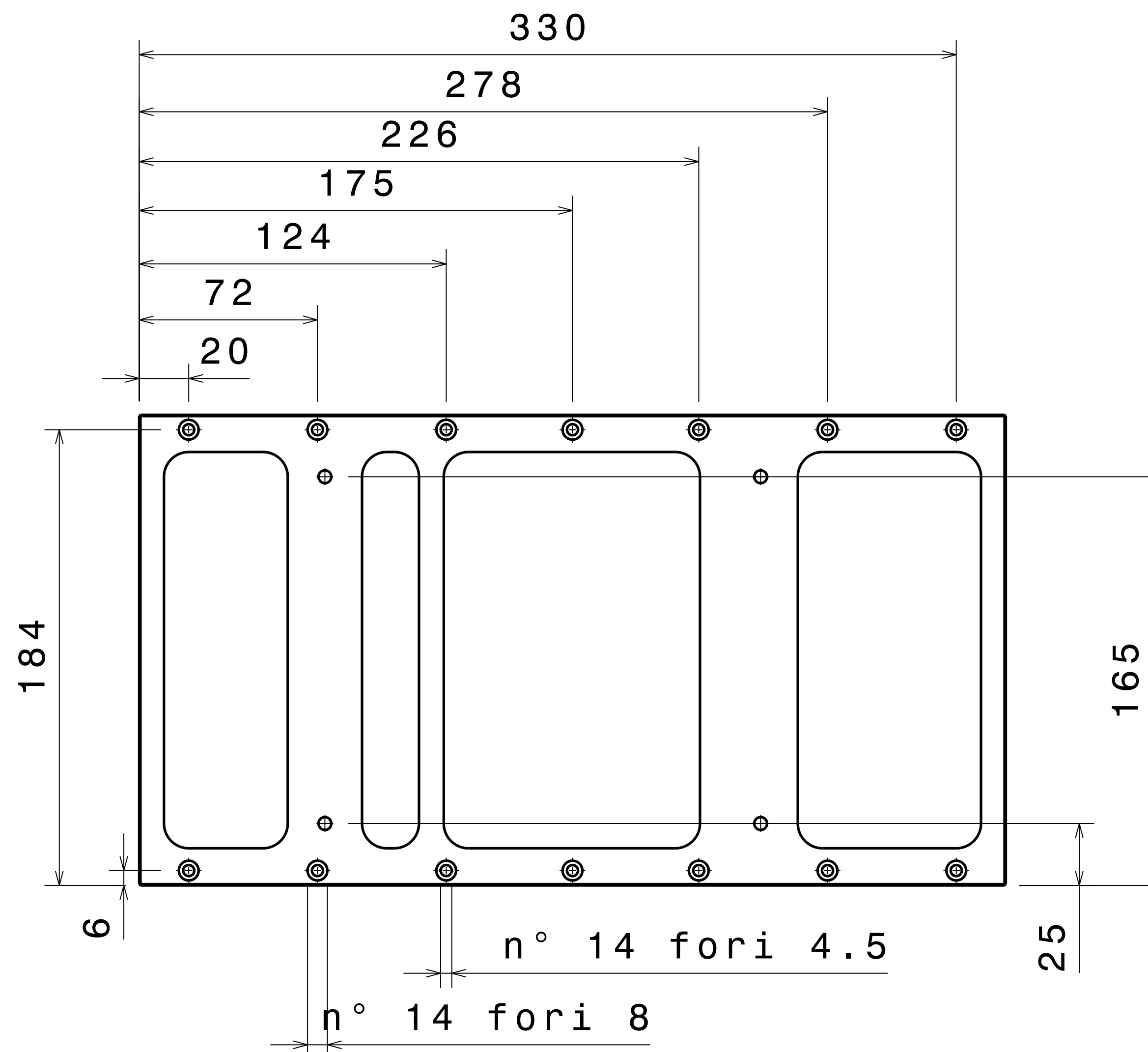
340



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SOTTOGRUPPO	Denominaz.:		DATA 07/07/2016
TOLLER. GENER. DI LAVORAZIONE	TRATT. TERMICI	Sostituisce il	Gianmarco Ducci
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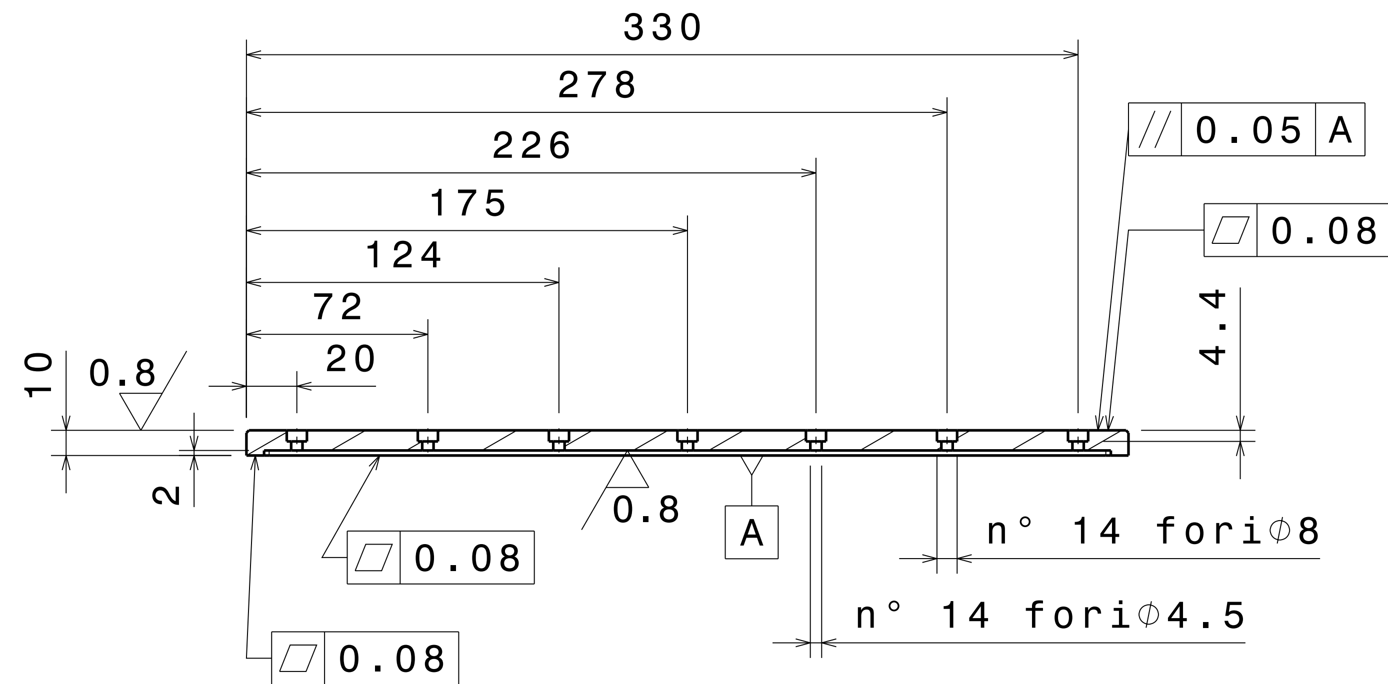

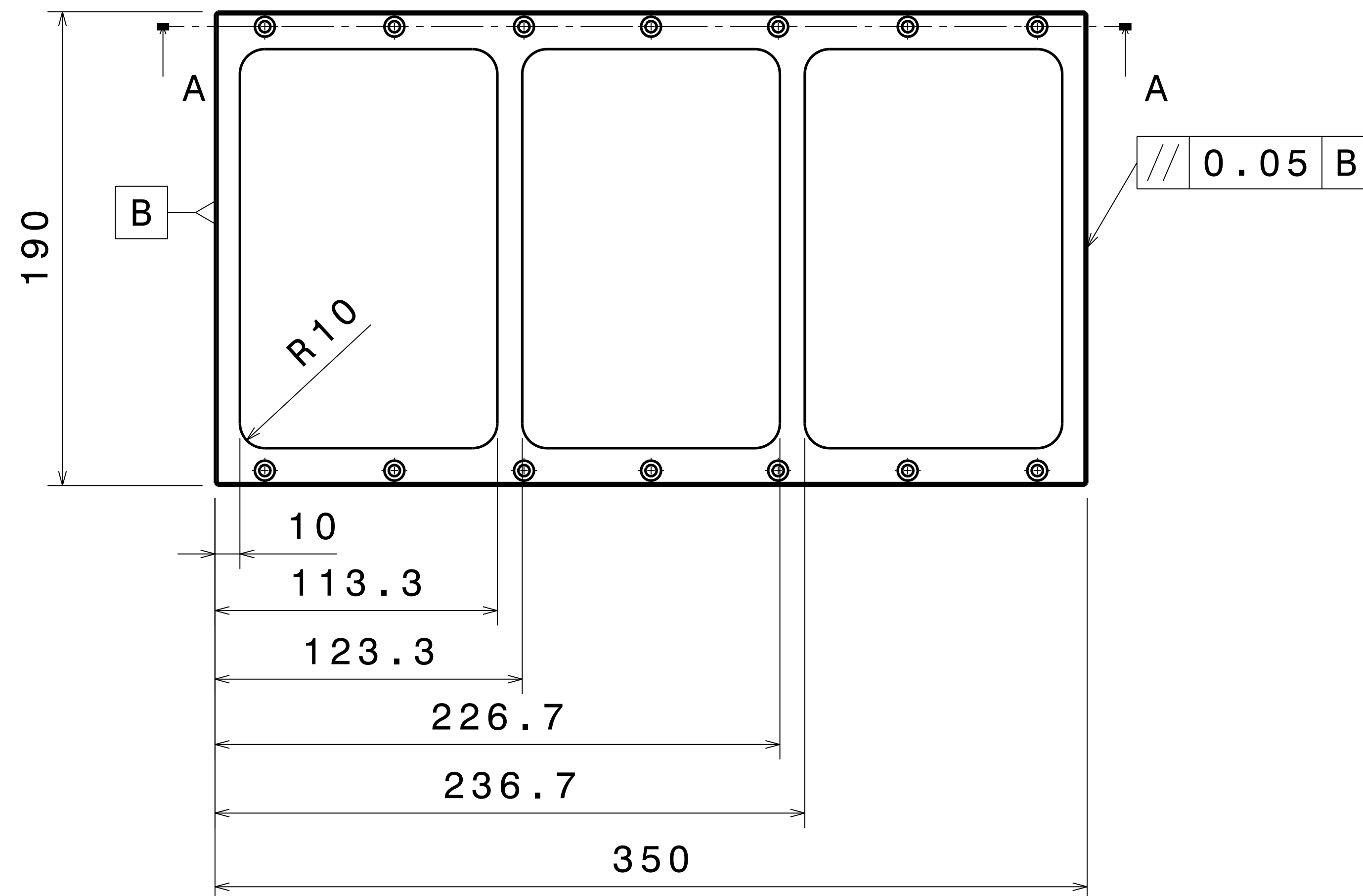

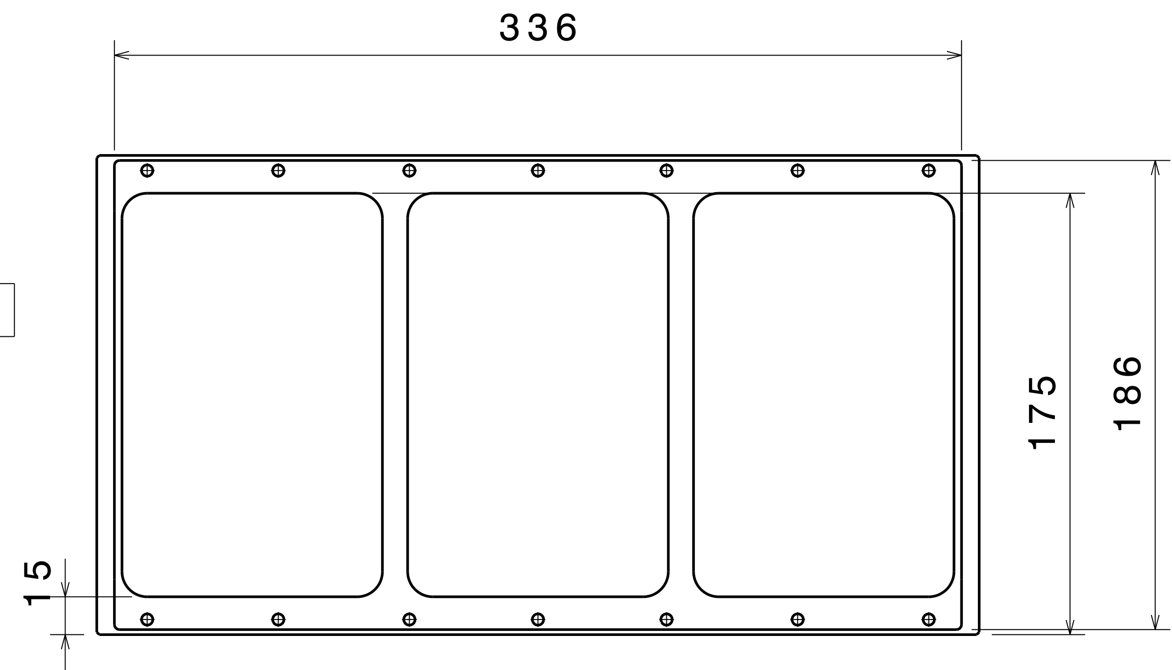

UNIVERSITA' DEGLI STUDI DI PISA
FACOLTA' D'INGEGNERIA

PARTICOL.N°3	Denominaz.: Crate top		MATERIALE Al1100-O
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GRUPPO	Denominaz.: Crate		SCALA 1:3
SOTTOGRUPPO	Denominaz.:		DATA 10/07/2016
TOLLER. GENER. DI LAVORAZIONE	TRATT. TERMICI	Sostituisce il	Dis. Gianmarco Ducci
		Sostituito dal	App. Fabrizio Raffaelli

Tutti i raggi non quotati: R10

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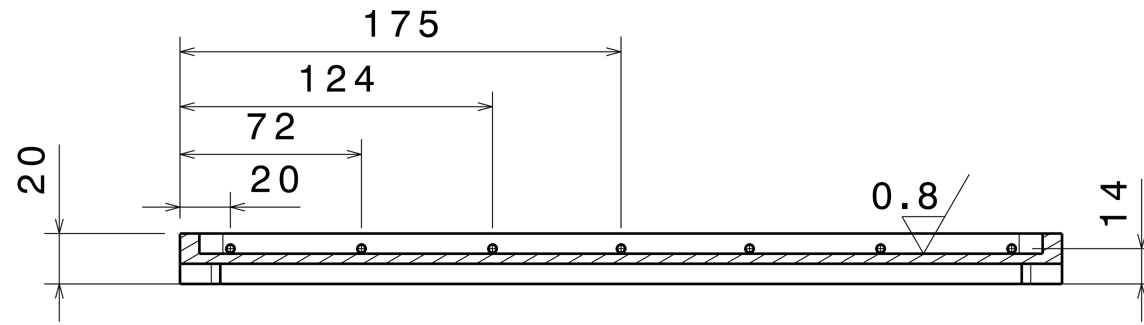

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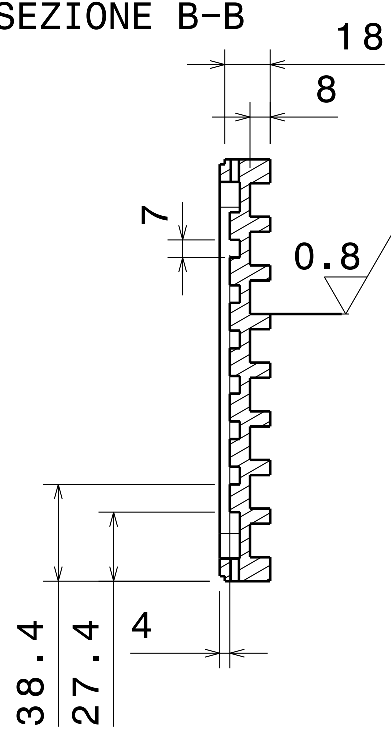

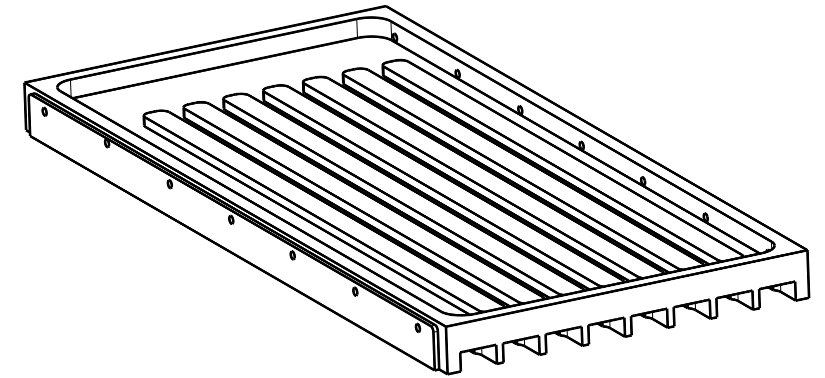

Vista isometrica
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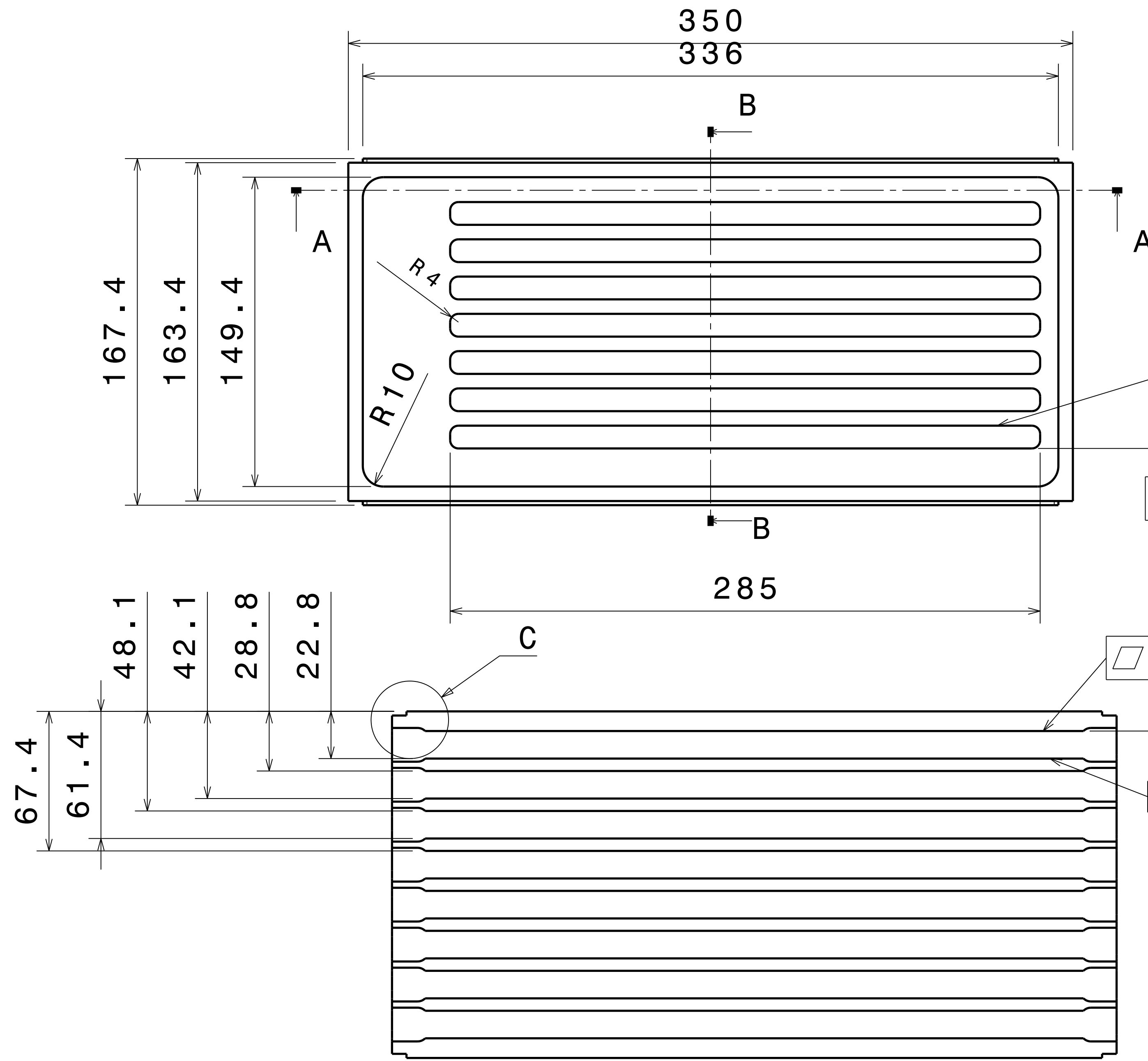

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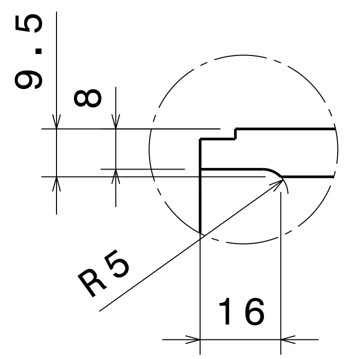

Dettaglio C
Scala 2:3

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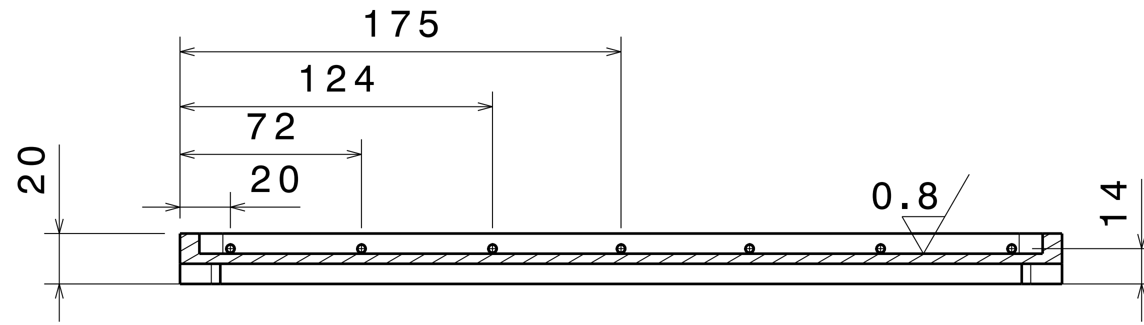
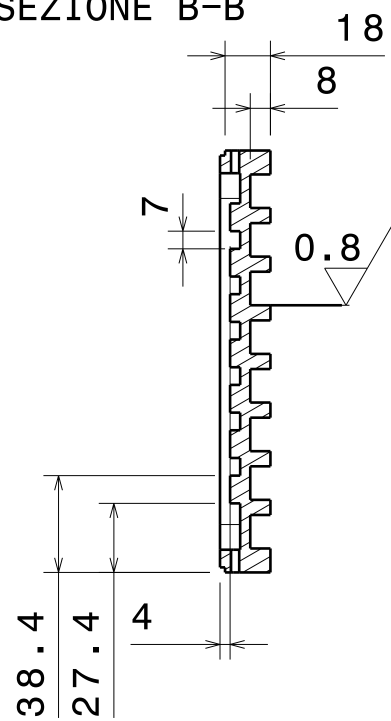
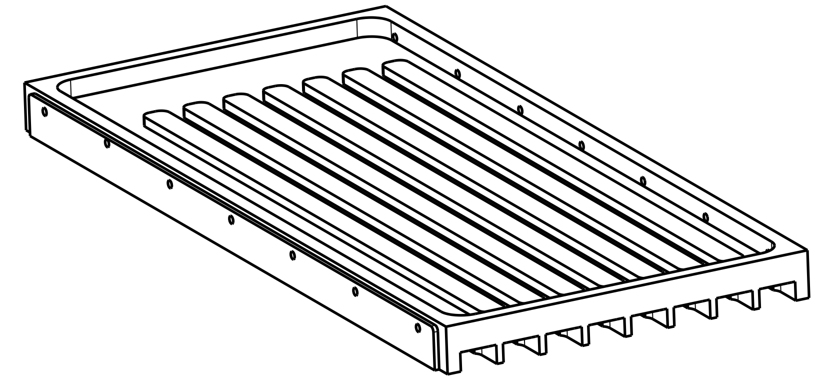
COMPLESSIVO	Denominazione Mu2e calorimeter		FOGLIO 1 di 1
GRUPPO	Denominaz.: Crate		SCALA 1:3
SOTTOGRUPPO	Denominaz.:		DATA 10/07/2016
TOLLER. GENER. DI LAVORAZIONE	TRATT. TERMICI	Sostituisce il	Dis Gianmarco Ducci
		Sostituito dal	App Fabrizio Raffaelli

SEZIONE A-A

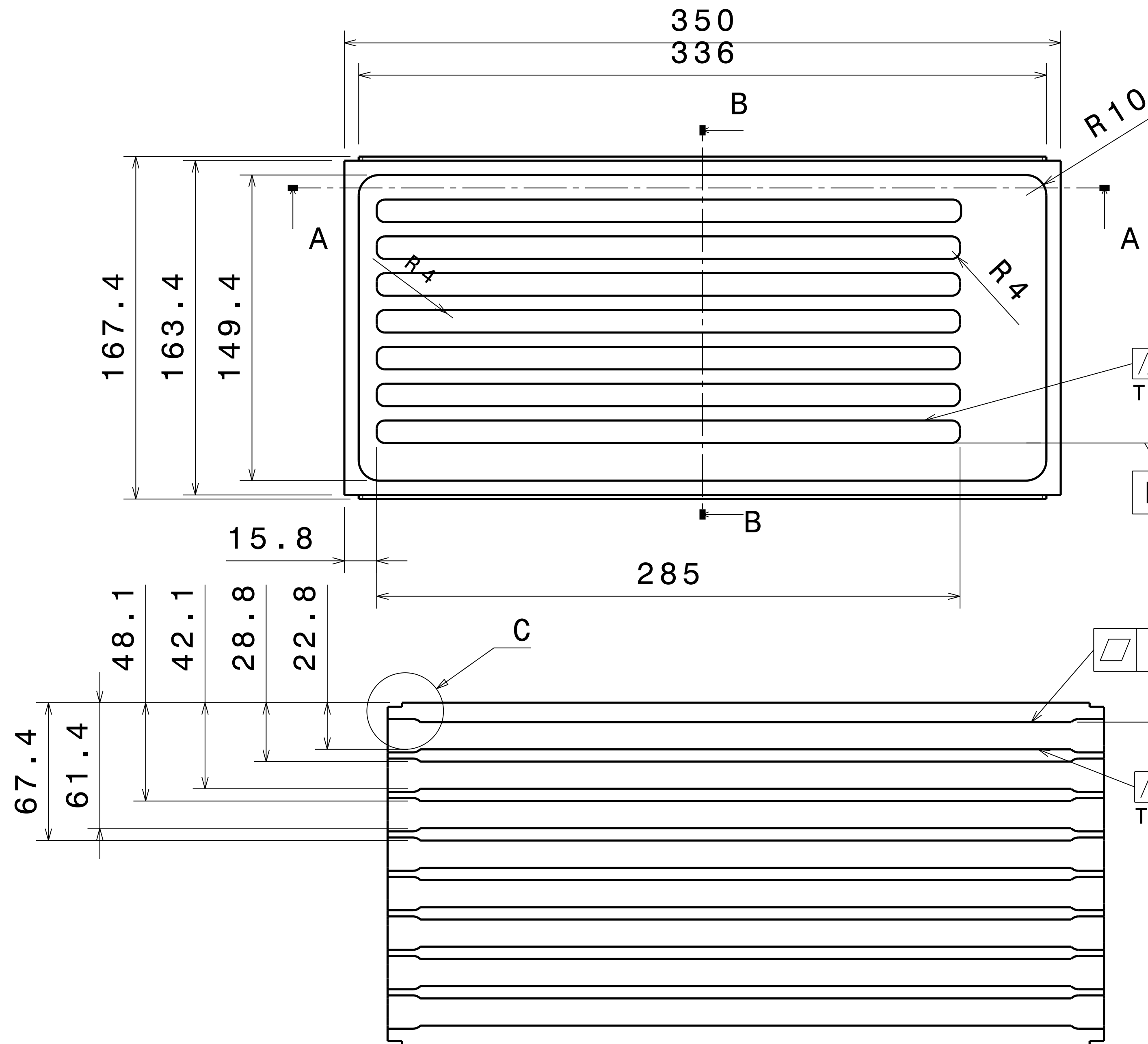


SEZIONE B-B





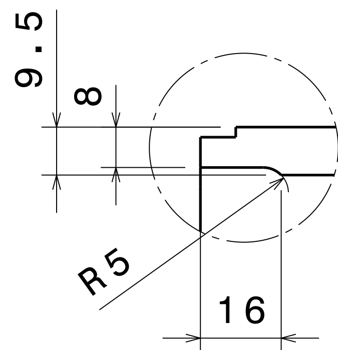
Vista isometrica
Scala: 1:3



// 0.05 B
Tolleranza da rispettare per ogni scanalatura

B

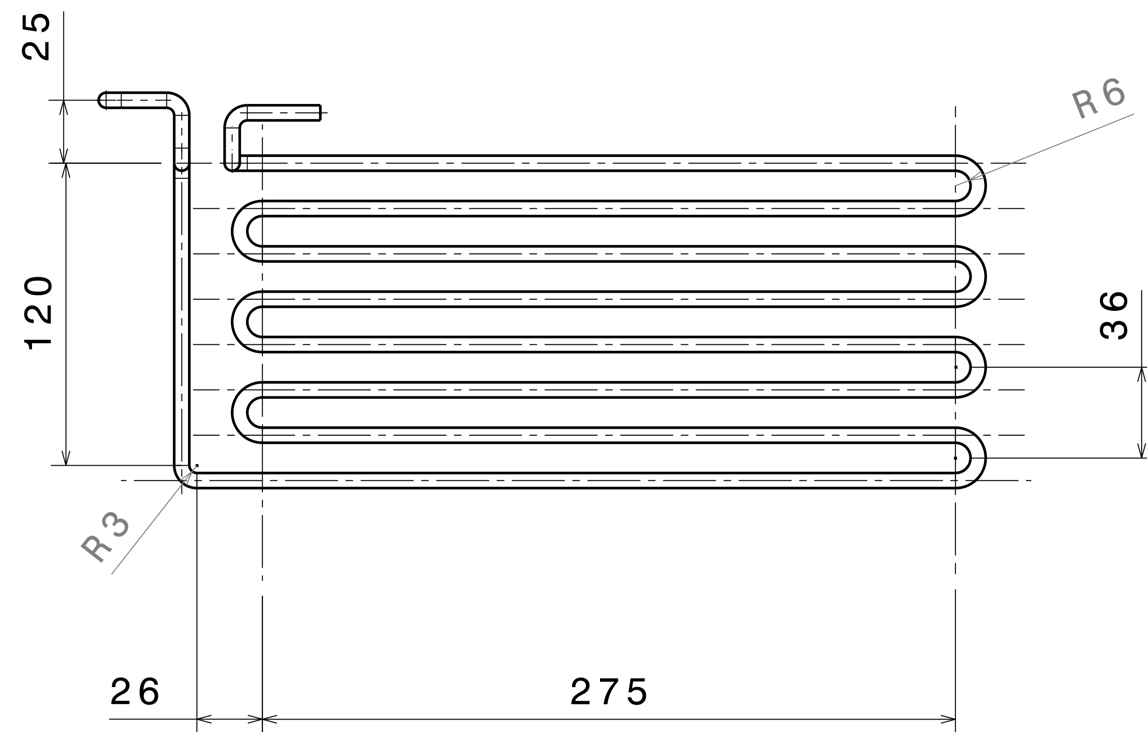
// 0.05 A
Tolleranza da rispettare per ogni scanalatura

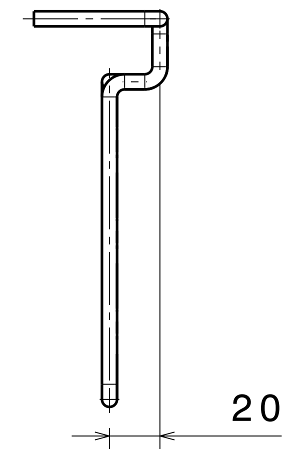


Dettaglio C
Scala 2:3

UNIVERSITA' DEGLI STUDI DI PISA
FACOLTA' D'INGEGNERIA

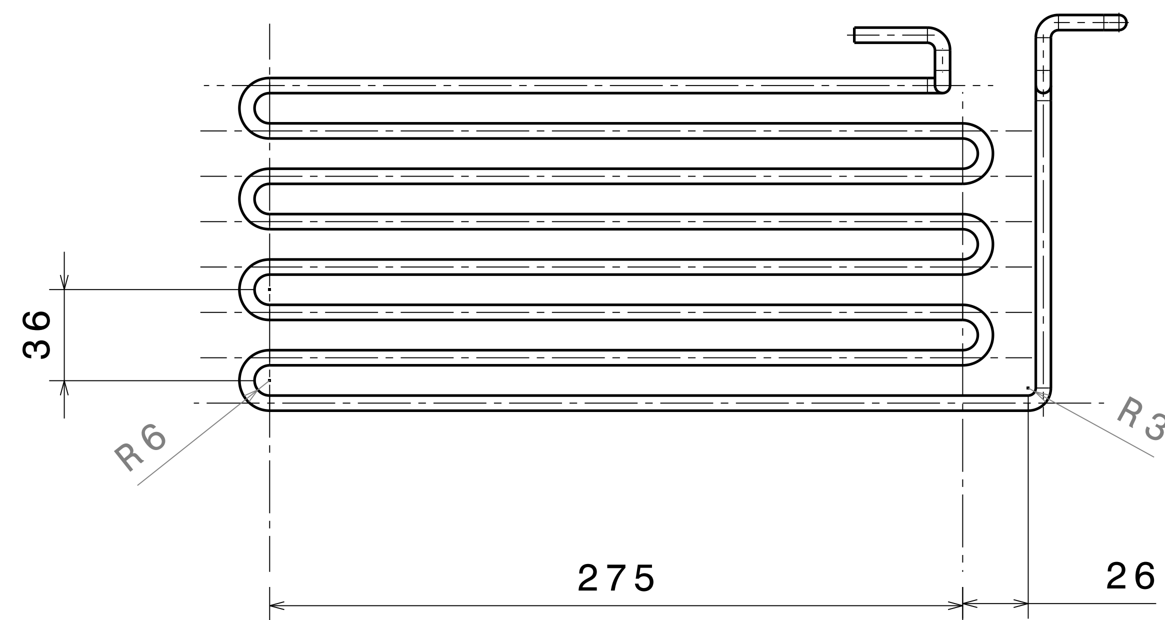
PARTICOL.N°1	Denominazione Crate side 2		MATERIALE Al1100-O
COMPLESSIVO	Denominazione Mu2e calorimeter		FOGLIO 1 di 1
GRUPPO	Denominaz.: Crate		SCALA 1:3
SOTTOGRUPPO	Denominaz.:		DATA 10/07/2016
TOLLER. GENER. DI LAVORAZIONE	TRATT. TERMICI	Sostituisce il	Dis Gianmarco Ducci
		Sostituito dal	App Fabrizio Raffaelli

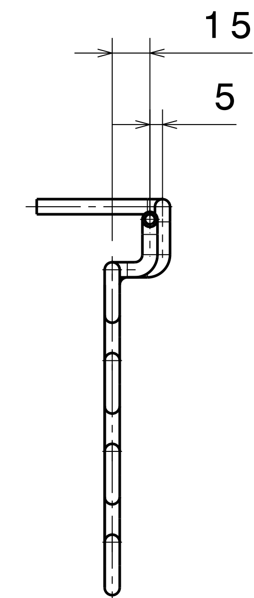




UNIVERSITA' DEGLI STUDI DI PISA
FACOLTA' D'INGEGNERIA

PARTICOL.N°1	Denominaz.: Serpentina lato 1		MATERIALE Cu DHP
COMPLESSIVO	Denominaz. Mu2e calorimeter		FOGLIO 1 di 1
GRUPPO	Denominaz.: Crate		SCALA 1:3
SOTTOGRUPPO	Denominaz.:		DATA 10/07/2016
TOLLER. GENER. DI LAVORAZIONE	TRATT. TERMICI	Sostituisce il	Dis Gianmarco Ducci
		Sostituito dal	App Fabrizio Raffaelli





UNIVERSITA' DEGLI STUDI DI PISA FACOLTA' D'INGEGNERIA			
PARTICOL.N°1	Denominaz.: Serpentina lato 2		MATERIALE Cu DHP
COMPLESSIVO	Denominaz. Mu2e calorimeter		FOGLIO 1 di 1
GRUPPO	Denominaz.: Crate		SCALA 1:3
SOTTOGRUPPO	Denominaz.:		DATA 10/07/2016
TOLLER. GENER. DI LAVORAZIONE	TRATT. TERMICI	Sostituisce il	Dis Gianmarco Ducci
		Sostituito dal	App Fabrizio Raffaelli

n° 3 fori Φ9 passanti

R703

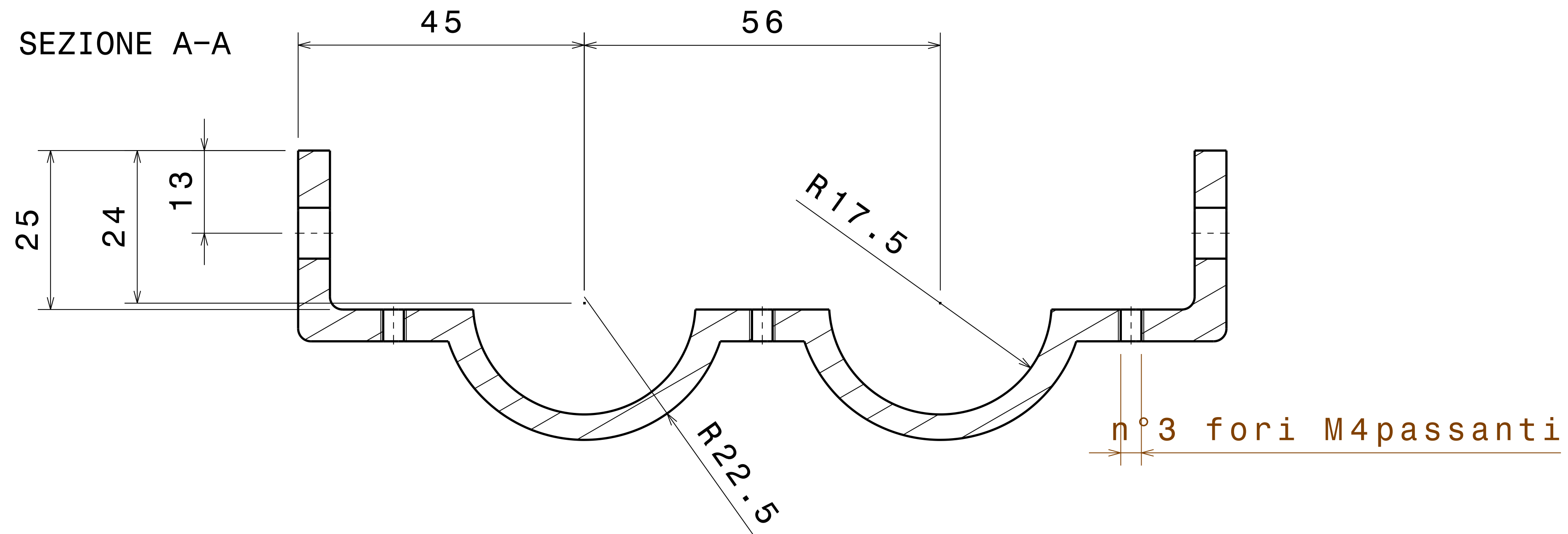
5°

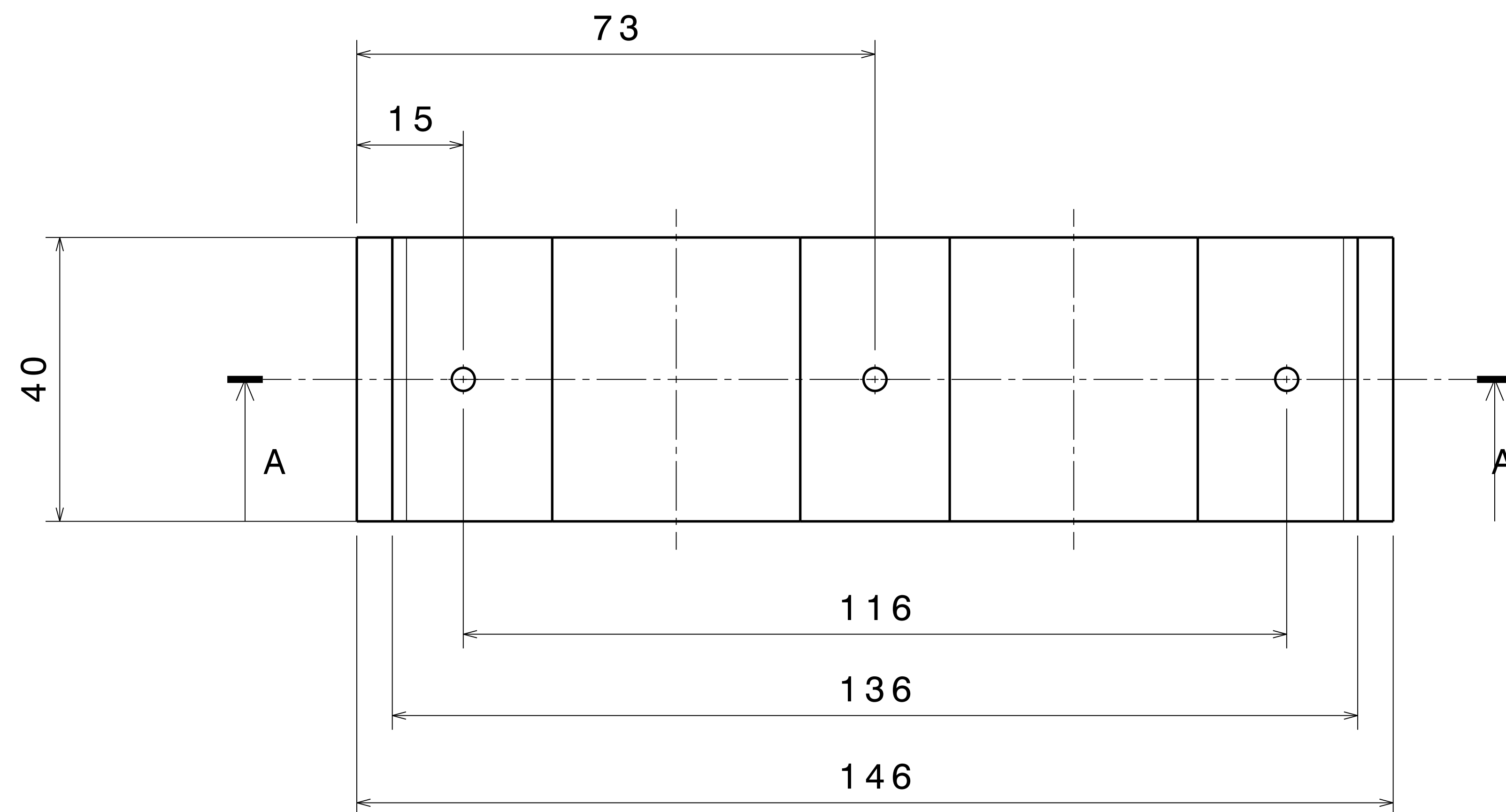
5°

UNIVERSITA' DEGLI STUDI DI PISA
FACOLTA' D'INGEGNERIA

INFN Istituto Nazionale di Fisica Nucleare

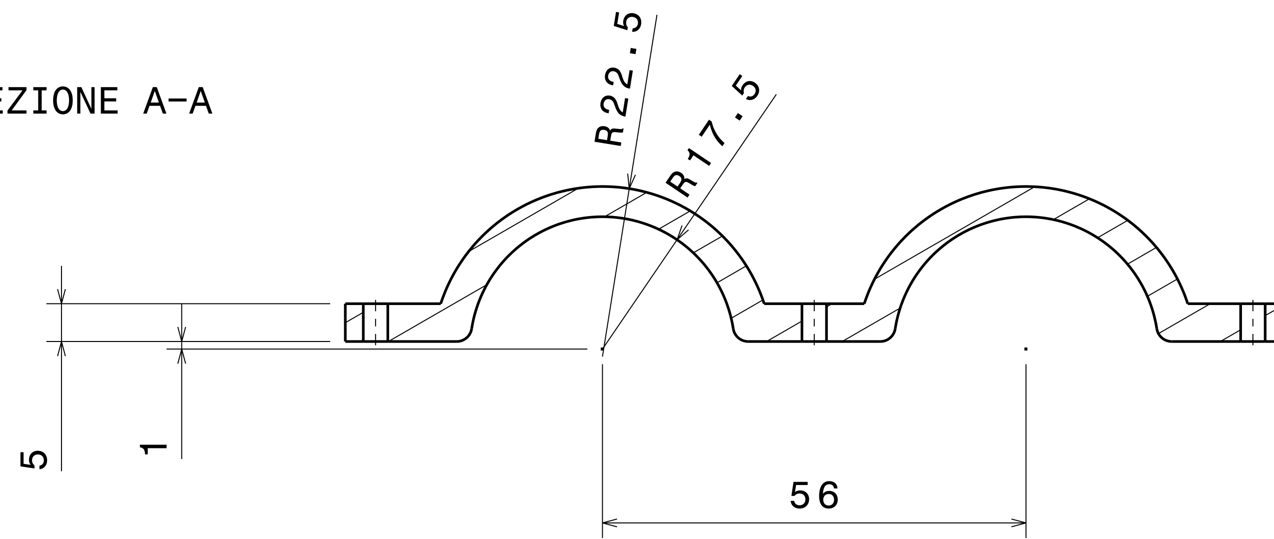
INTERFACCIA	Denominaz.: Lavorazione anello		MATERIALE
COMPLESSIVO	Denominaz. Mu2e calorimeter		FOGLIO 1 di 1
GRUPPO	Denominaz.: Crate		SCALA 1:3
SOTTOGRUPPO	Denominaz.:		DATA 10/07/2016
TOLLER. GENER. DI LAVORAZIONE	TRATT. TERMICI	Sostituisce il	Dis Gianmarco Ducci
		Sostituito dal	App Fabrizio Raffaelli

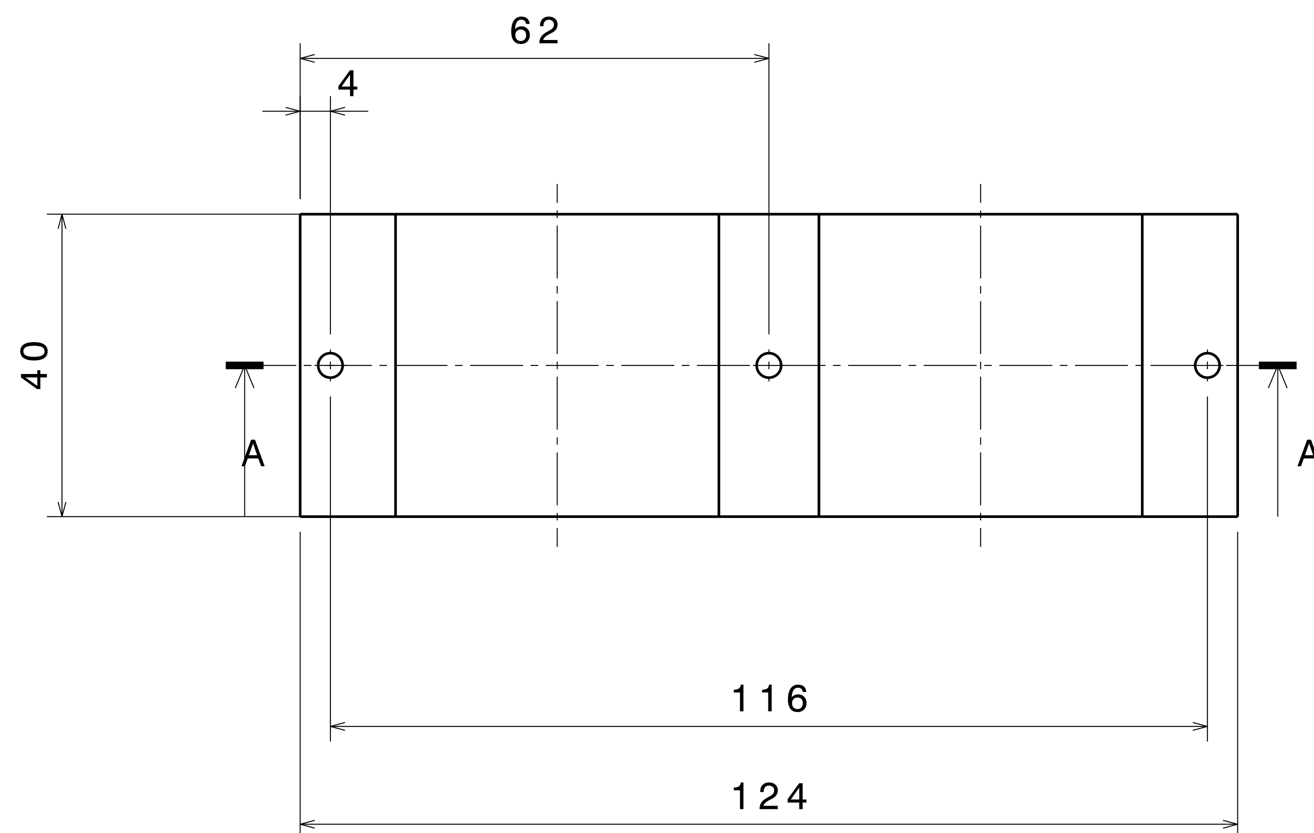




UNIVERSITA' DEGLI STUDI DI PISA
FACOLTA' D'INGEGNERIA

PARTICOL.N°1	Denominaz.: Supporto		MATERIALE FR 4
COMPLESSIVO	Denominaz. Mu2e calorimeter		FOGLIO 1 di 1
GRUPPO	Denominaz.: Crate		SCALA 1:1
SOTTOGRUPPO	Denominaz.:		DATA 10/07/2016
TOLLER. GENER. DI LAVORAZIONE	TRATT. TERMICI	Sostituisce il	Dis Gianmarco Ducci
		Sostituito dal	App Fabrizio Raffaelli





UNIVERSITA' DEGLI STUDI DI PISA FACOLTA' D'INGEGNERIA			
PARTICOL.N°1	Denominaz.: Tappo supporto		MATERIALE FR 4
COMPLESSIVO	Denominaz. Mu2e calorimeter		FOGLIO 1 di 1
GRUPPO	Denominaz.: Crate		SCALA 1:1
SOTTOGRUPPO	Denominaz.:		DATA 10/07/2016
TOLLER. GENER. DI LAVORAZIONE	TRATT. TERMICI	Sostituisce il	Dis Gianmarco Ducci
		Sostituito dal	App Fabrizio Raffaelli

Appendix B

Analysis of the DAQ crate bolt connection

We verified the screw connection between the DAQ crate and the outer ring. The worst case is when the DAQ crate is in the horizontal position with respect to the outer ring. For a conservative estimate of the load conditions, we have considered a total mass of one crate of $m \approx 20\ kg$. For this connection we have used M5 A2 70 stainless steel screws. We refer to Figure B.2. where:

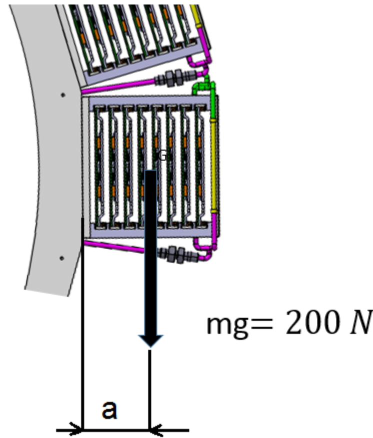


Figure B.1: Load condition used in order to verify the screw connection.

- b= 88 mm;
- h= 70 mm;
- a= 84 mm.

We report the procedure for the estimate.

$$T = 200\ N$$
$$T_{yi} = \frac{T}{4} = 50\ N$$

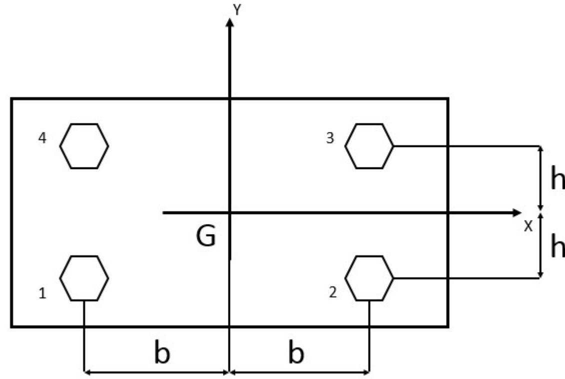


Figure B.2: 2D sketch of the screws position.

Note that the force T is the shear force and is the same value for each screw.
With respect to the reference system of Figure B.2 we have evaluated the bending moment around x-axis:

$$M_x = mg\ a \approx 16800\ Nmm$$

The normal force for each screw is given by the equation:

$$N_{x,i} = \frac{M_x Y_i}{\sum_{j=1}^{4} \left(Y_b\right)^2}$$

The screws 1 and 4 are clearly the most critical.

$$N_{x,3} = N_{x,4} = 60\ N$$

We will verify this connection. Let us call the preload force N_0:

$$N_0 = 0.8 \cdot A_r \cdot \sigma_{el} \approx 5000\ N$$

The total shear force that the connection can guarantee is:

$$T_{max} = 2 \cdot \frac{0.3N_0}{1.25} + 2 \cdot \frac{0.3(N_0 - N_i)}{1.25} \approx 4700\ N > mg$$

We have also verified the condition:

$$0.8N_0 = 4000\ N > N_{3,4} = 60\ N$$

Let us call $\sigma_{b,amm} = 373\ MPa$ and $\tau_{b,amm} = 264\ MPa$ for the A2 class of resistance and $\sigma_b = \frac{60\ N}{12.5\ mm^2} \approx 5\ MPa$ and $\tau_b = \frac{50\ N}{12.5\ mm^2} \approx 4\ MPa$
We want to verify that:

$$\phi_t = \left(\frac{\sigma_b}{\sigma_{b,amm}}\right)^2 + \left(\frac{\tau_b}{\tau_{b,amm}}\right)^2 \approx 4 \cdot 10^{-4} < 1$$

Appendix C

Dividing manifold flat end design

The design of the dividing manifold flat end respect the EN 13445-3 regulation. With respect to the figure C.1, the regulation EN 13445-3 imposes to determine

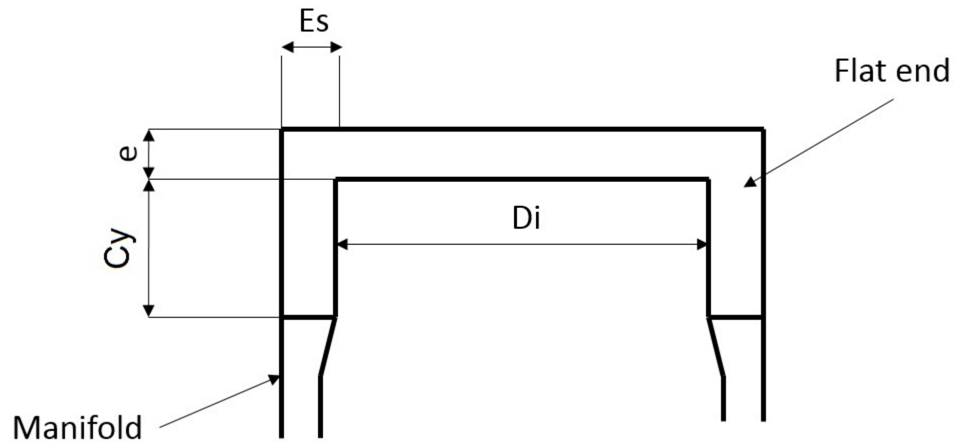


Figure C.1: Sketch of the dividing manifold flat end.

the value e with the following formula:

$$e = max\left\{\left(C_1 D_i\sqrt{\frac{P}{f}}\right),\left(C_2 D_i\sqrt{\frac{P}{f}}\right)\right\} \tag{C.1}$$

where:

- C_1, C_2 are the shape factors for calculation of circular flat end. In our case (by Figure 10.4-4 and 10.4.5 pp. 135-136) $C_1 = 0.410$ and $C_2 = 0.6$;
- D_i is the inside diameter of the cylindrical shell welded to a flat end;
- f is the nominal design stress at ambient temperature (we have assume 120 MPa for stainless steel).

Equation C.1 give a minimum value of e:

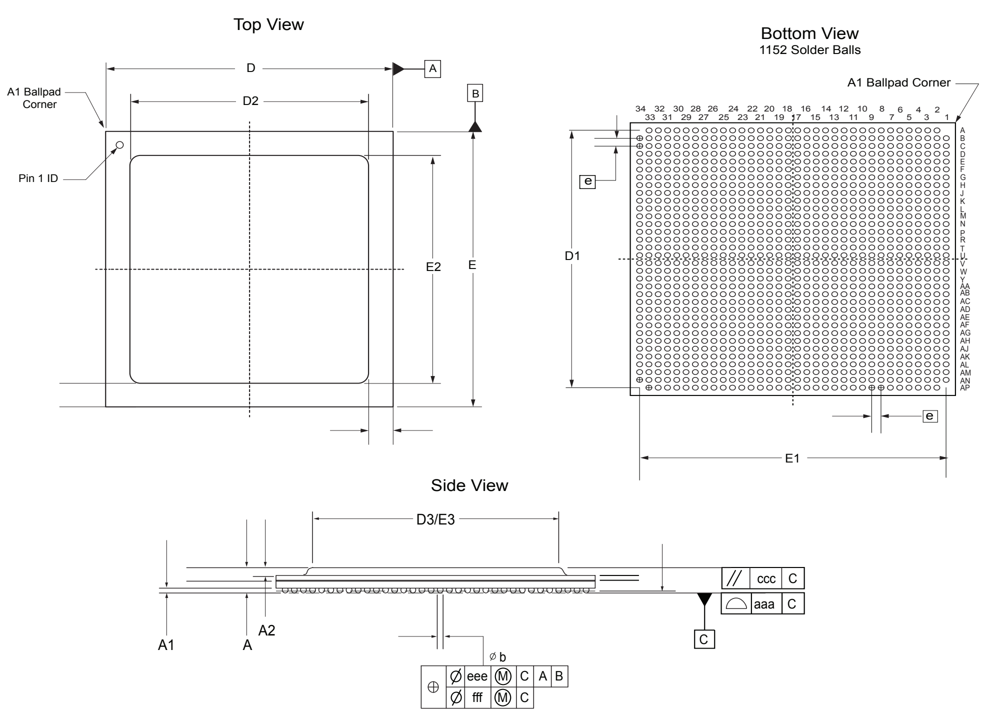
$$e_{min} = 1.5\ mm$$

Appendix D

Data-sheets

D.1 FPGA

FC1152



Note: Dimensions are in millimeters. Refer to the "FC1152 Package Mechanical Drawing Dimensions" section on page 70 for the dimensions.

Supported Devices	
SmartFusion2 (M2S150)	IGLOO2 (M2GL150)

FC1152 Package Mechanical Drawing Dimensions

JEDEC Equivalent	FC1152 (page 69)		
Dimension	**Min.**	**Nom.**	**Max.**
A	2.34	2.62	2.90
A1	0.40	0.50	0.60
A2	0.8		
aaa	0.20		
b	0.50	0.64	0.70
ccc	0.25		
D	34.85	35.00	35.15
D1	33.00 BSC		
D2	29.00 REF		
D3	27.00 REF		
E	34.85	35.00	35.15
E1	33.00 BSC		
E2	29.00 REF		
E3	27.00 REF		
e	1.00 BSC		
eee	0.25		
fff	0.10		

Notes:
1. *All dimensions are in millimeters.*
2. *BSC = Basic spacing between centers.*

2 – SmartFusion2 DC and Switching Characteristics

General Specifications

Operating Conditions

Table 2-1 • **Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
T_J	Junction temperature	Commercial	0	25	85	°C	
	Junction temperature	Industrial	–40	25	100	°C	
VDD	DC core supply voltage		1.14	1.2	1.26	V	
VPP	Power supply for charge pumps (for normal opeartion and programming)	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
PLLx_VDDA	Analog power supply for PLL0 to PLL5	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
PLL_PCIE_x_VDDA	Auxiliary power supply voltage by core to macro	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
PLL_MDDR_VDDA	Analog power supply for PLL MDDR	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
PLL_FDDR_VDDA	Analog power supply for PLL FDDR	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
PCIExVDD	PCIe/PCS power supply		1.14	1.2	1.26	V	
PCIExVDDIO[L/R]	Tx/Rx analog I/O voltage supply		1.14	1.2	1.26	V	
PCIExVDDPLL[L/R]	Anlog power supply for SERDES PLL of PCIe		2.375	2.5	2.625	V	
VDDIx	1.2 V DC supply voltage		1.14	1.2	1.26	V	
	1.5 V DC supply voltage		1.425	1.5	1.575	V	
	1.8 V DC supply voltage		1.71	1.8	1.89	V	
	2.5 V DC supply voltage		2.375	2.5	2.625	V	
	3.3 V DC supply voltage		3.15	3.3	3.45	V	
	LVDS differential I/O		2.375	2.5	3.45	V	
	B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O		2.375	2.5	2.625	V	
	LVPECL differential I/O		3.15	3.3	3.45	V	
VREFx	Reference voltage supply for FDDR (bank 0) and MDDR (bank 5)		0.49 * VDDI0	0.5 * VDDI0	0.51 * VDDI0	V	
VCCENVM	Embedded nonvolatile memory supply	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	

Table 2-2 • **FPGA and Embedded Flash Programming, Storage and Operating Limits**

Product Grade	Storage Temperature	Programming Temperature	Element	Grade Programming Cycles	Retention
Commercial	Min. T_J = 0°C Max. T_J = 85°C	Min. T_J = 0°C Max. T_J = 85°C	FPGA	500	20 years
		Min. T_J = 0°C Max. T_J = 85°C	Embedded Flash	< 1,000	20 years
				< 10,000	10 years
Industrial	Min. T_J = –40°C Max. T_J = 100°C	Min. T_J = 0°C Max. T_J = 85°C	FPGA	500	20 years
		Min. T_J = –40°C Max. T_J = 100°C	Embedded Flash	< 1,000	20 years
				< 10,000	10 years

Power Supply Sequencing and Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every SmartFusion2 SoC FPGA. These circuits ensure easy transition from powered-off state to powered-up state of the device. The SmartFusion2 system controller is responsible for systematic power-on reset whenever the device is powered on or reset. All the I/Os are held in a high-impedance state by the system controller until all power supplies are at their required levels and the system controller has completed the reset sequence. The power-on reset circuitry in SmartFusion2 devices requires the VDD supply to ramp at a predefined rate. Four ramp rate options are available during design generation: 50 µs, 100 µs, 1 ms, and 100 ms.

Thermal Characteristics

Introduction

The temperature variable in the SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - \theta_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance

θ_{JB} = Junction-to-board thermal resistance

θ_{JC} = Junction-to-case thermal resistance

T_J = Junction temperature

T_A = Ambient temperature

T_B = Board temperature (measured 1.0 mm away from the package edge)

T_C = Case temperature

P = Total power dissipated by the device

Table 2-3 • **Package Thermal Resistance**

Product	θ_{JA}			θ_{JC}	θ_{JB}	**Units**
	Still Air	**1.0 m/s**	**2.5 m/s**			
M2S050T-FG896	14.7	12.5	10.9	7.2	4.9	°C/W

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

The maximum power dissipation allowed is calculated using EQ 4.

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100°C. EQ 5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2S050T-FG896 package at commercial temperature and in still air, where

θ_{JA} = 14.7°C/W (taken from Table 2-3 on page 2-3).

T_A = 85°C

$$\text{Maximum Power Allowed} = \frac{100°C - 85°C}{14.7°C/W} = 1.088\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

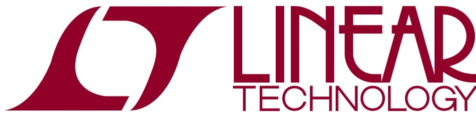
Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

D.2 DC-DC Converter



LTM8033

Ultralow Noise EMC 36V_{IN}, 3A DC/DC µModule Regulator

FEATURES

- **Complete Step-Down Switch Mode Power Supply**
- **Wide Input Voltage Range: 3.6V to 36V**
- **3A Output Current**
- **0.8V to 24V Output Voltage**
- **EN55022 Class B Compliant**
- Current Share Multiple LTM8033 Regulators for More Than 3A Output
- Selectable Switching Frequency: 200kHz to 2.4MHz
- Current Mode Control
- SnPb or RoHS Compliant Finish
- Programmable Soft-Start
- Compact Package (11.25mm × 15mm × 4.32mm) Surface Mount LGA and (11.25mm × 15mm × 4.92mm) BGA Packages

APPLICATIONS

- Automotive Battery Regulation
- Power for Portable Products
- Distributed Supply Regulation
- Industrial Supplies
- Wall Transformer Regulation

DESCRIPTION

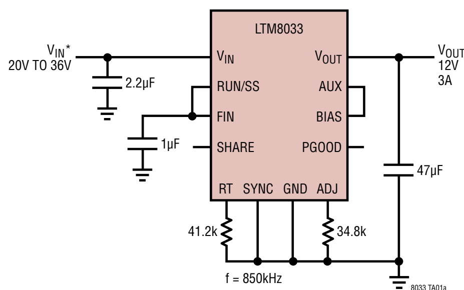
The LTM®8033 is an electromagnetic compatible (EMC) 36V, 3A DC/DC µModule® buck converter designed to meet the radiated emissions requirements of EN55022. Conducted emission requirements can be met by adding standard filter components. Included in the package are the switching controller, power switches, inductor, filters and all support components. Operating over an input voltage range of 3.6V to 36V, the LTM8033 supports an output voltage range of 0.8V to 24V, and a switching frequency range of 200kHz to 2.4MHz, each set by a single resistor. Only the bulk input and output filter capacitors are needed to finish the design.

The LTM8033 is packaged in a compact (11.25mm × 15mm × 4.32mm) overmolded land grid array (LGA) and ball grid array (BGA) package suitable for automated assembly by standard surface mount equipment. The LTM8033 is available with SnPb (BGA) or RoHS compliant terminal finish.

LT, LTC, LTM, Linear Technology, the Linear logo, µModule and Burst Mode are registered trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

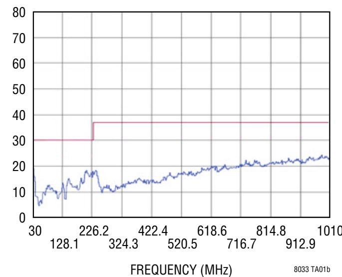
TYPICAL APPLICATION

Ultralow Noise 12V/3A DC/DC µModule Regulator



* RUNNING VOLTAGE RANGE. PLEASE REFER TO THE APPLICATIONS INFORMATION SECTION FOR START-UP DETAILS.

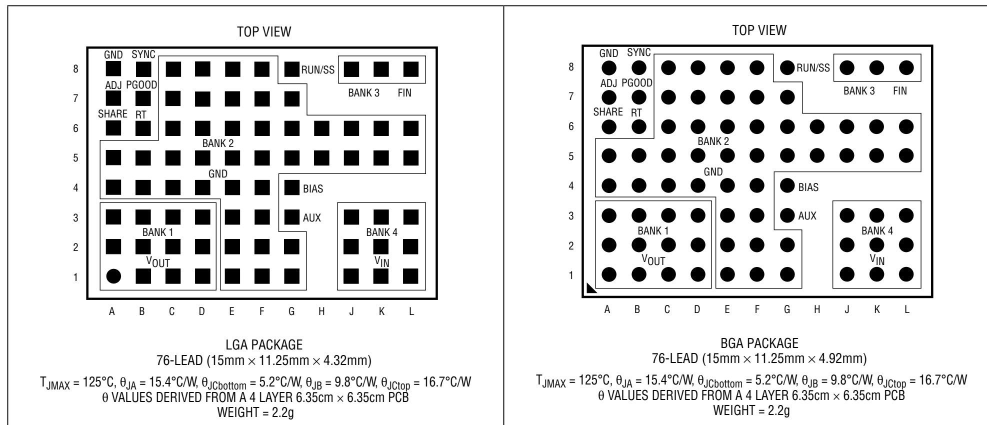
EMI Performance



ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN}, FIN, RUN/SS Voltage 36V
ADJ, RT, SHARE Voltage 6V
V_{OUT}, AUX 25V
PGOOD, SYNC 30V
BIAS 25V
Maximum Junction Temperature (Note 2) .... 125°C
Solder Temperature .... 245°C

PIN CONFIGURATION



LGA PACKAGE
76-LEAD (15mm × 11.25mm × 4.32mm)
T_{JMAX} = 125°C, θ_{JA} = 15.4°C/W, $\theta_{JCbottom}$ = 5.2°C/W, θ_{JB} = 9.8°C/W, θ_{JCtop} = 16.7°C/W
θ VALUES DERIVED FROM A 4 LAYER 6.35cm × 6.35cm PCB
WEIGHT = 2.2g

BGA PACKAGE
76-LEAD (15mm × 11.25mm × 4.92mm)
T_{JMAX} = 125°C, θ_{JA} = 15.4°C/W, $\theta_{JCbottom}$ = 5.2°C/W, θ_{JB} = 9.8°C/W, θ_{JCtop} = 16.7°C/W
θ VALUES DERIVED FROM A 4 LAYER 6.35cm × 6.35cm PCB
WEIGHT = 2.2g

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 2)
		DEVICE	FINISH CODE			
LTM8033EV#PBF	Au (RoHS)	LTM8033V	e4	LGA	3	–40°C to 125°C
LTM8033IV#PBF	Au (RoHS)	LTM8033V	e4	LGA	3	–40°C to 125°C
LTM8033MPV#PBF	Au (RoHS)	LTM8033V	e4	LGA	3	–55°C to 125°C
LTM8033EY#PBF	SAC305 (RoHS)	LTM8033Y	e1	BGA	3	–40°C to 125°C
LTM8033IY#PBF	SAC305 (RoHS)	LTM8033Y	e1	BGA	3	–40°C to 125°C
LTM8033IY	SnPb (63/67)	LTM8033Y	e0	BGA	3	–40°C to 125°C
LTM8033MPY#PBF	SAC305 (RoHS)	LTM8033Y	e1	BGA	3	–55°C to 125°C
LTM8033MPY	SnPb (63/67)	LTM8033Y	e0	BGA	3	–55°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Terminal Finish Part Marking: www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings: www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, RUN/SS = 12V unless otherwise noted (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		●			3.6	V
Output DC Voltage	0A < I_{OUT} < 3A, R_{ADJ} Open, V_{IN} = 24V 0A < I_{OUT} < 3A, R_{ADJ} = 16.5k, V_{IN} = 32V			0.8 24		V V
Output DC Current	V_{IN} = 24V		0		3	A
Quiescent Current into V_{IN}	RUN/SS = 0.2V Not Switching BIAS = 0V, Not Switching			0.01 30 100	1 60 150	µA µA µA
Quiescent Current into BIAS	RUN/SS = 0.2V Not Switching BIAS = 0V, Not Switching			0.01 75 0	0.5 120 5	µA µA µA
Line Regulation	5.5V < V_{IN} < 36V			0.3		%
Load Regulation	0A < I_{OUT} < 3A, V_{IN} = 24V			0.4		%
Output RMS Voltage Ripple	V_{IN} = 24V, 0A < I_{OUT} < 3A			5		mV
Switching Frequency	R_T = 45.3k			780		kHz
Voltage at ADJ Pin		●	775	790	805	mV
Current Out of ADJ Pin	ADJ = 1V, V_{OUT} = 0V			2		µA
Minimum BIAS Voltage for Proper Operation				2	2.8	V
RUN/SS Pin Current	RUN/SS = 2.5V			5	10	µA
RUN/SS Input High Voltage			2.5			V
RUN/SS Input Low Voltage					0.2	V
PGOOD Threshold (at ADJ)	V_{OUT} Rising			730		mV
PGOOD Leakage Current	PGOOD = 30V, RUN/SS = 0V			0.1	1	µA
PGOOD Sink Current	PGOOD = 0.4V		200	735		µA
SYNC Input Low Threshold	f_{SYNC} = 550kHz		0.5			V
SYNC Input High Threshold	f_{SYNC} = 550kHz				0.7	V
SYNC Bias Current	SYNC = 0V			0.1		µA
500kHz Narrowband Conducted Emissions	$24V_{IN}$, $3.3V_{OUT}$, I_{OUT} = 3A, 5µH LISN			89		dBµV
1MHz Narrowband Conducted Emissions				69		dBµV
3MHz Narrowband Conducted Emissions				51		dBµV

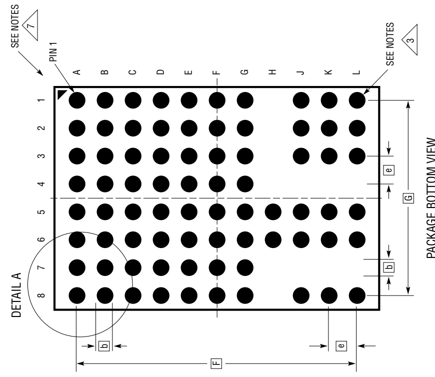
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

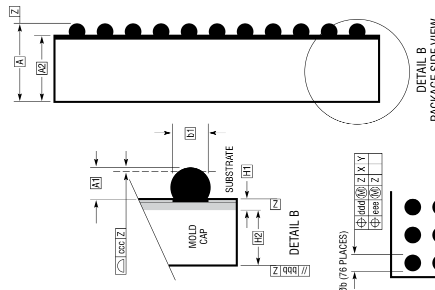
Note 2: The LTM8033E is guaranteed to meet performance specifications from 0°C to 125°C internal. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM8033I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM8033MP is guaranteed to meet specifications over the full –55°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

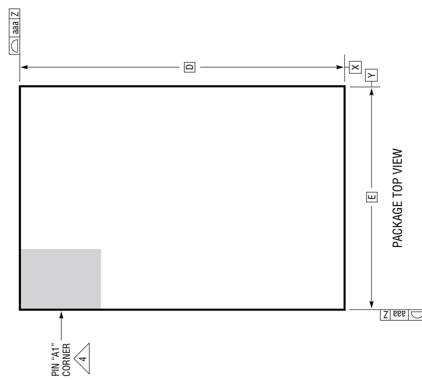
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

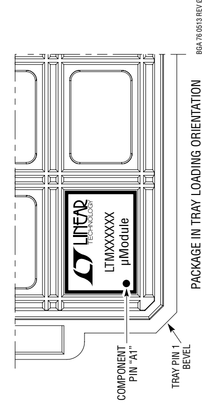
BGA Package
76-Lead (15mm × 11.25mm × 4.92mm)
(Reference LTC DWG # 05-08-1952 Rev Ø)





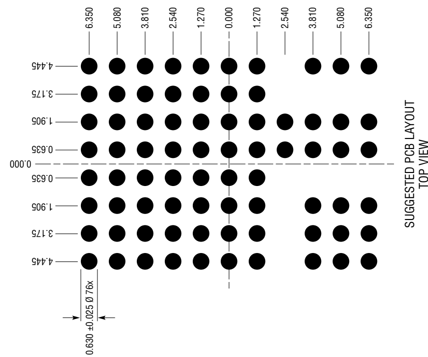


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. SOLDER BALL COMPOSITION IS 96.5% Sn/3.0% Ag/0.5% Cu
7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



SYMBOL	MIN	NOM	MAX	NOTES
	DIMENSIONS			
A	4.72	4.92	5.12	
A1	0.50	0.60	0.70	
A2	4.22	4.32	4.42	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		15.00		
E		11.25		
e		1.27		
F		12.70		
G		8.89		
H1	0.27	0.32	0.37	
H2	3.95	4.00	4.05	
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	

TOTAL NUMBER OF BALLS: 76



REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/14	Add BGA package option	1, 2, 22, 24
B	09/14	BGA ball A1 was missing, corrected	2
		Changed quiescent current V_{IN} and BIAS from 20µA and 50µA to 30µA and 75µA, respectively	13

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

D.3 ADC

12-Bit, 170 MSPS/210 MSPS/250 MSPS, 1.8 V Analog-to-Digital Converter

AD9230

FEATURES

SNR = 64.9 dBFS @ f_{IN} up to 70 MHz @ 250 MSPS
ENOB of 10.4 @ f_{IN} up to 70 MHz @ 250 MSPS (−1.0 dBFS)
SFDR = −79 dBc @ f_{IN} up to 70 MHz @ 250 MSPS (−1.0 dBFS)
Excellent linearity
- **DNL = ±0.3 LSB typical**
- **INL = ±0.5 LSB typical**

LVDS at 250 MSPS (ANSI-644 levels)
700 MHz full power analog bandwidth
On-chip reference, no external decoupling required
Integrated input buffer and track-and-hold
Low power dissipation
- **434 mW @ 250 MSPS—LVDS SDR mode**
- **400 mW @ 250 MSPS—LVDS DDR mode**

Programmable input voltage range
- **1.0 V to 1.5 V, 1.25 V nominal**

1.8 V analog and digital supply operation
Selectable output data format (offset binary, twos complement, Gray code)
Clock duty cycle stabilizer
Integrated data capture clock

APPLICATIONS

Wireless and wired broadband communications
Cable reverse path
Communications test equipment
Radar and satellite subsystems
Power amplifier linearization

FUNCTIONAL BLOCK DIAGRAM

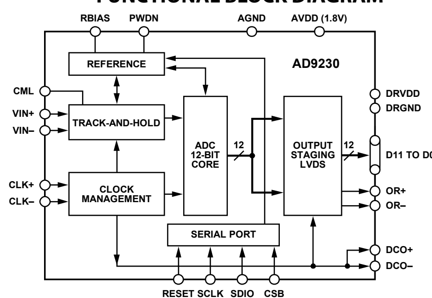


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The AD9230 is a 12-bit monolithic sampling analog-to-digital converter optimized for high performance, low power, and ease of use. The product operates at up to a 250 MSPS conversion rate and is optimized for outstanding dynamic performance in wideband carrier and broadband systems. All necessary functions, including a track-and-hold (T/H) and voltage reference, are included on the chip to provide a complete signal conversion solution.

The ADC requires a 1.8 V analog voltage supply and a differential clock for full performance operation. The digital outputs are LVDS (ANSI-644) compatible and support either twos complement, offset binary format, or Gray code. A data clock output is available for proper output data timing.

Fabricated on an advanced CMOS process, the AD9230 is available in a 56-lead LFCSP, specified over the industrial temperature range (−40°C to +85°C).

PRODUCT HIGHLIGHTS

1. High Performance—Maintains 64.9 dBFS SNR @ 250 MSPS with a 70 MHz input.
2. Low Power—Consumes only 434 mW @ 250 MSPS.
3. Ease of Use—LVDS output data and output clock signal allow interface to current FPGA technology. The on-chip reference and sample and hold provide flexibility in system design. Use of a single 1.8 V supply simplifies system power supply design.
4. Serial Port Control—Standard serial port interface supports various product functions, such as data formatting, disabling the clock duty cycle stabilizer, power-down, gain adjust, and output test pattern generation.
5. Pin-Compatible Family—10-bit pin-compatible family offered as AD9211.

Rev. 0
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ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
ELECTRICAL	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to DRGND	−0.3 V to +2.0 V
AGND to DRGND	−0.3 V to +0.3 V
AVDD to DRVDD	−2.0 V to +2.0 V
D0+/D0− through D13+/D13− to DRGND	−0.3 V to DRVDD + 0.3 V
DCO to DRGND	−0.3 V to DRVDD + 0.3 V
OR to DGND	−0.3 V to DRVDD + 0.3 V
CLK+ to AGND	−0.3 V to +3.9 V
CLK− to AGND	−0.3 V to +3.9 V
VIN+ to AGND	−0.3 V to AVDD + 0.2 V
VIN− to AGND	−0.3 V to AVDD + 0.2 V
SDIO/DCS to DGND	−0.3 V to DRVDD + 0.3 V
PDWN to AGND	−0.3 V to +3.9 V
CSB to AGND	−0.3 V to +3.9 V
SCLK/DFS to AGND	−0.3 V to +3.9 V
ENVIRONMENTAL	
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

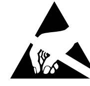
The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 6.

Package Type	θ_{JA}	θ_{JC}	Unit
56-Lead LFCSP (CP-48-3)	30.4	2.9	°C/W

Typical θ_{JA} and θ_{JC} are specified for a 4-layer board in still air. Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, and through holes, ground, and power planes reduces the θ_{JA}.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

OUTLINE DIMENSIONS

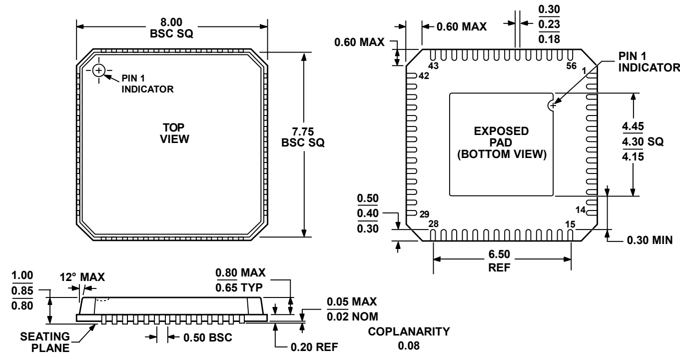


Figure 65. 56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
8 mm × 8 mm Body, Very Thin Quad
(CP-56-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9230BCPZ-170[1]	−40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-56-2
AD9230BCPZ-210[1]	−40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-56-2
AD9230BCPZ-250[1]	−40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-56-2
AD9230-170EBZ[1]		LVDS Evaluation Board with AD9230BCPZ-170	
AD9230-210EBZ[1]		LVDS Evaluation Board with AD9230BCPZ-210	
AD9230-250EBZ[1]		LVDS Evaluation Board with AD9230BCPZ-250	

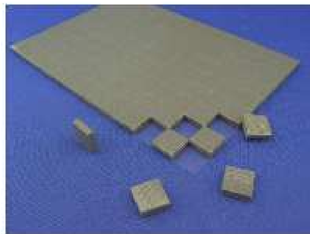
[1] Z = Pb-free part.

D.4 Thermal Pad

NEW! Silicone-Free

Thermal Pad – CPSS Series

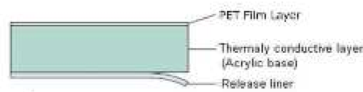
RoHS Compliant



Ultra-soft (ASKER C 8) silicone-free thermal pad

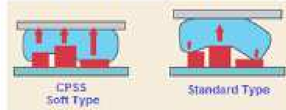
- Super soft and compliable material allows for less pressure on the heat source, such as the IC or PCB, when compared to a standard TIM
- Pliability of the material allows for lower thermal resistance on an uneven surface
- Silicone-free material – no siloxane outgassing
- Suitable for vibration control

Structure

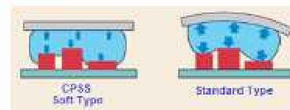


Features of Soft Type Thermal pad

- Soft type thermal pads provide low thermal resistance, while conforming well to uneven surfaces.



- Soft type thermal pads more evenly distribute pressure.



Typical properties

(Not guaranteed values)

Item	CPSS	Test Method
Thickness (mm)	1 ±0.1, 2 ±0.2, 3 ±0.3, 4±0.4	-
Standard Sheet Size (mm)	210 x 510 ±2.5	-
Color	Dark Green	
Thermal Conductivity (W/m·K)	2	Hot Wire Method
Hardness (ASKER C)	8	Asker C
Volume Resistivity (Ω·cm)	10^{12}	MCC Method
Dielectric Breakdown Voltage	1.0mm=1kv, 3.0mm=3kv	
Operating Temperature	-20°C~+100°C	ASTM D 2240
Flame Resistance	UL94 V2	UL94
Outgassing	TBA	ASTM E 595

D.5 Cardlock

Card-Lok

Product Series	3 or 5 pc.	Actuation	Profile Width (nominal) x Relaxed Height (max)	Profile Height Expanded (min)	Length (min)	Approximate Clamping Force[2] N(lbs)	Recommended Torque Setting N-cm (in-lbs)	DSCC	DSCC CID
223	5	Screw	5.72 (.225) x 6.86 (.270)	8.26 (.325)	121.9 (4.80)	tbd	limited		
224	5	Screw	5.33 (.210) x 7.24 (.285)	8.64 (.340)	121.9 (4.80)	tbd	limited		
225	3	Screw	5.72 (.225) x 6.86 (.270)	8.26 (.325)	54.61 (2.15)	489 (110)	68 (6)	84103	59590
E225	3	Screw	5.72 (.225) x 6.86 (.270)	8.26 (.325)	71.12 (2.80)	489 (110)	68 (6)		
L225	3	Lever	5.72 (.225) x 6.86 (.270)	8.26 (.325)	54.61 (2.15)	533 (120)	N/A		
226	5	Screw	5.72 (.225) x 6.86 (.270)	8.26 (.325)	121.92 (4.80)	800 (180)	68 (6)	89064	59789
230	3	Screw	5.59 (.220) x 5.72 (.225)	6.99 (.275)	54.61 (2.15)	489 (110)	68 (6)	84103	59590
231	5	Screw	5.59 (.220) x 5.72 (.225)	6.99 (.275)	121.92 (4.80)	800 (180)	68 (6)	89064	59789
235	3	Screw	5.84 (.230) x 7.32 (.288)	8.64 (.340)	71.12 (2.80)	445 (100)	68 (6)		
236	5	Screw	5.84 (.230) x 7.32 (.288)	8.64 (.340)	147.32 (5.80)	800 (180)	68 (6)		
240	3	Screw	6.10 (.240) x 4.57 (.180)	5.59 (.220)	54.61 (2.15)	489 (110)	68 (6)	84103	59590
245	3	Screw	6.60 (.245) x 6.86 (.270)	8.26 (.325)	54.61 (2.15)	622 (140)	113 (10)		59590
250	3	Screw	9.53 (.375) x 9.78 (.385)	11.94 (.470)	63.50 (2.50)	1111 (250)	227 (20)		59590
255	3	Screw	12.70 (.500) x 11.68 (.460)	15.24 (.600)	54.61 (2.15)	1778 (400)	351 (31)		59590
260	5	Screw	6.35 (.250) x 6.26 (.270)	8.26 (.325)	54.61 (2.15)	1778 (400)	68 (6)	89024	
261	3	Screw	6.35 (.250) x 6.26 (.270)	8.26 (.325)	54.61 (2.15)	667 (150)	68 (6)		59789
L260	5	Lever	6.35 (.250) x 6.26 (.270)	8.26 (.325)	54.61 (2.15)	556 (125)	N/A		59789
LE260	5	Lever	6.35 (.250) x 6.26 (.270)	8.26 (.325)	54.61 (2.15)	556 (125)	N/A		59789
263	5	Screw	6.35 (.250) x 7.44 (.293)	8.89 (.350)	54.61 (2.15)	1778 (400)	68 (6)		
264	3	Screw	6.35 (.250) x 7.44 (.293)	8.89 (.350)	54.61 (2.15)	667 (150)	68 (6)		59789
265	5	Screw	5.72 (.225) x 5.84 (.230)	7.37 (.290)	54.61 (2.15)	1556 (350)	68 (6)		
266	3	Screw	5.72 (.225) x 5.84 (.230)	7.37 (.290)	54.61 (2.15)	600 (135)	68 (6)		
267	5	Screw	6.35 (.250) x 5.00 (.197)	5.99 (.236)	54.61 (2.15)	1556 (350)	68 (6)		
280	5	Screw	9.27 (.365) x 9.65 (.380)	11.68 (.460)	60.96 (2.40)	3334 (750)	227 (20)		59789
281	3	Screw	9.27 (.365) x 9.65 (.380)	11.68 (.460)	60.96 (2.40)	1245 (280)	227 (20)		

Channel-Lok

Product Series	3 or 5 pc.	Actuation	Width x Height (max)	Board Thickness	Length[1] (min)	Approximate Clamping Force N (lbs)	Recommended Torque Setting N-cm (in-lbs)
227	3	Screw	12.57 (.495) to 8.89 (.350)	1.14 (.045) to 2.62 (.103)	76.20 (3.00)	489 (110)	68 (6)
228	5	Screw	12.57 (.495) to 8.89 (.350)	1.14 (.045) to 2.62 (.103)	101.6 (4.00)	801 (180)	68 (6)

Retainers & Card Guides

Product Series	Material	Conductive	Application	Board Thickness	Length[1] (min)	UL rating
125/126	CR	Yes	Sheet Metal	1.6 (.063) & 2.4 (.094)	31.75 (1.25) to 311.15 (12.25)	N/A
165/166	BeCu	Yes	Sheet Metal	1.6 (.063) & 2.4 (.094)	31.75 (1.25) to 311.15 (12.25)	N/A
NW125/NW126	CR	Yes	Cold Wall	N/A	31.75 (1.25) to 311.15 (12.25)	N/A
NW165/NW166	BeCu	Yes	Cold Wall	N/A	31.75 (1.25) to 311.15 (12.25)	N/A
120	Nylon	No	Sheet Metal	1.6 (.063) & 2.4 (.094)	101.60(4.00),152.40(6.00),177.8(7.00),215.90(8.50),241.30(9.50)	V-2 (V-0 available)
C120	Polycarbonate	Yes	Sheet Metal	1.6 (.063) & 2.4 (.094)	101.60(4.00),152.40(6.00),177.8(7.00),215.90(8.50),241.30(9.50)	V-2 (V-0 available)

Plastic Extractors & Inserter-Extractors

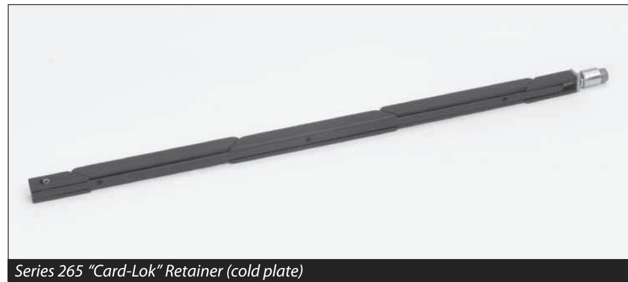
Product Series	Material	Function[4]	Mechanical Advantage	Board Thickness	UL Rating
107	Glass-filled Nylon	I & E	4.5:1	1.6 (.063) & 2.4 (.094)	V-0
107-10	Glass-filled Nylon	I & E	3.3:1	1.6 (.063) & 2.4 (.094)	V-0
107-20	Glass-filled Nylon	I, E & L	4.5:1	1.6 (.063) & 2.4 (.094)	V-2 (V-0 available)
107-30	Glass-filled Nylon	I & E	5.5:1	1.6 (.063)	V-0
107-40-3	Glass-filled Nylon	I & E	4.5:1	1.6 (.063) & 2.4 to 3.2 (.094 to .125)	V-0
107-70	Glass-filled Nylon Latch - Nylon	I, E & L	4.5:1	1.6 (.063), 2.4 (0.94) & 3.2 (.125)	V-0 (Inserter-Extractor) V-2 (Latch)

Metal Extractors & Inserter-Extractors

Product Series	Material	Function[4]	Mechanical Advantage	Board Thickness
107-35	Al	I & E	5.5:1	1.6 (.063), 2.4 (.094) & 3.2 (.125)
107-50	Al	I & E	4.5:1	1.6 (.063), 2.4 (.094) & 3.2 (.125)
107-51	Al	I & E	3.3:1	1.6 (.063), 2.4 (.094) & 3.2 (.125)
107-55	Al	I & E	8.0:1	1.6 (.063), 2.4 (.094) & 3.2 (.125)
107-73	Al	I, E & L	4.2:1	1.6 (.063), 2.4 (.094) & 3.2 (.125)
107-75	Al	I, E & L	7.0:1	1.6 (.063), 2.4 (.094) & 3.2 (.125)
109	Al or CR	E	4.5:1	1.6 (.063), 2.4 (.094) & 3.2 (.125)

1-Other assembly lengths available upon request 2-Clamping forces based on Chemical Film Option – Other finishes and options will yield different results
3-101 available in 1.6 (.063) only 4-Function: E=Extract I=Insert L=Latch or Lock 5-Units are metic (inch)

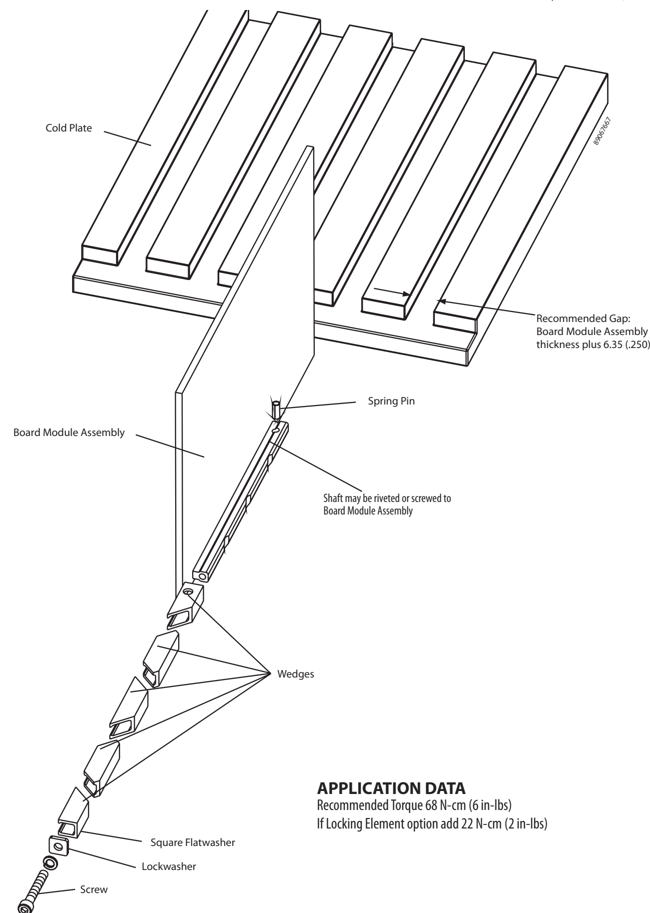
Calmark offers the narrow, advance design Series 265 “Card-Lok” retainer for cold plate/heat exchanger applications. This totally unique design incorporates design advancements that provide increased thermal transfer, easy insertion, lighter weight and now closer center to center board spacing.



Series 265 “Card-Lok” Retainer (cold plate)

FEATURES

- Narrow design permits closer board spacing
- Maximum uniform clamping force
- Increased thermal transfer
- Maintains wedge and body alignment for easy installation
- Captivated rear wedge
- Choice of screw head style
- Lighter weight
- Lower cost - faster delivery
- Design Flexibility - Special lengths, finishes, or other design options available on request



WEDGES, BODIES & SHAFT

Material:

Wedges: Aluminum alloy 6061-T6 per ASTM-B221 or AMS-QQ-A-200/8

Shaft: Aluminum alloy 7075-T6 per ASTM-B221 or AMS-QQ-A-200/11

Finish:

See Finish Table

SCREW, LOCK & FLAT WASHER

Material:

NAS1352C, Modified NAS1352C04 or 18-8 stainless steel, Stainless steel per ASTM-A582

Finish:

Passivate per Mil-S-5002

ROLL PIN

Material:

400 Series Stainless Steel

Finish:

Passivate per Mil-S-5002

WEIGHT

.89 g/cm (.080 oz/in)

APPLICATION DATA

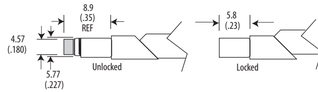
Recommended Torque 68 N-cm (6 in-lbs)

If Locking Element option add 22 N-cm (2 in-lbs)

OPTION PREFIX

Detail "V"

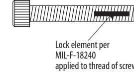
Provides visual lock indication.



OPTION SUFFIX

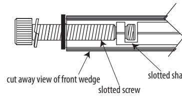
Detail "L"

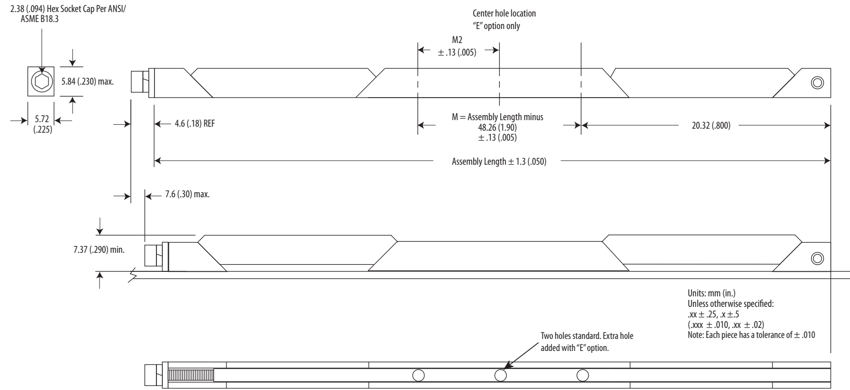
Provides prevailing torque for resistance to loosening from shock and vibration. Adds 22 N-cm (2 in-lbs) torque to assembly. See application data on previous sheet.



Detail "K"

Prevents the unintentional disassembly of screw from front wedge.





Part Number Code
Series 265 Card-Lok Five Piece

M V A 265 - 3.80 E H L K

Prefix options

Option	Code
Metric Screw Head M2.5 Hex Drive	M
Standard Screw Head 3/32 Hex Drive	*[blank]*
Visual Indicator	V
No Visual Indicator	*[blank]*
Black Anodize	A
or choose from Finish Table	*see table*

Suffix options

Option	Code
Assembly length in inches. Standard lengths range from 71.12 (2.80), 96.52 (3.80) and 121.9 (4.80). Other lengths available upon request	*length.xx*
Additional Center Mounting Hole	E
None	*[blank]*
Mounting Options - through mounting holes	H
or choose from Mounting Option Table	*see table*
Lock Element	L
None	*[blank]*
Captive Screw	K
None	*[blank]*

Part Number Code Example:

M265-4.80H

Series 265 Card-Lok five piece 121.9 (4.80) long with M2.5 hex drive, gold chemical film finish and standard rivet hole mounting

FINISH TABLE

Code Letter	Finish
[blank]	Chemical Film per Mil-DTL-5541 Class 1A, Type 1, Gold
"R"	Chemical Film per Mil-DTL-5541 Class 3, Type II, Clear
"A"	Black Anodize per Mil-A-8625 Type II, Class 2
"HA"	Hard Black Anodize per Mil-A-8625 Type III, Class 2
"EN"	Electroless Nickel per Mil-C-26074 Class 4, Grade B, Bright

MOUNTING METHOD TABLE

Code Letter	Method
"H"	Ø1.73/1.85 (.068/.073) dia. through holes countersink 100° x 1.52 (.060) deep
"T0"	0-80 tapped hole
"T2"	2-56 tapped hole
"TM2"	M2 x 0.40 tapped hole
"TM2.5"	M2.5 x 0.45 tapped hole

The clamping outputs indicated in the table below are the results of averaged data. Within each series numerous Card-Loks of various lengths, finishes, and configurations were cycle tested. The accumulated data verified the following:

- Clamping output is not dependent on length
- Clamping output is greatly affected by choice of finish
- Clamping output is greatly improved when washers are used

Customized Card-Lok variations for specific applications are available on request

Product Series	Screw Size	Torque Setting N-cm (in-lbs)	Clamping Force			
			Chem Film Finish N (lbs)	Chem Film Finish With Washers N (lbs)	Black Anodize N (lbs)	Black Anodize With Washers N (lbs)
223	4-40	N/A	Consult factory	Consult factory	Consult factory	Consult factory
224	4-40	N/A	Consult factory	Consult factory	Consult factory	Consult factory
225	4-40	68 (6)	445 (100)	778 (175)	1223 (275)	1423 (320)
E225	4-40	68 (6)	445 (100)	778 (175)	1223 (275)	1423 (320)
L225	4-40	N/A	N/A	N/A	533 (120)	N/A
226	4-40	68 (6)	801 (180)	1402 (315)	2224 (500)	2755 (615)
227	4-40	68 (6)	N/A	778 (175)	N/A	1423 (320)
228	4-40	68 (6)	N/A	1402 (315)	N/A	2775 (615)
230	4-40	68 (6)	489 (110)	890 (200)	3334 (300)	1512 (340)
231	4-40	68 (6)	801 (180)	1402 (315)	2224 (500)	2755 (615)
235	M3	68 (6)	445 (100)	N/A	1223 (275)	N/A
236	M3	68 (6)	801 (150)	N/A	2224 (500)	N/A
240	4-40	68 (6)	489 (110)	623 (140)	1446 (325)	1490 (335)
245	6-32	110 (10)	623 (140)	1023 (230)	1779 (400)	1779 (400)
250	8-32	220 (20)	1112 (250)	1779 (400)	2958 (665)	3114 (700)
255	10-32	350 (31)	1779 (400)	2669 (600)	3336 (750)	3670 (825)
260	4-40	68 (6)	N/A	1779 (400)	N/A	2224 (500)
261	4-40	68 (6)	N/A	667 (150)	N/A	1223 (275)
L260	4-40	N/A	N/A	N/A	556 (125)*	N/A
LE260	4-40	N/A	N/A	N/A	556 (125)*	N/A
263	4-40	68 (6)	N/A	1779 (400)	N/A	2224 (500)
264	4-40	68 (6)	N/A	667 (150)	N/A	1223 (275)
265	4-40	68 (6)	N/A	1557 (350)	N/A	2113 (475)
266	4-40	68 (6)	N/A	600 (135)	N/A	801 (180)
267	4-40	68 (6)	N/A	1557 (350)	N/A	2113 (475)
280	8-32	220 (20)	N/A	3336 (750)	N/A	4003 (900)
281	8-32	220 (20)	N/A	1245 (280)	N/A	2224 (500)

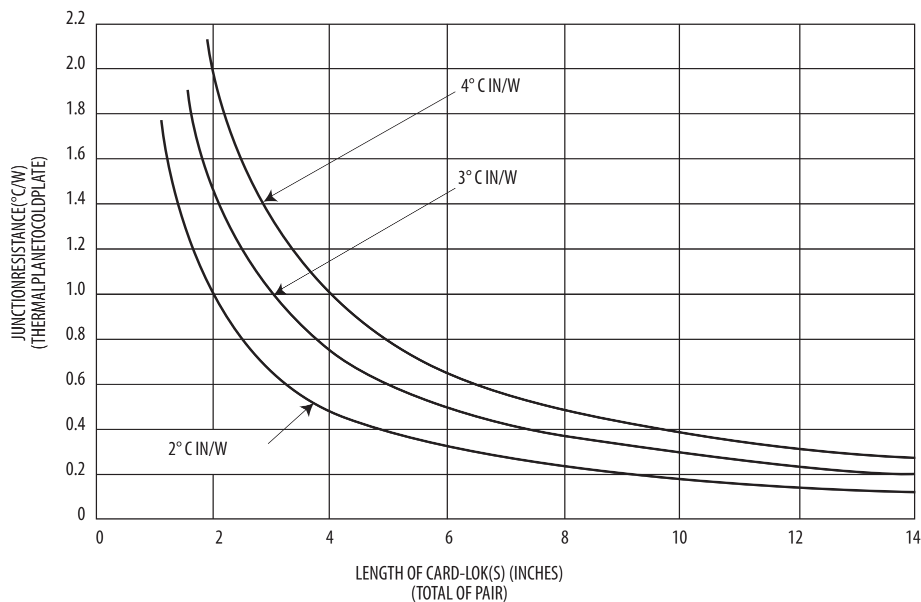
* Finish is dry film lube over black anodize

Testing performed by numerous users of Calmark's Series 225 and similar size Card-Loks (approx. 6.35 [.25] high) has shown that the thermal resistance across the interface of a card which is clamped to a cold plate will usually fall within the range of 2° to 4°C inch/watt. Three piece Card-Loks of shorter lengths will usually provide results close to the 2, while longer Card-Loks (over 6 inches) may fall closer to the 4.

These thermal resistance numbers apply when testing is performed at or near sea level. When the same testing is performed at high altitude or near vacuum conditions the results can be significantly affected. Increases of from 10 to 40 percent would not be unusual, especially with the longer three piece Card-Loks.

Five piece Card-Loks, such as the Series 260 or 265, with their greater and more evenly distributed clamping force, will greatly reduce these potential gradients.

The following chart provides an easy method of estimating the temperature rise across the interface (junction) of the card and cold plate when thermal conductivity is the only means of heat transfer considered (heat loss due to radiation and convection minimized).



Example: A card using a pair of 127mm (5.00 inch) long Card-Loks is clamped to a pair of cold plates and is dissipating 50 watts of power:

Total length of Card-Loks is 254 (10), [127 (5) x 2]
Junction resistance is shown as between 0.2° and 0.4°C/W

Therefore, at their junction, card temperature will rise between 10° and 20°C above the cold plate. [0.2°C/W x 50(W) = 10°C]