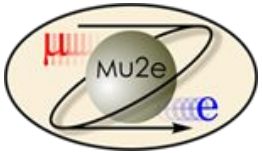


Fermilab

Firmware development for the electronics of the mu2e tracker

Ian Biagioni
Final review

Supervisor:
Vadim Rusu

21 September 2016

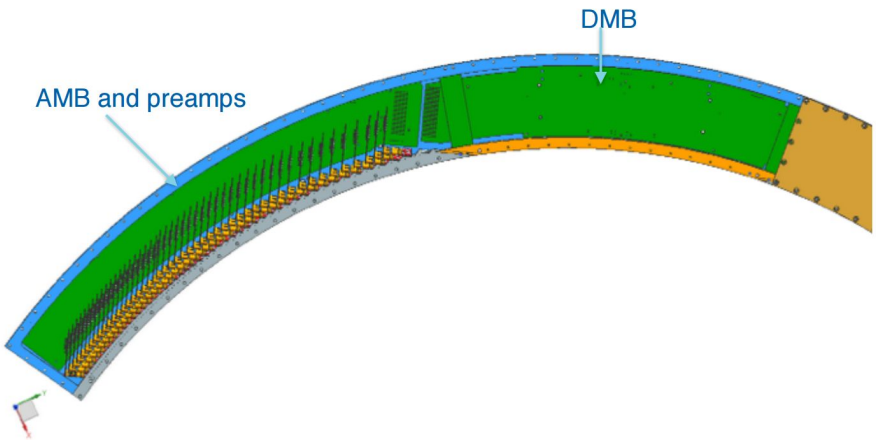
Tracker electronics

AMB:

- connection for preamps
- transmission lines for data, calibration, control, HV, LV

DMB:

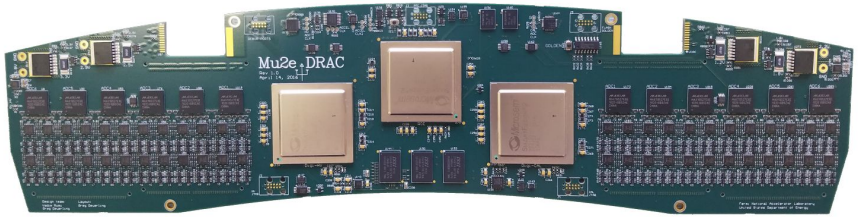
- connection between AMB and DRAC



DRAC

3 FPGAs M2S150T-FC1152:

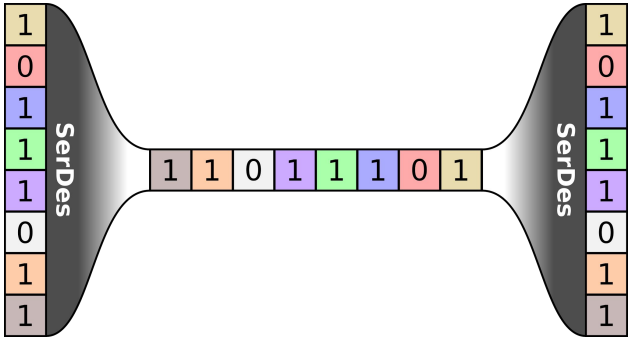
- Two digitizer
  - digitize signals coming from AMB
- ROC (ReadOut Controller)
  - collecting and organizing data from digitizer



SmartFusion 2

SerDes

- Permit to use one pin for channel
- High speed communication
- 8b/10b encoding

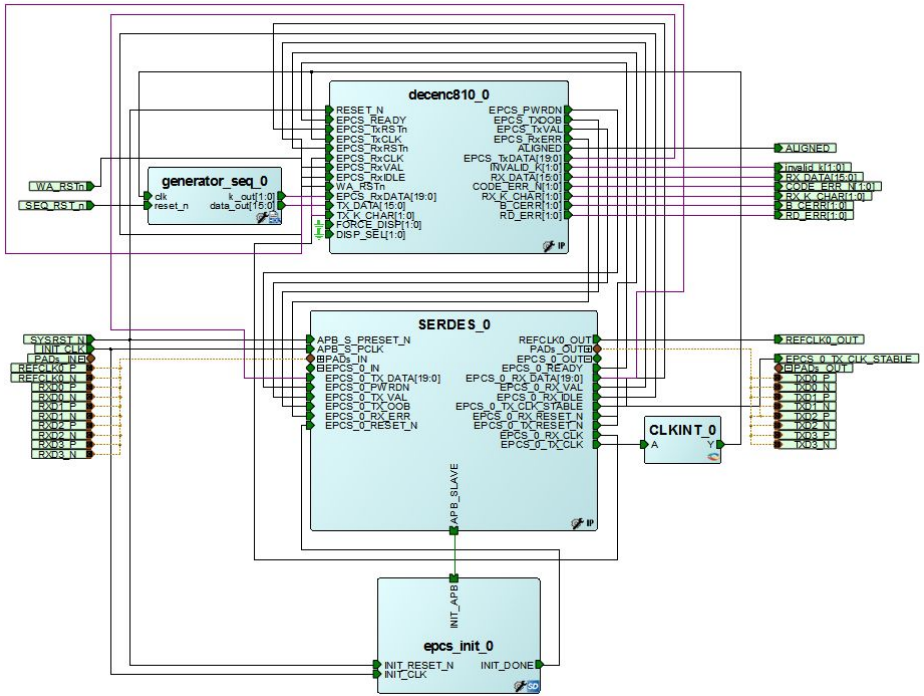


Project flow

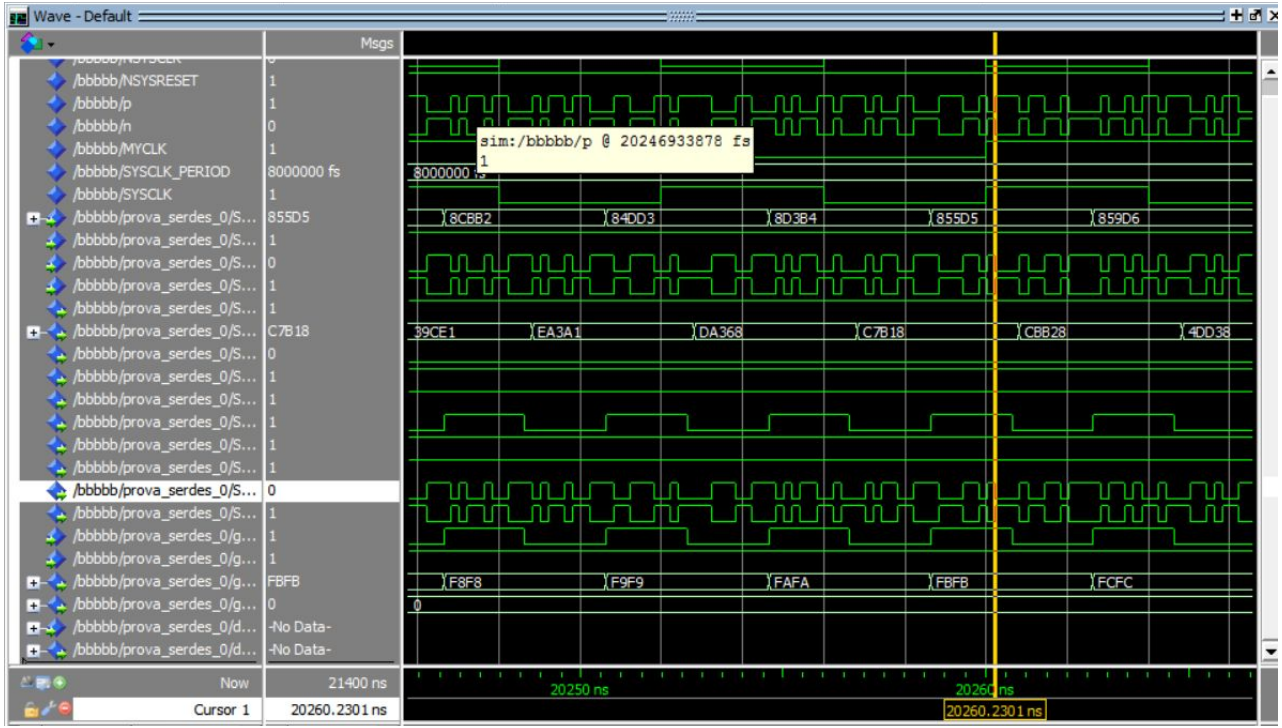
- Get used to Microsemi systems
- Project systems
  - VHDL
  - block programming
- Write software for embedded processor

SerDes implementation

- Custom communication protocol
- 8b/10b encoding
- 5 Gbit/s datarate
- Simulated in loopback configuration



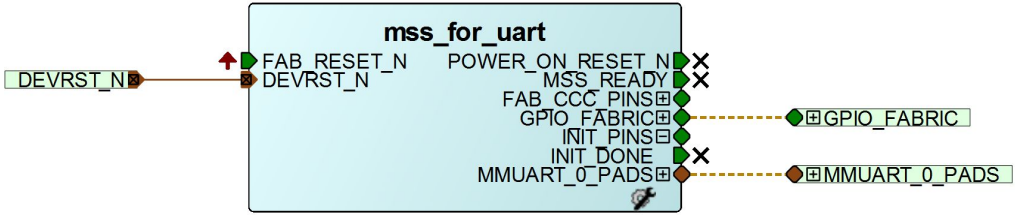
SerDes implementation



UART comunication

- Way to check system behaviour

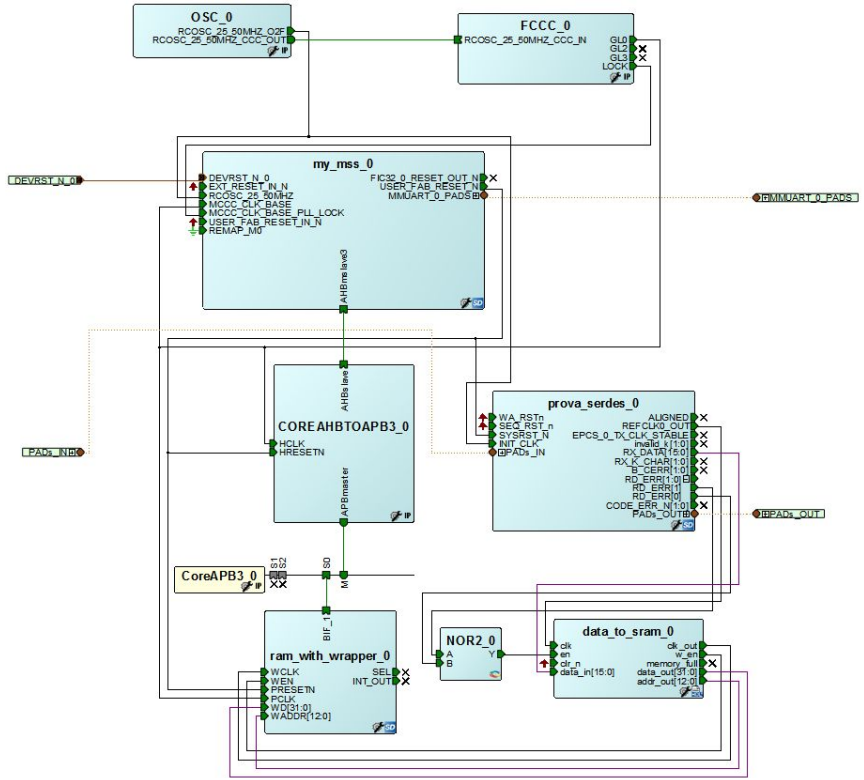
- Software development for serial comunication



SoftConsole

System implementation

- Logic to write data from SerDes to SRAM
- Read data from SRAM using UART



System implementation

Test on SF2-STARTER-KIT-ES-2 (M2S050T)

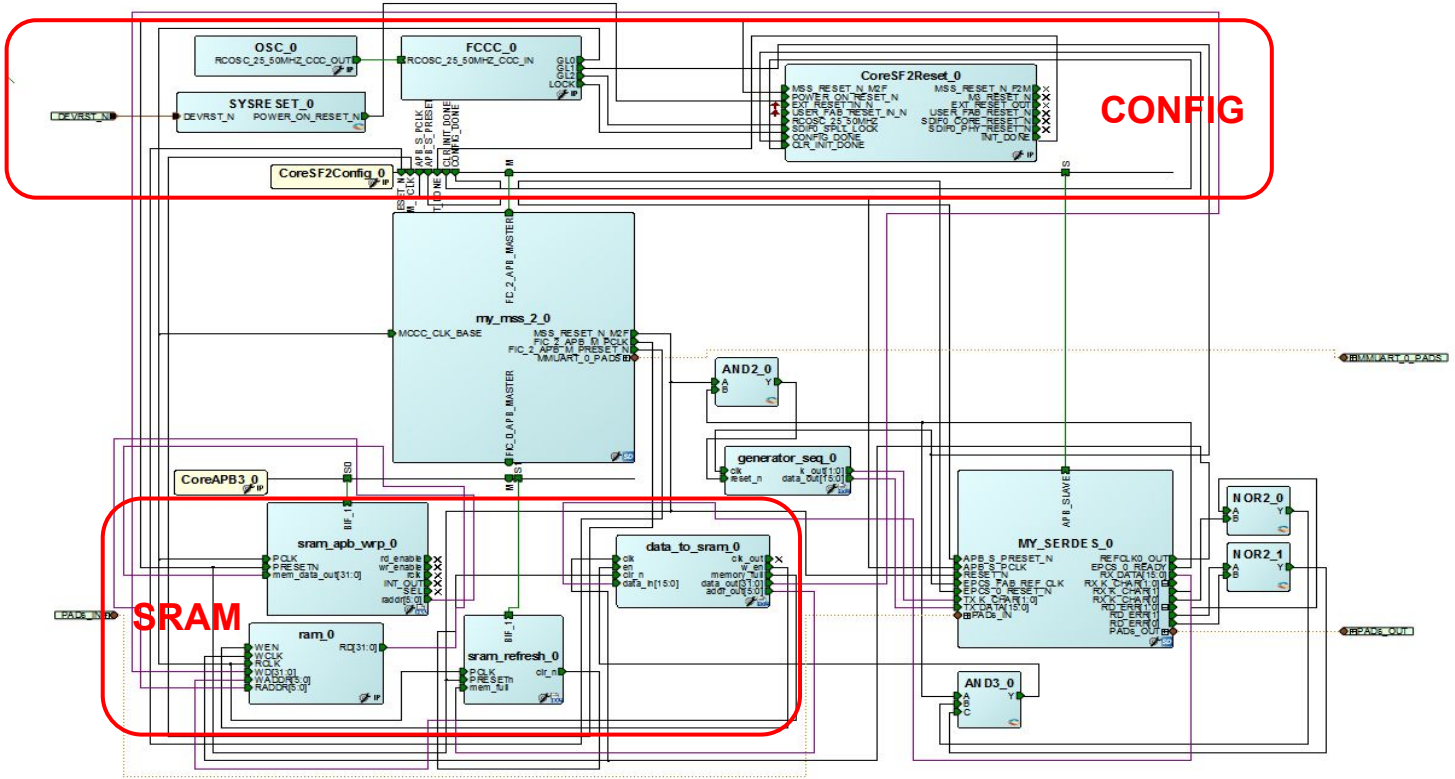
Errors in the design:

- SerDes configuration and initialization
- APB bus
- Timing violations

Missing logic:

- Refresh SRAM memory
- Check data validity

System implementation



System porting

M2S150T bigger footprint than M2S050T → New project costraints and new design for clocks structure

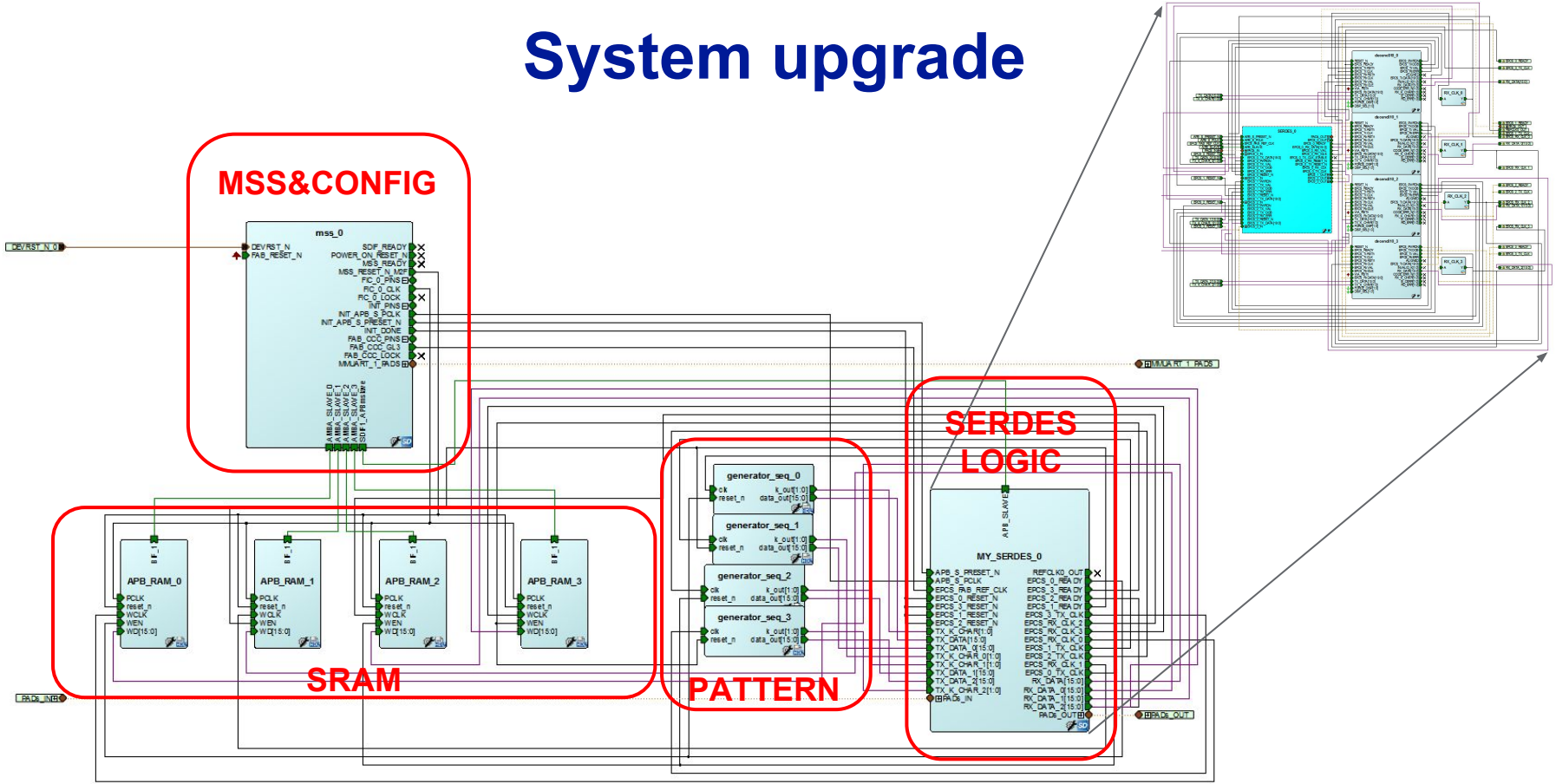
Problems with buses → New design for resets, buses and configuration logic

System upgrade

Upgrading from 1 lane to 4 lanes per SerDes block → More complex system, need to simplify some parts

Timing problem with SRAM → New design for SRAM control and other changes on clocks structure

System upgrade



DRAC tests

Different projects for ROC, HV and CAL:

- ROC needs 2 SerDes blocks and logic to power up the board
- HV and CAL need 1 SerDes block each

Tests comunications between different FPGAs:

- ROC-HV and ROC-CAL, separately and simultaneously

DRAC tests

Errors in protocol implementation led to unexpected behaviour:

- Data pattern correction to achieve the right syncronization between transmitter and receiver

Problems

Couldn’t solve timing violations when implementing 2 SerDes on ROC

Using PLL inside FPGA to get 100 MHz clock for SerDes communication. SerDes clock on DRAC is 156.25 MHz

First Solution

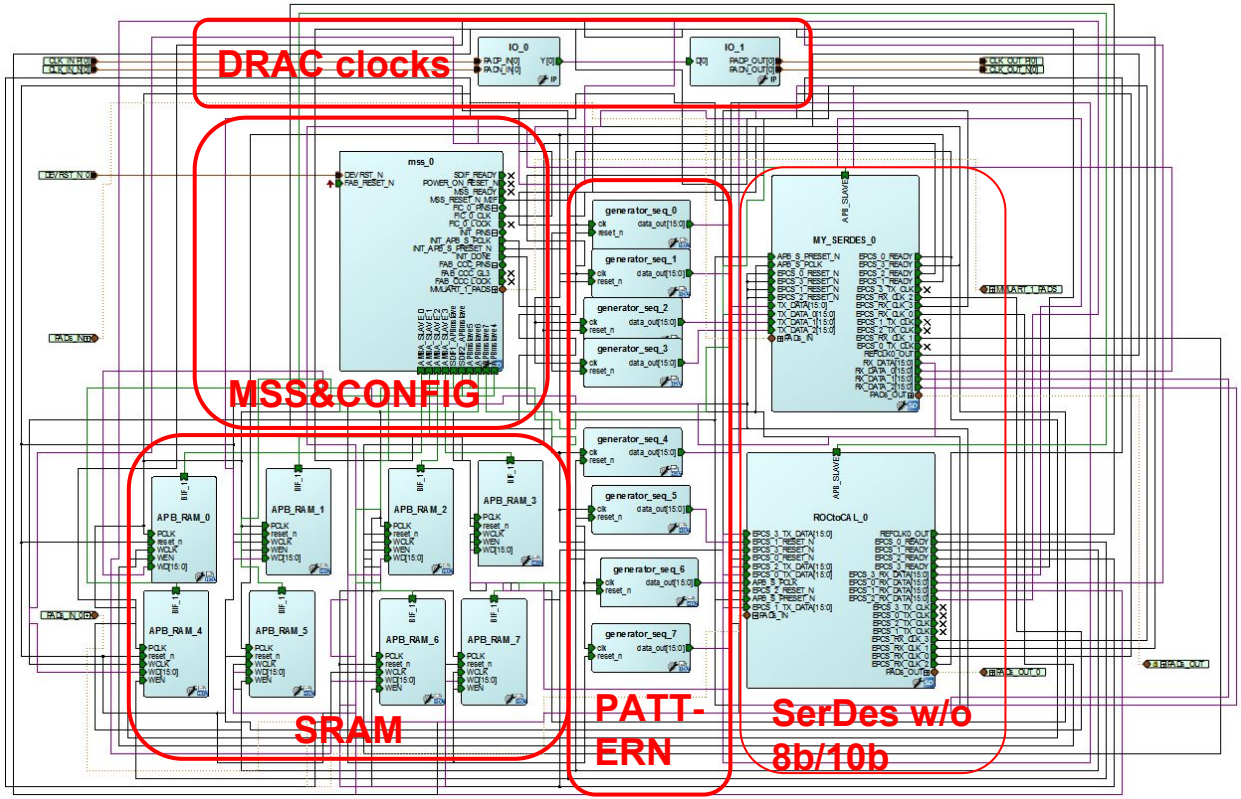
Send data without 8b/10b encoding:

- Can use DRAC clock, 16 bit at 156.25 MHz for 2.5 Gb/s datarate per lane
- Less logic, no more timing problems on ROC

Problems to be solved:

- Errors in packet recognition, bit shifted in received data

First Solution on ROC



Second Solution

In previous projects communication is bidirectional but no need to send data from ROC to HV or CAL. Use unidirectional communication:

- Needs less logic, can mantain 8b/10b encoding
- 8b/10b don’t have data shift problem

Cons:

- Need to use 100 MHz clock generated inside FPGA, 1.6 Gb/s true datarate

Implementation on final system

- Need to interface a FIFO with the SerDes

- Need to send FIFO status with the data

Thank you