



Characterization of CMOS Transistors and Testing of LVDS Circuit at Cryogenic Temperatures

Davide Severin Supervisor: Davide Braga Final Report– 25th September 2018

1) Characterization of CMOS Transistors at Cryogenic Temperatures

Characterization of CMOS transistors at different temperatures, starting from room temperature down to 65K

Goals

- Get familiar with standard device models
- Understand the effect of temperature on devices
- Learn how to use the test structure boards and instrumentations (SMU, cryocoolers, ..)
- Do measurement to model device



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Test Structure Boards

Devices that are to be characterized at <u>300K down to 65K</u>:

- Standard 65nm CMOS transistor thick-oxide: 2 nMOS and 2 pMOS (10/0.28 and 10/0.36)
- (Standard 65nm CMOS transistor thin-oxide: 15 nMOS and 15 pMOS)



Measurement Setup Room (300K) and **Low Temperature**



Cupper plate **Test Structure Board**

Cryocooler

Parameter Analyzer (SMU)







Examples of Measurement Performed at Room Temperature – Thick Oxide



nMOS $10\mu x 360n$ Output Characteristic



nMOS 10µ x 360n Input Characteristic



nMOS 10 μ x 280n Output Characteristic



nMOS 10µ x 280n Input Characteristic

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Example of Optimized Measurement at Room Temperature – Thick Oxide



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nMOS 10µ x 280n Input Characteristic

Measurement Performed at Low Temperature (Only Thick Oxide)

Type of Measurement:

- Input Characteristic
- Output Characteristic
- Weak Inversion Output Char.
- Strong Inversion Output Char.

Temperatures:

- 200K
- 173K
- 120K
- 87K Liquid Argon
- 77K Liquid Nitrogen
- 65K Lowest Temp. Achievable

Procedure:

- Measurement taken while decreasing Temperature (Step-Down cycle)
- Measurement taken while increasing Temperature (Step-Up cycle)

List of Device Tested:

- 65nm nMOS W/L (μ m) = 10/0.28
- 65nm nMOS W/L (μ m) = 10/0.36
- 65nm pMOS W/L (μm) = 10/0.28
- 65nm pMOS W/L (μ m) = 10/0.36



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Results – Saturation Current Graph:







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Troubleshooting

Small technologies are very sensitive to ESD and mechanical damages

Manipulating cables is the main cause of damages



Documentation

- The measurement setup: performing measurement and instrumentation instruction
- Test structure boards report: boards layout
- UTMOST software manual: synthesis of UTMOST software configuration

D	ocumentation			
Test Structure Board	T	OP – JP4 Jumps	er	
Standard CMOS 65nm thick ox	ide – CDP1 green board			
On this chip there are 4 transistor 65n - NMOS 1: W/L = 10/0.28 μm - NMOS 2: W/L = 10/0.36 μm - PMOS 1: W/L = 10/0.28 μm - PMOS 2: W/L = 10/0.36 μm PAD LIST:	m thick oxide:	CtP4	/	
1. SUBSTRATE p - always stuck a 2. PMOS1 - Gate 3. PMOS1 - Drain 4. PMOS1 - Source 5. PMOS1 - Bulk 6. PMOS2 - Gate 7. PMOS2 - Gate 7. PMOS2 - Drain 8. PMOS2 - Source 9. PMOS2 - Bulk 10. NMOS1 - Gate PMOS4.	t Vss 10. NMOS1 – Drain 11. NMOS1 – Source 12. NMOS1 – Buik 13. NMOS2 – Deep nWell 14. NMOS1 – Deep nWell 15. NMOS2 – Source 16. NMOS2 – Buik 17. NMOS2 – Buik 17. NMOS2 – Gate 18. NMOS2 – Drain SILVACO U	always stuck o always stuck o	rt Vad rt Vad	ual
	Prerequisites National Instrument – LabVIEW and NI NI-488.2 driver for LabVIEW (<u>http://sir</u> GPIB-USB Instrument Control Device Setup To do measurement it is necessary to connect Control Device. Connect the GPIB to the SMU SMU on.	MAX we.ni.com/psp/a the SMU with U and plug the U	jpp/doc/p/id/p JTMOST throu SB into your ci	sp-356/lang/en) gh the GPIB-USB Instrument amputer port, then turn the
	Open NI MAX software then click on Devices a If everything is correctly connected, NI GPIB-Li it. Be sure that GPIB interface ID is set on the correct name of the USB port (commonly GPIB1) otherwise change it and then click on Save. To check the name of the port in which the SMU is plugged in, use the Device Manager on your Windows. Finally click Scan for Instrument on the top menu and wait until the SMU is correctly detected (Instrument 0).	No official states	shown. Click o an an a	File Edit View Tools Help U Bufging and Decentral Information
	Check the primary address of the device (17 in this case) and write it down.	Ele folt View Tools Help Hennesdander weiter Station Weiter	H 21then Schwitz Settings Name Model Sinta Pinnay Address Identification	Inform & Consument University Internet inter

2) Preparing a LVDS prototype circuit to be tested at room and liquid argon temperature

LVDS (Low-Voltage Differential Signaling) is a technical standard protocol of serial communication with differential signals both in input and in output



Receiver:

- Input voltage : 2.5V to 1.8V
- Input diff. voltage: from ±100mV
- Output voltage: 1.2V (to the TX)



Transmitter:

- Input voltage: 1.2V (from the RX)
- Output voltage: 2.5V to 1.8V
- Programmable output current for driving long cables: ±2mA, ± 4mA, ± 6mA, ± 8mA

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Type of Measurement and Instrumentation



Type of Measurement

- Eye-Diagram
- Jitter
- BER
- Delay

Speed: Temperature:

- Supply Voltage:
- 128 MHz 2.5 V (nominal)

87 K

300K

- 1 GHz
 - Minimum one

TekTronic 1400 Mb/s Bit **Error Rate Tester** Generator and Analyzer

TekTronic DSA 72004C **Digital Serial Analyzer**



Designing and realizing the test structure board



- Wire-bonding pads and connector pins
- 1000hm resistor between the input of the receiver
- Test resistor to measure thermal variation
- SMA connectors
- Power supply by-pass capacitances



- Holes consistent with the cryostat grid
- General purpose
- Copper plates to make the temperature distribution more uniform

Simulations – Differential Output

128MHz, 300K and 84K, Different Corner, 2.5V HVDD, 1.2V VDD





Simulations – Differential Output

1GHz, 300K and 84K, Different Corner, 1.5V HVDD, 1.1V VDD



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Cable Measurements at Room Temperature



25m Samtec Cable – 50 MHz (200ns)

- BER < $1x10^{-12}$
- Total Jitter p-p = 630 ps
- Delay ≈ 200 ps



25m Samtec Cable – 100 MHz (100ns)

- BER < $1x10^{-11}$
- Total Jitter p-p = 830 ps
- Delay $\approx 200 \text{ ps}$







- Prepare and test the board

Future Plans

- Perform BER, Jitter and Delay measurement





Thanks for the attention



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