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Final report

Characterization of CMOS Transistors and Testing of LVDS Circuit at Room and Cryogenic Temperatures

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Characterization of MOSFET at cryogenic temperature

1.1 Introduction

Although silicon is the most studied material, the behavior of silicon device at very low temperatures is still under research. Several non-idealities occur when ICs are cooled down to 1K or even below. With the advent of quantum computing theories, the necessity of accurate low-temperature models of electronic devices has become more urgent. Most qubits are operated below 100mK, but, at the state of the art, readout CMOS electronic works at room temperature. Data are sent through expensive amplifications to be read and vice versa controlling quantum components requires sending signals from room temperature down to 100mK through 90dB cold attenuation. Given that the complexity of such control and readout system scales linearly with the number of qubits, these operations are complicated and inefficient in size, power, cost and speed [1].

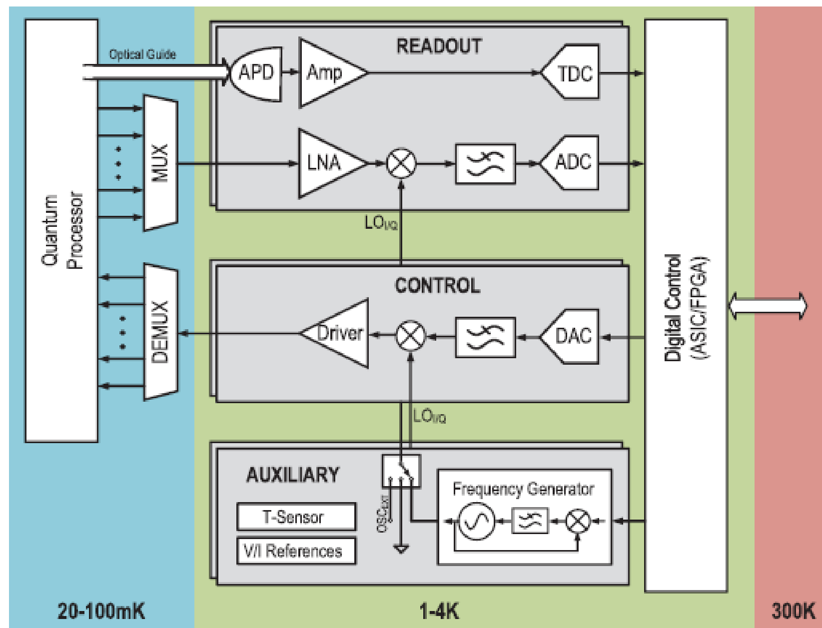


Figure 1.1: Scheme of a generic CMOS readout system

The ultimate goal of this project is to design a new readout system that works at cryogenic temperature, so this first and most important stadium of signal processing would operate at temperatures which are similar to the qubits' one (Fig. 1.1). This improvement permits to optimize the two-way communication between computer and readout/control front-end, considering that cooling systems must not be more power-consumptive than the original system (i.e. cryo-readout must be low-power). The first obstacle which must be confronted is the lack of reliable device models for operating at deep-cryogenic temperatures. This work aims to address the creations of such models.

1.2 Low-temperature effects and non-idealities

At the beginning cryogenic effects and non-idealities of CMOS technology were investigated. According to [2], the most relevant ones are:

- Increase in carrier mobility and mean free path (except for pMOS in weak inversion region). It is caused by the freezing of silicon lattice
- Carriers freeze-out: below 100K, carriers are mostly generated by ionization of dopants. As the temperature decreases, thermal energy reduces and ionized carrier density diminishes as well (Fig. 1.2). It depends on doping concentration too

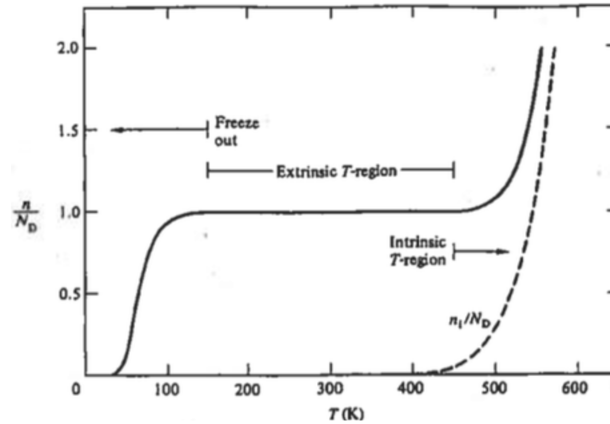


Figure 1.2: Carrier concentration vs Temperature

- Long-term increase of V_{th}, due to hot carrier damages (Fig. 1.3). Hot carrier injection (HCI) is a phenomenon in MOS devices where an electron or a hole gains sufficient kinetic energy (especially near the drain terminal, where electric field is more intense) to overcome the potential barrier and becomes trapped in the gate dielectric.

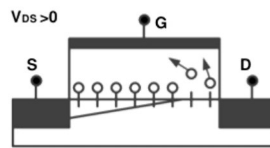
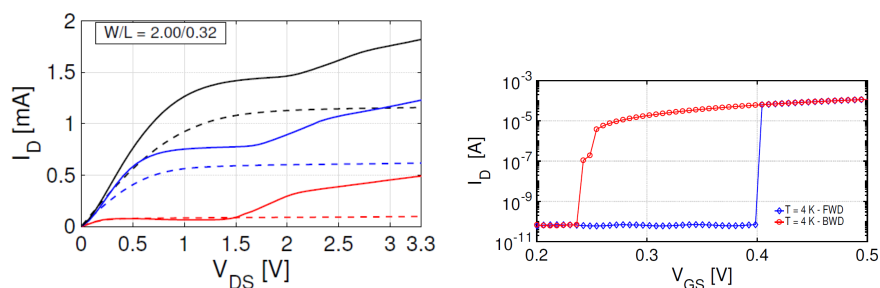


Figure 1.3: Hot Carrier effect

- Increasing of Sub-threshold Slope due to intrinsic temperature dependence of diffusion current
- Kink effect and hysteresis: non-idealities occurring in mature technologies (typically $> 130nm$) that cause anomalous behaviors. Experimental characteristics are strongly divergent from theoretical ones (Fig: 1.4)



(a) Tilt on an nMOS characteristic caused by Kink Effect

(b) Hysteresis on an turn-on/turn-off cycle caused by the Kink Effect

Figure 1.4: Kink Effect and Hysteresis

It was possible that some of these effects were evident during the experiment.

1.3 Models

Modeling a device behavior means defining algebraic equations that closely describe experimental characteristic curves. In practice, there are many established models, each with its pros and cons. Modeling involves choosing the appropriate one and adjusting some standard parameters to make the equations fit the physical behavior of the device. Some of the most prevalent models are:

- BSIM: most famous and used. BSIM 4 is adequate to model transistor of different sizes, down to 65nm and below
- EKV: the simplest and most versatile one. Probably not adequate for 65nm transistors and incomplete for cryo-application
- PSP: more adequate at extreme temperatures but less used and known

BSIM 4.0 was chosen to compare with the BSIM4 models provided by the foundry for standard-temperature operation.

1.4 The experiment

The experiment consisted in measuring and characterizing the following transistors at room temperature down to 50 K (all dimensions in μm):

- Standard 65nm CMOS transistors - thick-oxide:
  1. nMOS W/L = 10/0.28
  2. nMOS W/L = 10/0.36
  3. pMOS W/L = 10/0.28
  4. pMOS W/L = 10/0.36
- Standard 65nm CMOS transistors - thin-oxide:
  1. nMOS W/L = 0.5/0.06
  2. nMOS W/L = 0.5/0.1
  3. nMOS W/L = 0.5/0.2
  4. nMOS W/L = 1/0.06
  5. nMOS W/L = 1/0.1
  6. nMOS W/L = 1/0.2
  7. nMOS W/L = 2.5/0.06
  8. nMOS W/L = 2.5/0.1
  9. nMOS W/L = 2.5/0.2
  10. nMOS W/L = 5/0.06
  11. nMOS W/L = 5/0.1
  12. nMOS W/L = 5/0.2
  13. nMOS W/L = 10/0.06
  14. nMOS W/L = 10/0.1
  15. nMOS W/L = 10/0.2
  16. nMOS W/L = 25/0.06
  17. nMOS W/L = 25/0.1
  18. nMOS W/L = 25/0.2
  19. pMOS W/L = 0.5/0.06
  20. pMOS W/L = 0.5/0.1
  21. pMOS W/L = 0.5/0.2

22. pMOS W/L = 1/0.06
23. pMOS W/L = 1/0.1
24. pMOS W/L = 1/0.2
25. pMOS W/L = 2.5/0.06
26. pMOS W/L = 2.5/0.1
27. pMOS W/L = 2.5/0.2
28. pMOS W/L = 5/0.06
29. pMOS W/L = 5/0.1
30. pMOS W/L = 5/0.2
31. pMOS W/L = 10/0.06
32. pMOS W/L = 10/0.1
33. pMOS W/L = 10/0.2
34. pMOS W/L = 25/0.06
35. pMOS W/L = 25/0.1
36. pMOS W/L = 25/0.2

These devices are fabricated in several test ICs, which are mounted on custom test boards. Some of these boards are in ceramic, which has a coefficient of thermal expansion similar to silicon's one. The other side of the board directly contacts the copper plate in the cryostat: this plate is then cooled down and so do the chip.

In every chip, transistor are manufactured one close to the other in a chain: drain and source pads are in common. The pads for the gates are instead independent: in this way it is possible to turn on only one transistor per measurement, to test them separately.

A cryostat was used to cool down transistors.(Fig. 1.5). It could chill down to 50K.

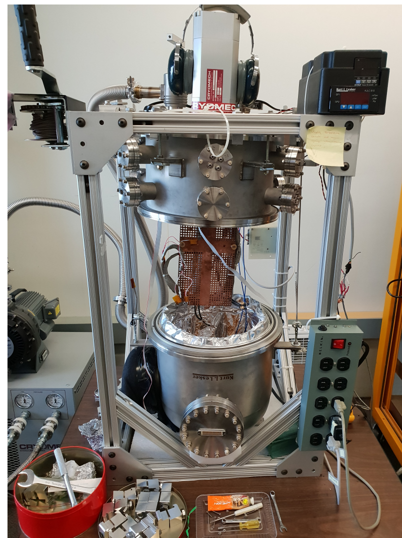


Figure 1.5: The cryostat used for this experiment can reach temperatures down to 50K

1.5 Setup and Measurements

1.5.1 Go/No-go testing

The first measurement involved a 65nm thick-oxide test chip which was wired-bonded to a 64 PGA socket. The purpose was to get familiar with the instrumentation and try the device functioning at room temperatures (Fig. 1.6).

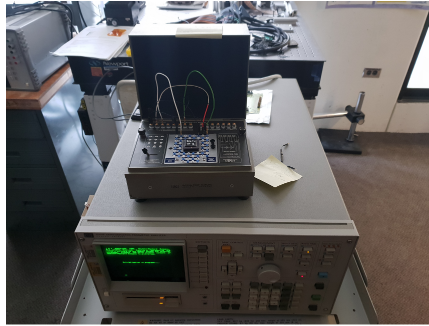
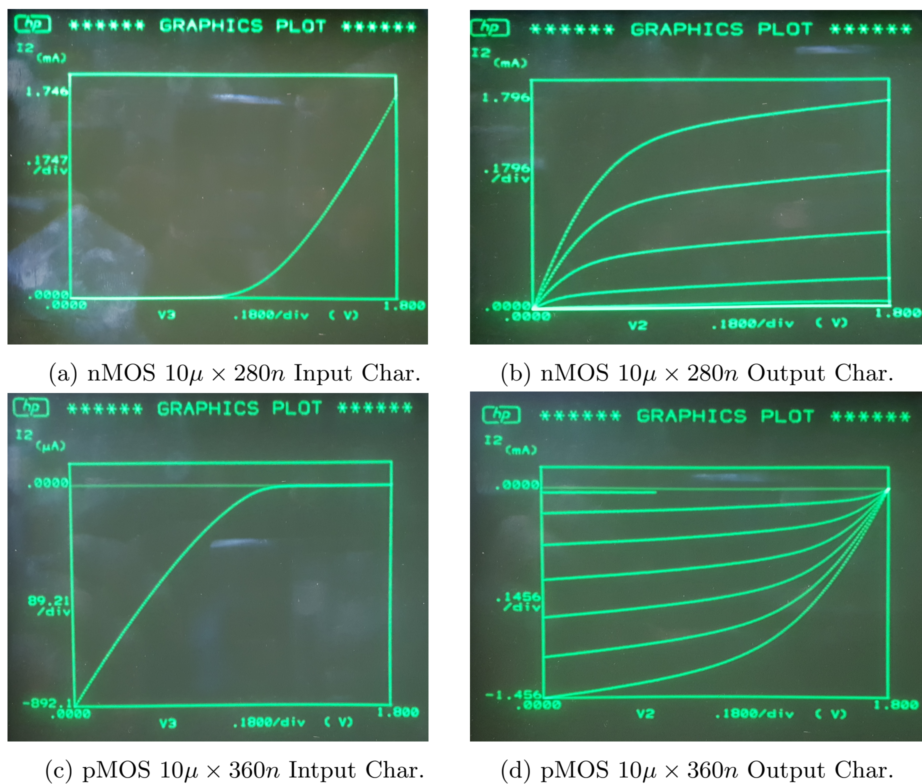


Figure 1.6: Testing of the 65nm thick-oxide board



(a) nMOS $10\mu \times 280n$ Input Char. (b) nMOS $10\mu \times 280n$ Output Char.

(c) pMOS $10\mu \times 360n$ Intput Char. (d) pMOS $10\mu \times 360n$ Output Char.

Figure 1.7: Devices characteristics

To test, the following instrumentation was used:

- HP 16058A Test Fixture to connect the socket pin to the SMU
- HP 4145B Semiconductor Parameter Analyzer (SMU) to obtain automatically the characteristics

Both pMOS and nMOS (10/0.28 and 10/0.36) were tested and found to be working properly (Fig. 1.7).

1.5.2 Performing measurement – Room Temperature

The same instrumentation was used to perform measurement on test structure boards. Silvaco UTMOST was the software used to control automatically the settings on the SMU and to store acquired data. It could communicate with the instrumentation through an NI GPIB-USB Instrument Control Device, which was used to connect the laptop with the SMU (Fig. 1.8).

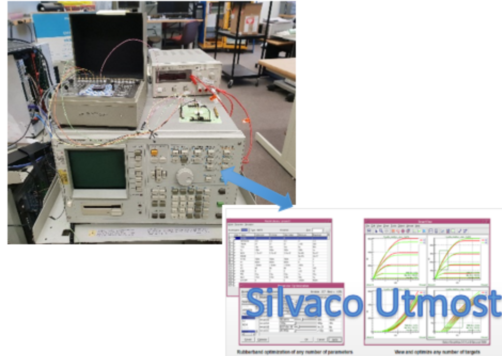


Figure 1.8: Measurement Setup

Silvaco UTMOST includes an optimization tool too, which is able to fit the curves, extract the model parameters and, if necessary, do comparison between different models.

1.5.3 Type of Measurements

Set of measurements to be performed on nMOS (V_{DD} = 1.5V):

- Input Characteristic – I_D vs V_{GS} (V_{BS} parametric):
  1. Source stuck at GND
  2. Drain stuck at 1V
  3. Gate sweep [0V, 1.5V]
  4. Bulk sweep [-400mV, 0V] - Body effect
- Output Characteristic – I_D vs V_{DS} (V_{GS} parametric):
  1. Source stuck at GND
  2. Drain sweep [0V, 1.5V]
  3. Gate sweep [0V, 1.5V]
  4. Bulk shorted to Source
- Weak Inversion Output Characteristic – I_D vs V_{DS} (V_{GS} parametric):
  1. Source stuck at GND
  2. Drain sweep [0V, 1.5V]
  3. Gate sweep [400mV, 800mV]
  4. Bulk shorted to Source

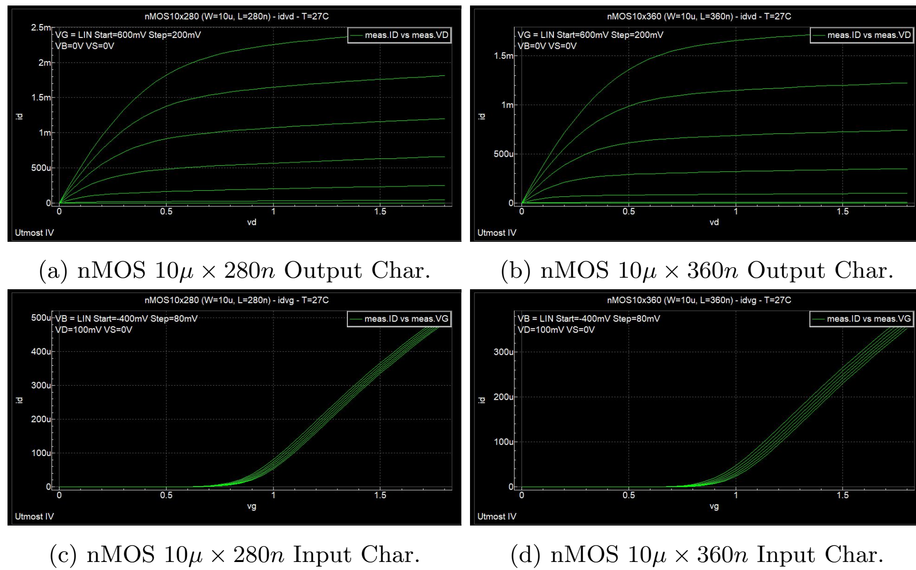
Type of measurement to be performed on pMOS (V_{DD} = 1.5V):

- Input Characteristic – I_D vs V_{GS} (V_{BS} parametric):
  1. Source stuck at V_{DD}
  2. Drain stuck at 500mV
  3. Gate sweep [0V, 1.5V]

4. Bulk sweep [1.5V, 1.9V] - Body effect

- Output Characteristic – I_D vs V_{DS} (V_{GS} parametric):
  1. Source stuck at V_{DD}
  2. Drain sweep [0V, 1.5V]
  3. Gate sweep [0V, 1.5V]
  4. Bulk shorted to Source
- Weak Inversion Output Characteristic – I_D vs V_{DS} (V_{GS} parametric):
  1. Source stuck at V_{DD}
  2. Drain sweep [0V, 1.5V]
  3. Gate sweep [700mV, 1.1V]
  4. Bulk shorted to Source

Both 65nm thick-oxide and 65nm thin-oxide boards were measured at room temperature: input and output characteristics were taken (Fig. 1.9). Input characteristic was then processed with the optimization tool and fitted with an approximating error lower than 2% (Fig. 1.10).



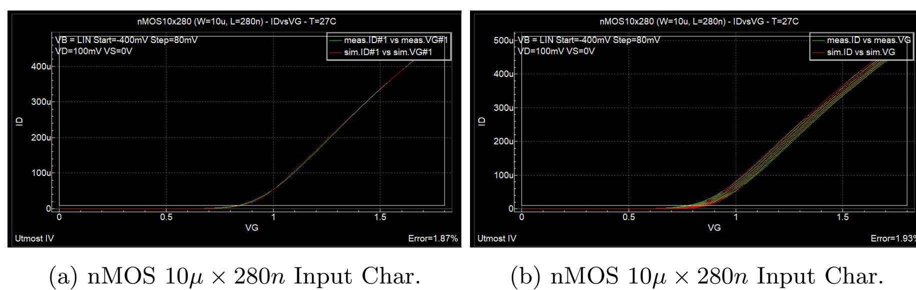
(a) nMOS $10\mu \times 280n$ Output Char.

(b) nMOS $10\mu \times 360n$ Output Char.

(c) nMOS $10\mu \times 280n$ Input Char.

(d) nMOS $10\mu \times 360n$ Input Char.

Figure 1.9: Devices characteristics



(a) nMOS $10\mu \times 280n$ Input Char.

(b) nMOS $10\mu \times 280n$ Input Char.

Figure 1.10: Optimization and modeling of characteristics

1.5.4 Performing measurement – Low Temperature

Test structure boards were then placed inside the cryostat to be chilled. The back side of the ceramic board contacted the main copper plate inside the cryocooler. The vacuum (40 mTorr down to 1 mTorr) was then achieved inside the cryocooler and a closed loop of liquid helium directly cooled the copper plate down. All the necessary pins were taken out with a bundle of cables: measurement were performed externally with the same equipment used at room temperature. On the plate there were three RTDs (Resistance Temperature Detectors): one of them was a feedback sensor to set correctly the temperature on the top of the copper plate from the outside with a thermostat. The others were used to sense the temperature on the bottom of the copper plate and on the board. In fact, the system was not entirely at the same temperature: there were some losses due to the thermal impedance of the plate and the ceramic. There was approximately 7K difference between the copper plate and the front side of the ceramic board. To compensate this loss, temperature was always set at a lower value. Only the 65nm thick-oxide board was measured at low temperature and precisely at 200K, 173K, 120K, 89K, 77K and down to the minimum temperature achievable (65K). Measurement were taken starting from room temperature down to the bottom (step down cycle) and then again from 65K up to 300K (step up cycle). Theoretically there should not be any difference between cooling down and warming up: the two cycle should be similar. As the temperature decreases, saturation current should increase due to the increasing channel mobility, even if the threshold voltage is rising.
Our observations are:

1. pMOS 10/0.36 was most certainly damaged as the temperature reached 150K, and no more data were collected from it

2. pMOS 10/0.28 (Fig. 1.11): this is the best result achieved. Step up and step down cycle are very similar (error below the 4%) and the current increases as the temperature diminishes. There is a current spike at 173K, probably due to a measurement artifact

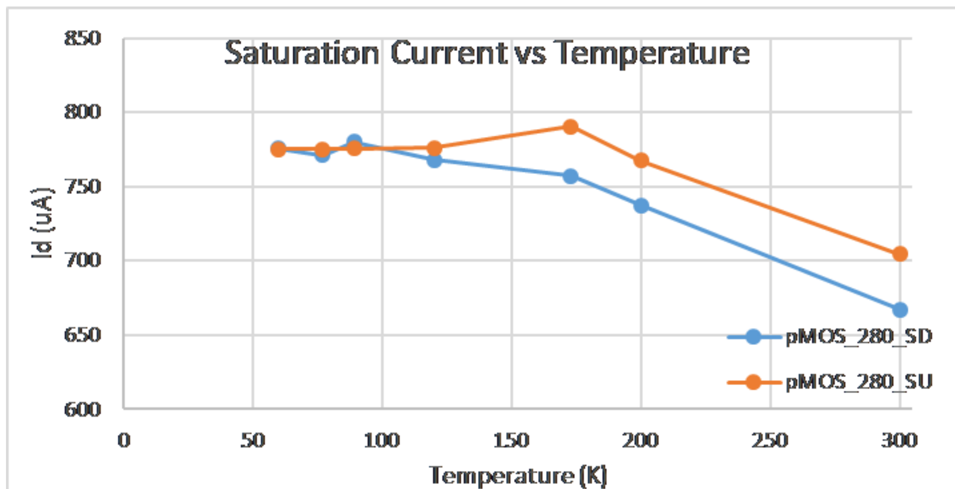


Figure 1.11: Saturation Current vs Temperature - pMOS 10x280

3. nMOS 10/0.28 (Fig. 1.12): globally the curve is descending as expected but there are two critical steps. During step down cycle, between 120K and 89K the curve rapidly increases, and then again between 65K and 77K while warming up. This behavior is a symptom of irreversible degradation of the device. Therefore, the two cycles are not similar: there is a mean error greater than 30%

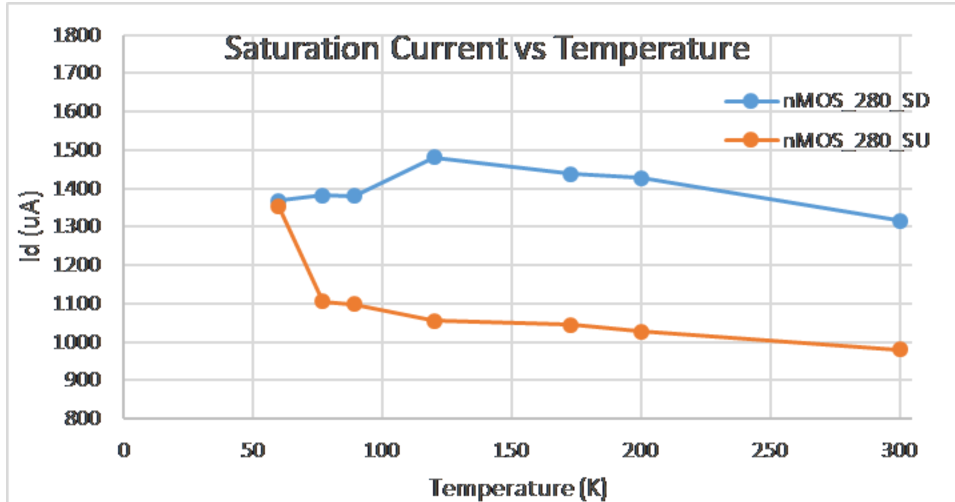


Figure 1.12: Saturation Current vs Temperature - nMOS 10x280

4. nMOS 10/0.36 (Fig. 1.13): there is an irreversible damage in the very first measure (from 300K to 200K). Saturation current diminishes of more than 50% of its mean value. Step up and step down cycle are very similar, but the trend is ascending as the temperature rises, which is inconsistent with the theoretical behavior. It seems like the increasing of the threshold voltage prevails on the increasing of the channel mobility

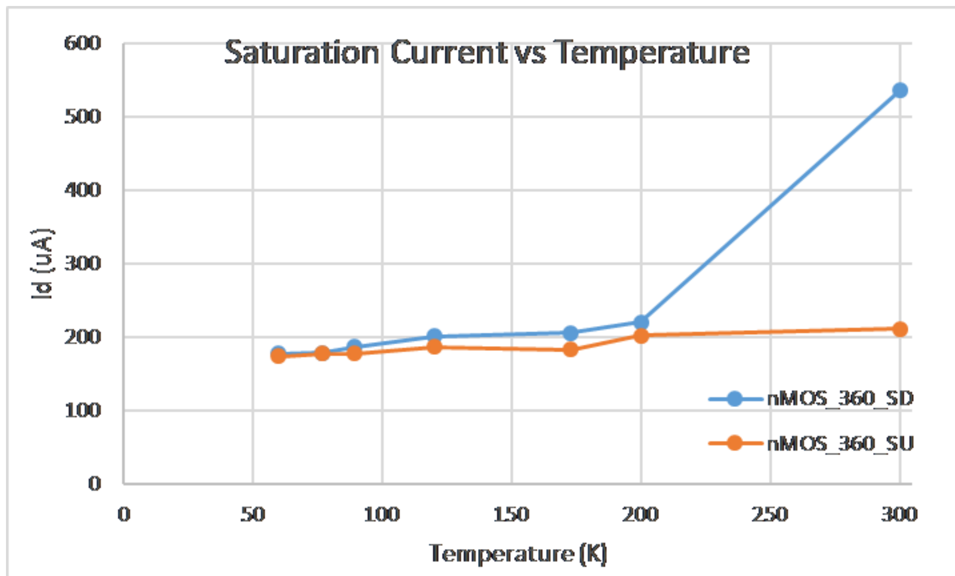


Figure 1.13: Saturation Current vs Temperature - nMOS 10x360

Results are conflicting and not completely coherent with the theoretical behavior: the curve is not always descending and there are some symptoms of devices degradation. Those results are not completely reliable: it is necessary to test other boards to compare data.

Causes of measurement failures:

- Cooling-down process: damage from hot-carrier ionization can manifest itself as permanent degradation even in the first milliseconds of operations under stressful conditions. It should explain the critical behavior of the nMOS 10/0.36 between 300K and 200K
- Wire bonding and measurement procedure: 65nm technology is very sensible to ESD and mechanical damages (especially gate terminals which are thin and fragile), which could strongly

affect device performances. Those damages get more critical when cooling down. Probably the most dangerous thing is handling wires: to connect pins to the SMU wires were manually connected. In many procedures, it is suggested not to manipulate cables because it is the main cause of damages

New measurement should be taken using a switching system: it does not require any manipulation. All the cables are connected to an input matrix and the output is chosen via software.

A Keithley 7002 switch system (Fig. 1.14) is chosen: it can support up to 10 input for every output. It is fully compatible with UTMOST software: there is no need of manual configuration.

Figure 1.14: Keithley 7002 - switch system

1.5.5 Break in activities – Documentation

Since the UTMOST software license expired, no more measurement could be performed. A documentation of the job was redacted and it summarized:

- Test structure boards report (*Appendix A*): how test structure boards are made, which pins are connected and how, how many transistors there are and which dimensions they have
- UTMOST software manual (*Appendix B*): a synthesis of UTMOST software configuration. It also describes how to connect the *GPIB-USB Control Device* using *NI LabVIEW* software

Preparing a LVDS prototype circuit to be tested at room and liquid argon temperature

2.1 Introduction

LVDS (Low-Voltage Differential Signaling) is a technical standard protocol of serial communication with differential signals both in input and in output. As suggested by the name itself, it commonly operates at very low power. It works at low voltages (2V down to some hundreds of mV) and can run at high-speed (up to some GHz) along cheap twisted pair cables. A new LVDS circuit was designed with 65nm standard CMOS technology in Fermilab for operation at cryogenic temperatures (liquid argon high energy physics detector). It has not been tested yet. The aim of the experiment is realizing a test structure board where chip will be mounted on with appropriate pins which will be wire-bonded to the corresponding pads. Then the circuit will be tested at room temperature and at 87K with different supply voltages and at different speeds. In fact, the circuit should work at frequencies below 128 Mbit/s but, to test the limits, it will be run at higher speeds too, up to 1 Gbit/s. Parameters that should be extract are:

- BER (Bit Error Rate)
- Eye-Diagram
- TJ@BER (Total jitter at a specified bit error rate (BER). This combines the random and deterministic effects, and predicts a peak-to-peak jitter that will only be exceeded with a probability equal to the BER)
- Delay between input and output signals

To perform measurements, the instrumentation used was:

- TekTronic 1400 Mb/s Bit Error Rate Tester Generator and Analyzer (Fig. 2.1): this system generates PRBS Pseudo Random Bit Streams (up to 23 bits at $2V\ peak - to - peak$ and 1400 MHz) which are sent through the LVDS circuit and then collected by a receiver which calculates the BER (counting the number of bit error)

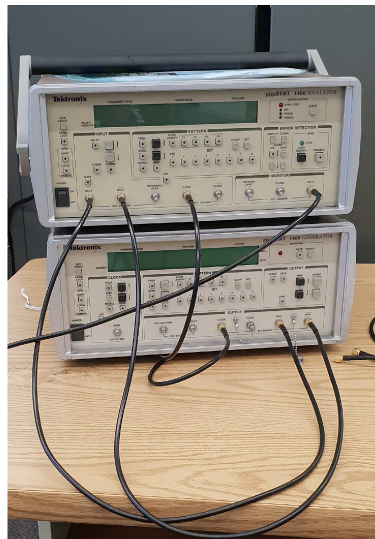


Figure 2.1: TekTronic 1400 Mb/s Bit Error Rate Tester Generator and Analyzer

- TekTronic DSA 72004C Digital Serial Analyzer (Fig. 2.2): this oscilloscope can analyze the output PRBS from the LVDS and calculate the eye-diagram, the jitter and the delay.
- Cryostator: it can chill down to 50K

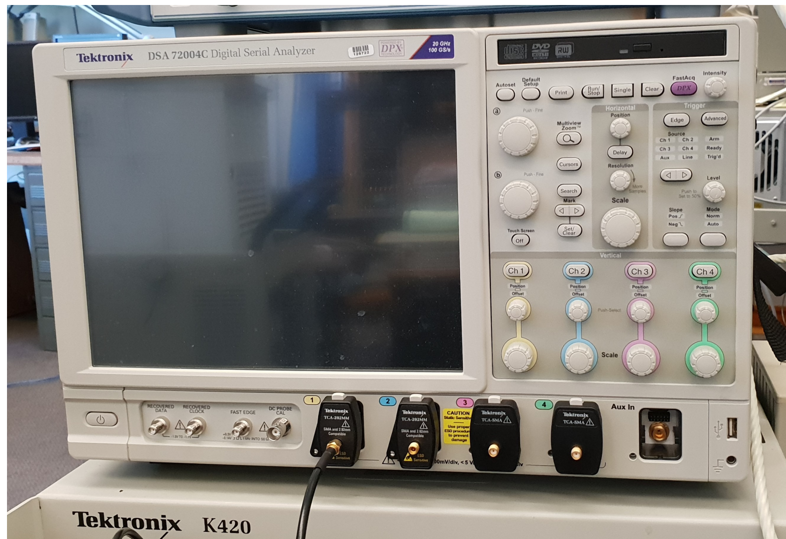


Figure 2.2: TekTronic DSA 72004C Digital Serial Analyzer

2.2 LVDS Schematic

The circuit is composed basically of a receiver (Fig. 2.3), which processes the input signal and send it to the chip core, followed by a transmitter (Fig. 2.4), which replicates the signal elaborated by the receiver.

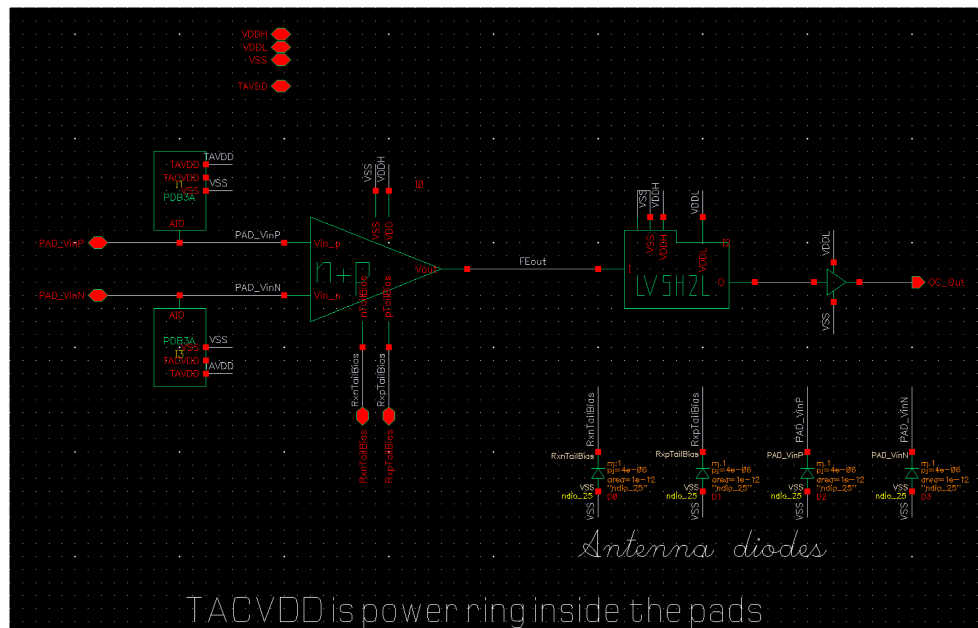


Figure 2.3: LVDS Receiver - Schematic

Receiver main features are:

- Input voltage domain: $2.5V$ to $1.8V$ (from the chip I/O supply). Input differential voltage from $\pm 100mV$. Output voltage: $1.2V$ (to the chip core)
- Operating temperature range: intended for room temperature as well as liquid argon (87K)
- Low profile layout: approximately $115\mu m \times 20\mu m$, excluding the output pads

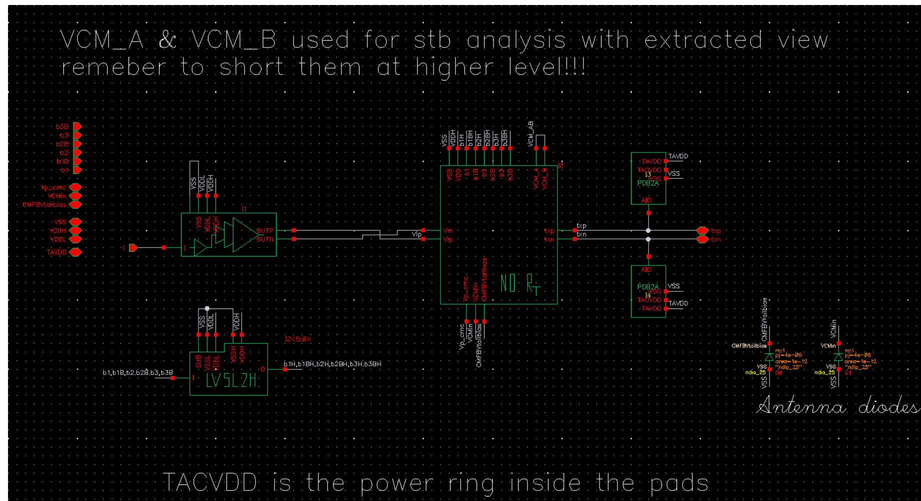


Figure 2.4: LVDS Transmitter - Schematic

Transmitter main features are:

- Input voltage: $1.2V$ (from chip core). Output voltage: $2.5V$ to $1.8V$ (from chip I/O supply)
- Programmable output current for low power operation: $\pm 2mA$, $\pm 4mA$, $\pm 6mA$, $\pm 8mA$
- Operating temperature range: intended for room temperature as well as liquid argon (87K)
- Includes an active common mode feedback (CMFB) to stabilize the CM to $1/2\ V_{DD}$
- Low profile layout: approximately $180\mu m \times 65\mu m$, excluding the output pads

2.3 Simulations

The circuit schematic was simulated in different conditions:

- High Supply Voltage: from $2.5V$ (nominal) down to $1.5V$
- Low Supply Voltage: $1.2V$ (nominal) and $1.1V$
- Technology Corner: Fast, Slow, Room Temperature, -186°C
- Output current: $2mA$, $4mA$, $6mA$, $8mA$
- Frequency: 128MHz and 1GHz

The intention was to simulate the circuit in nominal conditions, but even pushing it to the limit in frequency, voltages and manufacturing corners to detect the theoretical working maximum. The system should work correctly in various conditions: the input signal is regenerated, adapted and then replicated with a very short delay ($< 1ns$ in nominal condition). Below $1.8V$ of HV_{DD}, the power supply is too low to properly bias all the subcircuits: at $1.5V$ (Fig. 2.7) the signal is, in some cases, not valid.
Technology corners could be simulated:

- A faster device has a lower threshold: it can work even at lower voltages and it responds earlier
- A cooled device has a higher threshold but higher currents too (at fixed supply voltages)

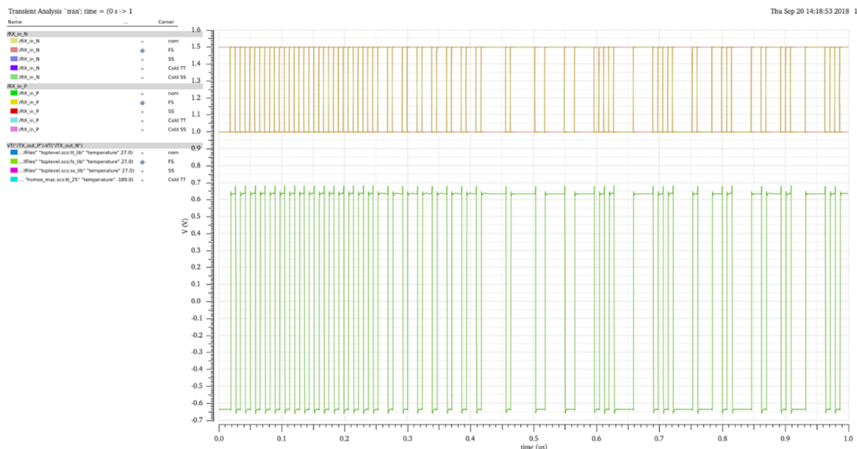


Figure 2.5: Diff. Input and Output - 128MHz, 300K, Nominal Corner, 2.5V HV_{DD}, 1.2V V_{DD}

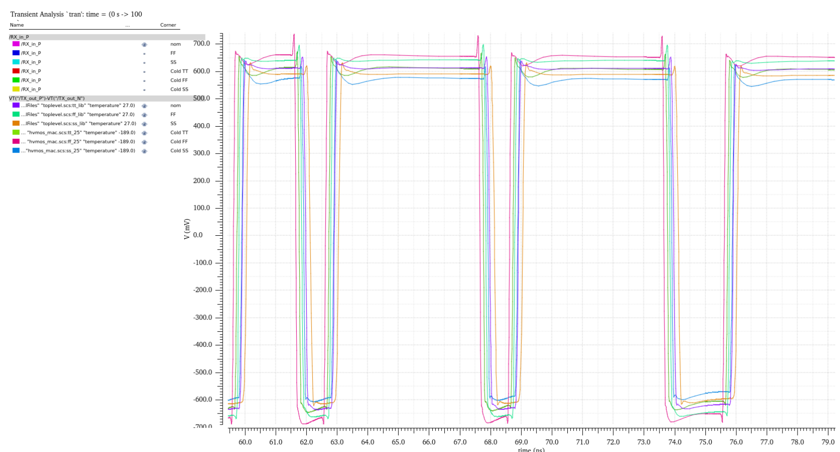


Figure 2.6: Differential Output - 1GHz, 300K and 84K, Different Corner, 2.5V HV_{DD}, 1.2V V_{DD}

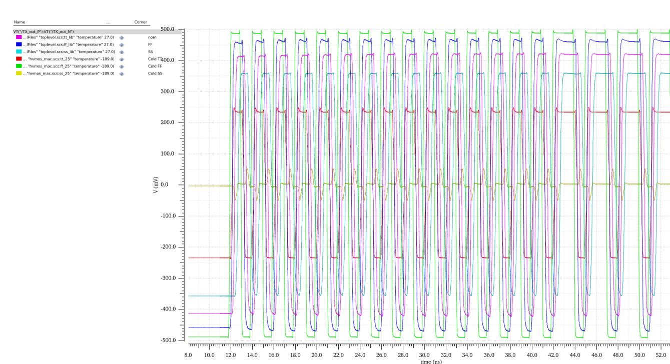


Figure 2.7: Differential Output - 1GHz, 300K and 84K, Different Corner, 1.5V HV_{DD}, 1.1V V_{DD}

2.4 Getting accustomed to the instrumentation

To get familiar with the instrumentation a 25m Samtec cable was tested at room temperature: nominally it should be robust up to 50 MHz and down to 77K and below.

- Initially a 50MHz signal was generated: the eye-diagram obtained (Fig. 2.8) is clearly open and the expected BER for a correct sampling should be lower than $1x10^{-12}$. In fact, the BER analyzer did not registered any stream error in an entire day of testing

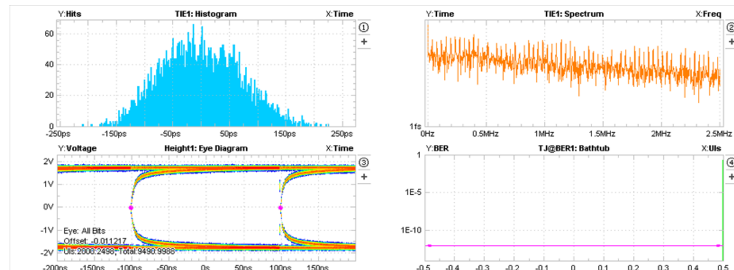


Figure 2.8: TIE, eye-diagram and TJ bathtub diagram of a 25m cable at 50MHz

TJ@BER	630ps
BER	<$1x10^{-12}$
Delay	$\approx$ 200ps

- The cable was already tested at 100MHz: the eye is more constrained but still opened. The low-pass behavior of the cable begins to be evident. The bathtub diagram shows the suggested interval of sampling for a fixed BER: this interval is narrower if compared to the 50MHz one

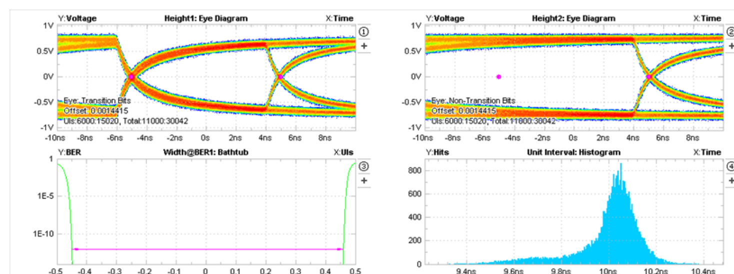


Figure 2.9: TIE, eye-diagram and TJ bathtub diagram of a 25m cable at 100MHz

TJ@BER	830ps
BER	<$1x10^{-11}$
Delay	$\approx$ 200ps

- The system was tested with a 500MHz signal too: the period was too short and the eye completely shut. The instrumentation even failed to determine the correct period of the signal

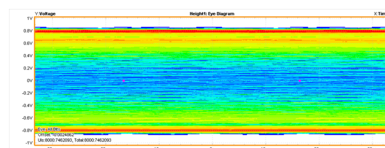


Figure 2.10: Eye-diagram of a 25m cable at 500MHz

2.5 Test structure board realization

Since the chip had not been tested yet, there was no board compatible which the chip could be mounted on and wire-bonded. Therefore, a new board was designed and realized: the intention was to reuse the other test-structures layout (which is general purpose) and modify it. In this way new boards were suitable both for transistors IC and for LVDS IC. The LVDS IC has twelve pads for the transmitter and the receiver (differential signals), the power supplies, the output bias voltage and swing controllers.

New boards (Fig. 2.11) should have had:

- Wire-bonding pads and pin connectors
- 100Ω resistor between the input of the receiver (to convert the current input into a voltage one).
- Test resistor (100Ω) to measure resistance variation while cooling down
- SMA connectors for the receiver and the transmitter
- Power supply by-pass capacitors

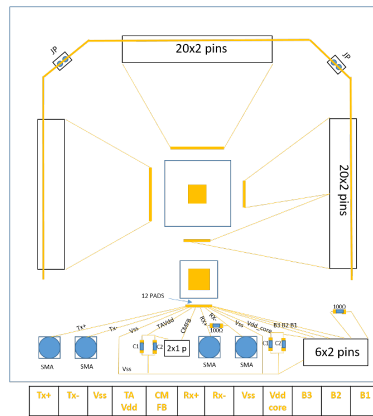
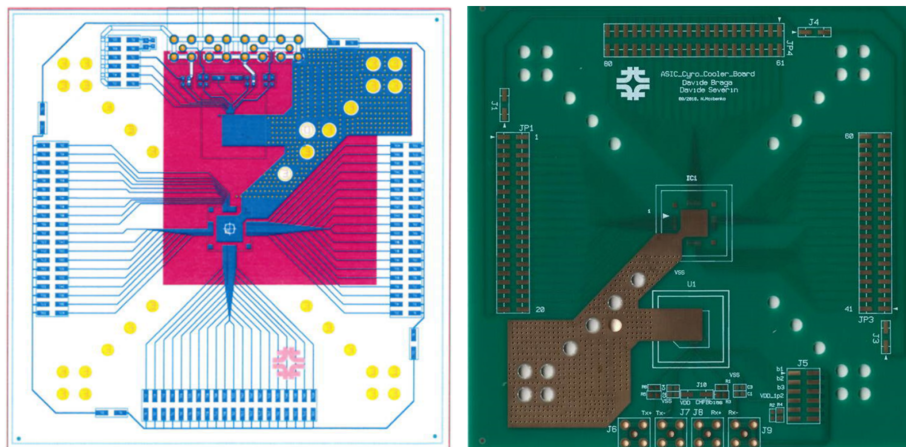


Figure 2.11: Scheme of the new test structure board designed

Board was designed and realized in FR4 (Fig. 2.12): it is less expensive but it has a higher thermal resistance. To compensate the temperature loss between the top and the bottom layer the cryostat was set at a lower temperature. In this way the top layer temperature was at the nominal one (87K). Copper plates were added to make the temperature distribution more uniform.



(a) Layout of board (b) Final aspect of the board

Figure 2.12: New test structure board

2.6 Measurements

2.6.1 Room Temperature

The chip was mounted on the board and tested at room temperature. Delay measurements were not taken due to lack of time.

- 128 MHz – $2mA$ output current – $2.5V$ V_{DD} – Room Temperature

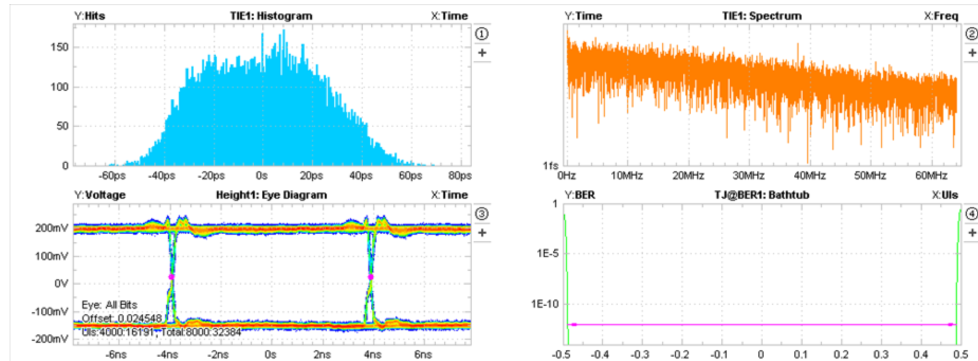


Figure 2.13: Eye Diagram and Time Interval Error (TIE) at 128 MHz - Room Temperature

The eye is open (Fig. 2.13) and the bathtub curve is wide. Data obtained are:

TJ@BER	$184ps$
BER	$<1 \times 10^{-10}$
Delay	-

- 1 GHz – $2mA$ output current – $2.5V$ V_{DD} – Room Temperature

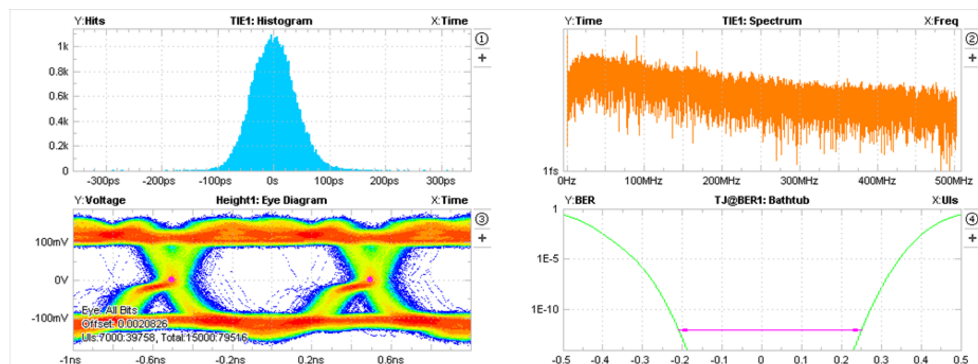


Figure 2.14: Eye Diagram and Time Interval Error (TIE) at 1 GHz - Room Temperature

The eye is more constrained (Fig. 2.14) and the optimum sampling interval is narrower than the one at 128 MHz. Data obtained are:

TJ@BER	$527ps$
BER	$<1 \times 10^{-9}$
Delay	-

2.6.2 Low Temperature - 120K

The board was then put into the cryostat and chilled down: unfortunately, the thermal resistance of FR4 was too high and the system could not chill the chip down to 87K in time. Therefore, measurements were taken at 120K. Furthermore, the maximum frequency reached was 512 MHz: above this, the output signal was no more recognizable and processable. Delay and BER measurements were not taken due to lack of time.

- 128 MHz – $2mA$ output current – $2V$ V_{DD} – 120K

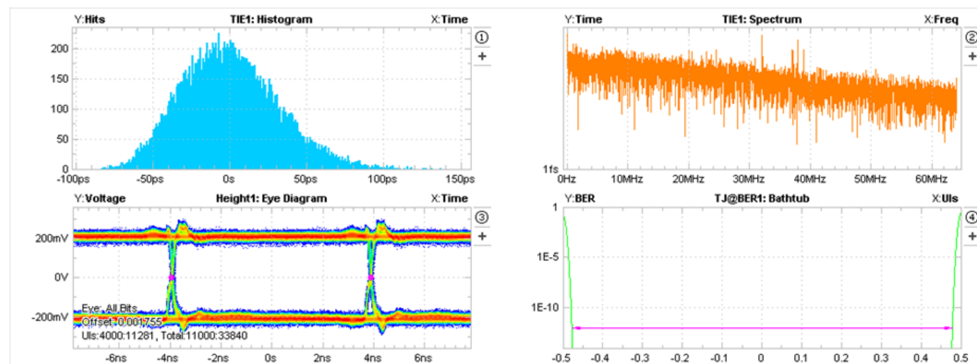


Figure 2.15: Eye Diagram and Time Interval Error (TIE) at 128 MHz - 120K - $2V$ V_{DD}

The eye is open (Fig. 2.15) and the bathtub curve is wide. Data obtained are:

TJ@BER	$340ps$
BER	-
Delay	-

- 1 GHz – $2mA$ output current – $2V$ V_{DD} – 120K

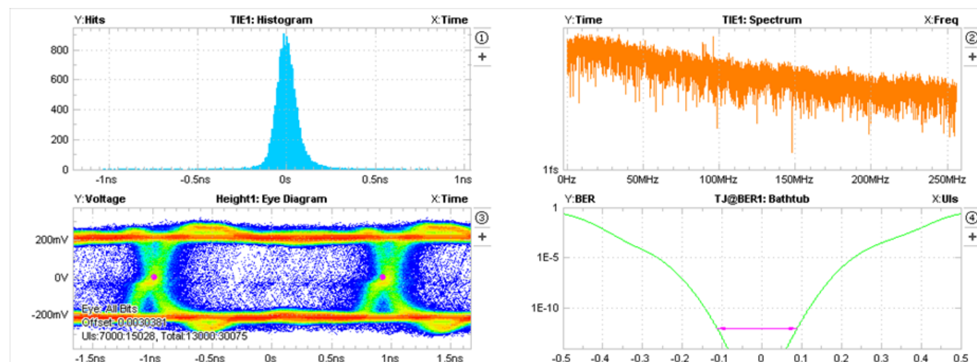


Figure 2.16: Eye Diagram and Time Interval Error at 1 GHz - 120K - $2V$ V_{DD}

At 512MHz (Fig. 2.16), even if the eye was recognizable, the jitter was too elevated and the bathtub curve almost shut: the chip was working out of its limit. No data are then reported.

2.7 Final considerations and future developments

The board developed has all the necessary requirements. The output signal is not completely compatible with the simulation and data measured are sometimes worse than the expected ones. Even if the bathtub curve registers in many cases a theoretical BER value below of 1×10^{12}, direct measurements are actually near to 1×10^{10}. This critical difference is imputable to:

- A systematic delay between the two output differential signal attributable to different lengths of the SMA connectors mounted on the board. This causes a wrong alignment between the output that is a distortion of the differential signal (Fig. 2.17).

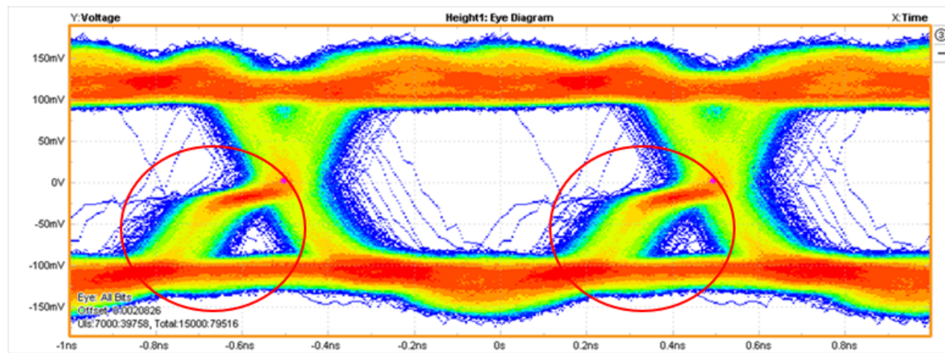


Figure 2.17: Macro - Eye Diagram

  That causes a higher jitter and constriction of the eye: replace the connectors (using 4 identical components) in a future new test structure board could improve the performances

- The output signal is actually affected (not visible from the diagrams) by some glitches that compromises the integrity of the signal. Those glitches have still an unknown origin: probably the output section requires an additional resistor or the signal is too fast to be measured with a coaxial cable and it is necessary a twisted pair cable and a differential probe to perform better measurements

Bibliography

[1] Bishnu Patra, *Student Member, IEEE*, Rosario M. Incandela, *Student Member, IEEE*, Jeroen P. G. van Dijk, Harald A. R. Homulle, Lin Song, Mina Shahmohammadi, *Member, IEEE*, Robert Bogdan Staszewski,*Fellow, IEEE*, Andrei Vladimirescu, *Fellow, IEEE*, Masoud Babaie, *Member, IEEE*, Fabio Sebastiano, *Senior Member, IEEE*, and Edoardo Charbon, *Fellow, IEEE - Circuits and Systems for Quantum Computing Applications*, 2018, IEEE.

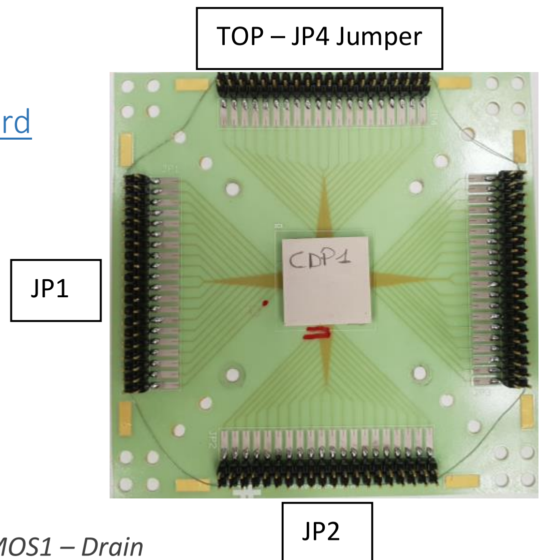
[2] Rosario M. Incandela, *Student, IEEE*, Lin Song, Harald Homulle, Edoardo Charbon, *Fellow, IEEE*, Andrei Vladimirescu, *Fellow, IEEE*, and Fabio Sebastiano, *Senior Member, IEEE - Characterization and Compact Modeling of Nanometer CMOS Transistors at Deep-Cryogenic Temperatures.*

Appendix A
- Documentation -

Documentation

Test Structure Board

Standard CMOS 65nm thick oxide – CDP1 green board

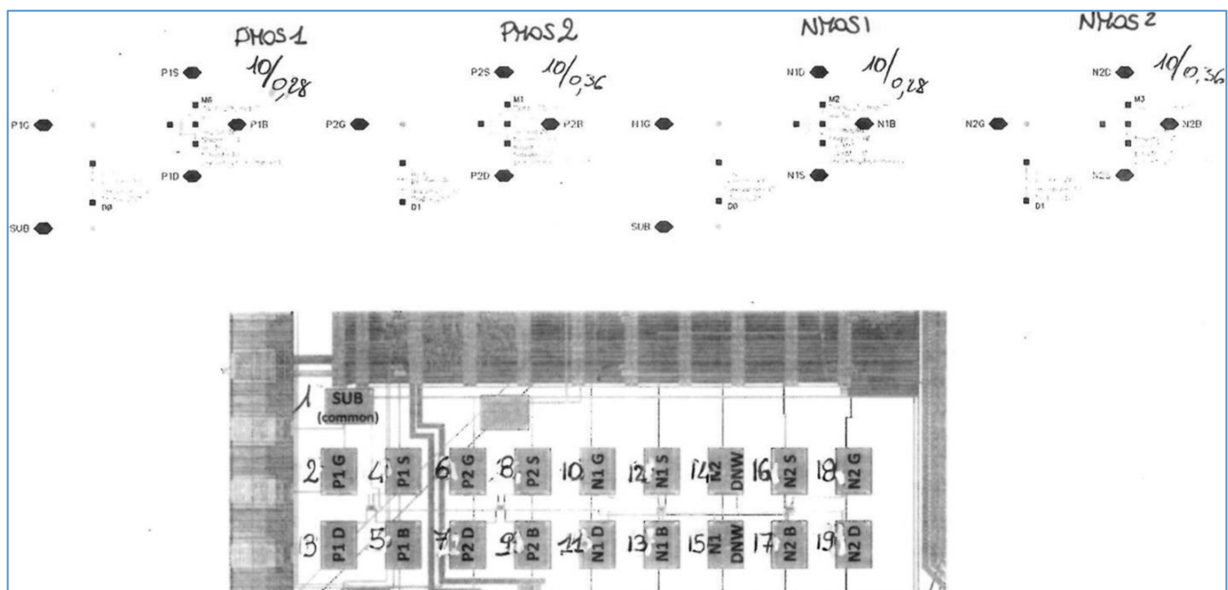


On this chip there are 4 transistor 65nm thick oxide:

- NMOS 1: W/L = 10/0.28 (µm)
- NMOS 2: W/L = 10/0.36 (µm)
- PMOS 1: W/L = 10/0.28 (µm)
- PMOS 2: W/L = 10/0.36 (µm)

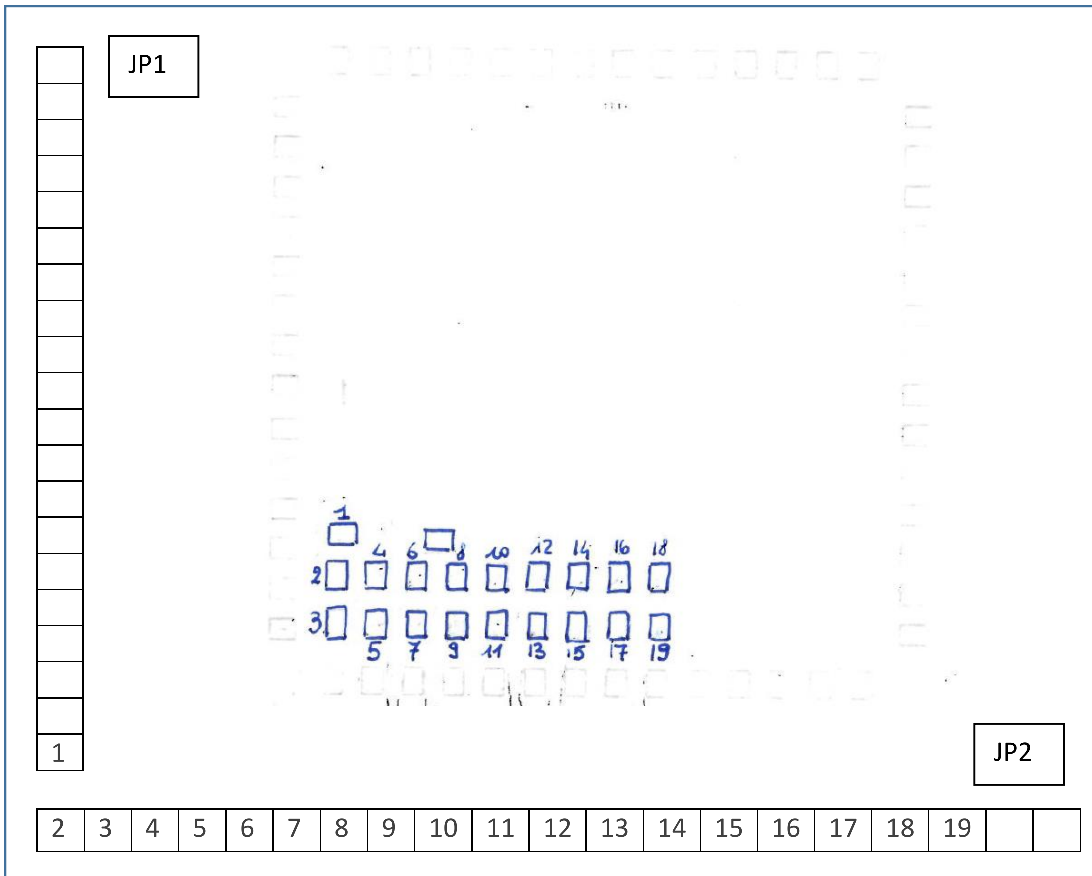
PAD LIST:

1. *SUBSTRATE p – always stuck at Vss*
2. *PMOS1 – Gate*
3. *PMOS1 – Drain*
4. *PMOS1 – Source*
5. *PMOS1 – Bulk*
6. *PMOS2 – Gate*
7. *PMOS2 – Drain*
8. *PMOS2 – Source*
9. *PMOS2 – Bulk*
10. *NMOS1 – Gate*
11. *NMOS1 – Drain*
12. *NMOS1 – Source*
13. *NMOS1 – Bulk*
14. *NMOS2 – Deep nWell – always stuck at Vdd*
15. *NMOS1 – Deep nWell – always stuck at Vdd*
16. *NMOS2 – Source*
17. *NMOS2 – Bulk*
18. *NMOS2 – Gate*
19. *NMOS2 – Drain*



WIRE BONDING:

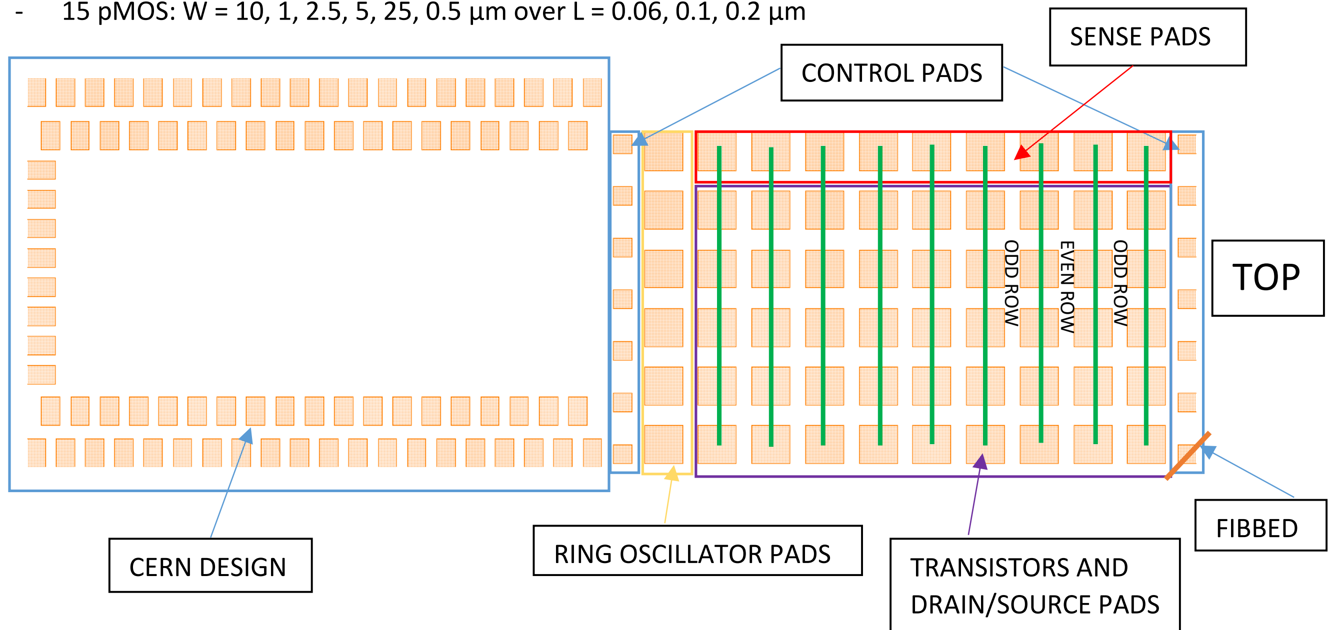
Only JP1 and JP2 are used



Standard CMOS 65nm thin oxide – Fibbed Board

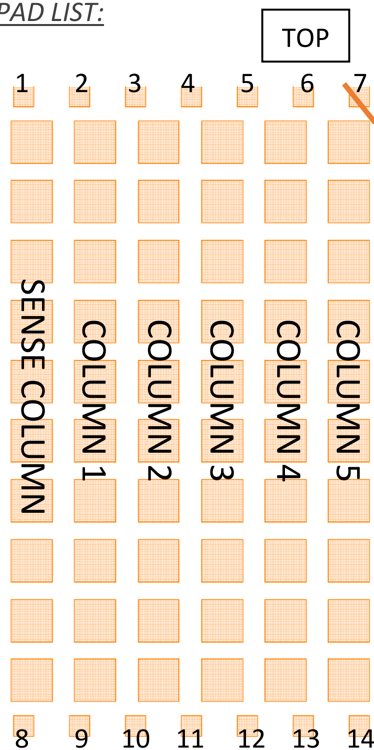
On this chip there are approximately 40 transistor 65nm thin oxide:

- 15 nMOS: W = 10, 1, 2.5, 5, 25, 0.5 µm over L = 0.06, 0.1, 0.2 µm
- 15 pMOS: W = 10, 1, 2.5, 5, 25, 0.5 µm over L = 0.06, 0.1, 0.2 µm



CERN design and Ring Oscillator have not been examined. Sense pads and source/drain pads are shorted per rows (every row) as shown by the *green* lines. Every transistor is located between two rows of pads: the pads above and below are its own source and drain. Odd rows are for nMOS, even rows for pMOS.

PAD LIST:



1. *SUBSTRATE p – always stuck at Vss/GND*
2. *PMOS nWell*
3. *PMOS Gate – Column 1*
4. *PMOS Gate – Column 2*
5. *PMOS Gate – Column 3*
6. *PMOS Gate – Column 4*
7. *PMOS Gate – Column 5*
8. *ESD- – always stuck at Vss/GND*
9. *ESD+ – always stuck at Vdd*
10. *NMOS Gate – Column 1*
11. *NMOS Gate – Column 2*
12. *NMOS Gate – Column 3*
13. *NMOS Gate – Column 4*
14. *NMOS Gate – Column 5*

TRANSISTOR LIST:

G1e G2e G3e G4e G5e CONTR

SUB GND | nWELL Vdd | GATE pMOS 1 COL | GATE pMOS 2 COL | GATE pMOS 3 COL | GATE pMOS 4 COL | GATE pMOS 5 COL

1 2 3 4 5

SENSE

odd

10/0,06 10/0,1 10/0,2 1/0,2 1/0,2

SENSE

even

10/0,06 10/0,1 10/0,2 1/0,2 1/0,2

SENSE

2,5/0,06 2,5/0,1 2,5/0,2 0,5/0,2 0,5/0,2

SENSE

2,5/0,06 2,5/0,1 2,5/0,2 0,5/0,2 0,5/0,2

SENSE

5/0,06 5/0,1 5/0,2 1/0,06 1/0,1

SENSE

5/0,06 5/0,1 5/0,2 1/0,06 1/0,1

SENSE

25/0,06 25/0,1 25/0,2 0,5/0,06 0,5/0,1

SENSE

25/0,06 25/0,1 25/0,2 0,5/0,06 0,5/0,1

SENSE

R.O.

RING 1 1µ/60n | RING 2 1µ/130n | RING 3 1µ/200n | RING 4 1µ/300n

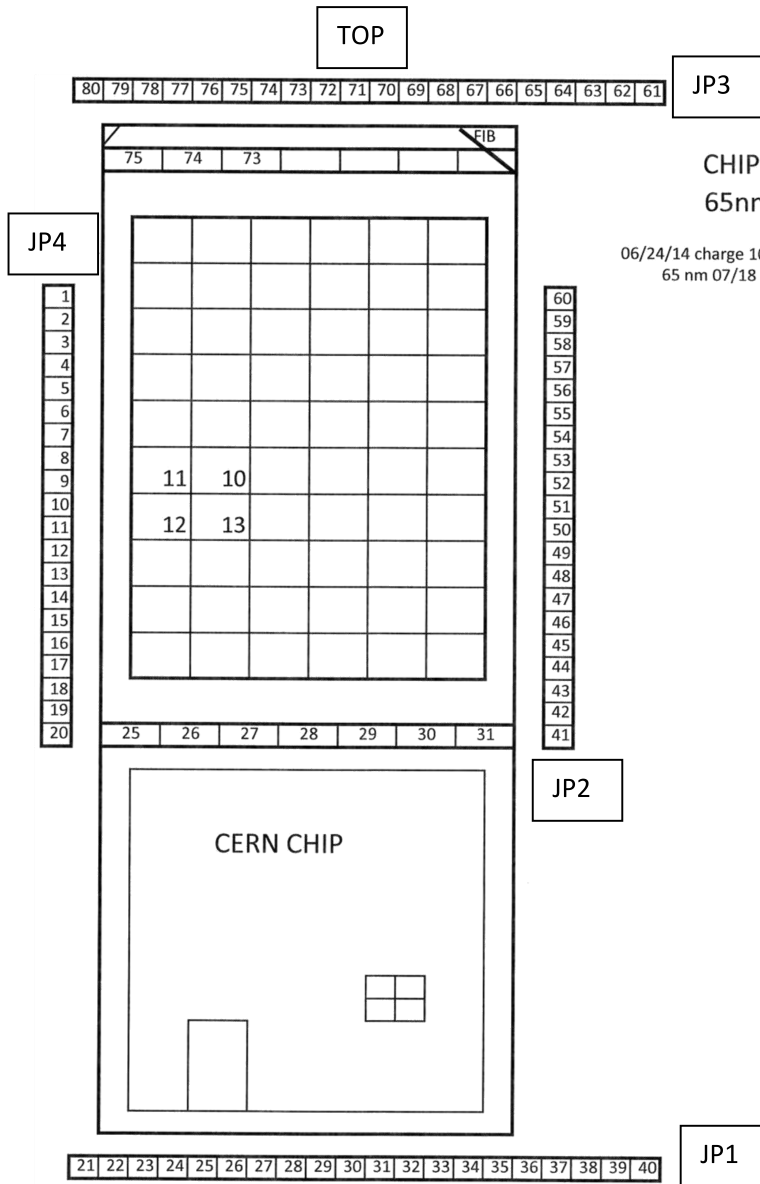
Vss | Vdd | OUT 1 | OUT 2 | OUT 3 | OUT 4

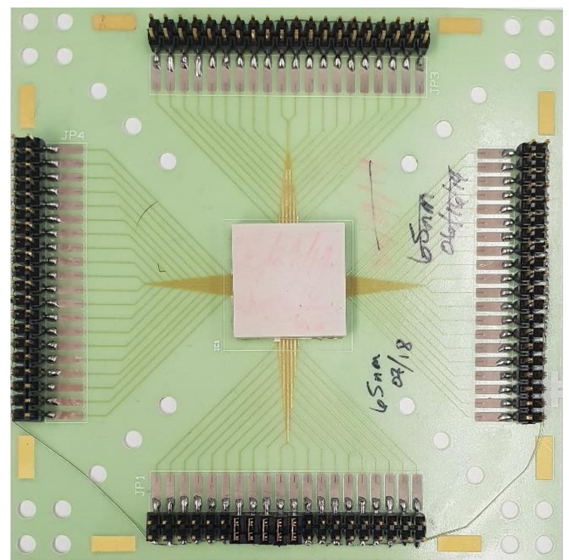
ESD- GND | ESD+ Vdd | GATE nMOS 1 COL | GATE nMOS 2 COL | GATE nMOS 3 COL | GATE nMOS 4 COL | GATE nMOS 5 COL

G1o G2o G3o G4o G5o

WIRE BONDING:

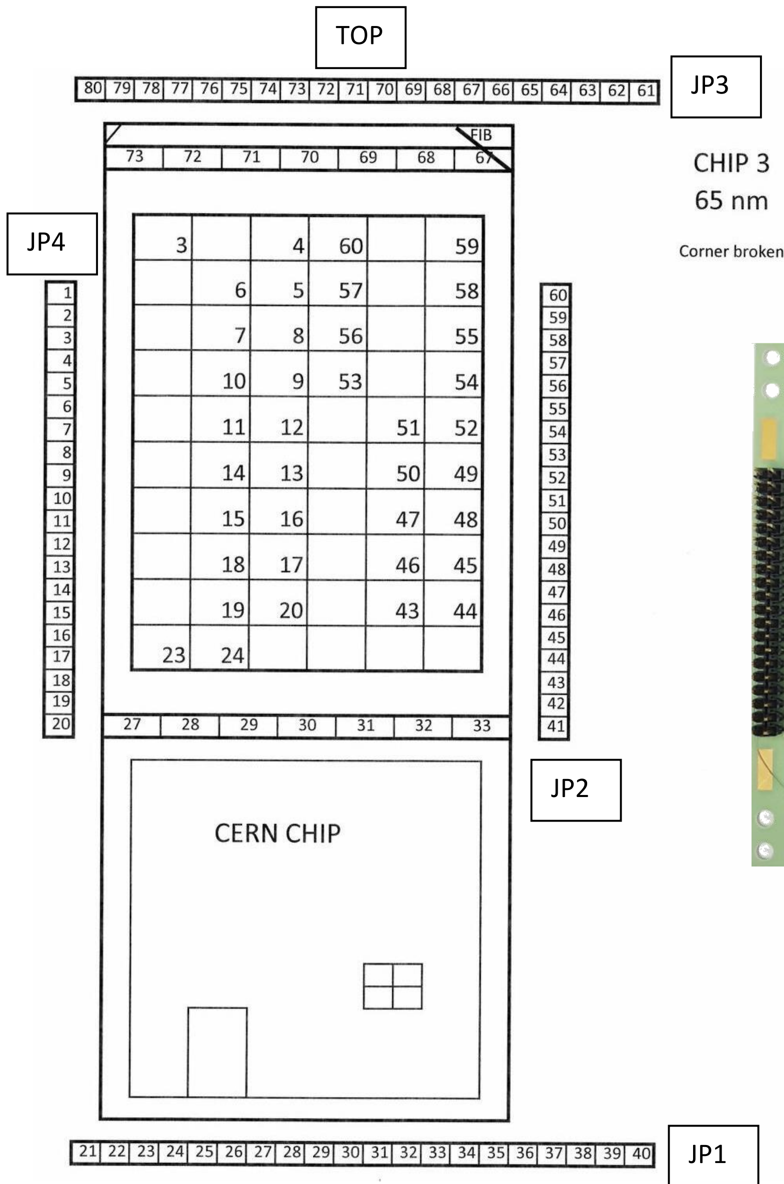
- CHIP 1 - 65nm

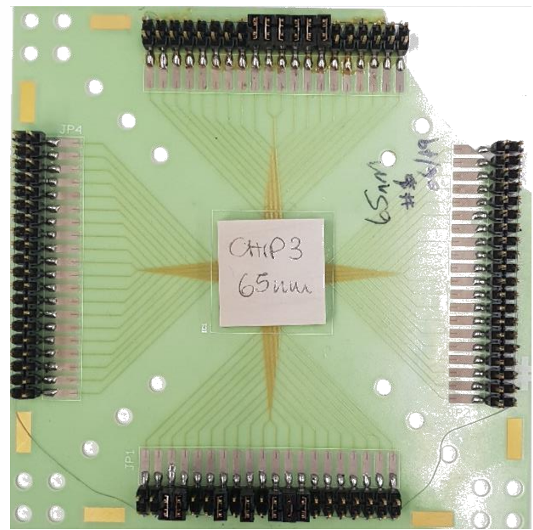




JP2 is not used. Pads and pins that have the same number are wired bonded.

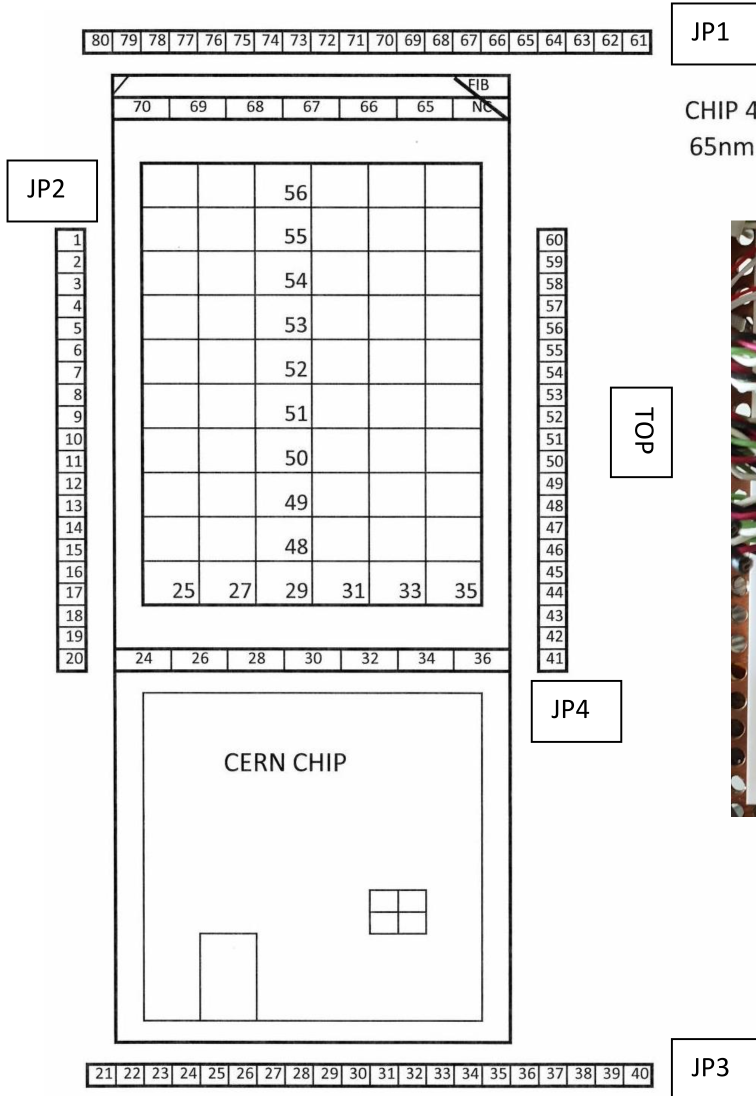
- CHIP 3 - 65nm

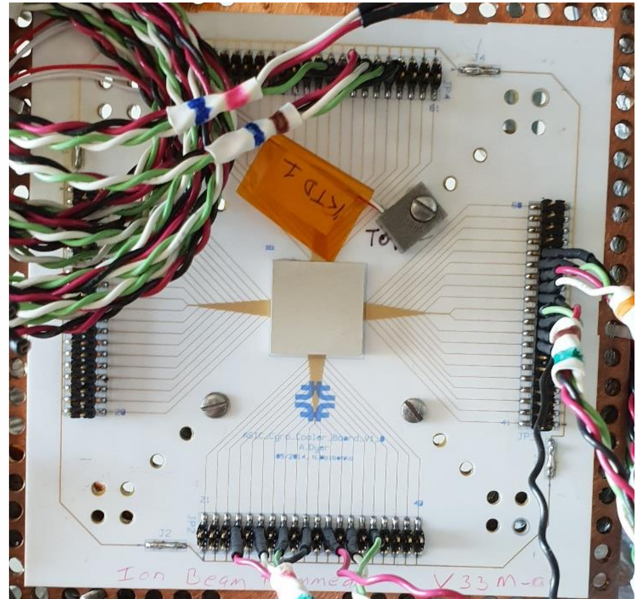




JP2 is not used. Pads and pins that have the same number are wired bonded.

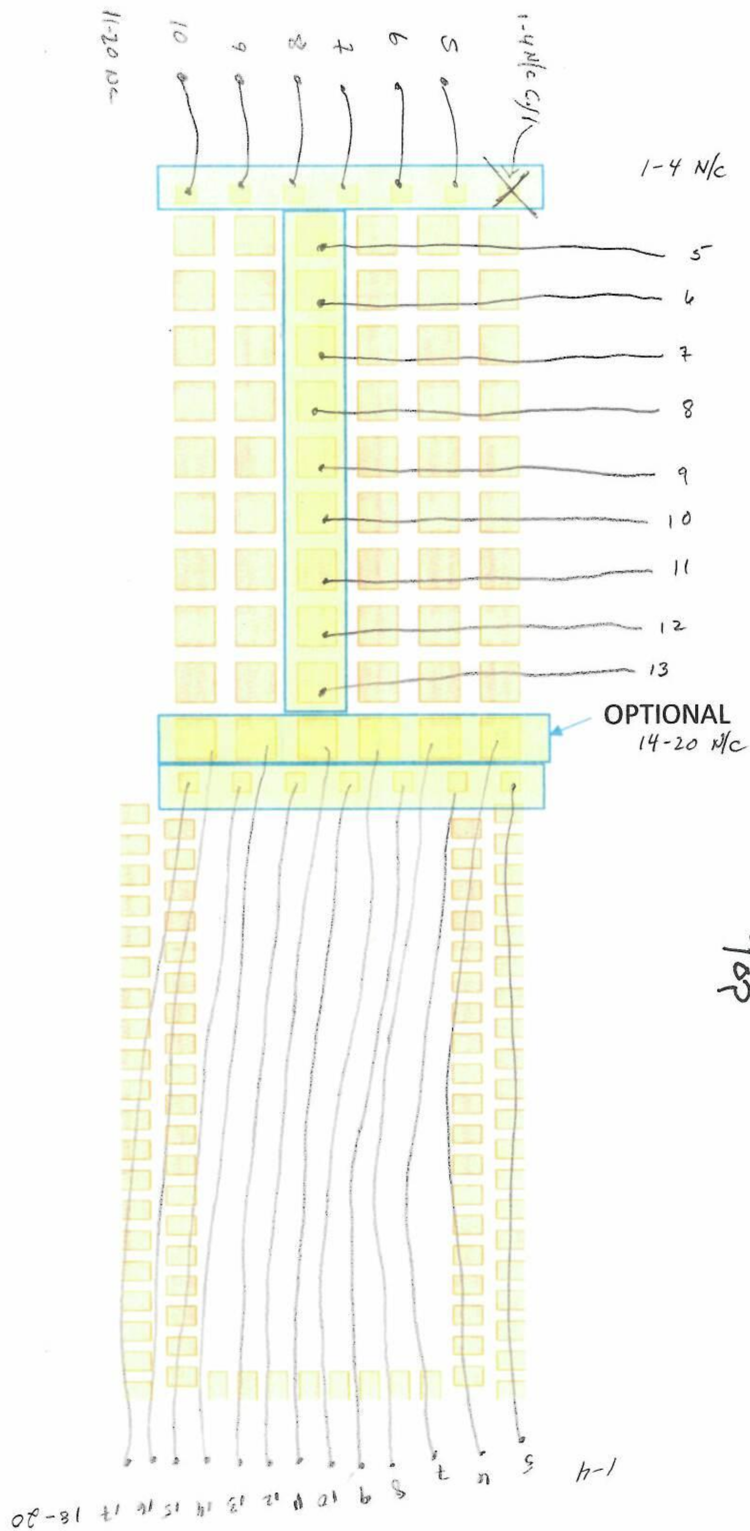
- CHIP 4 - 65nm (V33m-aa Ion Beam Trimmed)



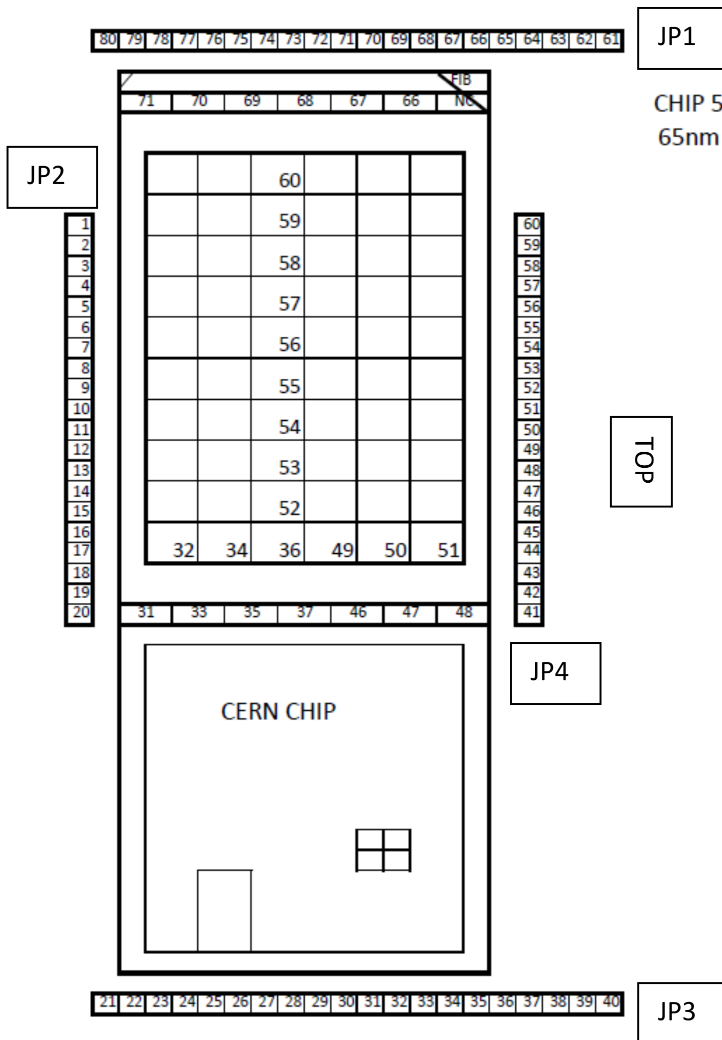


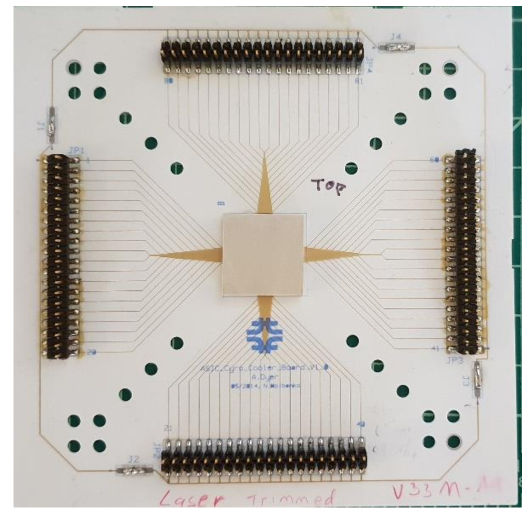
JP2 is not used. Pads and pins that have the same number are wired bonded.

WIRE-BONDING DIAGRAM:



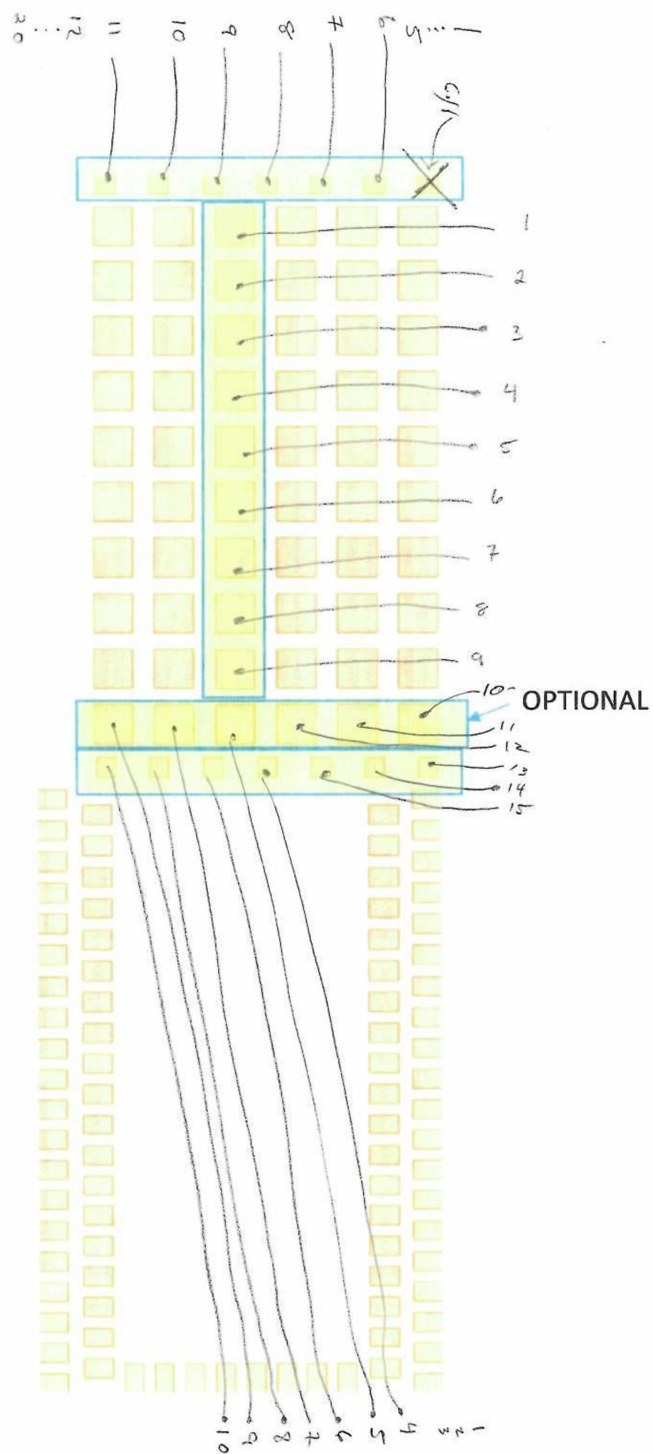
- CHIP 5 - 65nm (V33m-AA Laser Trimmed)





JP2 is not used. Pads and pins that have the same number are wired bonded.

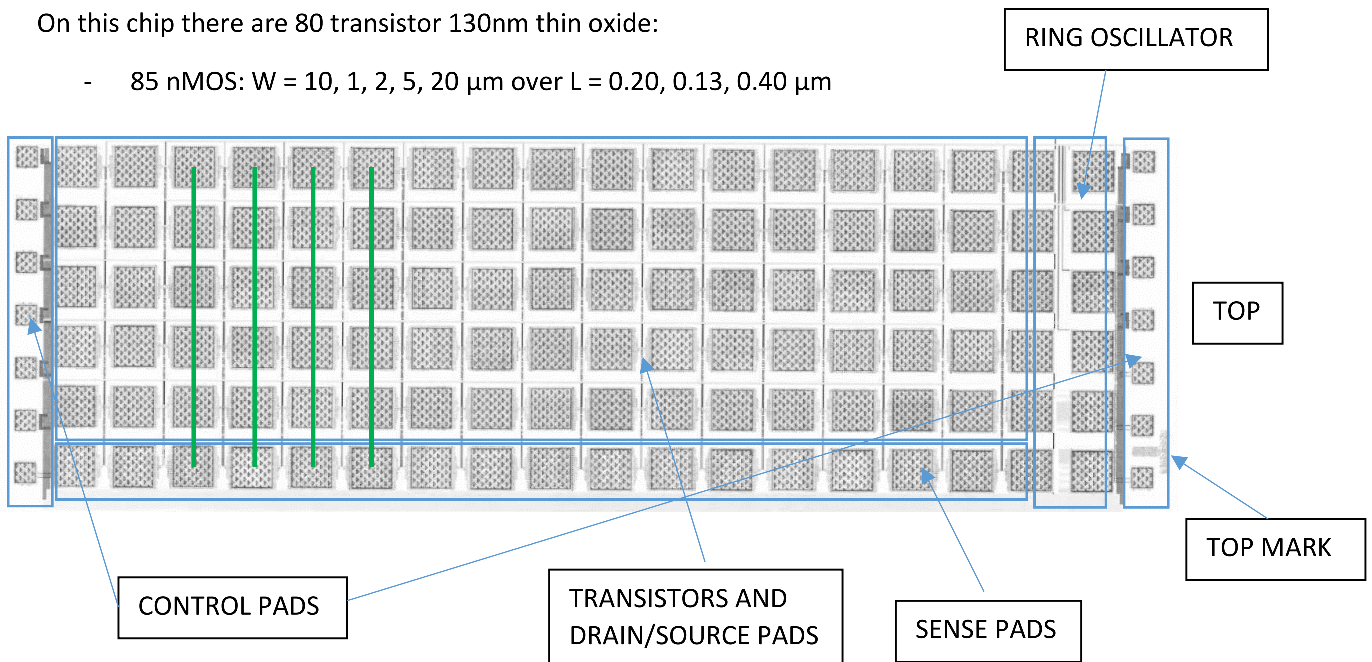
WIRE-BONDING DIAGRAM:



Standard CMOS 130nm thin oxide

On this chip there are 80 transistor 130nm thin oxide:

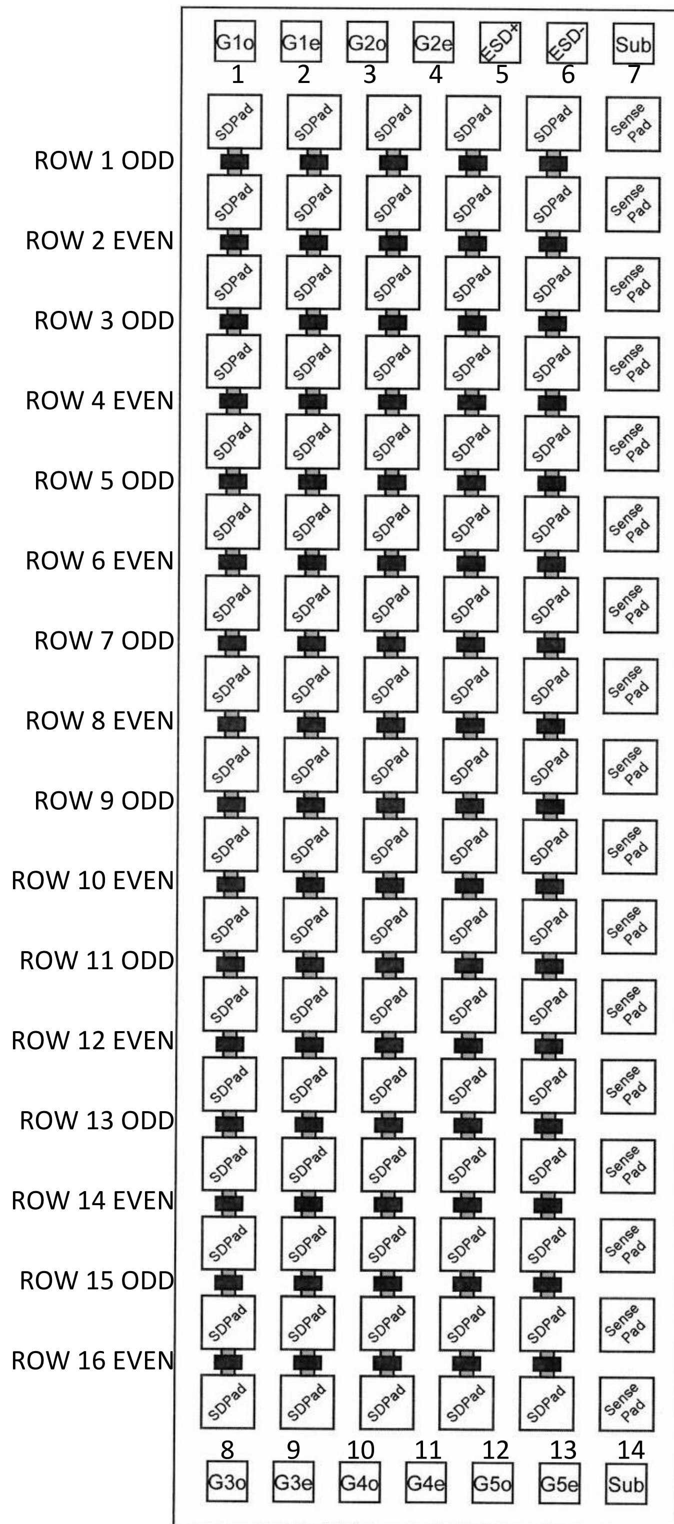
- 85 nMOS: W = 10, 1, 2, 5, 20 µm over L = 0.20, 0.13, 0.40 µm



Ring oscillator design has not been examined. Sense pads and source/drain pads are shorted per rows (every row) as shown by the *green* lines. Every transistor is located between two different rows of pads: the pads above and below are its own source and drain.

PAD LIST:

1. *Gate nMOS – Column 1, odd rows*
2. *Gate nMOS – Column 1, even rows*
3. *Gate nMOS – Column 2, odd rows*
4. *Gate nMOS – Column 2, even rows*
5. *ESD+ – always stuck at Vdd*
6. *ESD- – always stuck at Vss/GND*
7. *SUBSTRATE p – always stuck at Vss/GND*
8. *Gate nMOS – Column 3, odd rows*
9. *Gate nMOS – Column 3, even rows*
10. *Gate nMOS – Column 4, odd rows*
11. *Gate nMOS – Column 4, even rows*
12. *Gate nMOS – Column 5, odd rows*
13. *Gate nMOS – Column 5, even rows*
14. *SUBSTRATE p – always stuck at Vss/GND*



Ring oscillator row is not shown: it should be above the first row of source/drain pads.

TRANSISTOR LIST:

	L= 0.20	L= 0.13	L= 0.40	L= 0.20	L= 0.13
	RING OSCILLATOR				
ROW 1 ODD	W= 1	W= 1	W= 10	W= 10	W= 10
ROW 2 EVEN	W= 1	W= 1	W= 10	W= 10	W= 10
ROW 3 ODD	W= 1	W= 1	W= 10	W= 10	W= 10
ROW 4 EVEN	W= 1	W= 1	W= 10	W= 10	W= 10
ROW 5 ODD	W= 2	W= 2	W= 10	W= 10	W= 10
ROW 6 EVEN	W= 2	W= 2	W= 10	W= 10	W= 10
ROW 7 ODD	W= 2	W= 2	W= 10	W= 10	W= 10
ROW 8 EVEN	W= 2	W= 2	W= 10	W= 10	W= 10
ROW 9 ODD	W= 2	W= 2	W= 5	W= 5	W= 5
ROW 10 EVEN	W= 1	W= 1	W= 5	W= 5	W= 5
ROW 11 ODD	W= 1	W= 1	W= 5	W= 5	W= 5
ROW 12 EVEN	W= 1	W= 1	W= 5	W= 5	W= 5
ROW 13 ODD	W= 2	W= 2	W= 20	W= 20	W= 20
ROW 14 EVEN	W= 2	W= 2	W= 20	W= 20	W= 20
ROW 15 ODD	W= 2	W= 2	W= 20	W= 20	W= 20
ROW 16 EVEN	W= 2	W= 2	W= 20	W= 20	W= 20

L= 0.40

WIRE BONDING:

- CHIP 1 - 130nm

TOP

80	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64	63	62	61

JP1

CHIP 1
130nm

G1o	G1e	G2o	G2e	ESD+	ESD-	SUB
73	72	71	70	69	68	67

SENSE

RING

JP2

JP2: 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20

JP4: 60, 59, 58, 57, 56, 55, 54, 53, 52, 51, 50, 49, 48, 47, 46, 45, 44, 43, 42, 41

			2	1	
			3	4	
			6	5	
			7	8	
			10	9	
			11	12	
			14	13	
			15	16	
			18	17	
			19	20	

JP4

28	29	30	31	32	33	34
G3o	G3e	G4o	G4e	G5o	G5e	SUB

21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40

JP3

CHIP 1

JP4 is not used. Pads and pins that have the same number are wired bonded.

- CHIP 2 - 130nm

TOP

80	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64	63	62	61

JP1

CHIP 2
130nm

G1o	G1e	G2o	G2e	ESD+	ESD-	SUB
74	73	72	71	70	69	68

SENSE

JP2

RING

				60	59
				58	57
				56	55
				54	53
					52
					51
					50
					49
					48
				47	46
				45	44
				43	42

JP2 pins: 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20

JP4 pins: 60, 59, 58, 57, 56, 55, 54, 53, 52, 51, 50, 49, 48, 47, 46, 45, 44, 43, 42, 41

JP4

28	29	30	31	32	33	34
G3o	G3e	G4o	G4e	G5o	G5e	SUB

21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40

JP3

JP2 is not used. Pads and pins that have the same number are wired bonded.

Appendix B
- UTMOST Manual -

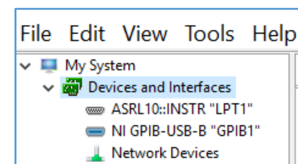
SILVACO UTMOST Manual

Prerequisites

- National Instrument – LabVIEW and NI MAX
- NI-488.2 driver for LabVIEW (http://sine.ni.com/psp/app/doc/p/id/psp-356/lang/en)
- GPIB-USB Instrument Control Device

Setup

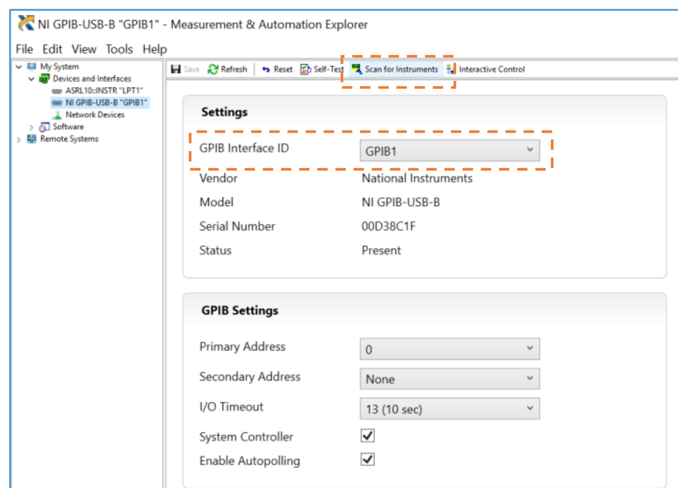
To do measurement it is necessary to connect the SMU with UTMOST through the GPIB-USB Instrument Control Device. Connect the GPIB to the SMU and plug the USB into your computer port, then turn the SMU on.



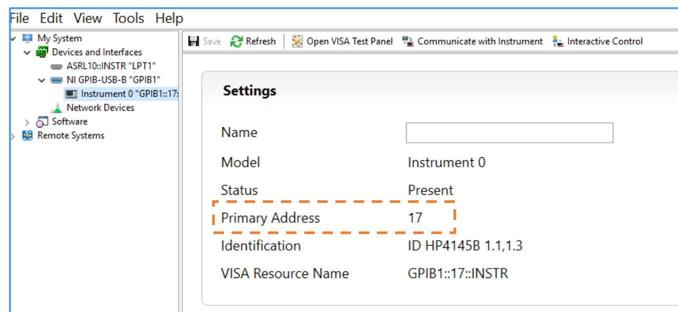
Open ***NI MAX* software** then click on **Devices and Interfaces.**
If everything is correctly connected, *NI GPIB-USB-B* should be shown. Click on it.

Be sure that *GPIB interface ID* is set on the correct name of the USB port (commonly GPIB1) otherwise change it and then click on **Save**. To check the name of the port in which the SMU is plugged in, use the *Device Manager* on your Windows.

Finally click *Scan for Instrument* on the top menu and wait until the SMU is correctly detected (*Instrument 0*).



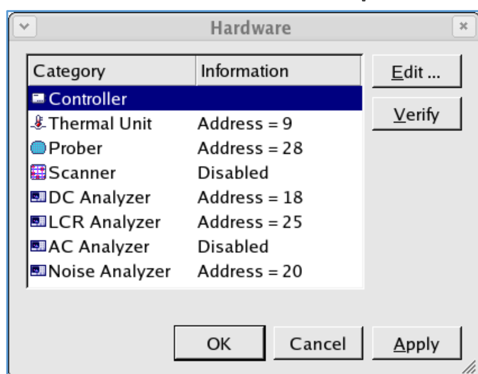
Check the primary address of the device (*17* in this case) and write it down.



Open **Silvaco UTMOST software → Acquisition Module**.

On the project menu select **Measure → Measurement** to enable the acquisition mode. In the *simulation mode* connections and external acquisition module are not enabled: the software accesses the device libraries and perform simulation. In *measurement mode* the project hardware and connections become enabled and when you run the measurement sequence the data will be generated from direct measurement of your devices. This is especially useful if you want to compare models or convert from one model type to another.

On the main menu select **Setup → Hardware → Controller → Edit → Type:** switch to NI GPIB-NI488



↳ **Port Name:** change to the name of the USB port (GPIB1 commonly)

↳ **Verify:** if there is an error, the GPIB has not been correctly configured

↳ **DC Analyzer → Edit → Enable:** switch to *True*

↳ **Address:** change to the *Primary Address* of the Instrument (17)

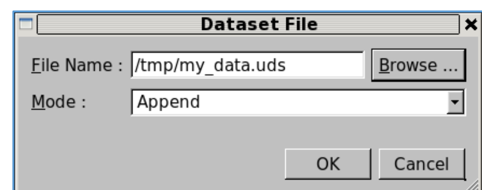
↳ **Driver File:** change to *HP4145*

↳ **Verify:** if there is an error, the GPIB has not been correctly configured

Before performing a measurement, it is necessary to save the project file and create/open the dataset. Project file contains all the instructions (hardware definition, measurement setup, device type and name) to do measurement or simulation only in the acquisition module. Dataset contains all the measurement acquired and it is valid also in the optimization module. As well as containing the measured data itself, the dataset also contains all of the information about how that measurement was performed (temperature, measurement setup applied, etc.).

To Save the project, click on **File → Save As.**
To open a project **File → Open**.

To open a dataset, click on **File → Dataset File → Browse:** select the correct path of the file.
If you want to create a new file, just add manually the name of your personal dataset (.uds) at the end of the path and it will be automatically generated.



If you set **Mode → Append** you will be able to add data to the file, but not edit or overwrite any data which are already present

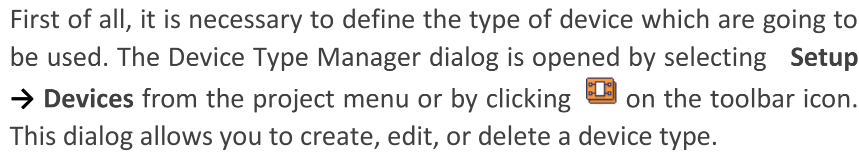
↳ **Modify** you can edit and overwrite all datasets in the file

To view or edit your datasets settings, click on **Dataset → Edit**.

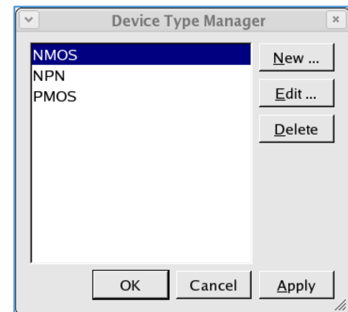
ACHTUNG: often (always) the project files and datasets are not correctly generated. The software does not automatically set the correct extension of them which should be .prj (for project) and .uds (for dataset). For this reason, while browsing the path, files are not listed. To find them, just set 'All File' in the file type menu or change manually the extension.

Performing Measurements

Device Type Manager

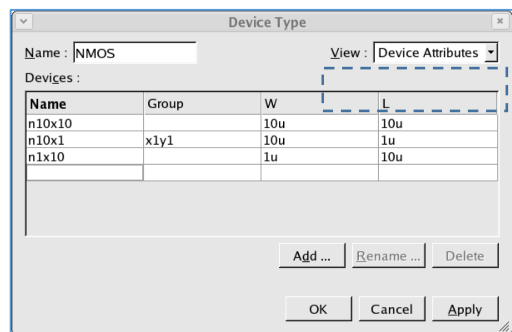


First of all, it is necessary to define the type of device which are going to be used. The Device Type Manager dialog is opened by selecting **Setup → Devices** from the project menu or by clicking on the toolbar icon. This dialog allows you to create, edit, or delete a device type.

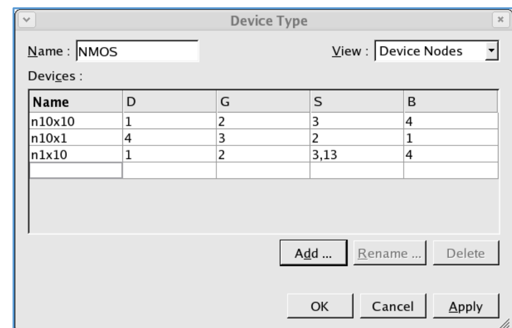


Creating or adding a device type will open up the device type editor dialog. This dialog allows you to enter any number of devices within this device type.

A device to be measured is described by its name, nodes, and attributes. Additionally, if the datasets are to be acquired using simulation, a simulation netlist can be defined for this device type. There are three views that can be selected in the device editor dialog. These are the **Device Attributes**, the **Device Nodes**, and the **Netlist Text**.

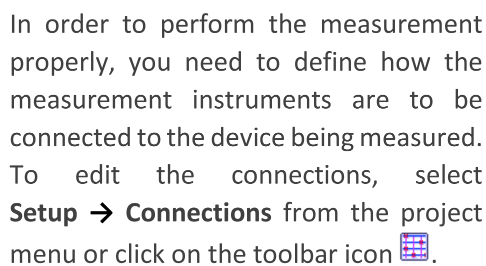


When you view the **Device Nodes**, you can add, rename, or delete the nodes for this device. You can also add any number of devices to the device type and for these devices you must specify the scanner pins to which the nodes are connected.

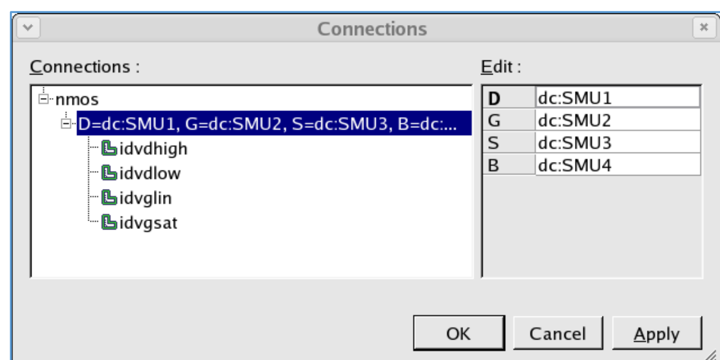


Connections

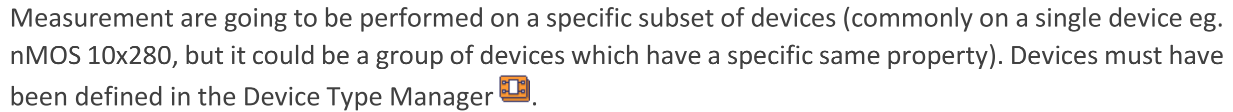
As soon as a device is defined, the connection definition gets available.



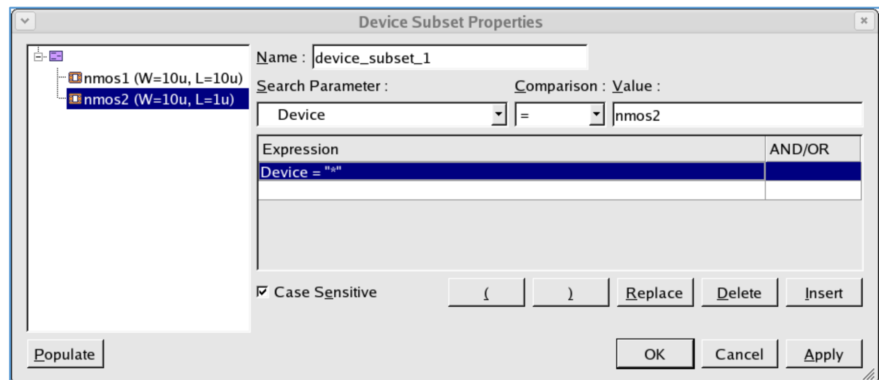
In order to perform the measurement properly, you need to define how the measurement instruments are to be connected to the device being measured. To edit the connections, select **Setup → Connections** from the project menu or click on the toolbar icon.

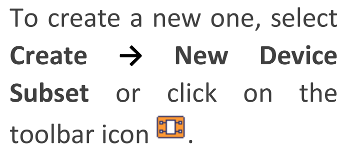


Device Subset

Measurement are going to be performed on a specific subset of devices (commonly on a single device eg. nMOS 10x280, but it could be a group of devices which have a specific same property). Devices must have been defined in the Device Type Manager .

To modify an existing device subset, double-click on it or select it and then select **Edit → Properties** from the menu.



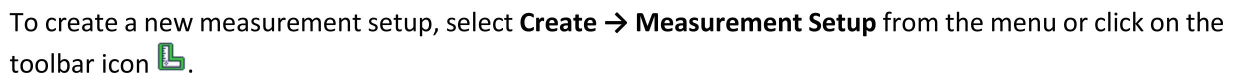
To create a new one, select **Create → New Device Subset** or click on the toolbar icon .

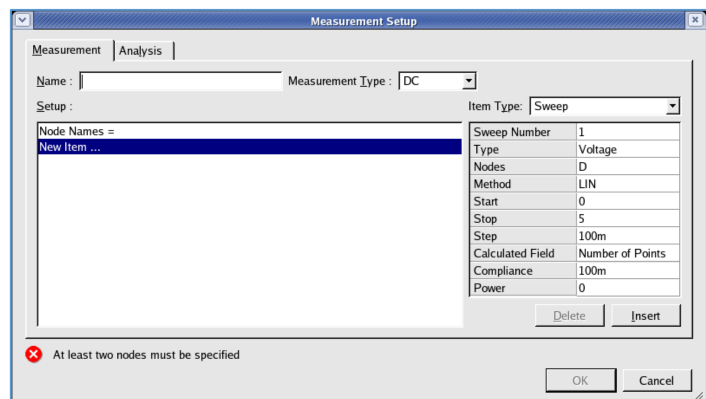
Select the name of the Subset (commonly the same name of the device you want to use). Insert the properties of your device (length, name, etc.): they will act like a filter. Automatically the software will consider only the devices (which are listed on the left) that match those properties and discard the other. Commonly you want to create a single subset for every device: to match the subset to a single device just click on the device listed on the left, click **Populate** and then **Insert**. All the others will be discarded.

Measurement Setup

At the end it is necessary to define every single type of measurement to perform on devices. Measurement setup is independent from device subsets: hypothetically a single measure could be applied to every subset if compatible (type of nodes).

To modify an existing setup, double-click on it or select it and select **Edit → Properties** from the menu.

To create a new measurement setup, select **Create → Measurement Setup** from the menu or click on the toolbar icon .

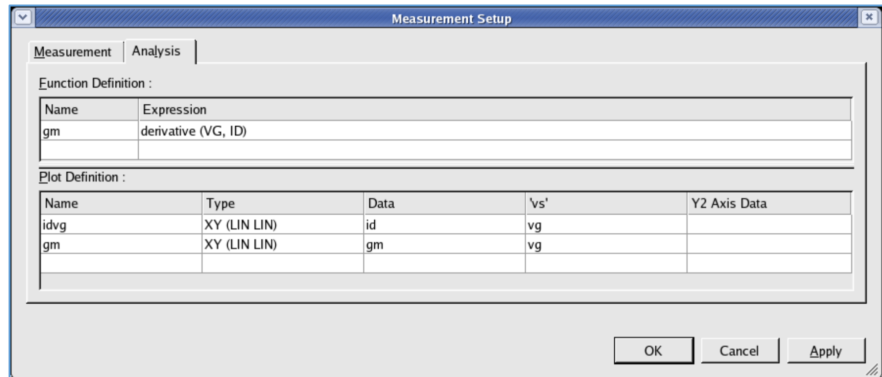


Insert a unique Measurement Setup name. Then click on *Node Names* and insert all the device nodes (eg. *S* – enter – *B* – enter – *D* – and so on), then click on *New Item*. On *New Item* you can define sweeps, constants and targets of your measurement. As you have defined an item, click **Insert** and then *New Item* again to add a new one.

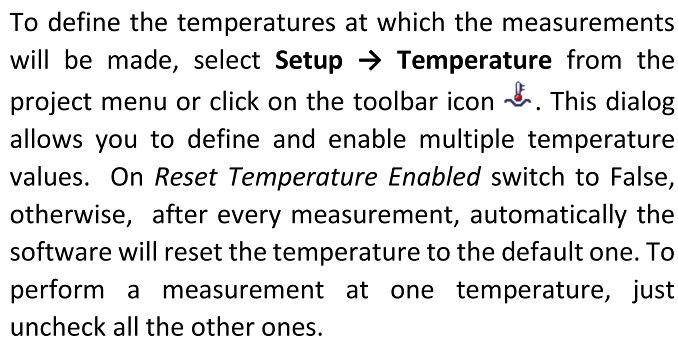
Tips:

- Primary Sweep should have 1 as *Sweep Number*
- Start point has to have a lower value than Stop point
- There must always be at least one target (eg. drain current)

At the end click on **Analysis** to define function (if necessary) and plot settings.

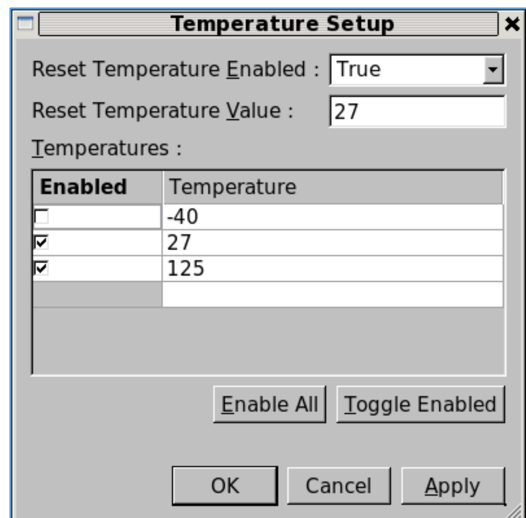


Defining Temperature



To define the temperatures at which the measurements will be made, select **Setup → Temperature** from the project menu or click on the toolbar icon . This dialog allows you to define and enable multiple temperature values. On *Reset Temperature Enabled* switch to False, otherwise, after every measurement, automatically the software will reset the temperature to the default one. To perform a measurement at one temperature, just uncheck all the other ones.

ACHTUNG: all temperatures are in CELSIUS.

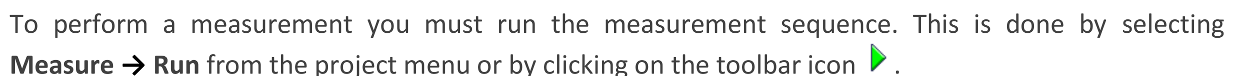


Performing Measurements

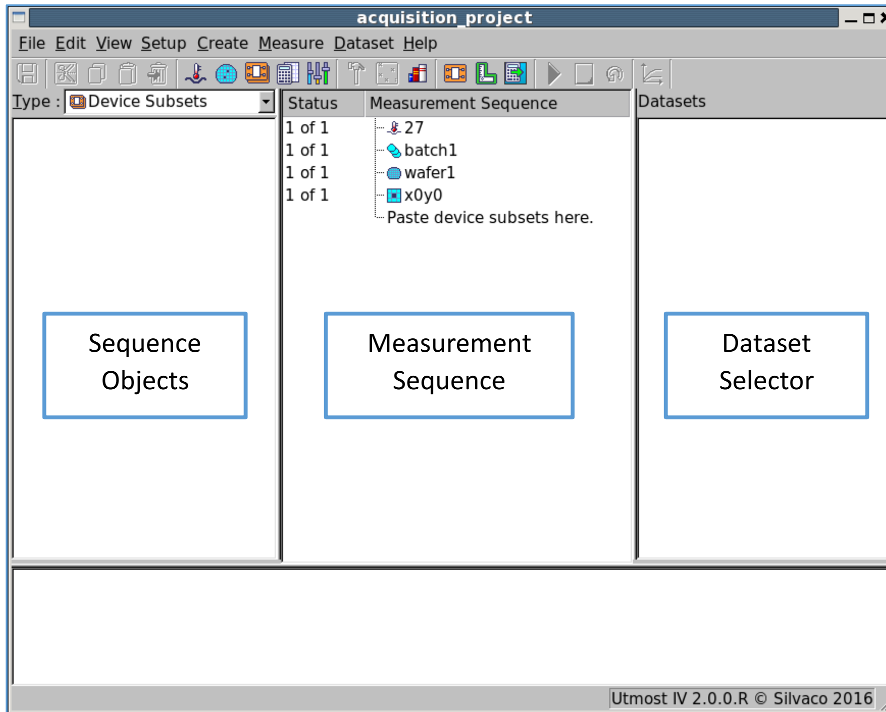
Before running a measurement it is necessary to link the device subset to the correct measurement setup.

On the left side of the display there is the *Sequence Objects* where are shown all the device subsets or (changing the type) all the measurement setups previously defined.

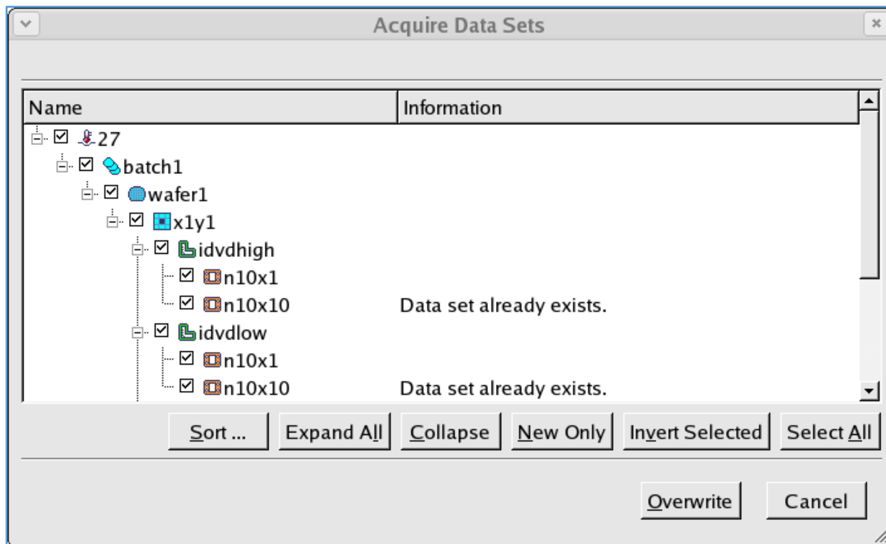
To perform a measurement, click on the correct device subset in the *Sequence Object* area and drag it into the *Measurement Sequence*. Then do the same with the measurement setup: release it on the device subset you want to couple with.



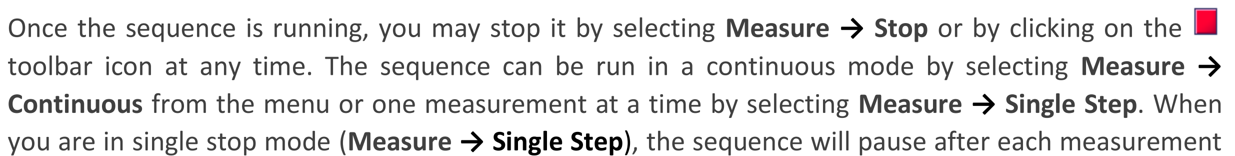
To perform a measurement you must run the measurement sequence. This is done by selecting **Measure → Run** from the project menu or by clicking on the toolbar icon .



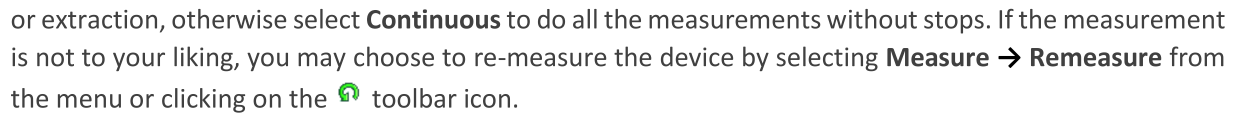
When you run the sequence from idle, the following dialog will be opened.



This allows you to select exactly which datasets you wish to measure and clearly shows if any datasets will be overwritten when the measurement is performed.



Once the sequence is running, you may stop it by selecting **Measure → Stop** or by clicking on the toolbar icon at any time. The sequence can be run in a continuous mode by selecting **Measure → Continuous** from the menu or one measurement at a time by selecting **Measure → Single Step**. When you are in single stop mode (**Measure → Single Step**), the sequence will pause after each measurement



or extraction, otherwise select **Continuous** to do all the measurements without stops. If the measurement is not to your liking, you may choose to re-measure the device by selecting **Measure → Remeasure** from the menu or clicking on the toolbar icon.

On the right side of the display there is the *Selector Dataset* area where are displayed all the measurements already acquired. To plot one, just toggle it (only one), right-click and then **Plot**.