A Digital Hadronic Calorimeter
with a new readout generation

CIEMAT, IHEP, IPNL, LAL, LAPP, LLR

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OUTLINE

• Motivation for ILC-like DHCAL
• Detectors
• 4-chip project
• 1 m² project
• Perspectives
Motivations

Analog and Digital HCAL studies are followed within the CALICE collaboration in order to choose the best hcal for future ILC experiments.

Why the digital solution?
Going from analog readout to 1:2-bit readout electronics:
• One can increase detector granularity and hence PFA performance while reducing cost.
• Cheap, robust detectors suitable for the digital version exist and are very attractive: GRPC, μMEGAS, GEM…

Does the digital option mean energy measurement degradation?
Simulation

Digital-1bit

Analog

σ/mean ~22%

Landau Tails + path length

σ/mean ~19%

Gaussian

π⁺ 5GeV

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E dep

E pion (GeV)

Nhits

E pion (GeV)

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Number of hits
• **1-bit digital** solution is better at **low energy**
• **Analog solution** is favored at **high energy** due to high number of particles in the central region.

**But what about the readout with 2 bits solution?**

The study of KEK group for the GLD HCAL using: 2-bit, 3 thresholds (0.5, 10, 100 MIPs) associated to \(1 \times 1 \text{ cm}^2\) tile size shows:

**Similar energy resolution with respect to the analog readout version for single particle at HE**
Comparison of Energy Resolutions

\[ \frac{\sigma}{E} = \sqrt{\frac{\sigma_{\text{stochastic}}^2}{E} + \sigma_{\text{constant}}^2} \]

- Analog: \( \sigma_{\text{sto}} = 48.9 \pm 0.6 \% \)
  \( \sigma_{\text{con}} = 5.0 \pm 0.2 \% \)
- Digital: \( \sigma_{\text{sto}} = 37.0 \pm 0.9 \% \)
  \( \sigma_{\text{con}} = 13.8 \pm 0.2 \% \)
- Semi: \( \sigma_{\text{sto}} = 45.1 \pm 0.6 \% \)
  \( \sigma_{\text{con}} = 6.8 \pm 0.1 \% \)
- Real data (analog):
  \( \sigma_{\text{sto}} = 46.7 \pm 0.6 \% \)
  \( \sigma_{\text{con}} = 0.9 \pm 0.9 \% \)

Digital: 0.5MIP
Semi-digital: 0.5, 10, 100 MIP
Tile size: 1cm \times 1cm


courtesy H. Matsunaga
• 1-bit digital solution is better at low energy
• Analog solution is favored at high energy due to number of particles in the central region.

But what about the 2-bit readout solution? The study of KEK group for the GLD HCAL using: 2-bit, 3 thresholds (0.5, 10, 100 MIPs) associated to $1 \times 1$ cm$^2$ tile size shows:

• Similar energy resolution with respect to the analog readout version for single particle at HE
• Better energy resolution for JETs
Jet Energy Resolution

- $e^+e^- \rightarrow qq \ (u/d/s)$
  - $\sqrt{s} = 91, 350, 500 \text{ GeV}$
- Energy measurement with (perfect) PFA
- In case of $1 \times 1 \text{ cm}^2$ tile size, digital calorimeter achieved similar or slightly better jet energy resolution

courtesy H. Matsunaga
Two efforts are followed in parallel to have high-granularity compact DHCAL:

**USA**: using GRPC/GEM with binary readout (1 bit) → Physics Prototype

**Europe**: using GRPC/MICROMEGAS with semi-digital readout and ILC-like features → Technological Prototype with the following guideline:

*• DHCAL as compact and as hermetic as possible*
Detectors for the DHCAL

Gas detectors:
Thickness of few millimeters

GRPC:
Robust but limited detection rate

µMEGAS, GEM:
delicate but high rate
Detector dimensions:
GRPC: 8×8, 32×8, 50×32, 100×32, 100×100 1cm²-pad: already produced and tested.

µMEGAS: 16×6, 32×8, 32×12 1cm² produced and tested. Larger size detectors are under development.

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The challenge:
How to have a detector of few thousands m² fully equipped with low consumption semi-digital readout and still very compact !!!!?
Embedded Daisy-chained electronics is the solution
4-Chip project
Aim: Validate the new electronics/acquisition scheme for DHCAL

- 8×32 pads detector (GRPC and μMEGAS)
- 8-layer PCB
- 4 chips (64 ch)
- Readout USB + FPGA
HARDROC

- 64 channels, 16mm²
- Digital/analog output.
- 2 thresholds (3 very soon)
- Low consumption, power pulsing (< 10 µW/ch)
- Digital memory able to store up to 128 evts.
- Large gain range
- Xtalk <2%
- Adequate for GRPC* (threshold > 10 fc)

*For µMEGAS another ASIC is developed in Lyon with a threshold as low as 3 fc
HARDROC: Scurves of 64 channels

Before Gain correction

After Gain correction

30 fC

10 fC

Piedestal
8-layer PCB

- TOP
- GND
- DIGITAL SIGNAL
- POWER
- ANALOG SIGNAL
- ANALOG SIGNAL
- GND
- BOTTOM

Through via  Blind via  Buried via
- 8-layer PCB, 800 µ thick
- 8×32 pads of 1 cm² and 500 µ separation

X-talk (<0.3 %)
Readout system

The 4 chips are *daisy-chained* and connected to a *FPGA* communicating with a pc through a *USB* device.

Firmware + Software were developed to allow charging the slow control parameters from *file/flux* and controlling the procedure.

Acquisition modes: different modes are allowed:

a) Internal triggers
b) External triggers: *cosmics* & *test beam*

Data output: The two kinds of data output of the hardroc chips are accessible: *digital* and *analog*
Assembled (IPNL)

Readout software (LLR)

First Daisy chain measurement
* Two thresholds

* Gain value of each channel can be chosen in [0-63]

Calibration is done automatically for all channels by injecting charge through internal capacitors
Slice test

On the test bench with GRPC
Example of a recorded mip
First results

**Graph**

- **Threshold**: \( \approx 100 \text{ fc} \)
- **GRPC**: 32\( \times \)8 pads
- **RP**: graphite
- **Mix**: TFE 93%, Isobutene 5%, SF6 2%

**Preliminary**

- Efficiency

**No gain corr.**

**Multiplicity**

- No gain corr.
First results

GRPC 32×8 pads
RP: licron

Threshold ≈ 100 fc

TFE  93%
Isobutene  5%
SF6    2%

preliminary

no gain corr.
Gain correction is ongoing for the different boards

before

\[ \sigma = 6.1 \text{ DAQ} = 15.25 \text{ fc} \]

after

\[ \sigma = 2.0 \text{ DAQ} = 5 \text{ fc} \]
Analog readout was recently integrated and will be used to choose the thresholds adequately.

Amplitude of the signal injected in one of the 64 channels of each of the 4 ASICs through internal capacitors.
Final confirmation of the success of our electronic readout system will be coming soon with the beam tests with 5 fully equipped detectors (32×8 pads each):

10-17 July :  
beam test@ps-cern
3-11 August :  
beam test@sps-cern

To study:
* Efficiency and multiplicity  
  vs:angle, position, particle multiplicity
* but also the first phase of the Hadronic shower
DIF is already designed and sent to fabrication
ASU hosting 24 hardroc chips is already designed
Connection between the different ASU is under study: signal transmission + mechanics (IPNL + CIEMAT)
Perspectives
A technological prototype ILC-module0 to be built before 2010

The technological prototype optimization is going on to optimize the design.
Conclusions

A digital hadronic calorimeter with semi-digital readout is very promising candidate for future colliders experiments.

A slice test based on the semi-digital readout was successfully tested in a laboratory cosmic bench.

A beam test is scheduled next months at CERN.

1 m² project is ongoing and the first plane is expected before the end of 2008.

A technological prototype is funded and expected in 2009-2010.
Back up
Energy Resolution

Segmentation dependence

Threshold: 0.5MIP

$\frac{\sigma_E}{E}(\%)$ vs $\frac{1}{\sqrt{E}}$ (GeV$^{-1/2}$)

- Smaller size is better in high energy region

Threshold dependence

Tile size: 1cm×1cm

→ No significant difference
HARDROC Power pulsing

PWR ON: ILC like (1ms,199ms)

DAC output (Vth)
New chip

A new chip with a low threshold for \( \mu \text{MEGAS} \)
is under development @IPNL

3 DACs (8 bits each)
BCID = 12 bits
memory depth = 8 ev.

64-ch chip
CMOS tech
power pulsed

Simple geometry

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The chip was designed and produced. A test board using OPERA DAQ developed @IPNL was used.

First results:
Mode $\mu$MEGAS
0.8 fc/DAQ
Resolution < 2.5 fc

Tests and improvement are going on