A Digital Hadronic Calorimeter

with a new readout generation

CIEMAT,IHEP,IPNL,LAL,LAPP,LLR

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IPN-Lyon

OUTLINE

- Motivation for ILC-like DHCAL
- Detectors
- 4-chip project
- 1 m^2 project
- Perspectives

Motivations

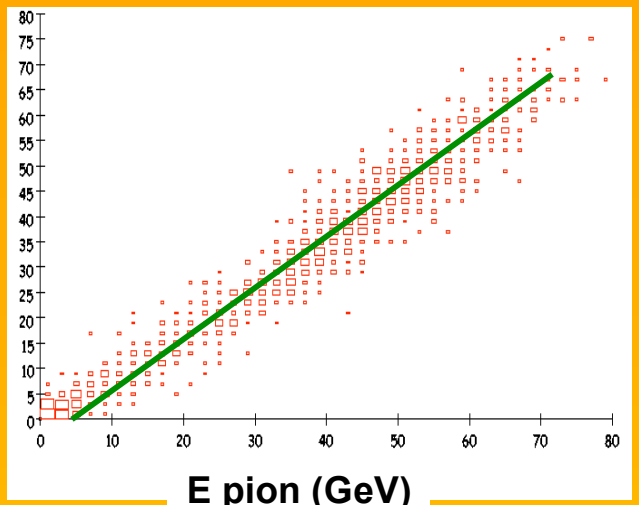
Analog and Digital HCAL studies are followed within the **CALICE** collaboration in order to choose the best hcal for future ILC experiments.

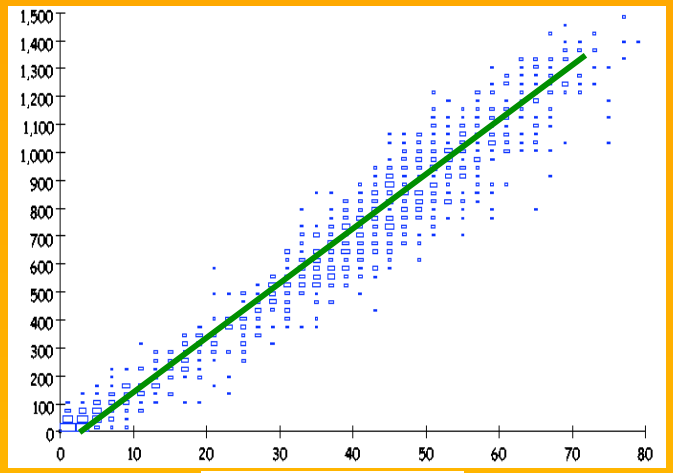
Why the digital solution?

Going from analog readout to 1:2-bit readout electronics:

- One can increase detector granularity and hence PFA performance while reducing cost.
- **Cheap**, robust detectors suitable for the digital version exist and are very attractive: GRPC, µMEGAS, GEM…

Does the digital option mean energy measurement degradation?



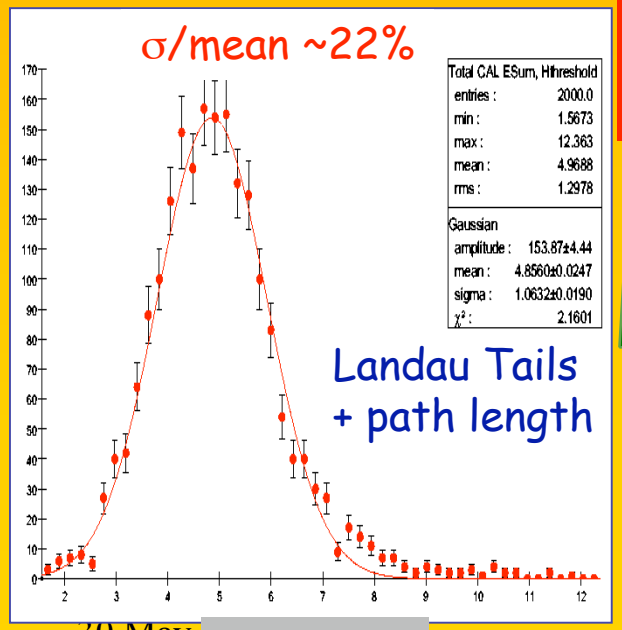


Analog

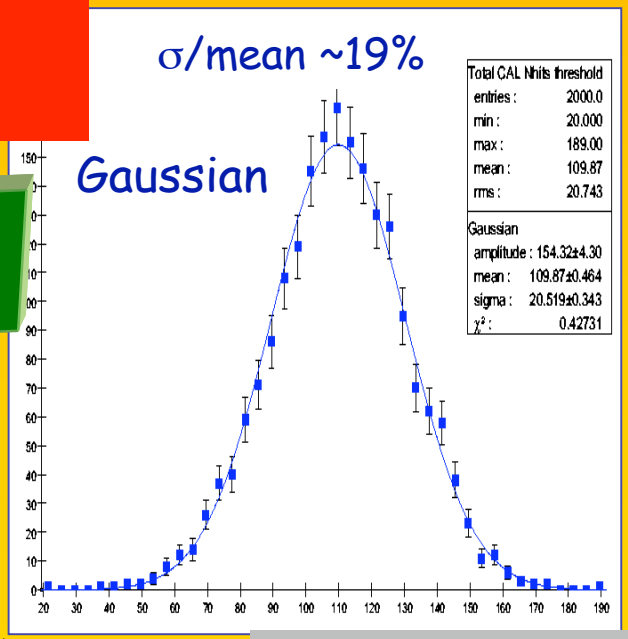
Simulation

calice

Digital-1bit



π^+ 5GeV



- 1-bit digital solution is better at low energy
- Analog solution is favored at high energy

due to high number of particles in the central region.

But what about the readout with 2 bits solution?

The study of KEK group for the GLD HCAL using :

2-bit, 3 thresholds (.5, 10, 100 MIPs) associated to

1×1 cm² tile size shows :

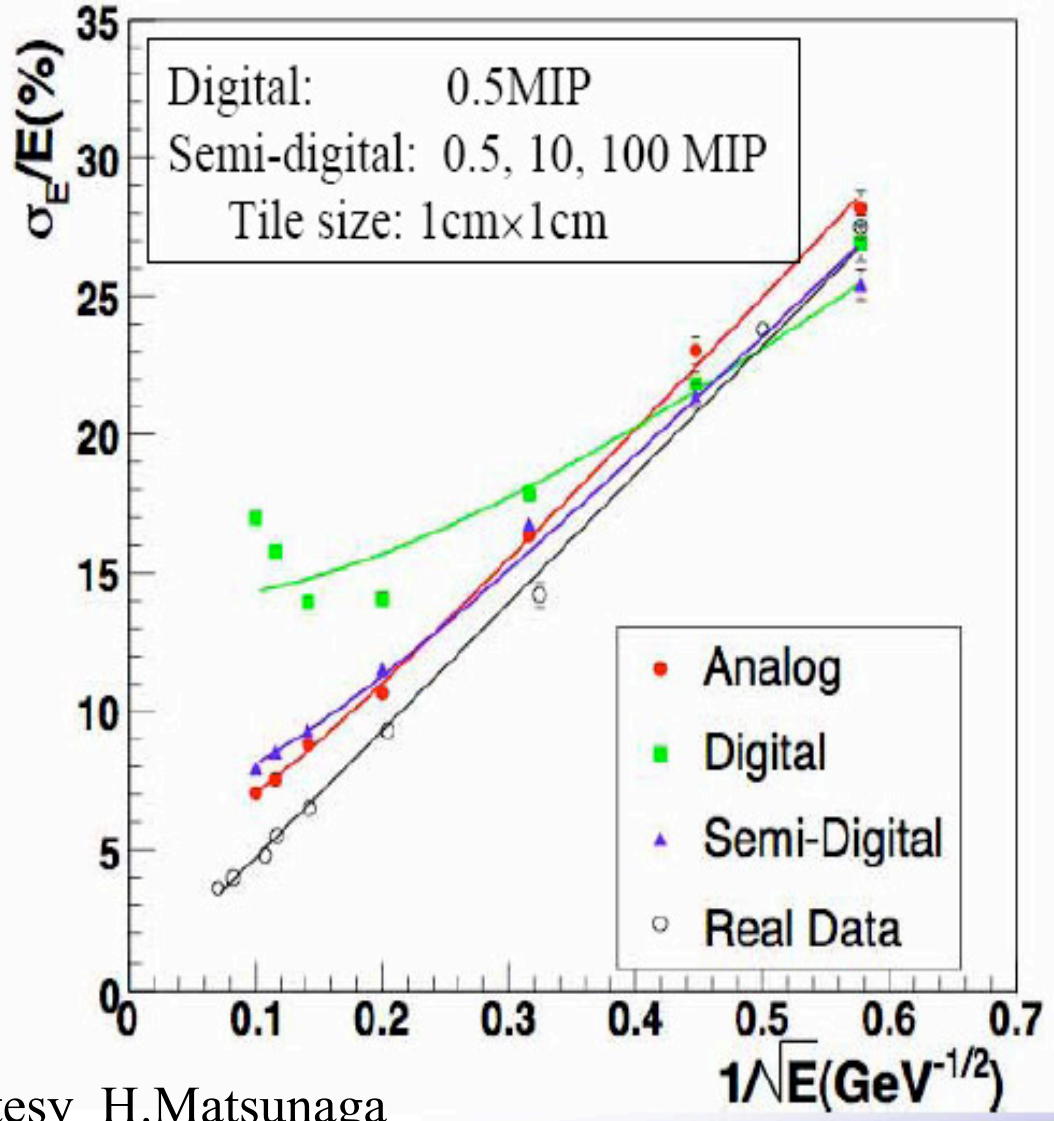
Similar energy resolution with respect to the analog readout version for single particle at HE

Comparison of Energy Resolutions

$$\frac{\sigma}{E} = \sqrt{\frac{\sigma_{stochastic}^{2}}{E} + \sigma_{constant}^{2}}$$

- Analog : $\sigma_{sto} = 48.9 \pm 0.6$ %
  $\sigma_{con} = 5.0 \pm 0.2$%
- Digital : $\sigma_{sto} = 37.0 \pm 0.9$%
  $\sigma_{con} = 13.8 \pm 0.2$%
- Semi : $\sigma_{sto} = 45.1 \pm 0.6$%
  $\sigma_{con} = 6.8 \pm 0.1$%
- Real data (analog) :
  $\sigma_{sto} = 46.7 \pm 0.6$%
  $\sigma_{con} = 0.9 \pm 0.9$%

NIM A 487 (2002) 291



courtesy H.Matsunaga

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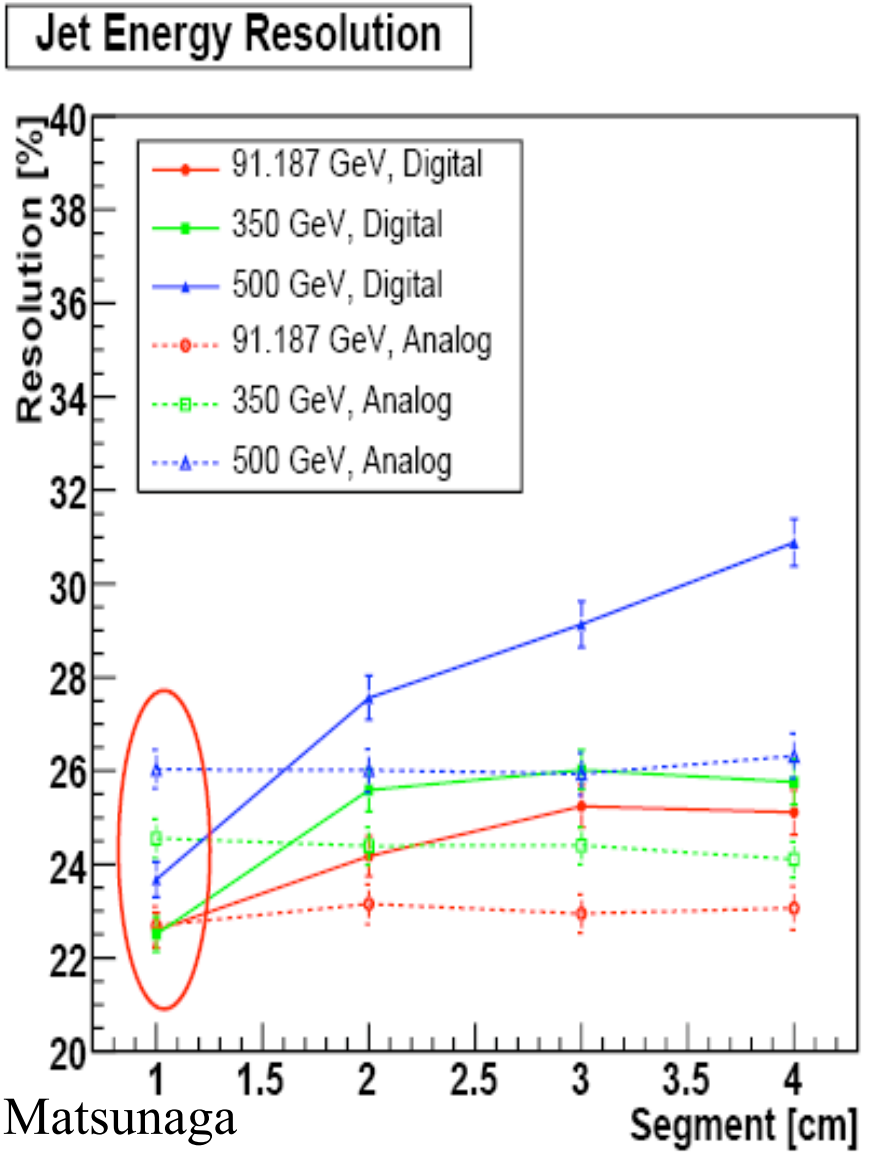
- Analog solution is favored at high energy due to number of particles in the central region.

But what about the 2-bit readout solution?
The study of KEK group for the GLD HCAL using :
2-bit, 3 thresholds (0.5, 10,100 MIPs) associated to
1×1 cm^2 tile size shows :

- Similar energy resolution with respect to the analog readout version for single particle at HE
- Better energy resolution for JETs

Jet Energy Resolution

- $e^+e^- \rightarrow qq$ (u/d/s)
  - $\sqrt{s} = 91, 350, 500$ GeV
- Energy measurement with (perfect) PFA
- In case of 1×1 cm^2 tile size, digital calorimeter achieved similar or slightly better jet energy resolution



courtesy H.Matsunaga

Digital HAdronic CALorimeter for ILC

Two efforts are followed in parallel to have high- granularity compact DHCAL:

USA: using GRPC/GEM with binary readout (1 bit) → Physics Prototype

Europe: using GRPC/MICROMEGAS
with semi-digital readout and ILC-like features →
Technological Prototype with the following guideline:

•DHCAL as compact and as hermetic as possible

Detectors for the DHCAL

Gas detectors:

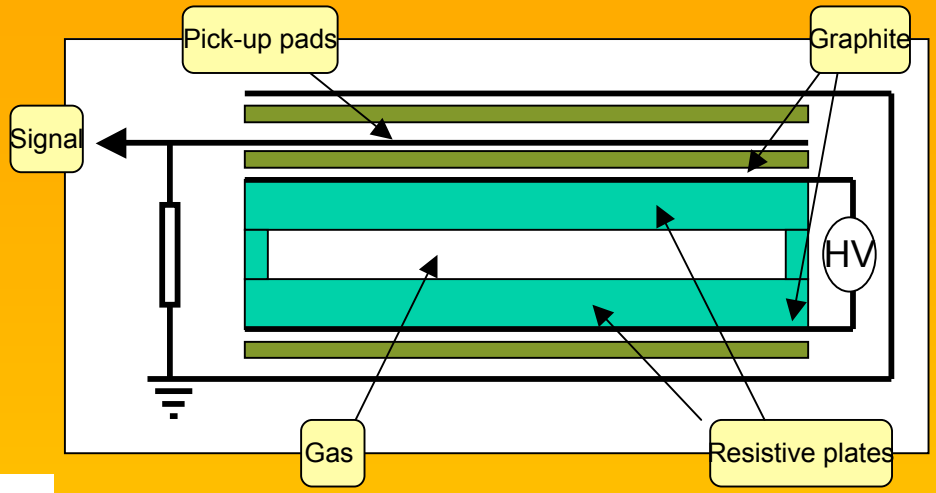
Thickness of few millimeters

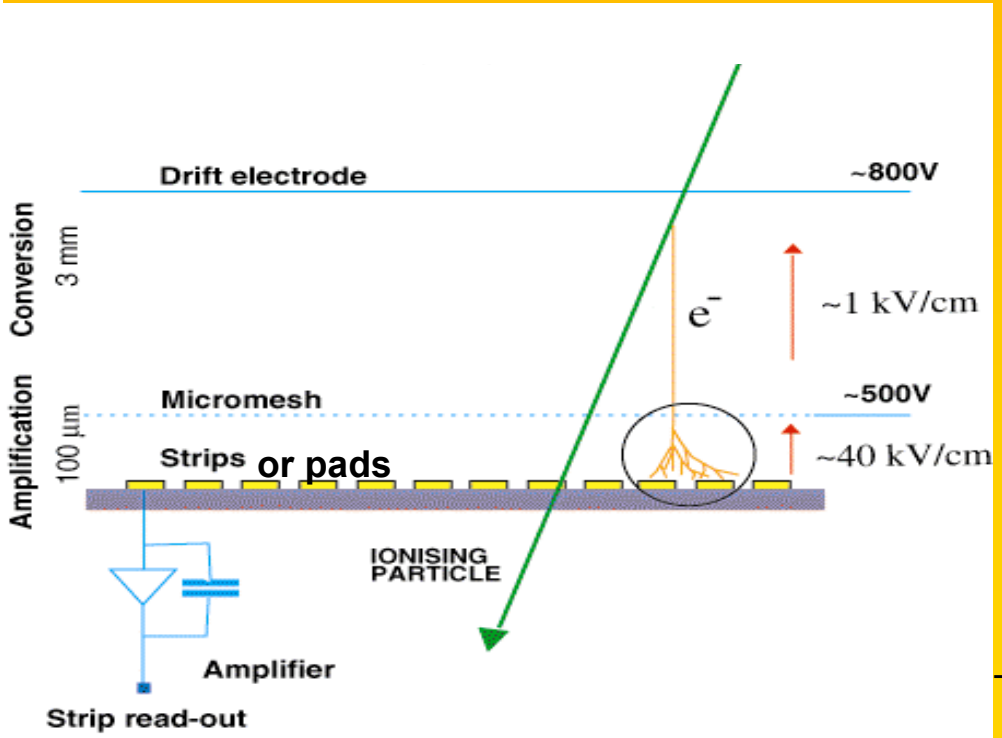
GRPC :

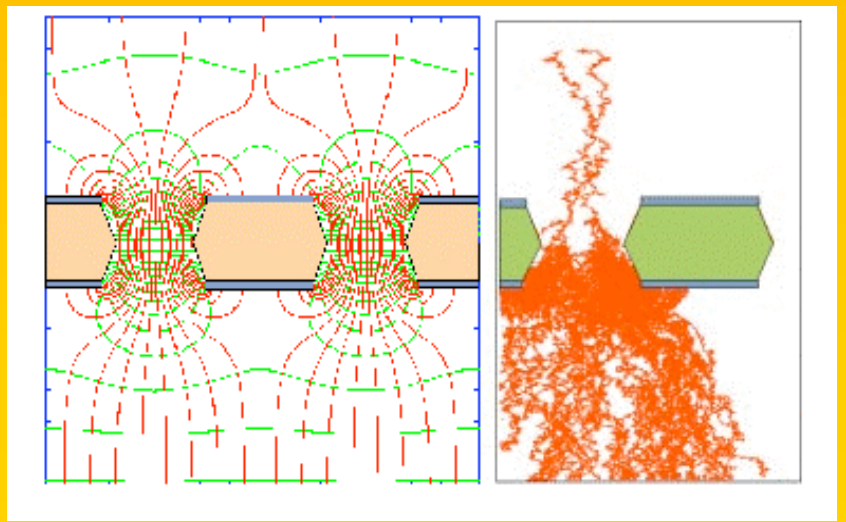
Robust but limited detection rate

µMEGAS,GEM :

delicate but high rate

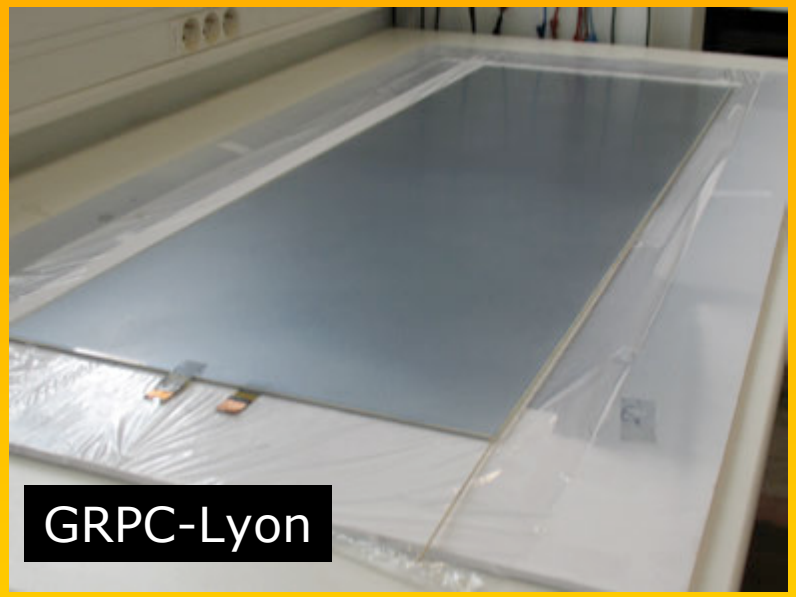




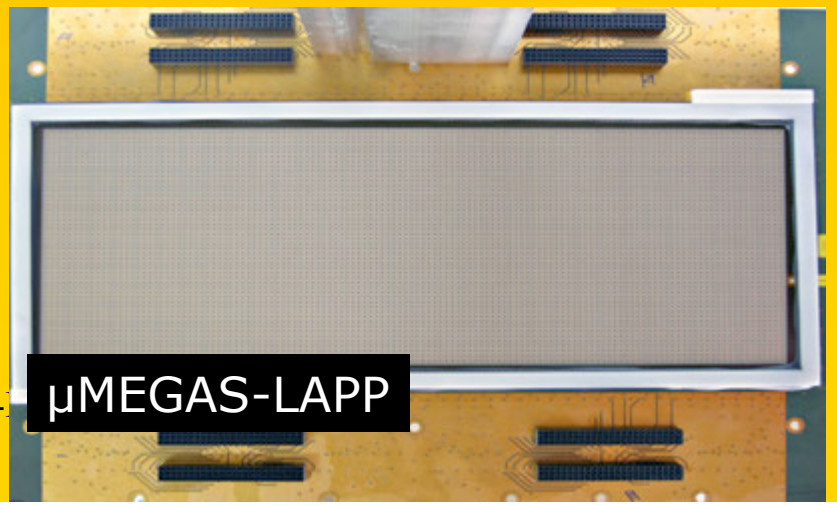


Detector dimensions :

GRPC: 8×8, 32×8, 50×32, 100×32, 100×100 1cm²-pad : already produced and tested.



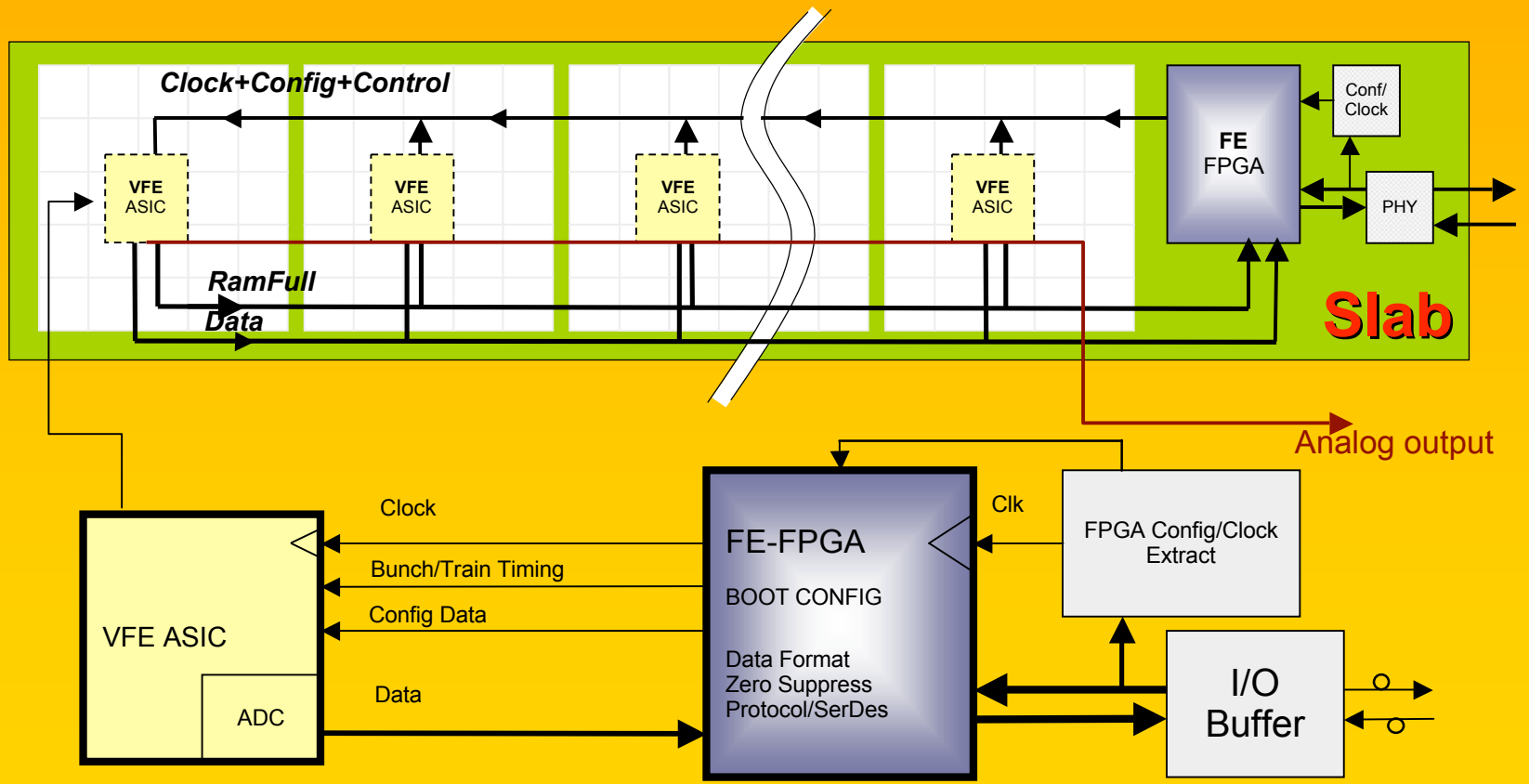
µMEGAS: 16×6, 32×8,32×12 1cm² produced and tested. Larger size detectors are under development



The challenge:

How to have a detector of few thousands m²
fully equipped with low consumption semi-digital readout
and still very compact !!!!?

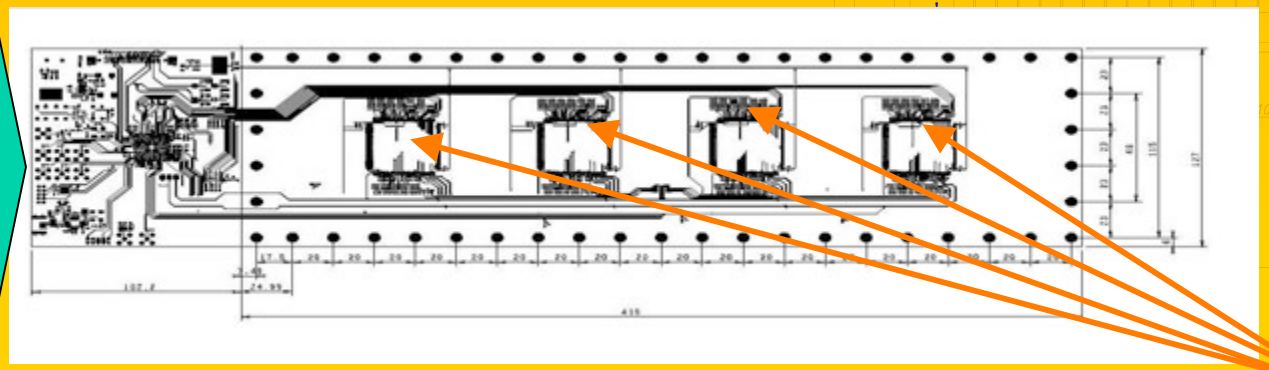
Embedded Daisy-chained electronics is the solution

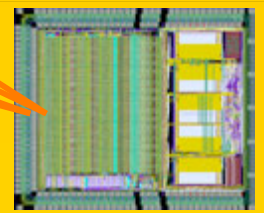


4-Chip project

Aim: Validate the new electronics/acquisition scheme for DHCAL

- 8×32 pads detector (GRPC and µMEGAS)
- 8-layer PCB
- 4 chips (64 ch)
- Readout USB + FPGA

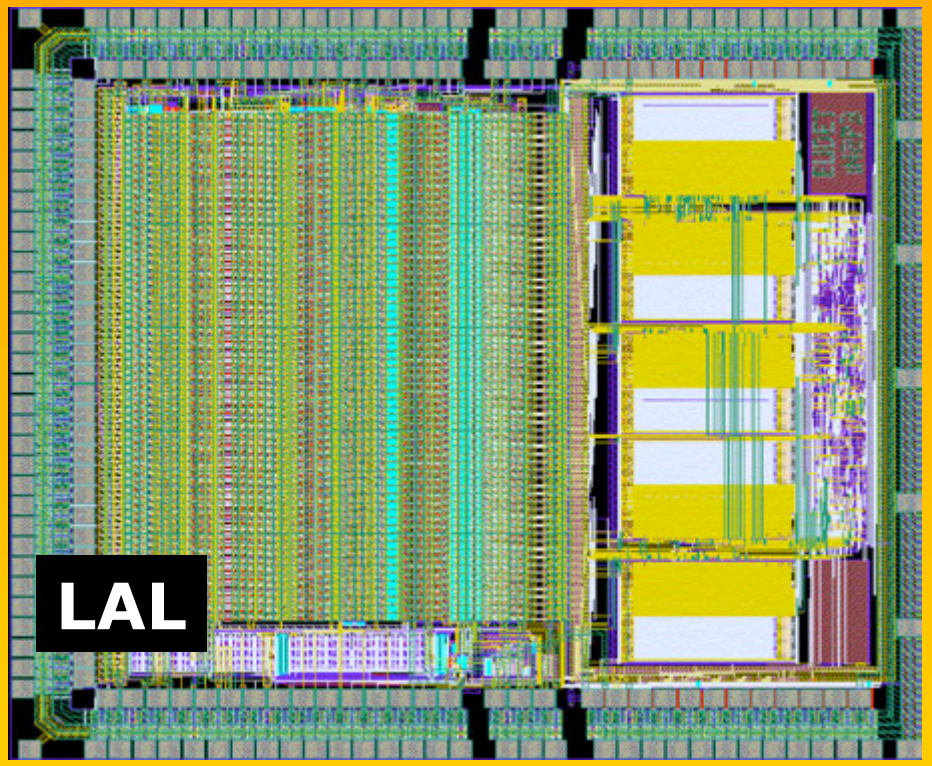




Electronics

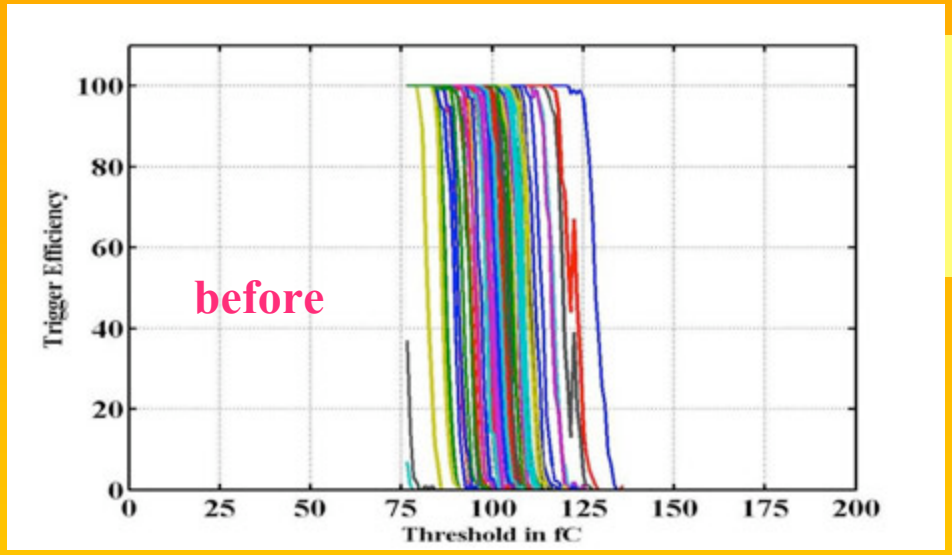
HARDROC

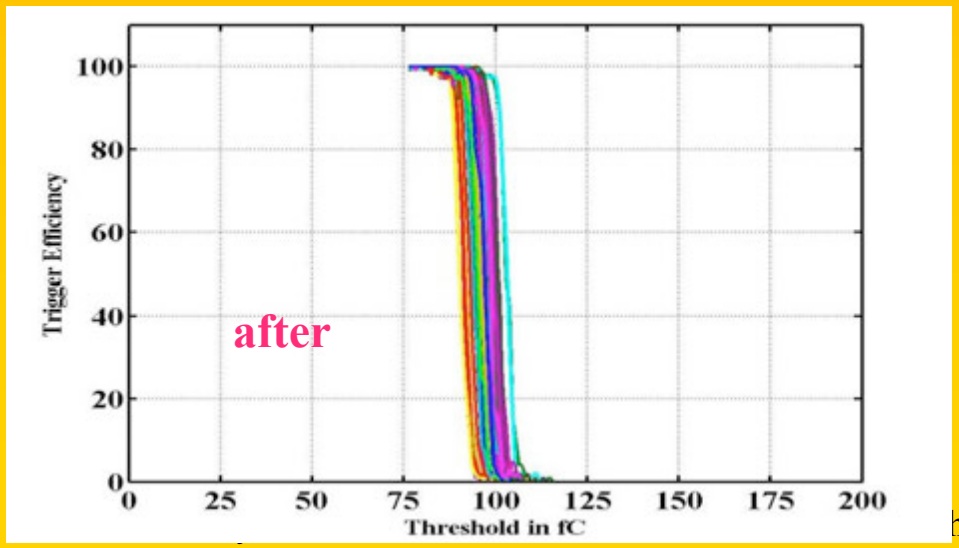
- 64 channels, 16mm²
- Digital/analog output.
- 2 thresholds(3 very soon)
- low consumption, power pulsing (< 10 µW/ch)
- Digital memory able to store up to 128 evts.
- Large gain range
- Xtalk <2%
- Adequate for GRPC* (threshold > 10 fc)

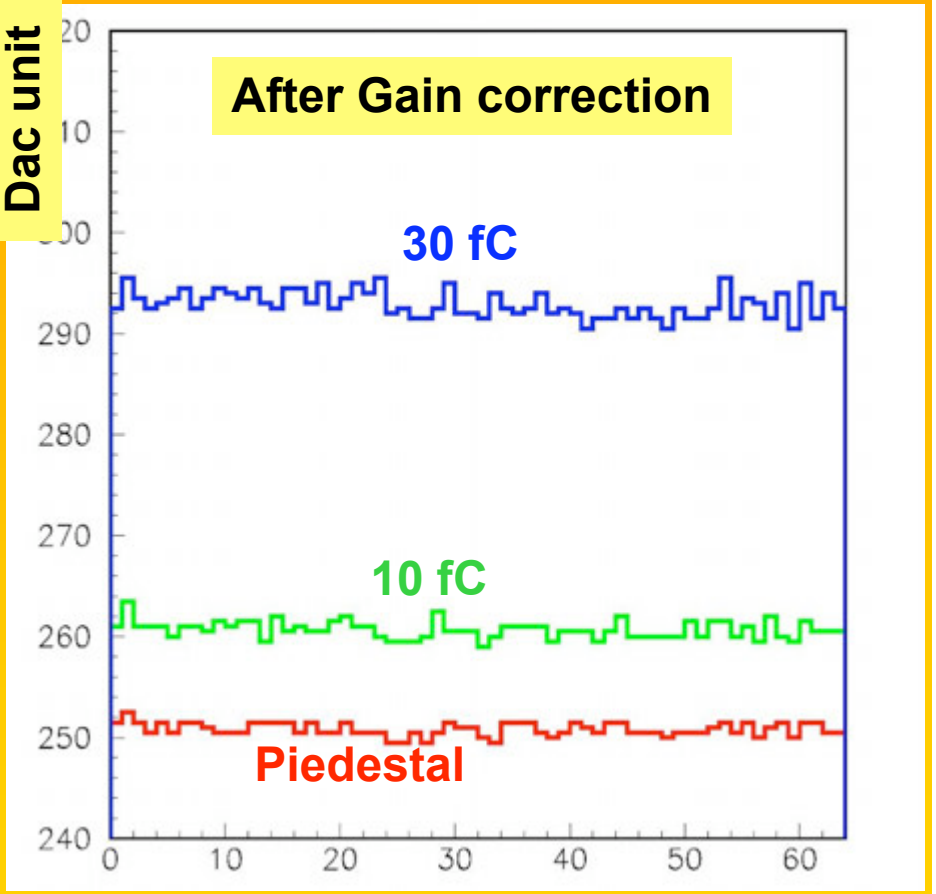


***For µMEGAS another ASIC is developed in Lyon with a threshold as low as 3 fc**

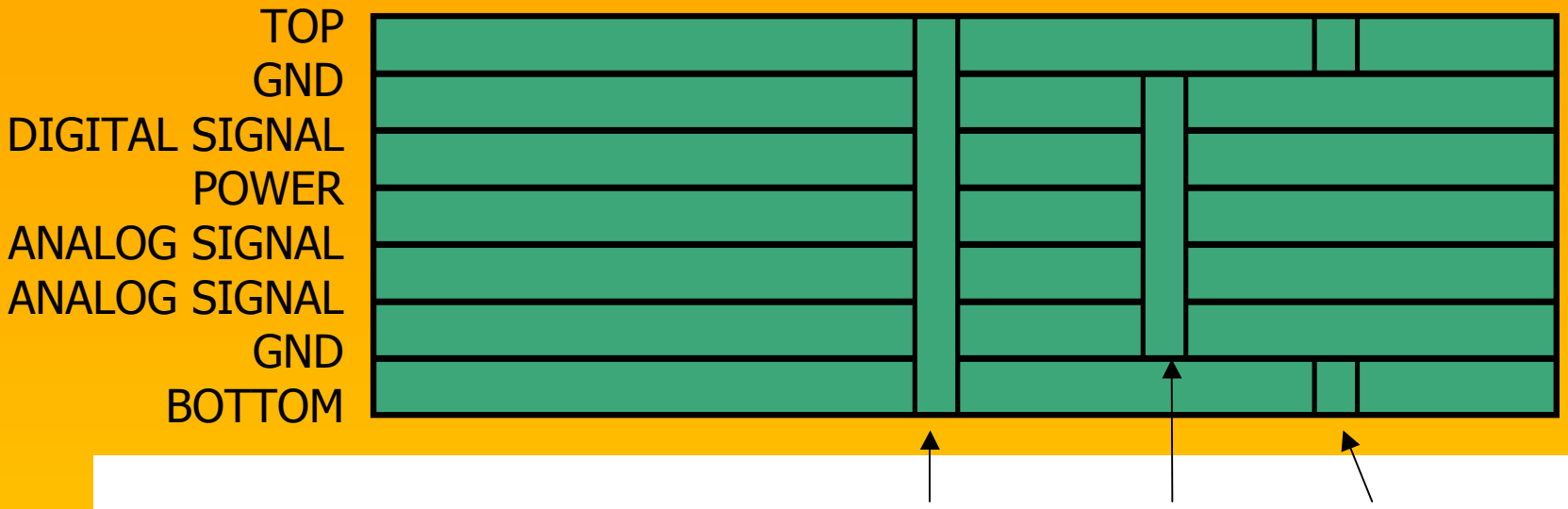
HARDROC: Scurves of 64 channels

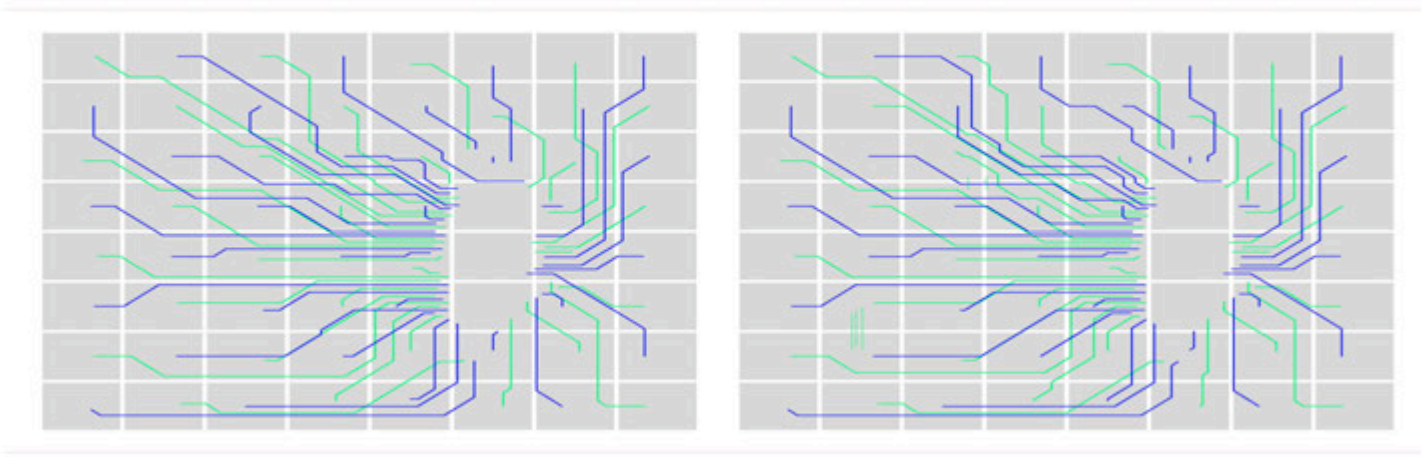




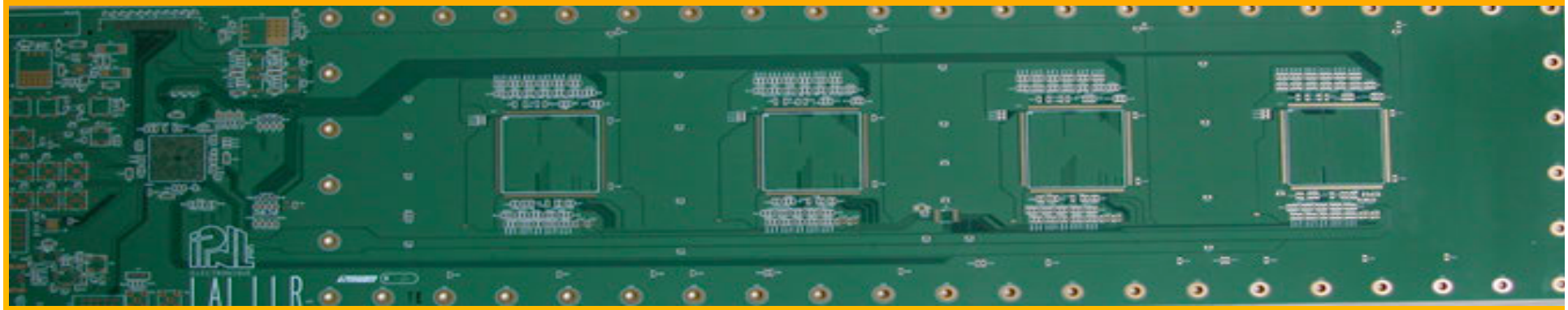


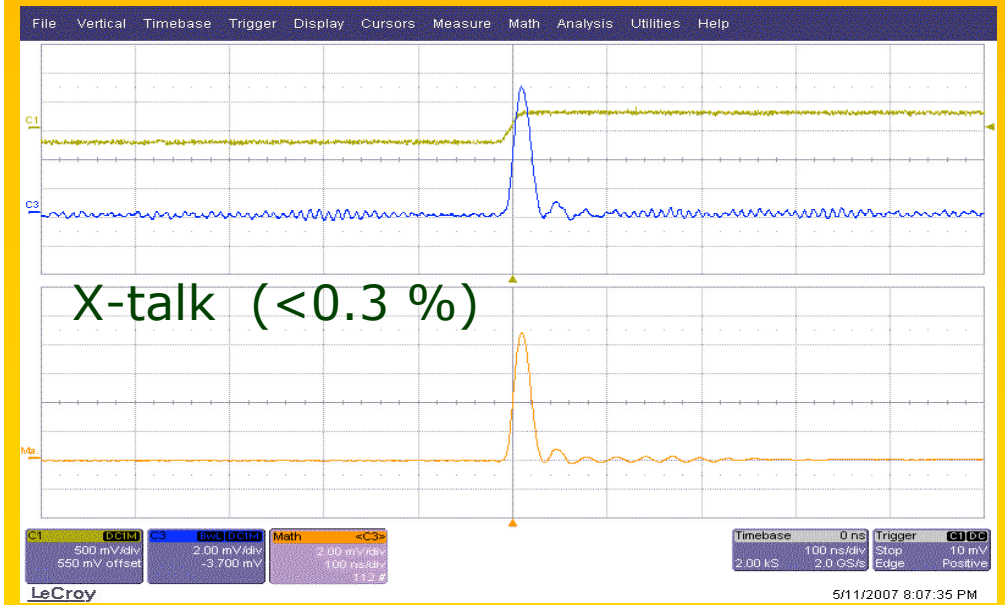
8-layer PCB

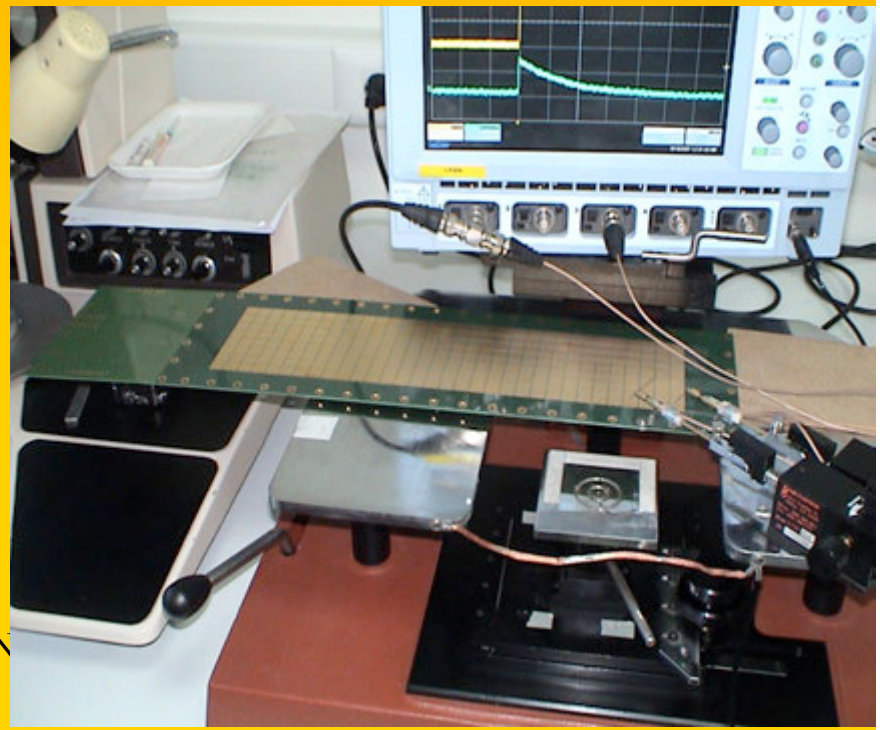

TOP
GND
DIGITAL SIGNAL
POWER
ANALOG SIGNAL
ANALOG SIGNAL
GND
BOTTOM
Through via
Blind via
Buried via



- 8-layer PCB , 800 µ thick
- 8×32 pads of 1 cm² and 500 µ separation







Readout system

The 4 chips are daisy-chained and connected to a FPGA communicating with a pc through a USB device.

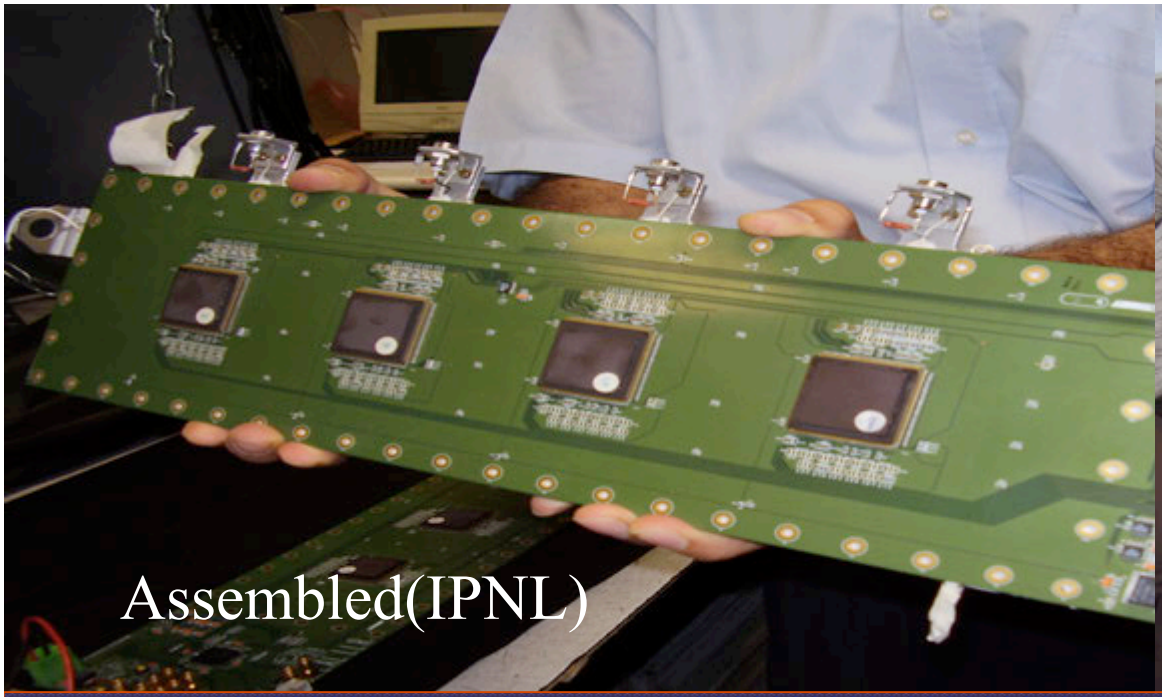
Firmware + Software were developed to allow charging the slow control parameters from file/flux and controlling the procedure.

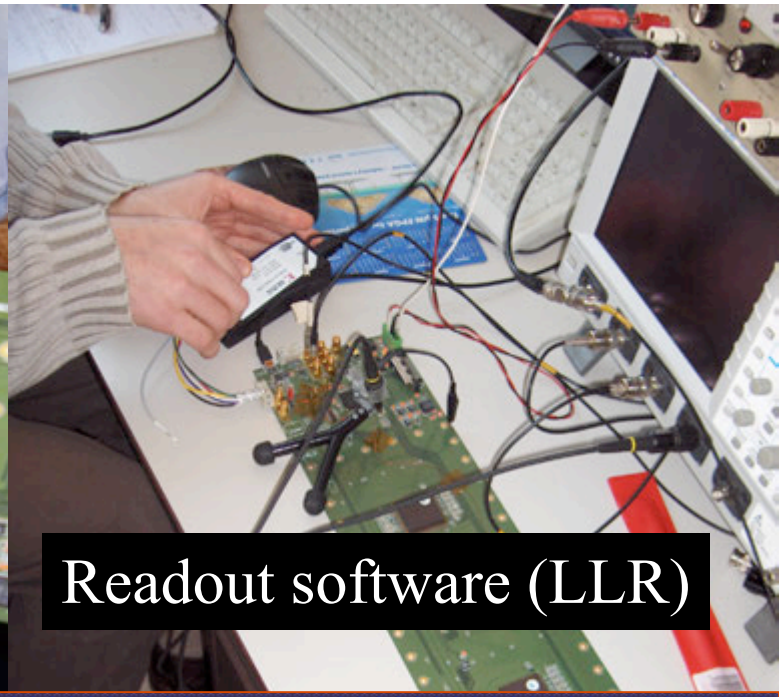
Acquisition modes : different modes are allowed:

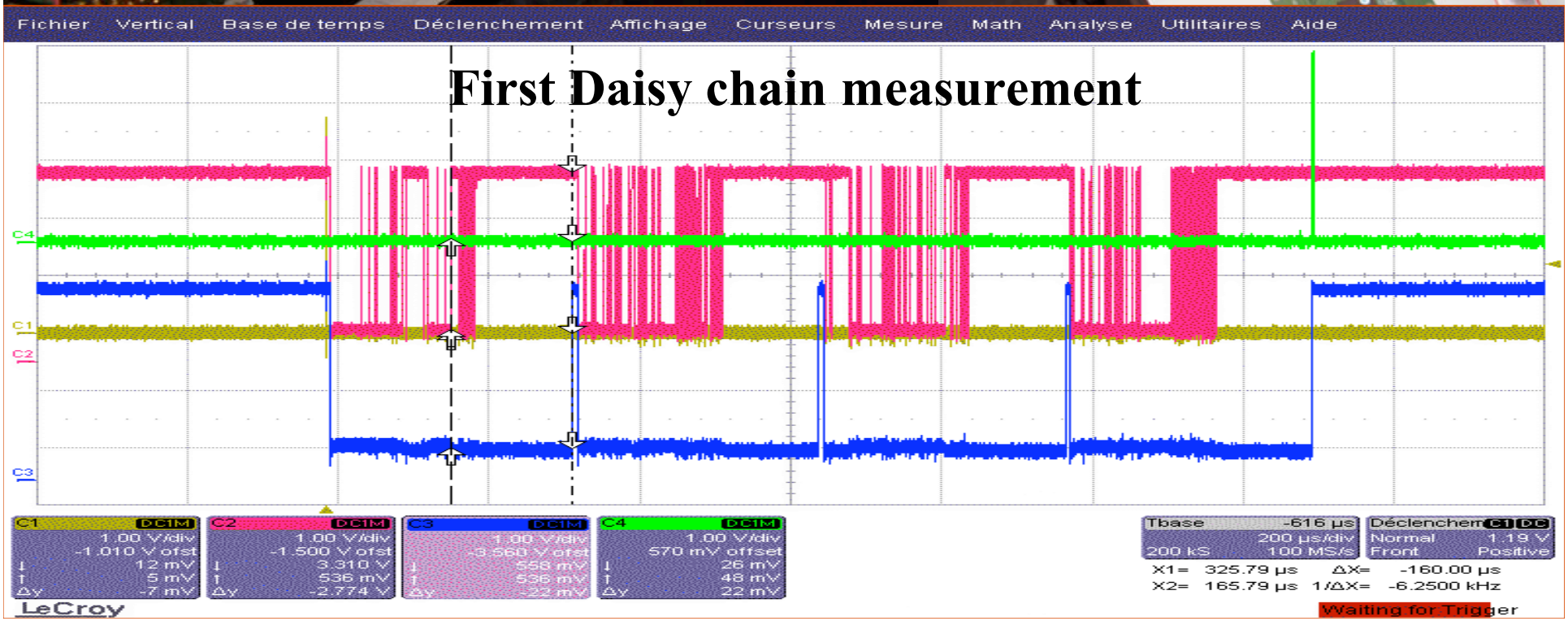
a) Internal triggers

b) External triggers : cosmics & test beam

Data output: The two kinds of data output of the hardroc chips are accessible: digital and analog


Assembled(IPNL)

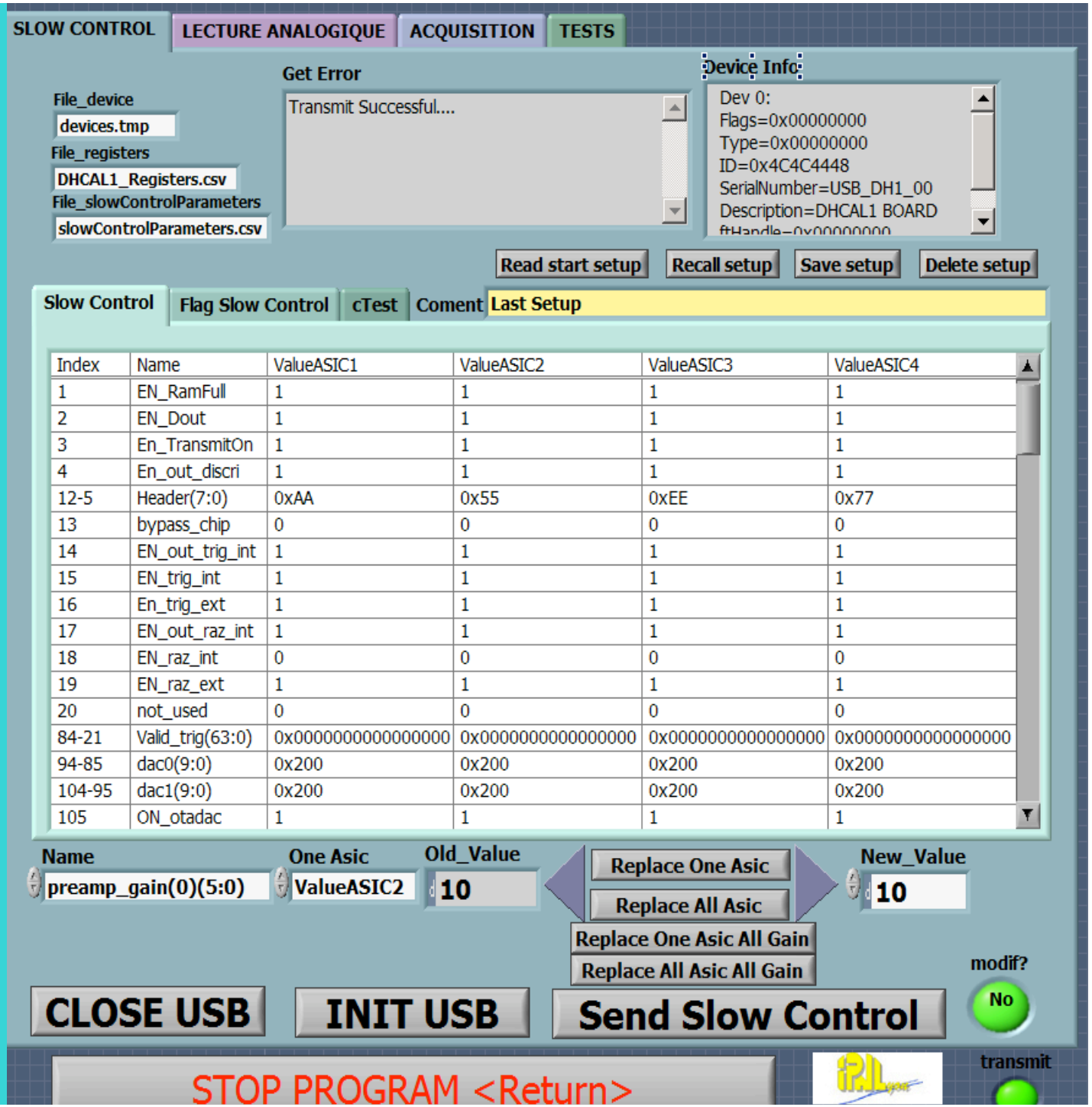

Readout software (LLR)


Fichier Vertical Base de temps Déclenchement Affichage Curseurs Mesure Math Analyse Utilitaires Aide
First Daisy chain measurement
C4
C1
C2
C3
C1 DC1M 1.00 V/div -1.010 V ofst 12 mV 5 mV -7 mV
C2 DC1M 1.00 V/div -1.500 V ofst 3.310 V 536 mV -2.774 V
C3 DC1M 1.00 V/div -3.560 V ofst 558 mV 536 mV -22 mV
C4 DC1M 1.00 V/div 570 mV offset 26 mV 48 mV 22 mV
Tbase -616 µs 200 µs/div 200 kS 100 MS/s
Déclenchem C1 DC Normal 1.19 V Front Positive
X1= 325.79 µs ΔX= -160.00 µs
X2= 165.79 µs 1/ΔX= -6.2500 kHz
LeCroy
Waiting for Trigger

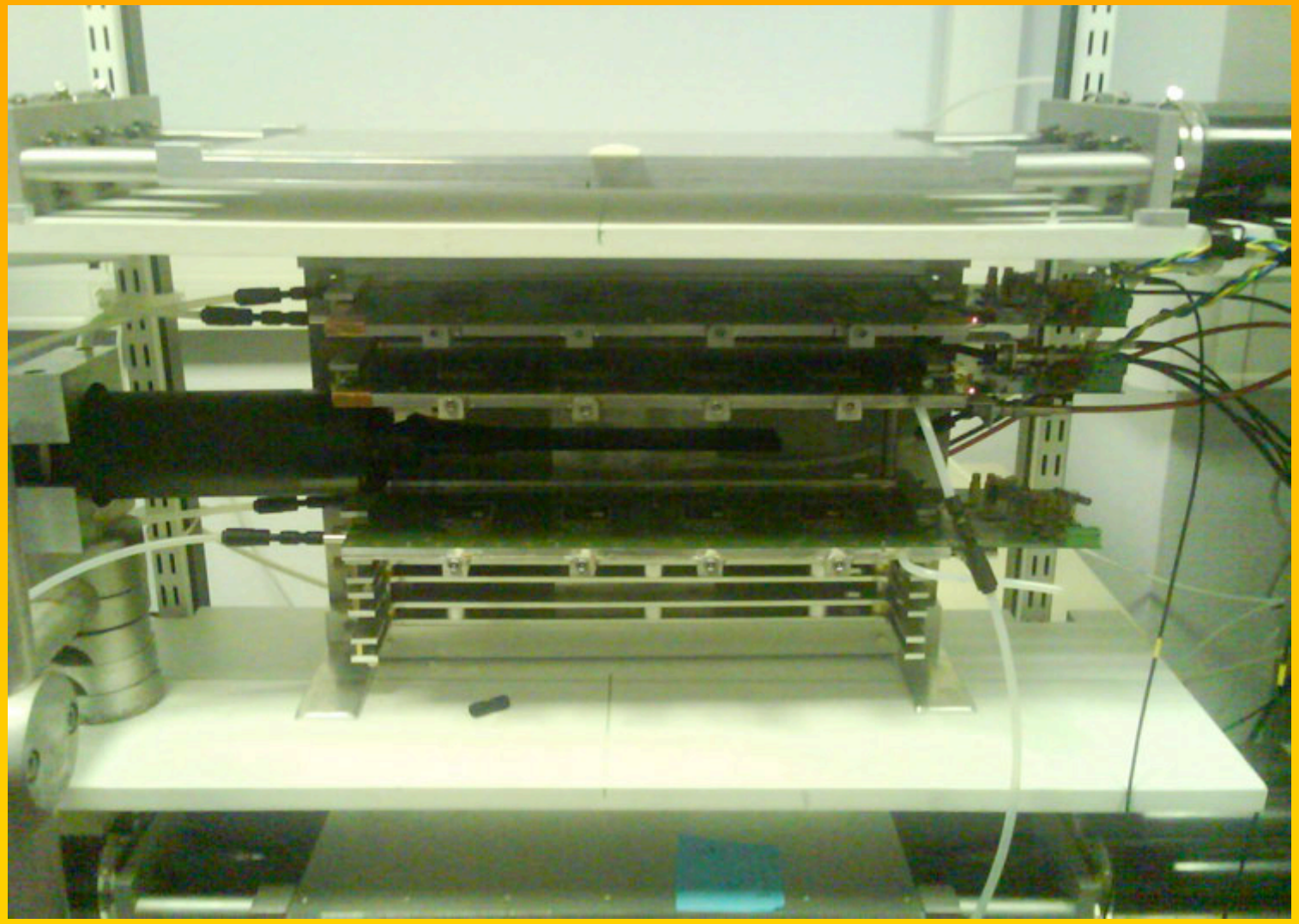
* Two thresholds

* Gain value of each channel can be chosen in [0-63]

•Calibration is done automatically for all channels by injecting charge through internal capacitors



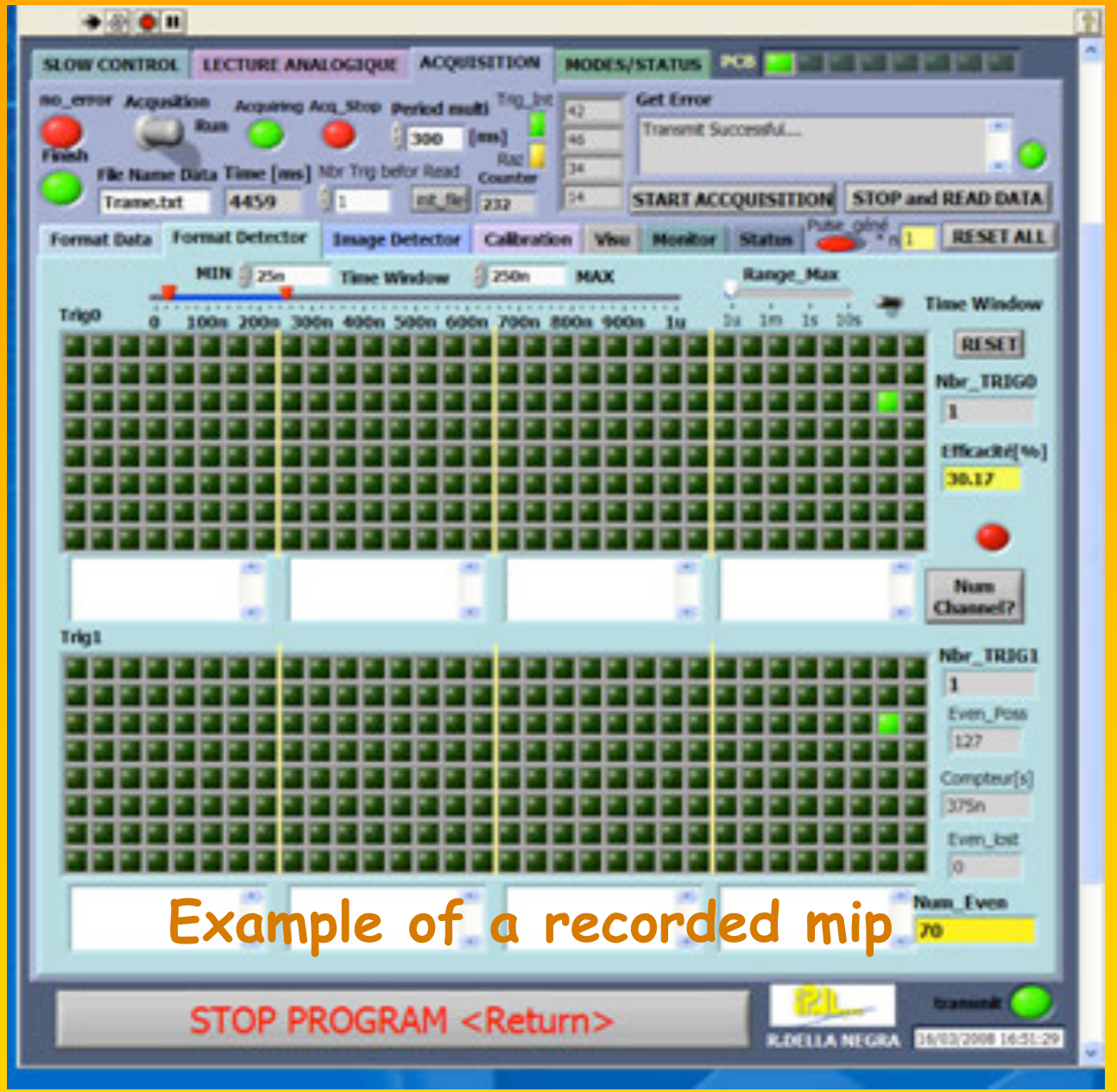
Slice test



On the test bench with GRPC

Second threshold

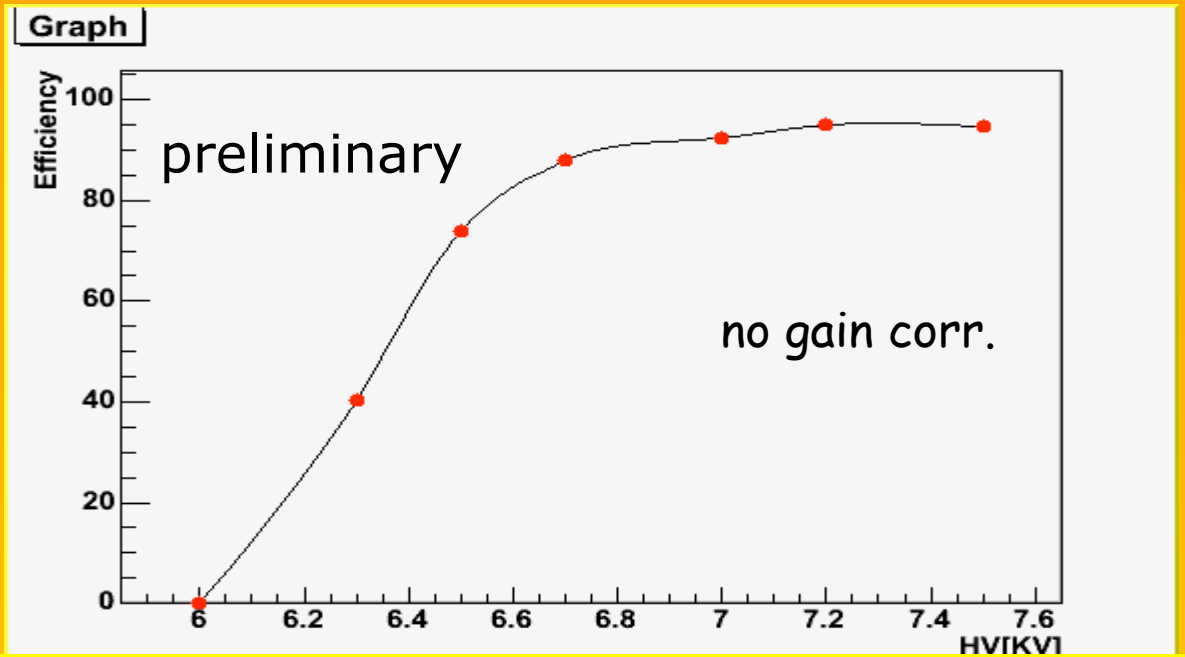
First threshold



Example of a recorded mip

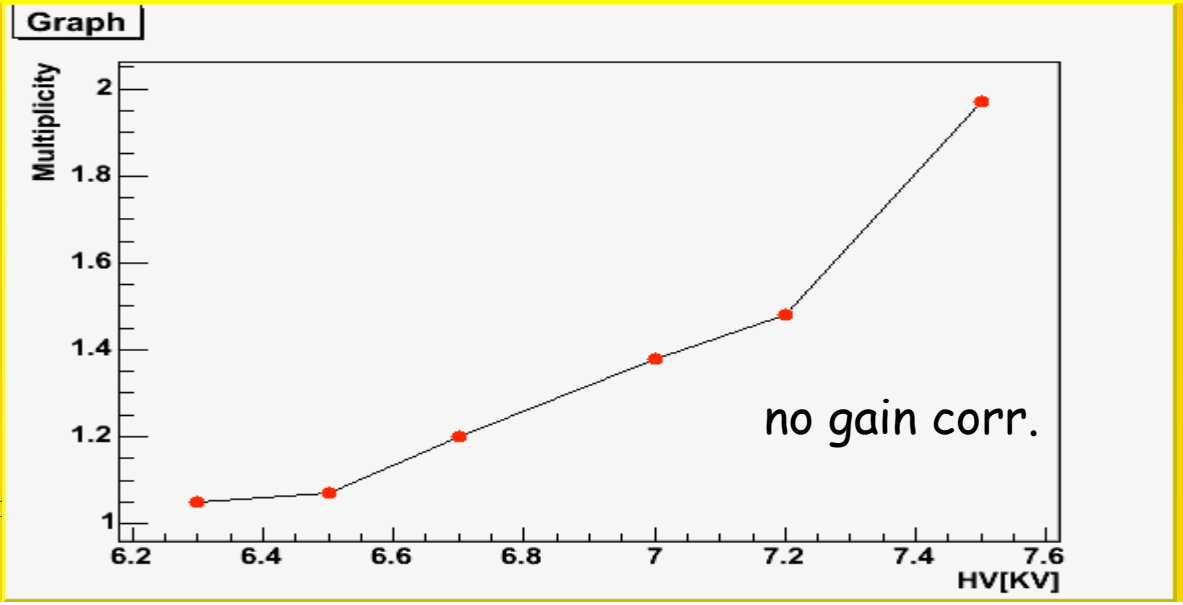
First results

GRPC
32×8 pads
RP:graphite



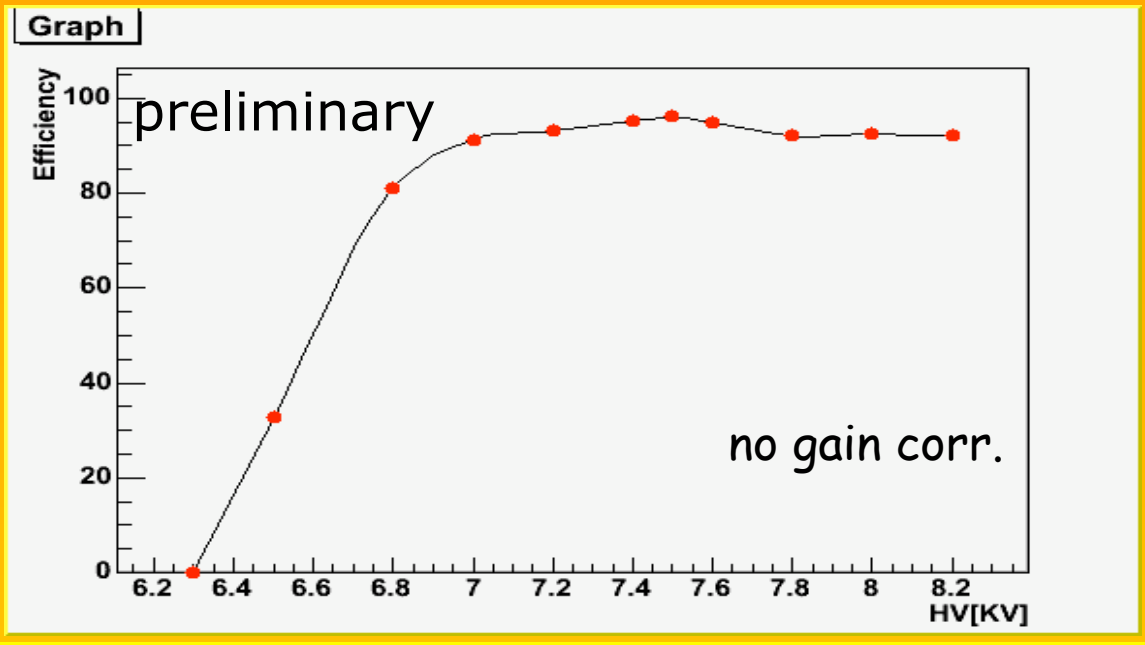
TFE 93%
Isobutene 5%
SF6 2%

Threshold≈ 100 fc



First results

GRPC
32×8 pads
RP:licron



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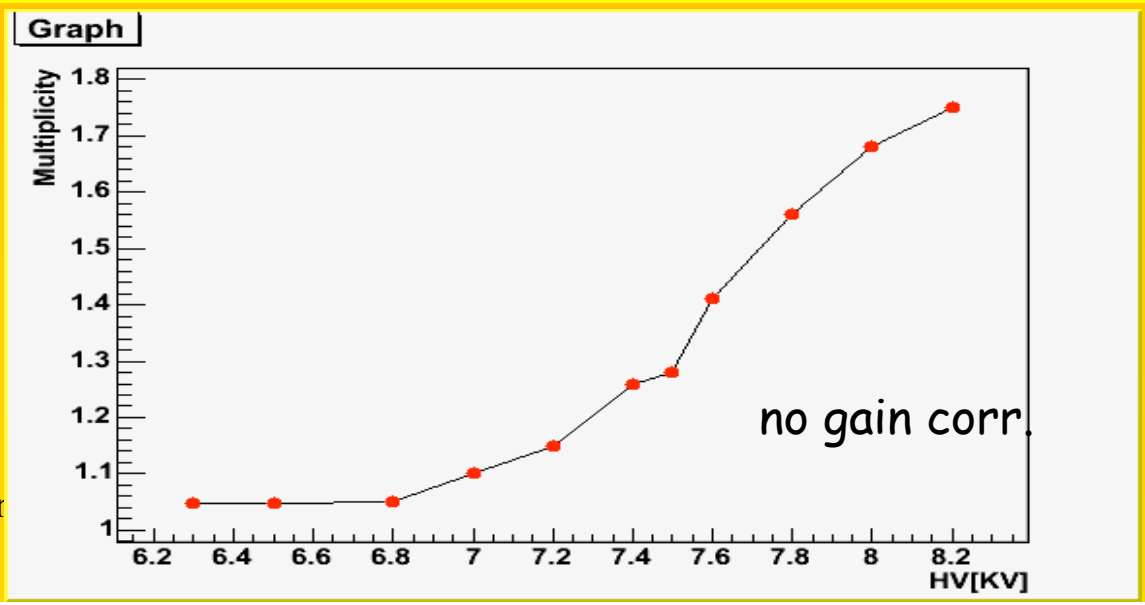
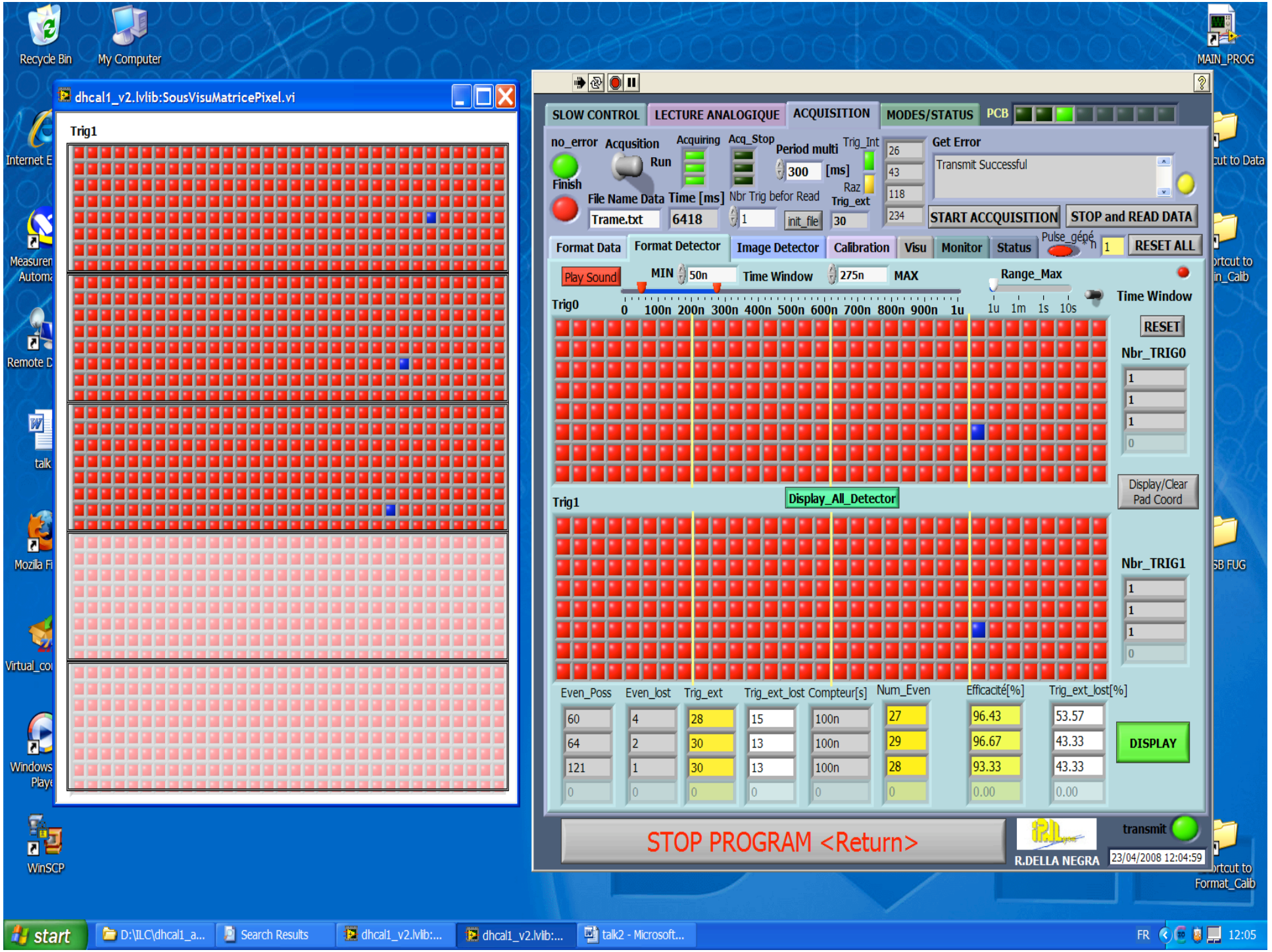
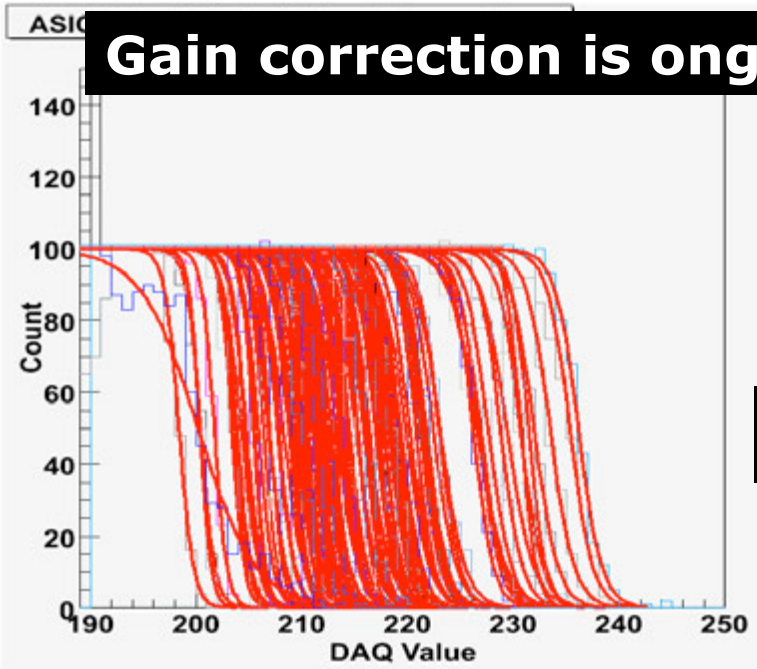
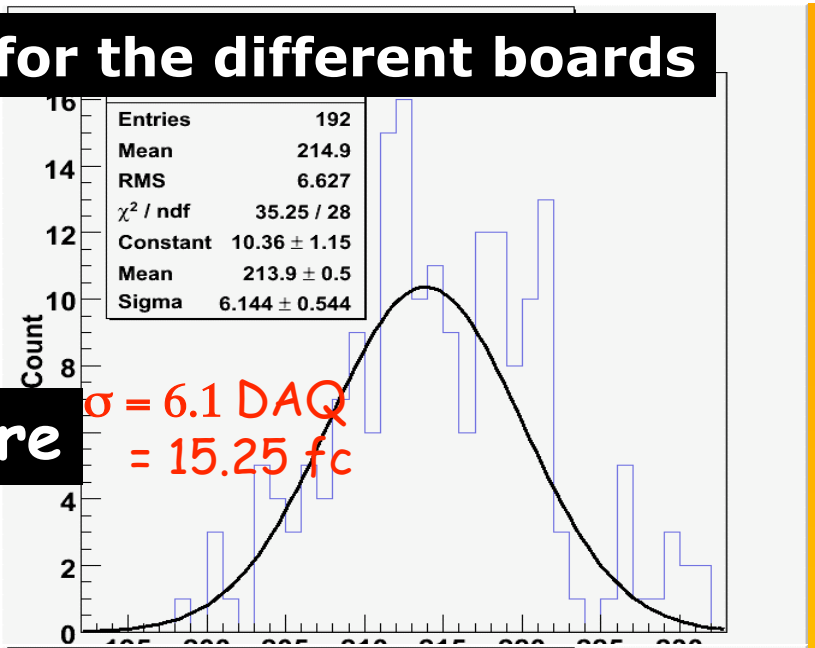



Recycle Bin
My Computer
MAIN_PROG
dhcal1_v2.lvlib:SousVisuMatricePixel.vi
Trig1
SLOW CONTROL
LECTURE ANALOGIQUE
ACQUISITION
MODES/STATUS
PCB
no_error
Acqusition
Run
Finish
Acquiring
Acq_Stop
Period multi
300
[ms]
Trig_Int
Raz
Trig_ext
Get Error
Transmit Successful
File Name Data
Trame.txt
Time [ms]
6418
Nbr Trig befor Read
1
init_file
30
26
43
118
234
START ACQUISITION
STOP and READ DATA
Format Data
Format Detector
Image Detector
Calibration
Visu
Monitor
Status
Pulse_gépé
1
RESET ALL
Play Sound
MIN
50n
Time Window
275n
MAX
Range_Max
Time Window
Trig0
0 100n 200n 300n 400n 500n 600n 700n 800n 900n 1u
1u 1m 1s 10s
RESET
Nbr_TRIG0
1
1
1
0
Display_All_Detector
Display/Clear Pad Coord
Trig1
Nbr_TRIG1
1
1
1
0
Even_Poss
Even_lost
Trig_ext
Trig_ext_lost
Compteur[s]
Num_Even
Efficacité[%]
Trig_ext_lost[%]
60 4 28 15 100n 27 96.43 53.57
64 2 30 13 100n 29 96.67 43.33
121 1 30 13 100n 28 93.33 43.33
0 0 0 0 0 0 0.00 0.00
DISPLAY
STOP PROGRAM <Return>
R.DELLA NEGRA
transmit
23/04/2008 12:04:59
WinSCP
start
D:\ILC\dhcal1_a...
Search Results
dhcal1_v2.lvlib:...
dhcal1_v2.lvlib:...
talk2 - Microsoft...
FR
12:05

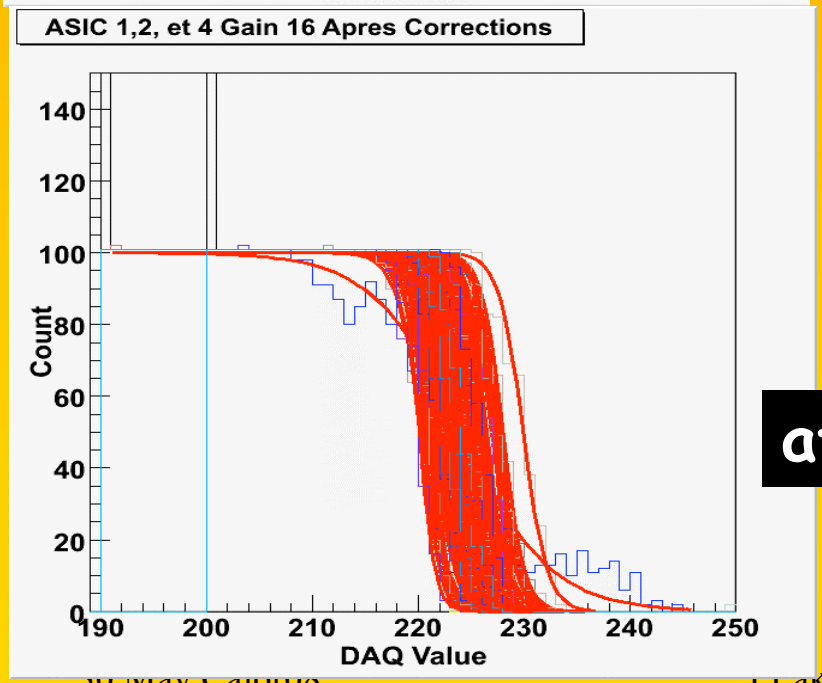
Gain correction is ongoing for the different boards



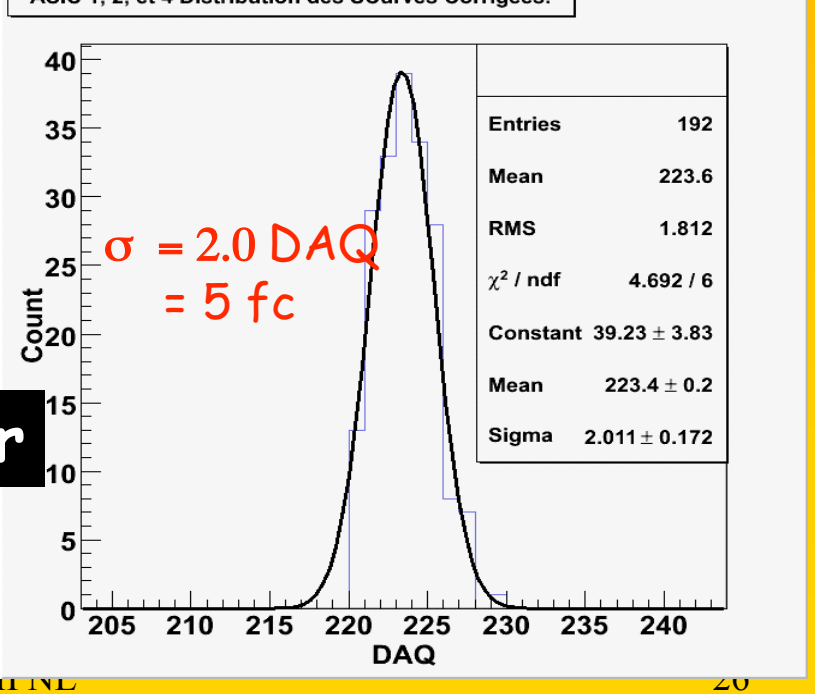


before

σ = 6.1 DAQ
= 15.25 fc

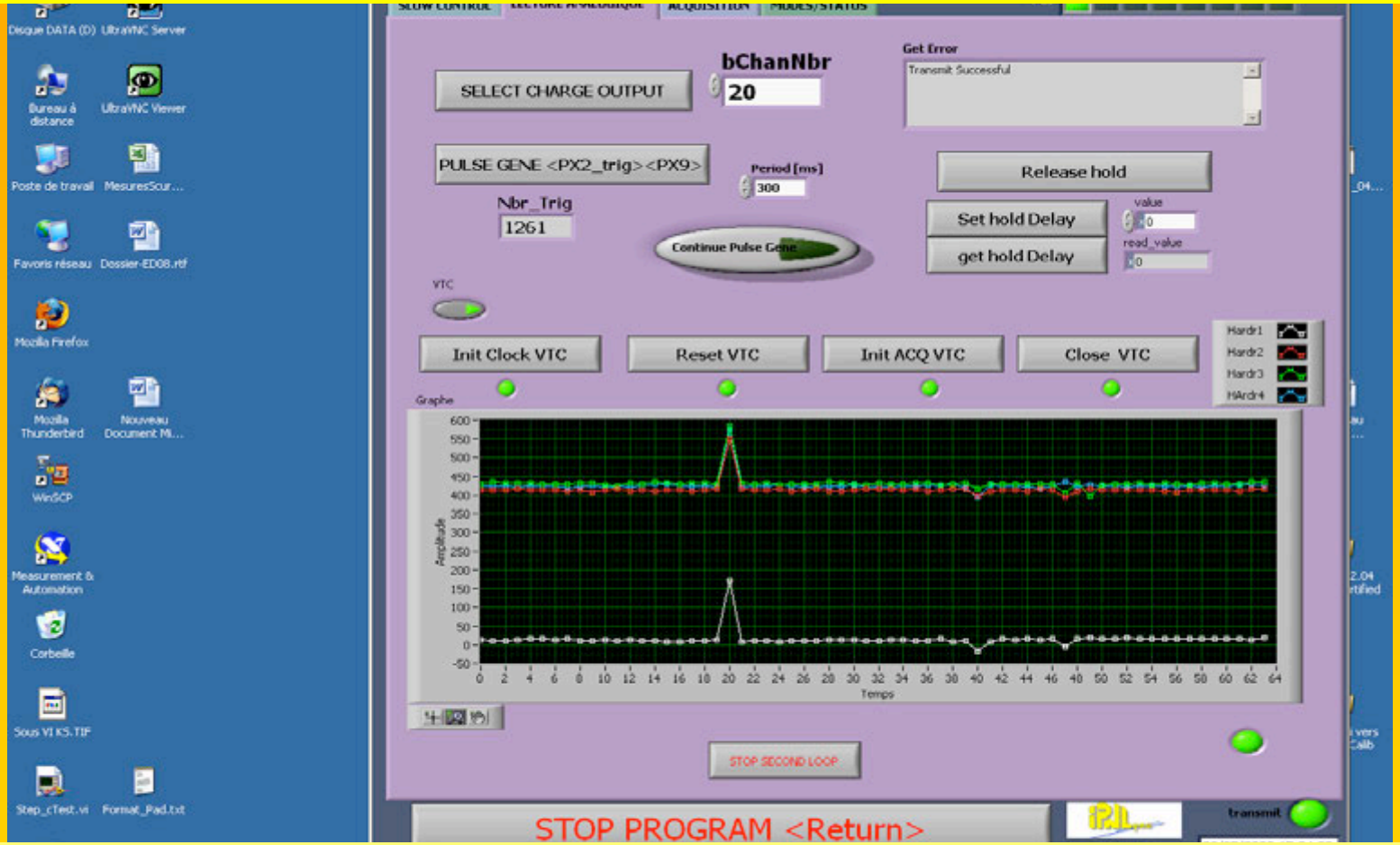


after



σ = 2.0 DAQ
= 5 fc

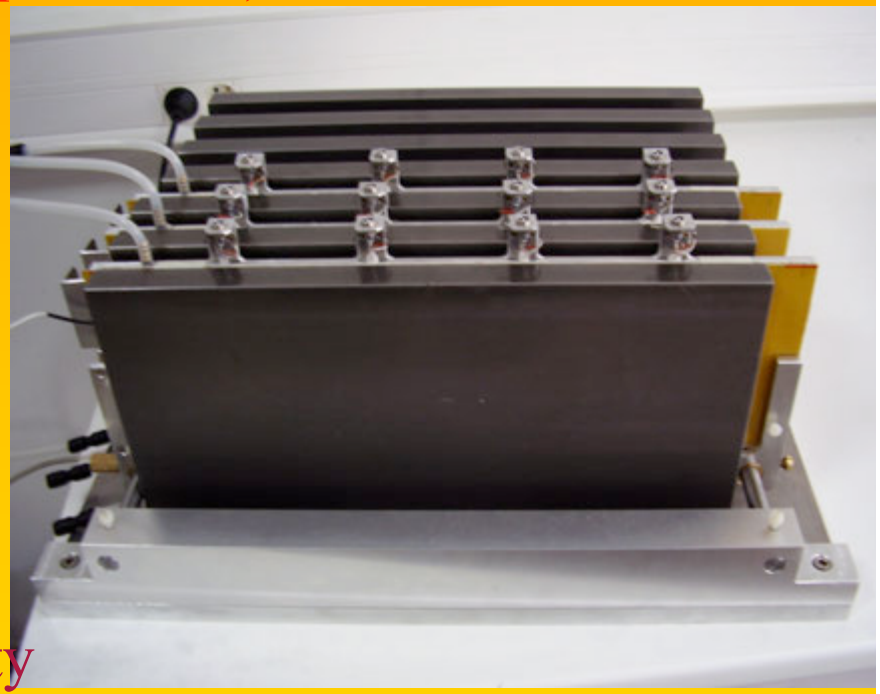
Analog readout was recently integrated and
will be used to chose the thresholds adequately



Amplitude of the signal injected in one of the 64 channels
of each of the 4 ASICs through internal capacitors

Beam test

Final confirmation of the success of our electronic readout system will be coming soon with the beam tests with 5 fully equipped detectors (32×8 pads each):

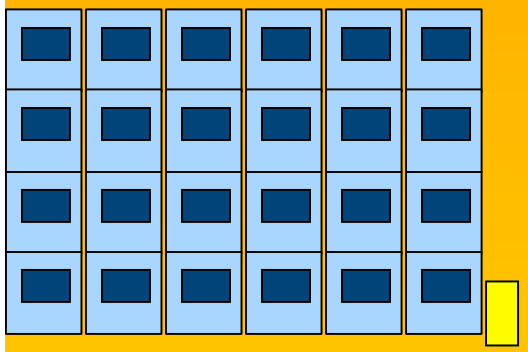


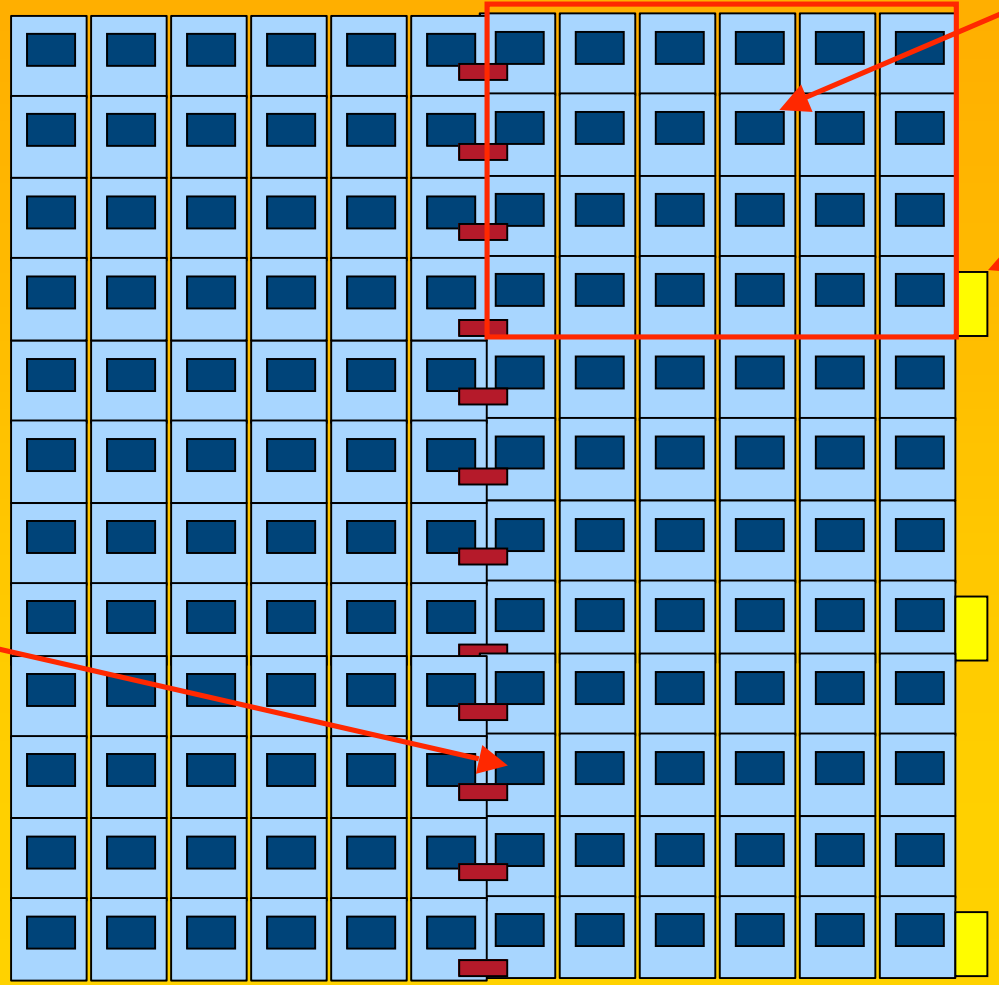
10-17 July :
beam test@ps-cern
3-11 August :
beam test@sps-cern

To study:
* Efficiency and multiplicity
vs:angle, position, particle multiplicity
* but also the first phase of the Hadronic shower

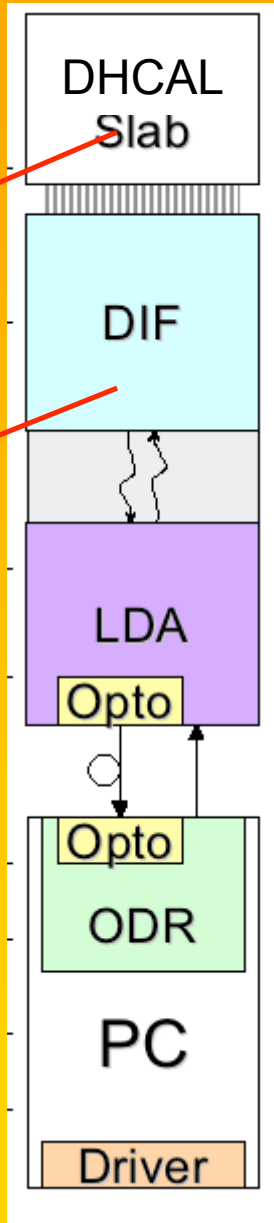
1m² project

ASU↔ 6×4 chips

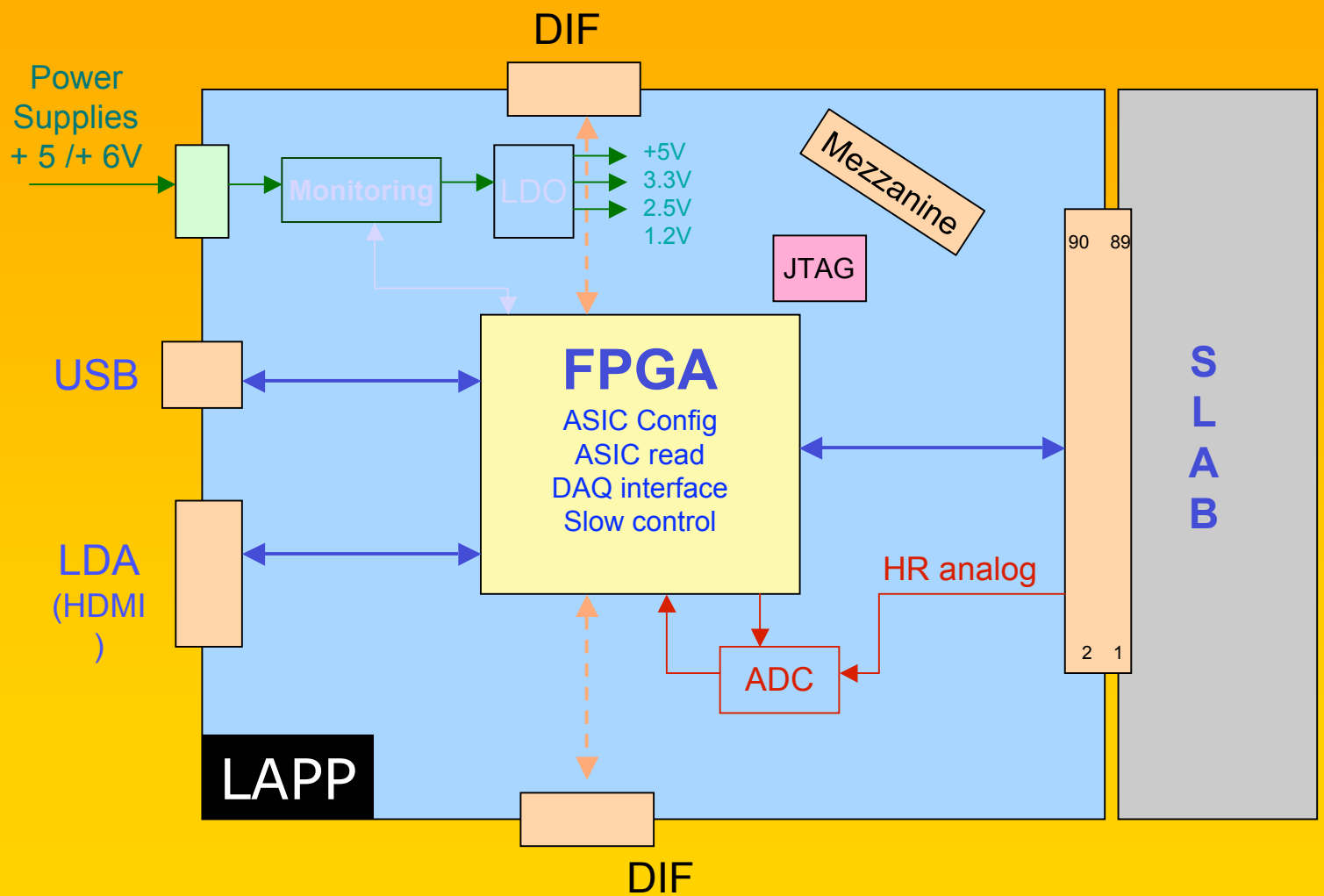




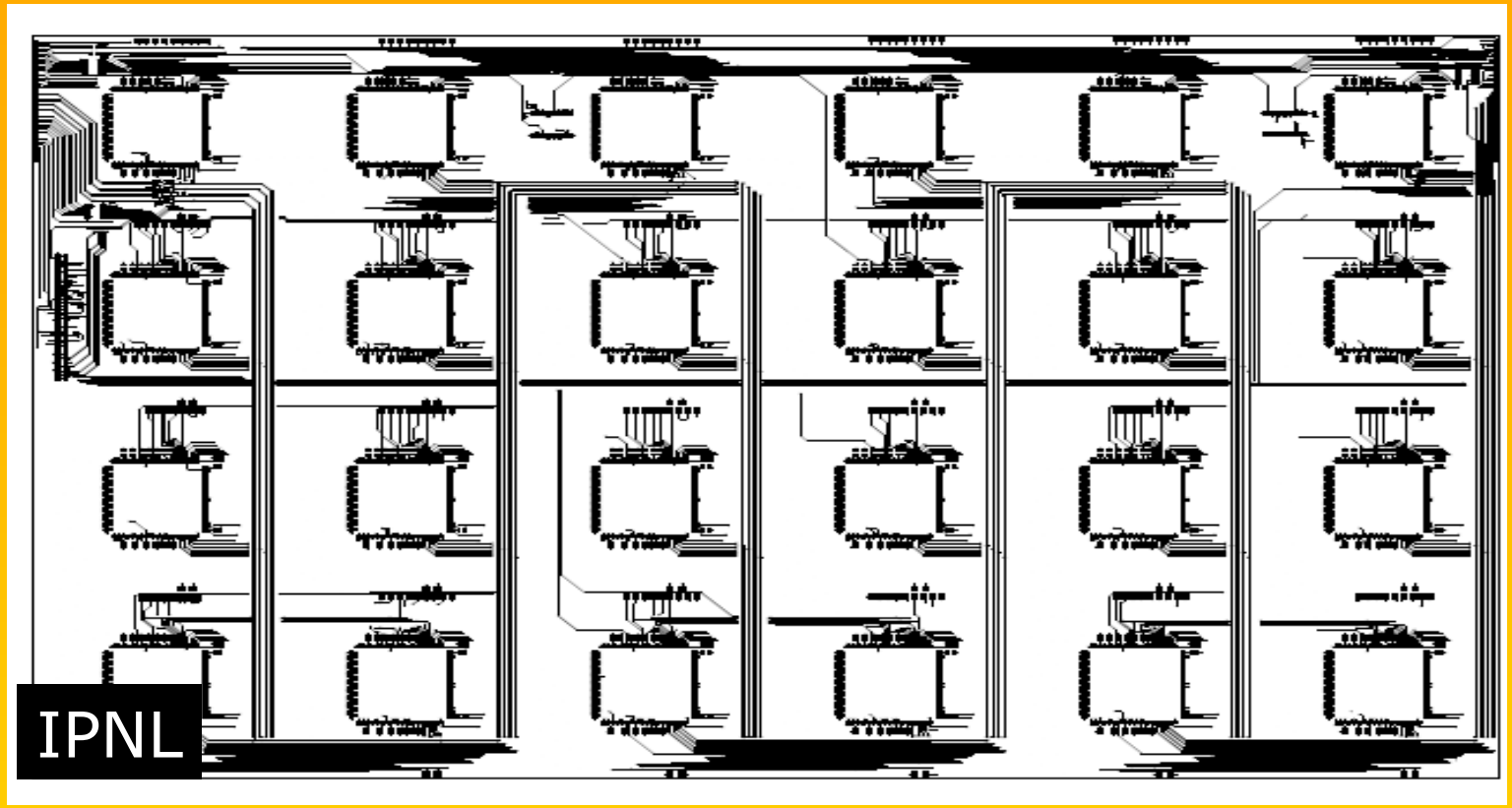
pcb-connector



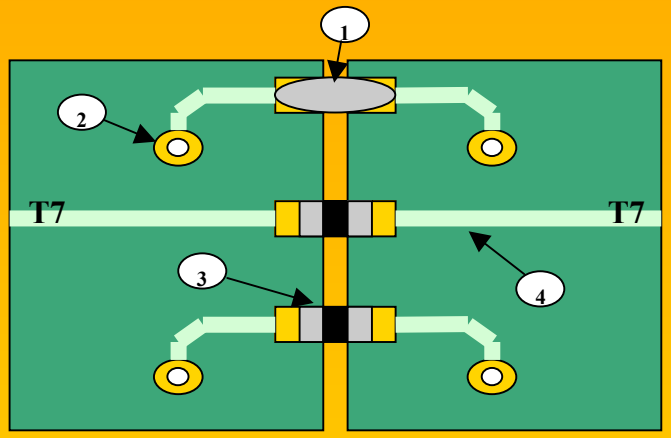
DIF is already designed and sent to fabrication



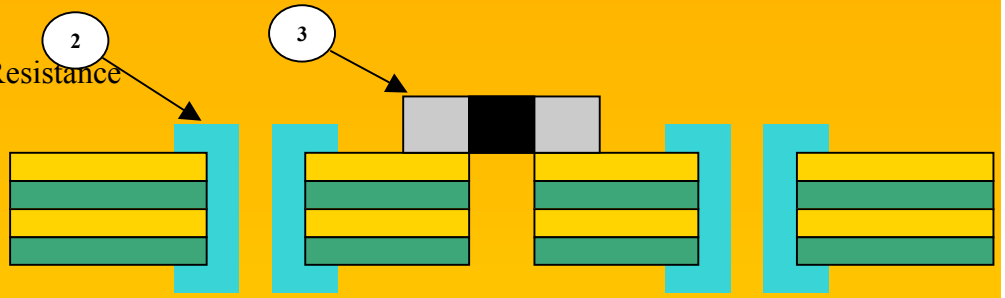
ASU hosting 24 hardroc chips is already designed

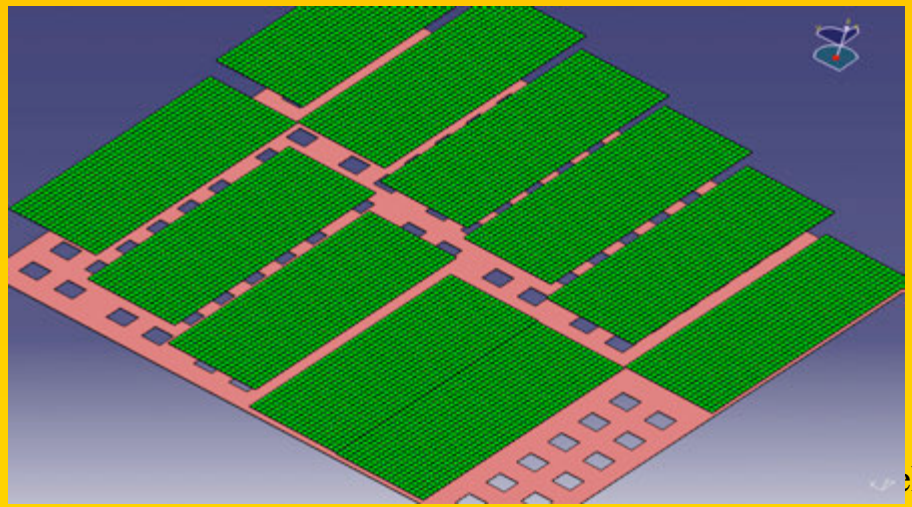


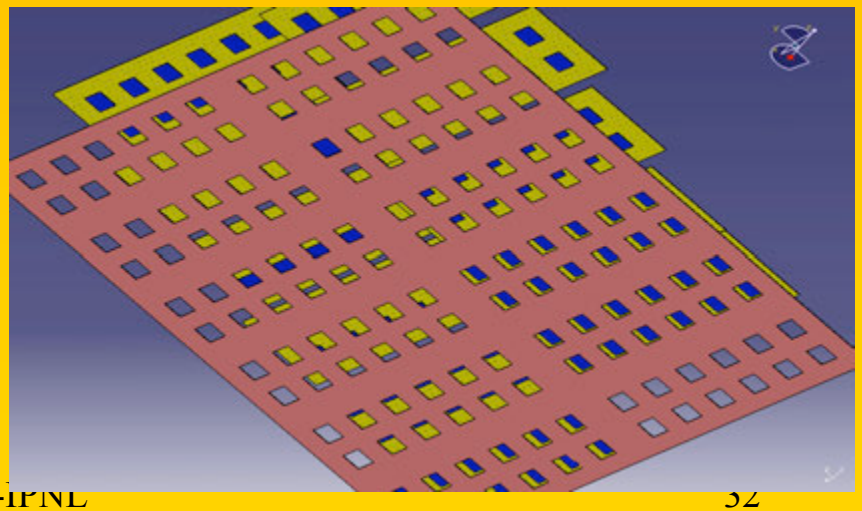
Connection between the different ASU is under study: signal transmission+ mechanics (IPNL+CIEMAT)



1 weld
2 Via
3 0 ΩResistance
4 Pist

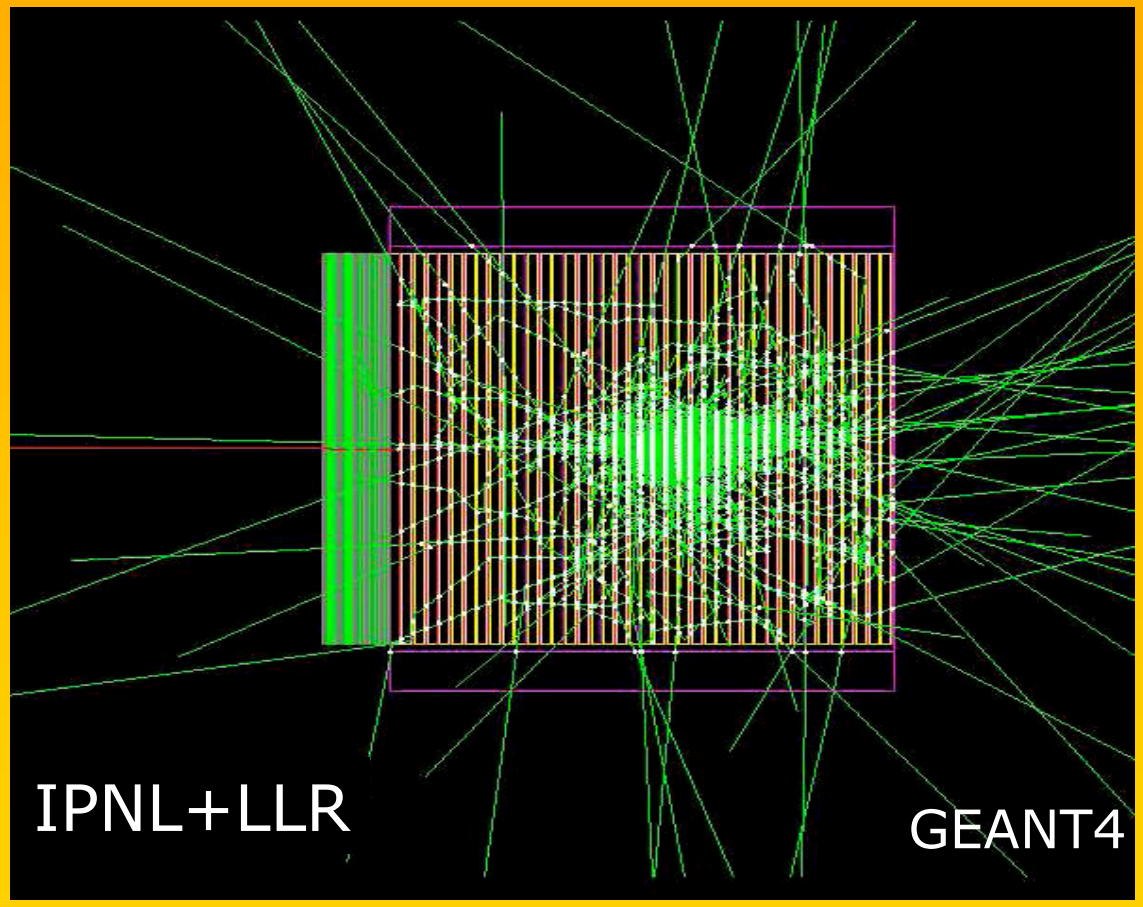






Perspectives

A technological prototype ILC-module0 to be built before 2010



The technological prototype optimization is going on to optimize the design

Conclusions

A digital hadronic calorimeter with semi-digital readout is very promising candidate for future colliders experiments

A slice test based on the semi-digital readout was successfully tested in a laboratory cosmic bench

A beam test is scheduled next months at CERN.

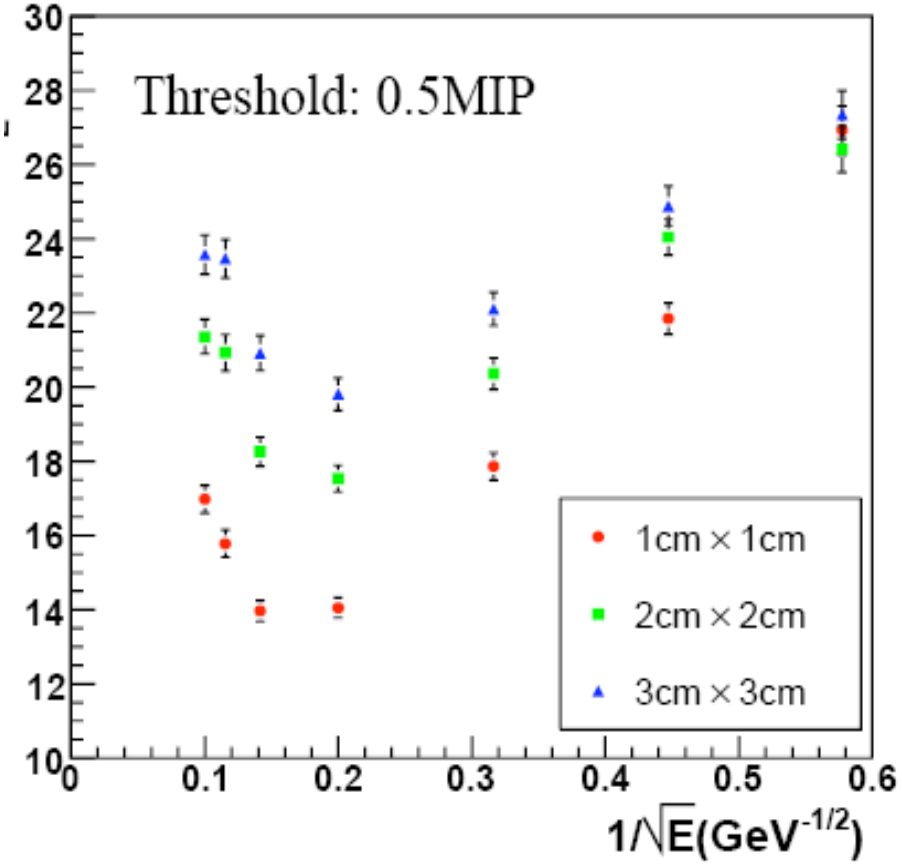
1 m^2 project is ongoing and the first plane is expected before the end of 2008.

A technological prototype is funded and expected in 2009-2010

Back up

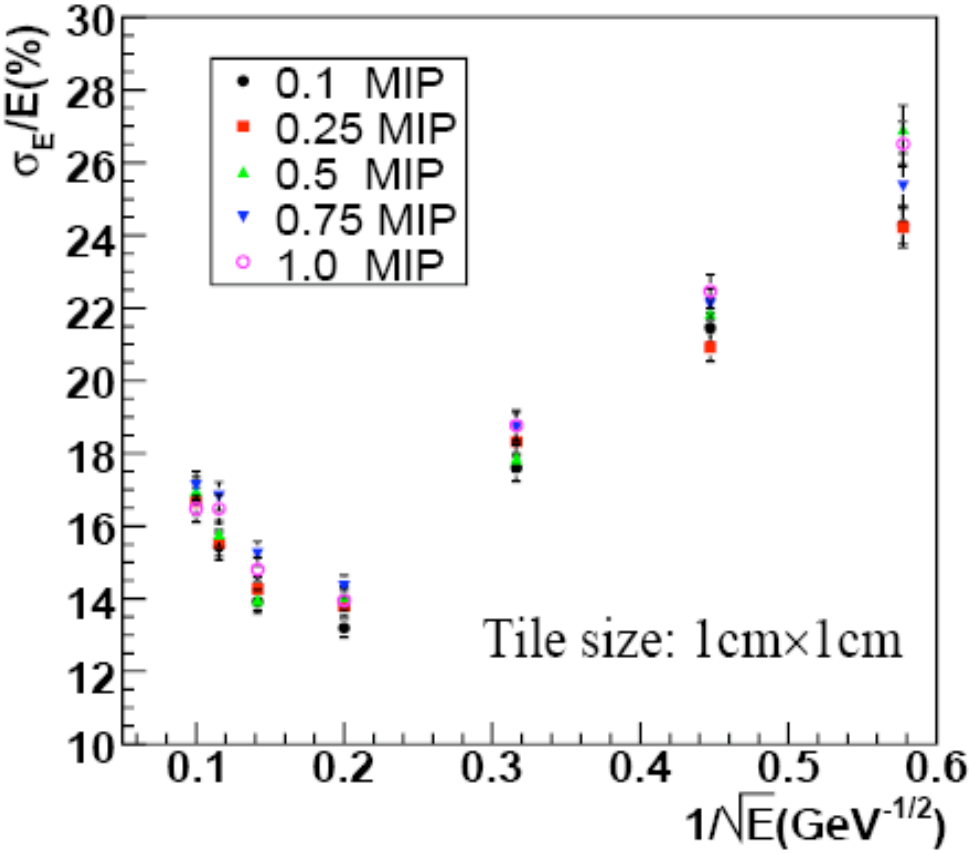
Energy Resolution

Segmentation dependence



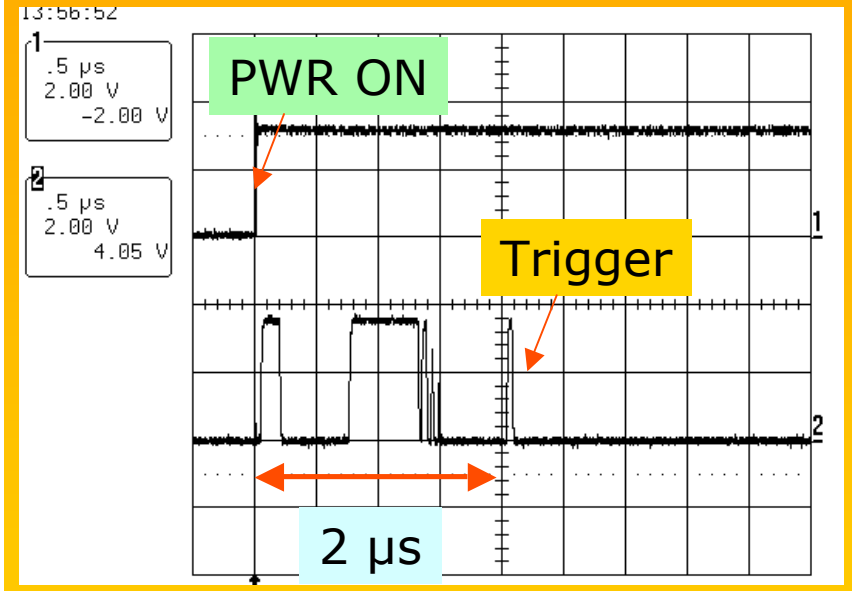
→ Smaller size is better in high energy region

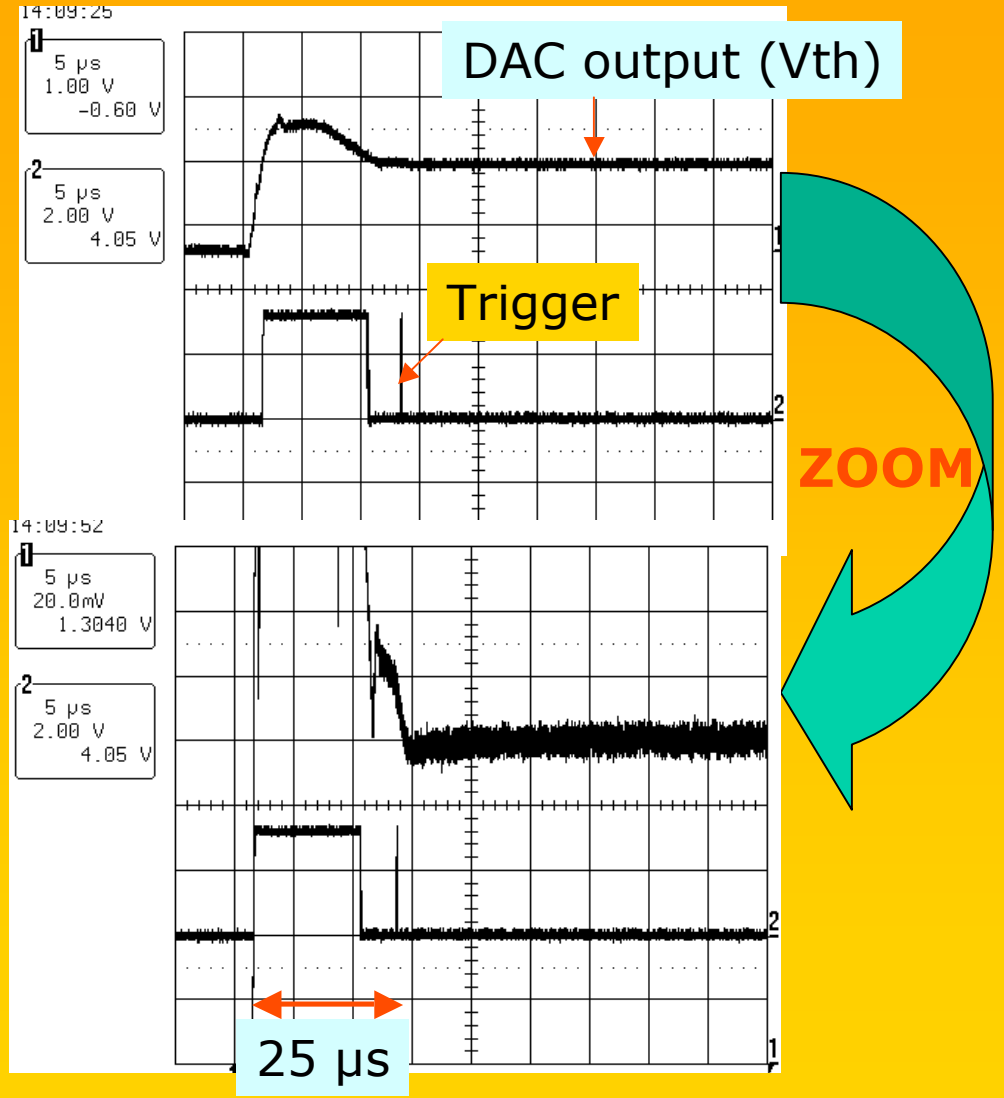
Threshold dependence



→ No significant difference

HARDROC Power pulsing

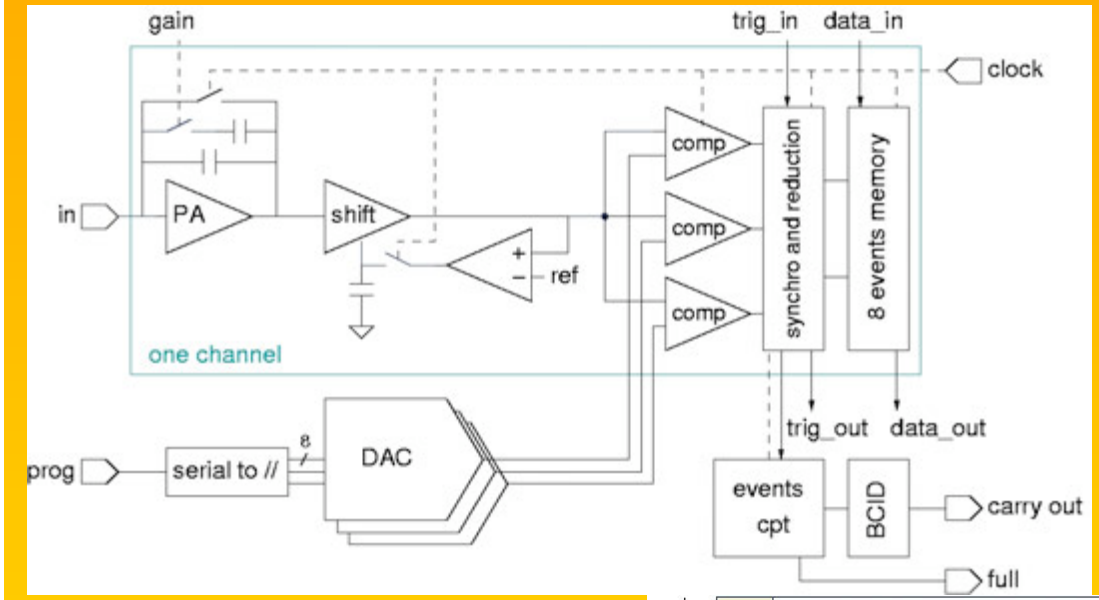




PWR ON: ILC like (1ms,199ms)

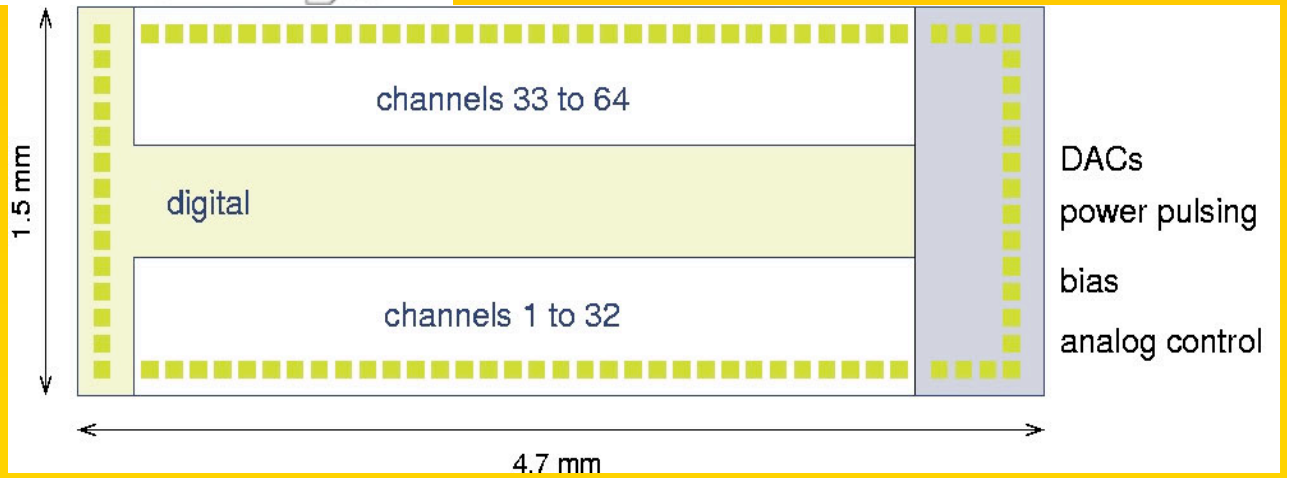
New chip

A new chip with a low threshold for µMEGAS is under development @IPNL

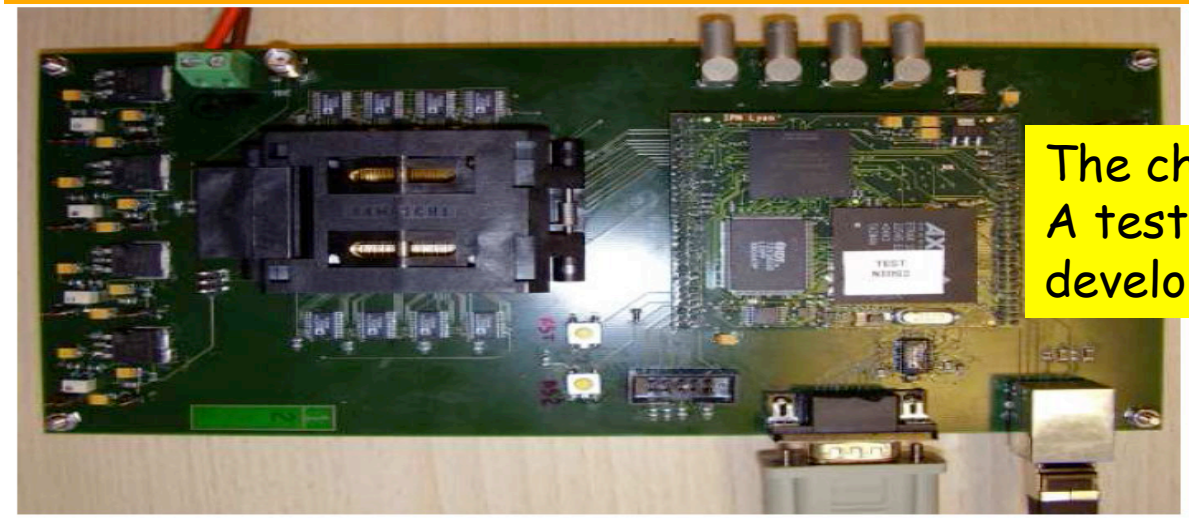


3 DACs (8 bits each)
BCID = 12 bits
memory depth= 8 ev.

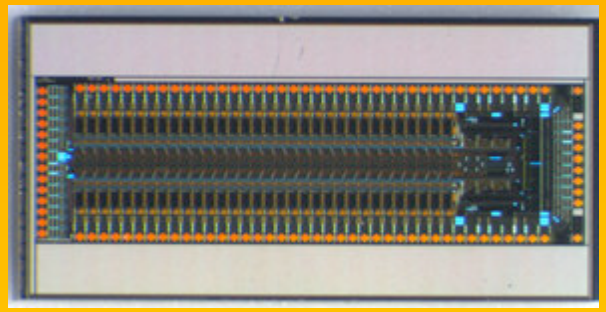
64-ch chip
CMOS tech
power pulsed

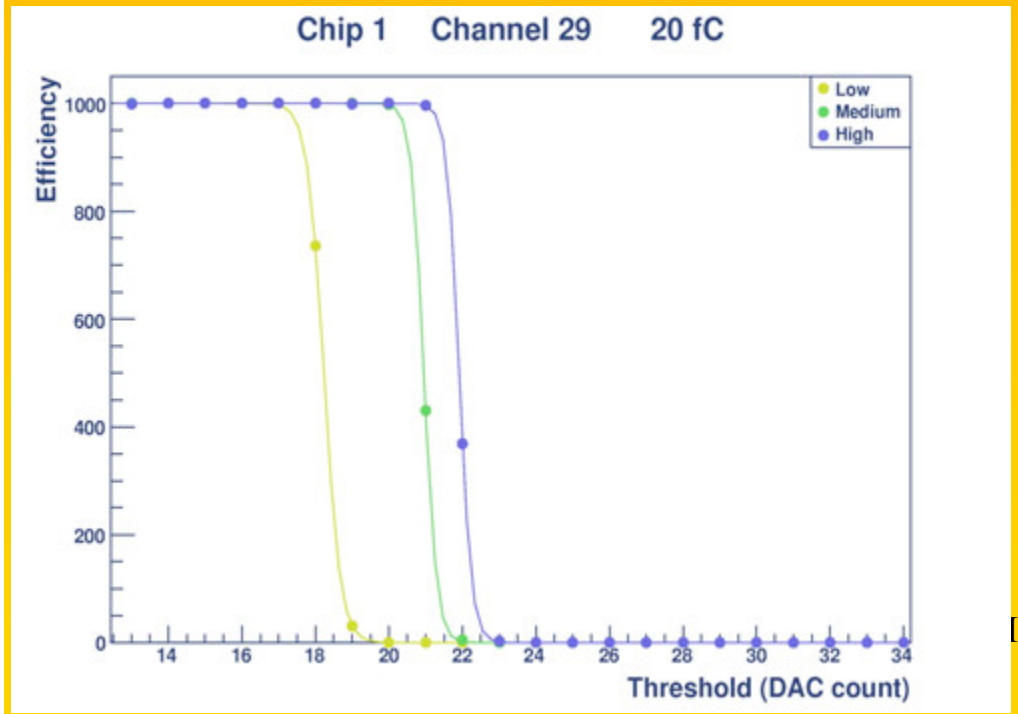


Simple geometry



The chip was designed and produced.
A test board using OPERA DAQ developed @IPNL was used.





First results:
Mode µMEGAS
0.8 fc/DAQ
Resolution < 2.5 fc

Tests and improvement are going on