Second generation ASICS for CALICE/EUDET calorimeters

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on behalf of the CALICE collaboration
ILC Challenges for electronics

- Requirements for electronics
  - Large dynamic range (15 bits)
  - Auto-trigger on ½ MIP
  - On chip zero suppress
  - Front-end embedded in detector
  - Ultra-low power: (25µW/ch)
  - 10^8 channels
  - Compactness
- « Tracker electronics with calorimetric performance »
- No chip = no detector!!

Ultra-low POWER is the KEY issue

ILC: 25µW/ch  
FLC_PHY3 18ch 10x10mm 5mW/ch  
ATLAS LAr FEB 128ch 400x500mm 1W/ch
First generation ASICs

- Readout of physics prototypes (ECAL, AHCAL, DHCAL)
  - Front-end ASICs outside the detector
  - Multiplexed analog output: digitization and readout in DAQ crate
  - FLC_PHY3 for SiW ECAL, FLC_SiPM for AHCAL (BiCMOS 0.8µm [LAL-Orsay]) and DCAL for DHCAL (CMOS 0.25 µm [FNAL])
  - Chips described at CALOR2004 and CALOR2006
  - [see also CALOR08 talks by JC Brient, R. Cornat, J. Repond, F. Sefkow, F. Salvatore & E. Garutti]
CALICE Testbeam at DESY, CERN & FNAL

TCMT

AHCAL (9 000 ch)

W-Si ECAL (9 000 ch)

DHCAL slice test

Imaging calorimetry

Common DAQ
16 000 ch
Second generation ASICs

- Add auto-trigger, analog storage, digitization and token-ring readout !!!
- Include power pulsing : <1 % duty cycle
- Address integration issues asap
- Optimize commonalities within CALICE (readout, DAQ...) [see talk by V. Bartsch]

**FLC_PHY3 (2003)**

**HardROC (2006)**

**SkiROC**

**SPIROC**
Technological prototypes: “EUDET module”

- Front-end ASICs embedded in detector
  - Very high level of integration
  - Ultra-low power with pulsed mode
  - Target « analog friendly » SiGe technology

- All communications via edge
  - 4,000 ch/slab, minimal room, access, power
  - Small data volume (~ few 100 kbyte/s/slab)

- EUDET funding for fab in 2009

- [AHCAL: see talk by F. Sefkow]
- [DHCAL: see talk by I. Laktineh]
EUDET module FEE: main issues

- “stitchchable” motherboards
  - Minimize connections between boards
- No external components
  - Reduce PCB thickness to <800µm
  - Internal supplies decoupling
- Mixed signal issues
  - Digital activity with sensitive analog front-end
- Pulsed power issues
  - Electronics stability
  - Thermal effects
  - To be tested in beam asap
- Low cost and industrialization are the major goal
ECAL detector slab

- Chips bonded on ASU (Active Sensor Units)
- Study connection between ASUs
Read out: token ring

- Readout architecture common to all calorimeters
- Minimize data lines & power

Data bus

Chip 0
- Acquisition
- A/D conv.
- DAQ
- IDLE MODE

Chip 1
- Acquisition
- A/D conv.
- IDLE
- DAQ
- IDLE MODE

Chip 2
- Acquisition
- A/D conv.
- IDLE
- IDLE MODE

Chip 3
- Acquisition
- A/D conv.
- IDLE
- IDLE MODE

Chip 4
- Acquisition
- A/D conv.
- IDLE
- DAQ
- IDLE MODE

1% duty cycle
- 1ms (.5%)

99% duty cycle
- 199ms (99%)
The front-end ASICs: the ROC chips

**SPIROC**
- Analog HCAL (SiPM)
- 36 ch. 32mm²
- June 07

**HARDROC**
- Digital HCAL (RPC, µmegas or GEMs)
- 64 ch. 16mm²
- Sept 06

**SKIROC**
- ECAL (Si PIN diode)
- 36 ch. 20mm²
- Nov 06
DHCAL chip: HaRDROC

- Hadronic Rpc Detector Read Out Chip (Sept 06)
  - 64 inputs, preamp + shaper + 2 discris + memory + Full power pulsing
  - Compatible with 1st and 2nd generation DAQ: token ring readout of up to 100 chips
  - 1st test of 2nd generation DAQ and detector integration

- Collaboration with IPNL/LLR/Madrid/Protvino/
  - 1m³ scalable detector
  - [see talk by I. Laktineh]
  - Production of 5000 chips in 2009
HaRDROCs architecture

- Variable gain (6 bits) current preamps (50 ohm input)
- One multiplexed analog output (12 bit)
- Auto-trigger on ½ MIP
- Store all channels and BCID for every hit. Depth = 128 bits
- Data format: 128(depth)[2bit*64ch +24bit(BCID)+8bit(Header)] = 20kbits
- Power dissipation: 1.5 mW/ch (unpulsed) -> >15µW with 1% cycle
- Large flexibility via >500 slow control settings
S-curves of 64 channels

- 10 bit DAC for threshold,
- Noise \( \sim 1 \text{ UDAC (2mV)} \)
- Pedestal dispersion : 0.4 UDAC rms
- Gain dispersion 3% rms
- Crosstalk : < 2%

![Diagram showing S-curves and 50% trigger versus channel number]
Power pulsing: «Awake» time

- PWR ON: ILC like (1ms, 199ms)
- All decoupling capacitors removed: difficult compromise between noise filtering and fast awake time
- Awake time:
  - Analog part = 2 µs
  - DAC part = 25 µs
- 0.5% duty cycle achieved, now to be tested at system level
SKIROC for W-Si ECAL

- Silicon Kalorimeter Integrated Read Out Chip (Nov 06)
  - 36 channels with 15 bits Preamp + bi-gain shaper + autotrigger + analog memory + Wilkinson ADC
  - Digital part outside in a FPGA for lack of time and increased flexibility
  - Technology SiGe 0.35µm AMS. Chip received may 07

1 MIP in SKIROC
12 bit Wilkinson ADC performance

**Pedestal value vs Channel number**

**Noise in low gain shaper**

- $r_m = 0.9 U_{ADC}$
- $MIP = 3 U_{ADC}$

**Noise vs Channel number**

**Noise in high gain shaper**

- $r_m = 4 U_{ADC}$
- $MIP = 30 U_{ADC}$
AHCAL chip: SPIROC

- Silicon Photomultiplier Integrated Read Out Chip
  - A-HCAL read out
  - Silicon PM detector G=10^5-10^6
  - 36 channels
  - Charge measurement (15bits)
  - Time measurement (<1ns)
  - many SKIROC, HARDROC, and MAROC features re-used
  - Submitted in June 07 in SiGe 0.35 µm AMS

- Collaboration with DESY
  - Production in 2009 for Eudet module
  - [see talk by F. Sefkow]
SPIROC main features

- Internal input 8-bit DAC (0-5V) for SiPM gain adjustment
- Energy measurement:
  - 2 gains / 12 bit ADC 1 pe → 2000 pe
  - Variable shaping time from 50ns to 100ns
  - pe/noise ratio : 11
- Auto-trigger on ½ pe
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~15ns
  - Auto-Trigger on ½ pe
- Time measurement : 12 bit TDC step~100 ps
- Analog memory for time and charge measurement : depth = 16
- Low consumption : ~25µW per channel (in power pulsing mode)
- Calibration injection capacitance
- Embedded bandgap for voltage references
- Embedded DAC for trigger threshold
- Compatible with physic prototype DAQ
  - Serial analogue output
  - External “force trigger”
- 12-bit Bunch Crossing ID
- SRAM with data formatting 2 x 2kbytes = 4kbytes
- Output & control with daisy-chain
SPIROC: one channel

- Slow Shaper
  - 50-100ns
- Fast Shaper
  - 15ns
- Gain selection
- Charge measurement
- Time measurement
- 12-bit Wilkinson ADC
- Conversion 80 µs
- Analog output

- Low gain Preamplifier
  - 1.5pF
- High gain Preamplifier
  - 15pF

- Analog memory

- 8-bit DAC
  - 0-5V

- 10-bit DAC
  - TDC ramp 300ns/5 µs
  - Common to the 36 channels

- 4-bit threshold adjustment

- Variable delay

- Flag TDC

- Trigger
  - Depth 16

- Hold

- Read
Chip ID register 8 bits

Gain

Trigger discriminator output

Wilkinson ADC

Discri output

StartRamp (Discri ADC Wilkinson)

EndRamp (Discri ADC Wilkinson)

ValGain (low gain or high Gain)

ExtSigmaTM (OR36)

Hit channel register 16 x 36 x 1 bits

BCID 16 x 8 bits

Conversion

ADC

Ecriture

RAM

ADC ramp

TDC ramp

ValidHoldAnalog

RazRampN

ReadMesureb

Chip ID register 8 bits

ValDimGray 12 bits

ValDimGray 12 bits

ChipID

StartRamp (wilkinson ramp)

StartRampb

Startrampb (wilkinson ramp)

StartAcqt

StartConvDAQb

Rstb

Clk40MHz

RAM

TransmitOn

EndReadOut

ChipID

StartAcqt

StartReadOut

StartConvDAQb

StartReadOut

StartConvDAQb

RamFull

OutSerie

NoTrig

StartAcqt

StartReadOut

Chipsat
SPIROC performance

- Good analog performance
  - Single photo-electron/noise = 8
  - Auto-trigger with good uniformity
  - Complex chip: many more measurements needed

S-curves

# events vs SPIROC out (mV)

trigger efficiency vs DAC value
Power supplies issues

- A very critical issue !!! As usual, noone’s looking...
- Power supplies won’t be dimensionned for continuous operation, but for 1/100 of the load. Total power : ~2kW, peak value ~200kW !!
- Need local storage (capacitors, even a battery!) on power board and regulators to accomodate large voltage swing
- Simple calculation (ECAL)
  - Slab = 24 000 channels
  - 1 mA/channel unpulsed => 24 A/slab peak, 240mA average
  - With a 24 000µF capacitor \( \frac{dV}{dt} = 1\text{V/ms} \Rightarrow \text{acceptable} \)
Conclusion

- Good progress on 2\textsuperscript{nd} generation ASICs
  - Power pulsing
  - Token-ring readout
  - Integration inside detector
  - Low noise/Large dynamic range

- Production foreseen beg 2009 for technological prototypes
  - Still many integration issues to be studied
  - Crucial for detector feasibility

- 3rd generation chips still to come
  - Alternative ADC designs
  - All channels treated independantly
Multi Project Run vs Dedicated Run

• **MPW: $1k€/mm^2$** => Hardroc= **25 k€**
  - 25 dies delivered in September 08, to be packaged
  - About 300 dies available (no guaranty): 100 euros/die + packaging
  - Price: **25 k€ + 100 € * nb_chips**

• **Engineering run:**
  - Wafer 8” Available area=23 000 mm²
  - 1 reticle=20x20 mm²=400 mm²
  - => 65 reticles/wafer
  - 16 chips (25 mm²) / reticle => 1000 Hardroc/wafer
  - Cost: **150 k€ (masks) + 5k€/wafer**
  - Price: **150 k€ + 5 € * nb_chips**
  - valuable for more than 1250 chips
Digital part

- Full daisy-chain readout
  - Internal or external Trigger
  - OR36 output
  - Discriminator
  - Validation fast input
  - 4kbyte RAM
  - "Open collector" output signals
  - LVDS clocks
  - Start conversion
  - Start/end readout