The SuperB Silicon Vertex Tracker

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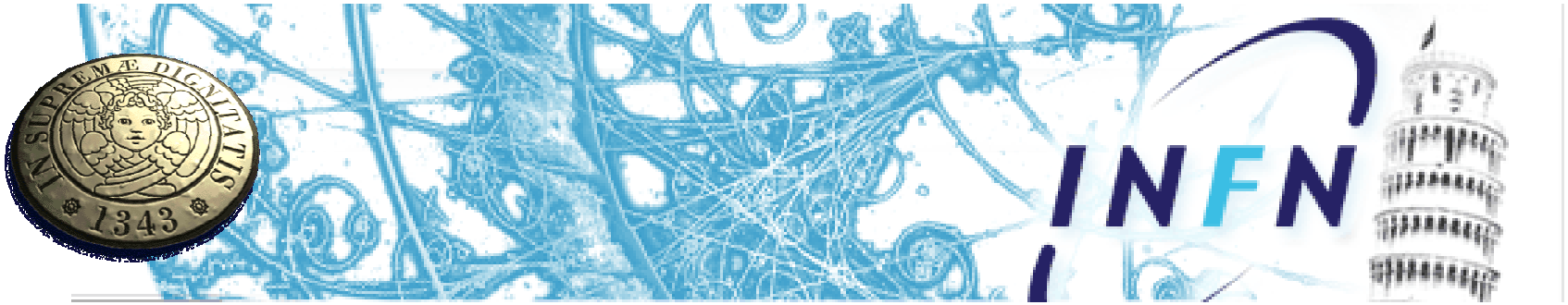


on behalf of the SuperB-SVT group

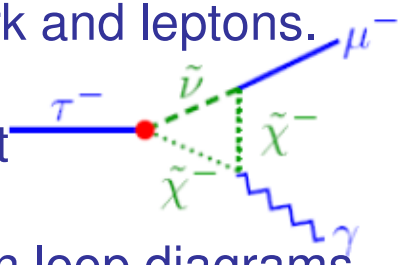
10th International Conference on Large Scale Applications and Radiation Hardness of Semiconductor Detectors – Florence, 8 July 2011

OUTLINE

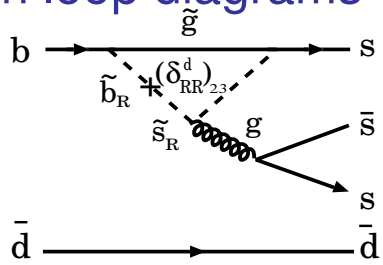
- The SuperB project
- The design of the SVT
  - Physics requirements
  - Current layout
- FE chip for all the layers
- Layer0:
  - Striplets
  - Pixels:
    - Hybrid pixels
    - DNW MAPS
    - V.I. (advanced 3D solutions)
    - mechanics
- Conclusions

Physics program clearly estabilished

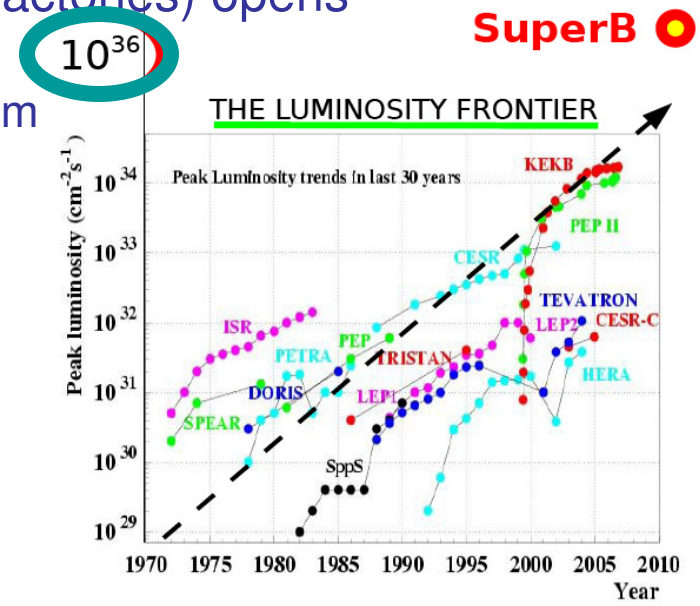
- Main motivation for a new generation of e+e- experiments:
measure the effects of New Physics on the decays of heavy quark and leptons.



- High luminosity is crucial to reach the sensitivity needed to set constraints on the models of the NP by flavour physics.
- Search for the effects of physics beyond the standard model in loop diagrams
  - Potentially large effects on rates of rare decays,
  time dependent asymmetries, lepton flavour violation, …
  - Sensitive even to large New Physics scale,
  as well as to phases and size of NP coupling constants



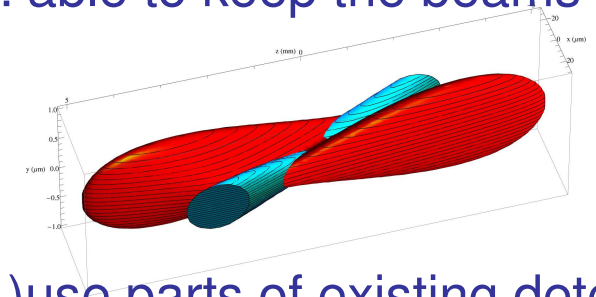
- A luminosity of 50 – 100 ab^{-1} (x 100 than past B-Factories) opens windows on NP:
  - Precision measurements to detect discrepancies from the standard model
  - Rare decay measurements
  - Lepton flavour violation
  - CP violation in Charm
  - Unique feature: Polarized e- beam
  - Possibility to run at tau/charm threshold



- Complementarity and synergy with LHC program.

The SuperB project: approval and site

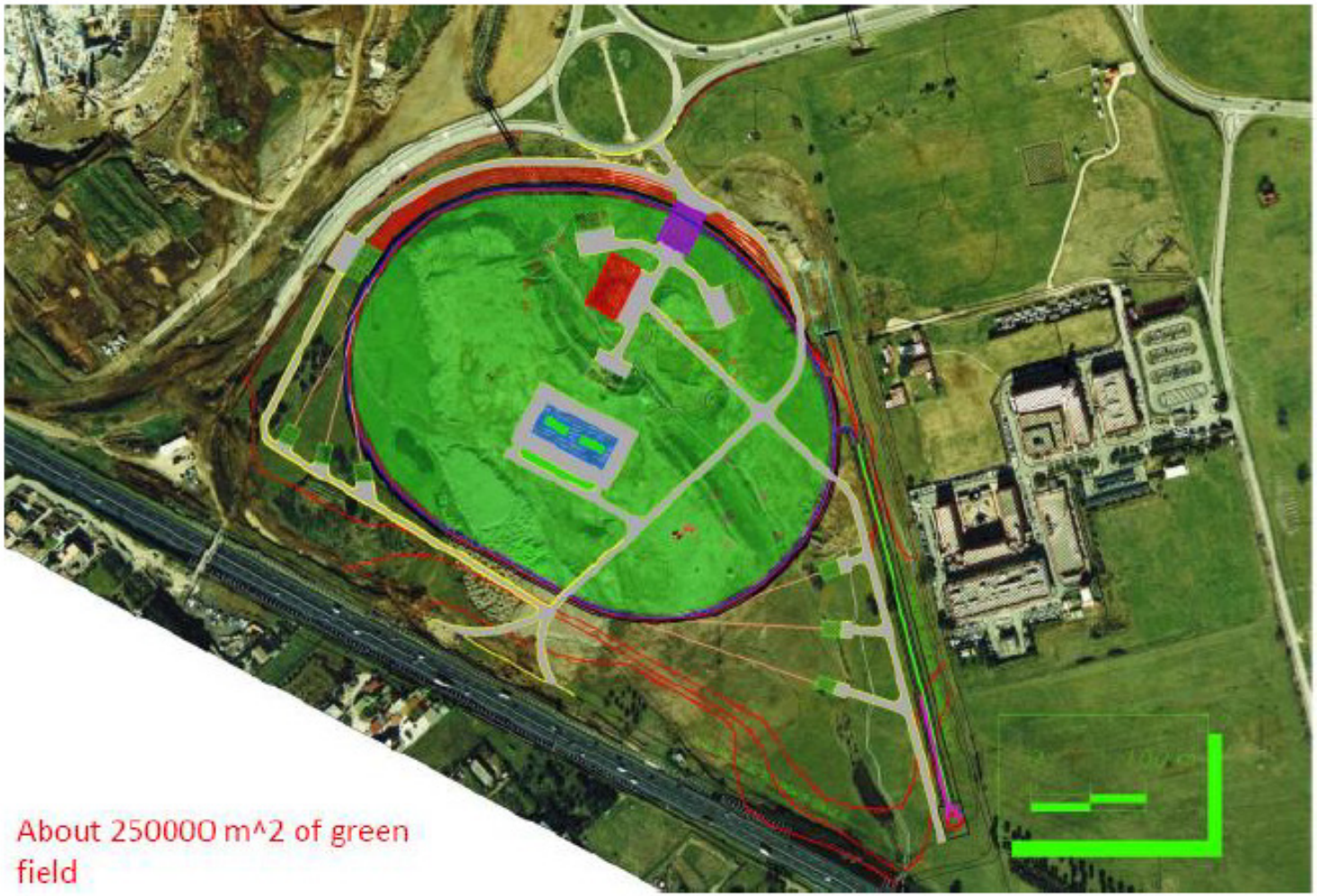
- SuperB has been approved by the Italian Government as the first in a list of 14 “flagship” projects within the new national research plan.
- The SuperB Italian accelerator concept allows to reach **L** $=10^{36}\,cm^{-2}\,s^{-1}$ with moderate beam current (2A). Very small beam size (~1/100 of past B-Factories beams) can be obtained by exploiting the ILC R&D on damping rings & final focus, with the help of the Crab Waist scheme at the IP. Verified with tests on Dafne: able to keep the beams small & stable after collision.



- This approach allows to (re-)use parts of existing detectors and machine components.
- A financial allocation of 250 Million Euros in about 5 years approved for the “superb flavour factory”.
- The site was decided: SuperB will be built in the campus of the Tor Vergata University (near Rome).
- Beam lines for synchrotron light (very high brightness) experiments will be available at the SuperB facility (I.I.T. interested).
- Collaboration forming since Elba meeting (May 2011).
- First collisions expected in mid 2016.

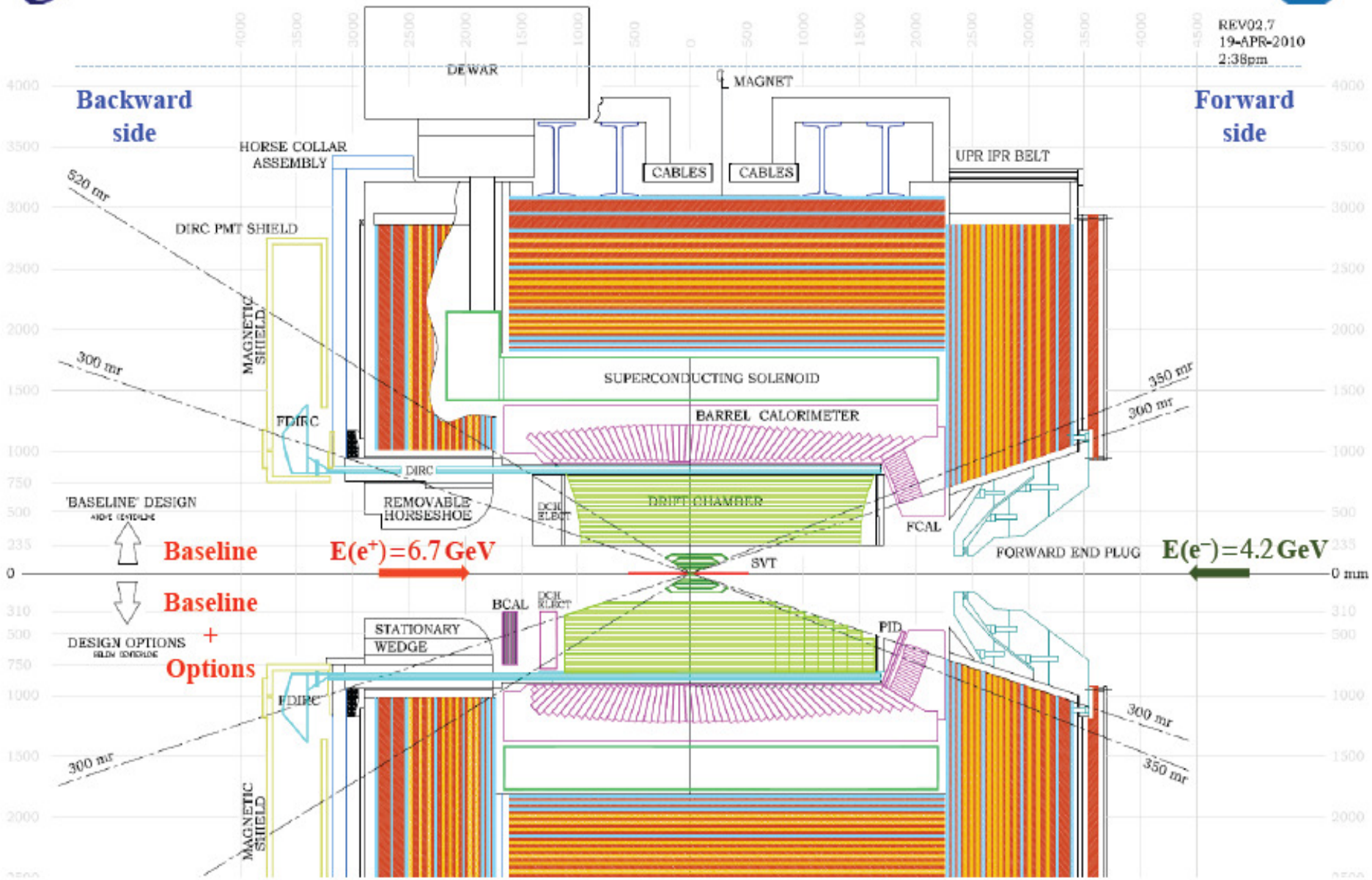
Site (Tor Vergata)

Cabibbo Lab.



In april 2011, a campaign of one week of vibration measurements: amplitude < 1 um, even in rush hours → not a problem!

SuperB Detector (with options)

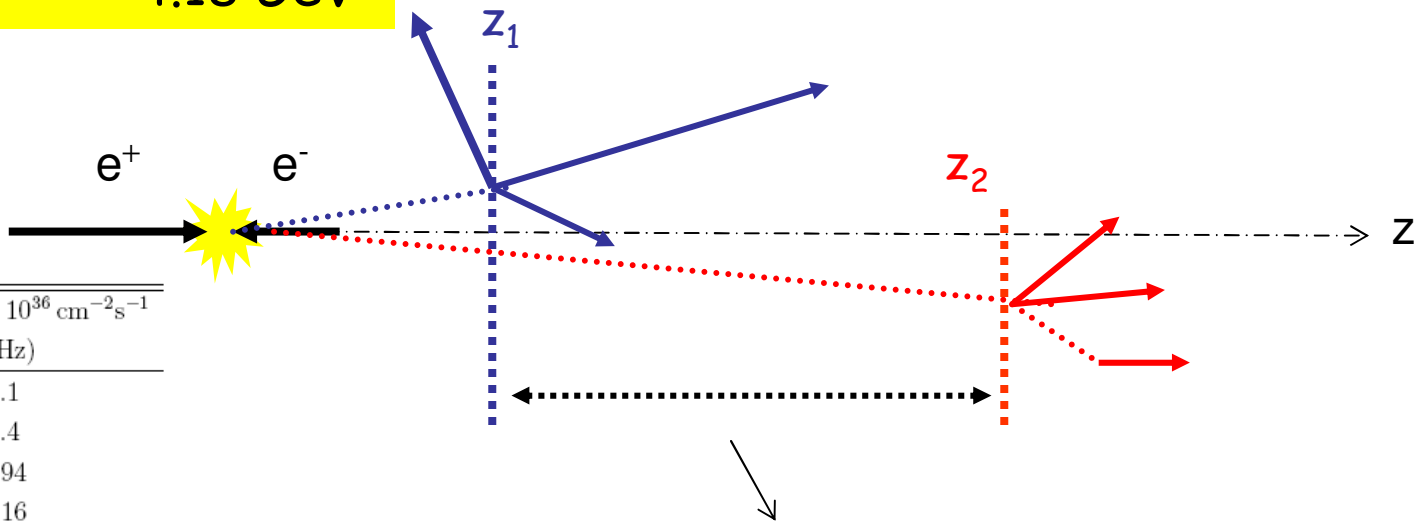


Time dependent measurements

$$e^+e^- \rightarrow \Upsilon(4s) \rightarrow B^0\overline{B^0}$$ (coherent production)

	Babar	SuperB
< Δz >	≈ 260 μm	≈ 130 μm
E (e+)	9 GeV	6.7 GeV
E (e-)	3.1 GeV	4.18 GeV

Vertex precision must be improved by a factor of 2 @ SuperB



Process	Rate at $\mathcal{L} = 10^{36}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ (kHz)
$\Upsilon(4S)\ to B\bar{B}$	1.1
$udsc$ continuum	3.4
$\tau^+\tau^-$	0.94
$\mu^+\mu^-$	1.16
e^+e^- for $\lvert\cos\theta_{\mathrm{Lab}}\rvert < 0.95$	30

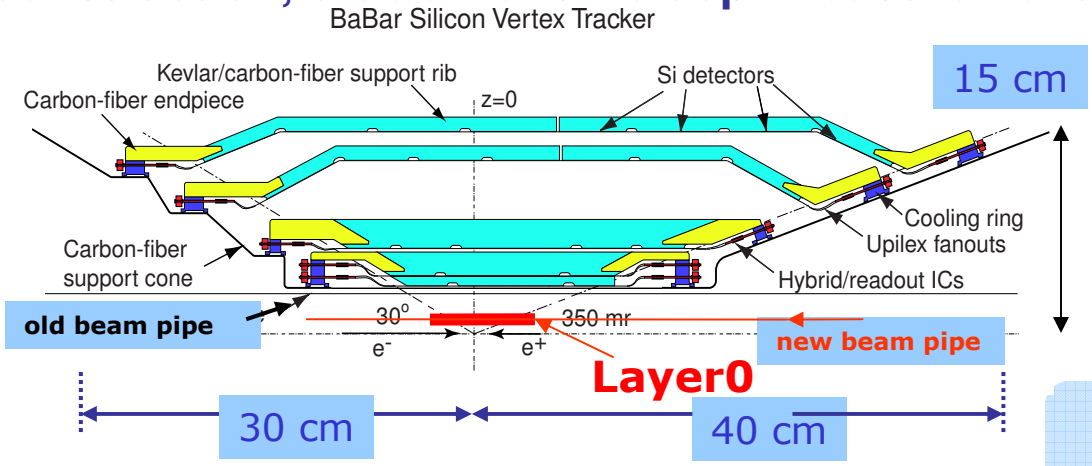
$$\Delta t = \frac{\Delta z}{c\gamma\beta} = \frac{z_2 - z_1}{c\gamma\beta}$$

15 ab^{-1}/y => **75 ab^{-1}** (5 years data taking)

- 0.8x10^{11} **B-B**bar pairs
- 1.0x10^{11} **c-c**bar pairs
- 0.7x10^{11} $\tau^+\tau^-$ pairs

The SuperB Silicon Vertex Tracker

The SVT provides precise tracking and vertex reconstruction, crucial for time dep. measurements.

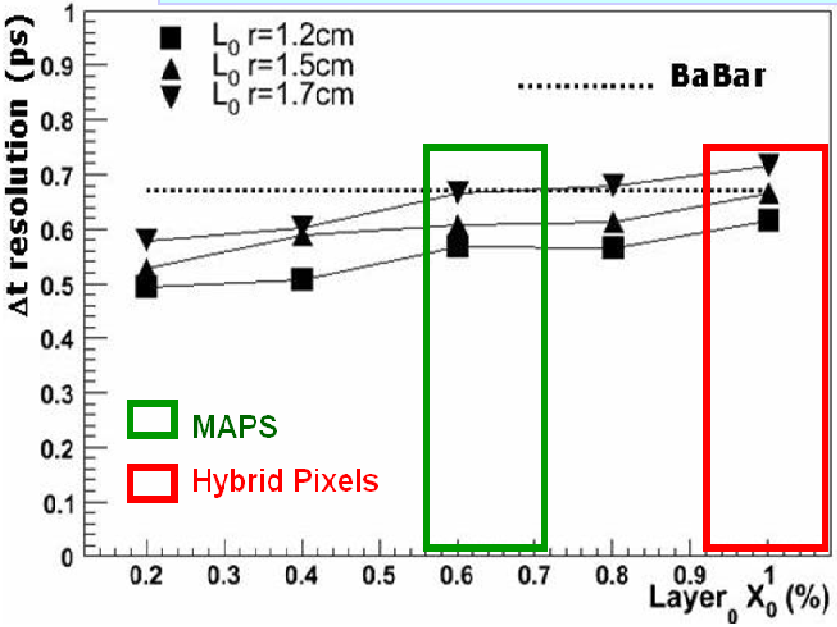


BaBar SVT

- 5 Layers of double-sided Si strip sensors
- Low-mass design
- Stand-alone tracking for soft particles.
- 97 % reconstruction efficiency
- Resolution: ~15μm at ⊥ incidence

SuperB SVT based on Babar SVT design:

B→π π decay mode, βγ=0.28, beam pipe X/X0=0.42%, hit resolution =10 μm



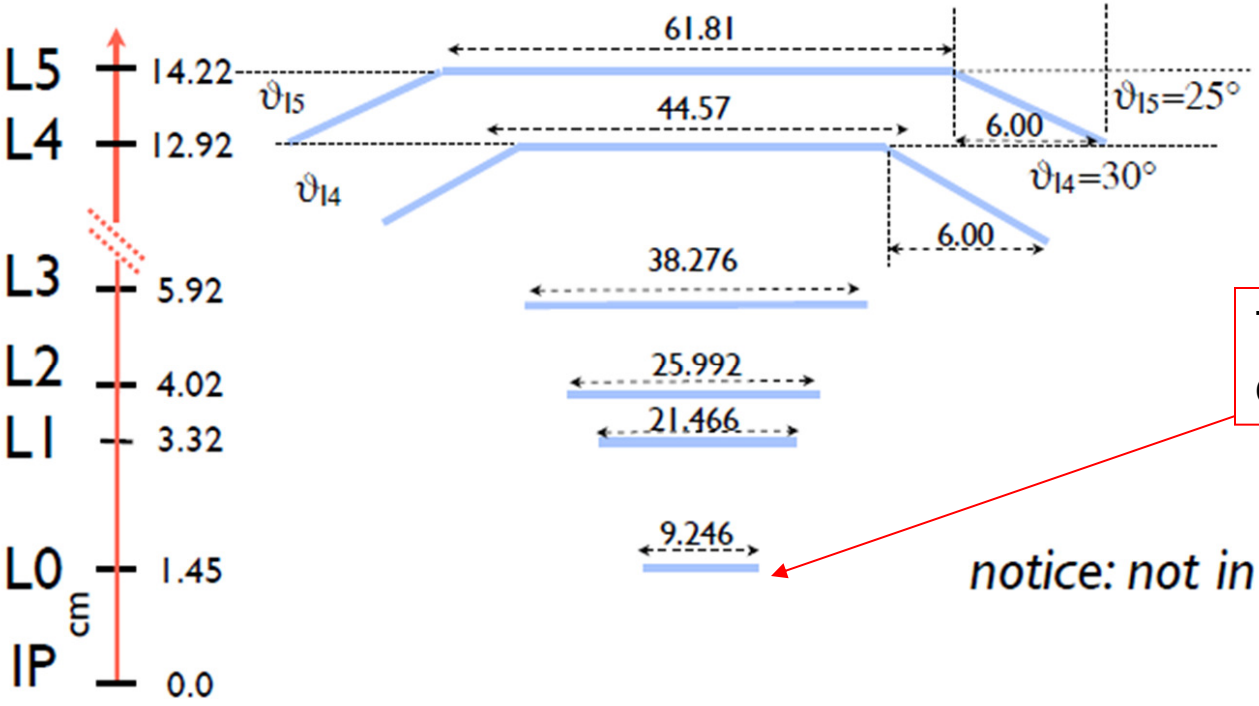
1) reduced beam energy asymmetry (6.7x4.2 GeV vs. 9x3.1 GeV) requires an improved vertex resolution:

- Layer0 very close to IP (@1.5 cm) with low material budget (<1% X_0) and fine granularity (50 μm pitch)
- Layer0 area 100 cm^2

2) bkg level depends steeply on radius

- Layer0 needs to be fast and rad hard (>20x5 MHz/cm^2, >3x5 MRad/yr)

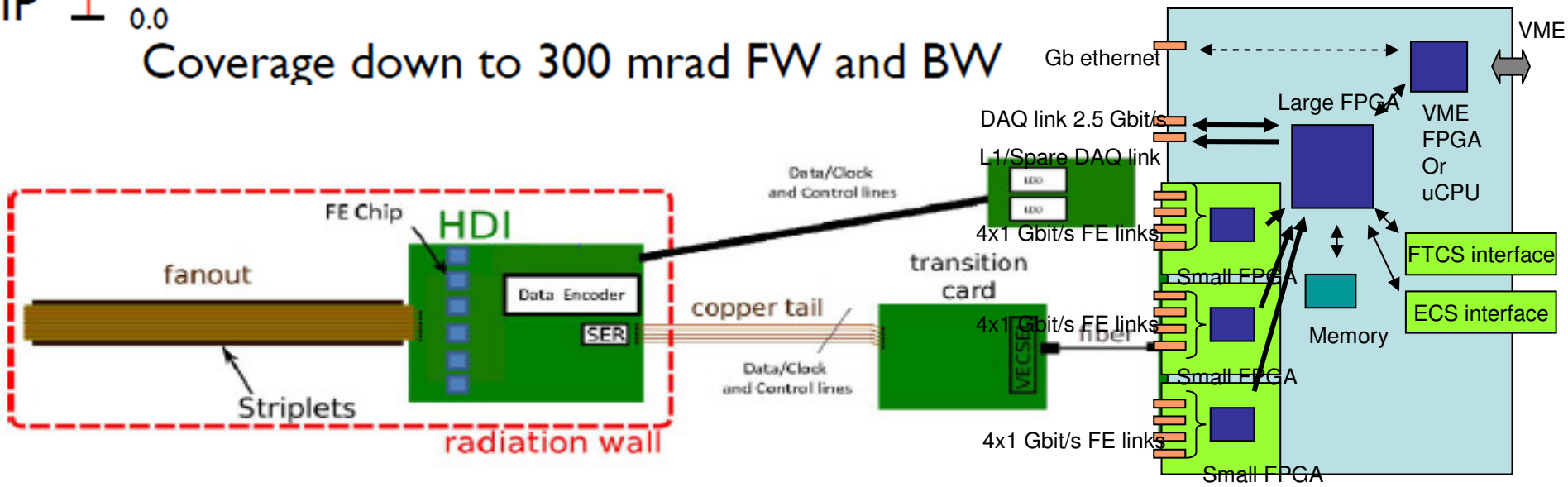
The SuperB SVT geometry



The Layer0 is the most challenging part of the SVT

notice: not in scale

Coverage down to 300 mrad FW and BW



The DAQ chain

The SVT strategy & timeline

- The SuperB TDR to be written by spring 2012
- SVT starts construction phase after TDR:
  - Baseline: striplets in Layer0 @ R~1.5 cm + 5 layers of silicon strip modules (with 300mrad coverage)

Construction phases (from the BaBar experience):
- Design & prototype: 2012
- Procure and Fabricate (+test): 2013-14
- Module Assembly & Det. Assembly: 2015
- Det. commissioning: 2016

- Upgrade Layer0 to thin pixel for full luminosity run(~2 years after first data)
  - more robust against background occupancy
  - SVT Mechanics will be designed to allow a quick access/removal of Layer0
  - Several pixel options still open & under development: R&D continue in 2012 after TDR → decision on pixel technology in 2013
    - CMOS MAPS: continue R&D on readout speed and radiation hardness
    - Hybrid Pixels: FE chip development 50x50 um pitch with fast readout and R&D on reduction of the total (module) material budget below 1% X_0.

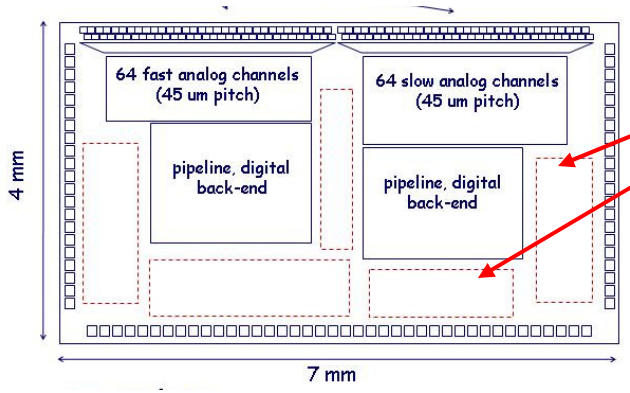
Despite the huge amount of work in the process of engineering the SVT project, in this talk I will focus on a selection of the most challenging aspects…

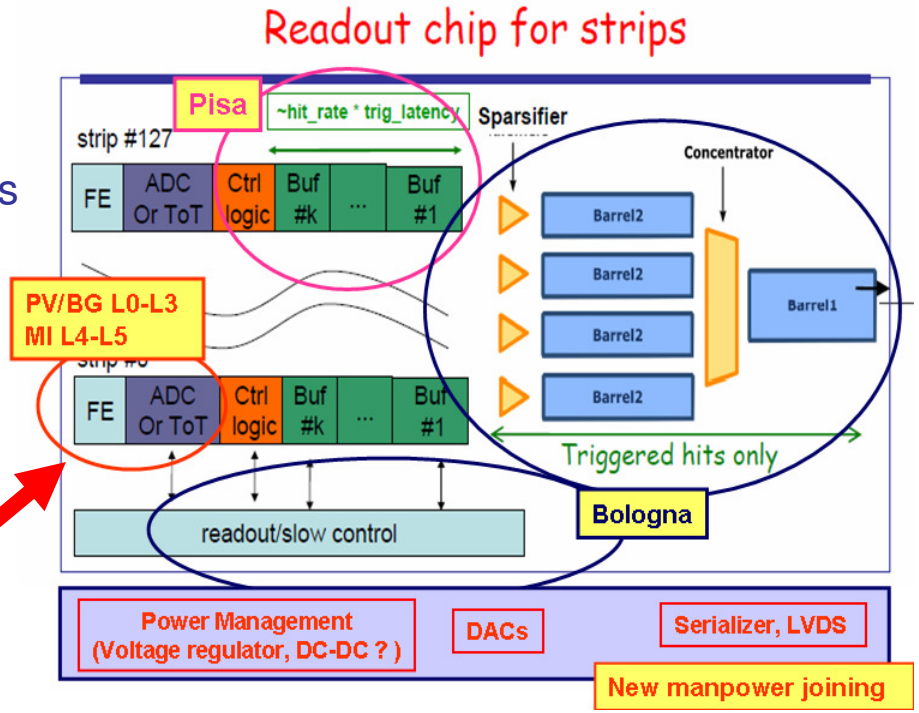
FE chip for strip/striplets

Current Plan:

- Defined the requirements for all the strip modules
- Need to develop 2 new chips (existent chips do not match all the requirements):
  - pulse height info (for dE/dx measurements)
  - very high rates in the inner Layers (up to 2 MHz/strip in Layer0) & short shaping time (25 -100ns)
  - long shaping time (0.5-1 us) in Layers 4-5 to reduce noise for long modules
- For strip readout chips adapt the readout architecture developed for pixel.

- First studies performed and no evident showstopper up to now. Full VHDL simulation of the chips for TDR
- Responsibility:
  - Analog front-end: fast channels for L0-L3 PV/BG, slow channels L4-L5 MI
  - Control Logic-in strip: PI
  - Readout architecture: BO
  - Auxiliary blocks: power management(V regulators, DC-DC,…), DACs, serializer, LVDS. Investigate use of blocks developed by CERN IBM 130 nm (all groups + cern support)



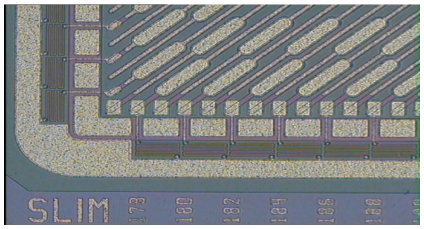


- Milestones for strip front-end development
- 2012: first test structures - 2 x 64 channels (fast and slow front-end), auxiliary blocks
- 2013: first fully operational prototype chip - 2 x 128 channels (fast and slow readout)
- 2014: production run
- Account for some contingency after the first or the second step

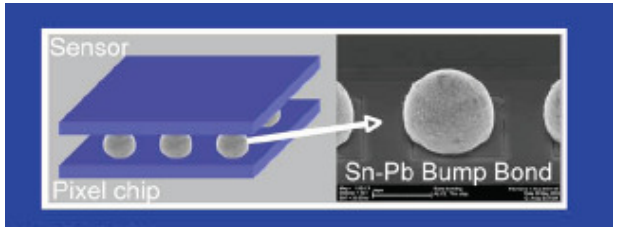
SuperB SVT Layer 0 technology options

Complexity

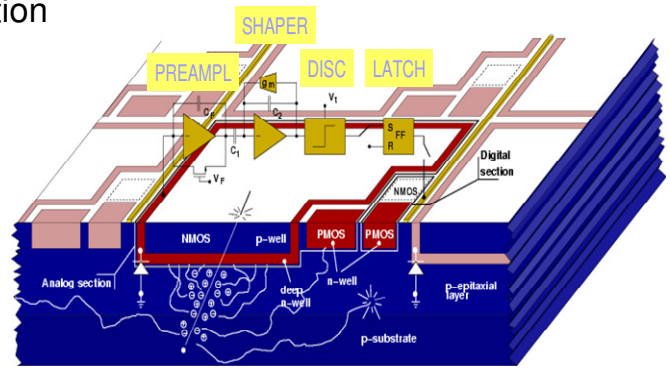
- **Striplets option:** mature technology, not so robust against background occupancy
  - Det's already tested with beam (2008)
  - Marginal with background rate higher than ~5 MHz/cm^2
  - Low material budget, but module design quite complex and new FE chip development needed.



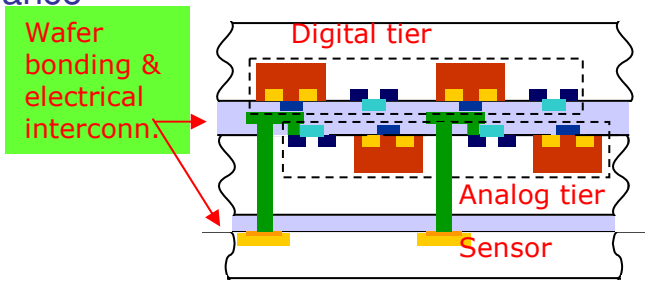
- **Hybrid Pixel option:** viable with some R&D. Slightly marginal because of material budget
  - FE chip with 50x50 μm^2 pitch and fast readout architecture under development
  - Pixel module design with ~ 1%X_0 with present technology: further reduction of total material:FE chip, sensor, pixel bus under evaluation



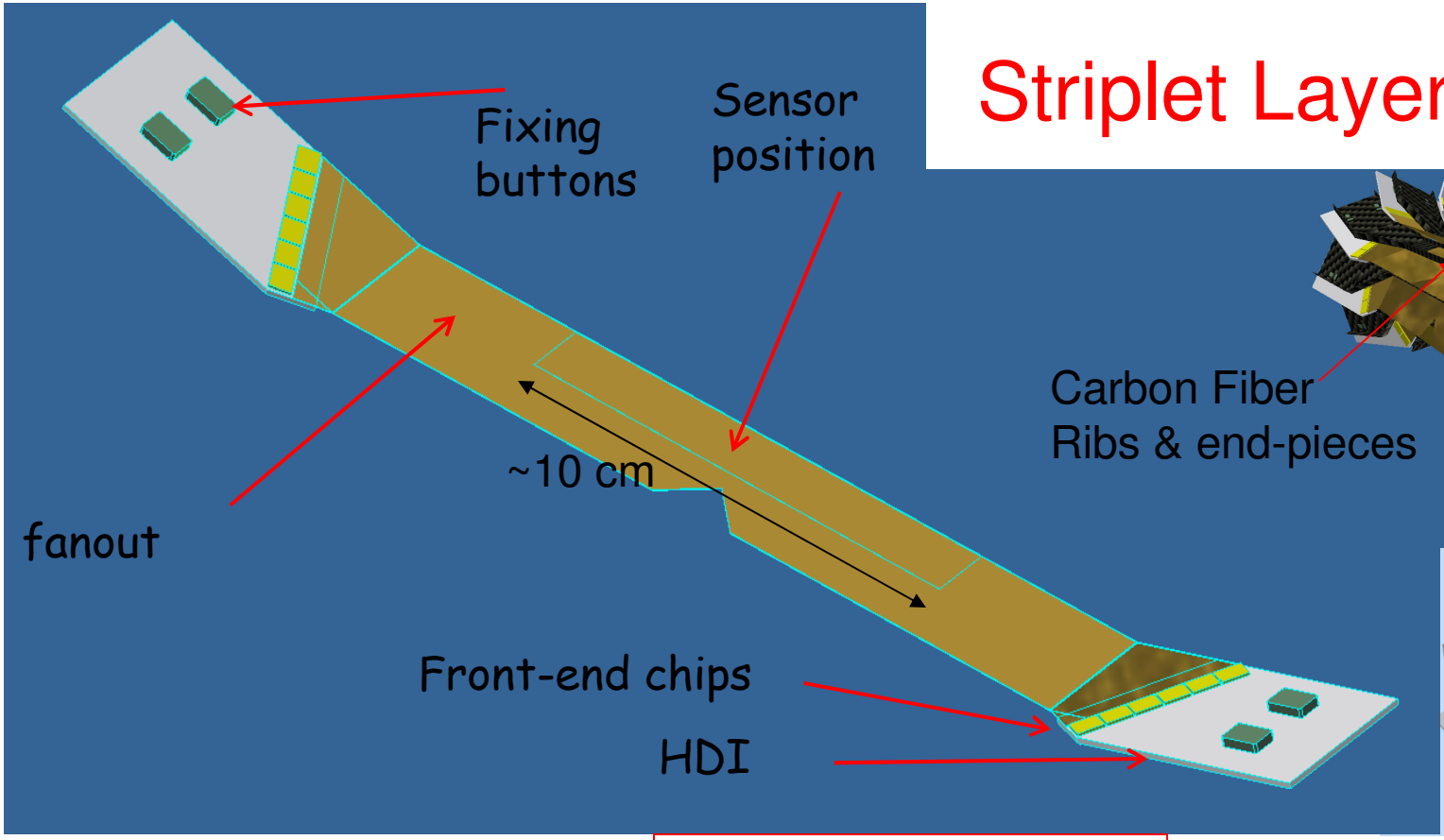
- **CMOS MAPS option:** new & challenging technology. Can they be made fast and rad-hard?
  - Sensor & readout in 50 μm thick chip!
  - Extensive R&D (SLIM5-Collaboration) on
    - Deep N-well devices 50x50μm^2 with in-pixel sparsification.
    - Fast readout architecture implemented
  - CMOS MAPS (4k pixels) successfully tested with beam.

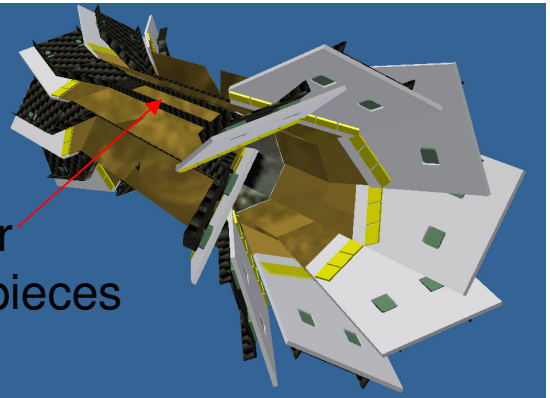


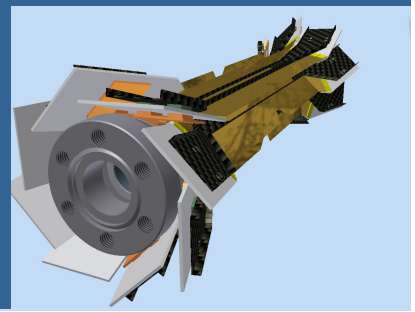
- **Thin pixels with Vertical (3D) Integration:** great performance breakthrough appears possible: reduction of material and improved performance.
  Is the R&D timescale compatible with the SuperB schedule?
  - Two options are being pursued (VIPIX-Collaboration)
    - DNW MAPS with 2 tiers
    - Hybrid Pixel: FE chip with 2 tiers + high resistivity sensor

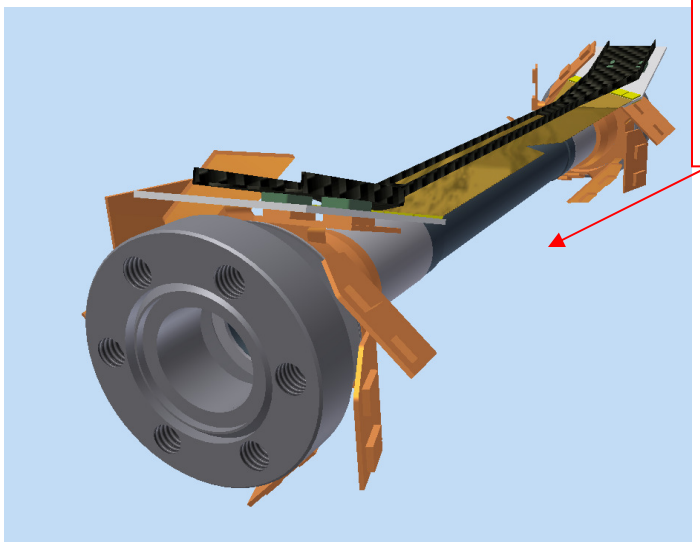


Striplet Layer0 module



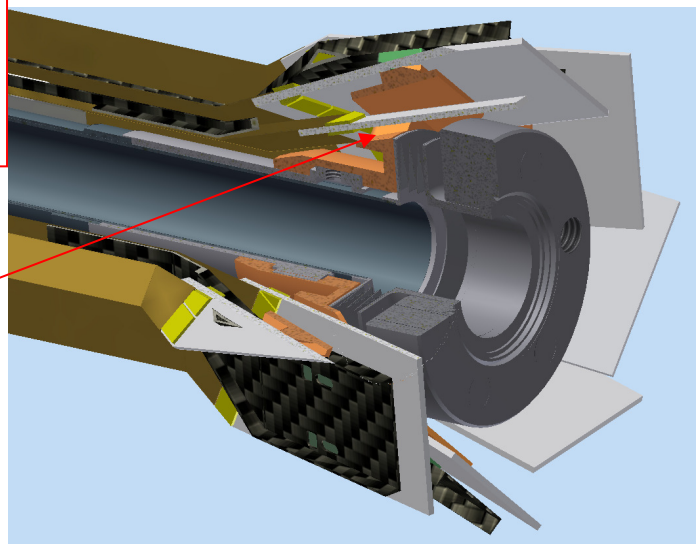






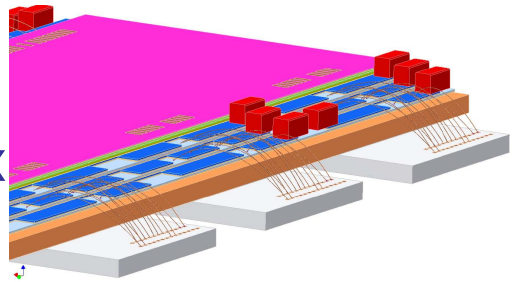
Striplet module positioned on the cold flanges with the Be beam-pipe

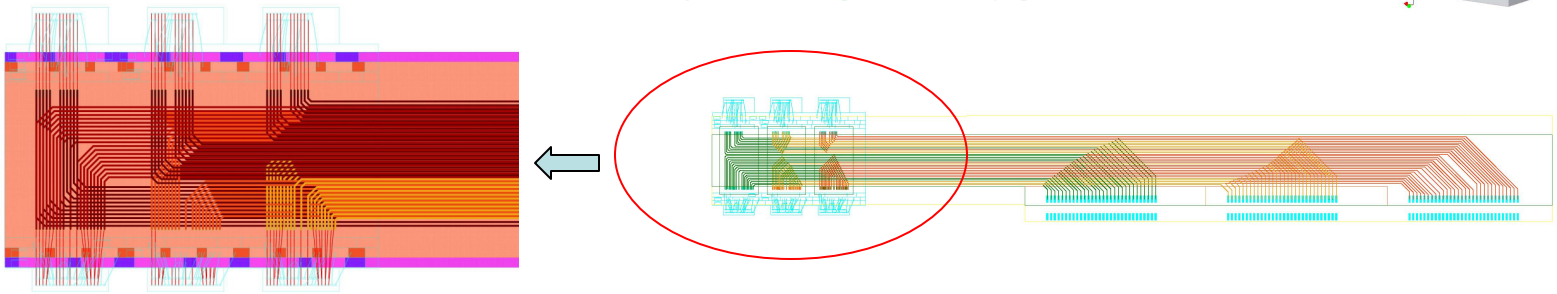
Very crowded region for cold flanges and beam pipe cooling connections



Hybrid Pixels R&D

- First Front-End chip (Superpix0) with 50x50 um pitch and a fast sparsified readout realized with ST 130 nm process (32x128 pixels).
- Chip characterized before and after the bump connection (by IZM) with a 200 um high resistivity sensor matrix (FBK) with excellent results. To be tested with beam in September.
- Prototype hybrid pixel module in preparation:
  - Bump-bonding of 3 FE chips with sensor matrix
  - Finalize Al bus design for prototype module

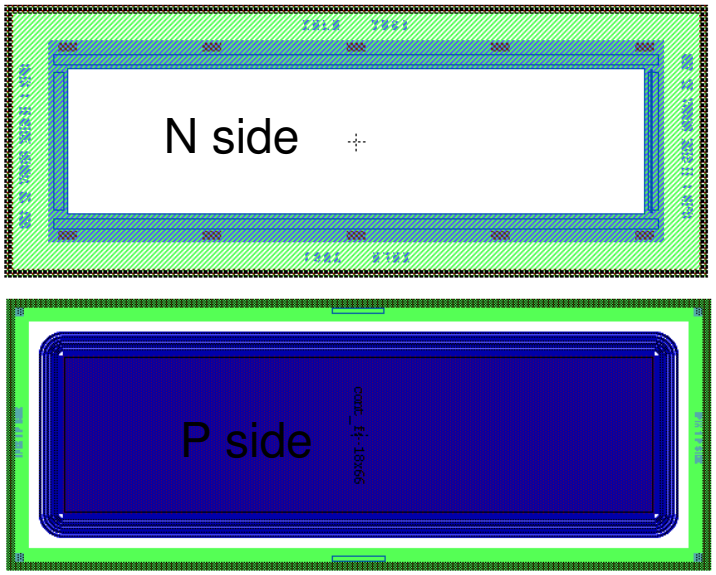




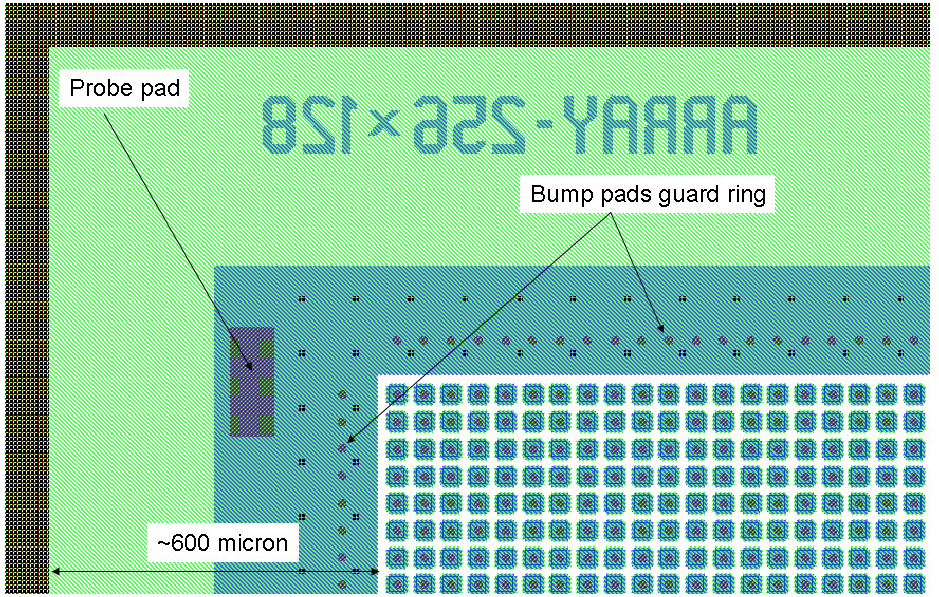
- Next FE chip in preparation with vertical integration process (Chartered/Tezzaron 130 nm) to split functionalities on two CMOS layers (analog/digital):
  - optimized pixel cell
  - new readout architecture (data push & triggered version)

Pixel Sensor Matrix

- Layout of the sensor wafer:
  - Several matrix sizes 32x128 → 256x128 (for multichip assembly)
  - N-on-N: P-spray isolation on n-side, p implant on the back side
- Wafer thickness: 200 μm (FZ, High-Ω silicon), fabricated by FBK
- Pixel capacitance (~ 20 fF) is dominated by the bump bond capacitance ~ 80 fF
- Termination structures:
  - Large GR on the pixel side
  - Multiguards on the bias side



Sensor corner, pixel size

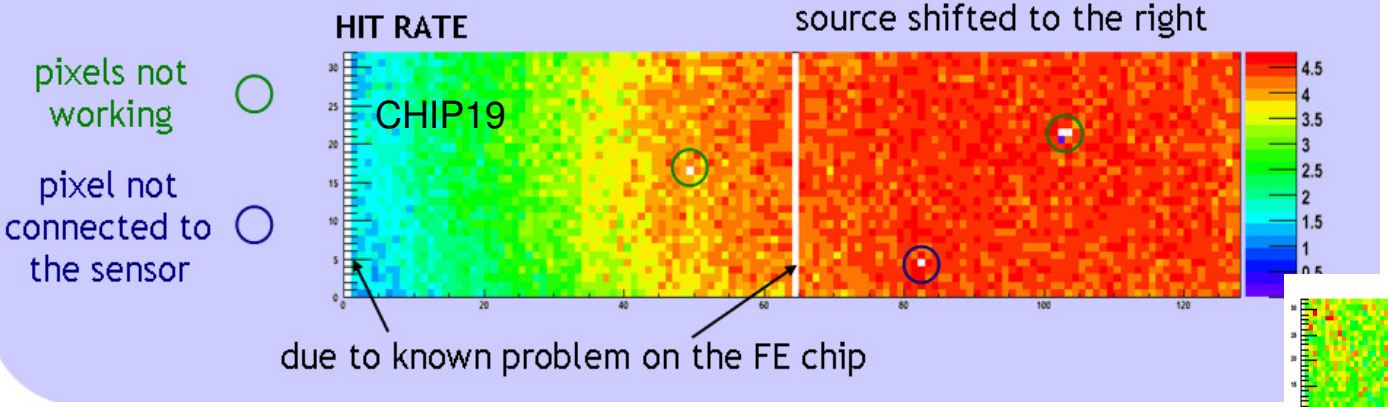


Test results on Superpix0

- Gain (by C_{inj} scans):
  - 38.0 mV/fC with sensor (6 % dispersion), 40.9 mV/fC w/o sensor (5 %)
- Noise (ENC= RMS_{noise}/Gain):
  - 66 e- w/o sensor , 81 e- with sensor → S/N = 200!
- Threshold dispersion ($RMS_{baseline}$/Gain):
  - 478 e- w/o sensor - 482 e- with sensor
  - Pixel threshold tuning circuit implemented in the next design

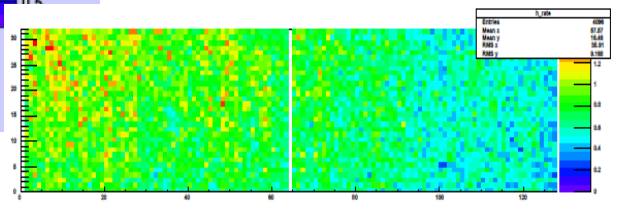
Response to a Sr90 source (e-) threshold@1/4 MIP (50σ noise)

→ good quality of the interconnection @ 50x50 μm² pitch & working sensor!!



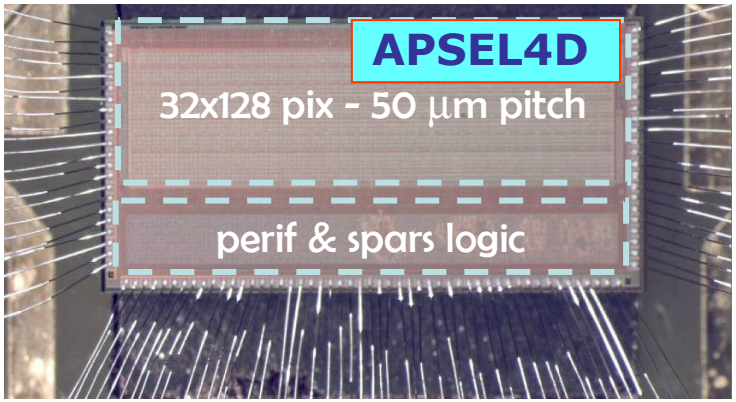
5 defects on 2 chips
6 x 10^{-4}

CHIP12: all ch. working



CMOS MAPS R&D

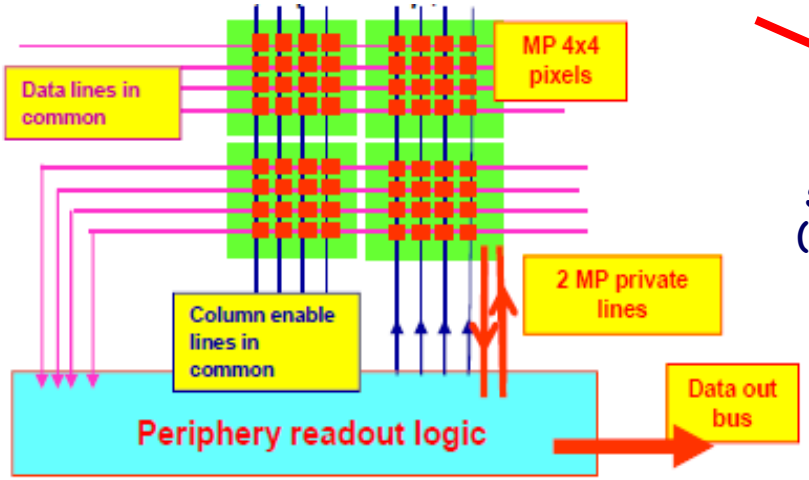
Development of deep N-well MAPS in single CMOS layer (ST 130 nm)

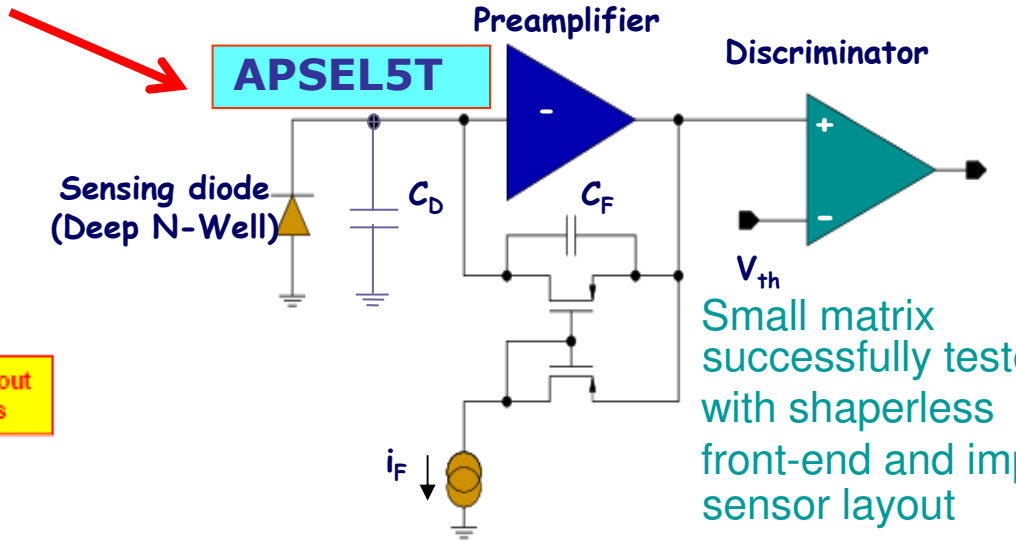


To reduce logic blocks with PMOS in the pixel, the matrix is subdivided in MacroPixel (MP=4x4) with point to point connection to the periphery readout logic:

- Register hit MP & store timestamp
- Enable MP readout
- Receive/sparsify/format data →output bus

With respect to APSEL4D, scaling to larger matrix size dictates to remove the shaper to make room for additional macropixel private lines



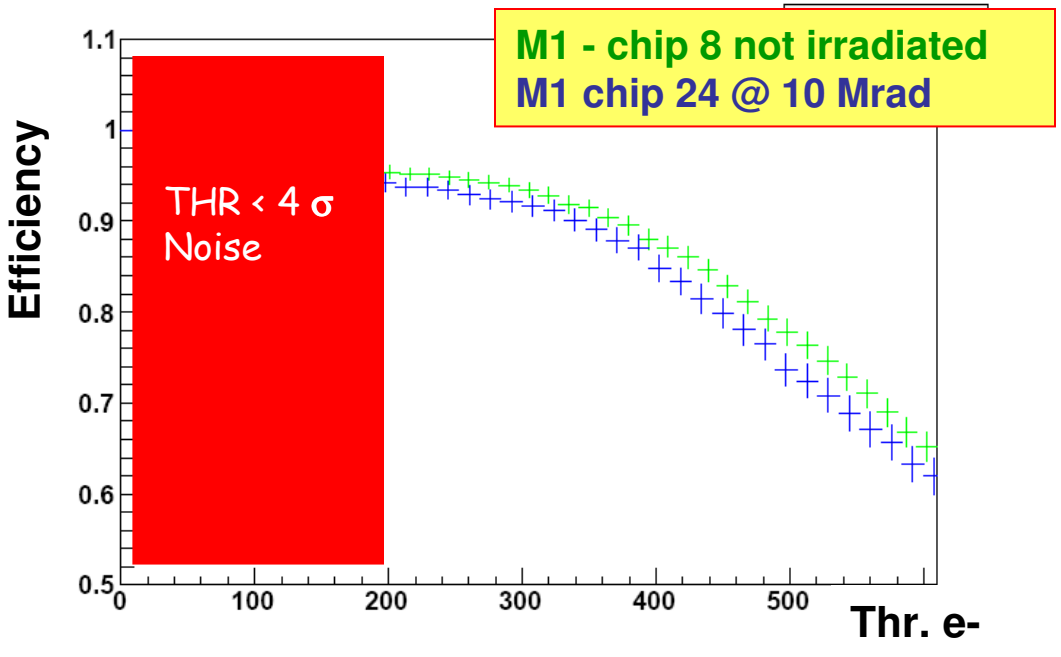


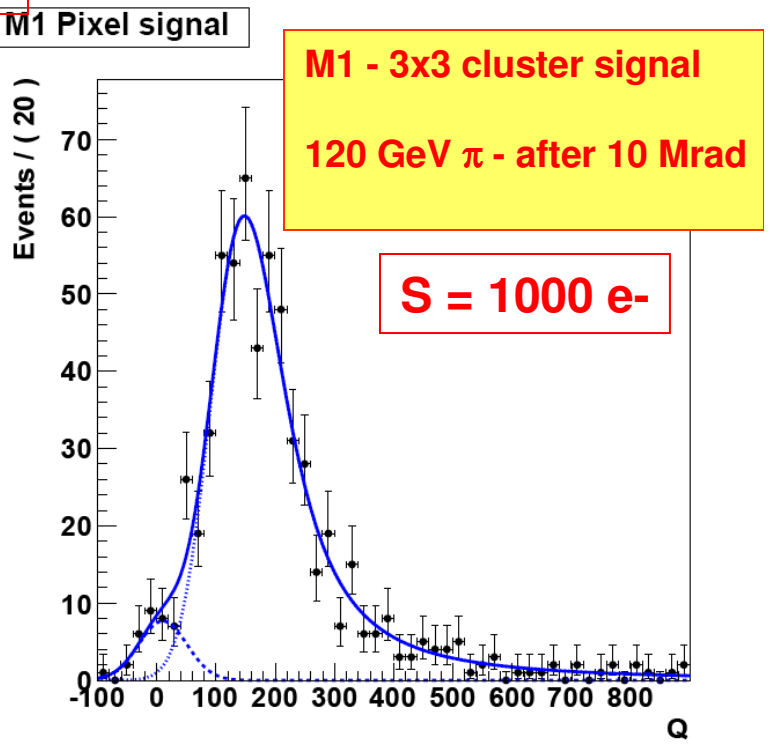
Small matrix successfully tested with shaperless front-end and improved sensor layout

Tesbeam with γ irradiated MAPS - 2009

Results for MAPS (3x3 matrix) with analog output (pre/post irrad. 10 Mrad ^{60}Co γ)

- Qcluster ~1000 e- for M1 (930 e- for M2)
- S/N~15-20 depending on the electrode geometry
- Efficiency~90% for both M1,2 in agreement with the measurements on digital MAPS
- Modest reduction in collected charge and efficiency in chip irradiated up to 10 Mrad
  - ENC increased by ~35% (after annealing)





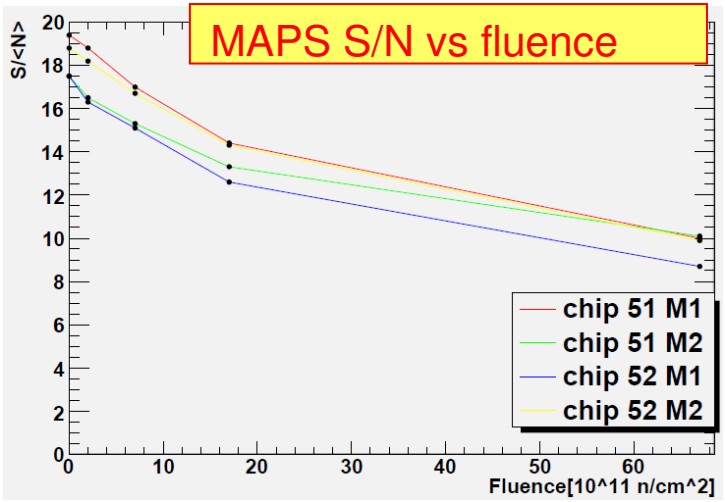
CMOS MAPS radiation hardness

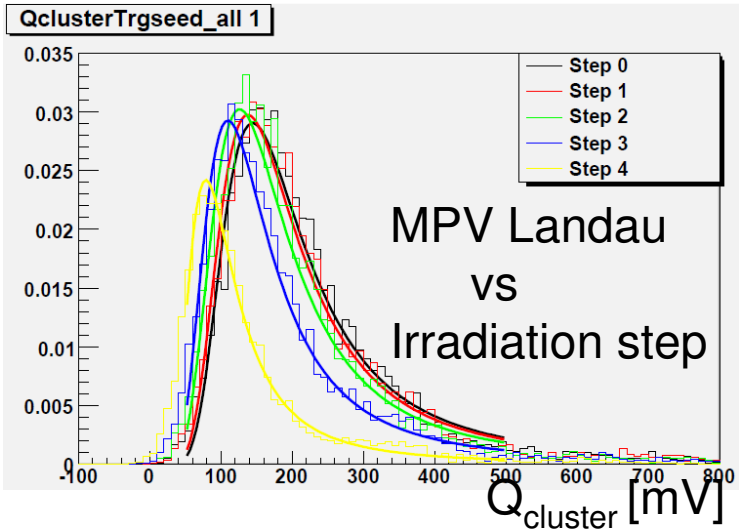
Charge collection studied after neutron irradiation up to fluence ~ 7 x 10^{12} n/cm^2

Expected 5 x 10^{12} n/cm^2 in 1 yr in Layer0 (no safety included!)

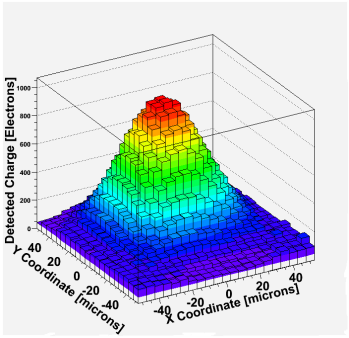
Results:

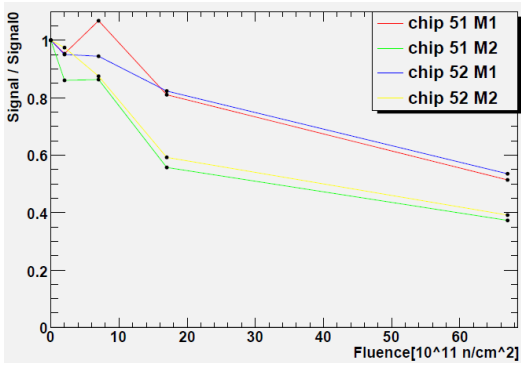
- Noise and gain not affected by neutron
- Signal degradation after each irradiation step studied with β Sr^{90} source:
  - S/N → 10 in last step
  - severe limitation for application in Layer0





- Results confirmed by i.r. laser scan:
  the max. amplitude of the signal decreases with fluence



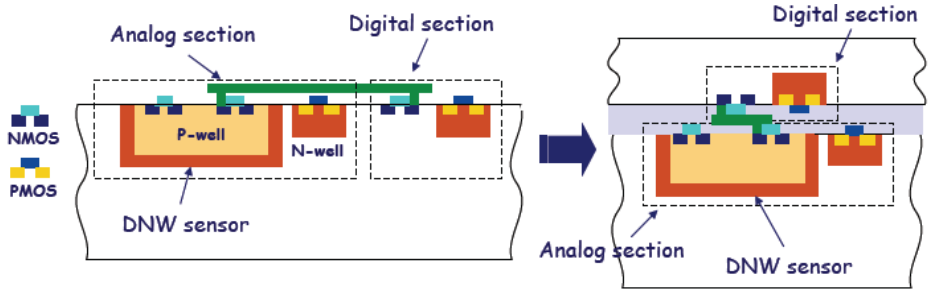


These structures will be tested (S/N with MIP and efficiency measurement) in the 2011 test-beam

Evolving from 2D to 3D

The use of vertical integration (2 CMOS layers interconnected) improves performance:

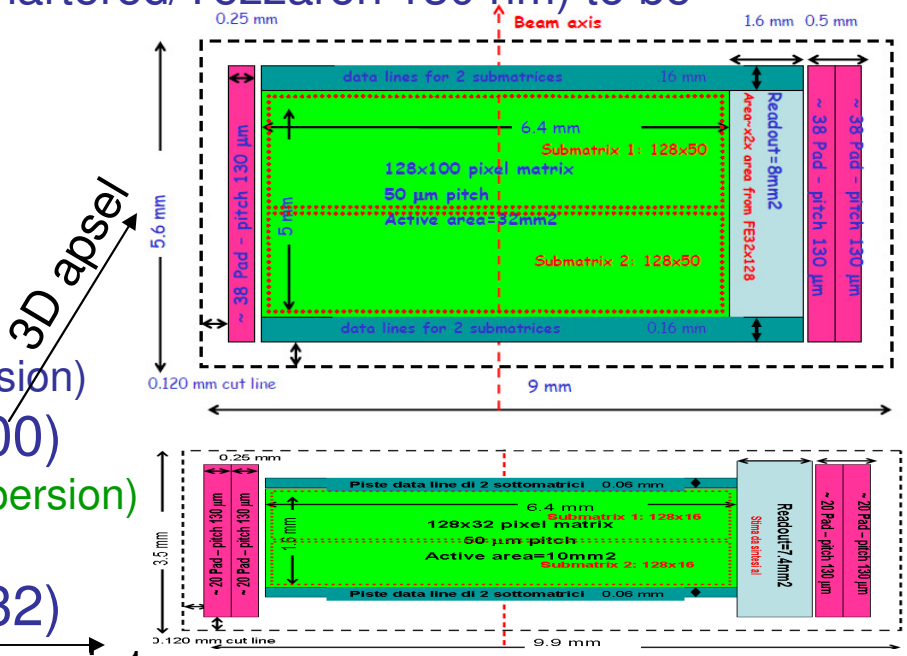
- higher sensor efficiency (PMOS and their competitive N-wells removed from the sensing layer)
- deep N-well area can be reduced (lower C_D → better noise/power trade-off)
- more advanced readout architecture can be integrated on pixel
- an extra high res. substrate can be used as pixel sensor and connected



- First 3D MAPS with vertical integration (Chartered/Tezzaron 130 nm) to be delivered soon, after long delay.
- After testing the chips the first 3D run,

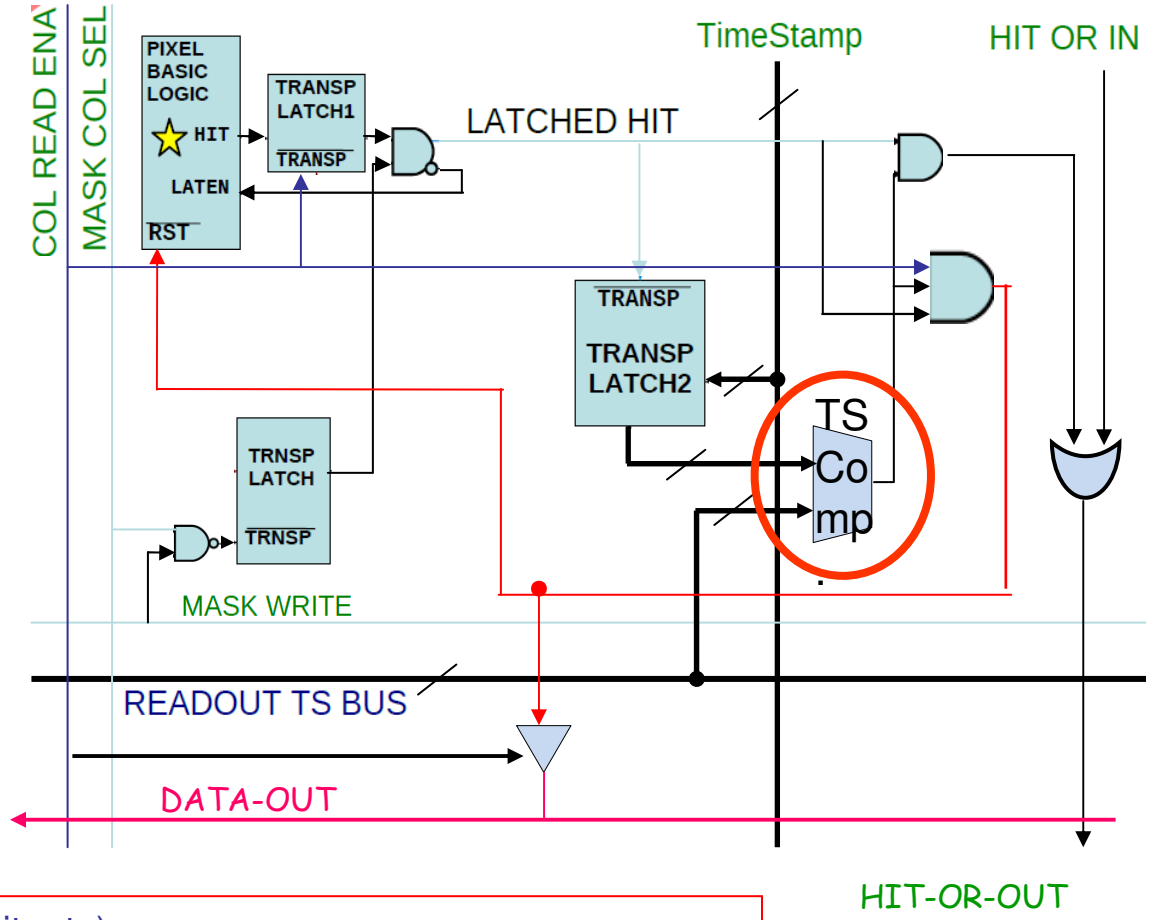
a new 3D run will be submitted in the Tezzaron/GlobalFoundries technology (organized by CMC/CMP/MOSIS) with a new readout architecture (flexible r.o. architecture: data push & triggered version)

- Larger CMOS MAPS matrix (128x100)
  - optimized analog cell (Gain & Thr. dispersion)
  - Time-ordered sparsified read-out
- Front-end chip for hybrid det. (128x32)



In-pixel logic with time-stamp for a time-ordered readout

- No Macropixel
- Timestamp (TS) is broadcast to pixels & pixel latches the current TS when is fired.
- Matrix readout is timestamp ordered
  - A readout TS enters the pixel, and a HIT-OR-OUT is generated for columns with hits associated to that TS.
  - A column is read only if HIT-OR-OUT=1
  - DATA-OUT (1 bit/pixel in the column) is generated for pixels in the active column with hits associated to that TS



VHDL simulation (100 MHz/cm^2 input hit rate):
- Triggered: r.o. efficiency ~ 98.2 % with 6 μs trigger latency; @ 50 MHz clock, (due to dead time during trigger latency for pixel already fired)
- Data push more efficient (> 99.9%) but very high bandwidth required on bus & HDI

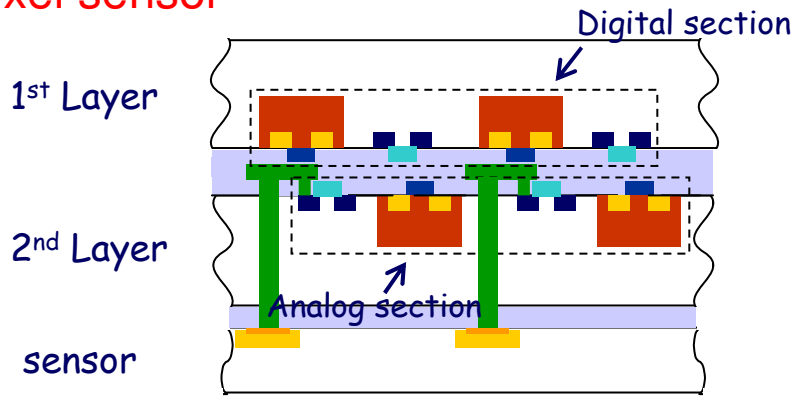
Layer0 will likely use triggered architecture.

This more complex in pixel logic will be implemented with 3D integration without reducing the pixel collection efficiency and improving the readout performance (*readout could be data push or triggered*)

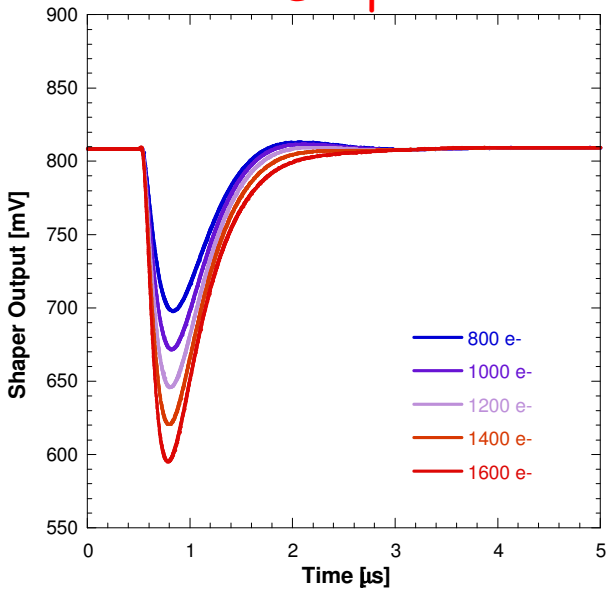
Design features and simulations for the 3D devices

	3D Apsel	Superpix1
Charge sensitivity	850 mV/fC	48 mV/fC
Peaking time	320 ns	260 ns
ENC	34 e rms	130 e rms
Threshold dispersion before/after correction	103/13 e	560/65 e
Analog power consumption	33 µW/pixel	10 µW/pixel
Detector capacitance	300 fF	150 fF
Matrix size	128x100	128x32
Pixel pitch	50 µm	50 µm

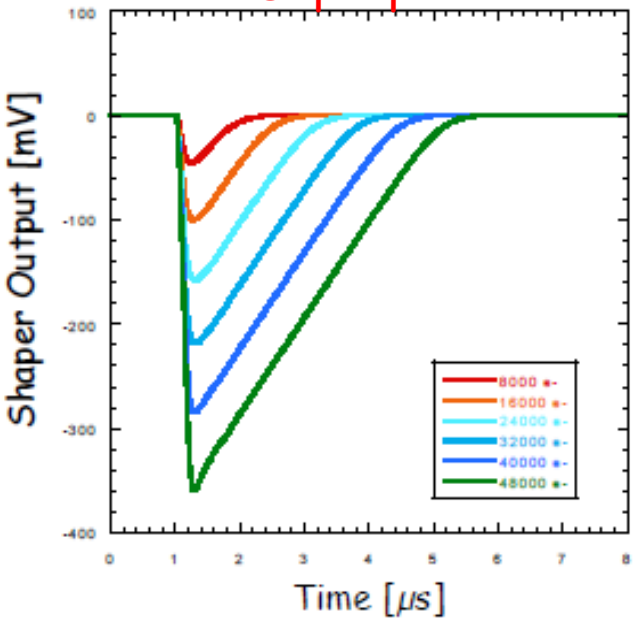
Superpix1 is to be connected to a high resistivity pixel sensor



3D Apsel

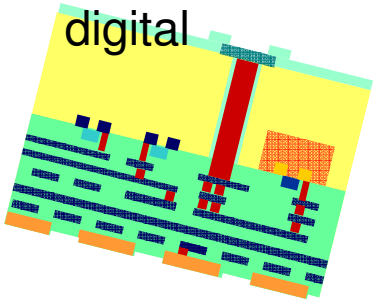


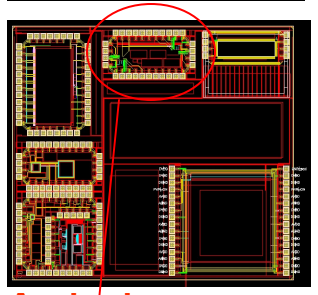
Superpix1



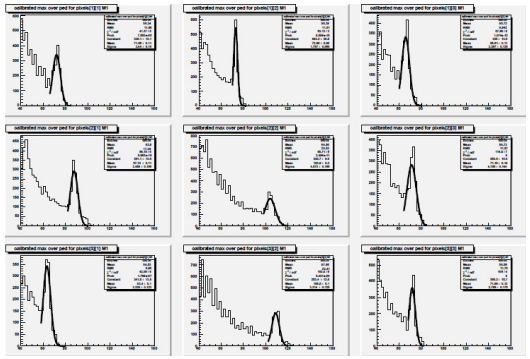
Tests of the layer with sensing electrode and analog front-end in APSEL chips from the first run of the 3D-IC consortium

(to test on beam in september)

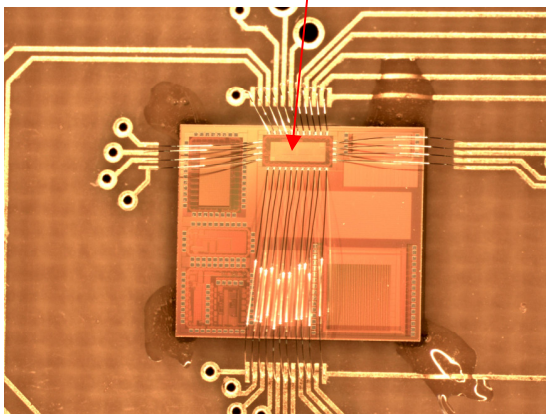


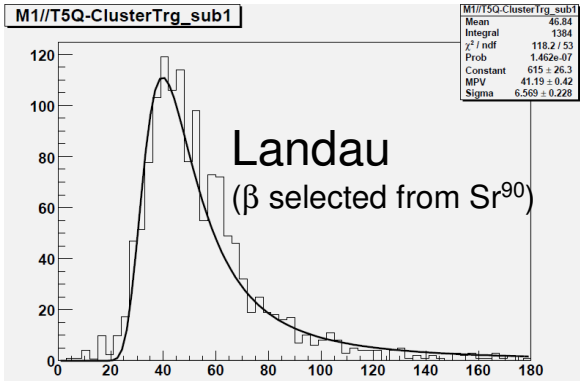


Fe^{55} γ (5.9 keV) on test (3x3) matrices



M	<μ> [mV]	<σ> [mV]	G [mV/fC]	ΔG/G [%]	<enc> [e-]
1	80	3.4	304	21	44
2	72	2.9	276	20	40





ENC~45e-
Gain([mV/fC] ~ 300

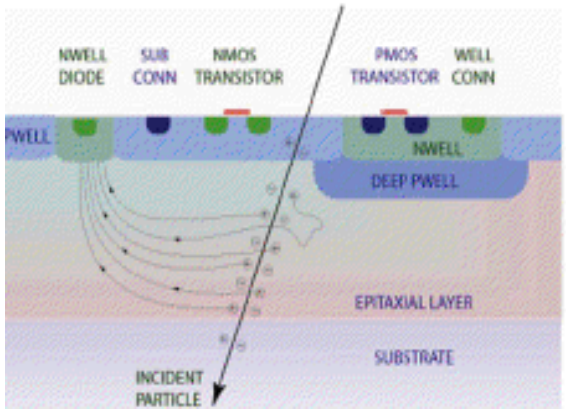
First estimate of
MIP-signal ~ 800e-

analog signal from a pixel

Open issues and further R&D

• **Hybrid pixels:** can they be thin enough?
Thinning studies of readout chips and sensors (epitaxial wafer / planar active edge) are being pursued by the pixel community (collaboration between SuperB and alice upgrade - Bari).

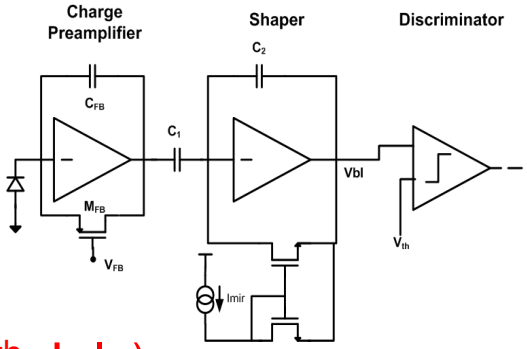
• **MAPS:** Tolerance to displacement damage could be a showstopper. A high-resistivity, fully depleted sensing layer with analog CMOS front-end might be the solution.



CMOS sensor in the 180nm INMAPS process with high-Ω epilayer

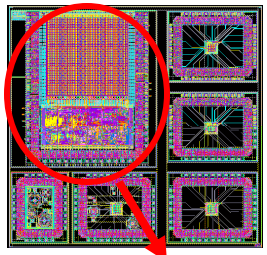
INMAPS developments for SuperB Layer0

- Small N-well collecting diodes with small input capacitance and low power consumption.
- The forth-well prevents charge stealing by the parasitic N-wells (→efficiency benefit).
- Same analog and digital architecture as APSEL chips, to fit at best the high background rate of Layer0.

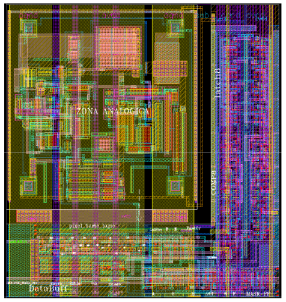


Charge sensitivity	930 mV/fC
Peaking time @ 800 injected electrons	240 ns
ENC (estimated C_D = 40 fF)	30 e rms
Threshold dispersion before/after correction	22 e rms
Analog power consumption	18 μW/pixel
Detector capacitance	40 fF
Matrix size	32x32 pixels
Pixel pitch	50 μm

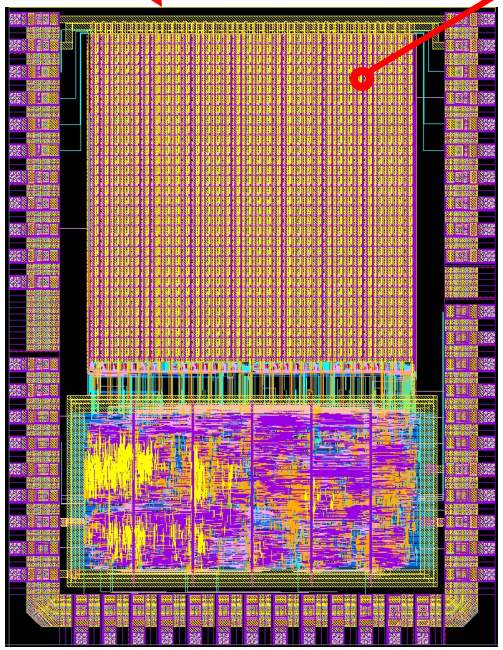
Submitted (4th July)



Chip(5x5 mm^2)



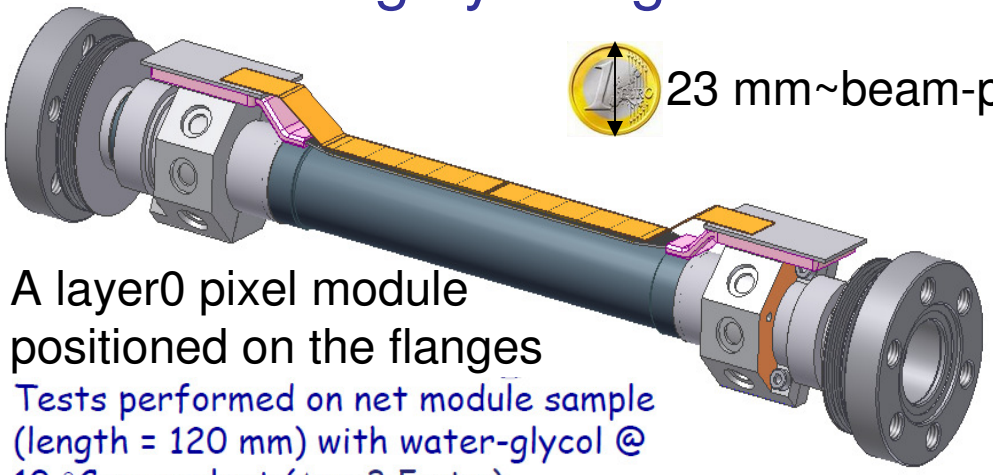
Pixel



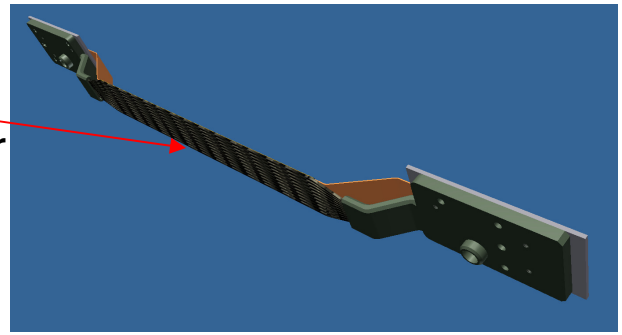
Matrix 32x32

R&D on Light support & cooling

Minimize material budget for the layer0 pixel support and cooling by using CF microchannels

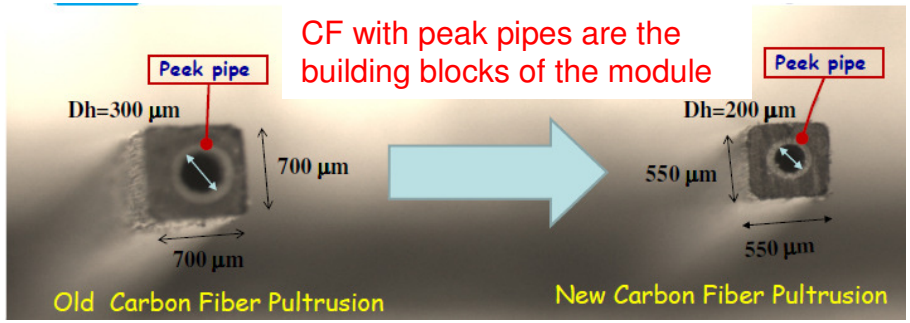


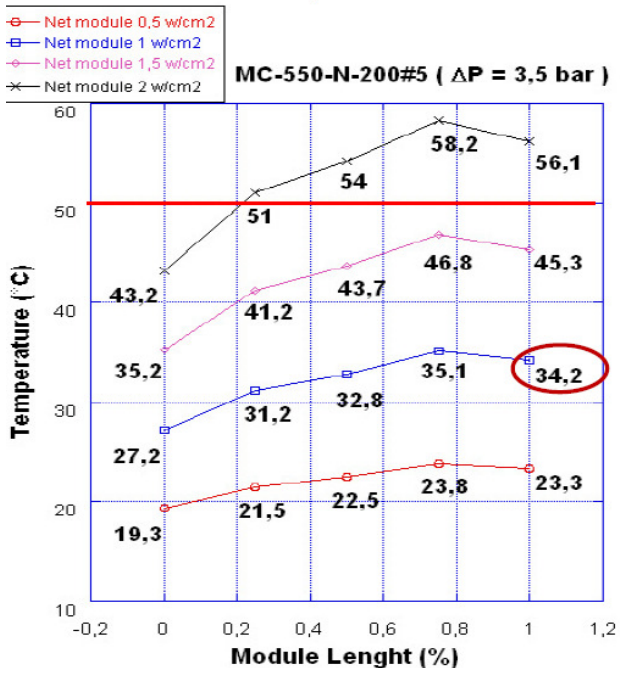
23 mm~beam-pipe diameter



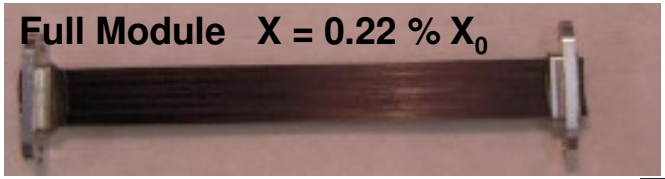
A layer0 pixel module positioned on the flanges

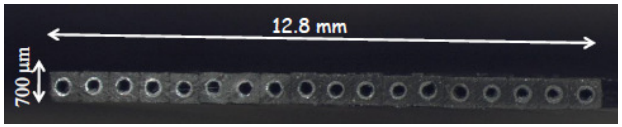
Tests performed on net module sample (length = 120 mm) with water-glycol @ 10 °C as coolant (Δp =3,5 atm).

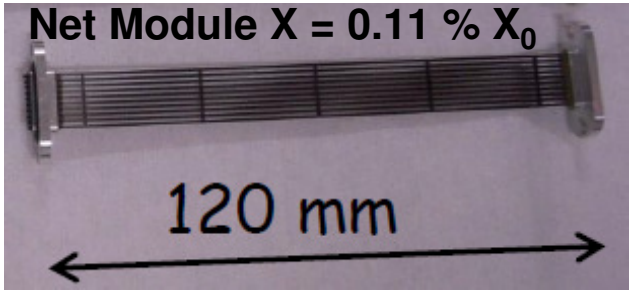


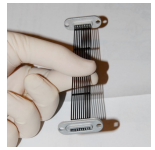


Material due to support:









SVT Institutions

Groups already working for the SVT:

- Trieste: Silicon sensors, striplets, fanout
- Pavia/BG: MAPS & FE chips (analog cells)
- RomaIII: MAPS
- Milano: fanout/pixel bus, FE chip, peripheral electronics, mechanics, SVT performance studies
- Bologna: SVT DAQ , MAPS & FE chips (digital architecture)
- Torino: testbeams mechanics.
- Pisa: SVT coordination, MAPS & FE chips, pixel & strip development (in-pixel logic, readout architecture, chips final layout, test of prototypes), module assembly & testing, SVT mechanics and cooling, testbeams.

« New » groups getting involved:

- Trento – pixel sensors, strip sensors
- University of Insubria – Mi-B (fanout external layers)
- Bari (Hybrid Pixel, other possible items)
- UK: QM (SVT mechanics, sensors?), RAL (MAPS)
- Strasbourg (MAPS)

Conclusions

- The SVT of SuperB is based on the design of the BaBar SVT, but must be equipped with an innermost layer0.
- Its baseline solution relies on $DSS_{triplet}D$

- A more advanced pixelated layer0 needed when SuperB operates at full luminosity, because of high occupancy due to irriducible (i.e. luminosity related) source of bkg.

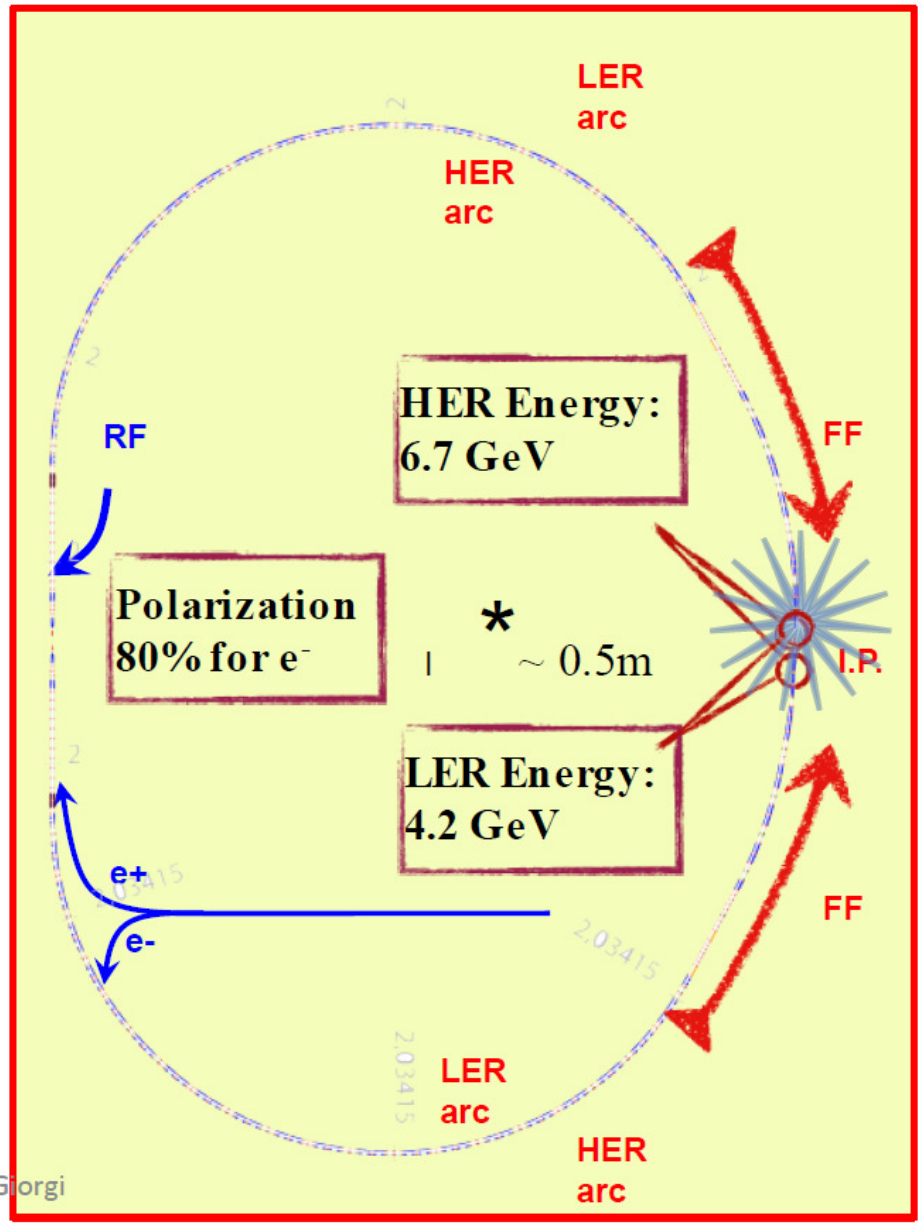
- Layer0 performance can greatly benefit from 3D integration, both for electronics and sensor.
- R&D on pixel (hybrid, CMOS-MAPS, V.I. pixel) to be finalized into a technology choice in about two years from now.

- Spring 2012: TDR ready.
- The SVT construction phase (with design & prototypes) starts in 2012.
- First data expected in mid 2016.

Back-up slides

Collider Parameters are "stable"

		Base Line		Low Emittance		High Current		Tau-charm	
Parameter	Units	HER (e+)	LER (e-)	HER (e+)	LER (e-)	HER (e+)	LER (e-)	HER (e+)	LER (e-)
LUMINOSITY	$cm^{-2}\,s^{-1}$	1.00E+36		1.00E+36		1.00E+36		1.00E+35	
Energy	GeV	6.7	4.18	6.7	4.18	6.7	4.18	2.58	1.61
Circumference	m	1258.4		1258.4		1258.4		1258.4	
X-Angle (full)	mrad	66		66		66		66	
β_x @ IP	cm	2.6	3.2	2.6	3.2	5.06	6.22	6.76	8.32
β_y @ IP	cm	0.0253	0.0205	0.0179	0.0145	0.0292	0.0237	0.0658	0.0533
Coupling (full current)	%	0.25	0.25	0.25	0.25	0.5	0.5	0.25	0.25
Emittance x (with IBS)	nm	2.00	2.46	1.00	1.23	2.00	2.46	5.20	6.4
Emittance y	pm	5	6.15	2.5	3.075	10	12.3	13	16
Bunch length (full current)	mm	5	5	5	5	4.4	4.4	5	5
Beam current	mA	1892	2447	1460	1888	3094	4000	1365	1766
Buckets distance	#	2		2		1		1	
Ion gap	%	2		2		2		2	
RF frequency	MHz	476.		476.		476.		476.	
Revolution frequency	MHz	0.238		0.238		0.238		0.238	
Harmonic number	#	1998		1998		1998		1998	
Number of bunches	#	978		978		1956		1956	
N. Particle/bunch (10^{10})	#	5.08	6.56	3.92	5.06	4.15	5.36	1.83	2.37
σ_z effective	μm	165.22	165.30	165.22	165.30	145.60	145.78	166.12	166.67
σ_y @ IP	μm	0.036	0.036	0.021	0.021	0.054	0.0254	0.092	0.092
Piwinski angle	rad	22.88	18.60	32.36	26.30	14.43	11.74	8.80	7.15
Σ_x effective	μm	233.35		233.35		205.34		233.35	
Σ_y	μm	0.050		0.030		0.076		0.131	
Hourglass reduction factor		0.950		0.950		0.950		0.950	
Tune shift x		0.0021	0.0033	0.0017	0.0025	0.0044	0.0067	0.0052	0.0080
Tune shift y		0.097	0.097	0.0891	0.0892	0.0684	0.0687	0.0909	0.0910
Longitudinal damping time	msec	13.4	20.3	13.4	20.3	13.4	20.3	26.8	40.6
Energy Loss/turn	MeV	2.11	0.865	2.11	0.865	2.11	0.865	0.4	0.17
Momentum compaction (10^{-4})		4.36	4.05	4.36	4.05	4.36	4.05	4.36	4.05
Energy spread (10^{-4}) (full current)	dE/E	6.43	7.34	6.43	7.34	6.43	7.34	6.43	7.34
CM energy spread (10^{-4})	dE/E	5.0		5.0		5.0		5.0	
Total lifetime	min	4.23	4.48	3.05	3	7.08	7.73	11.4	6.8
Total RF Wall Plug Power	MW	16.38		12.37		28.83		2.81	

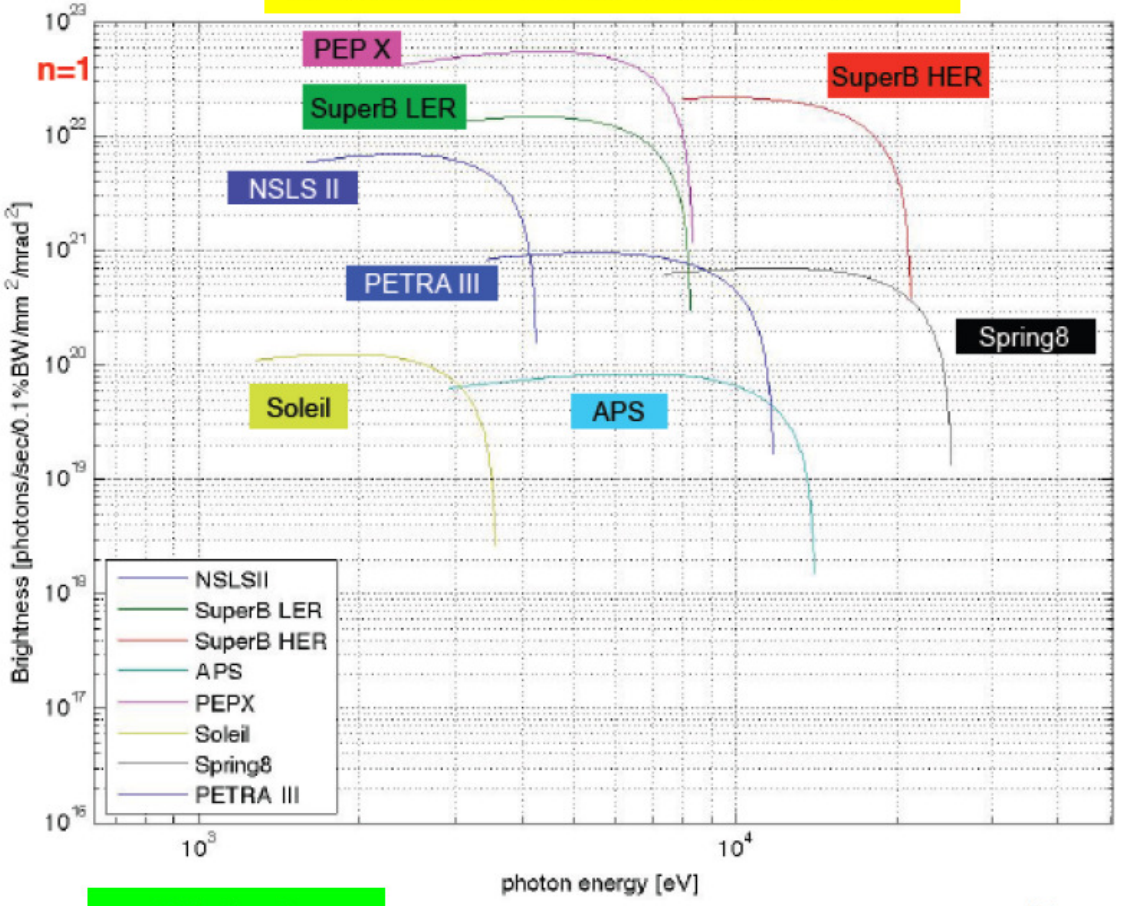


Synchrotron light options @ SuperB

- Comparison of brightness and flux from undulators for different energies dedicated SL sources & SuperB HER and LER
- Light properties from undulators better than most SL

Parameters *	SuperB HER	SuperB LER	NSLS II
	IVU20	IVU20	IVU20
E [GeV]	6.7	4.18	3
I [mA]	1892	2447	500
σx [mm]	60.0 E-3	66.5 E-3	33.3 E-3
σy [mm]	2.4 E-3	2.6 E-3	2.9 E-3
σx' [mrad]	33.3 E-3	37.0 E-3	16.5 E-3
σy' [mrad]	2.1 E-3	2.7 E-3	2.7 E-3
N [1]	148	148	148
λu [mm]	20	20	20
Kmax [1]	1.83	1.83	1.83
Kmin [1]	0.1	0.1	0.1

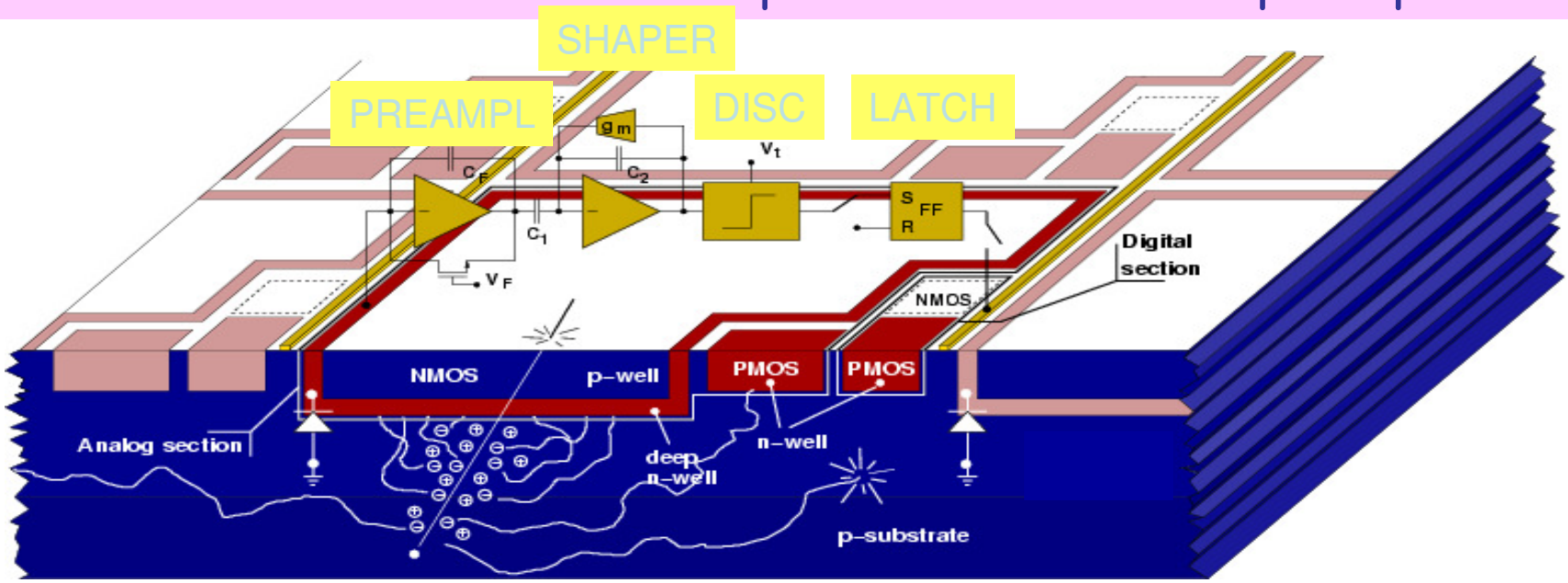
Brightness from undulators



W. Wittmer

Deep N-Well (DNW) sensor concept

New approach in CMOS MAPS design compatible with data sparsification architecture to improve the readout speed potential



A classical optimum signal processing chain for capacitive detectors can be implemented at pixel level:

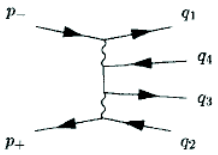
- Charge-to-Voltage conversion done by the charge preamplifier
- The collecting electrode (Deep N-Well) can be extended to obtain higher single pixel collected charge (the gain does NOT depend on the sensor capacitance), reducing charge loss due to competitive N-wells where PMOSFETs are located
- Need to keep the fill factor (DNW/tot N-well) as high as possible: ~ 90% in our design.

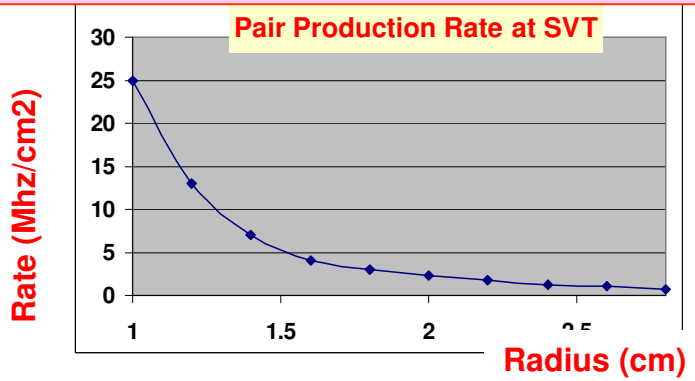
Backgrounds @ SuperB

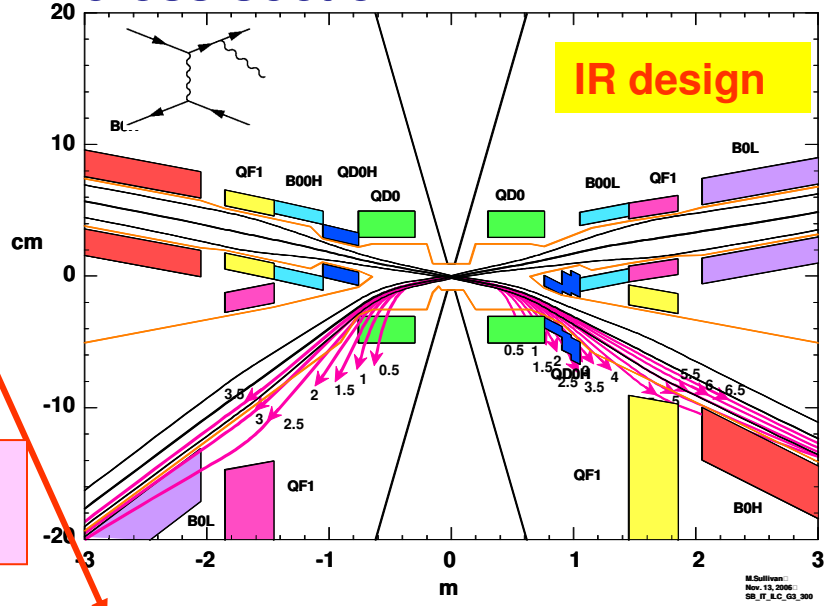
- Low currents (2A):
  - Beam-gas are not a problem (similar to BaBar)
  - SR fan can be shielded
- High luminosity → dominated by QED cross section

	Cross section	Evt/bunch xing	Rate
Radiative Bhabha	~340 mbarn (Eγ/Ebeam > 1%)	~680	0.3THz
e^+e^- pair production	~7.3 mbarn	~15	7GHz
Elastic Bhabha	O(10^{-5}) mbarn (Det. acceptance)	~20/Million	10KHz
$\Upsilon(4S)$	O(10^{-6}) mbarn	~2/million	1 KHz

Track rate reduced to ~5 MHz/cm^2 in Layer0
→ e+/e- have low energy and loop in the 1.5T B field.

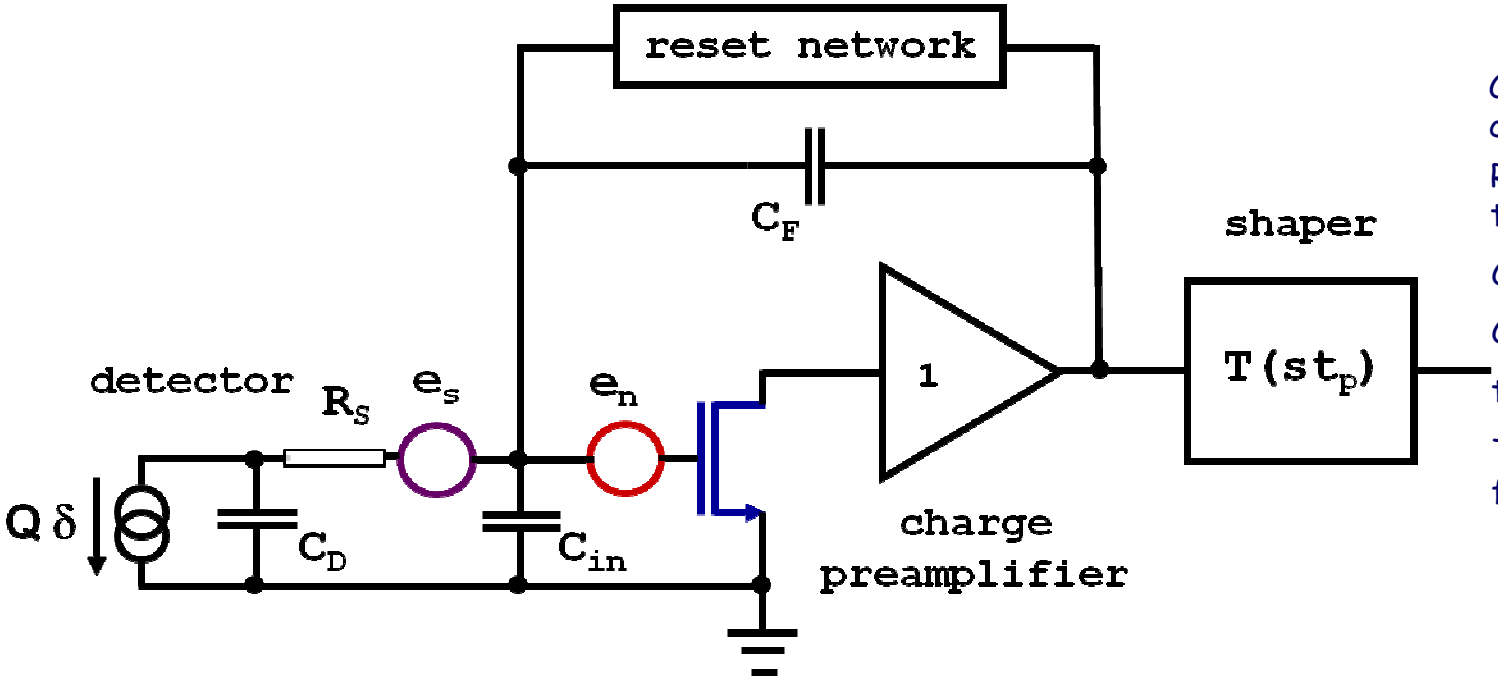






Rate reduced to ~ 100 kHz/cm2 @ SVT location with present IR design and proper shielding to prevent the produced shower from reaching the detector

Noise evaluation in SVT layers: analog channel model



C_D=detector capacitance+strays

R_S=series resistance of the detector

C_F=feedback capacitance

C_{in}=input capacitance

t_p=peaking time

$T(st_p)$=shaper transfer function

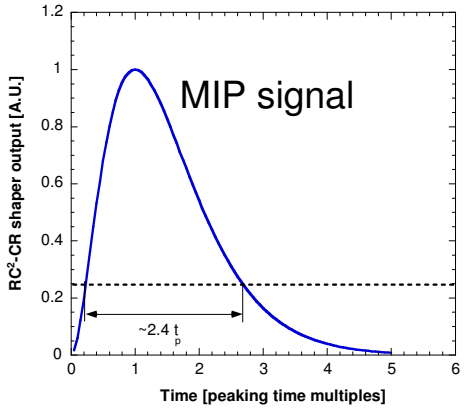
- We assume that the main contributions come from thermal and 1/f noise in the preamplifier input device and from thermal noise in the distributed strip resistance
- Noise in the detector leakage current and in the reset network not considered

Strip FE chip: ENC estimate

Layer	C_D [pF]	available t_p [ns]	selected t_p [ns]	ENC from R_S [e rms]	ENC [e rms]	Channel width [μm]	Hit rate/strip [kHz]	Efficiency 1/(1+N)
0	11.2	25, 50, 100, 200	25	220	**740**	3000	2060	0.890
1	26.7		100	460	**940**		697	0.857
2	31.2		100	590	**1100**		422	0.908
3	34.4		200	410	**940**		325	0.865
4	52.6	400, 600, 800, 1000 (or 500 and 1000)	500	490	**1000**	9000	47	0.947
			600	440	**940**			0.937
5	67.5		800	560	**1090**		28	0.949
			1000	500	**1030**			0.937

RC²-CR shaping, I_D=500 μA, L=200 nm, N-channel input device, analog dead time~2.4 t_p

The efficiencies are under-estimated because of the hypo. of 1MIP for the charge Q on each strip (bkg. tracks release: 4ke-<Q<< 16 ke- in 200 um Si). Lower Q→ shorter ToT and then shorter dead time.



Pixel for Layer0

- Definition of requirements for Layer0 pixels:

Physics:

- Resolution of 10-15 μm in both coordinates
- Total material budget ≤1% X_0
- Radius ~1.3 -1.5 cm

Background (x5 safety included)

- Rate ~100-300 MHz/cm^2 depends on radius and sensor thickness
  - Timestamp of 1 us → 5-10 Gbit/s link
- TID ~ 15 Mrad/yr
- Eq. neutron fluence: 2.5 10^{13} n/cm^2/yr
  - Standard CMOS MAPS marginal

Several options still open & under development → decision on technology in 2013

- Hybrid pixels: more mature and rad hard but with higher material budget
  - R&D on FE chip 50x50 um pitch with fast readout ongoing
  - Pixel module design with ~ 1 % X_0 with present technology
  - Evaluate reduction of material in silicon & pixel bus (synergy with ALICE ITS upgrade).
- CMOS MAPS: newer technology potentially very thin, readout speed and rad hardness challenging for application in Layer0.
  - R&D on DNW MAPS with sparsified fast readout well advanced
  - New submission in July with INMAPS CMOS process with high resistivity substrate & quadruple well→ to improve radiation hardness & charge collection efficiency.

DNW MAPS R&D

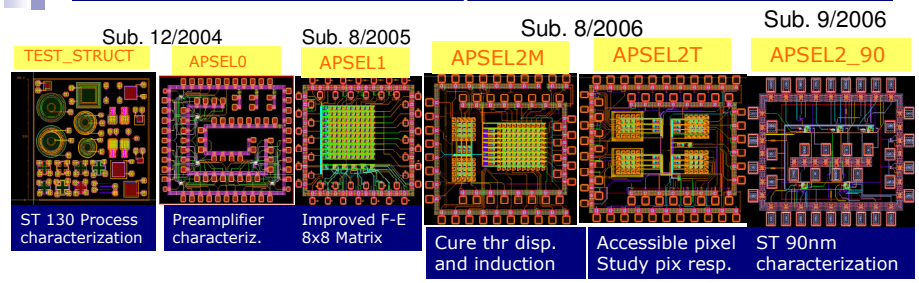
IC group contribution:
- **Pavia (PV)-Bergamo(BG) analog front-end**
- **Pisa(PI)-PV-BG in pixel digital logic**
- **Bologna-PI digital readout architecture**

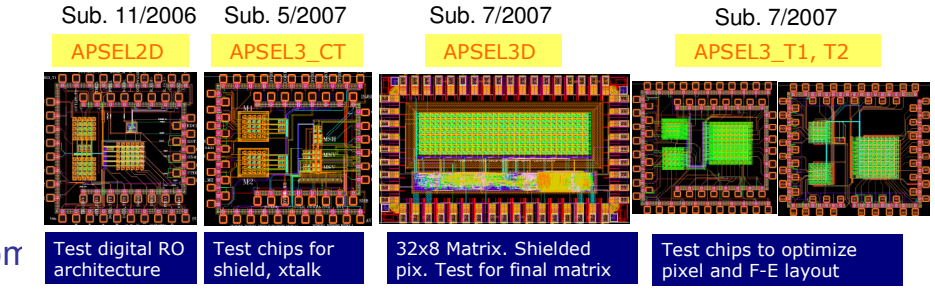
- **Implemented in ST 130 nm process**
- Proof of principle (APSEL0-2)
  - first prototypes realized in 130 nm triple-well ST-Micro CMOS process
- APSEL3
  - 32x8 matrix with sparsified readout
  - Pixel cell optimization (50x50 um^2)
    - Increase S/N (15→30)
    - reduce power dissipation x2
- **APSEL4D**: 4K(32x128) 50x50 μm^2 matrix
  - data-driven sparsified readout + timestamp
  - Pixel cell & matrix implemented with full custom design and layout
  - Sparsifying logic synthetized in std-cell from VHDL model
  - Periphery inlcudes a "dummy matrix" used as digital matrix emulator
- **Beam tests:**

  2008 - APSEL4D MAPS matrix + striplets

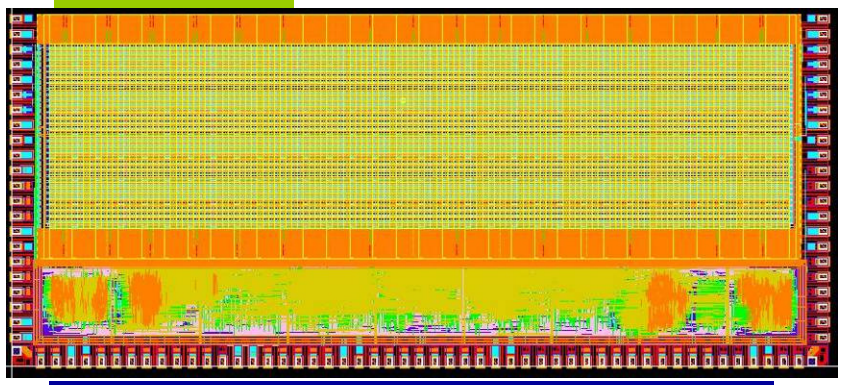
  2009 - MAPS structures with analog output & irrdiated devices
- **Radiation tests:**
  - Irradiation with ^{60}Co γ up to 10MRad
  - Irradiation with neutrons under way

Submitted MAPS Chips



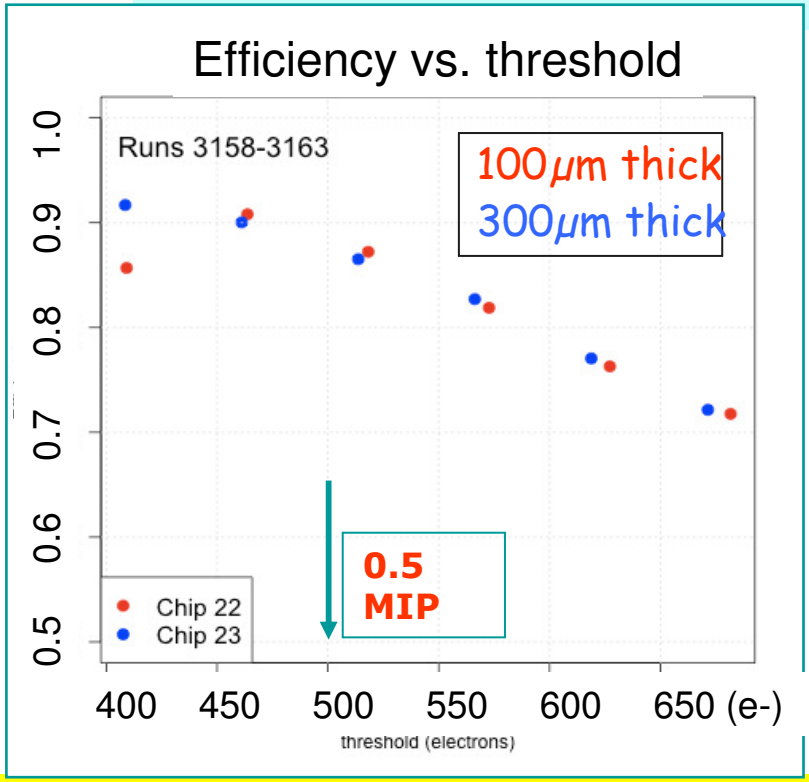


APSEL4D sub 11/2007- rec 3/2008



32x128 4k pixel matrix for beam test

DNW MAPS Hit Efficiency measured in a CERN beam test (APSEL4D)

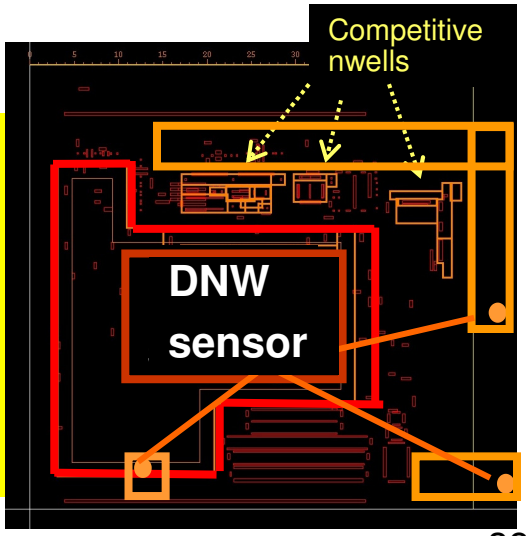


Measured with tracks reconstructed with the reference telescope extrapolated on MAPS matrix

- MAPS hit efficiency up to 92 % @ 400 e- thr.
- 300 and 100 μm thick chips give similar results
- Intrinsic resolution ~ 14 μm compatible with digital readout.

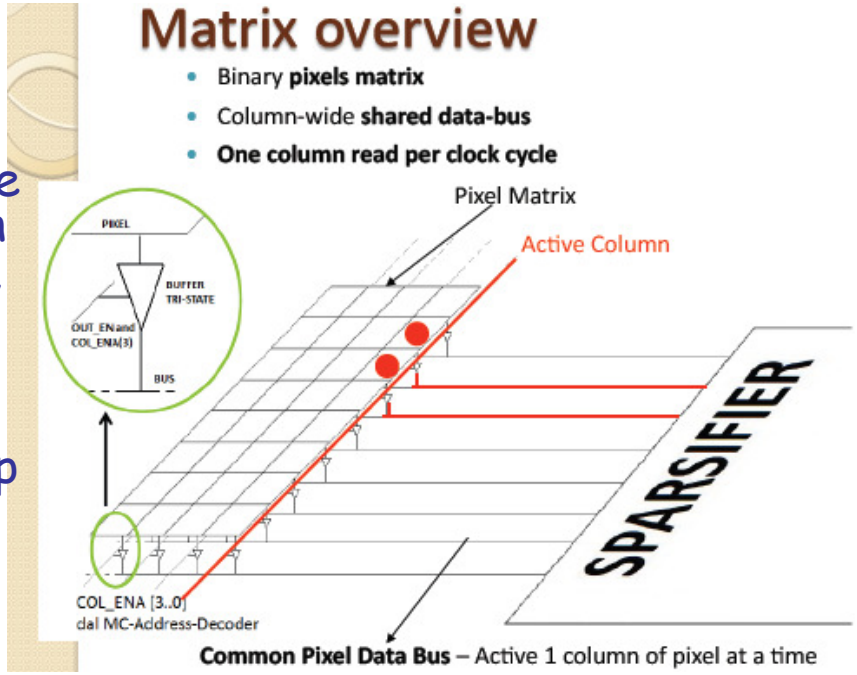
- Test Beam results in: *doi:10.1016/j.nima.2010.08.026*

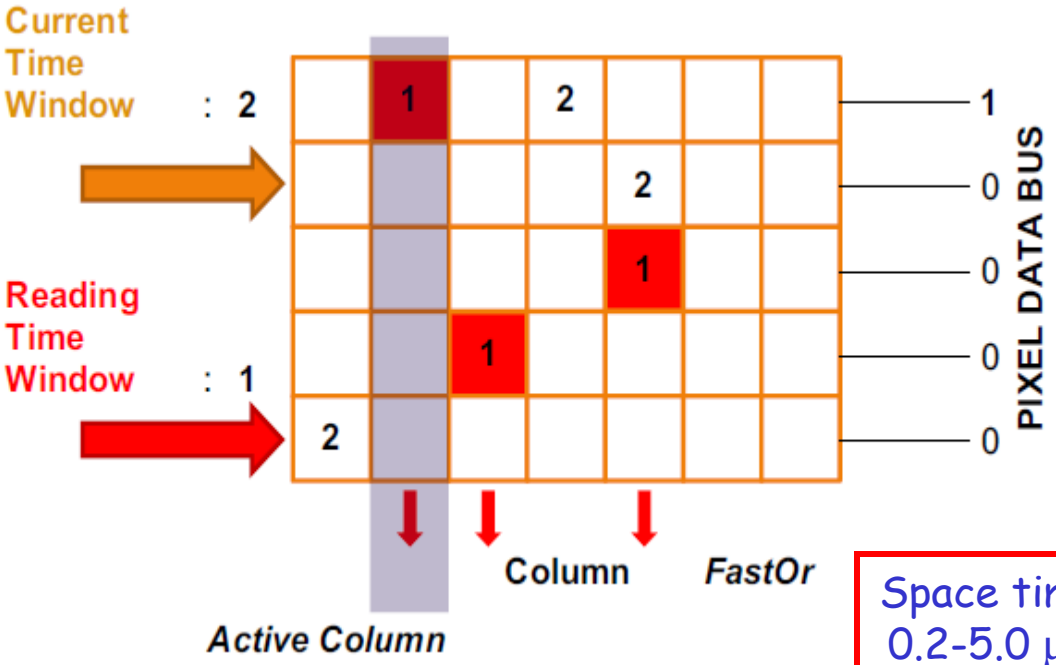
- Competitive N-wells (PMOS) in pixel cell steal charge reducing the hit efficiency: fill factor (DNW/tot N-well) ~ 90 %
  - **2D MAPS:** efficiency can improves adding multiple collecting electrodes around competitive nwells, even better using a quadruple well process (INMAPS being considered).
  - **3D MAPS:** (2 tiers for sensor&analog + digital) fill factor and efficiency can improves significantly.



Read-out architecture

- **Time-ordered hit extraction**: hits with the same time stamp are stored and sent out in bunches with a common time stamp header, saving on-chip memory and output bandwidth.
- **Triggered architecture** exploits hit latches as a buffer memory. If a timestamp was not triggered, all the corresponding hits are discarded in one clock cycle with the time-dependent reset signal. Otherwise, a column scan is performed for that time stamp.



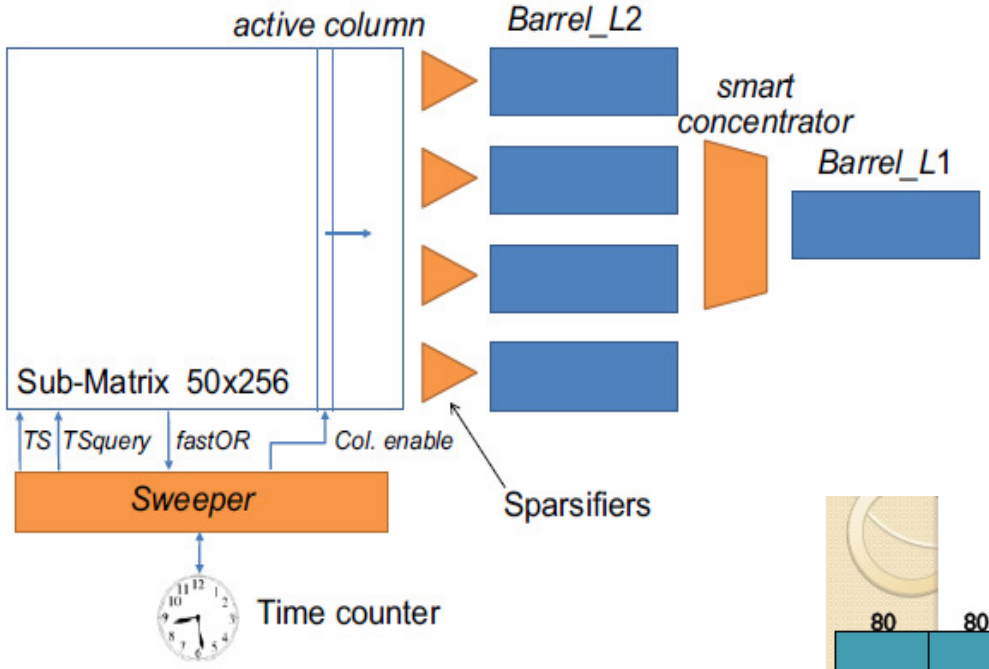


For each time stamp request,the active column sweeps over the columns with an active fast-OR.

Latched hits are extracted from the matrix by a data bus shared by the matrix columns and driven in turn by the current active column

Space time coordinates with time granularity 0.2-5.0 μs (BCO clock)

Readout architecture

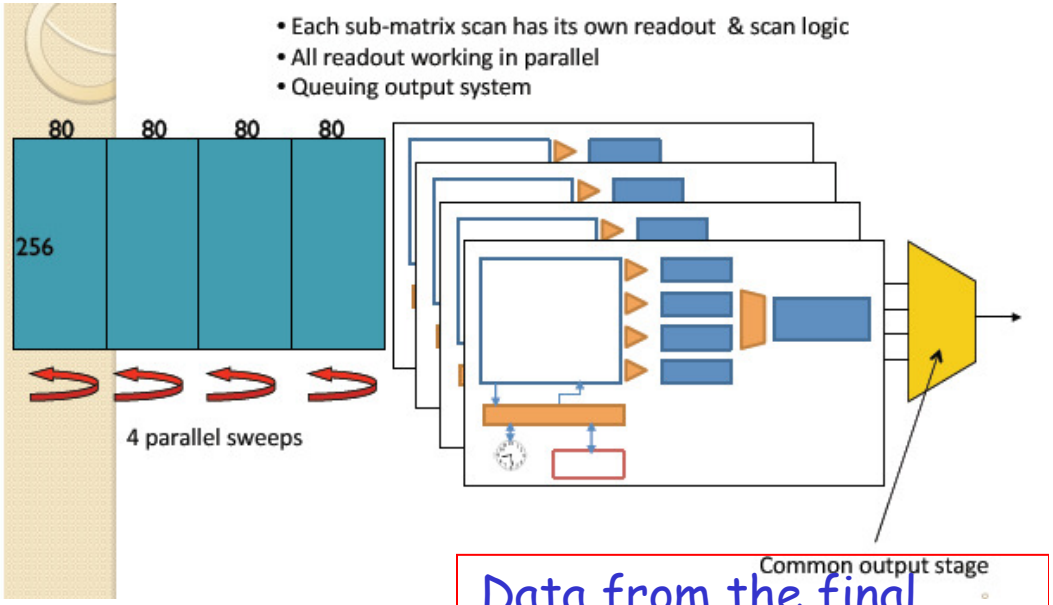


Four parallel sparsifiers encode hits found on the data bus in a single clock cycle.

The barrel-L2 acts like a FIFO memory conveying data to barrel-L1 by a concentrator which merges the flux of data and preserves the time order.

Since hit extraction efficiency depends on mean sweeping time, the matrix is divided into sub-matrices (e.g. 4) with fewer columns to be swept.

An additional concentrator is added at the back-end of the four barrels-L1, driving the chip output data bus.



Each readout sweeps a portion of the matrix with 60 MHz clock.

Data from the final barrel are sent to a common bus with a faster clock ~ 200 MHz

High-rate time-ordered readout efficiency

- Simulation Results with 100 MHz/cm^2 hit rate

Layer0 (including x5 safety factor)

50 μm thick sensor @ R=1.3 cm

or a 200 μm sensor @ R=1.9cm

-Triggered: readout efficiency ~ 98.2 % (6 μs trigger latency)

  - dead time during trigger latency for pixel already fired

-Data push more efficient (> 99.9%) but very high bandwidth required on bus & HDI

-Layer0 will likely use triggered architecture.