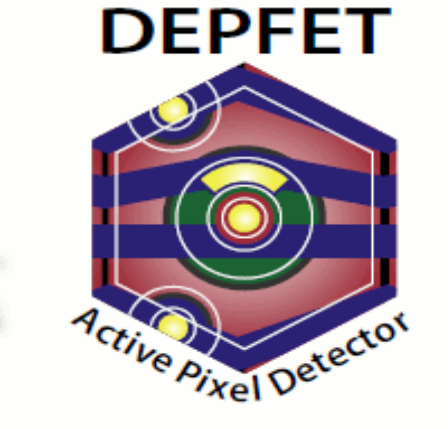
Belle II DEPFET pixel detector



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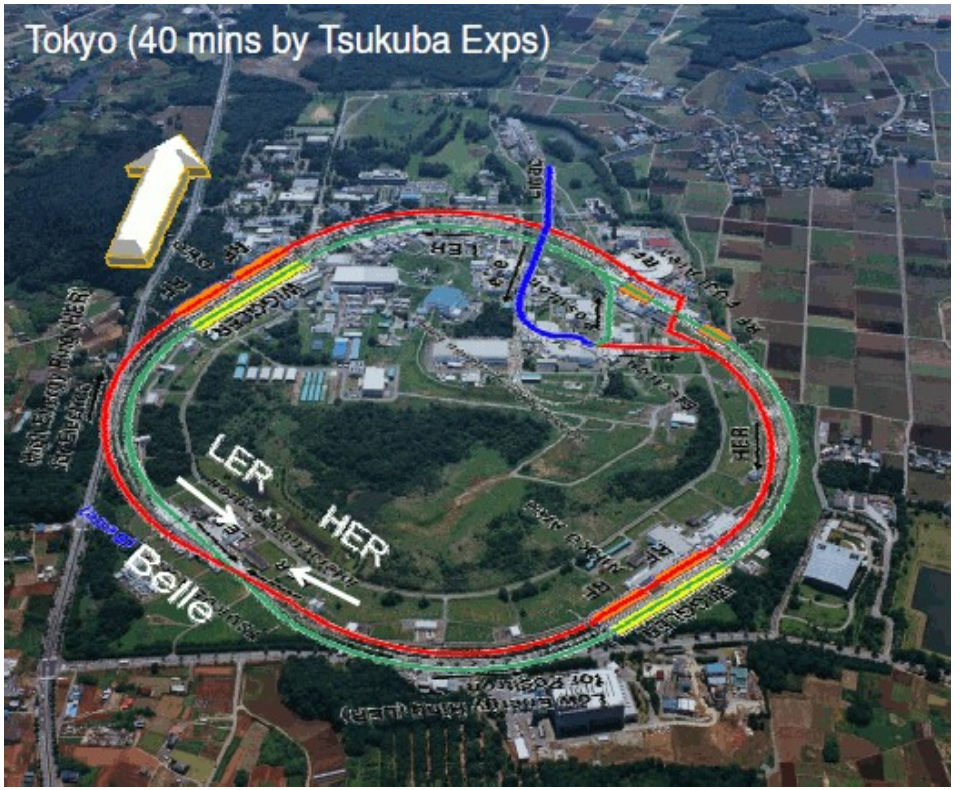
for the DEPFET Collaboration

RD11, 6-8 July 2011 Florence

Belle II DEPFET pixel detector

- Vertex detector layout for SuperKEKB
  - Challenges and requirements
- Overview of Belle-II PXD
  - DEPFET module concept
  - Mechanics and cooling
  - Front- end and PXD DAQ
- Results from test systems



Upgrade of B factory KEKB

SuperKEKB goal luminosity: $\mathcal{L} = 8 \times 10^{35}\ \mathrm{cm}^{-2}\ \mathrm{s}^{-1}$

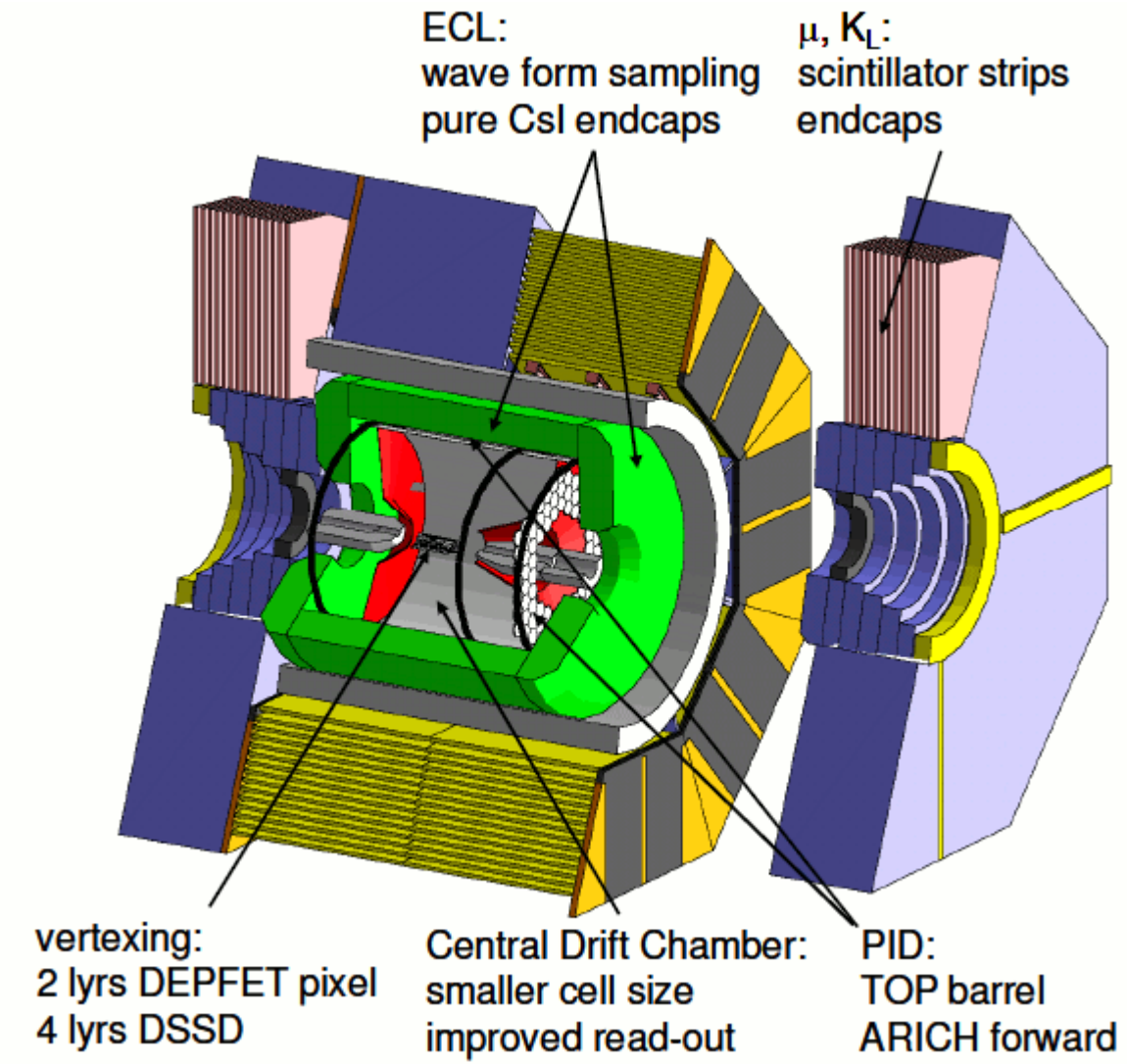
SuperKEKB and Belle II

Luminosity upgrade realized with Nano Beam option

- Larger crossing angle: 22mrad → 83mrad
- Smaller asymmetry LER/HER: 3.5/8GeV → 4/7GeV
- Squeeze beta functions (/20)
- Increase beam currents (x2)

Have to deal with

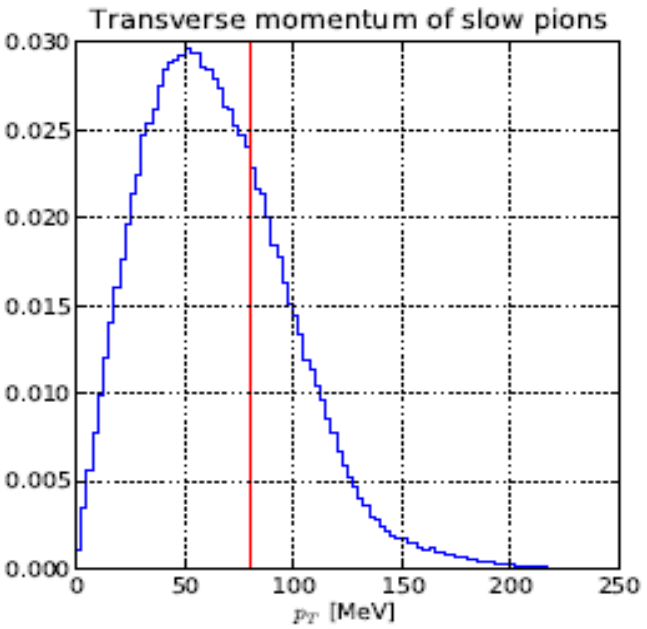
- Harsh radiation environment: 1MRad/year
- Higher density of background hits (x30 Touchek effect)
- L1 trigger rate ~30kHz



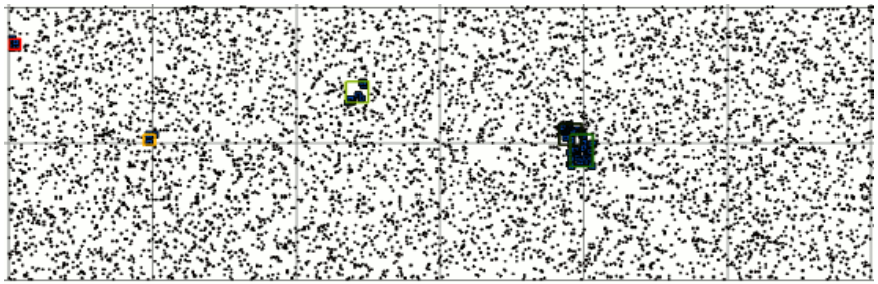
Vertex Detector Goals

- Improved vertex resolution for Belle II
  - DEPFET layers closest to IP
  - Single point resolution ~10μm
- Low material budget of 0.2% X_0 per ladder
  - All silicon ladders, thinned sensors
- Max. acceptable pixel occupancy < 3%
  - Small pixels and parallelized readout
- High hit efficiency down to p_T ~50MeV
- Data reduction to ~100kB/event at ~6kHz
- Very little space between beam pipe and SVD
  - Integrated cooling
- Sufficient radiation hardness Sensor/ASICs
  - See talk by A. Ritter

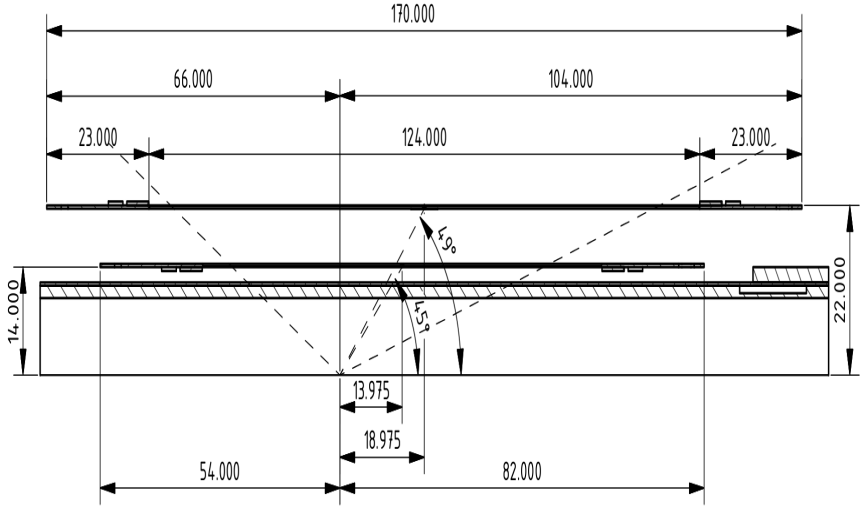
$D^{*+/-} \rightarrow D^0\pi^{+/-}$

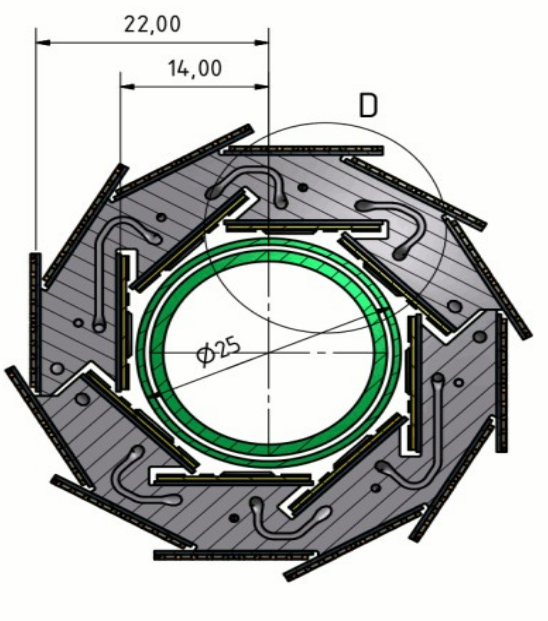


Module with 3% occupancy



DEPFET Pixel Detector



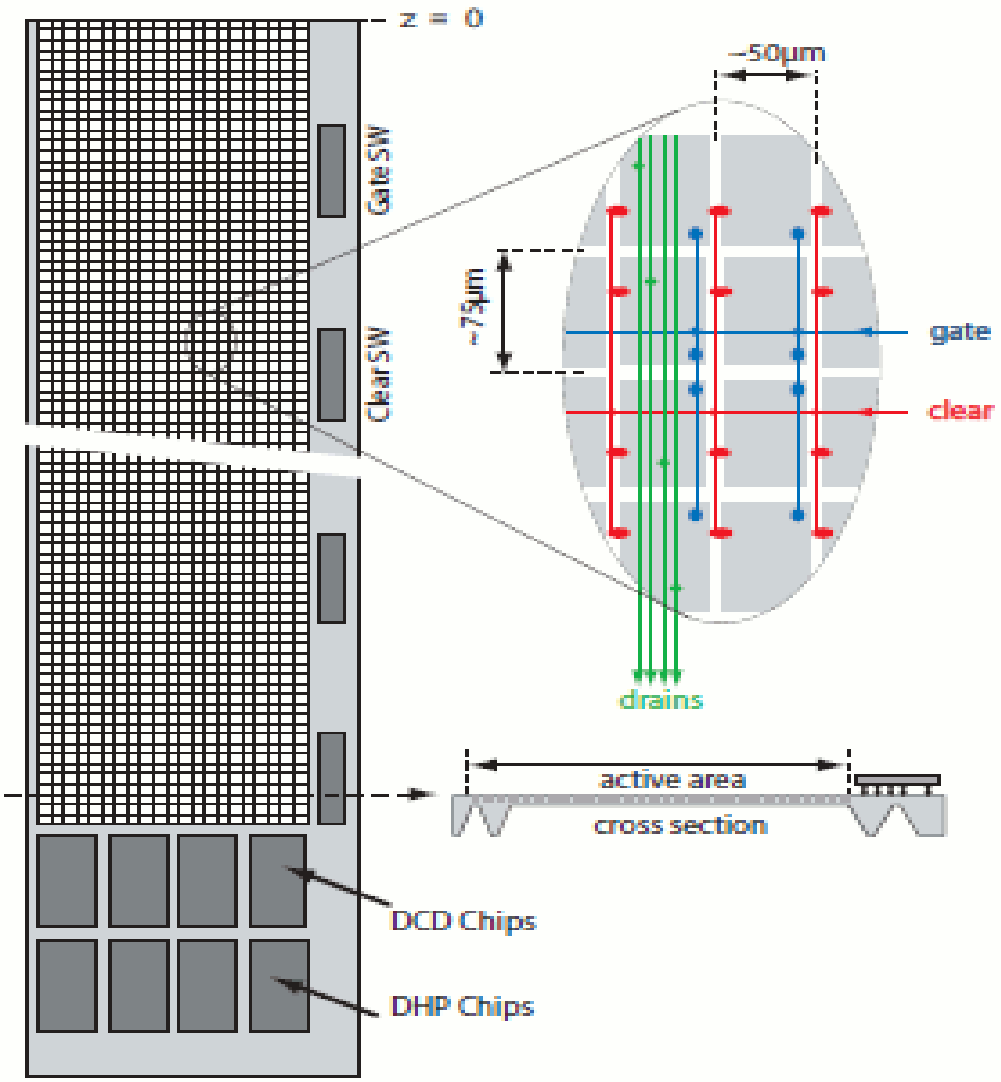


2 layers of 75µm thick pixel sensors of DEPFET type @14, 22mm

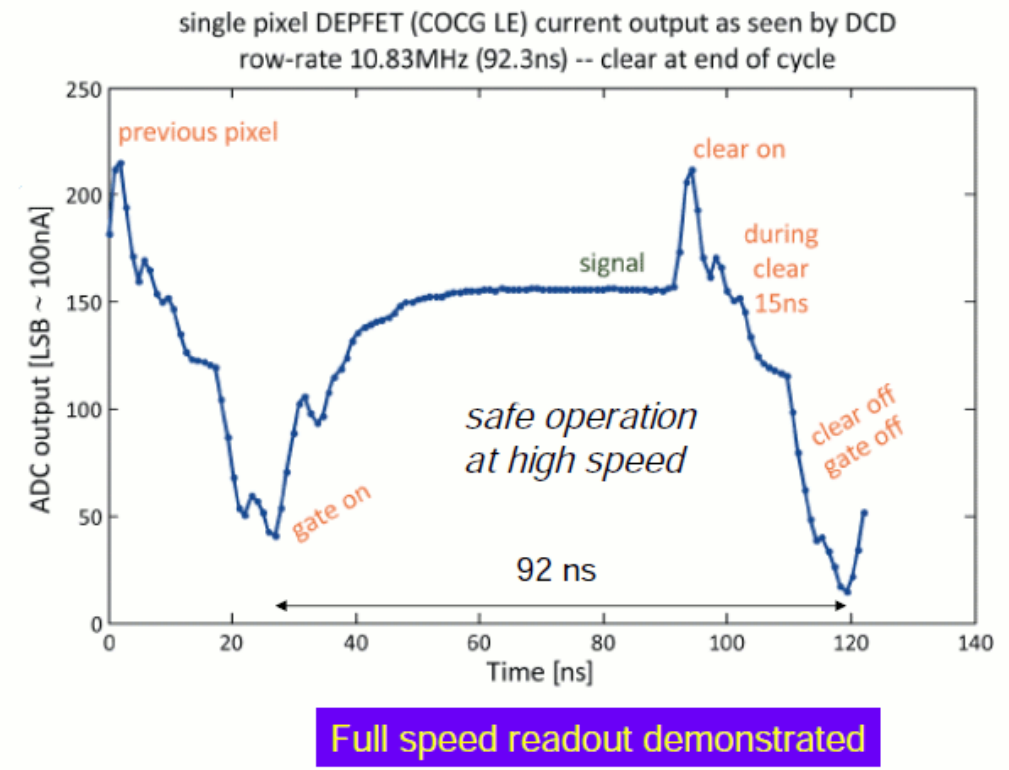
- 8 ladders @ 1st layer, 10 ladders @ 2nd layer
- Full ladder composed of 2 modules with 250x786 pixels
- Pitch 50x55µm^2 @ 1st layer, 50x75µm^2 @2nd layer
- Covers full acceptance of 17°< Θ < 155°
- Total of ~8 Mio. pixels very close to IP for vertexing

Module Concept

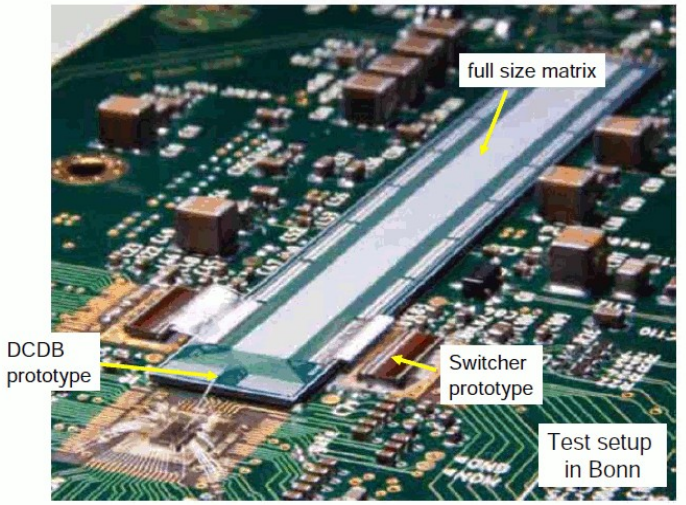
- All silicon module
  - Directly bonded support frame
  - All ASICS's bump bonded
  - 3 Metal layers for circuitry
- Front- end ASICS
  - Switcher-B: controls DEPFET gate and clear lines.
  - DCD-B: multichannel ADC chips; Digitizes drain currents.
  - DHP: digital processor chips; 0-supression & triggered readout
- Rolling shutter readout
  - Read signals row-by-row
  - 4 rows in parallel



Readout Timing

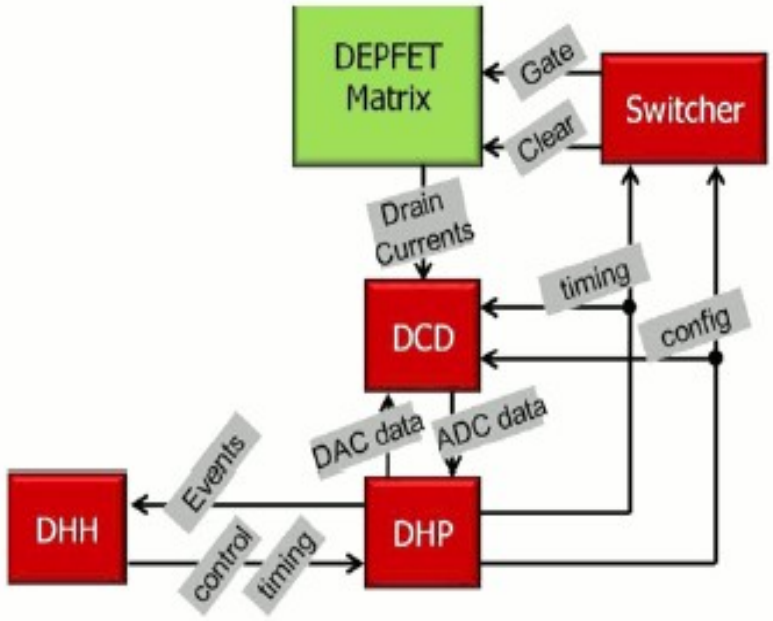


Full speed readout demonstrated



DEPFET PXD readout time is 20us

- Read-Clear cycle in ~100ns
- PXD integrates ~5000 bunch crossings
- 50KHz (Frame rate) vs. 30kHz (L1 Trigger)



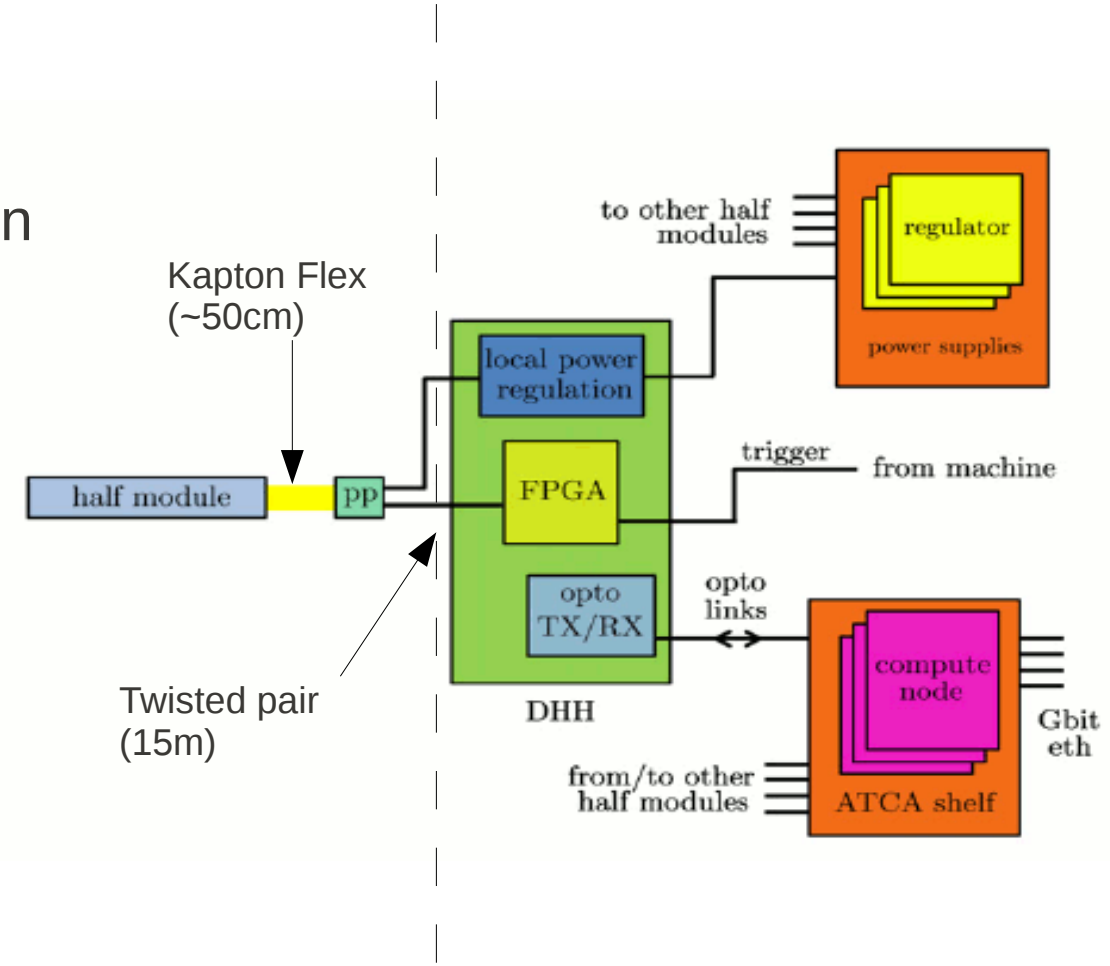
Readout Chain

Passive patch panel (PP)

- High radiation area
- Over-voltage protection
- Sense wires

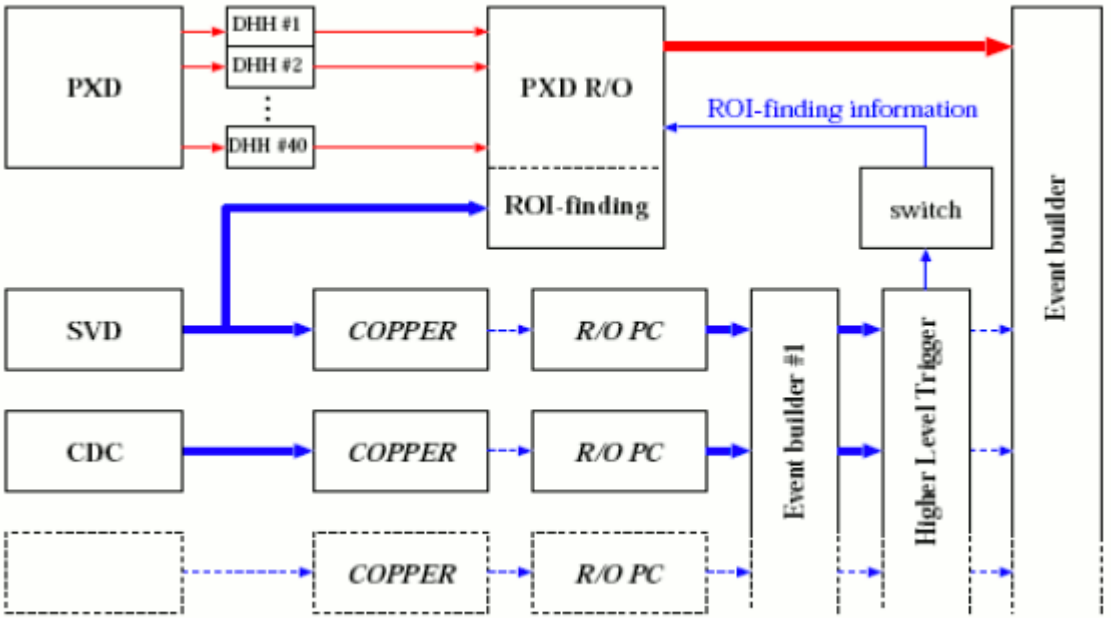
Total of 40 DHH modules

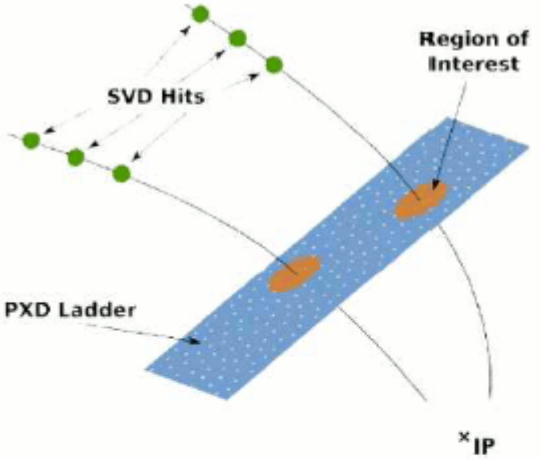
- Easy access
- Commercial FPGA's



PXD DAQ Layout

- PXD sends ~1MB/event at rate ~30kHz to PXD DAQ
- Required size reduction /10 using SVD (+CDC) tracks
- Required rate reduction /5 using HLT tag

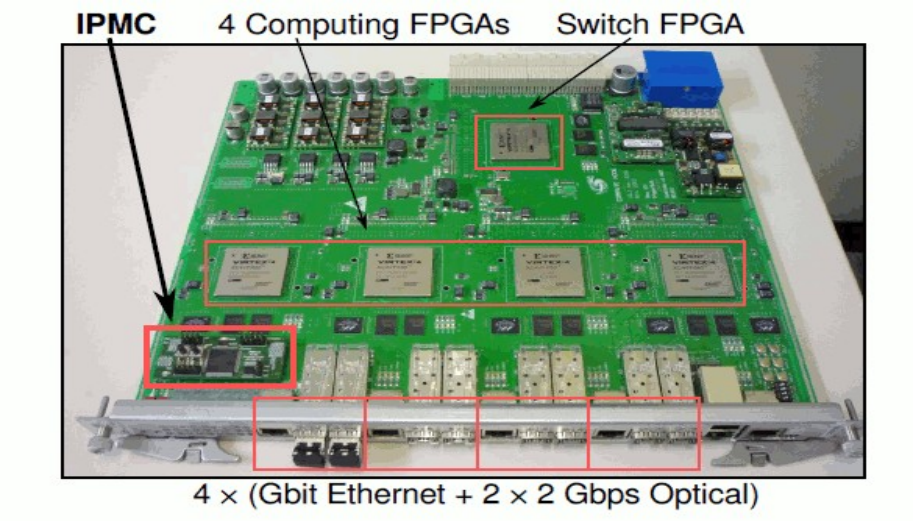


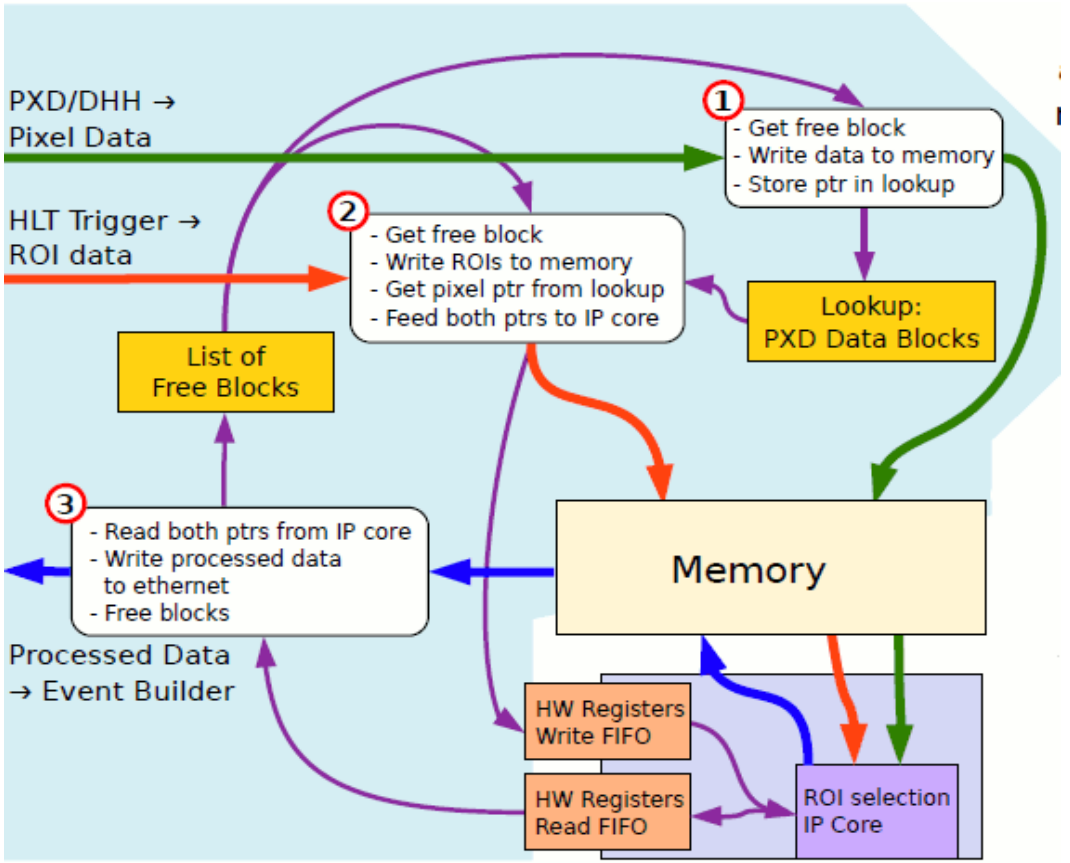


Noise reduction by track association: Only pixels inside the ROI will be stored (+ high energy deposition clusters)

PXD DAQ: ATCA System

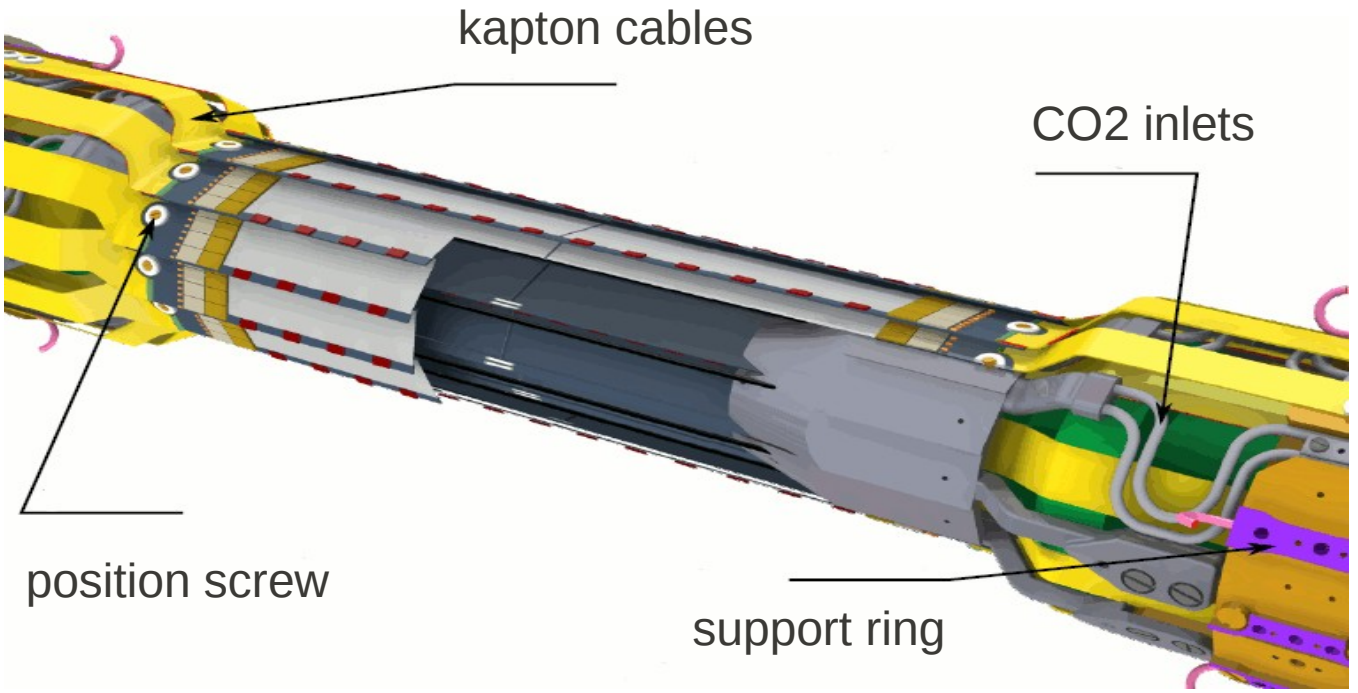
- Shelf with ~10 Compute Nodes
- Gbit Ethernet/FPGA
- 2 x 6.25 Gbps optical/FPGA
- 4 x 4GB DDR2 RAM memory
- Achieved 380MB/s read and 360MB/s write

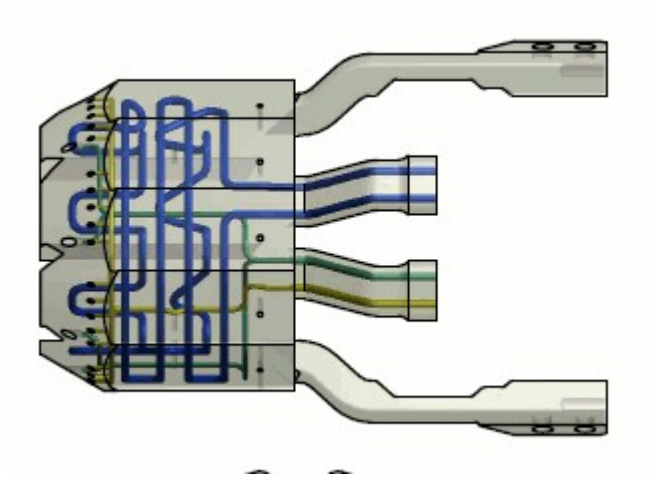


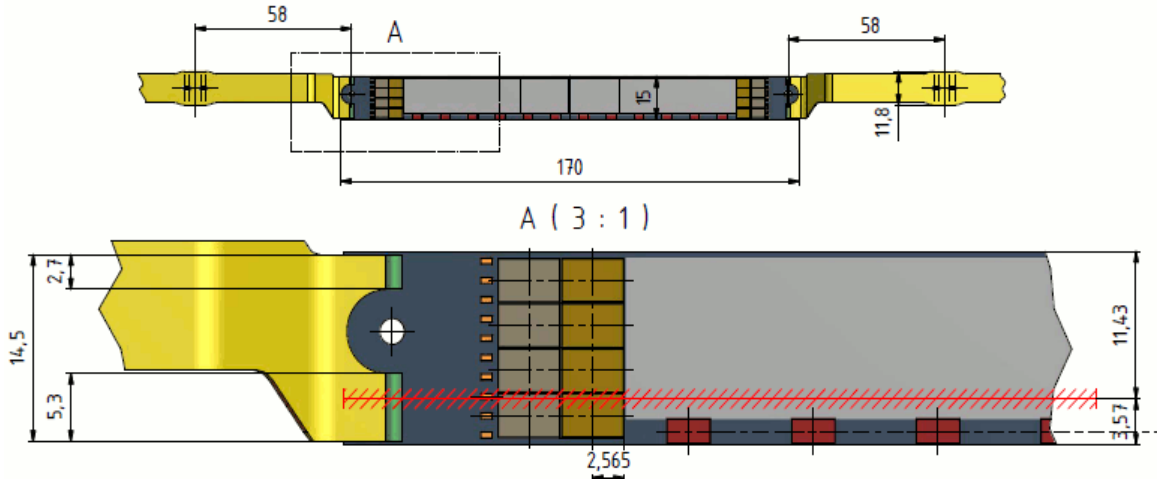


Highly Parallized ROI algorithm:
:- 4 IP core / FPGA
:- 31 ROI's / core

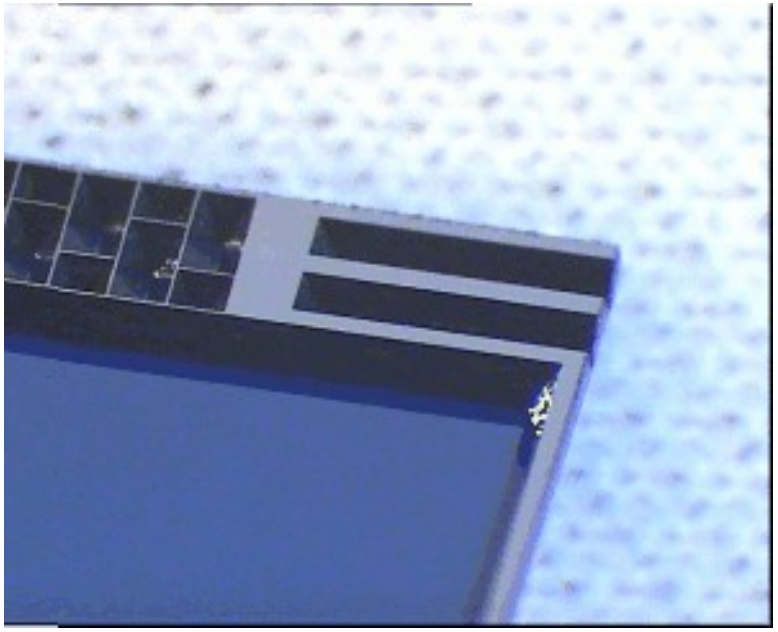
Mechanical Design

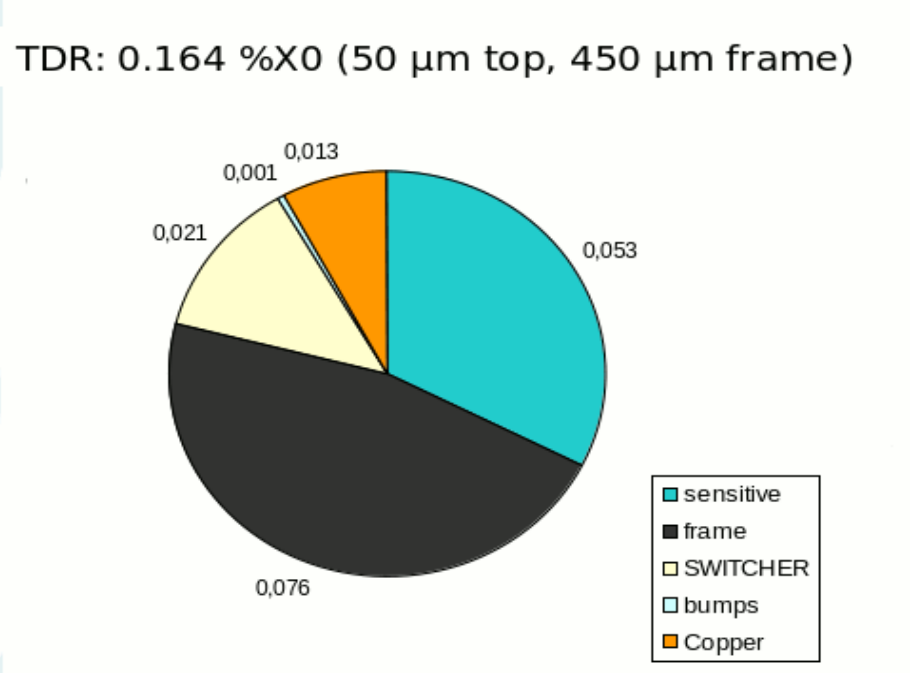


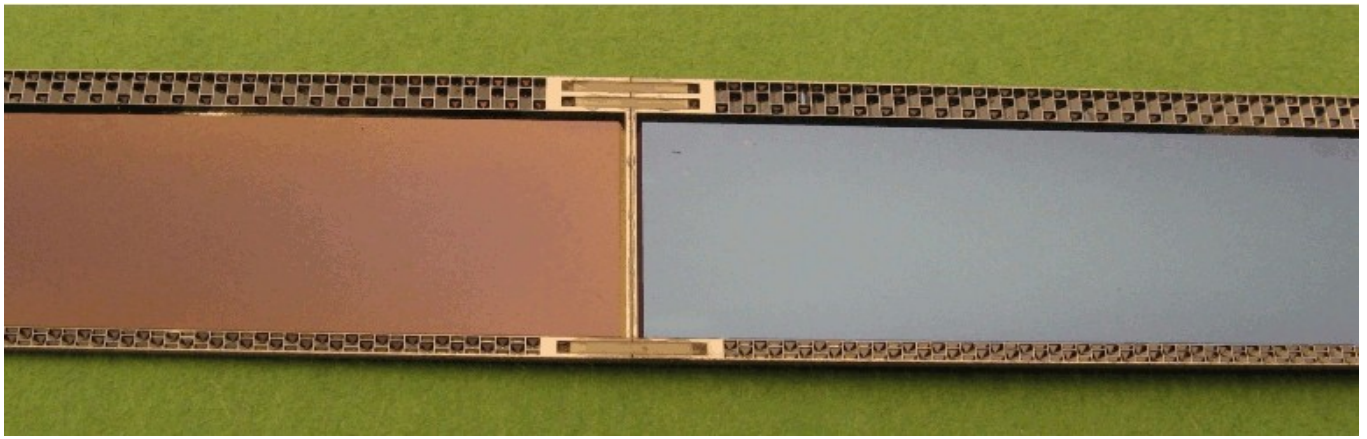




Thinning & Material Budget



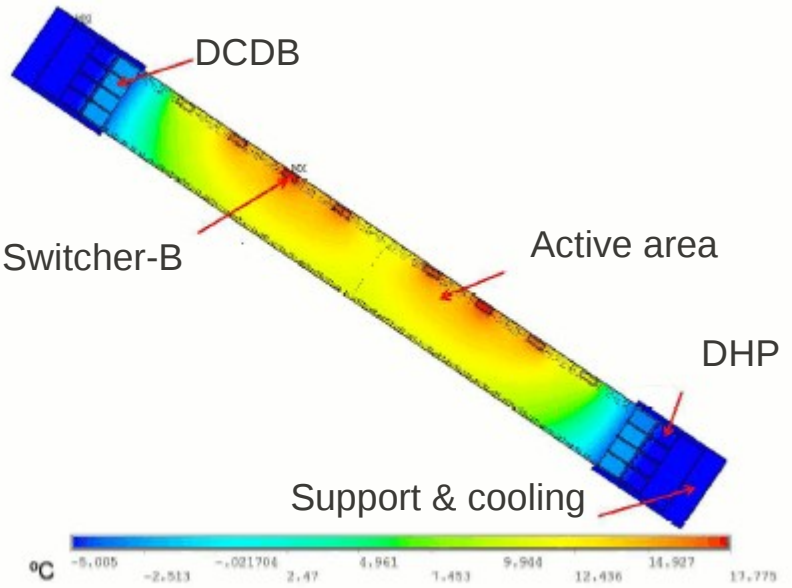




Thermal Environment

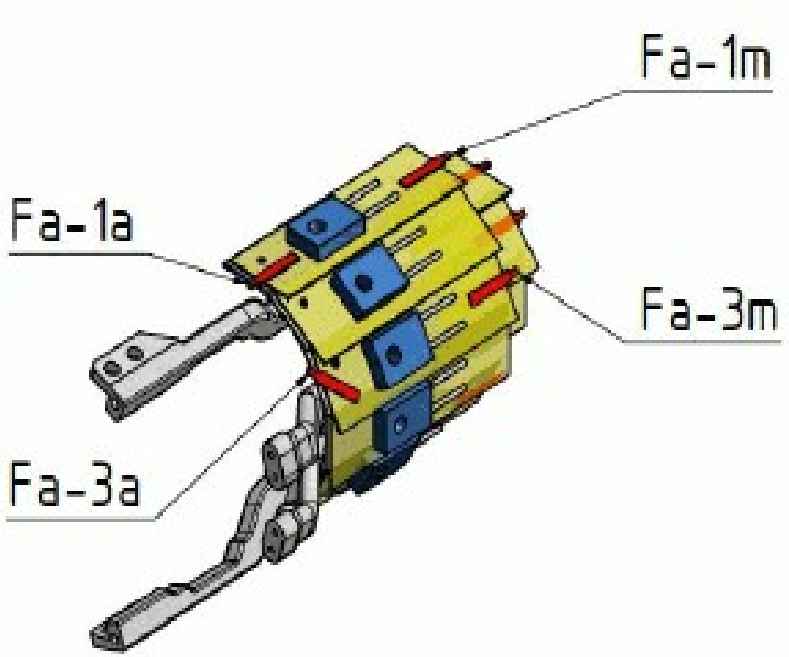
- Total heat load of 360W = 40 x 9W
  - 0.5W switchers
  - 0.5W DEPFET pixels
  - 6W DCD's && 2W DHP's
- DEPFET's < 30°C
  - Limit leakage currents
  - uniform response
- ASIC's < 60°C
- End of stave cooled by conducti
  - evaporative CO2 cooling
- Inner module cooled by convection
  - cold dry air blown at Switcher-B

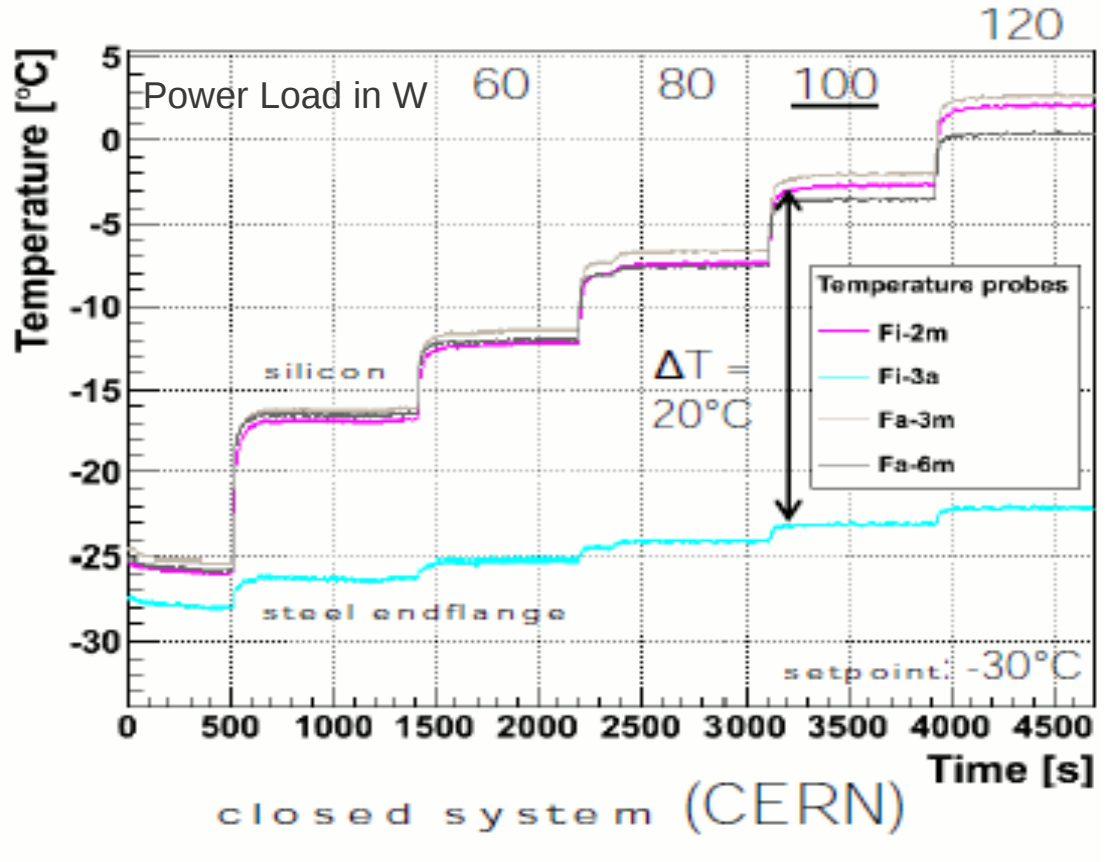
Thermal Simulations



Now, cooling tests ->

CO2 Cooling Test Setups

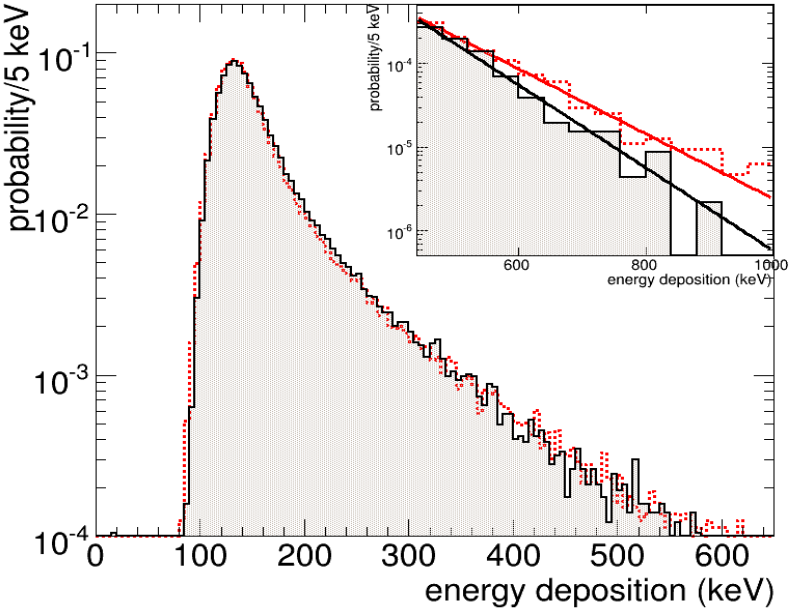


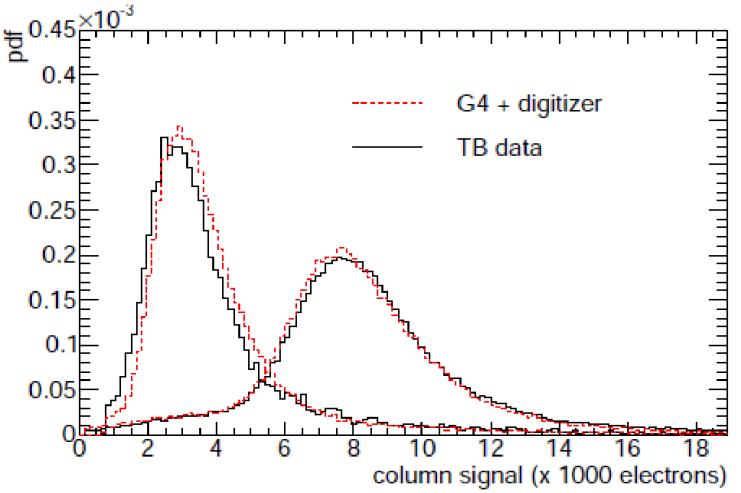


- CO2 cooling works with closed CO2 system @ CERN
- Common CO2 cooling system PXD + SVD in progress

DEPFET Test Systems

- Tests of DEPFET prototype devices
- Validation of fast DEPFET simulation
- Response to minimum ionizing particles @ CERN SPS:
  - Use most probable signal to extract $g_q = \Delta I_D / Q$
  - 6µm gate length -> ~300pA/e-
  - 5µm gate length -> ~650pA/e-
  - Resolution ~1µm @20x20µm^2 pitch and 450µm thick.
- New prototypes thinned down to 50µm thickness tested





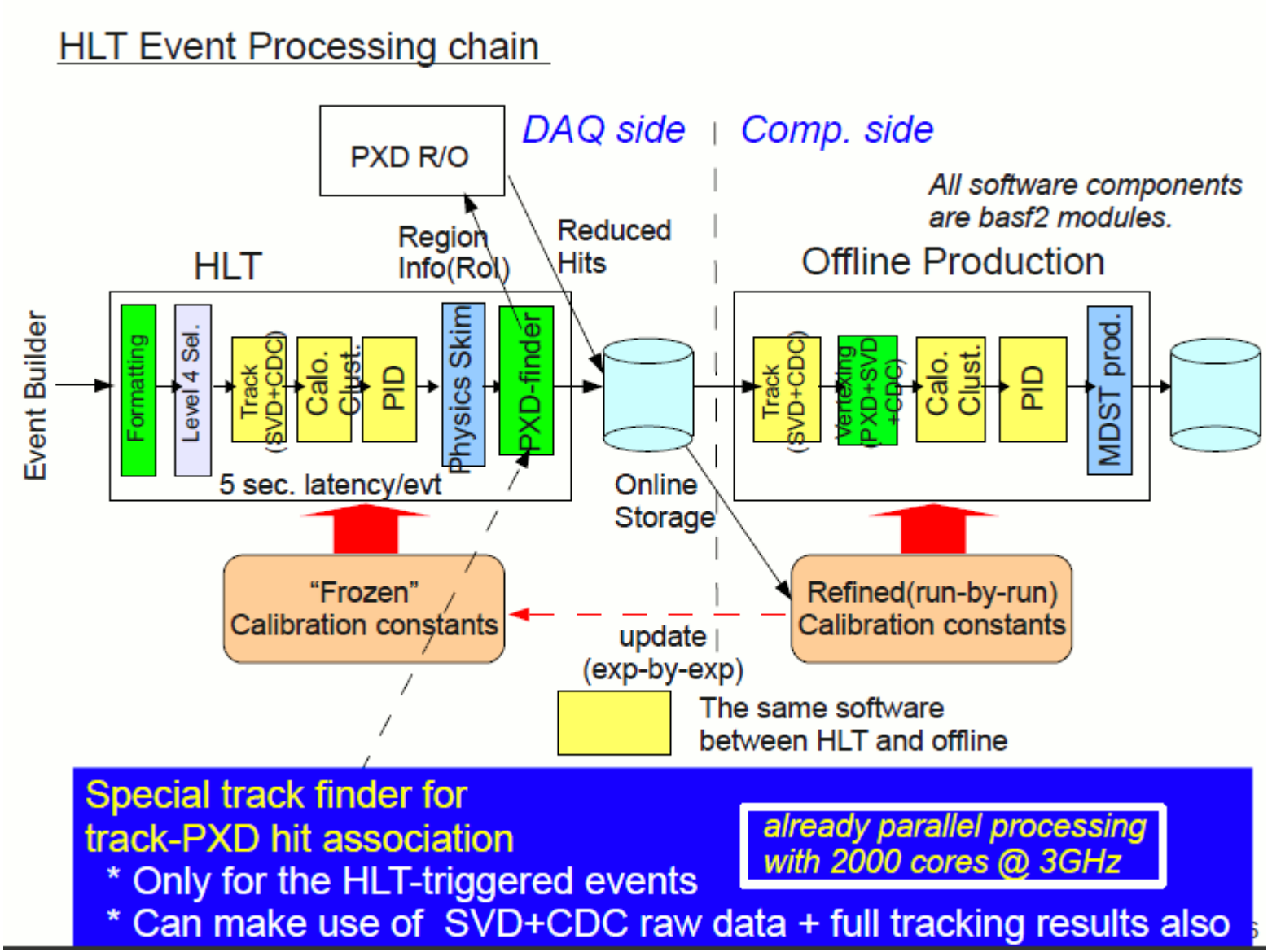
In Summary: Recent Achievments

- Prototype system with DEPFET (50um) DCDB and SWB operated in lab measurments:
  - Sample-Clear cycle in 100ns → full speed!!
  - S/N ~20 → goal is S/N ~20-40
- CO2 cooling of endflange with open CO2 system demonstrated and working.
- ATCA based PXD DAQ system is operational
- First combined simulation of backgrounds (QED, radiative bhabba, Touchek)
  - Occupancy in 1st layer < 1% → PXD DAQ can handle 3%

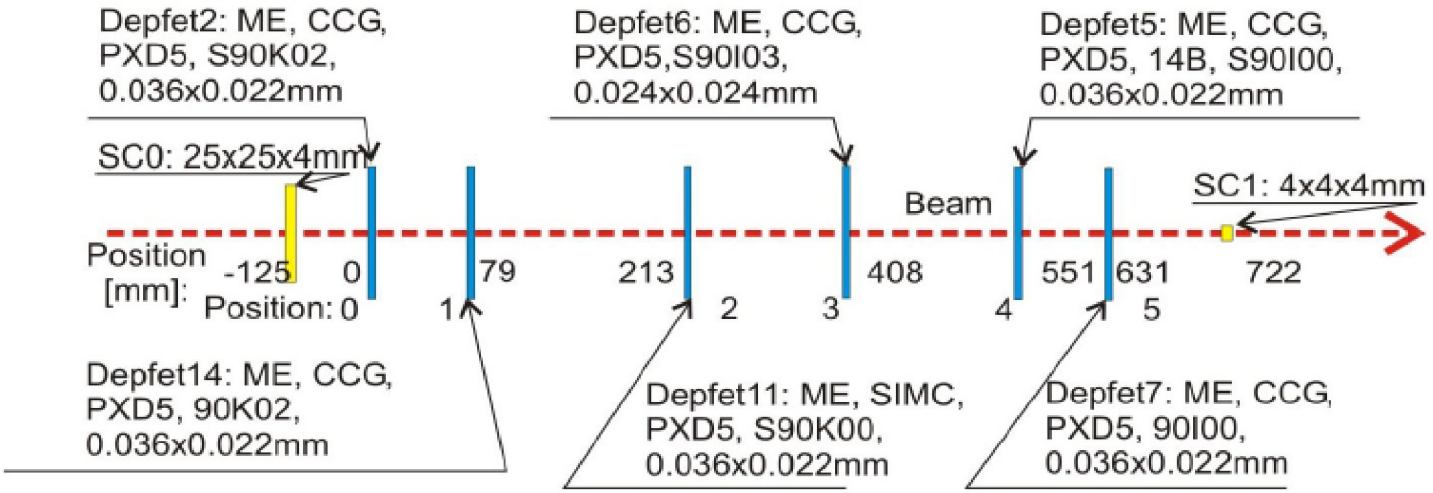
First collision data expected 2014; PXD in detector in 2015

Thank you for your attention

Backup Slides


HLT Event Processing chain
PXD R/O
DAQ side
Comp. side
All software components are basf2 modules.
Region Info(RoI)
Reduced Hits
HLT
Offline Production
Event Builder
Formatting
Level 4 Sel.
Track (SVD+CDC)
Calo. Clust.
PID
Physics Skim
PXD-finder
Track (SVD+CDC)
Vertexing (PXD+SVD +CDC)
Calo. Clust.
PID
MDST prod.
5 sec. latency/evt
Online Storage
"Frozen" Calibration constants
Refined(run-by-run) Calibration constants
update (exp-by-exp)
The same software between HLT and offline
Special track finder for track-PXD hit association
* Only for the HLT-triggered events
* Can make use of SVD+CDC raw data + full tracking results also
already parallel processing with 2000 cores @ 3GHz

DEPFET test beam campaigns



- Data from DEPFET test beams with 120GeV pions at CERN SPS collected in 2008/2009.
- DEPFET only telescope: ILC type DEPFET's with 128x64 or 256x64 pixels.
- Non zero suppressed analog readout at slow rate of ~2us per frame with S3A/S3B boards.
- Systematic studies for DEPFET characterization:
  - High statistics and low occcupancy scans → point resolution
  - Scan of DUT incidence angle
  - Scan of beam energy (down to 40GeV)
  - Scan of DEPFET backplane voltage ...