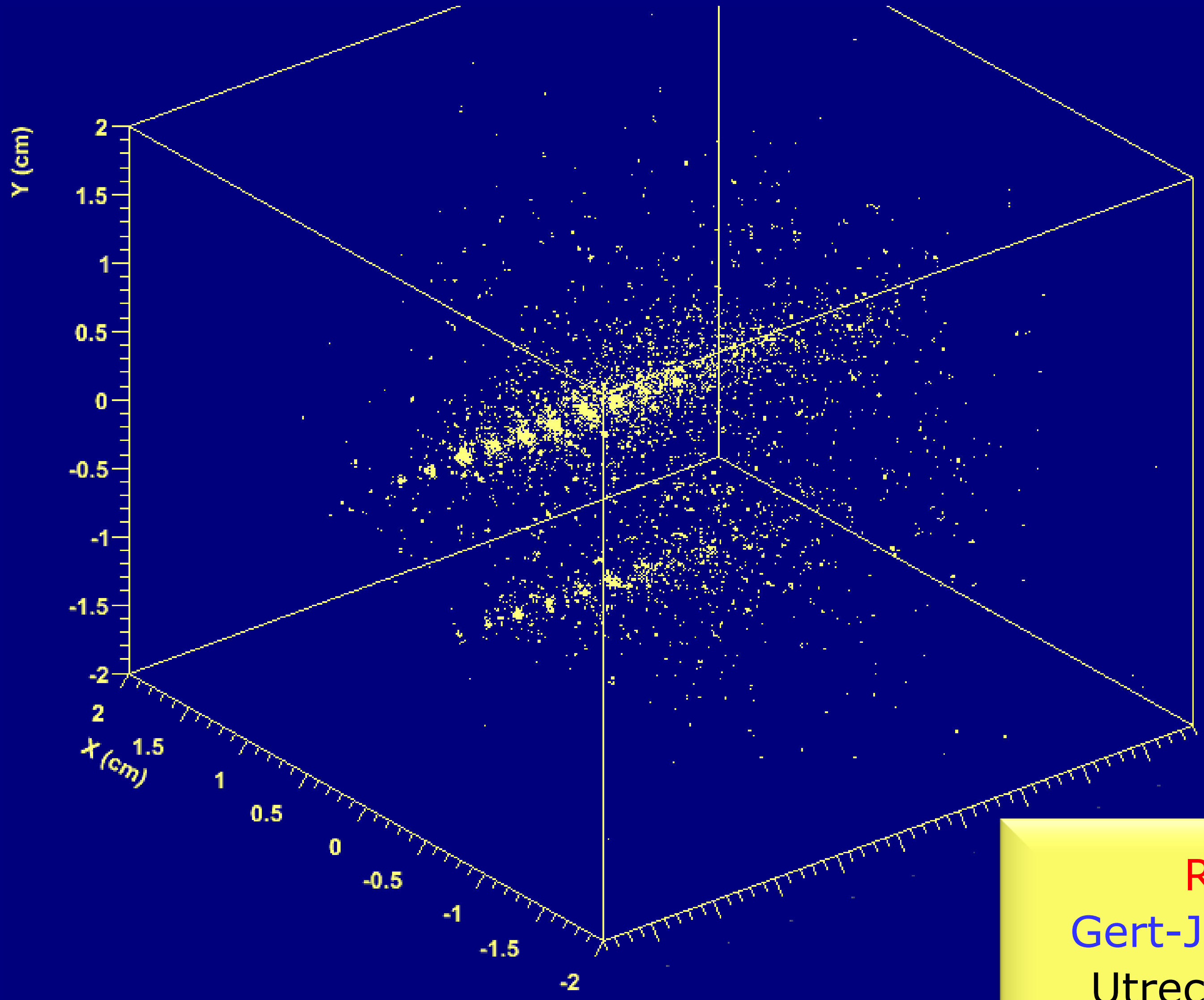
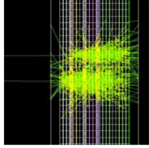
Extremely fine-grained Electro Magnetic Calorimeter



RD'11

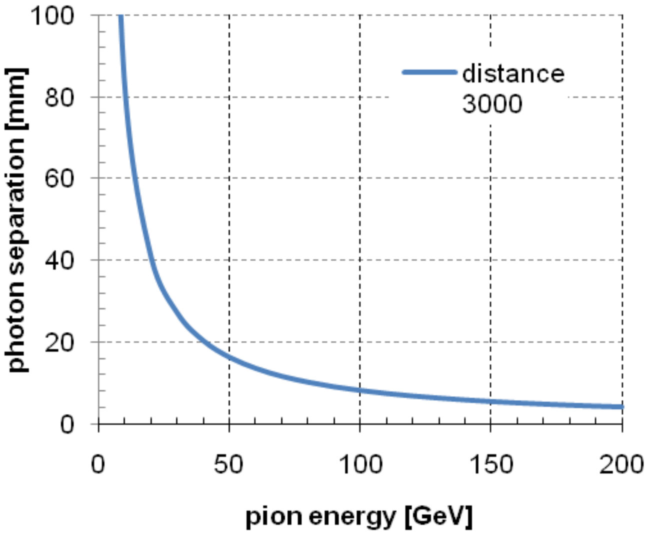
Gert-Jan Nooren

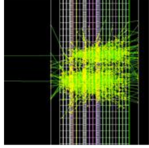
Utrecht/Nikhef



fine grained calorimetry

- why
  1. shower shape analysis for PID
  2. particle flow: need to track particles
  3. separate π^0 decay photons from direct photons
     - *example at 3 m*



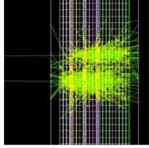


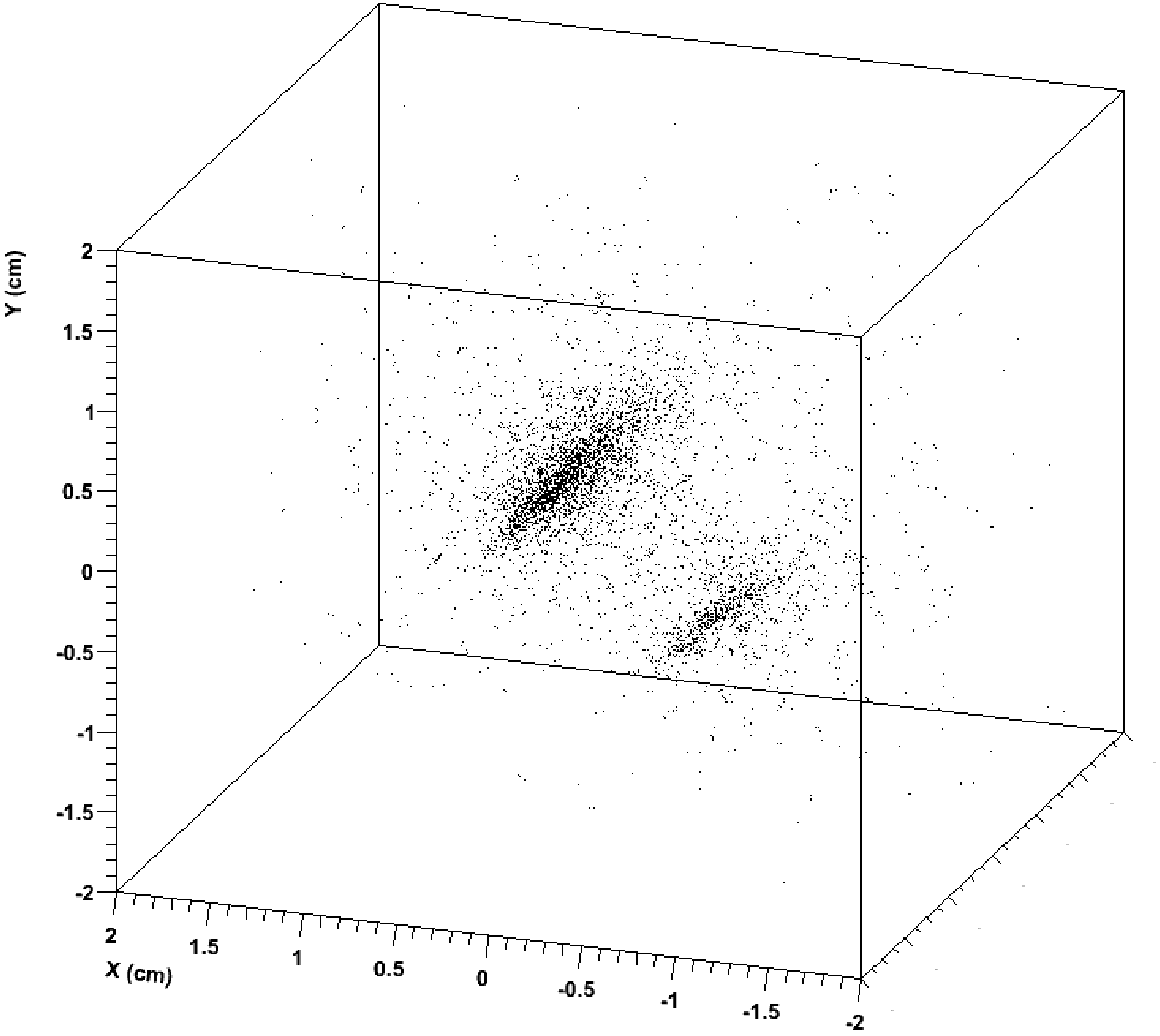
fine grained calorimetry

- why
  1. particle flow: need to track particles
  2. shower shape analysis
  3. separate π_0 decay photons from direct photons
- what
  - lateral 1 mm, longitudinal 1 X_0
  - small Moliere radius → compact, W + silicon
- many channels
  - only feasible with digital calorimetry, i.e. particle counting
    - particle density 10^3 mm^{-2}
    - may need even more, smaller pixels!

100 GeV π^0 GEANT simulation

0.1 mm pixels, 24 layers $1.14X_0$





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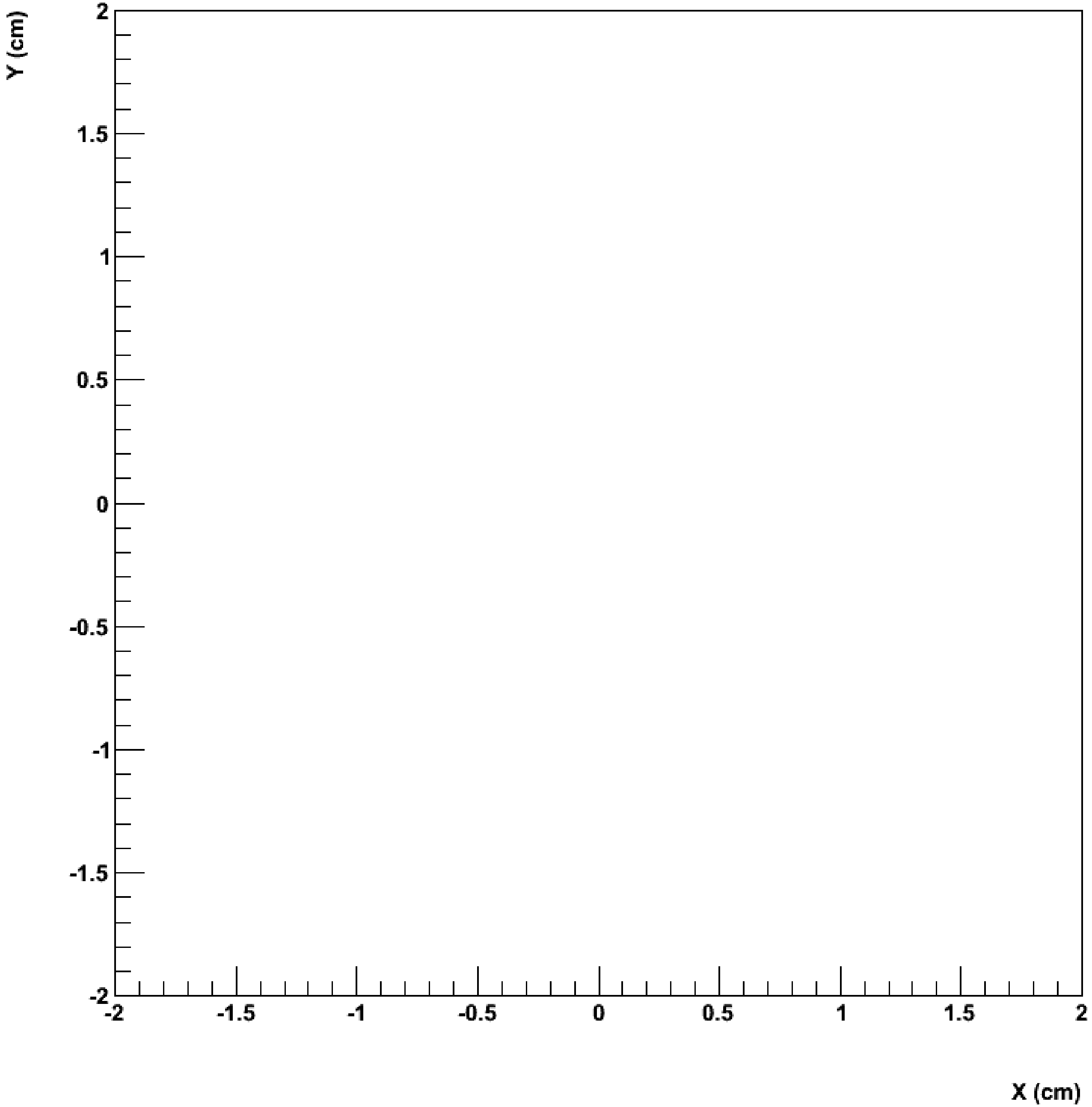

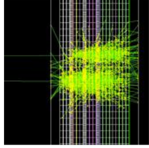

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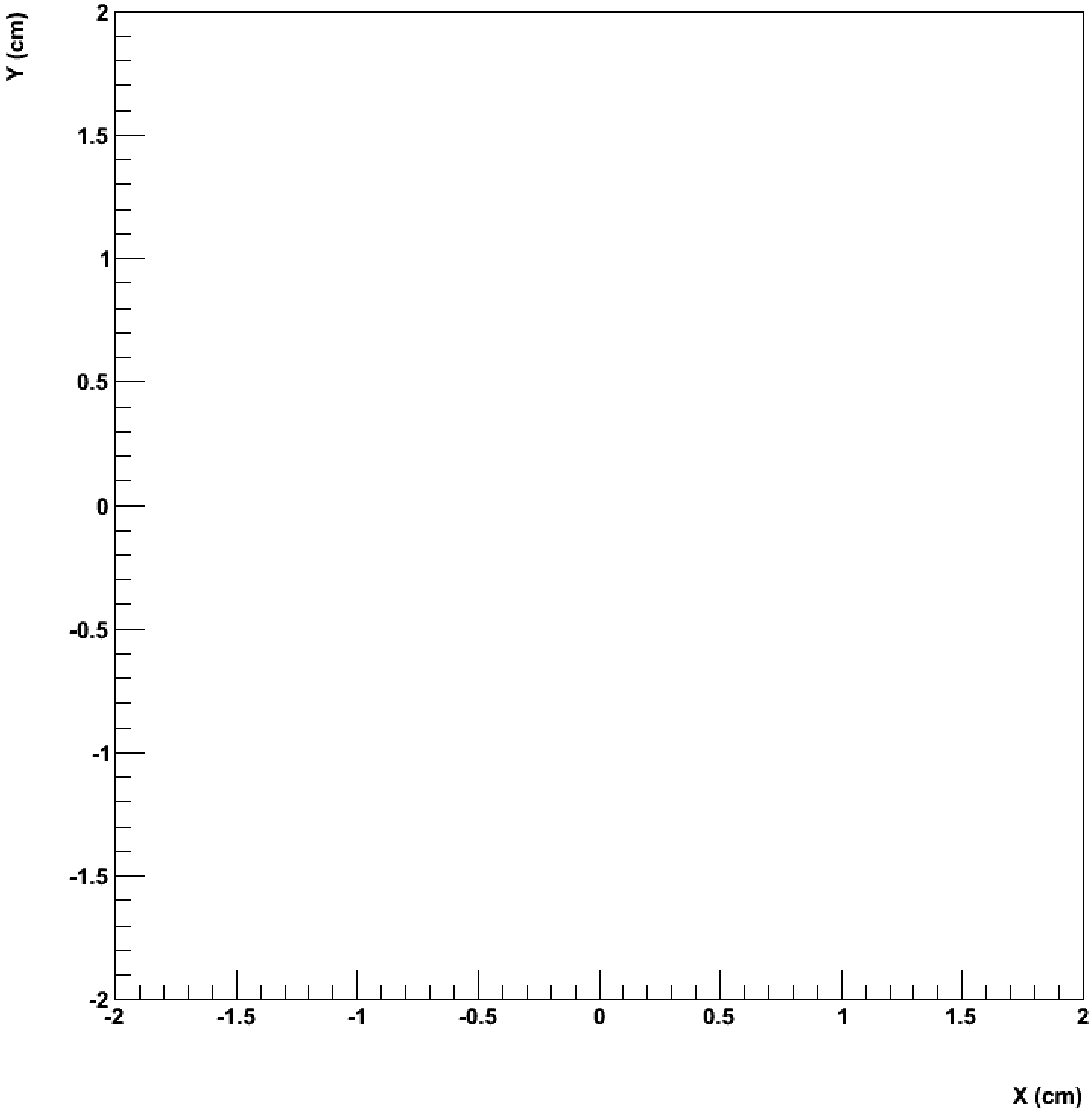

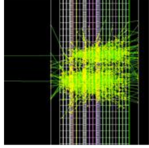

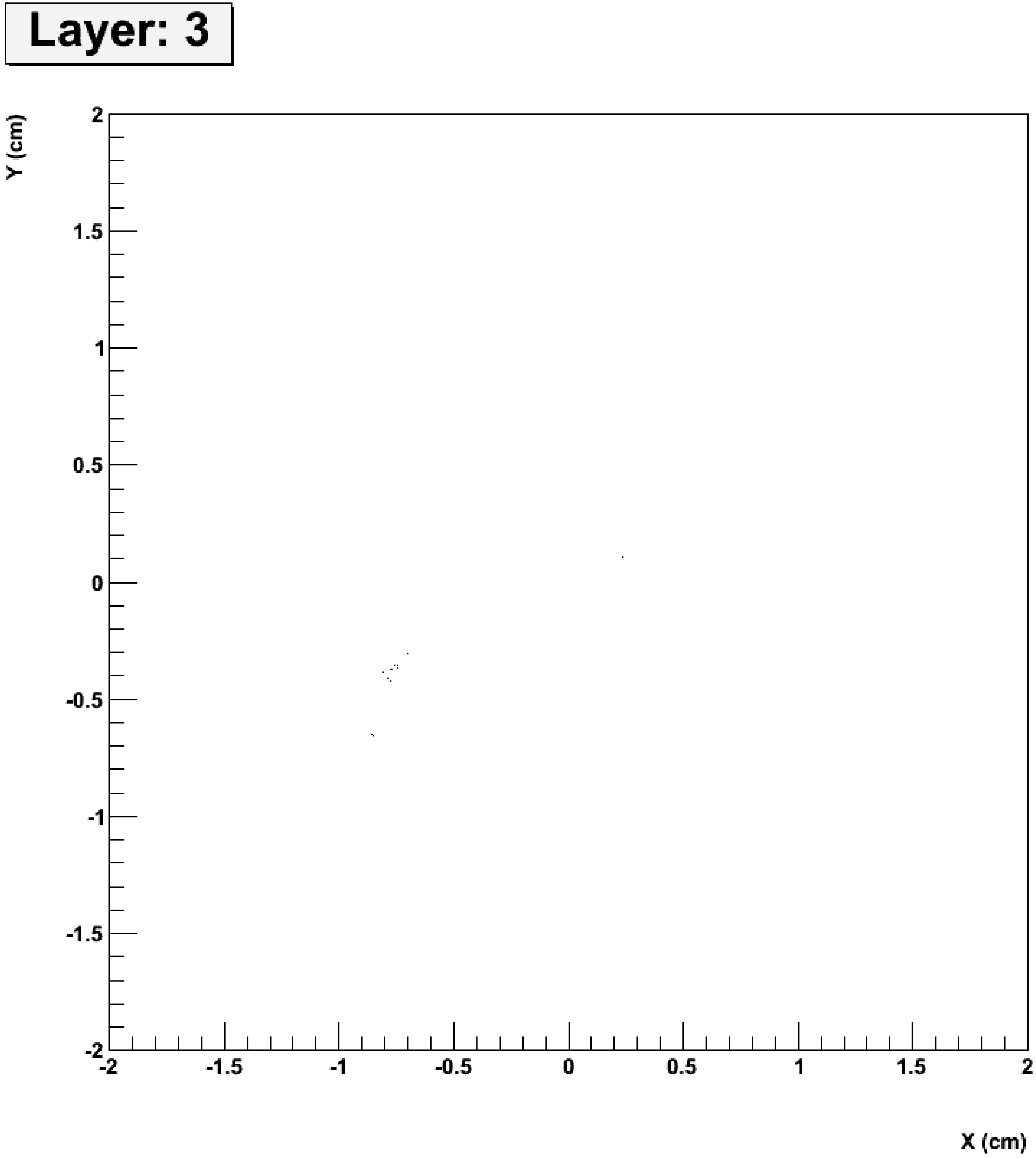
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X (cm)
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1.5
1
0.5
0
-0.5
-1
-1.5
-2
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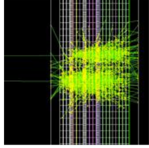
-1
-0.5
0
0.5
1
1.5
2

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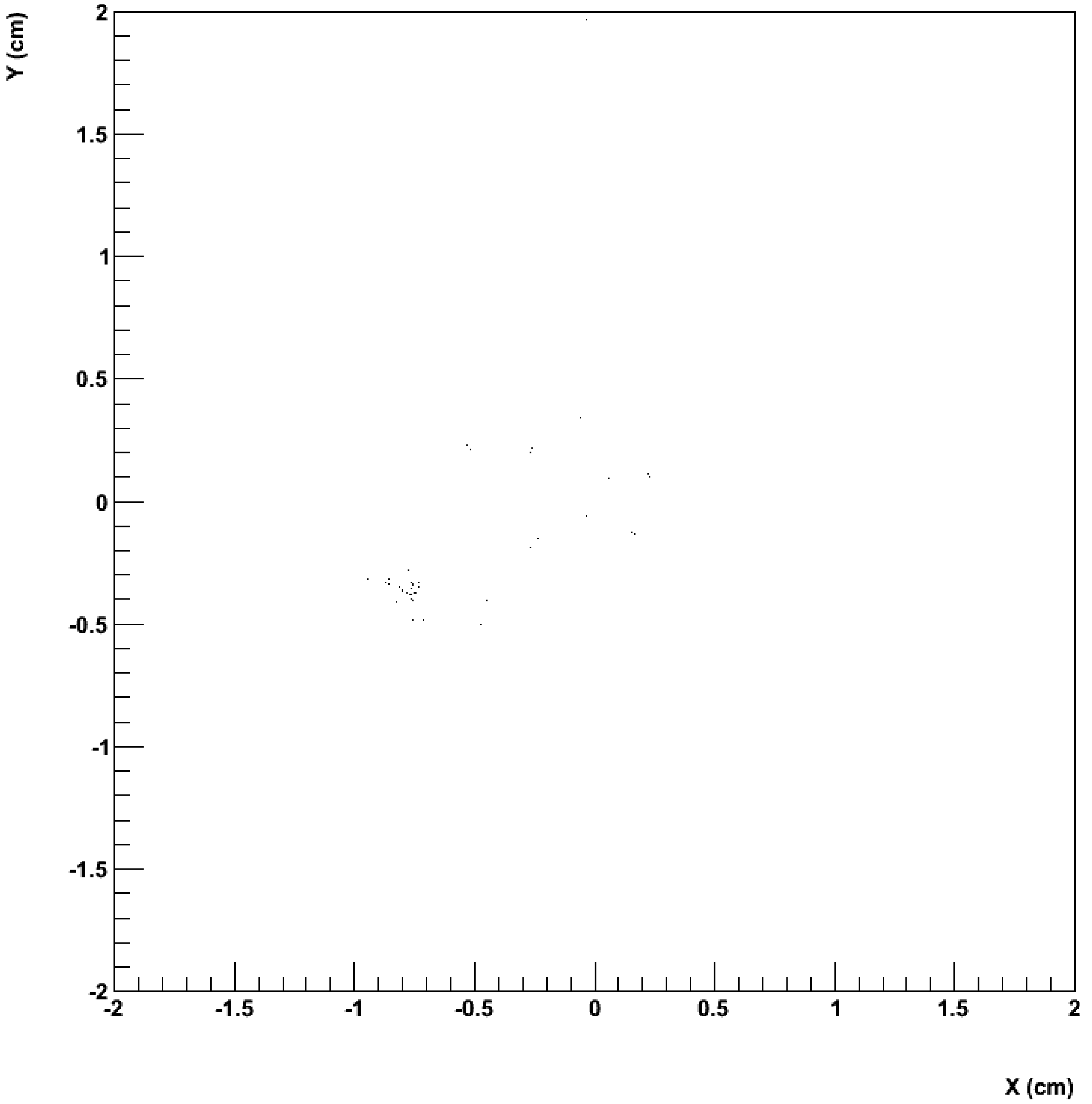
Y (cm)
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1.5
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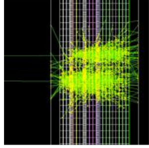
1
1.5
2
X (cm)



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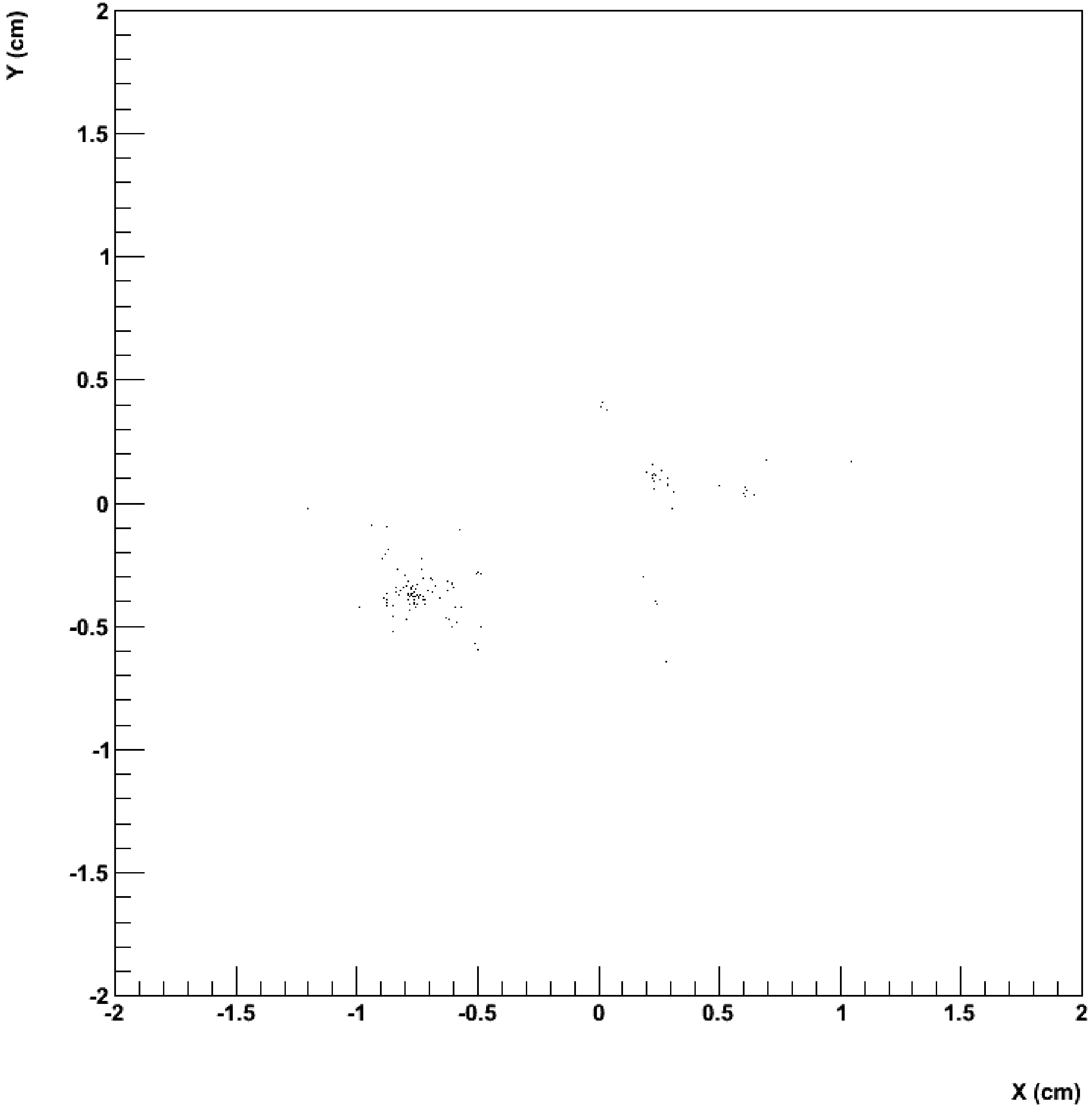

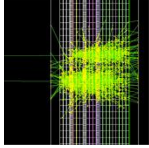

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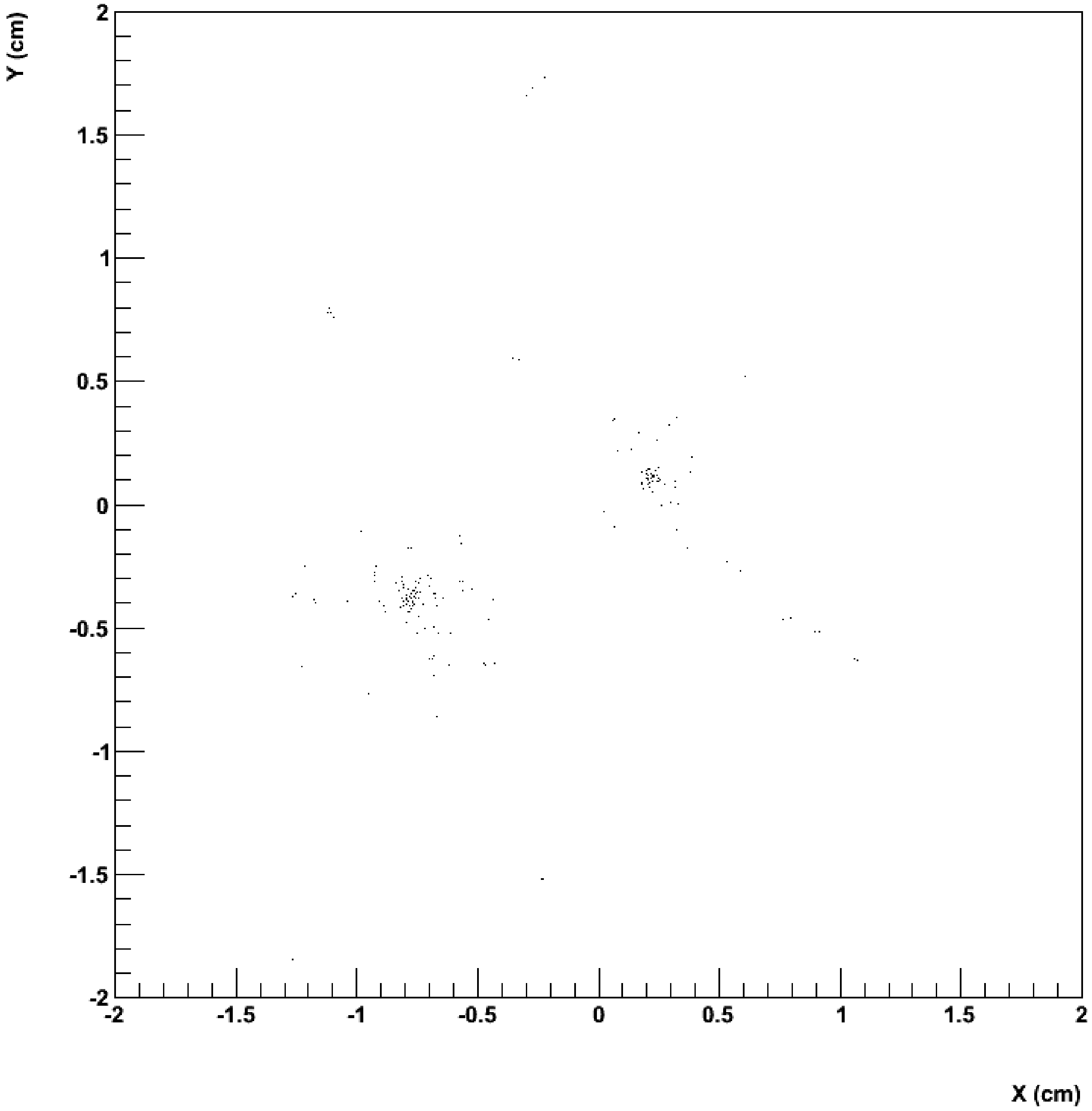

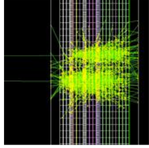

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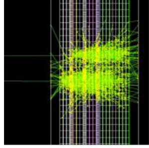

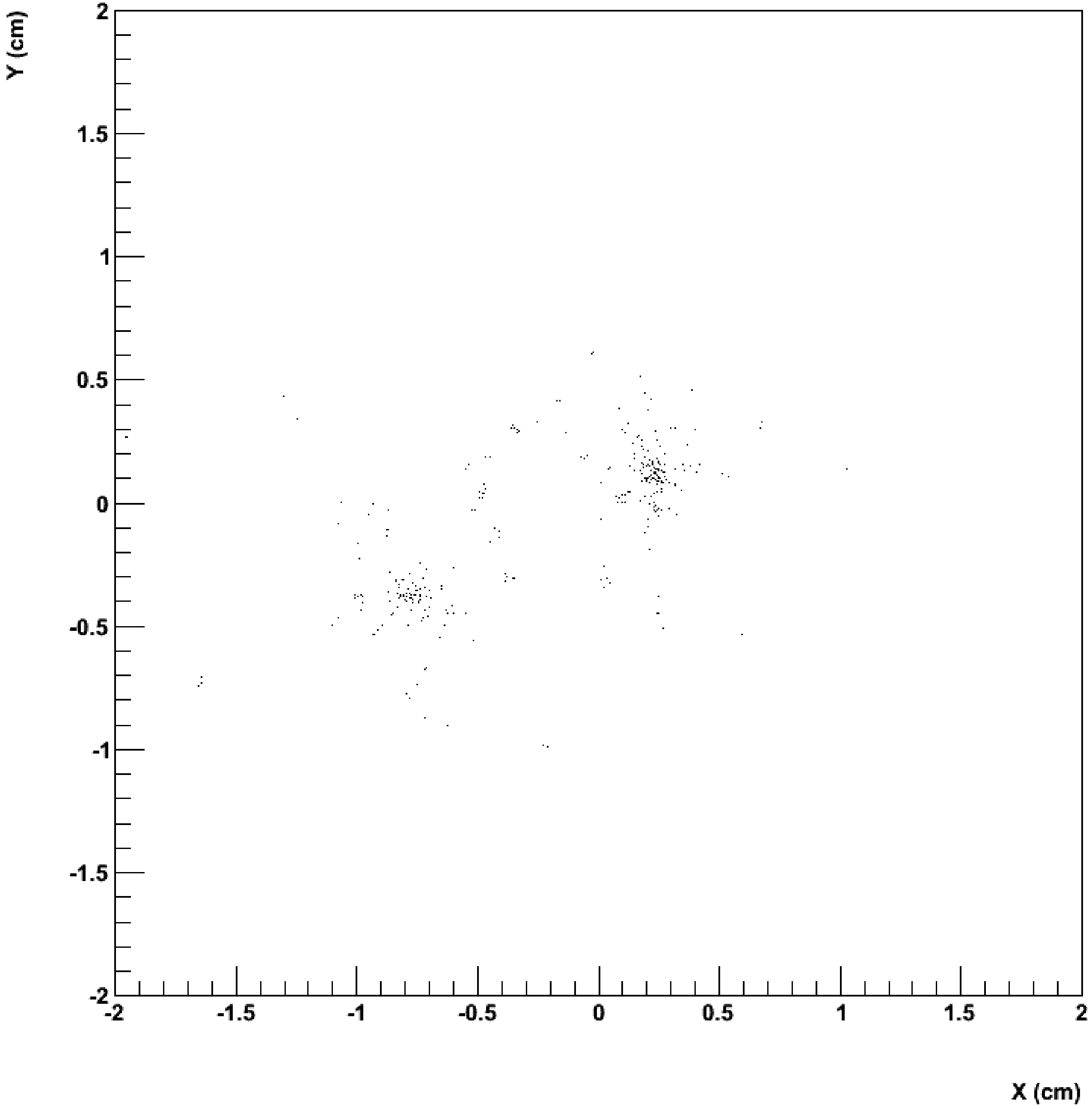

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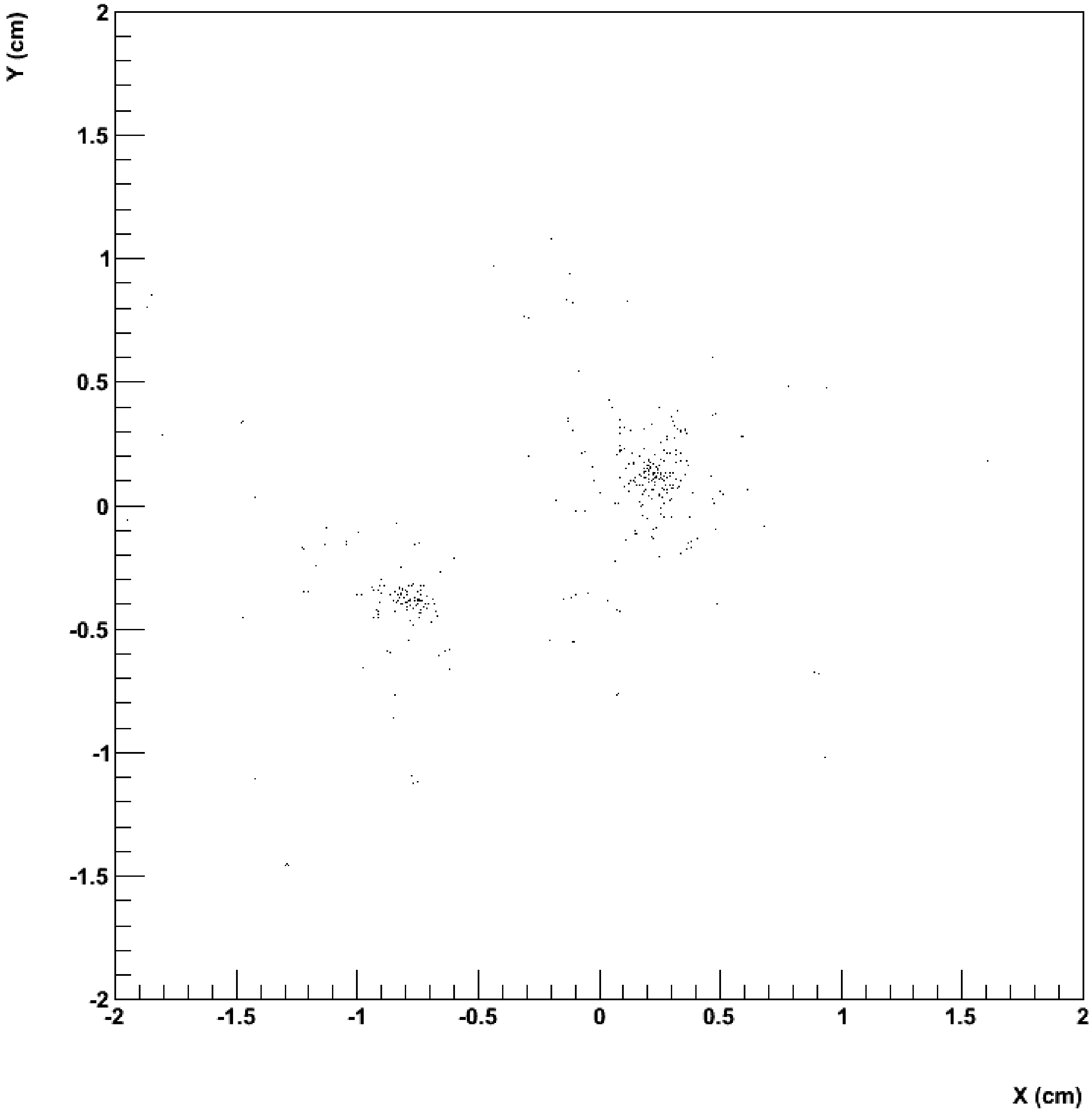

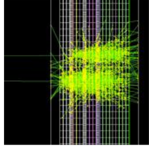

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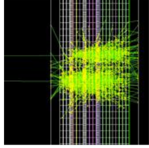

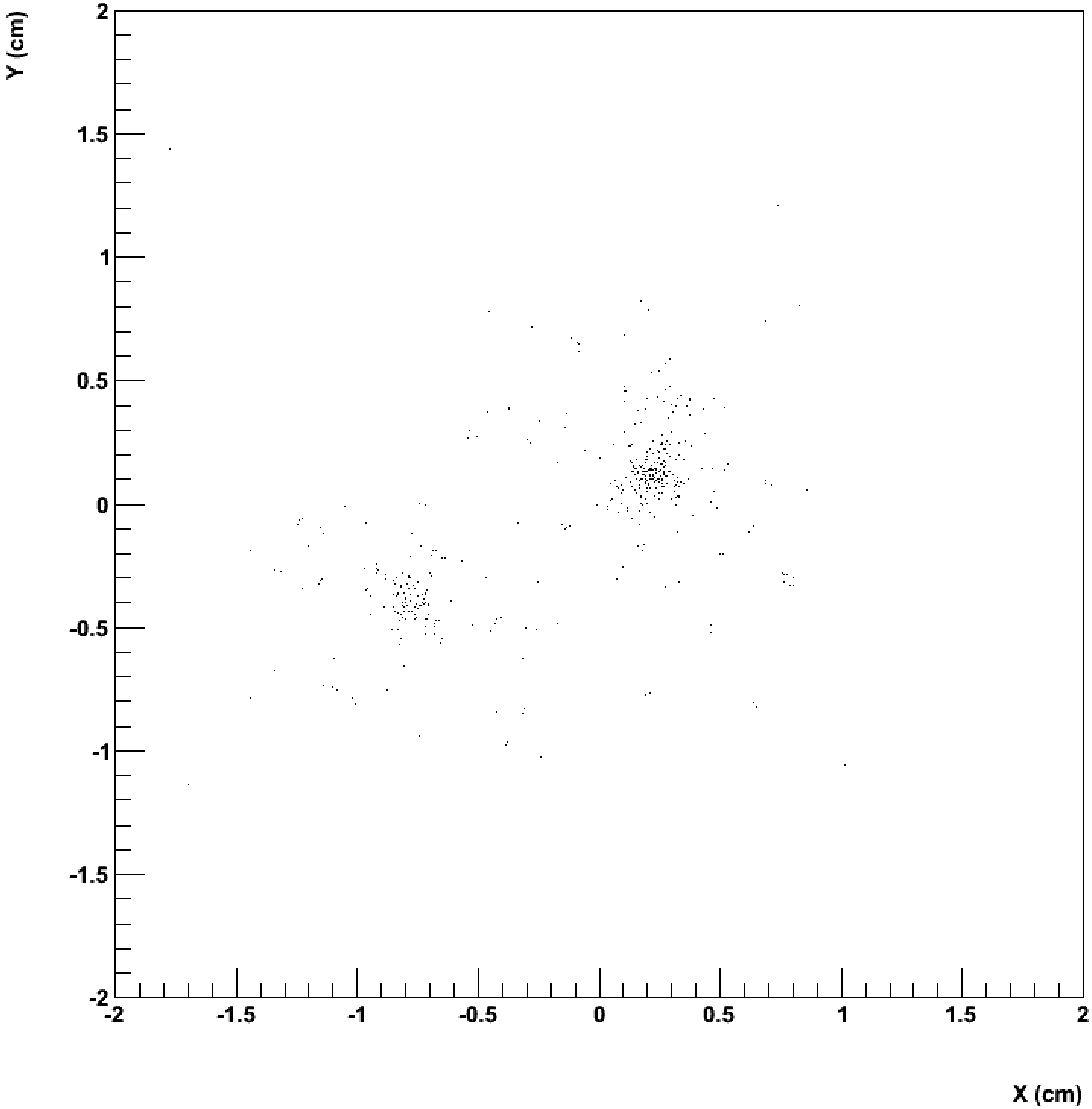

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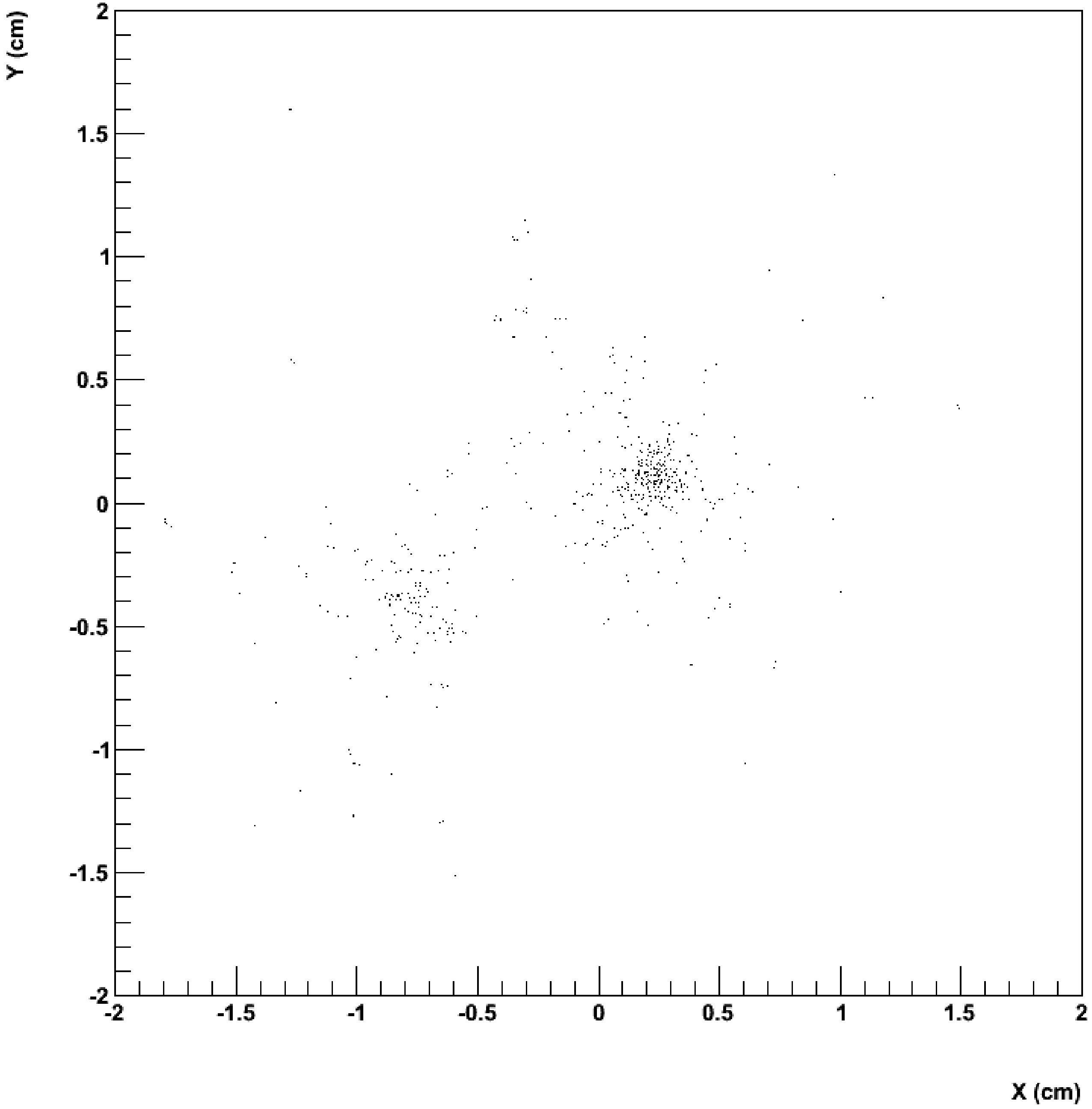

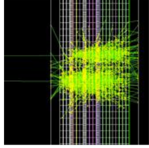

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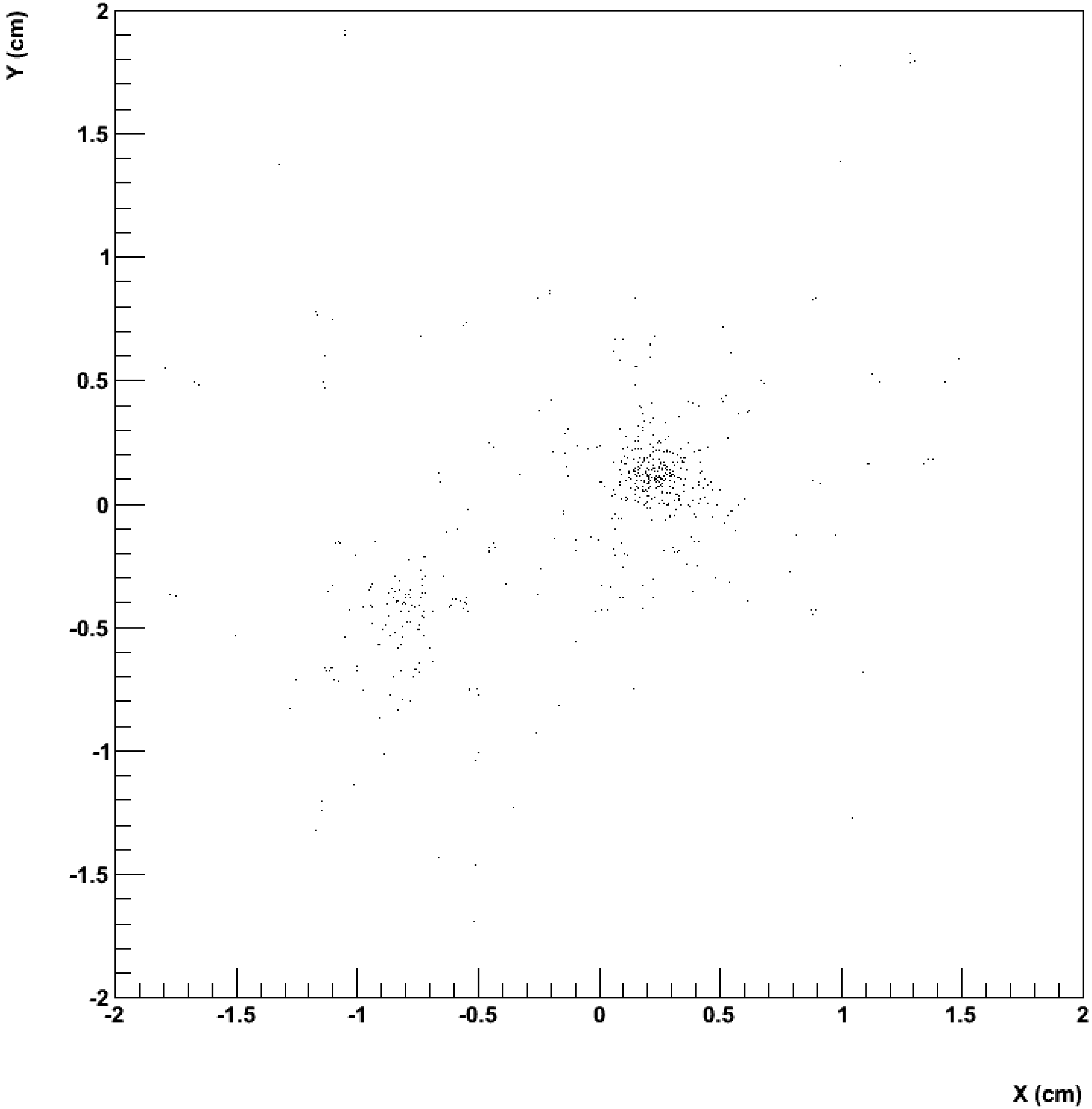

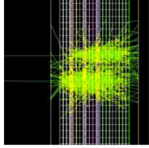

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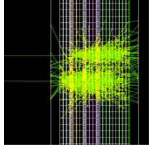

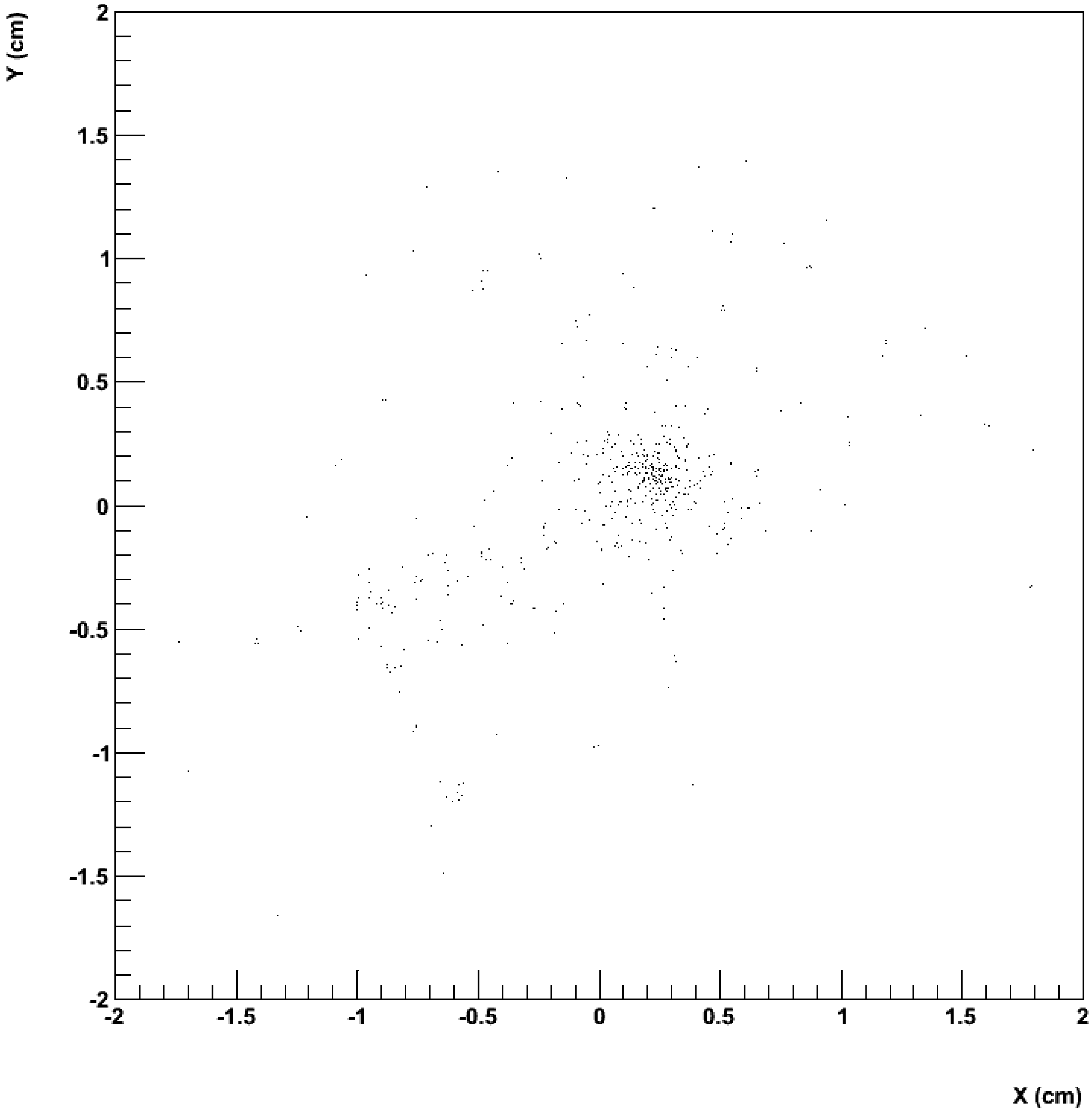

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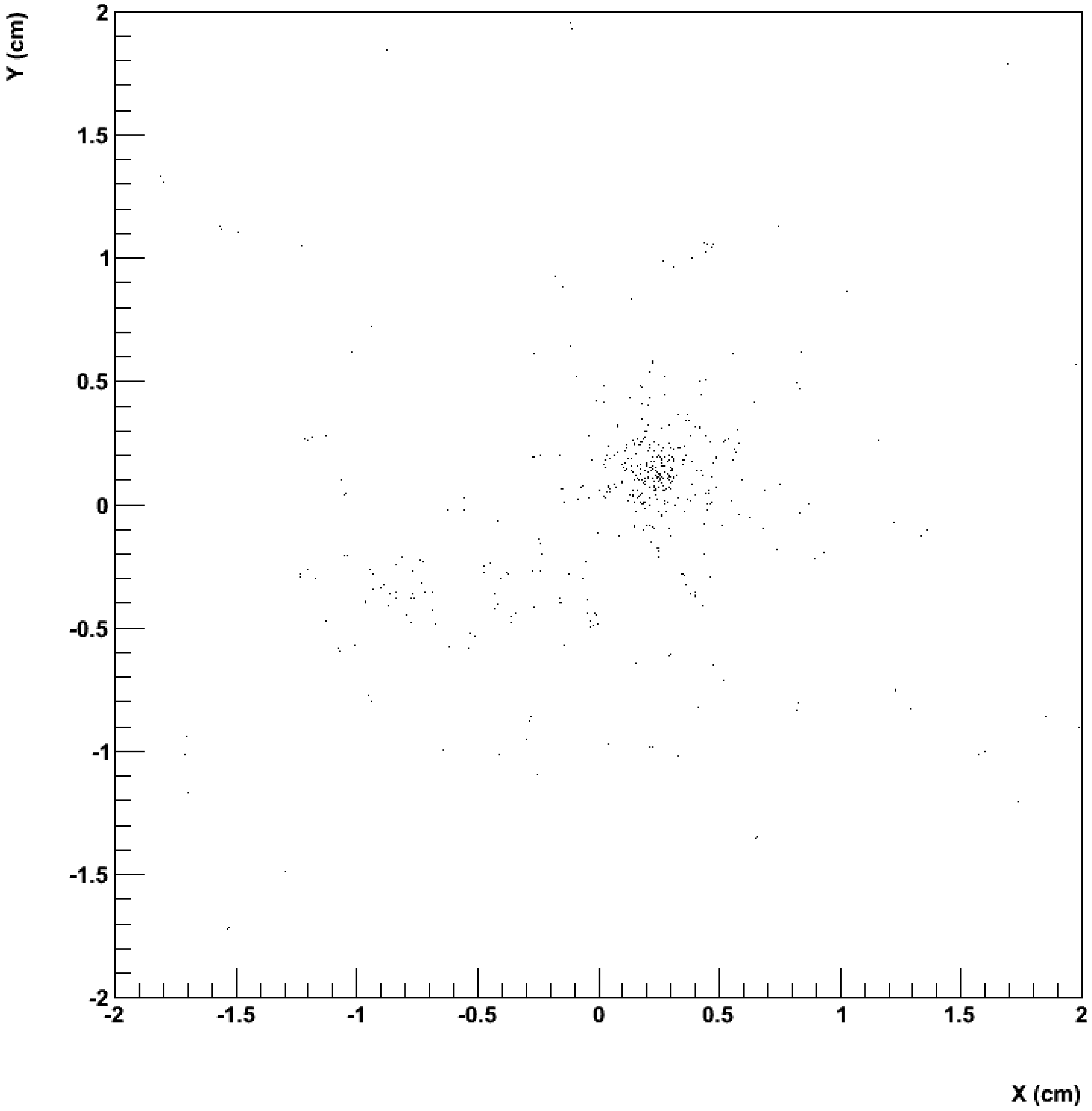

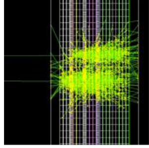

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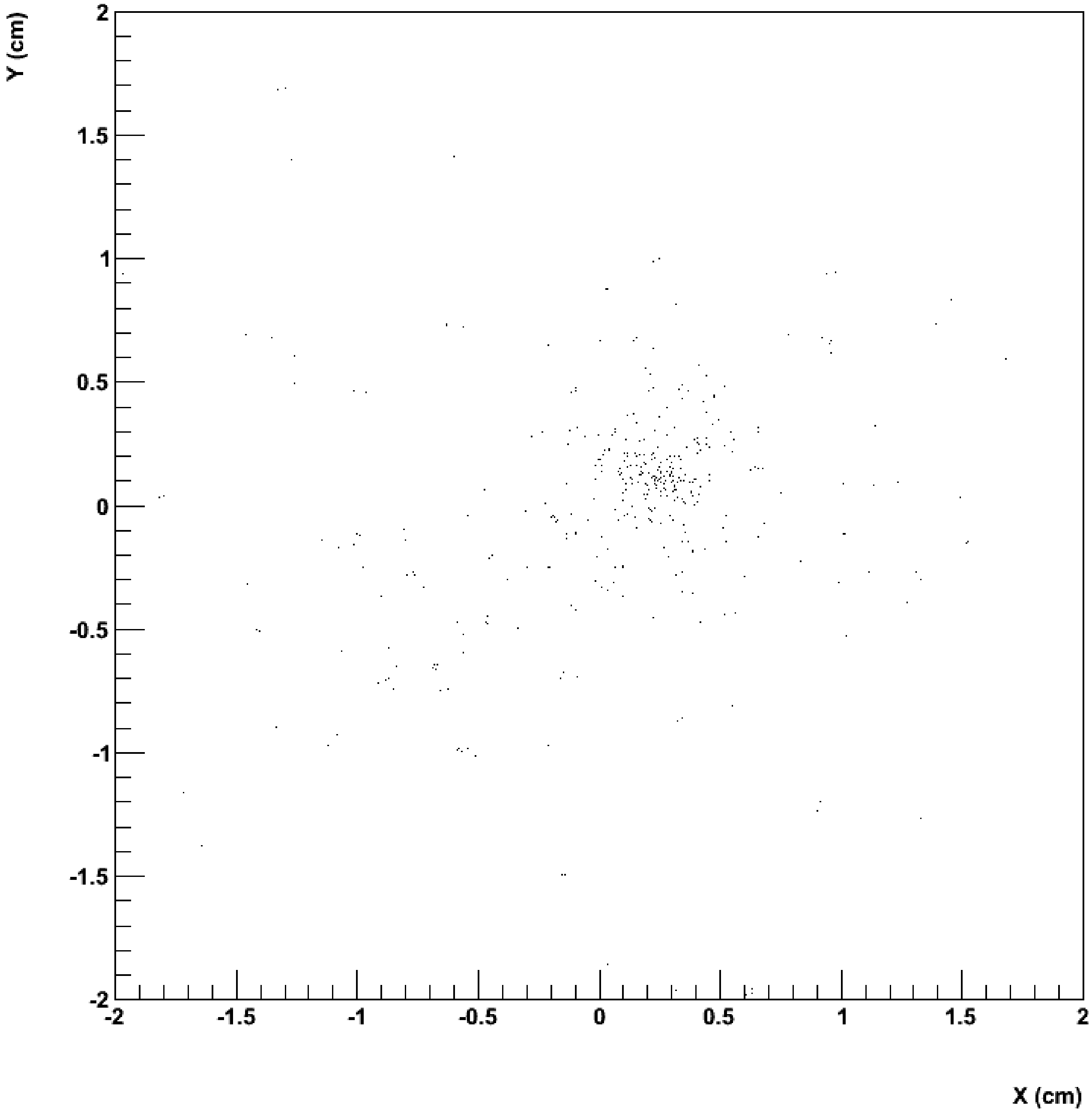

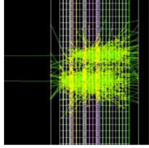

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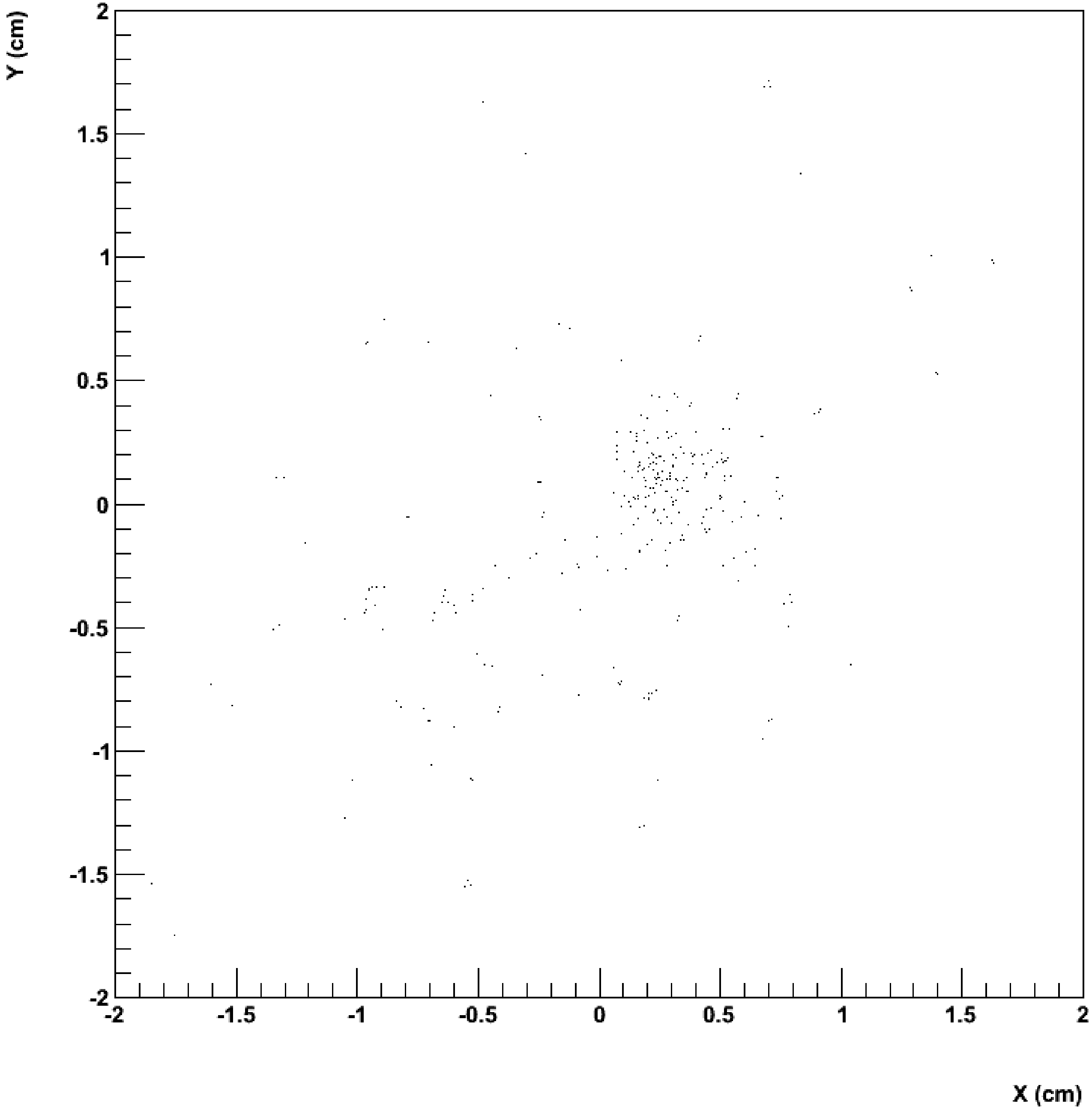

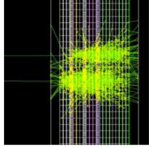

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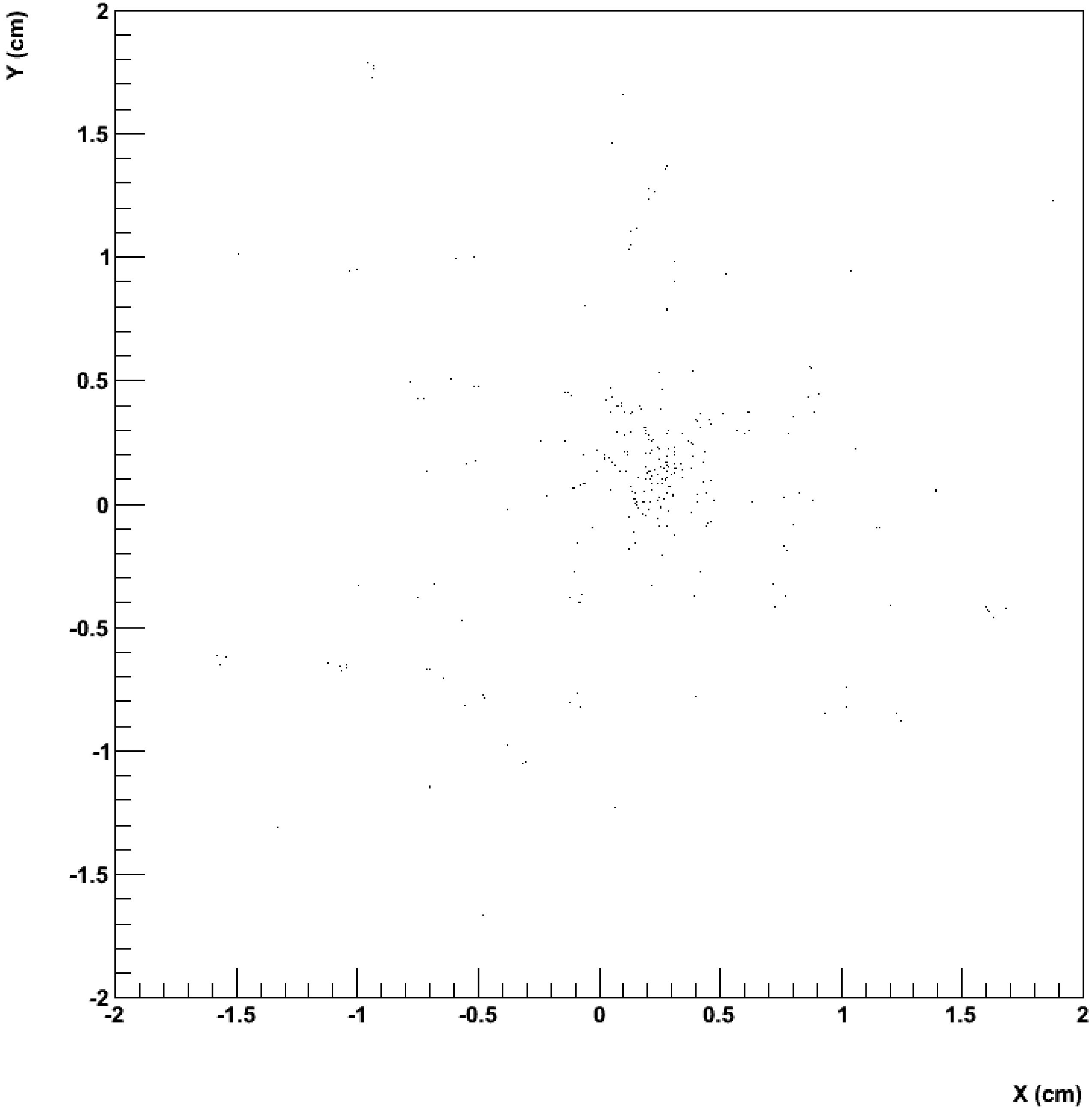

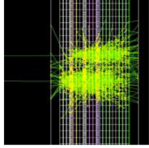

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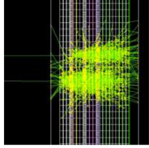

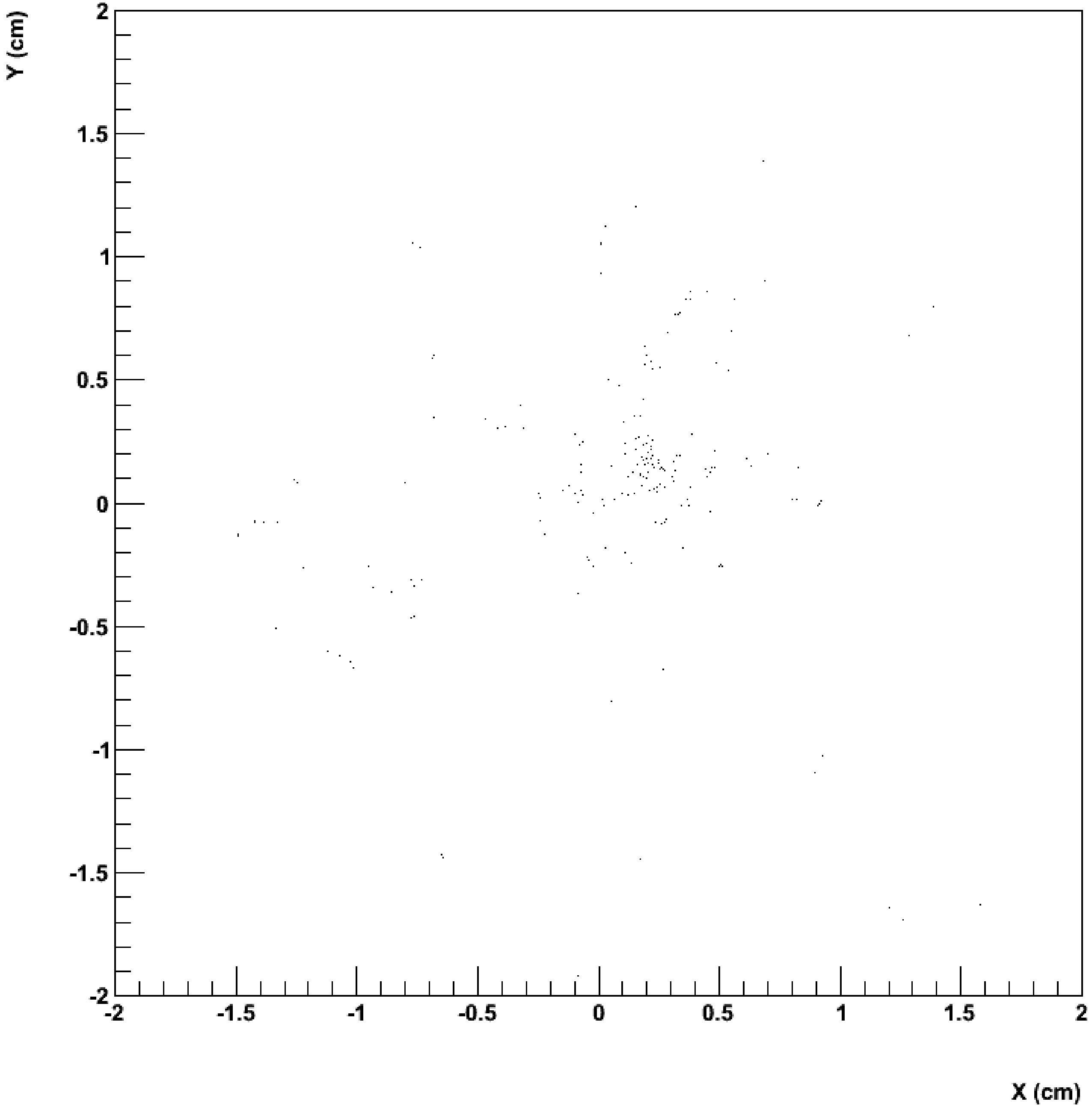

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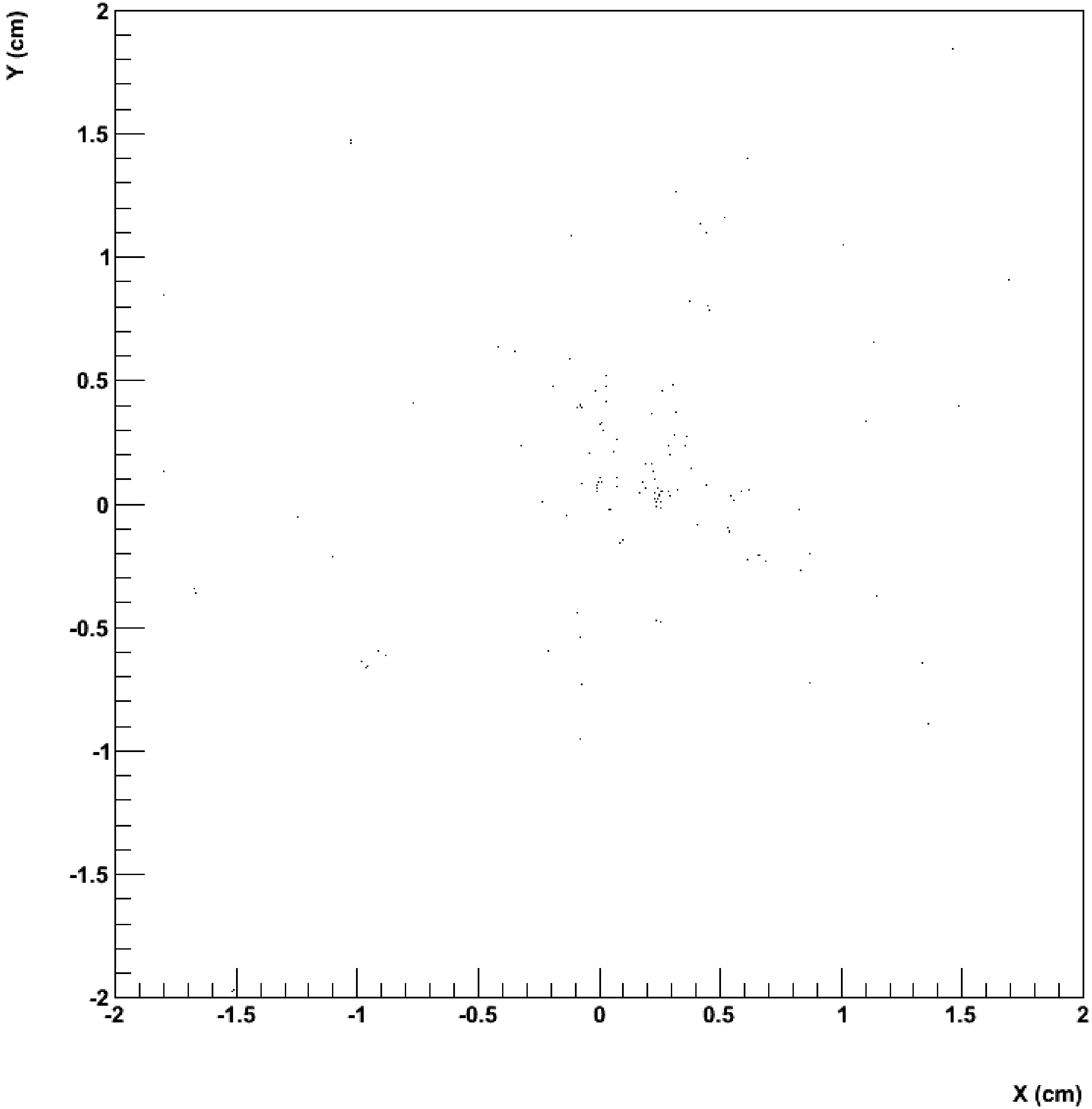

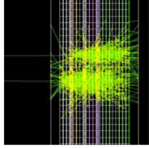

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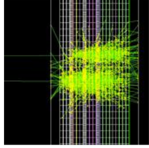

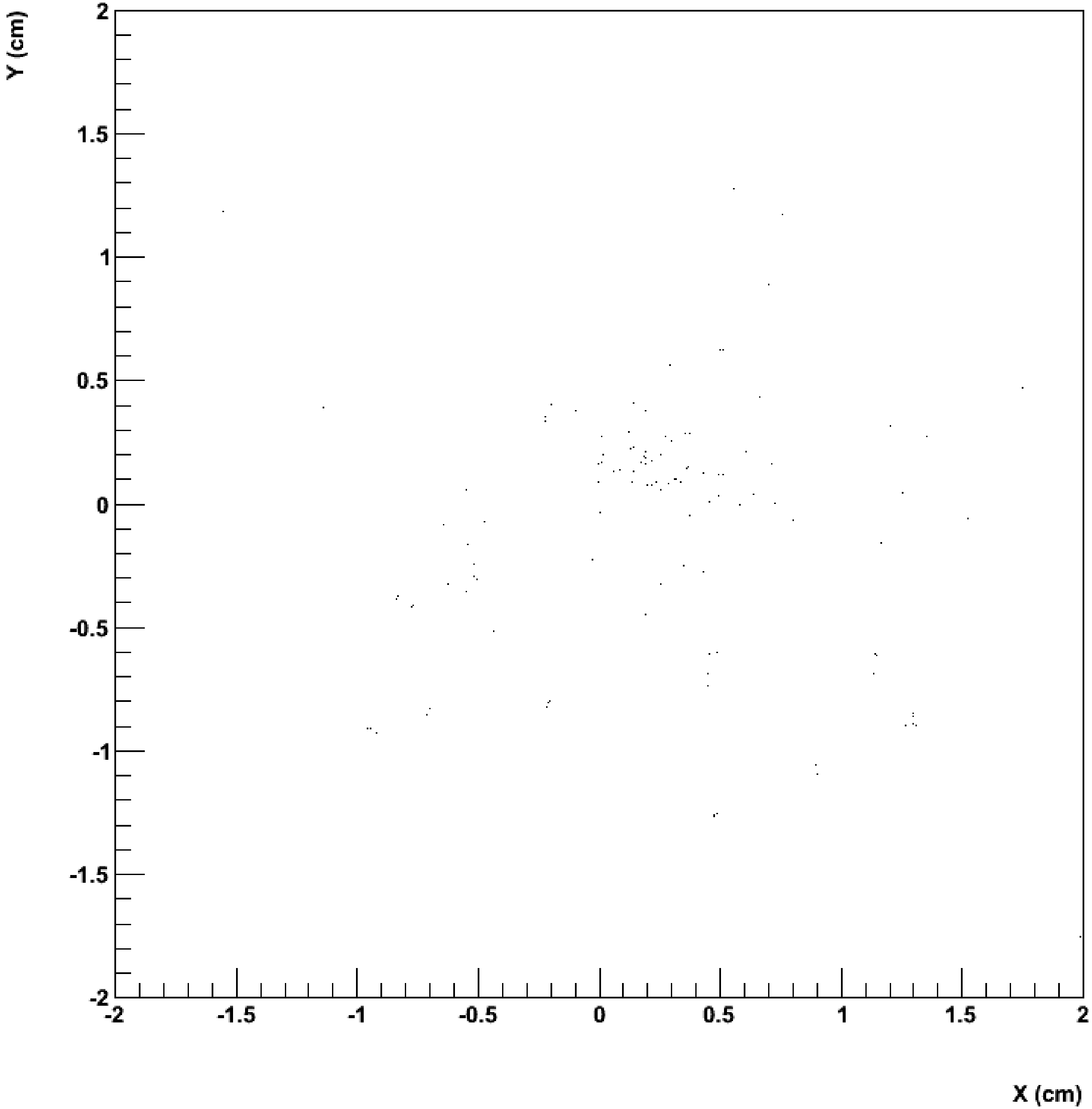

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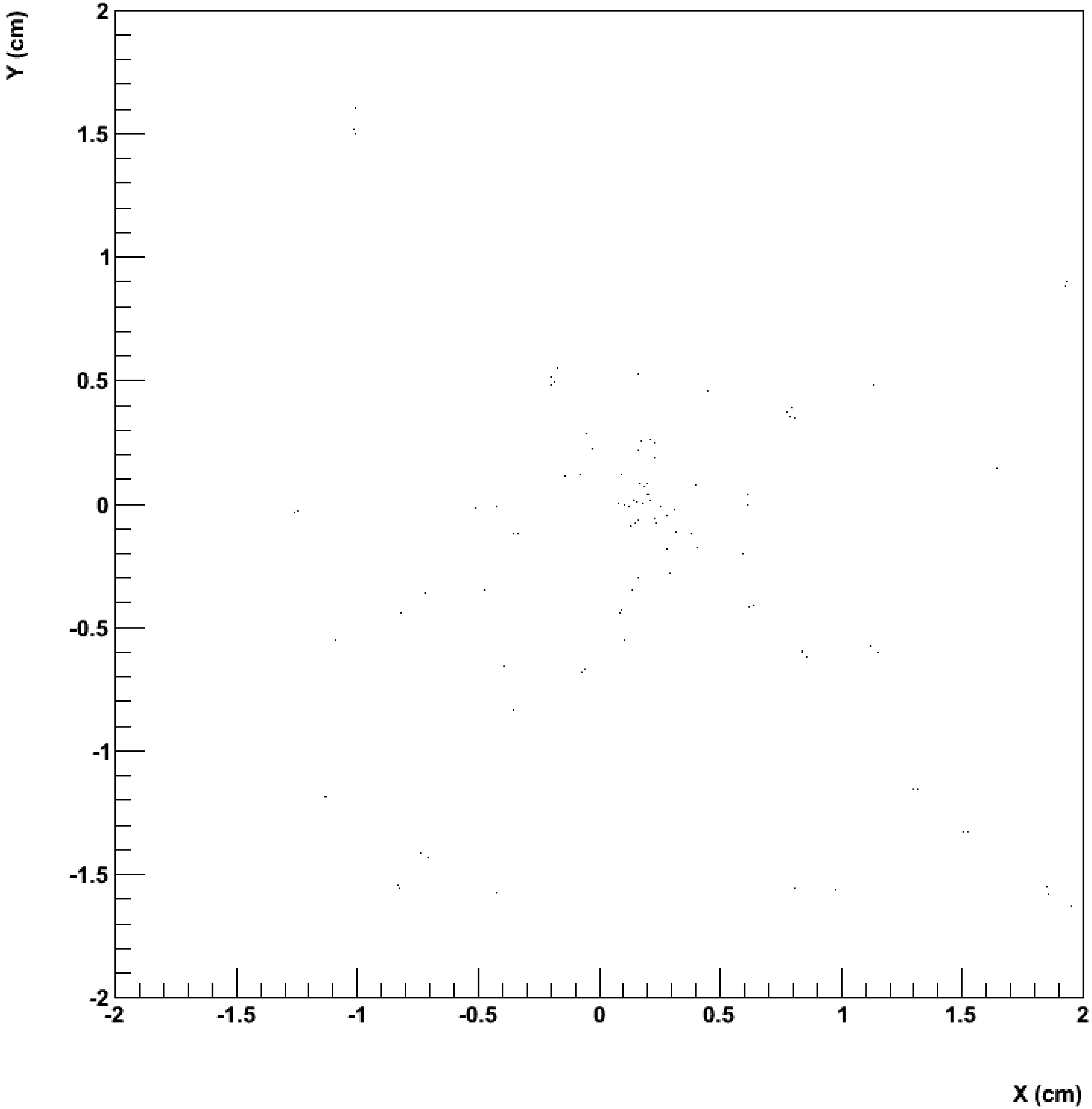

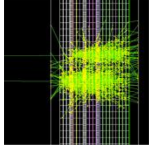

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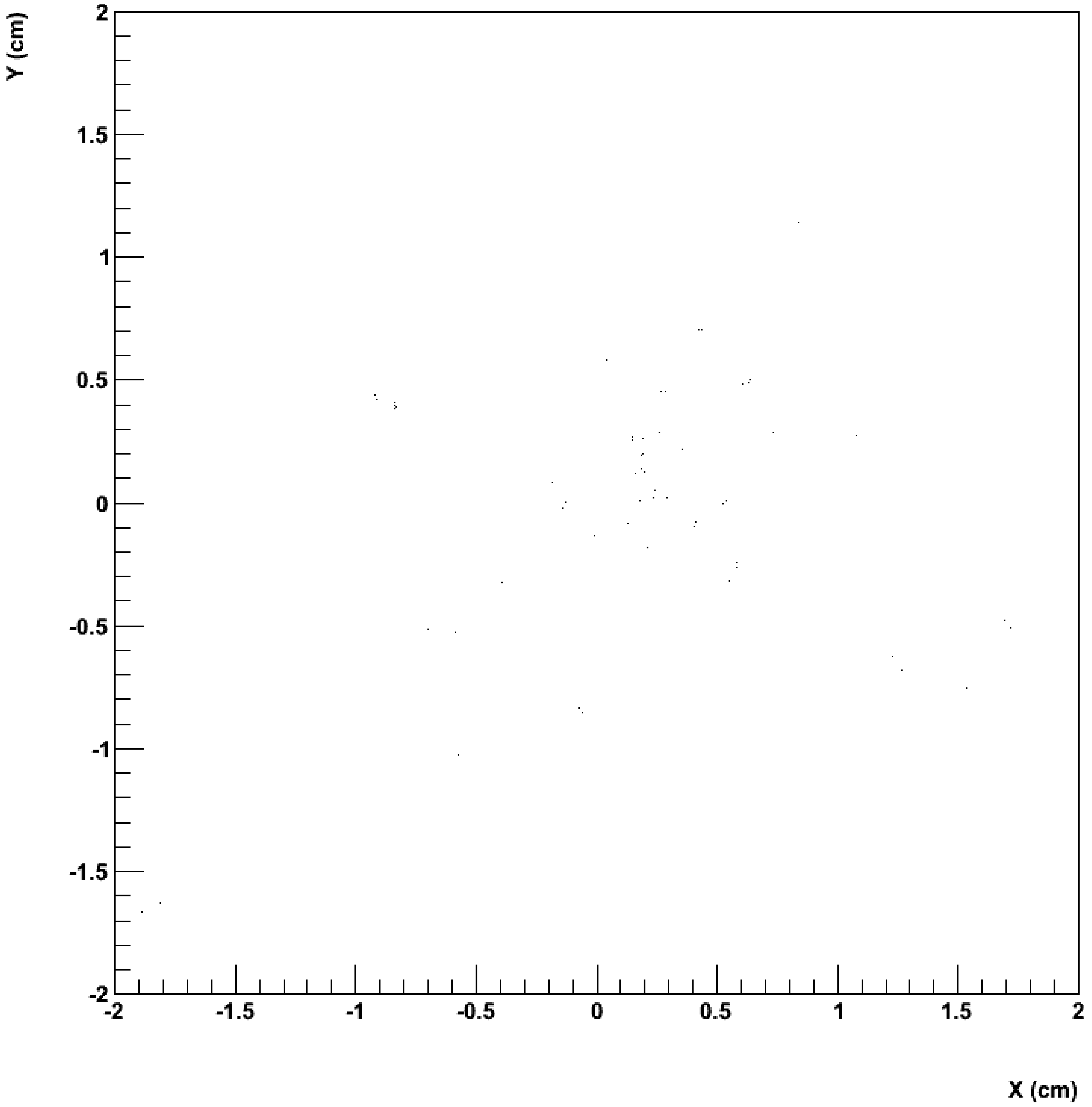

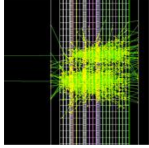

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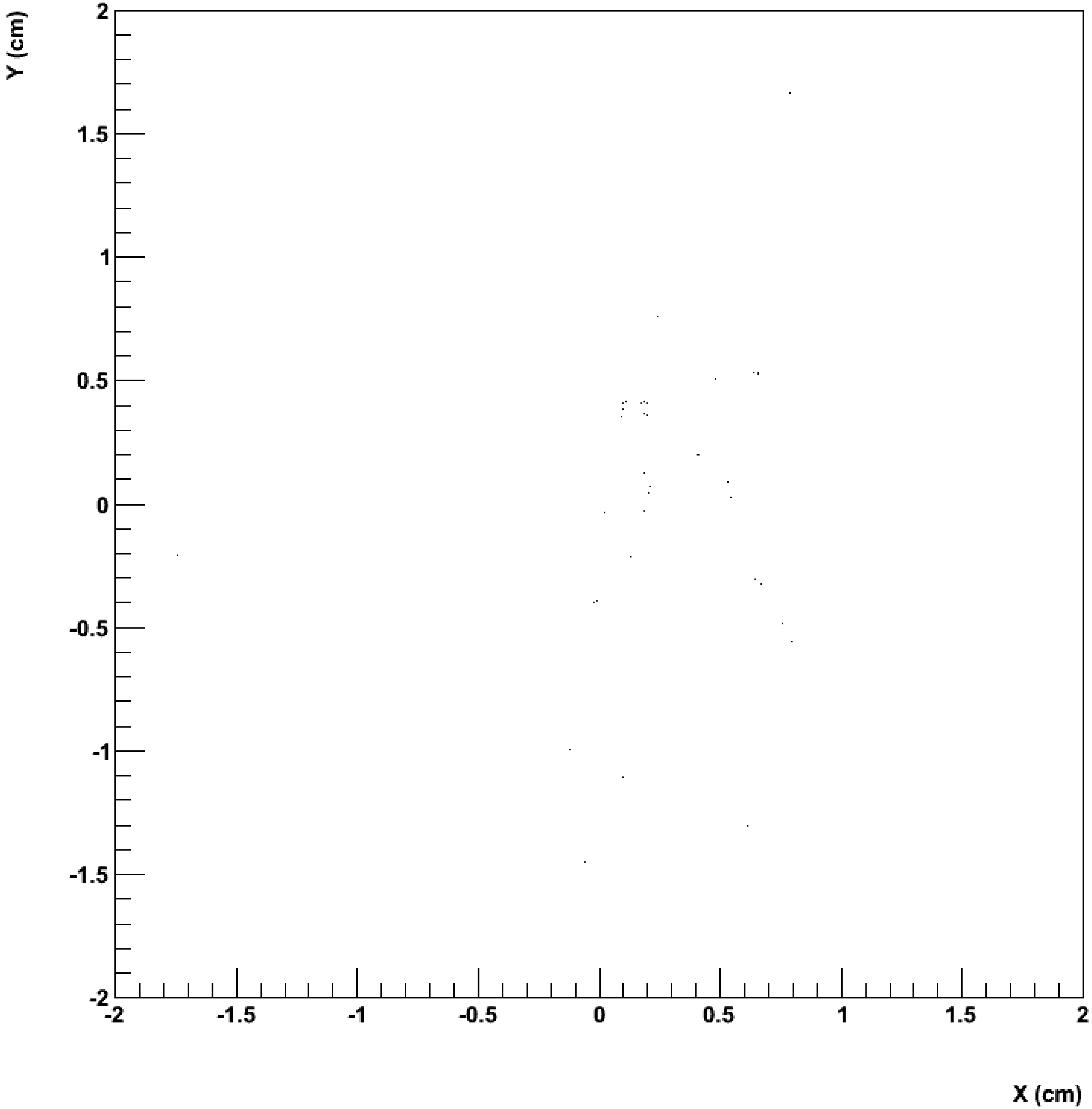

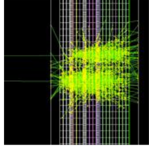

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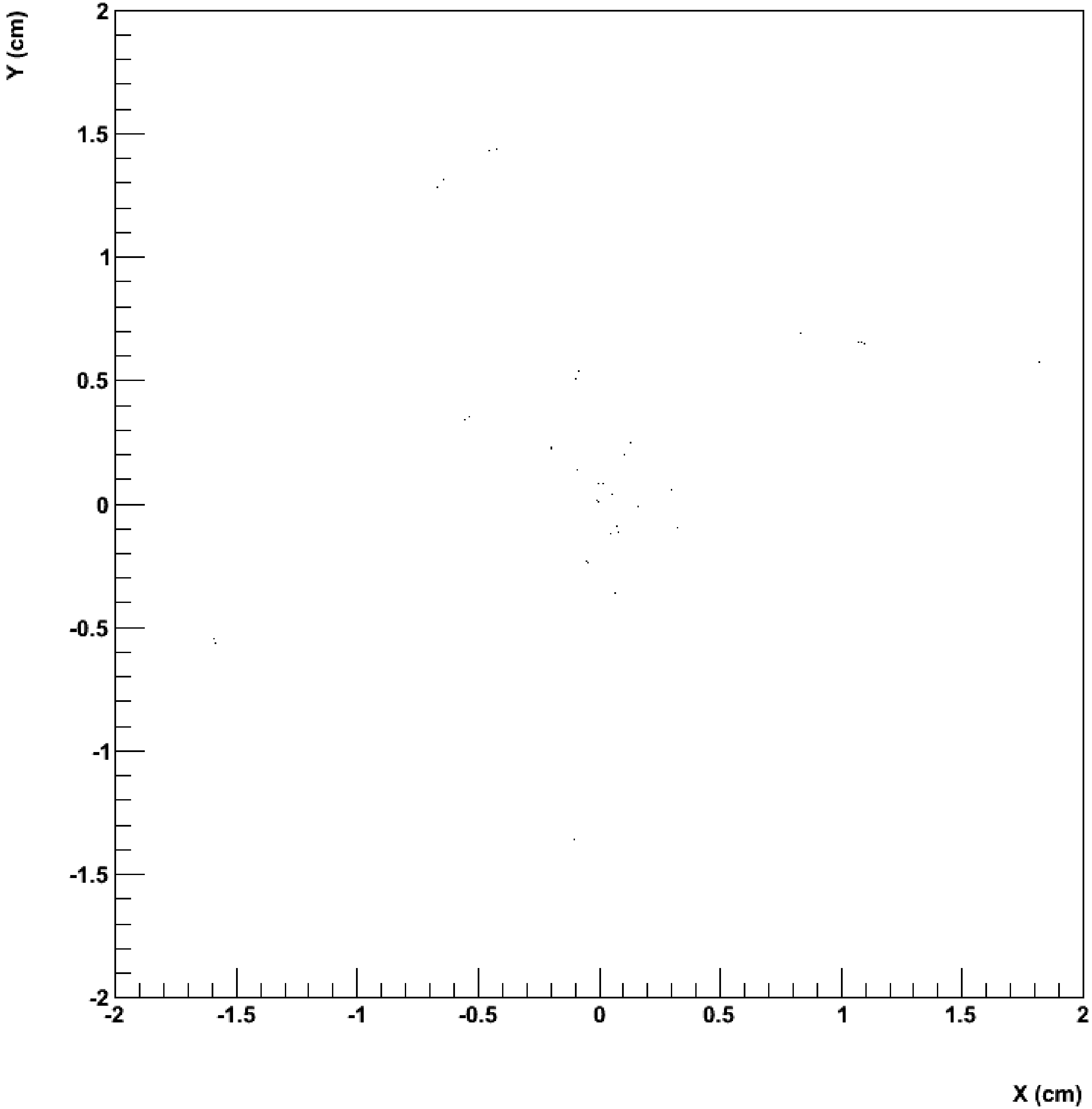

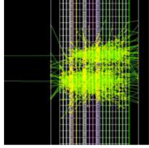

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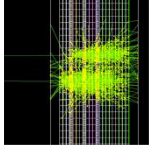
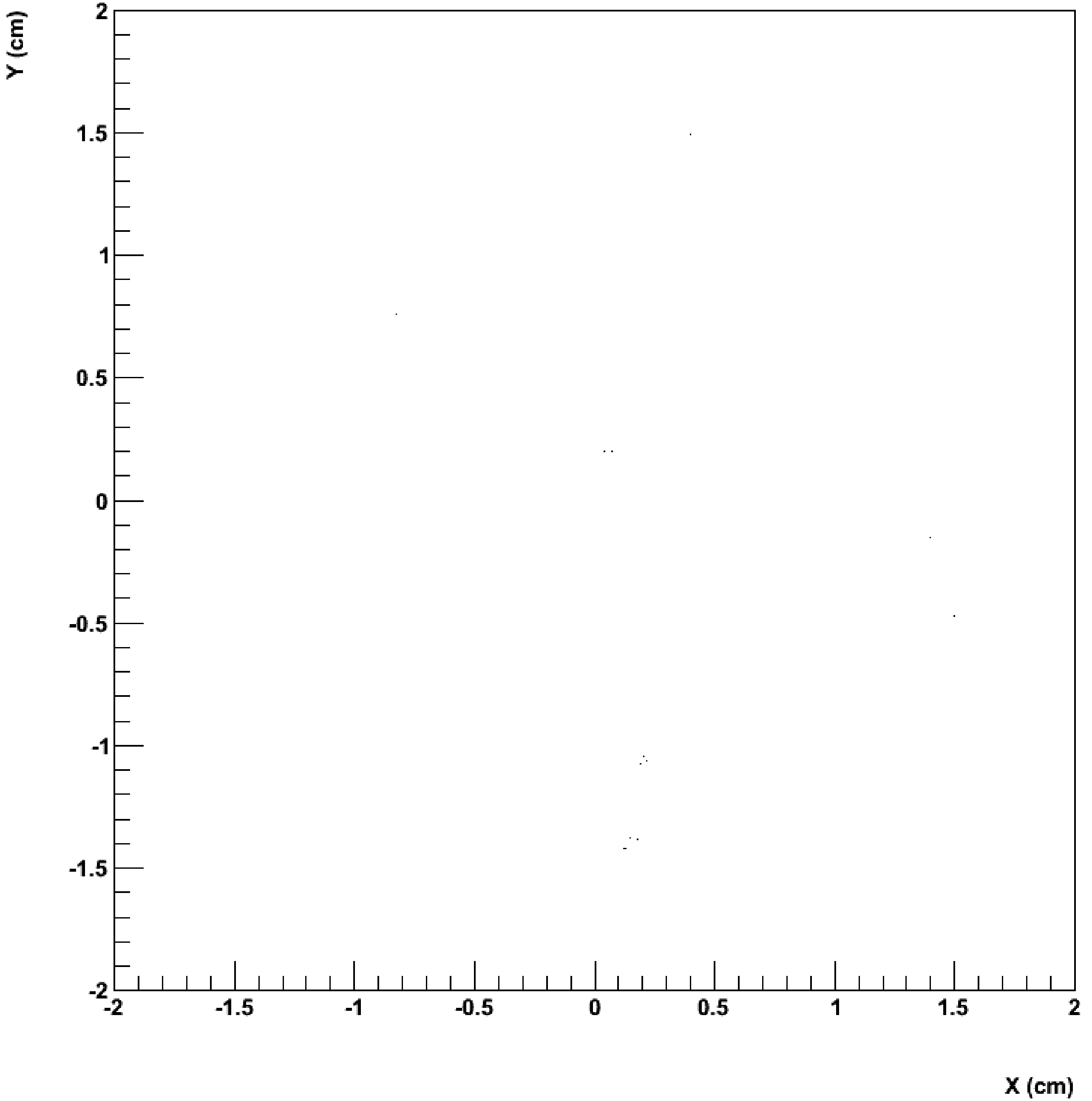
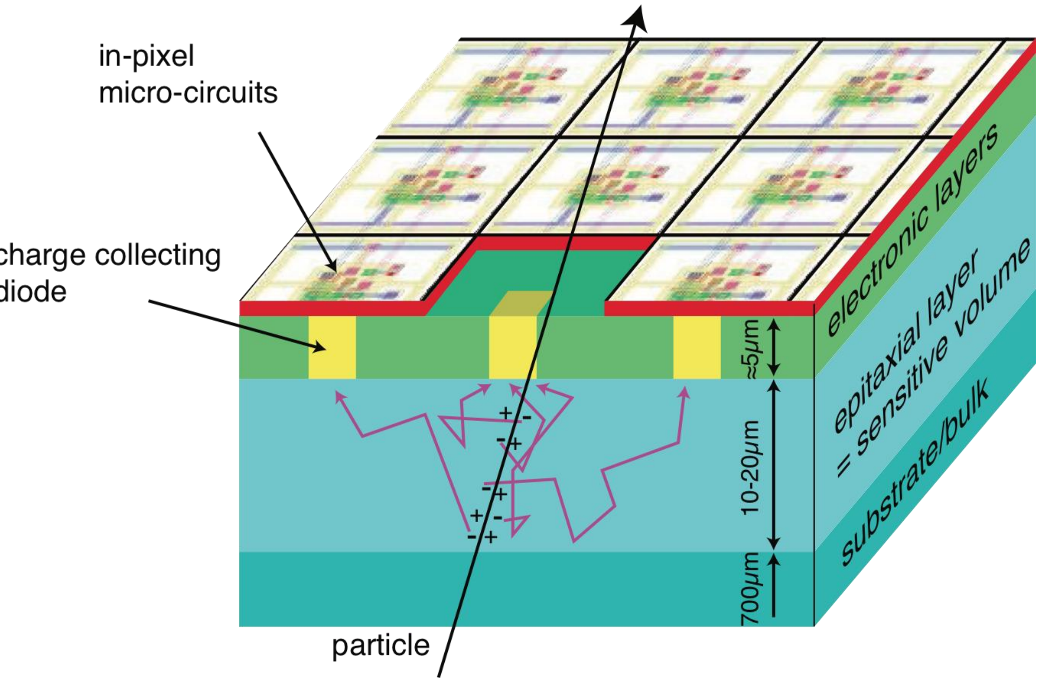
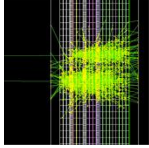




RD11

Monolithic Active Pixel Sensor



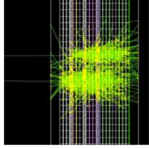


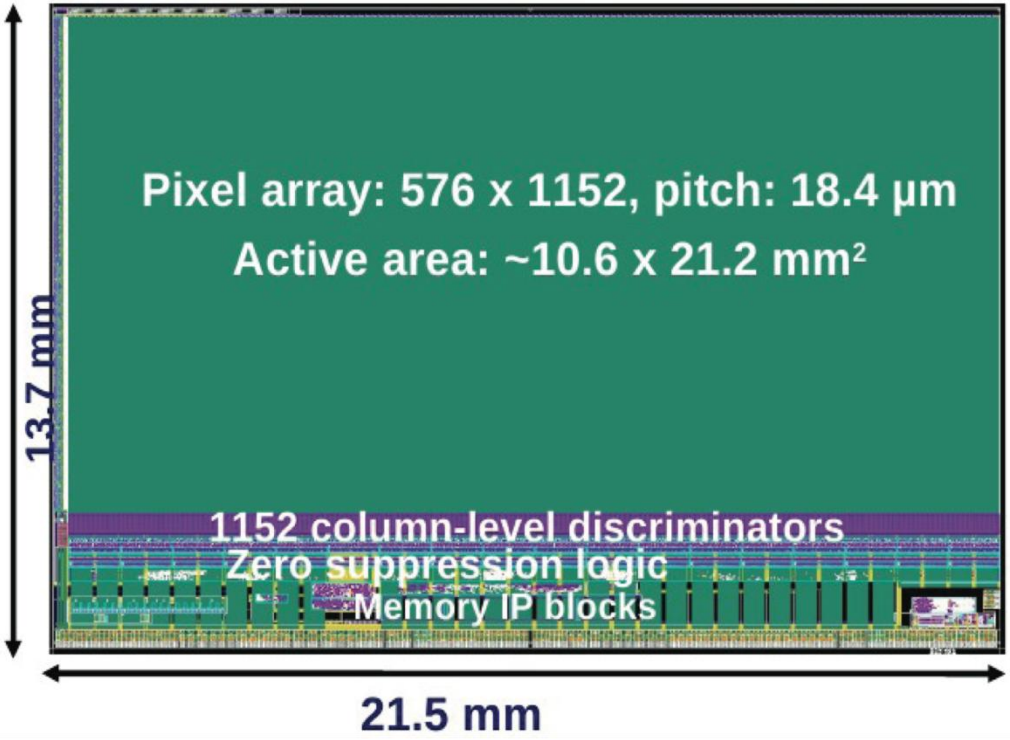
- ☺ solves the connection problem between sensor and front-end
- ☺ short input connections -> extremely low noise: tens of electrons

1 MIP = 80 e/h-pairs per micron

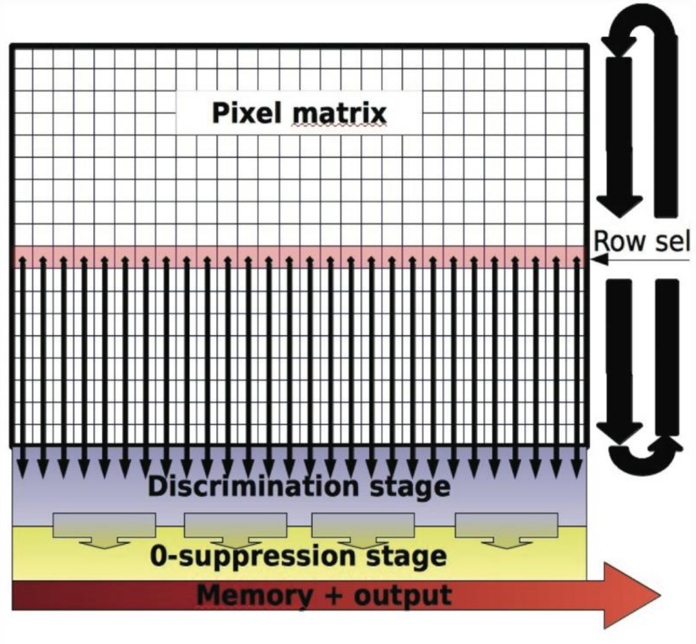
- ☹ high power density in sensor: dark current, cooling
- ☹ relatively slow -> not selftriggering
- ☹ charge collection
- ☹ radiation tolerance
- 😐 thin active layer
- ☺ intense development at several places, like RAL, IPHC, CERN

an implementation in 0.35 AMS: MIMOSA26





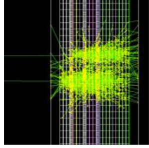
- “rolling shutter” readout
  - 115 μs per frame
  - 115 μs charge integration
- row-wise discrimination
- built-in zero suppression



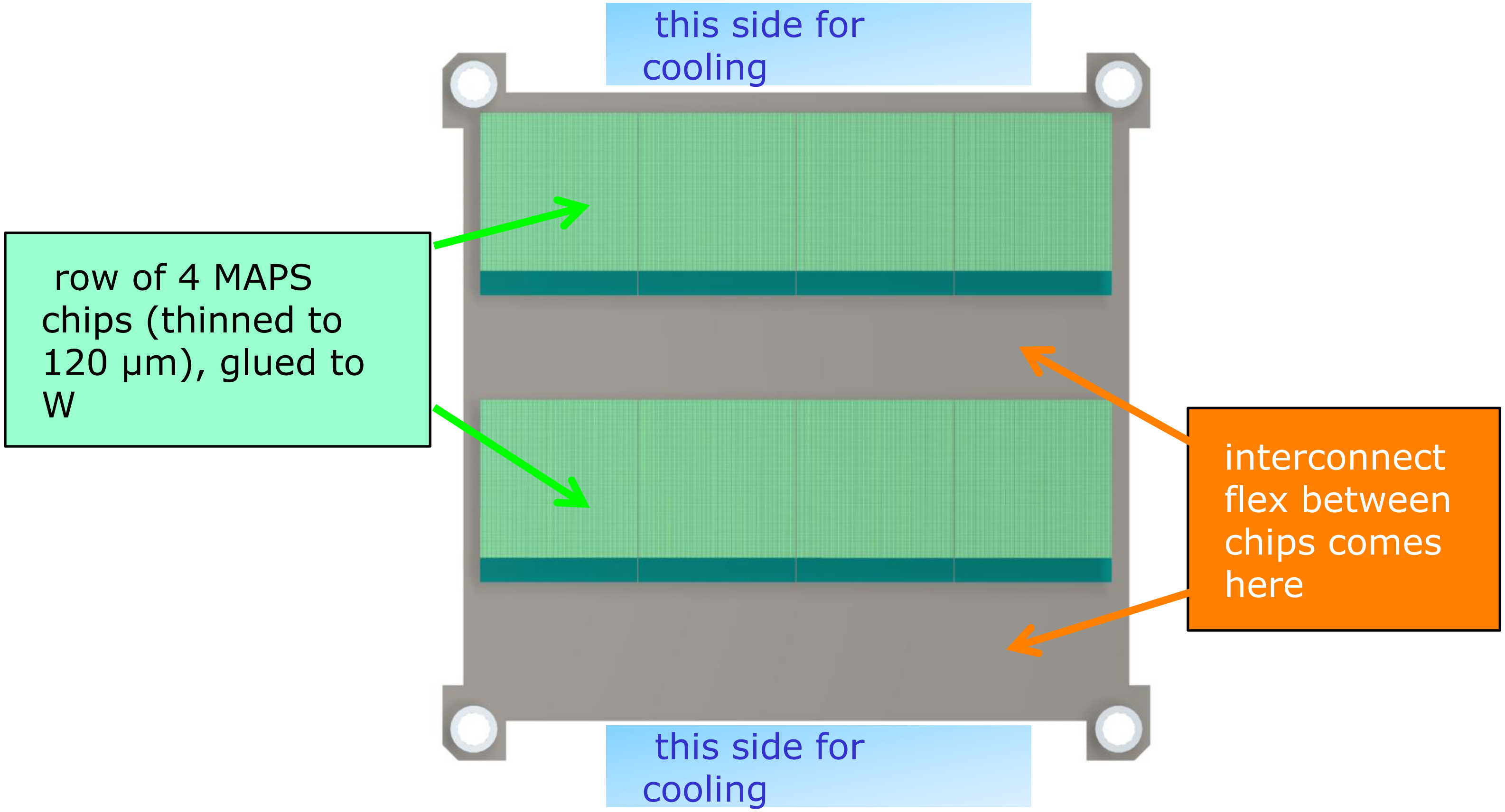
sketch of a tungsten + MAPS calorimeter

- digital areas of chips are dead -> need overlap
- ➢ each layer is composed of two rotated halflayers
- W is good heat conductor
  - glue chips directly on it
  - cool from the sides: 1 K/W

a design for one halflayer



Al+kapton flex can be bonded directly on chip



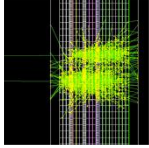
this side for cooling

row of 4 MAPS chips (thinned to 120 μm), glued to W

interconnect flex between chips comes here

this side for cooling

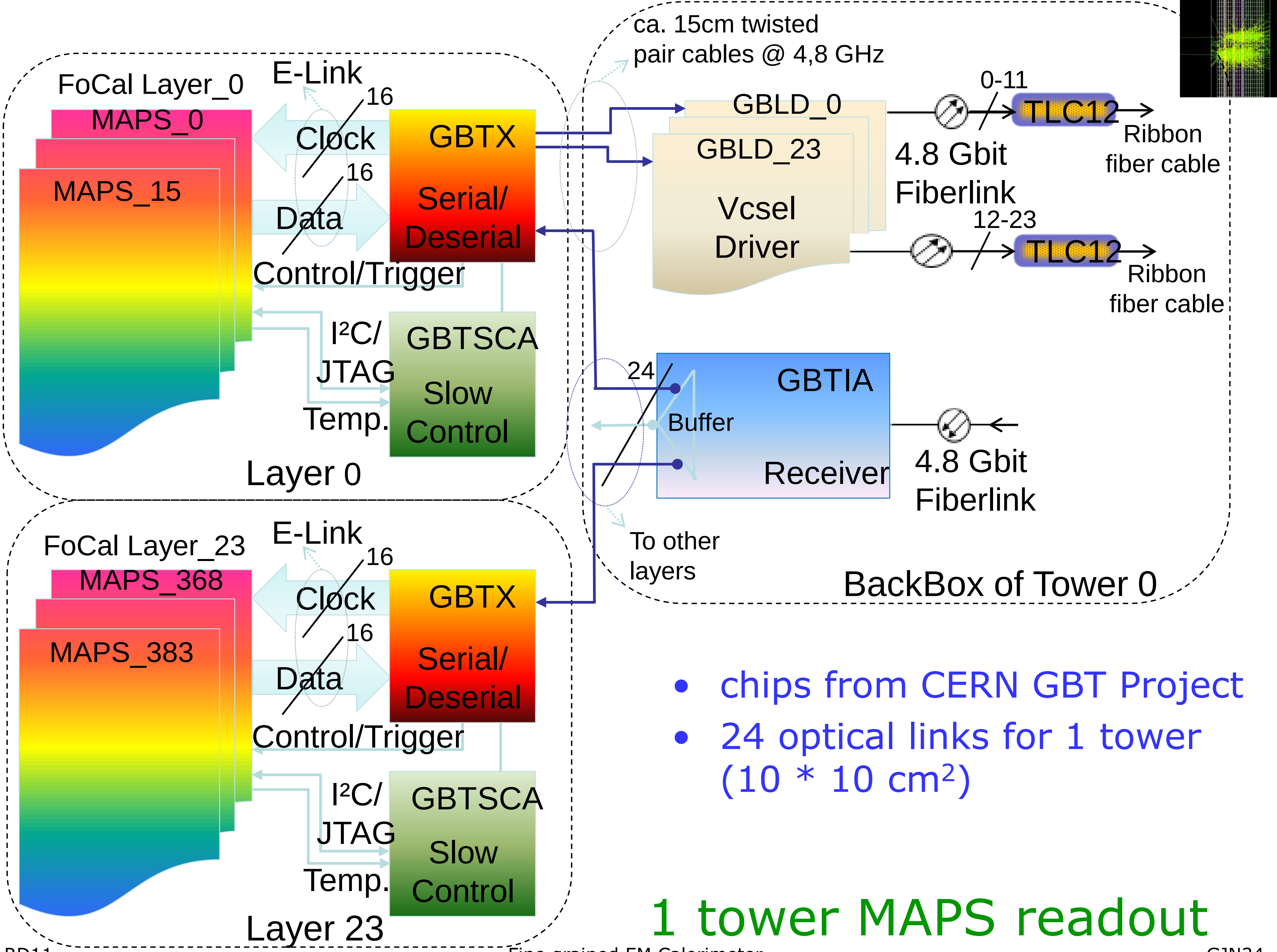
MAPS data volume



1. total silicon area 24 layers of 1 m^2 ~24 m^2 → 10^{10} pixels → 10 Gbit eventsize
2. rolling shutter provides full frame every 20 μs → 0.5 PB/s

- technical feasibility

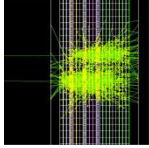
  2 kHz full read-out, see next slide



- chips from CERN GBT Project
- 24 optical links for 1 tower ($10 * 10\ \mathrm{cm}^2$)

1 tower MAPS readout

MAPS data volume, an estimate



1. total silicon area 24 layers of 1 m^2 ~24 m^2 → 10^{10} pixels → 10 Gbit eventsize
2. rolling shutter provides full frame every 20 μs → 0.5 PB/s
3. data reduction
   - *a.* select/compress locally, in layer or chips
     - zero suppress depends on occupancy, high for chips at core of the shower
   - *b.* selection at end of tower (16 chips per layer)
     - transport only frames with trigger
   - *c.* outside

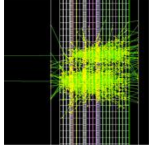
       high speed cabling, fibers

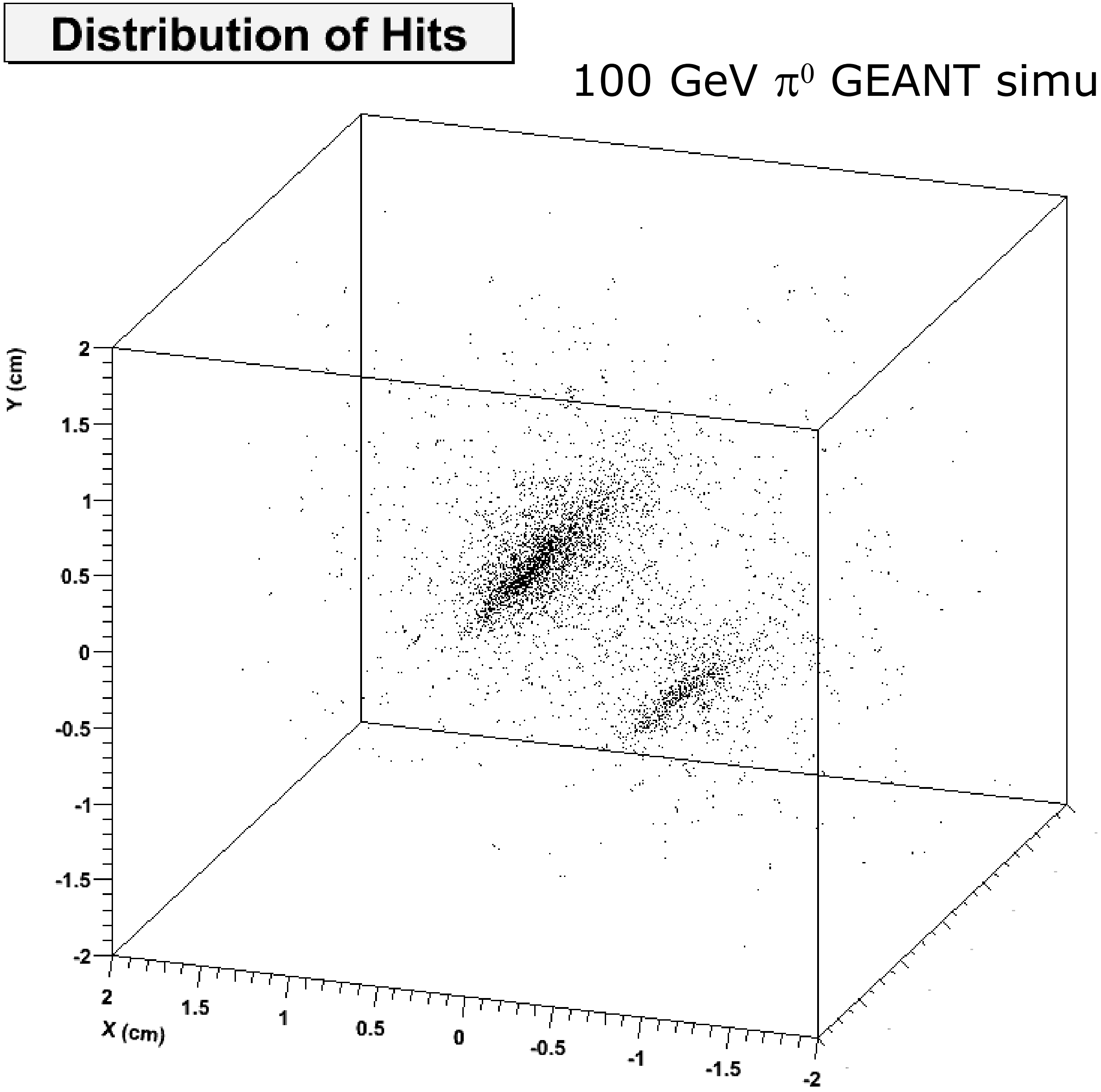
       combine frames

locally, bandwidth need remains high because of high particle density in shower

➢ different from tracker application

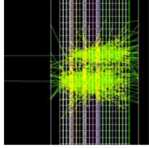
suppose we can measure this, what can we do with it?





100 GeV π^0 GEANT simulation

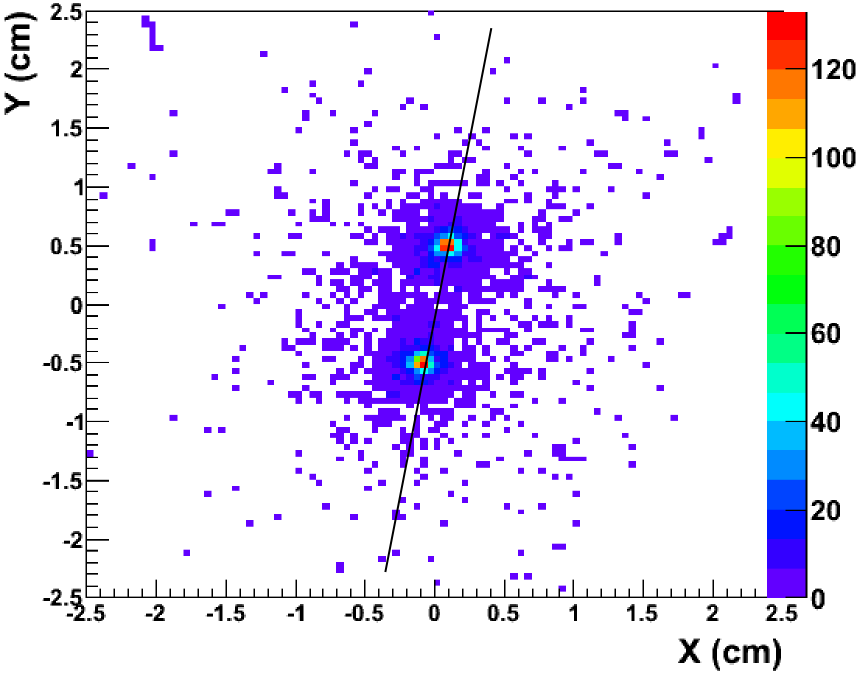
geometrical resolution



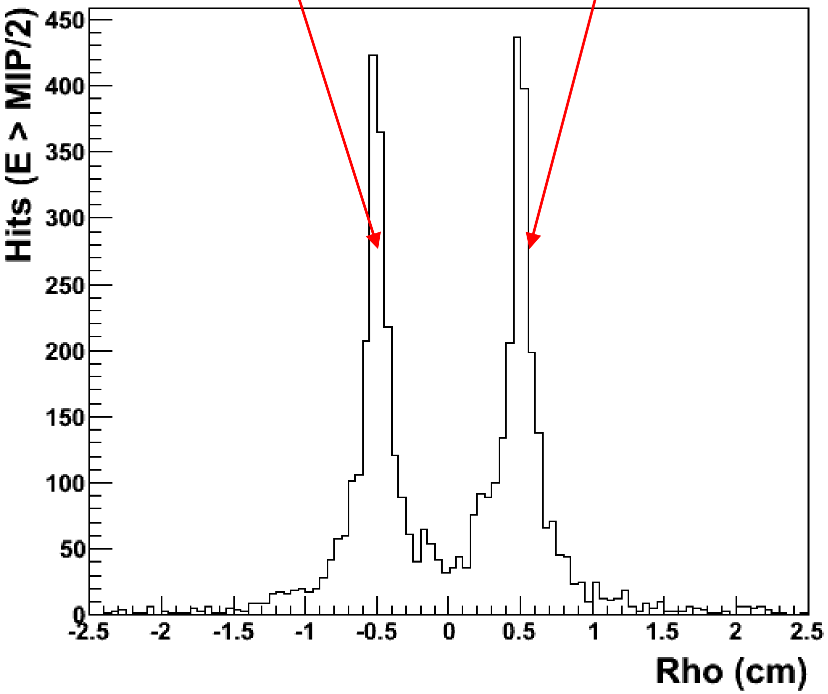
sum all layers

fit line in X-Y plane

project data onto fitted line

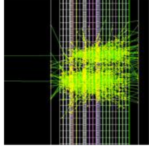


how well can we trust these widths from simulation?



- easy to find peakposition to submillimetre, what about energy?

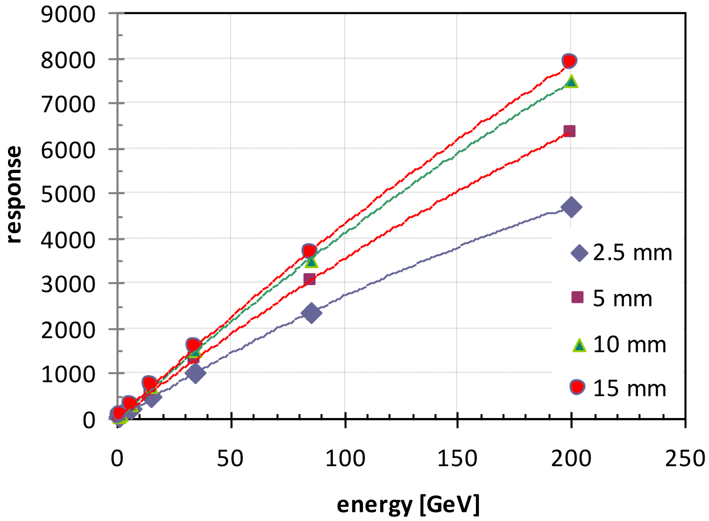
energy measurement "vide-pomme"



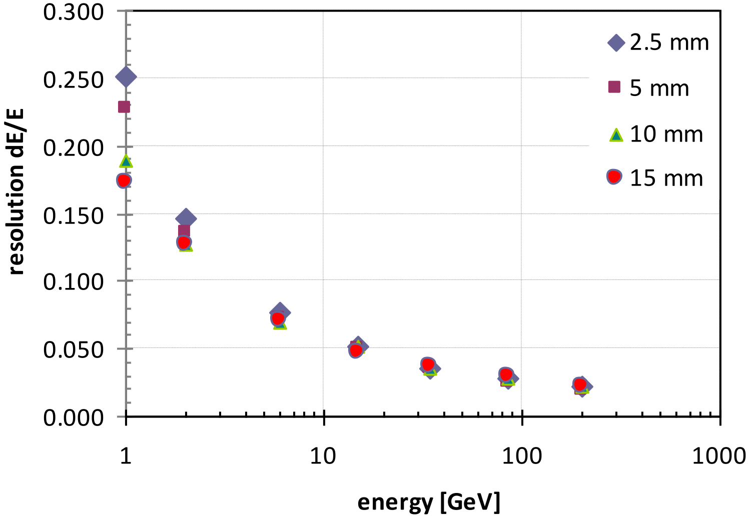
- cut out cylinder along shower axis
- count hit pixels for *energy measurement*

simulations for single photons with different cylinder radii

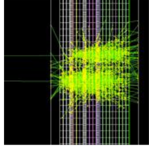
signal



energy resolution



“real” prototype

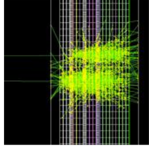


- uncertainties in simulation
  - small angles
  - low energy particles
  - thin sensor, charge collection (not simulated here)

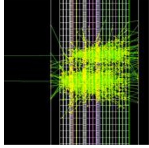
➢ build prototype and test with beam

  - need sensor size compatible with R_M
  - enough layers to study longitudinal shower development
  - based on available MAPS sensors
    - most are too small, like TPAC, many MIMOSA
    - all have pixel < 50 μm
    - ➢ take PHASE1 from IPHC

Beam test prototype objectives

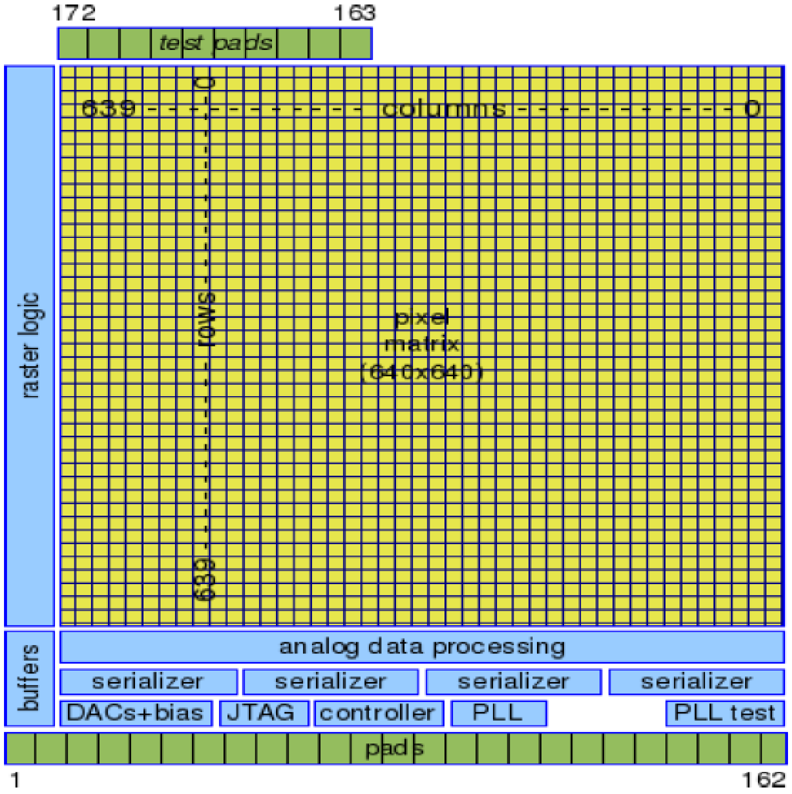


- YES:
  - proof-of-principle
    - resolution
    - Moliere radius
  - technology demonstrator
    - manage read-out at GB/s
    - cooling
    - integration
    - overlap, needed because of dead zones
  - collect data for study of
    - data volume/flow, data reduction
    - pixel size
- NO:
  - final chip (too slow)
  - rad hard
- may help in
  - detector simulation



prototype features

- 24 layers 3 to 4 mm W
- PHASE1/MIMOSA23
  - 640 * 640 pixels, 30 μm pitch
  - high resistivity (400 Ωcm) epilayer, 15 and 20 μm
  - 1 MHz rolling shutter → 640 μs integration time
  - 160 MHz read-out clock
  - no data reduction on board
  - radiation tolerance < 1 Mrad
- thinned to 120 μm
  - total sensor layer thickness ~1 mm
  - estimated R_M < 15 mm
- 4 PHASE1 per layer:
  - 4 * 4 cm^2 active area
  - overlap dead areas
- full read-out



some details

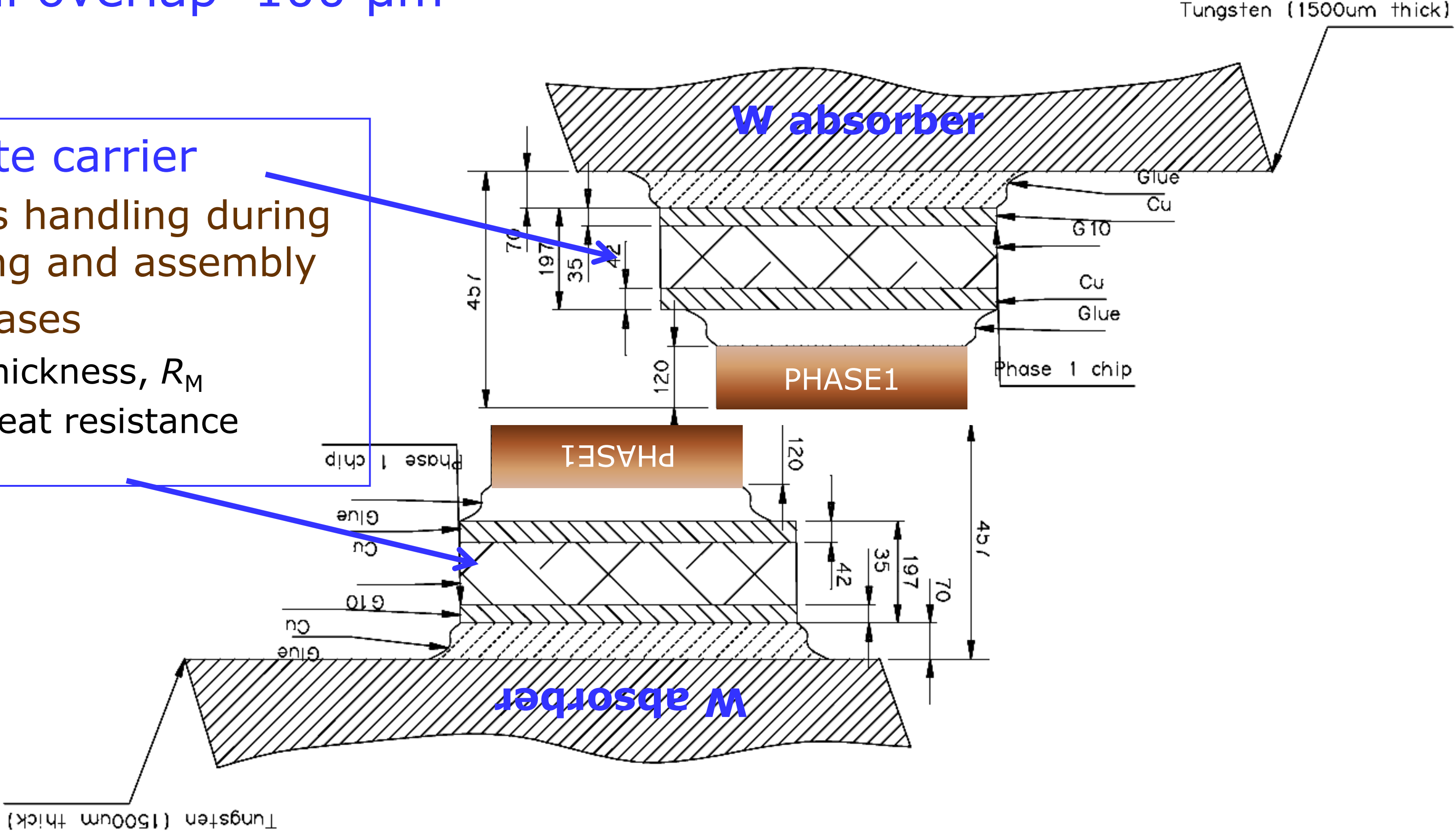
idea of direct gluing to W discarded:

- what to do with broken chips?
- need thin flex development
- use intermediate carrier (pcb) instead

keep small overlap 100 µm

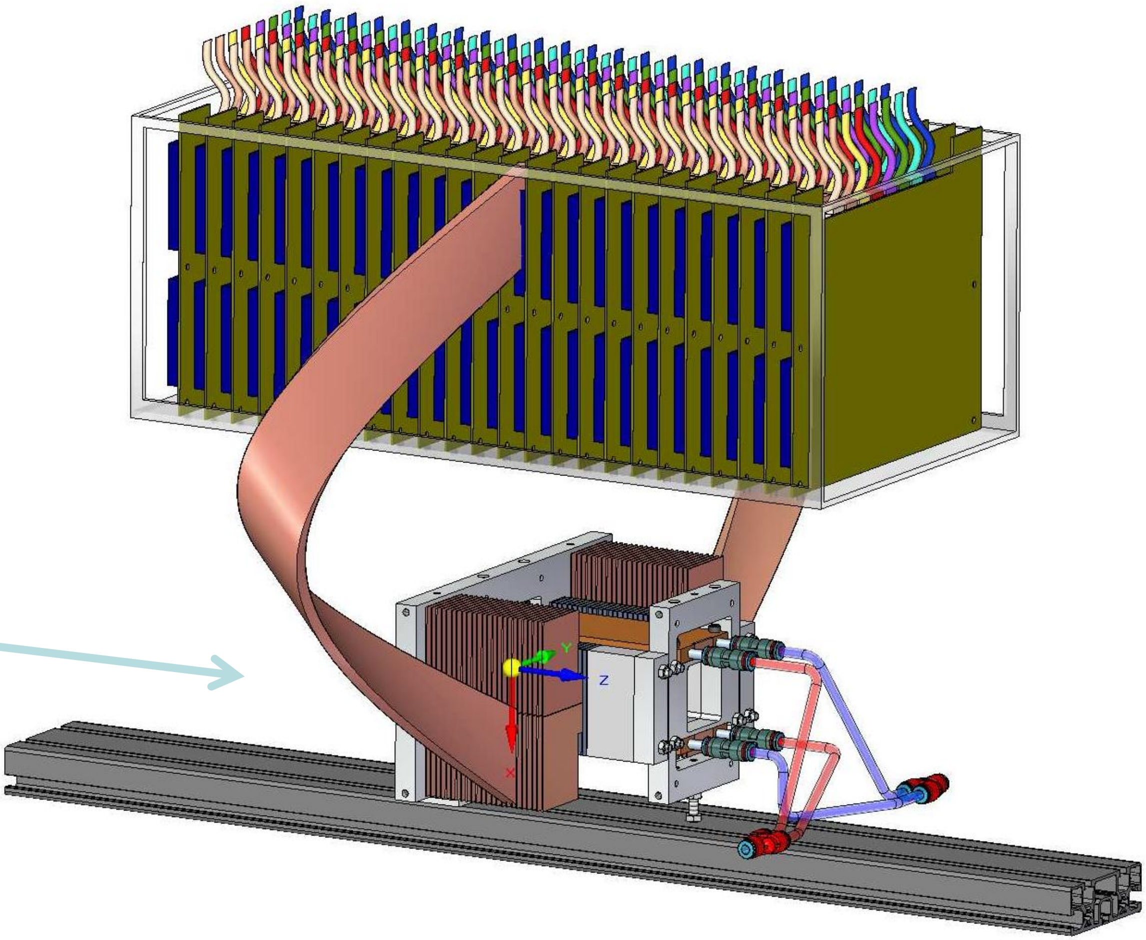
intermediate carrier

- eases handling during testing and assembly
- increases
  - thickness, R_M
  - heat resistance



beam test prototype

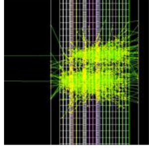
- 4 PHASE1 per layer: 24 * 4 cables from tower to read-out
- total 61 Gb/s
- several FPGA’s to manage this:
  - keep only 2 frames per trigger
  - big local buffer storage
  - small duty factor of PS/SPS

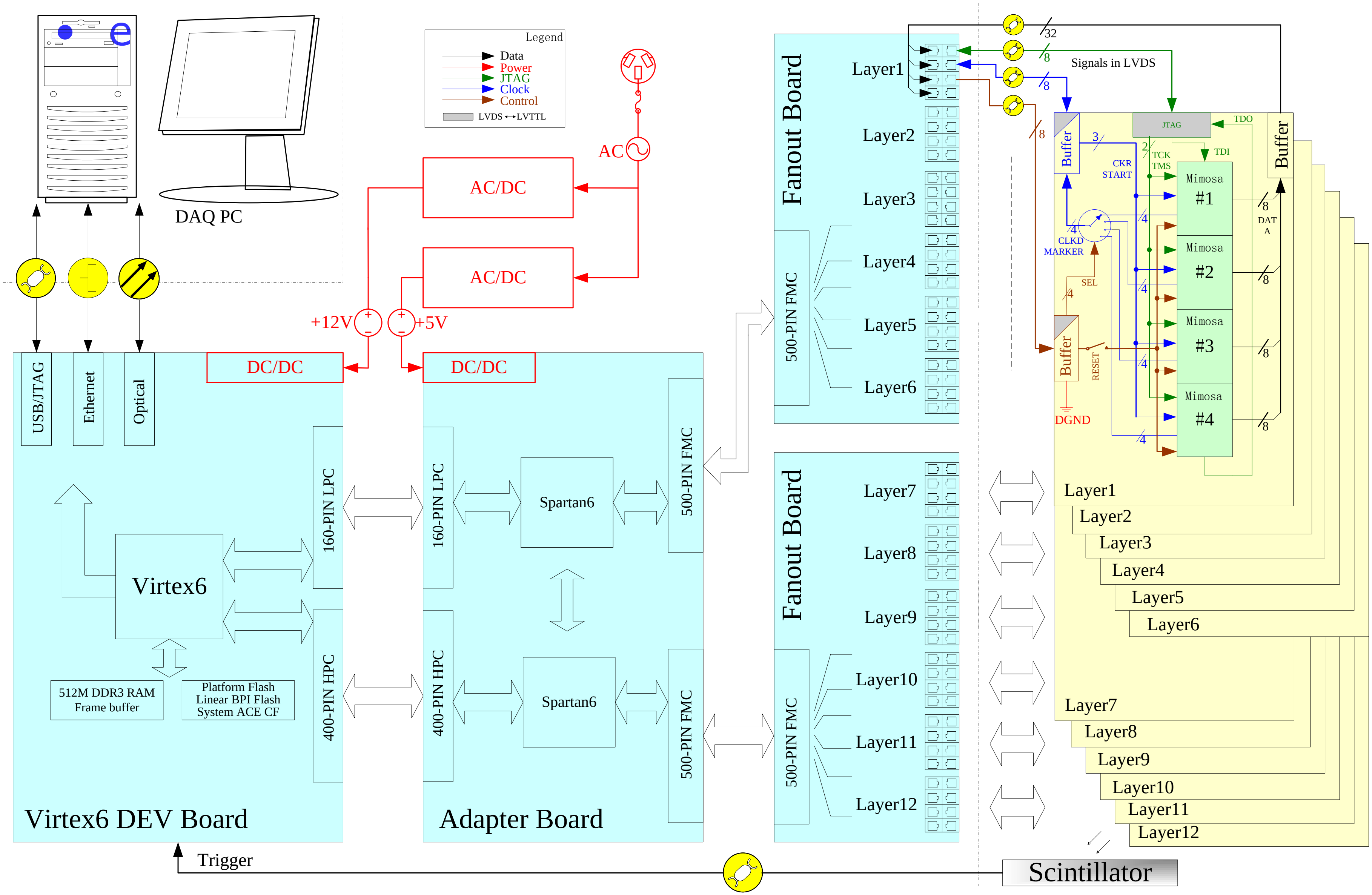


electron beam

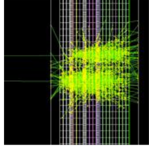
- CERN PS Nov 2011
- CERN SPS 2012

read-out electronics (one half)





summary, outlook

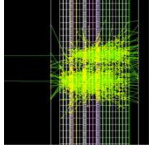


EM calorimeter with fine sampling and pixel counting is within reach

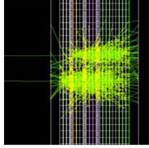
➢ would open new possibilities for particle identification

- uncertainties in simulations
  - shower development on this scale
  - importance of low-energy particles
  - charge collection
- prototype under construction (Utrecht/Nikhef, Bergen)
  - extremely fine pitch
  - full data read-out
  - very small Moliere radius

- an option for future forward calorimeter in ALICE



digital calorimetry



Richard Wigmans at EDIT2011

"was tried and abandoned in 1983, for good reasons: particle density in the core of EM showers is very high"

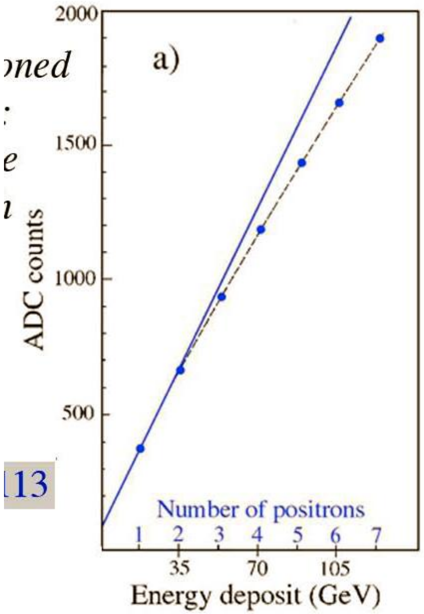
- non-linearity

Paul Dauncey at ICHEP 2010

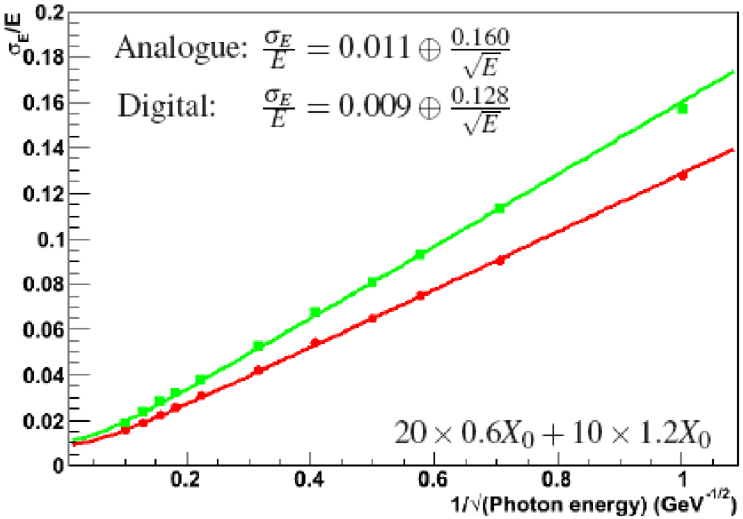
"improved resolution"

- beware: GEANT not tested at ~50 μm scale

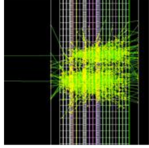
M. Atac et al. NIM 205 (1983) 113



simulation for CALICE ECAL

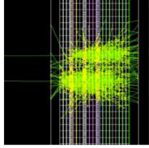


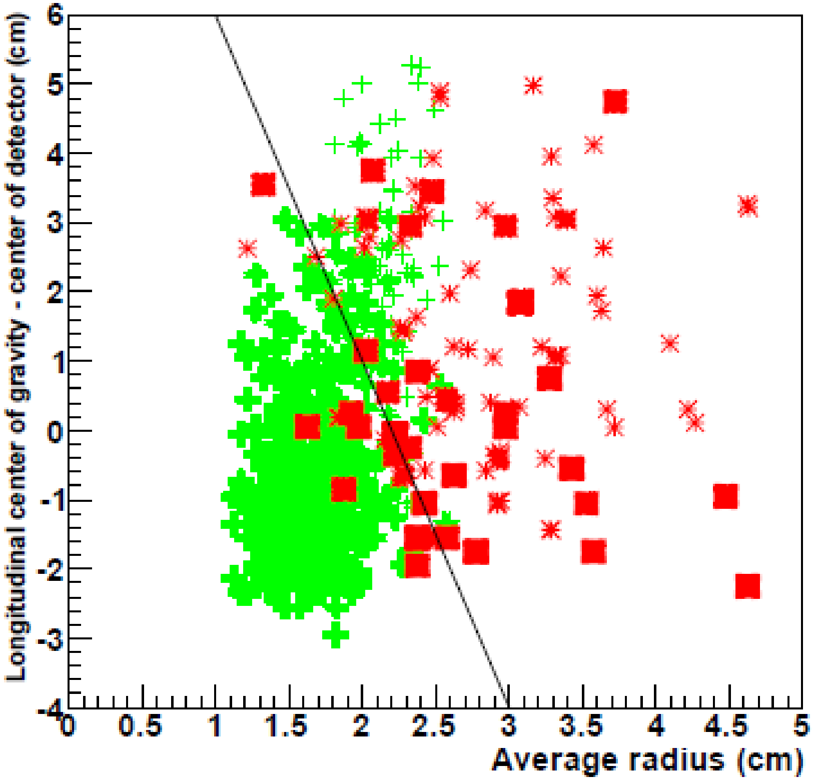
issues



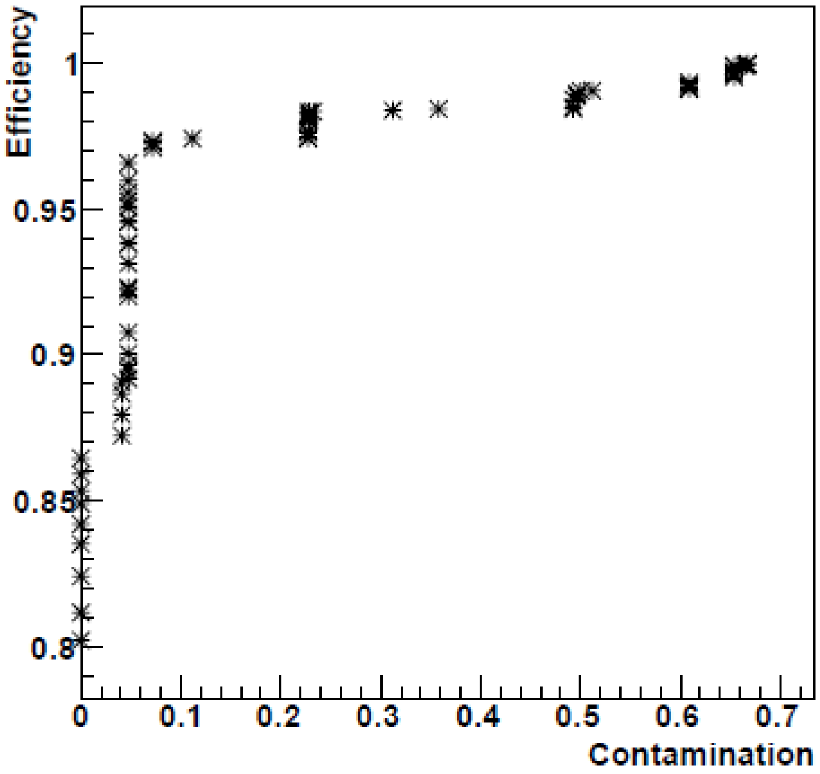
- pixel size:
  - current designs ≈ 20 μm
  - 50 .. 100 μm sufficient?
    - charge collection?
- trigger:
  - too slow for self triggering
  - need separate fast detector
    - ☹ fast Si or scintillator at around shower maximum
- power consumption:
  - currently ≈100 mW/cm^2 sensor
    - more functions ↑
    - newer technology ↓
- integration time:
  - pixel charge is integrated until next read-out
  - maximise rollingshutter speed
    - technology limit ~0.2 μs/row
    - shorter columns

Using shower shapes to discriminate γ and π^-

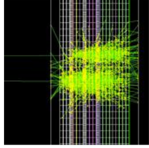




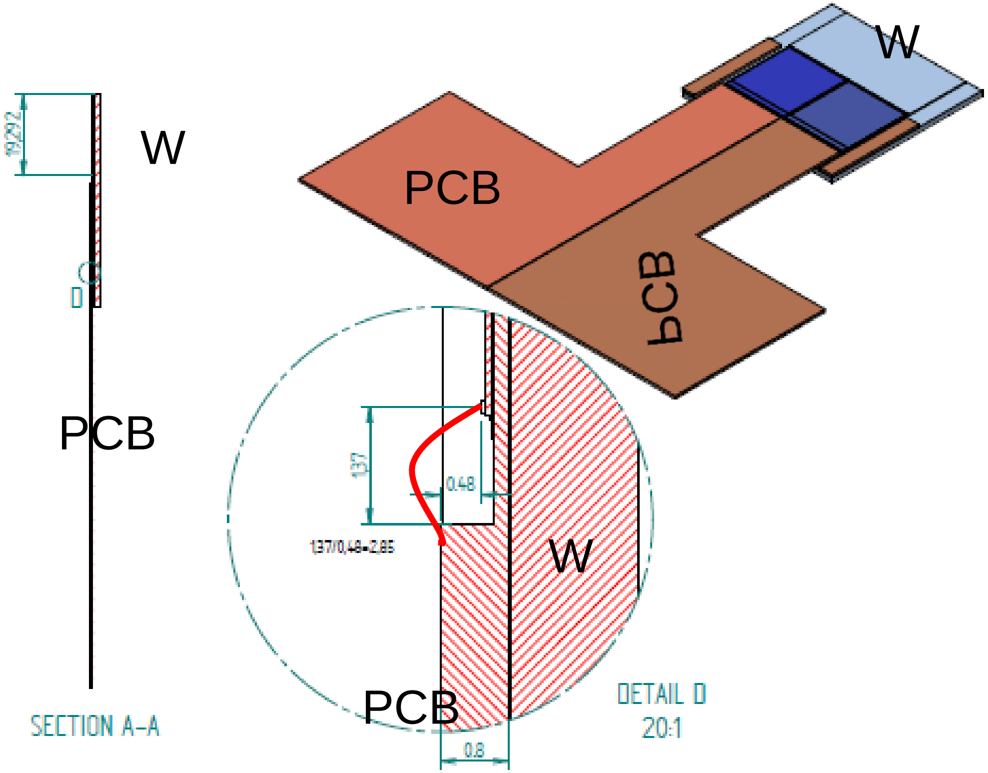
longitudinal and transverse shower shapes for γ and π^- with equal deposited energy (~10 GeV γ)



efficiency vs. contamination for γ



MAPS half layer



multilayer PCB

- is substrate for PHASE1
- connects bondwires to macroscopic world
- components for power regulation and filtering
- clock and signal at 160 MHz
- has connector for chiptesting, to be replaced by flatcable for read-out