Development of Readout System for Double-sided Silicon Strip Modules

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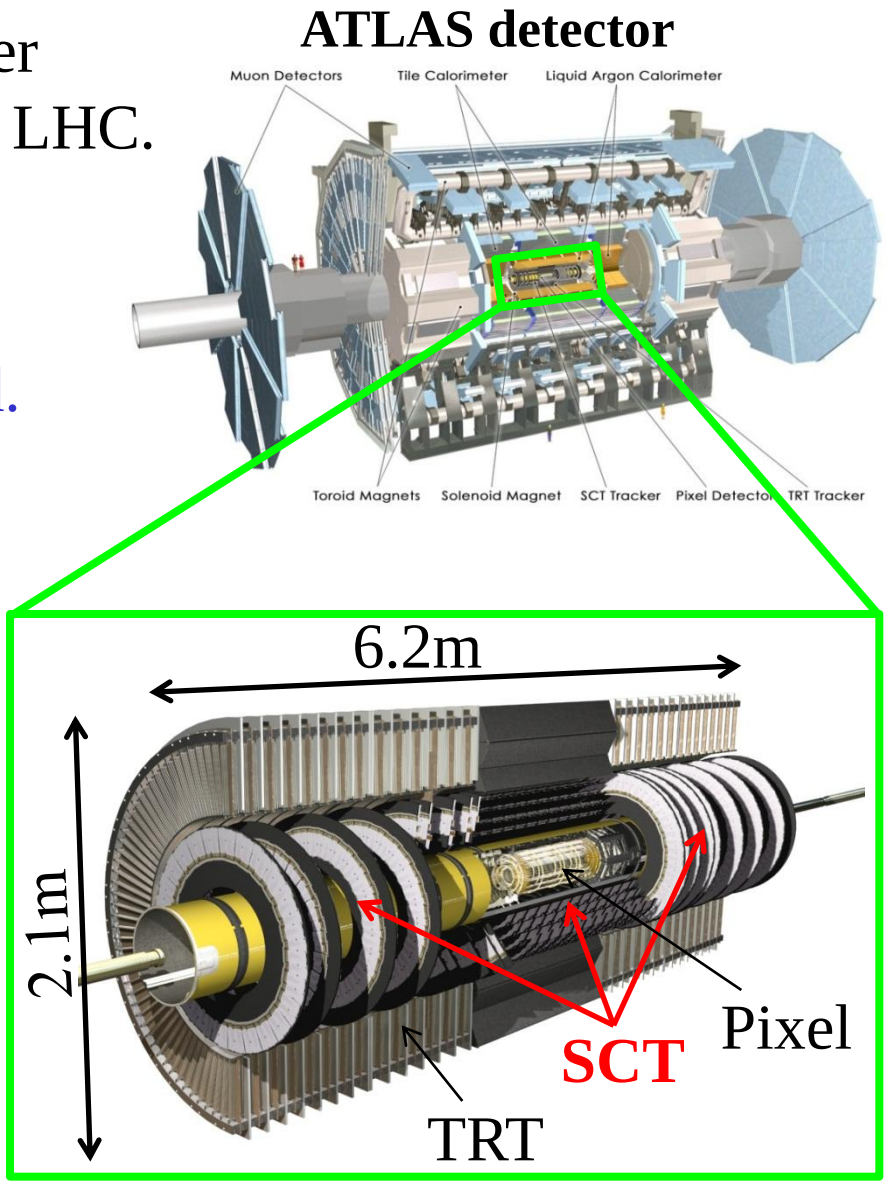
ATLAS detector upgrade

- ATLAS detector will be upgraded after 2022 for high luminosity operation at LHC.
- Target of the integrated luminosity is $3000fb^{-1}$.
- All the inner trackers will be replaced.
  - Pixel detector
  - SCT (Silicon tacker)
  - TRT (Transition radiation tracker)
    - ✓ replaced by SCT or others.

New double-sided SCT modules have been developed, based on super-module concept.

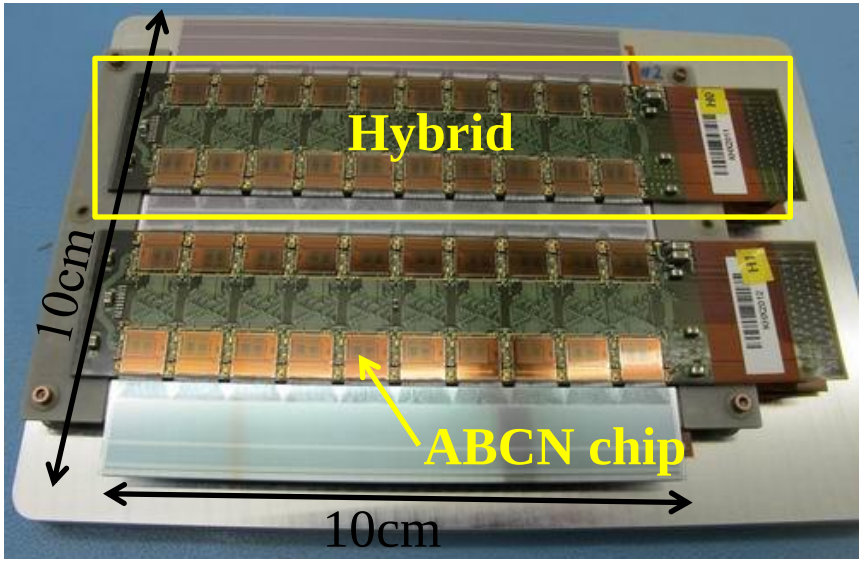


Super-module concept

SCT module

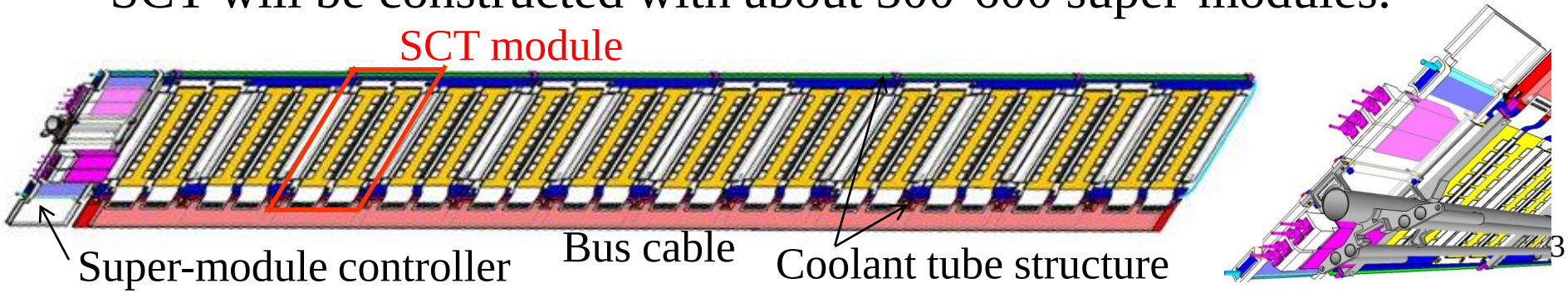
- n-in-p sensor (1280 strips)
- Sensor size: 10cm x 10cm
- Strip length: 2.4cm (74.5 um pitch)
- 4 hybrids are connected to the sensor.
  - 20 ABCN FE chips for each hybrid

SCT module



One super-module consists of 12 SCT modules.

- SCT will be constructed with about 500-600 super-modules.

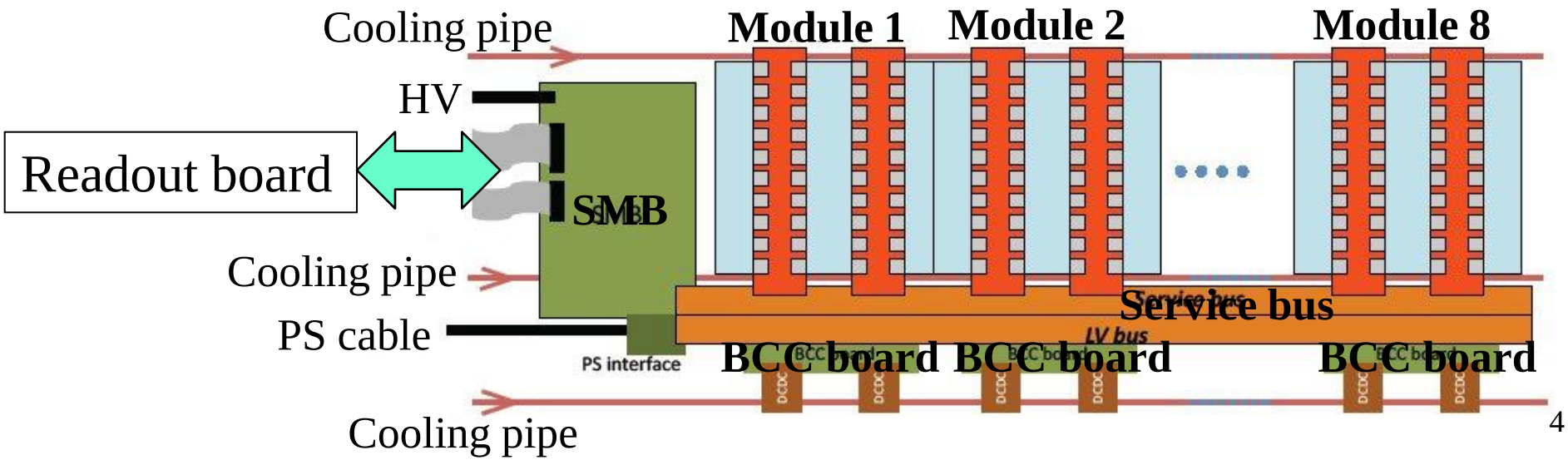


SCT super-module prototype

SCT super-module prototype is under construction.

- SCT module: 8
  - 640 ABCN FE chips
- BCC board: 16 (32 BCC chips)
- Service bus
- SMB (Super-module board)
  - A interface board between ASICs and a readout board.

These ASICs deal with signals from sensors.

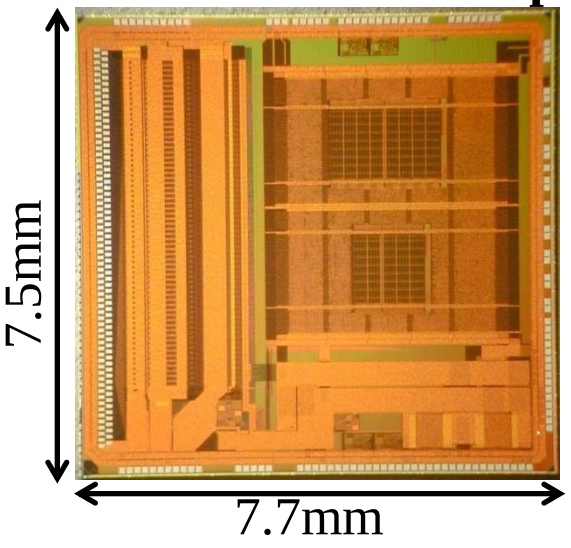


ABCN front-end chip & BCC chip

ABCN chip

- 0.25 um IBM CMOS6 technology
- # of readout strip: 128
- Hit data for 128 strips is output serially.
- Data output rate: 40/80MHz
- IEEE Nucl. Sci. Sym. Conf., Orlando, USA, 2009, p373-380.

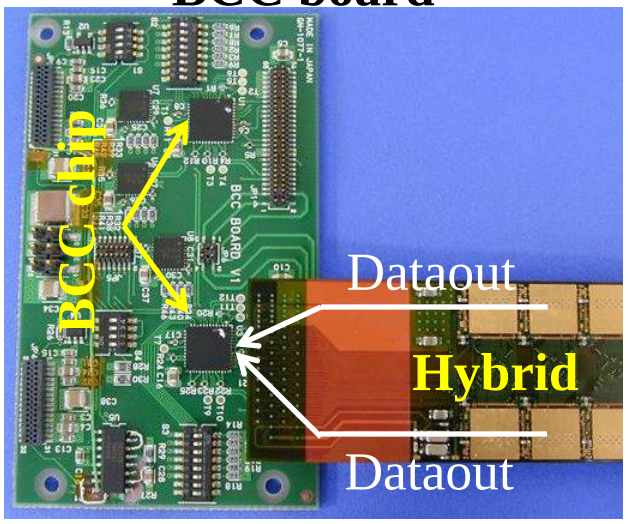
ABCN front-end chip



BCC chip

- Data multiplexer for two links of 10 ABCNs.
- Data output rate: 80MHz/160MHz
- Two BCCs are mounted on one BCC board.

BCC board



The new DAQ system is necessary to operate and readout ABCN/BCC chips.

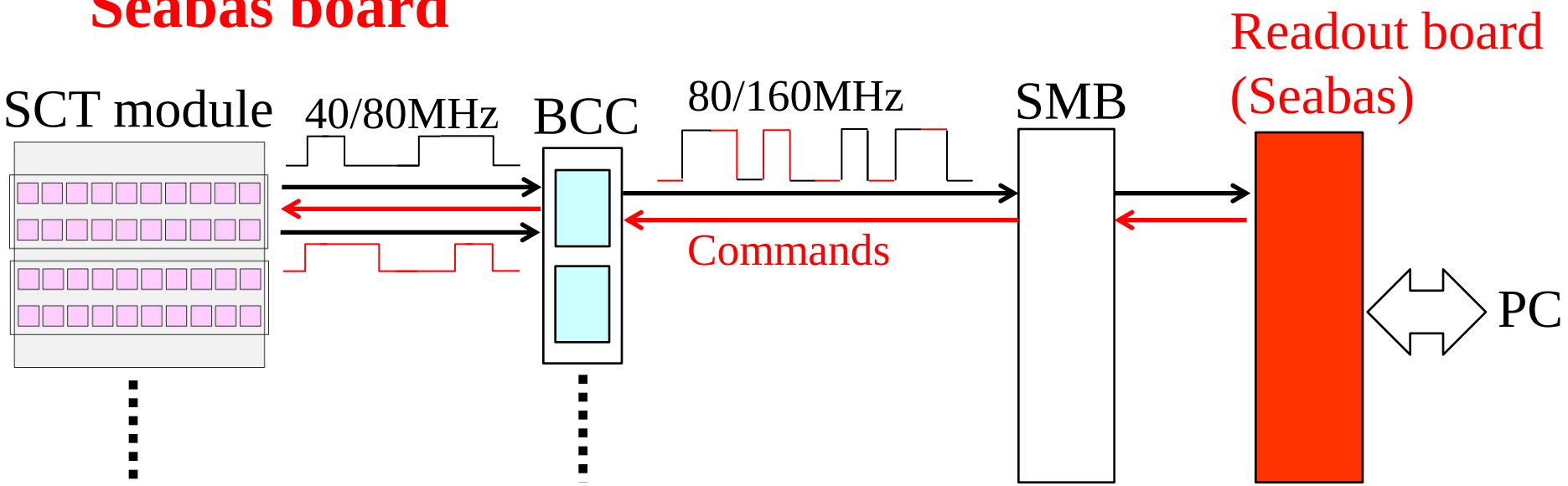
DAQ system for prototype testing

Requirement for DAQ system

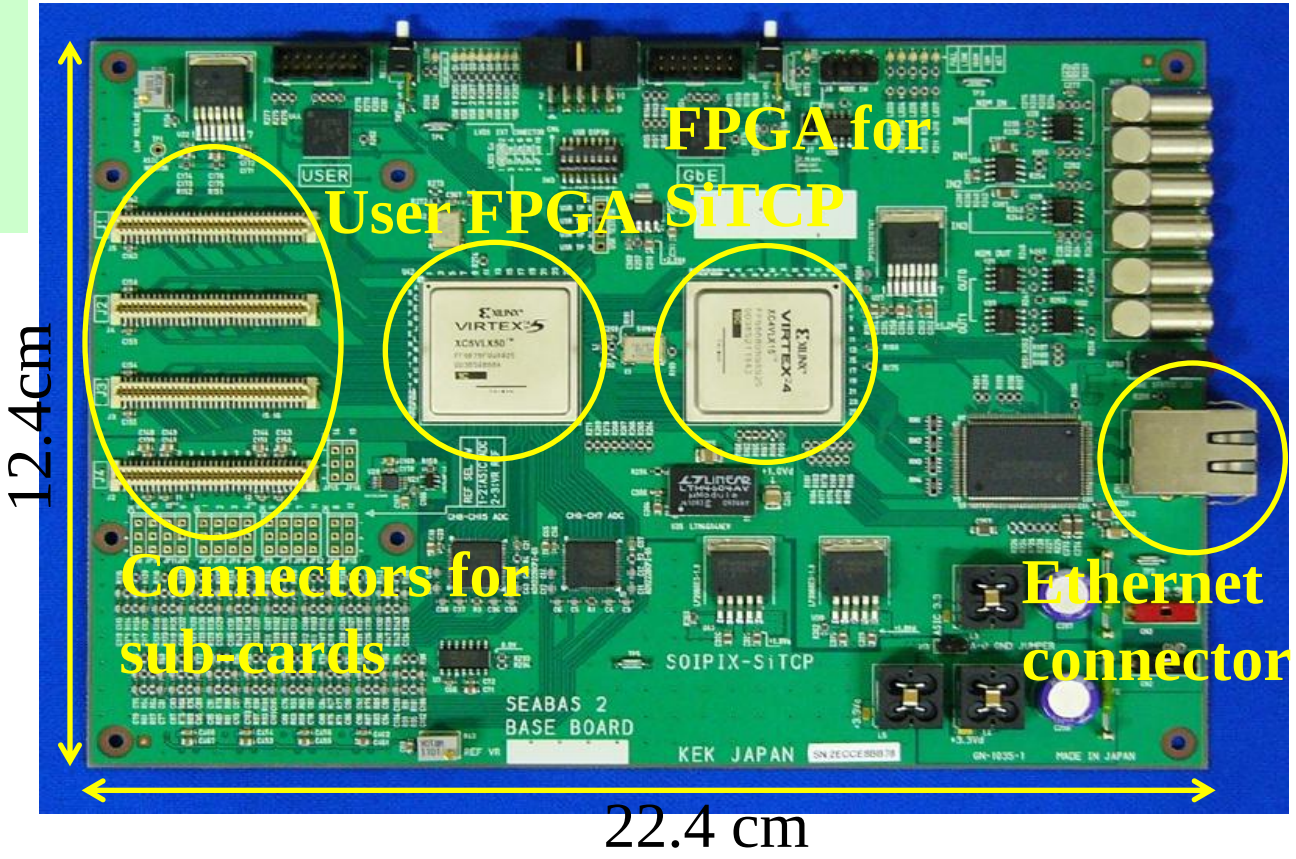
- Data readout rate: 80MHz/160MHz
- Operate 640 ABCN chips via 32 BCC chips
  - # of readout strips: 122,880

→ The fast multi-readout DAQ board is necessary.

Seabas board



Seabas



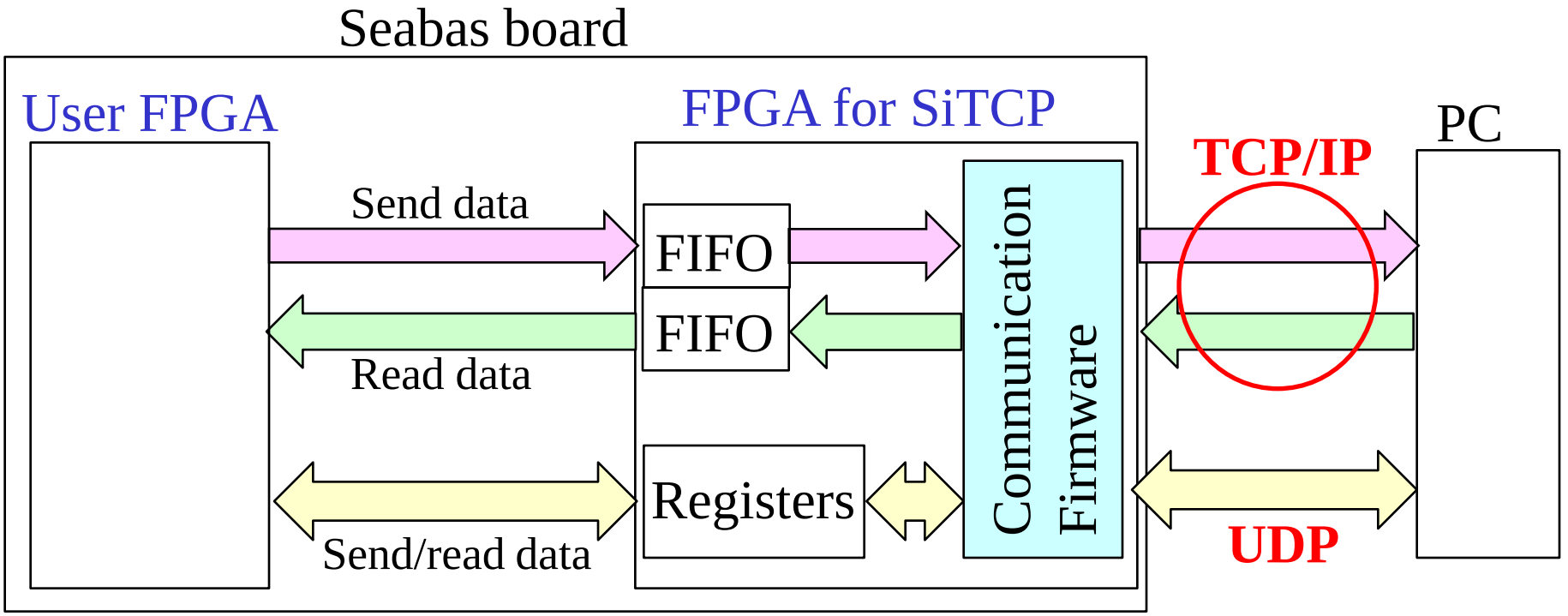
- Data processing is done with program implemented in a User-FPGA.
- **SiTCP realizes TCP/IP and UDP connection with a FPGA.**
  - Technology developed at KEK. (IEEE Trans. Ncul. Sci. Vol. 55, No. 3, 2008)
  - Data transfer rate: 100 Mbps (Latest version: 1Gbps)
- 4 sub-cards can be attached.

Seabas is easy to handle with PC via ether-net by using SiTCP.

Communication with PC via SiTCP

- SiTCP is interface of ether-net communication between User-FPGA and PC.
- Users only have to send(read) data to(from) FIFO/Registers in SiTCP.
- All the libraries for the communication is prepared in Unix-based OS.

→ **User can focus on only development of program in User-FPGA.**

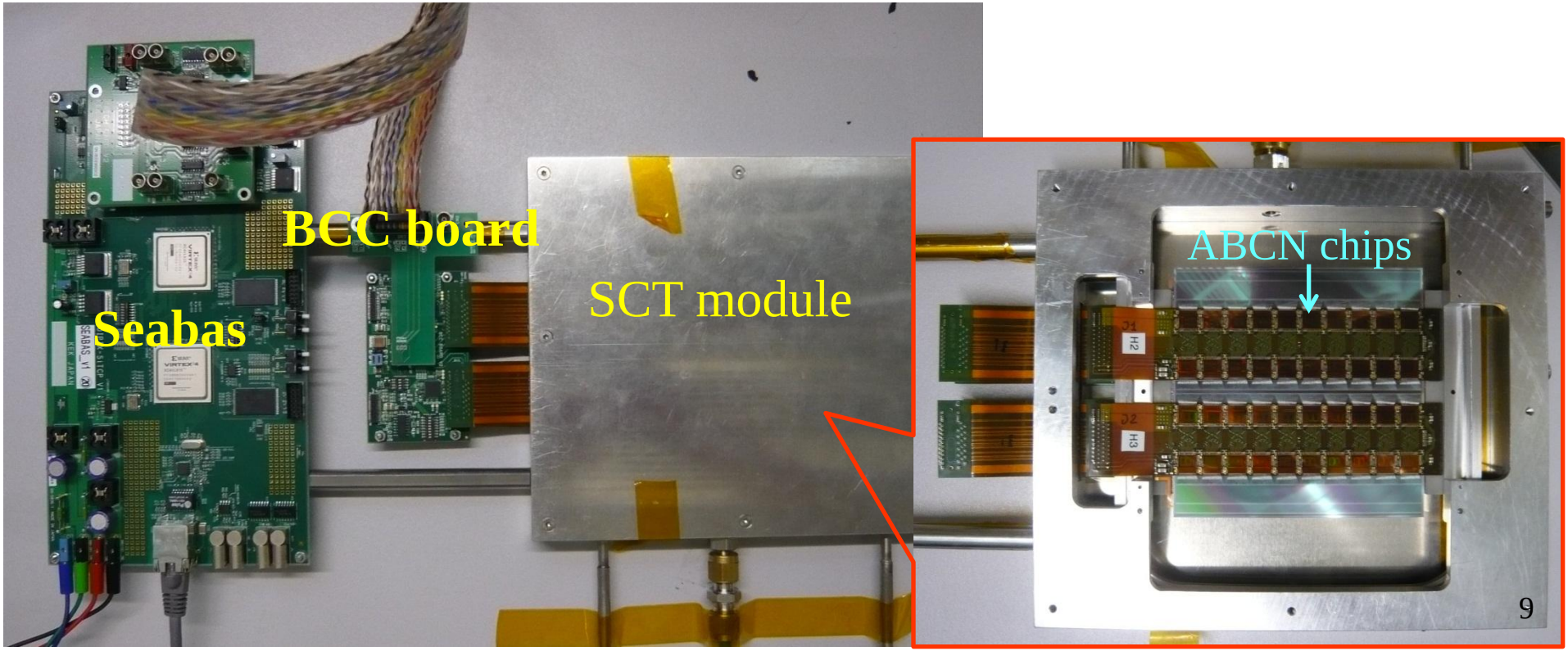


Setup for one SCT module readout

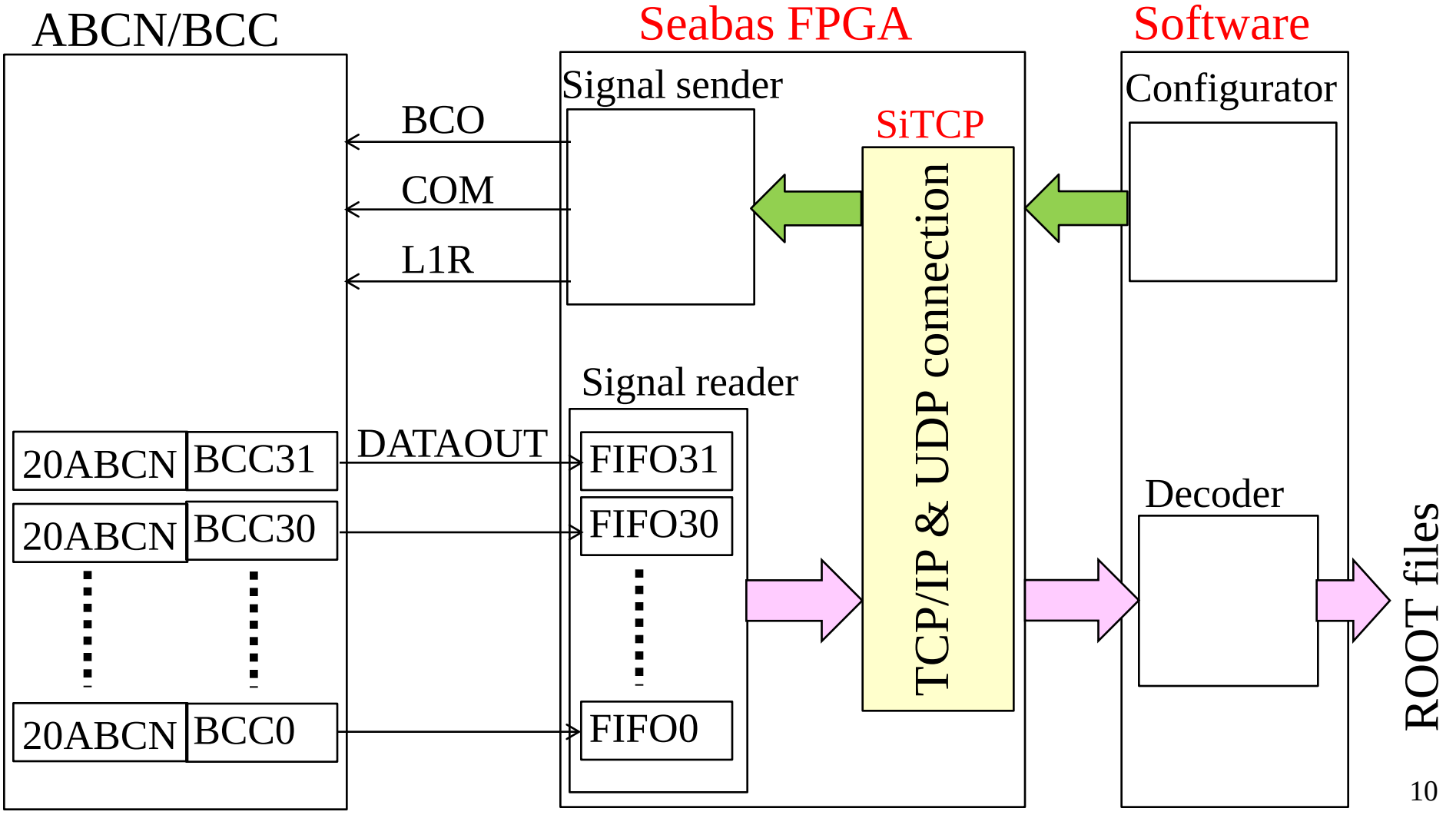
As the first step, DAQ system to read one SCT module was constructed.

- Components: 1 SCT module, 1 BCC board, Seabas board
- Readout strip: 10,240 (80 ABCN chips)

→ FPGA firmware and software were developed for Seabas board.



Firmware and software



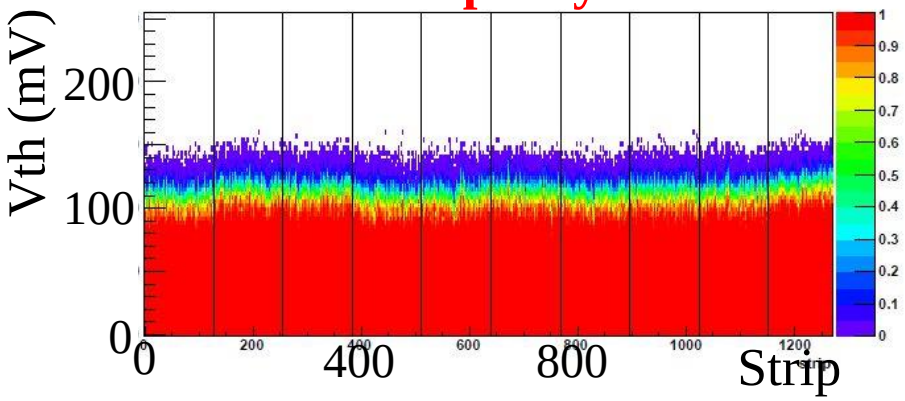
The performance check was done for one SCT module.

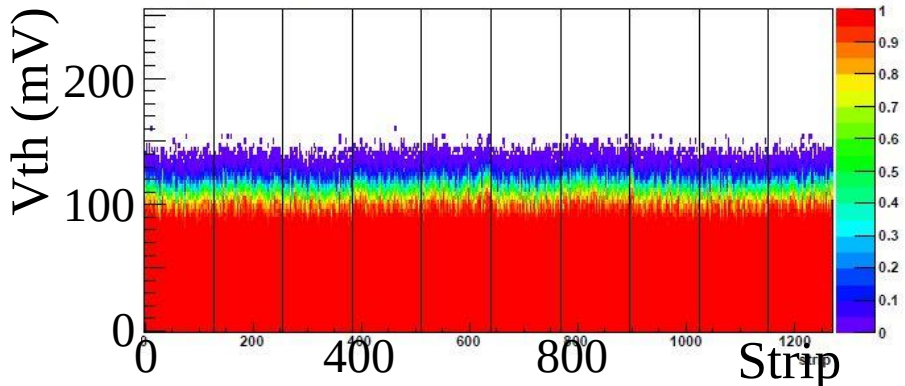
Threshold scan

Threshold scan was performed for the input charge of 1fC.

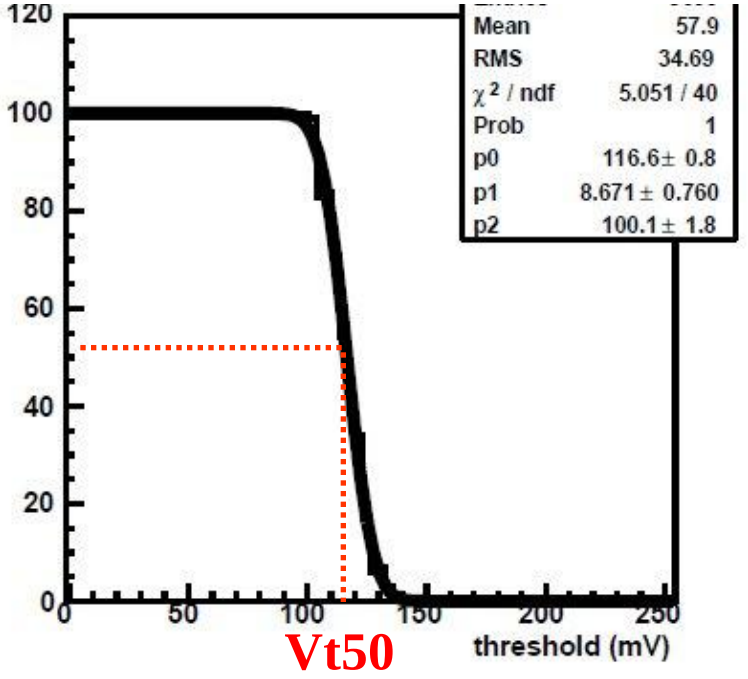
- The threshold is determined by fitting with error-functions.
- Threshold (vt50): threshold voltage at 50% efficiency

Hit occupancy





Typical threshold curve



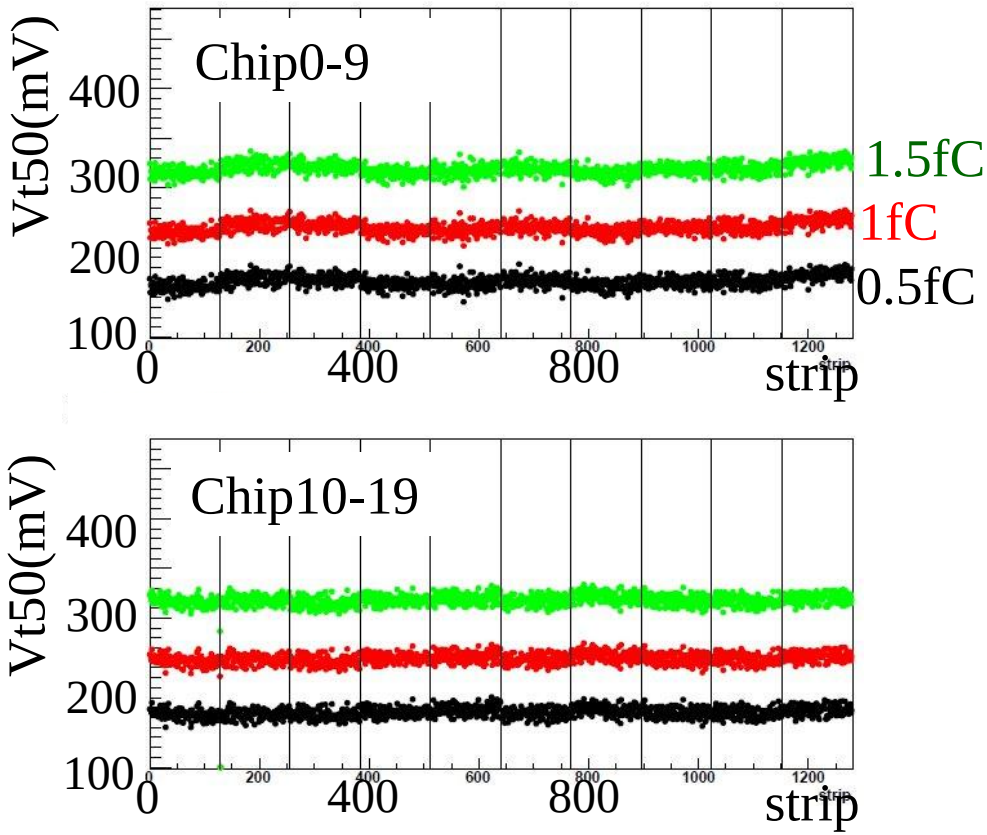
Measurement of 3-point gain

The threshold was measured for input charge of 0.52, 1, 1.52 fC.

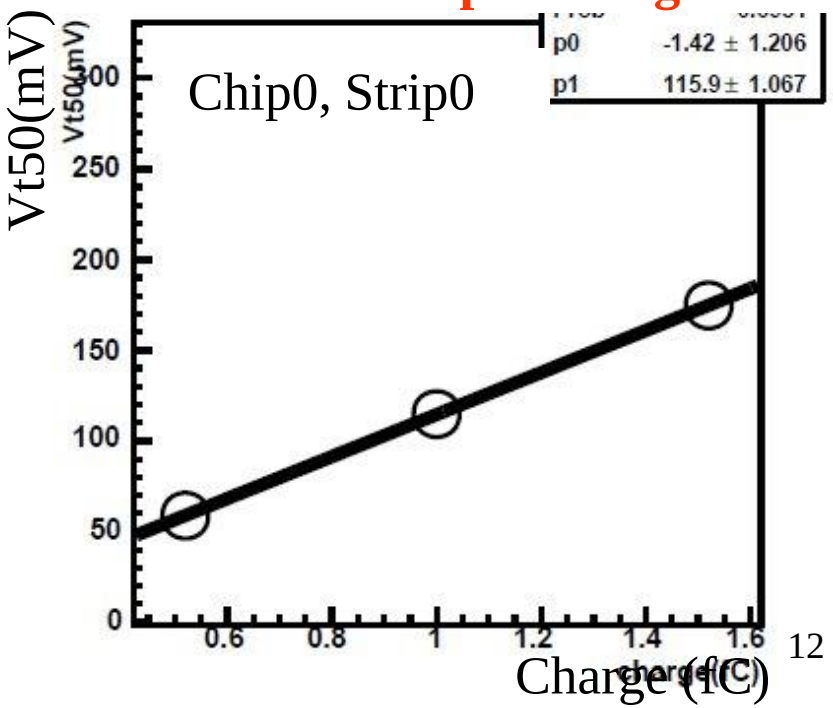
- Clear linear dependence of Vt50 on input charge can be seen.

→ Gain(mV/fC) was evaluated by fitting plots of charge v.s. Vt50.

Vt50 v.s. strip



Vt50 v.s. Input charge

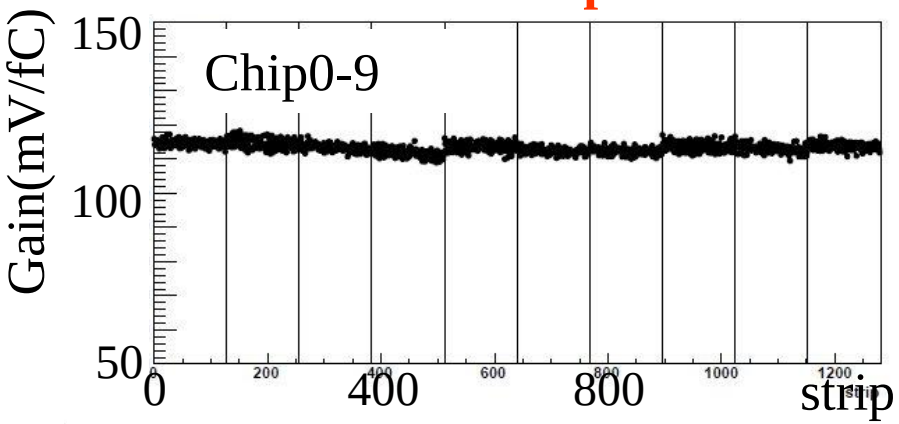


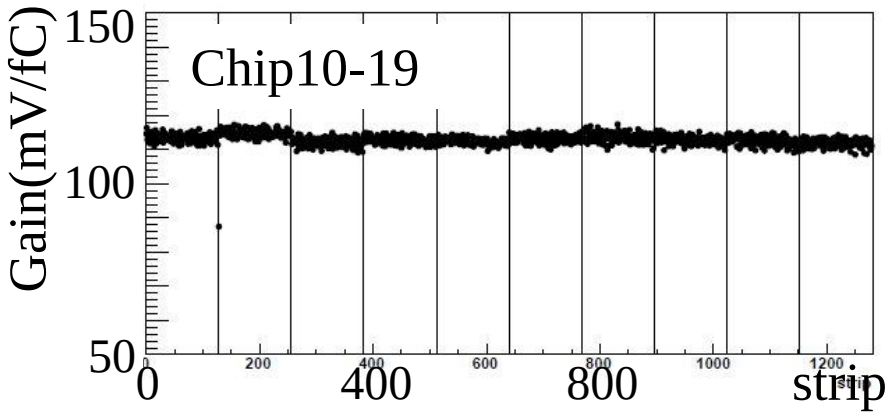
Gain distributions

The gain distributes around 110 mV/fC.

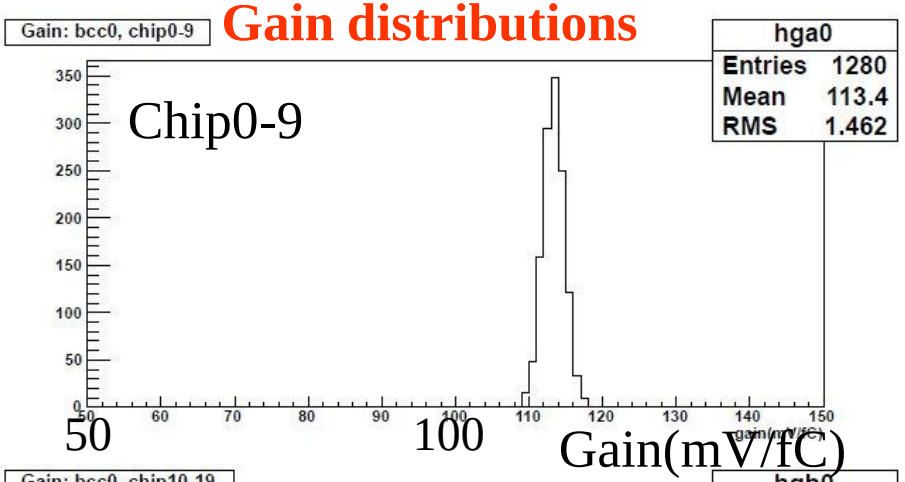
- Reference value of ABCN chips: 90 mV/fC.

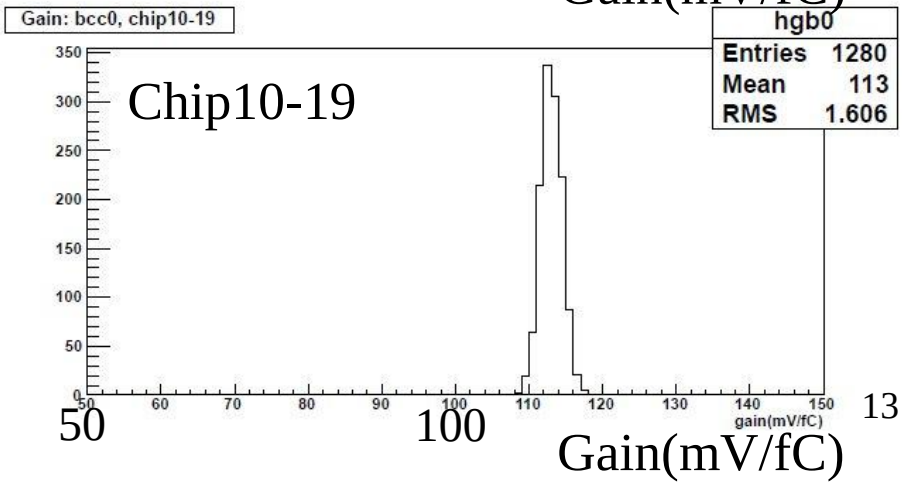
Gain v.s. strip





Gain distributions





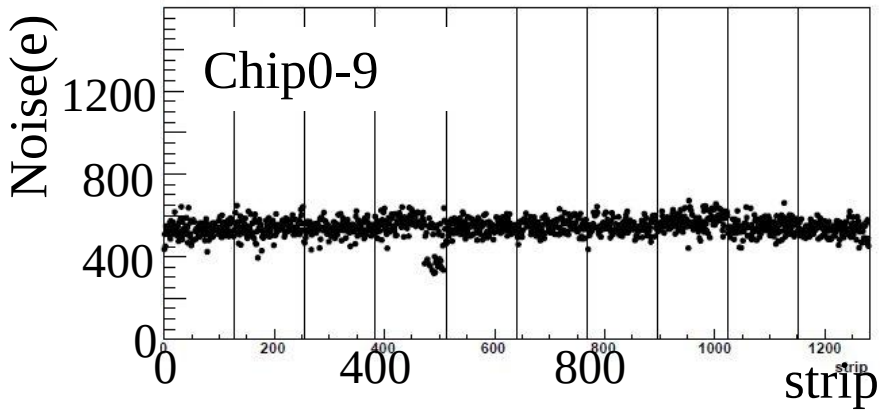
Noise level

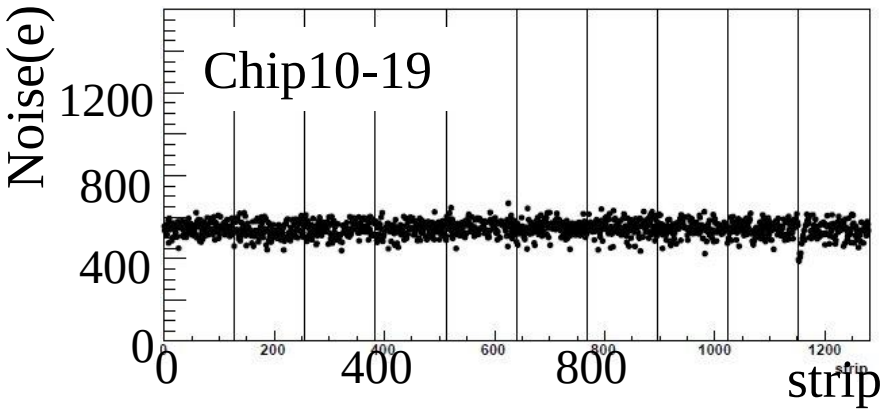
Noise level was evaluated by fitting threshold curves with err-func..

- Average noise: ~550e (ABCN chip only: ~375e)

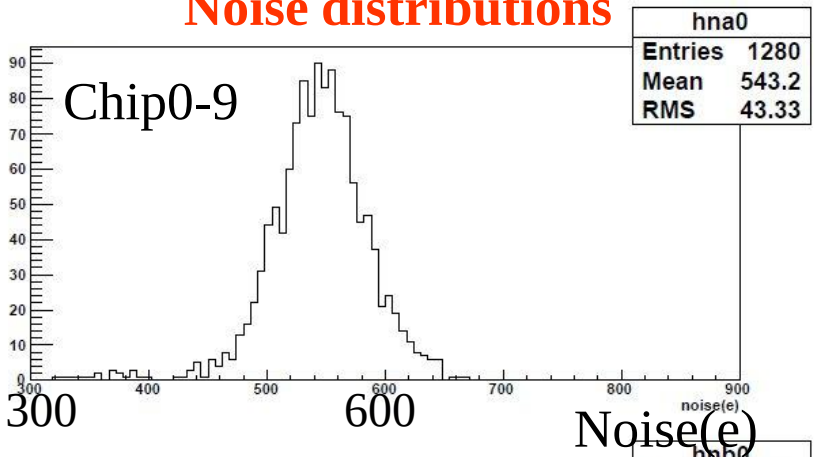
Seabas DAQ system works to read one SCT module!

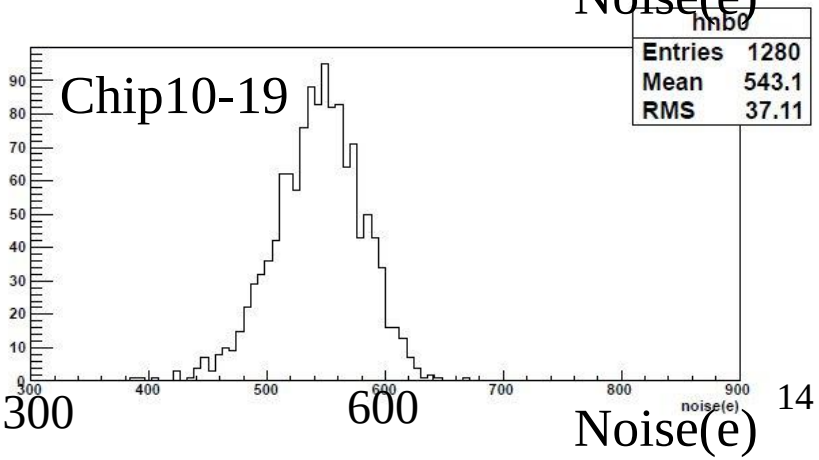
Noise v.s. strip





Noise distributions

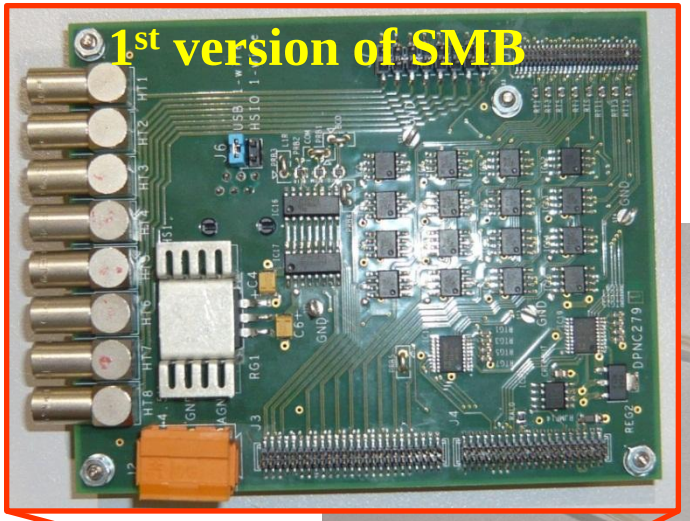




Readout of SCT super-module prototype

The super-module prototype will be constructed in August 2011.

- SMB and service bus are under development.
- The 1st version of SMB and service bus has design problem.



Prototype of SCT super-module will be tested with full-readout chain in August.

SCT module

SMB

Seabas

BCC board

Service bus

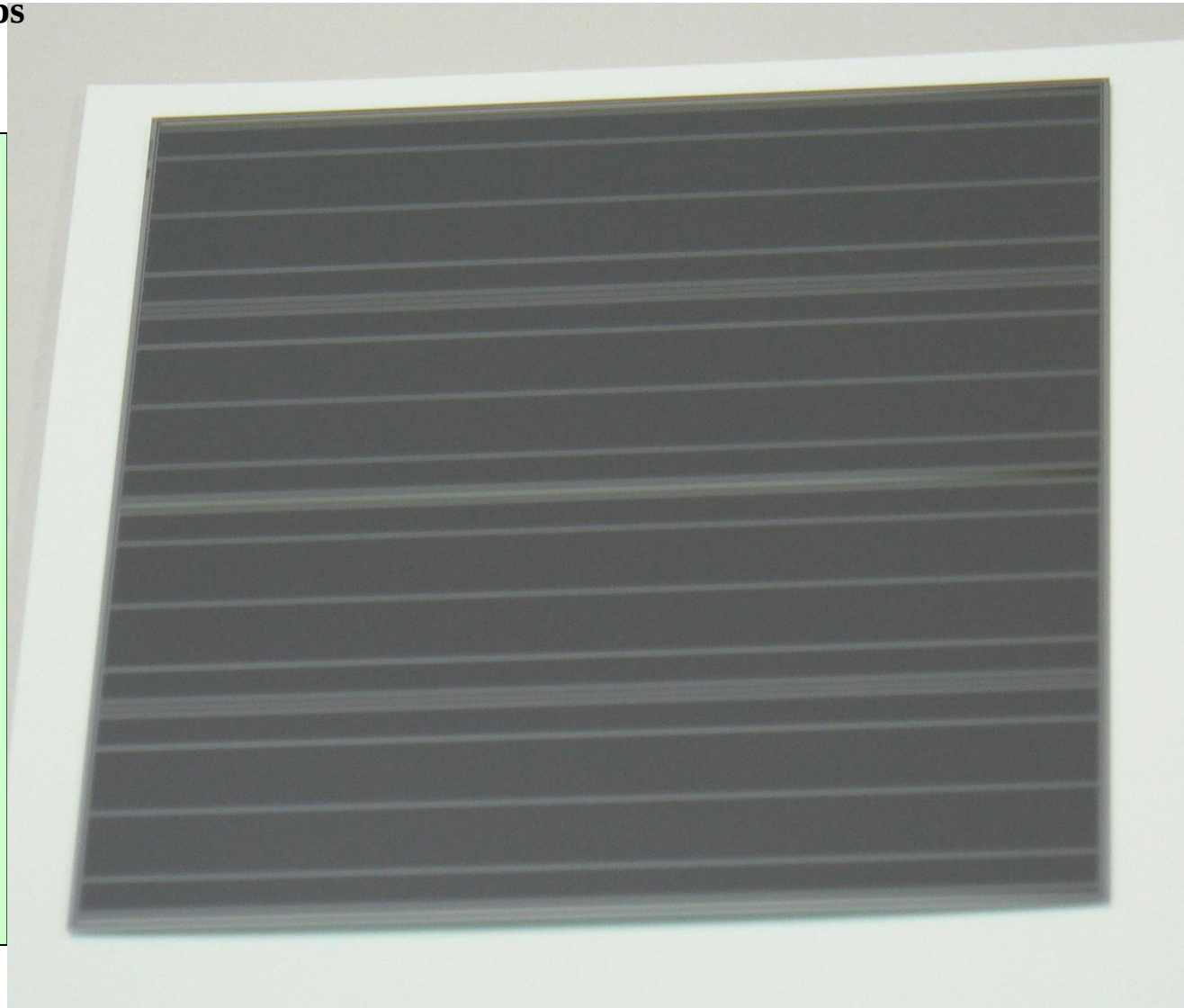
Summary & Conclusions

- The double-sided silicon strip modules are developed for ATLAS SCT upgrade after 2022.
- New DAQ system is developed to read prototype of SCT super-modules by using a Seabas board.
- Seabas board is easy to operate by PC via ether-net by using SiTCP.
- Seabas DAQ system works for performance check of one SCT module.
- Readout of the prototype will be started in August 2011.
  - SMB/service bus is under development.

Super-module sensors

- Strip segments
  - **4 rows of 2.38 cm strips (each row 1280 channels)**

- **Dimension**
  - **Full square**
- **Wafer**
  - **150 mm p-type FZ(100)**
  - **138 mm dia. usable**
  - **320 µm thick**
- **Axial strips**
  - **74.5 µm pitch**
- **Stereo strips**
  - **40 mrad**
  - **71.5 µm pitch**
- **Bond pads location**
  - **accommodating 24-40 mm distances**
- **n-strip isolation**
  - **P-stop**
  - **Spray on miniatures**



Material budget

Material budget accountancy on module:

• Sensors (300 μm)	0.64 %X_0	
• TPG +glue +AlN spacers + washers	0.29 %X_0	**Module: 1.82 %X_0**
• Hybrids + active components	0.70 %X_0	
• Hybrid bridge	0.19 %X_0	
• Cable bus	0.31 %X_0	
• Local support, pipes, blocks, inserts	0.45 %X_0	
	Total 2.58 %X_0	

Adjustment of data timing window

- Hit data is stored in ABCN chips for 6.7 us before L1 trigger.
  - Hit data for 3 bits is output.
- Timing to get 3-bit hit data must be adjusted.
  - $t_{up} + (t_{down} - t_{up})/4$ (t_{up}, t_{down}: Time at 50% efficiency)