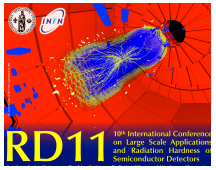


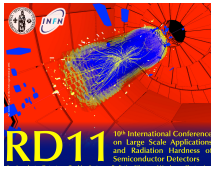
Results on Array-based Opto-Links

K.K. Gan, H.P. Kagan, R.D. Kass, H. Merritt,
J. Moore, A. Nagarkar, D. Pignotti, S. Smith, M. Strang
The Ohio State University

P. Buchholz, A. Wiese, M. Ziolkowski
Universität Siegen

July 8, 2011

Outline

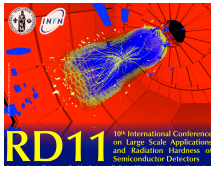


- Introduction
- Results on 4-channel Driver/Receiver with Redundancy
- Design of New 12-channel Driver/Receiver with Redundancy
- Summary

Why Optical Data Links?

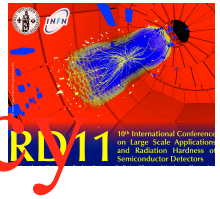
- Optical data transmission is now preferred over copper wire links:
  - lower mass
  - much higher data transmission rate over long distance (80 m)
  - break the ground loop between front and back-end electronics
- Optical transmitter: vertical cavity surface-emitting laser (VCSEL)
- Optical receiver: PIN diode
- Optical device can have one, four, or twelve channels

Array Optical Links: Today



- array solution has three major advantages:
  - compact: more channels in less space
  - robust: 12-fiber ribbon is stronger than an individual fiber
  - efficient: can reserve 1 in 12 channels for redundancy instead doubling the number of channels
- 120 Gb/s VCSEL/PIN array based links are now commercial standard
  - 12-fiber ribbon, 12 channel VCSEL/PIN array, 10 Gb/s each
- 12-channel array VCSEL and PIN are available from several vendors
  - vendors forthcoming on providing reliability and qualification info
  - quite a different situation than in ~2003 when implementing array based on-detector links for ATLAS pixel detector
    - enabled fabrication of only 272 array-based opto-modules instead of 1,744 single-link opto-modules

Driver/Receiver with Redundancy



- designed an updated version of VCSEL driver and PIN receiver of current ATLAS Pixel detector but with redundancy
  - possible applications include current ATLAS pixel detector and its upgrade, IBL (Insertable Barrel Layer), in 2013-4
  - experience gained from the development/testing of such new chips would help the development of on-detector array-based opto-links for HL-LHC
  - submission of 1st prototype chip (130 nm CMOS) in 2/2010

Chip Content

Design

Photo

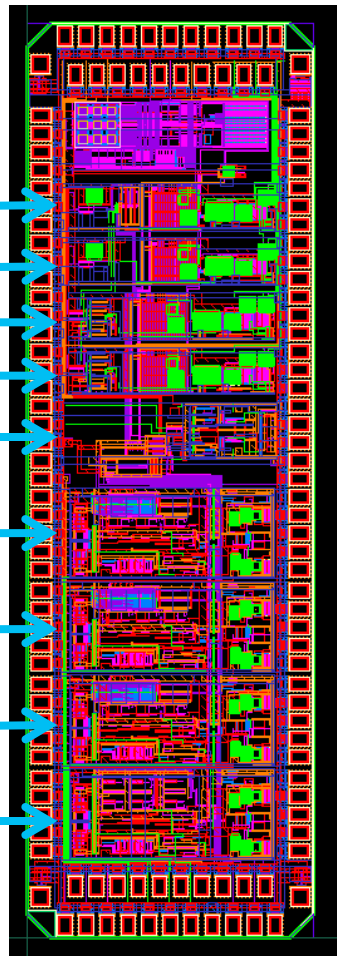
VCSEL Driver (spare)
VCSEL Driver
VCSEL Driver with pre-emphasis
VCSEL Driver with pre-emphasis
CML Driver with pre-emphasis

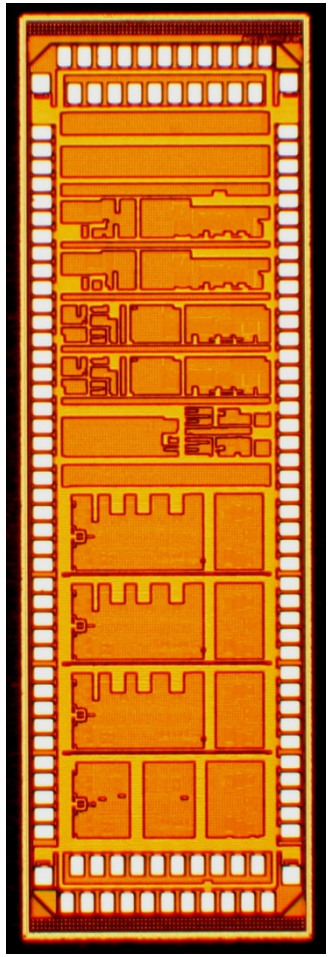
Decoder (40Mb/s)

Decoder (40Mb/s)

Decoder (40Mb/s)

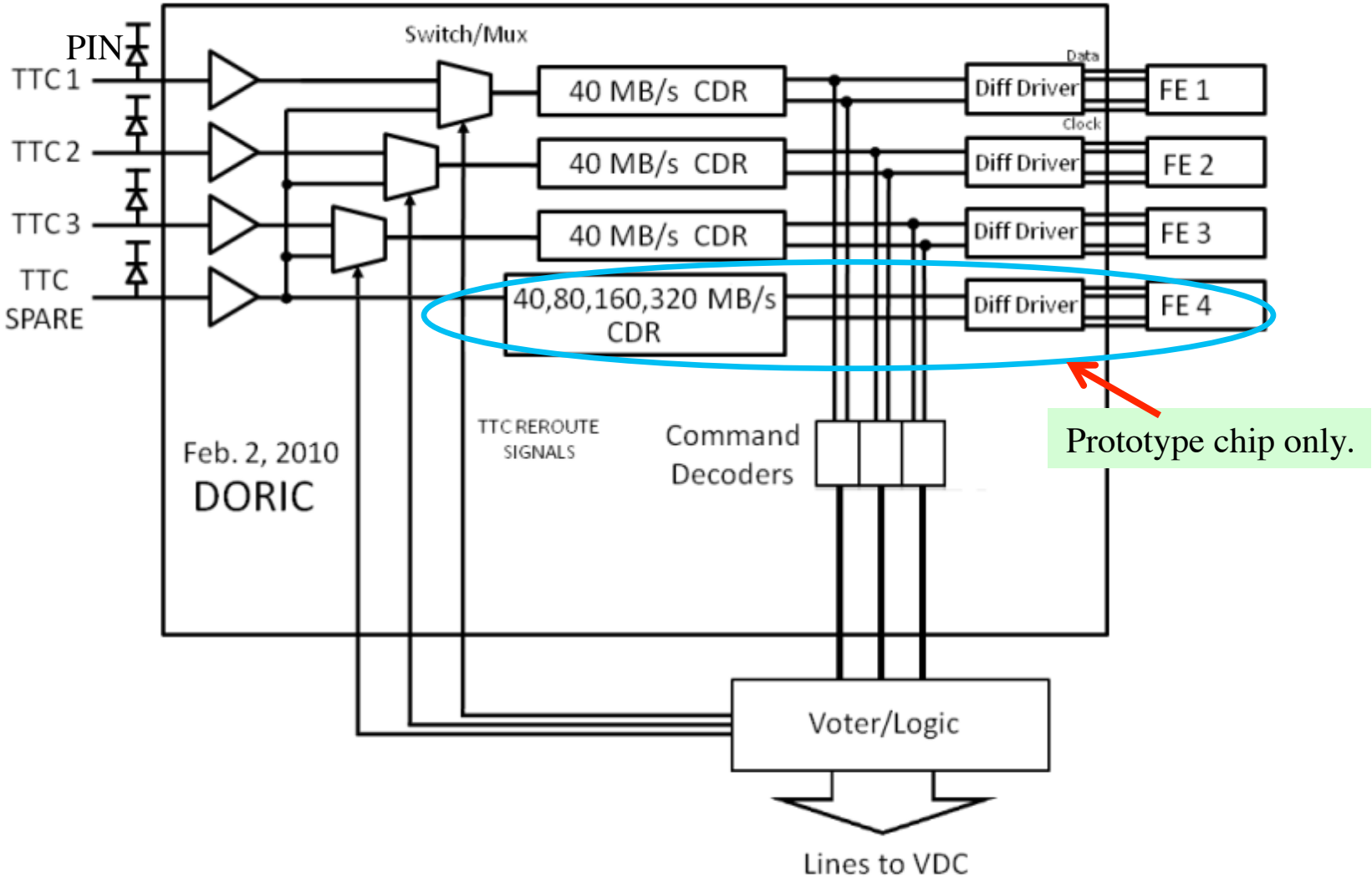
Decoder (40/80/160/320 Mb/s, spare)





1.5 mm

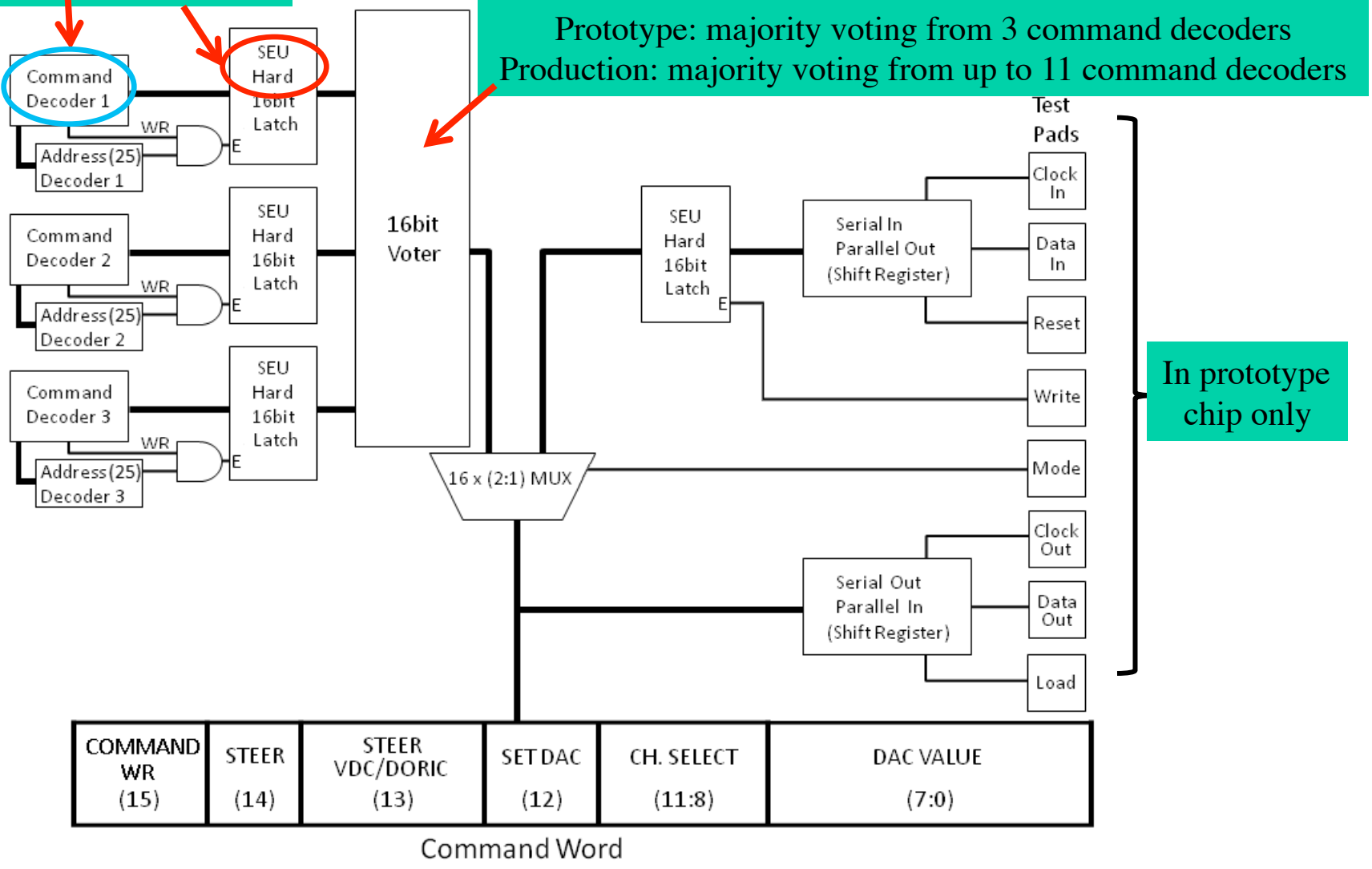
PIN Receiver/Decoder



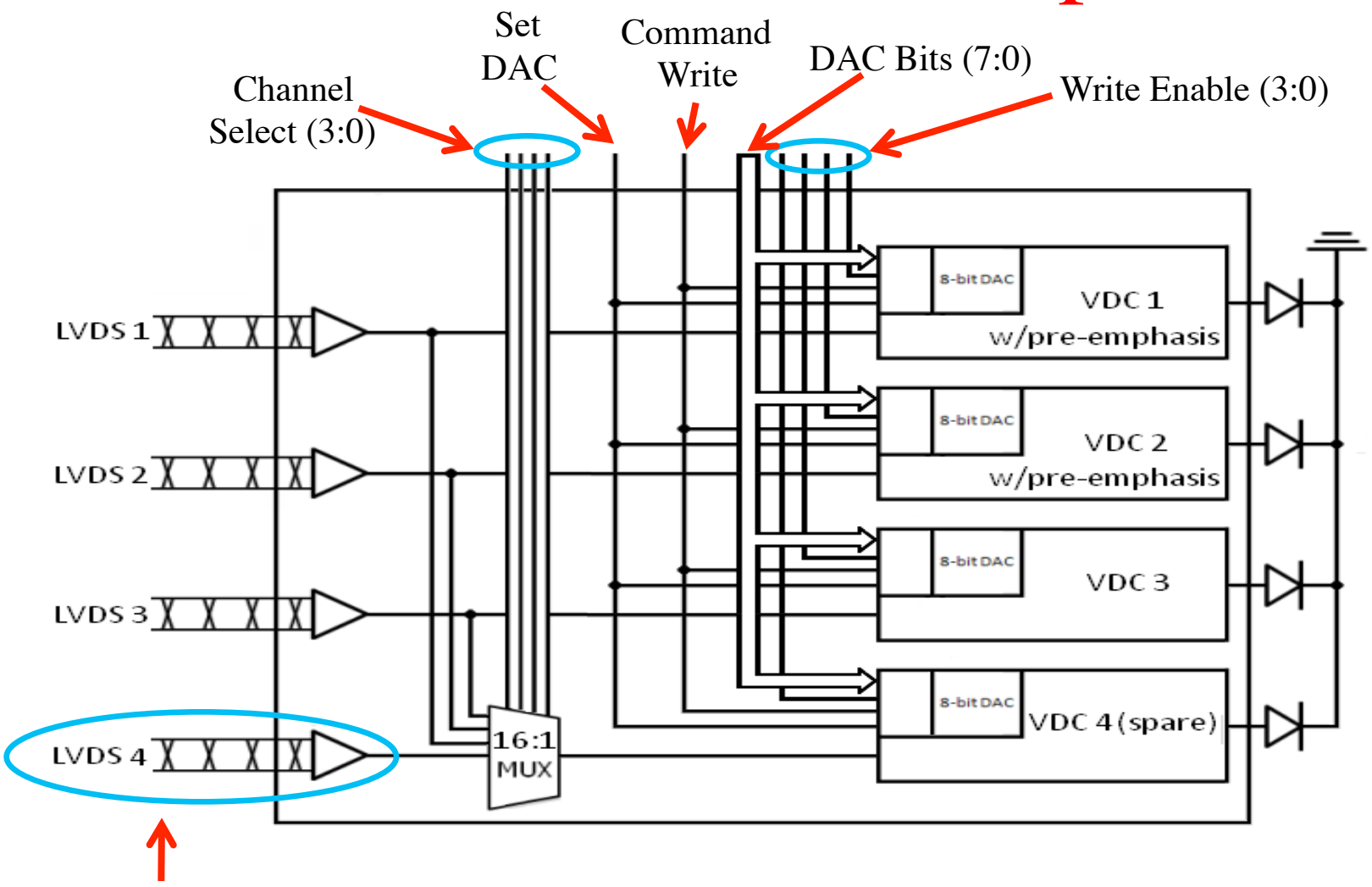
Command Decoder Interface

Courtesy of FE-I4 of IBL

Prototype: majority voting from 3 command decoders
Production: majority voting from up to 11 command decoders



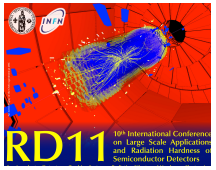
VCSEL Driver Chip



LVDS input added for prototype chip only.

Irradiation

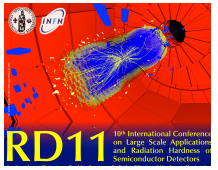
- 2 chips were packaged for irradiation with 24 GeV/c protons at CERN in August 2010
  - each chip contains 4 channels of drivers and receivers
  - total dose: 1.6 x 10^{15} protons/cm^2
  - all testing are electrical to avoid complications from degradation of optical components
    - ⇨ long cables limited testing to low speed
  - ✔ observe little degradation of devices



Single Event Upset

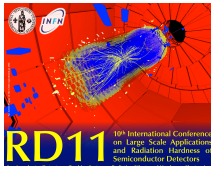
- SEU harden latches or DAC could be upset by traversing particles
  - 40 latches per 4-channel chip
  - SEU tracked by monitoring the amplitude of VDC drive current
  - 13 instants (errors) of a channel steered to a wrong channel in 71 hours for chip #1
    - similar upset rate in chip #2
    - ⇨ $\sigma = 3 \times 10^{-16}\ cm^2$
    - particle flux $\sim 3 \times 10^{9}\ cm^{-2}$/year @ opto-link location
    - ⇨ SEU rate $\sim 10^{-6}$/year/link

Summary of Prototype Chips



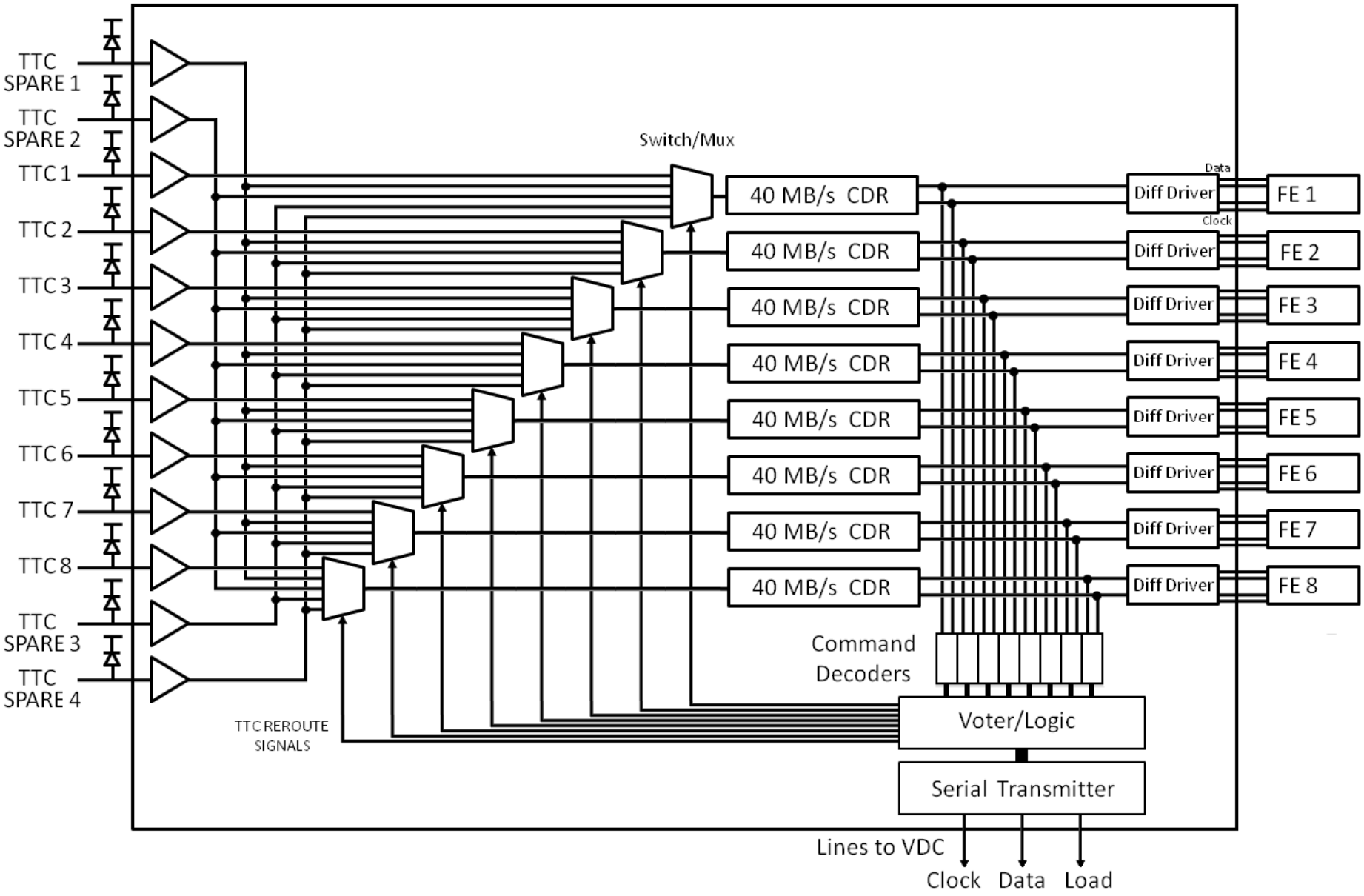
- prototyped 4-channel VCSEL driver and PIN receiver/decoder:
  - ✔ redundancy to bypass broken PIN or VCSEL channel
  - ✔ individual VCSEL current control
  - ✔ power-on reset to set VCSEL current to ~10 mA on power up
  - ✔ VCSEL driver can operate up to ~ 5 Gb/s with BER < 5×10^{-13}
  - ✔ receiver/decoder properly decodes signal with low threshold
  - ◆ irradiation with 24 GeV protons to 1.7 x 10^{15} p/cm^2
    - ✔ small decrease in VCSEL driver output current
    - ✔ very low SEU rate in latches: ~3×10^{-7}/year/link

2011 PIN Receiver/Decoder

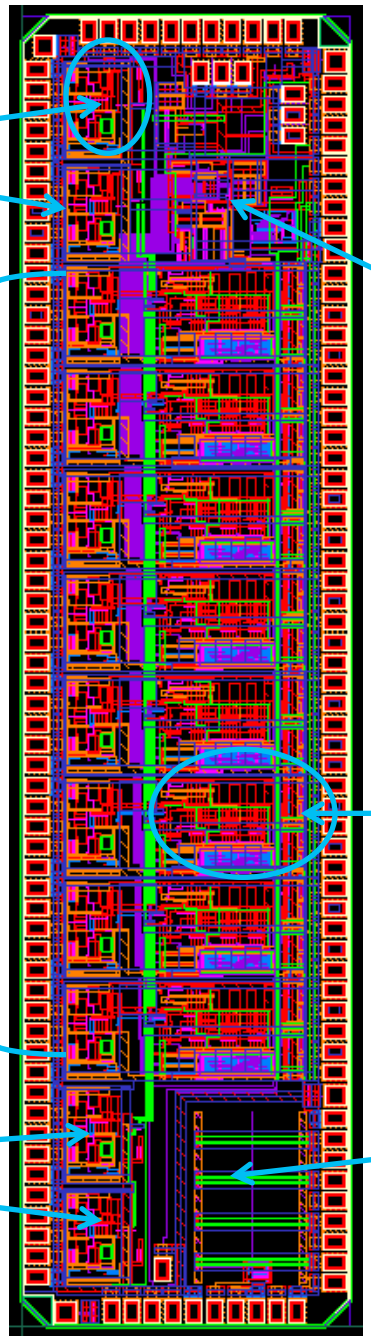


- Decodes 40 Mb/s bi-phase mark (BPM) signal
- 4 spare PIN receivers for redundancy
- 8 FE-I4 command decoders
  - Allows remote control by voting between commands received by the 8 FE-I4 command decoders
  - If one of the 8 inner PIN diodes fail
    - ⇨ signal from one of the 4 redundant channel amplifier outputs can be steered to the digital portion of the failed channel
  - Majority voting of the command decoder values determines the command to be executed
  - Allows working control if only 2 PIN channels are alive

2011 PIN Receiver/Decoder



PIN Receiver/Decoder



Spare PIN amplifiers

600 μm x 900 μm voltage regulator 2.5 V ⇨1.5 V

Submitted May 2011 – 6.5 mm x 1.6 mm

8 X DORIC

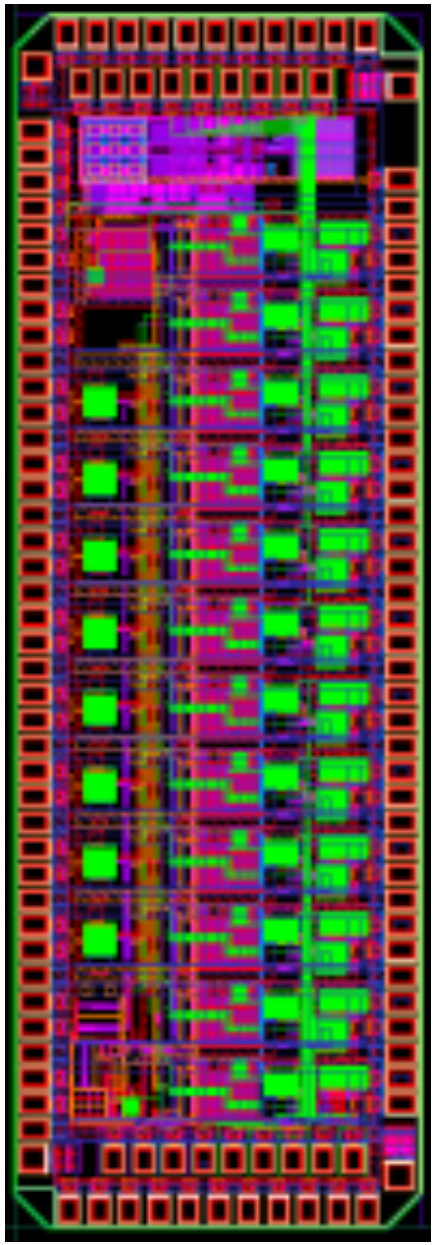
DLL + command decoder + LVDS driver

Spare PIN amplifiers

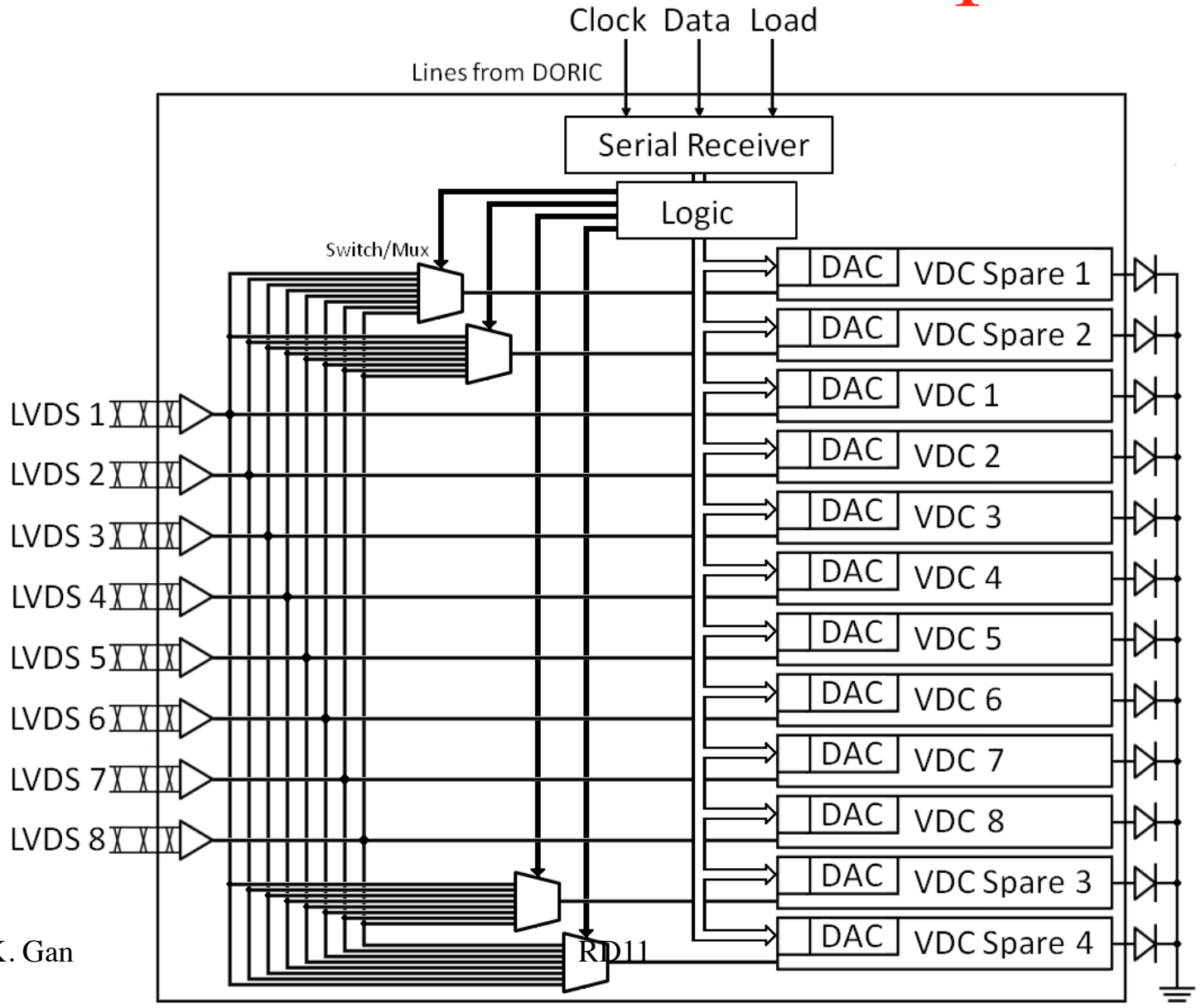
600 μm x 900 μm control logic

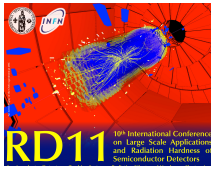
VCSEL Driver Chip

- Designed for 8 channel operation up to 5 Gb/s
- 4 spare VCSEL driver outputs
- Receives serial data from PIN receiver/decoder (command decoder vote) for configuration
- If one of the 8 inner VCSELs fail
  - ⇨ the data signal from the detector can be steered to any of the spare VCSELs
- 8 bit DAC for remote control of individual VCSEL current
- Submitted May 2011 – 1.5 mm x 4.5 mm



VCSEL Driver Chip





Summary

- 4-channel driver/receiver chips with redundancy and other improvements work well
- 12-channel driver/receiver chips with redundancy submitted in May
  - irradiation in September 2011
- Submit 4-channel driver/receiver compatible with HL-LHC in 2012