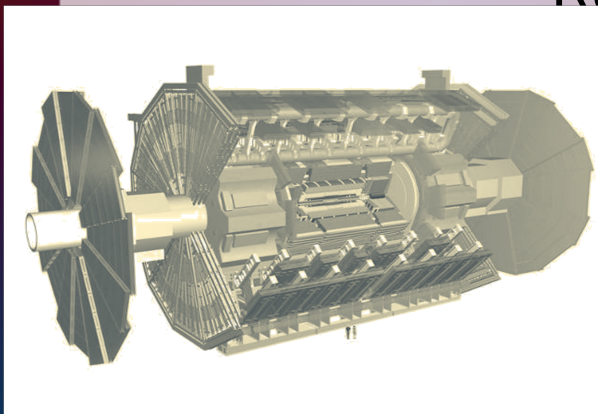# The EDRO board connected to the Associative Memory: a "Baby" FastTracKer processor for the ATLAS experiment

A. Annovi, **M. Beretta**, V. Bevacqua, F. Cervigni, F. Crescioli, L. Fabbri, P. Giannetti, F. Giorgi, D. Magalotti, A. Negri, M. Piendibene, C. Sbarra, C. Roda, M. Villa, R.A. Vitillo, G. Volpi
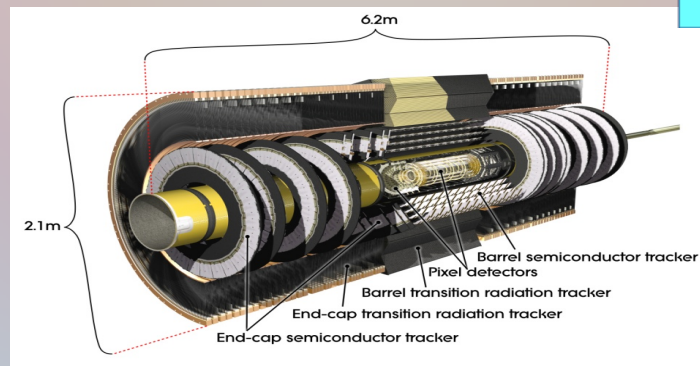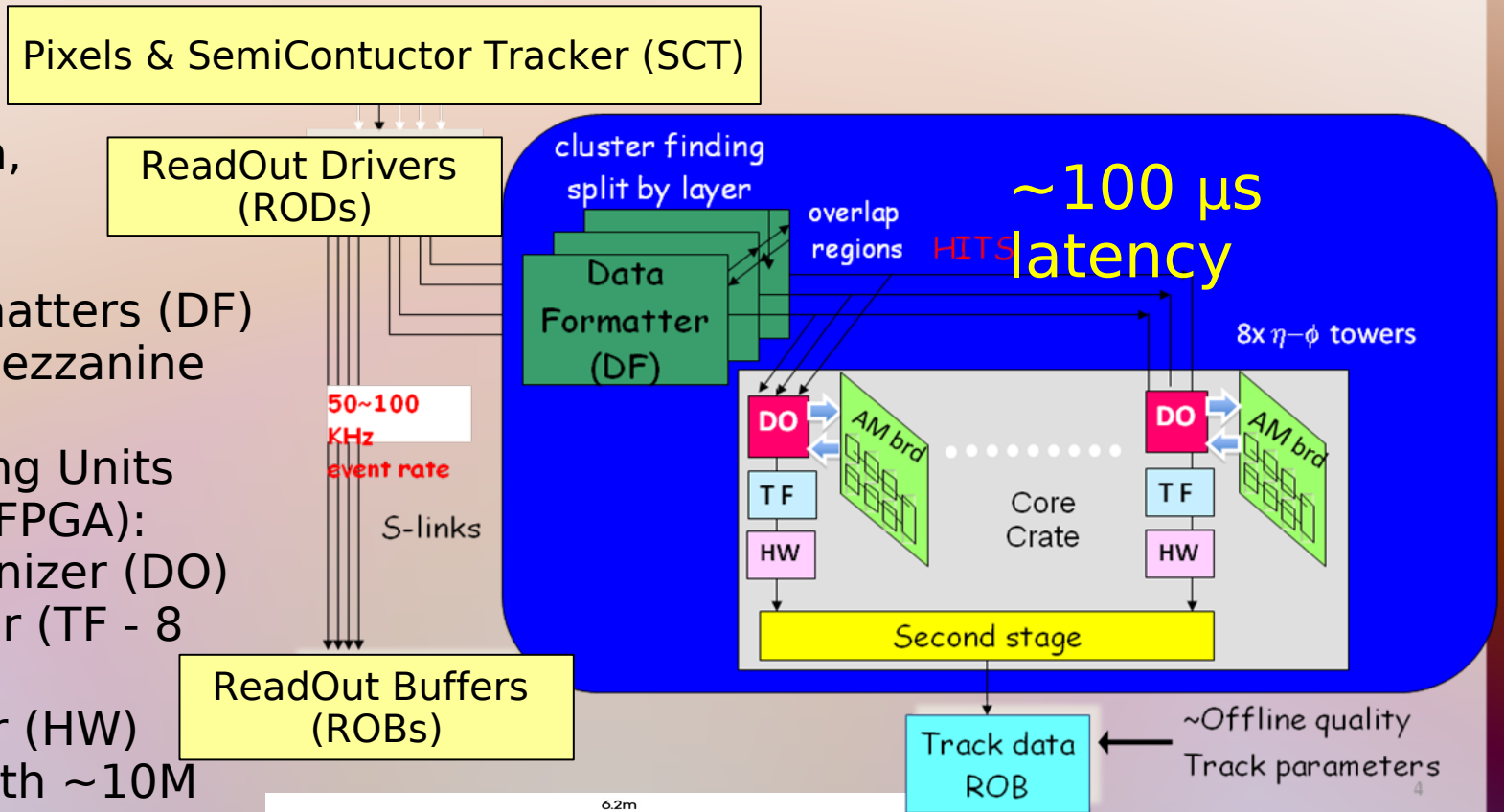
RD11 Conference
6-8 July 2011

FTK Architecture (final system)

Pixels & SemiContuctor Tracker (SCT)

Complex system, many units:

- **48** Data Formatters (DF)
  - Clustering Mezzanine

- **128** Processing Units
  - AUX Board (FPGA):
    - Data Organizer (DO)
    - Track Fitter (TF - 8 layers)
    - Hit Warrior (HW)
  - AM Board with ~10M patterns on AMchip04 custom CAMs

- **32** Final Boards (FPGA)
  - Final Fit (11 layers)
  - Final Hit Warrior

ReadOut Drivers (RODs)

ReadOut Buffers (ROBs)

cluster finding split by layer

overlap regions

HITS

Data Formatter (DF)

~100 μs latency

8x η–φ towers

DO

AM brd

TF

HW

Core Crate

DO

AM brd

TF

HW

Second stage

50~100 KHz event rate

S-links

Track data ROB

~Offline quality Track parameters

6.2m

2.1m

Barrel semiconductor tracker
Pixel detectors
Barrel transition radiation tracker
End-cap transition radiation tracker
End-cap semiconductor tracker

FTK will reconstruct tracks in all Inner Detector regions
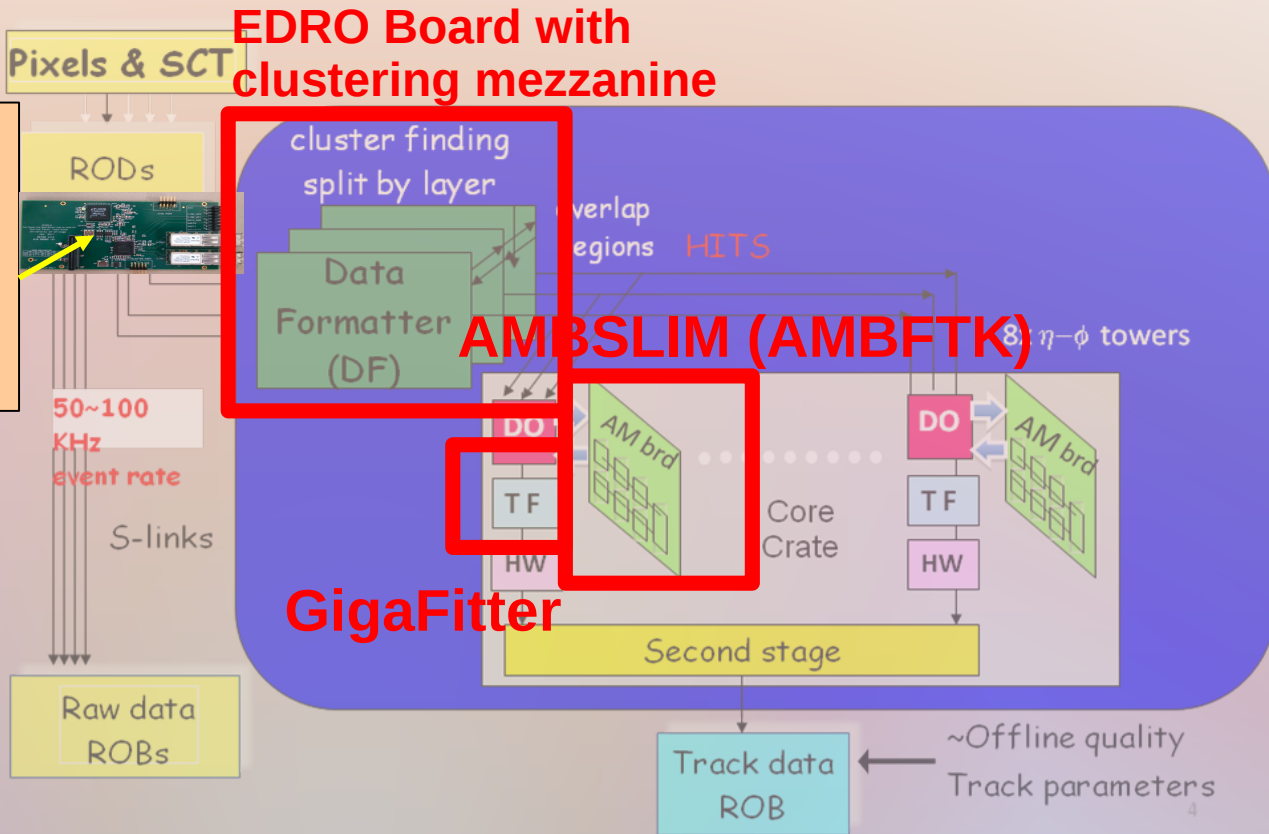
2

EDRO+AM(+GF) "baby FTK"

Data from a small projective slice of silicon detector.

Dual Port HOLA (silicon detector front-end)
Flow Control (XON/XOFF) on second port disabled → parasitic with respect to the ATLAS data flow.

Start <u>early development</u> of **software** and **firmware** on existing boards and prototypes.
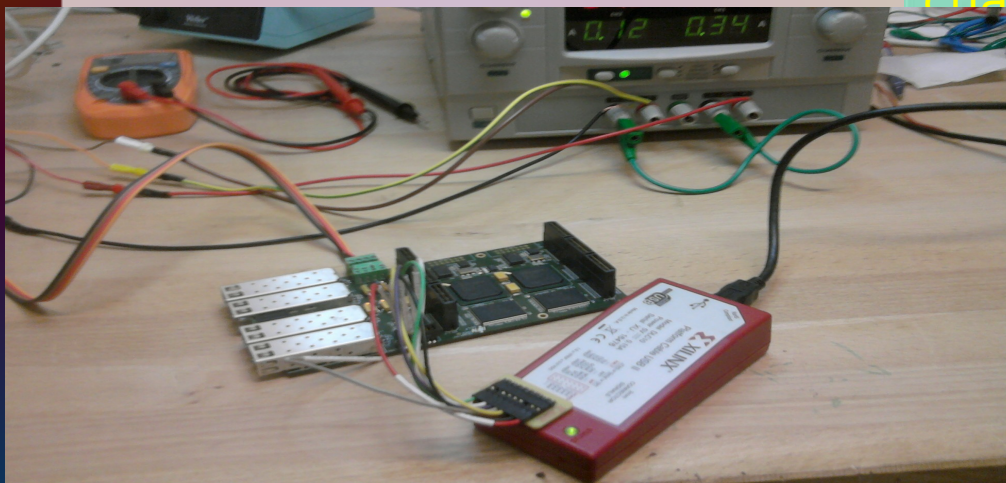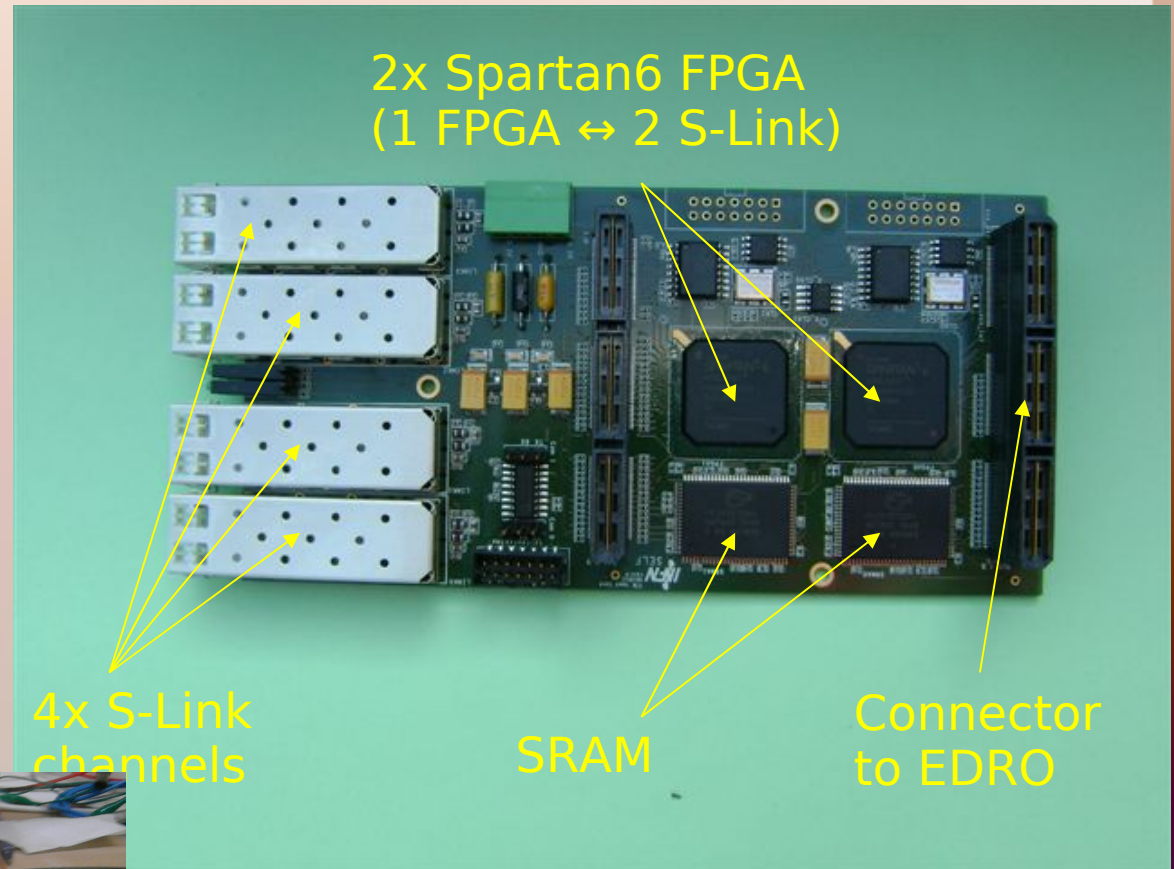
EDRO Board with clustering mezzanine

AMBSLIM (AMBFTK)

GigaFitter

Pixels & SCT

RODs

cluster finding
split by layer

overlap regions

HITS

Data Formatter (DF)

50~100 KHz event rate

S-links

DO

AM brd

TF

HW

DO

AM brd

TF

HW

8 η−φ towers

Core Crate

Raw data ROBs

Second stage

Track data ROB

~Offline quality Track parameters

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EDRO Board with **clustering mezzanine + AMBSLIM** (+ GigaFitter)

This setup is also the **environment for testing** future prototypes and production boards.

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Clustering Mezzanine

- Features
  - Receives up to 4 S-Link inputs
  - 2D clustering for pixels
    - Allows to correct with Time over Threshold information (TBC)
  - 1D association of contiguous SCT clusters from ABCD
  - Sustains input data rate of 40MHz S-Link words
 - Sends clusterized data out over 1 or more channels to mainboard (EDRO, DF)

2x Spartan6 FPGA
(1 FPGA ↔ 2 S-Link)

4x S-Link channels

SRAM

Connector to EDRO

First prototype just arrived (may 2011). Connection to EDRO tested.

Conceptual 2D pixel clustering firmware developed. Porting to mezzanine FPGAs ongoing.

EDRO Board

General purpose DAQ board:

- **S-Link** connection to DAQ PCs

- **Two mezzanine slots** for inputs from front-end. *FTK clustering mezzanine* is compatible with this slot.

- **Large FPGA** (Stratix II) for local computation

- EDRO to EDRO connection to build complex DAQ systems (not used in this application)

- **Backplane direct connection to AM Board**

Clustering mezzanine

Clustering mezzanine

6 output buses
1 input bus
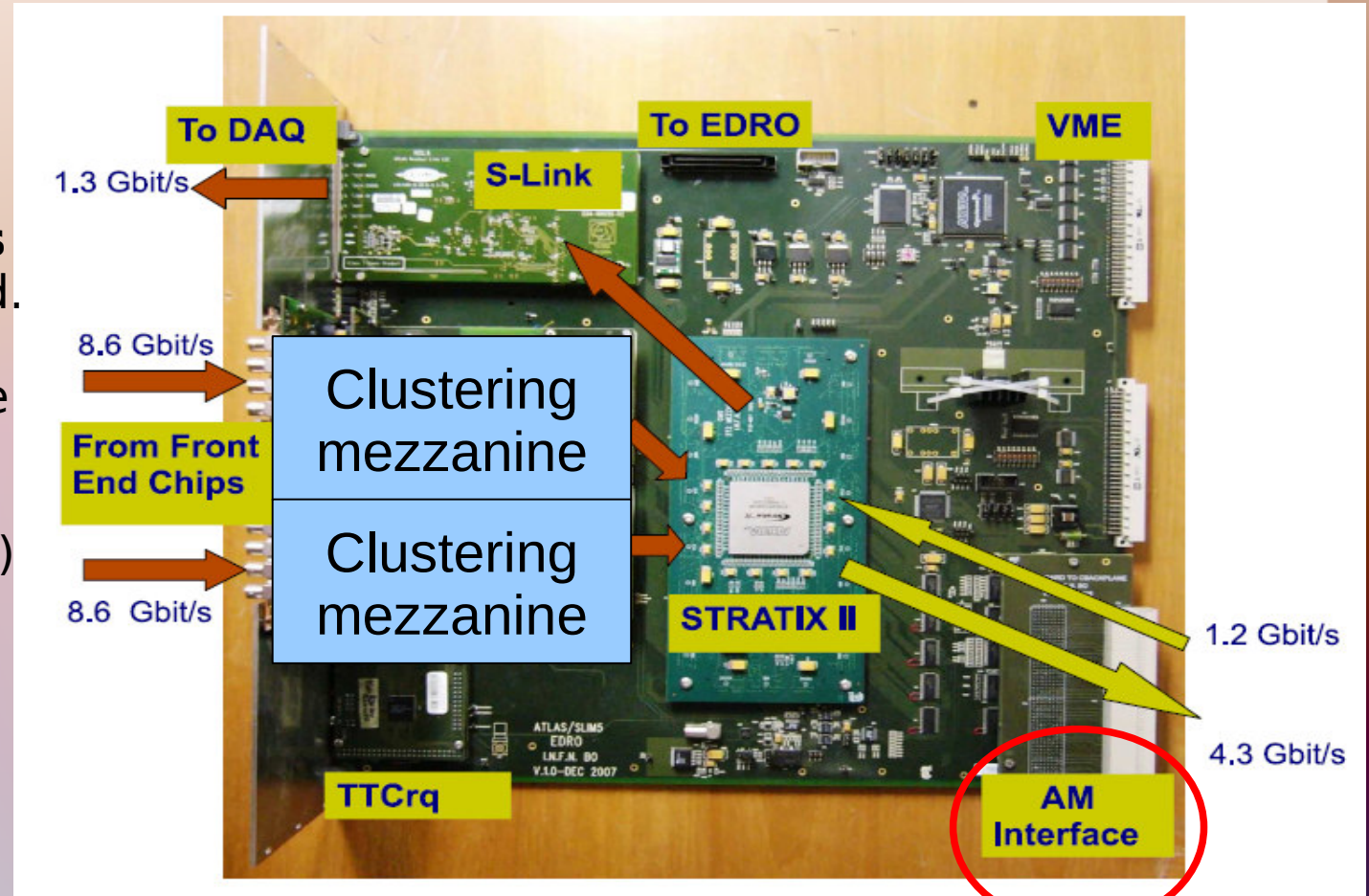
Used for data acquisition in:
ATLAS Lucid
SLIM5 (silicon detectors r&d project)

Associative memory board: AMBSLIM

New generation AM Board developed for SLIM5 and FTK:

- supports 4x CDF LAMB mezzanines (each up to 32 AMchip03) for a maximum capacity of 640k patterns (**320k** using CDF's single-sided LAMBs)

- **6 input buses**
- 1 output bus (roads)
- 6 output buses (hits, for pipelined AMBoards)

- Backplane connection to EDRO Board

Standard cell chip

AMchip03

~5000 patt/chip

CDF LAMB

Control FPGA

Input FIFOs

40 MHz clock

P3 serial LVDS

AMBSLIM
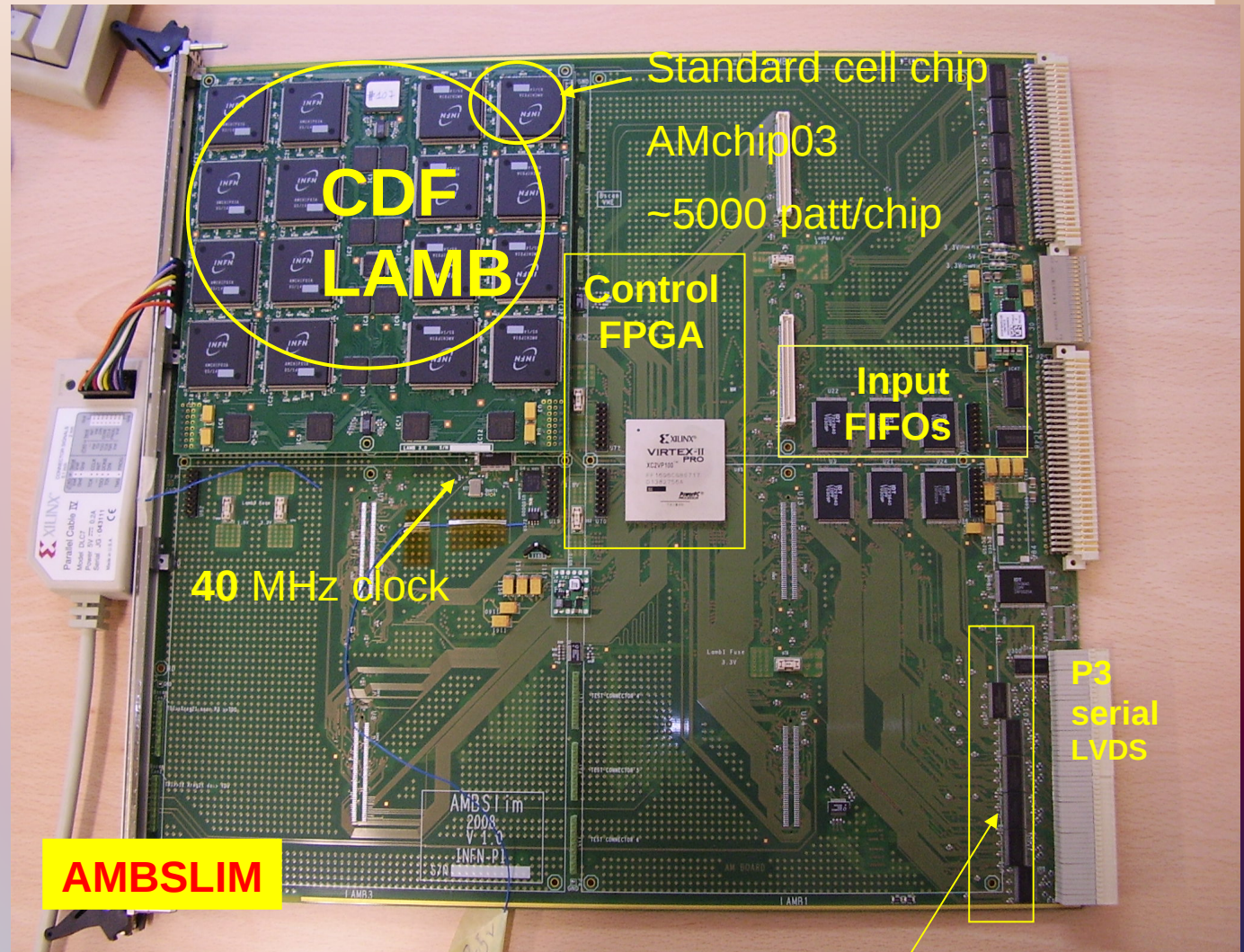
Hits from EDRO
Roads from AM pipeline to EDRO

AM full custom chip

Technology: TSMC 65nm Low Power

Mini Asic Prototype: 2^13 = 8192 pattern
(8 detector layer x 15 bit word)

Chip Area: 13mm^2

Memory core: Full custom design

Control logic: Standard Cell design

Mixed Current Race and Selective Precharge power saving techniques.

Each 15 bits memory word has 3 don't care bits this allow to store more tracks for each memory pattern.
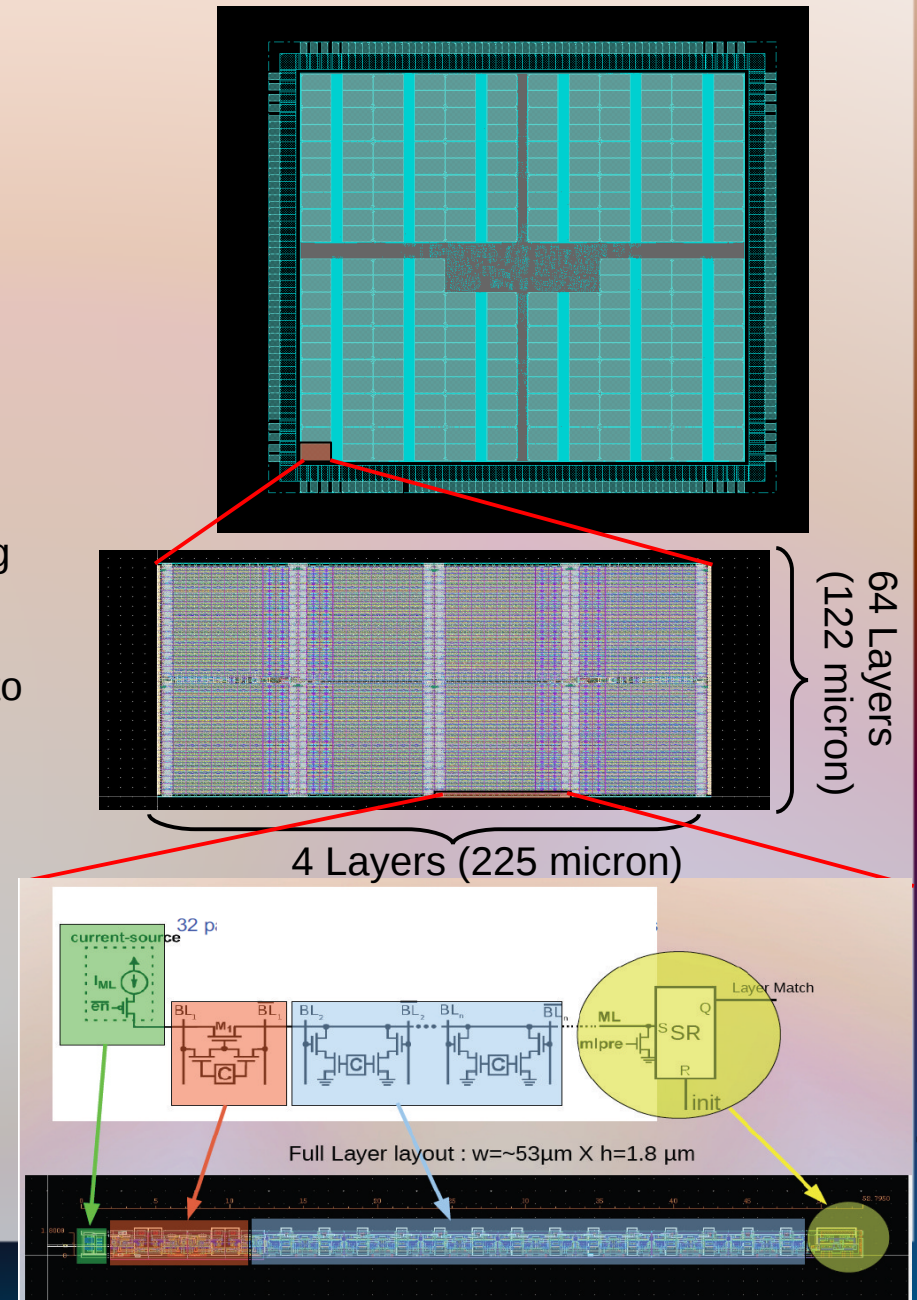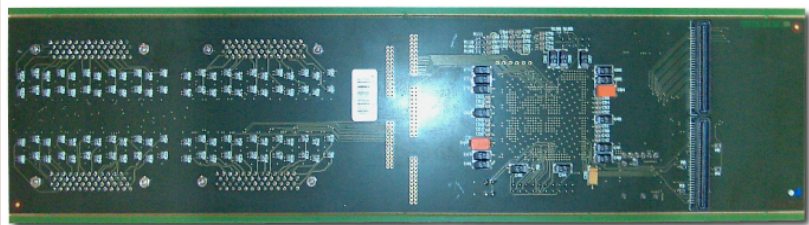
Goal working frequency: 100 MHz

Old CDF chip:

Technology: 180 nm (standard cell design)
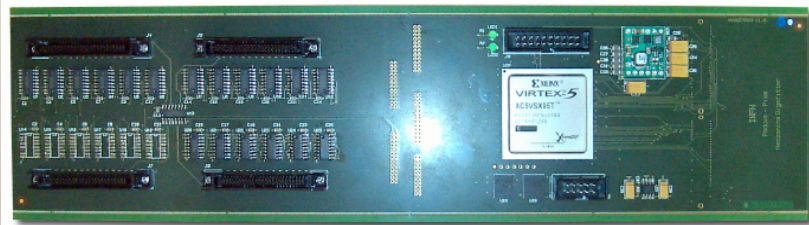
Area: 100 mm^2 (5120 pattern)

Working Frequency: 50 MHz

64 Layers
(122 micron)

4 Layers (225 micron)

32 pa
current-source

Layer Match

Full Layer layout : w=~53μm X h=1.8 μm

GigaFitter

(a) Back view of the mezzanine

(b) Front view of the mezzanine

Mezzanine for Pulsar Board (CDF/Magic experiments) with a powerful Virtex-5 FPGA.

Used in SVT (CDF) for the linear fit of all 12 phi slices in parallel
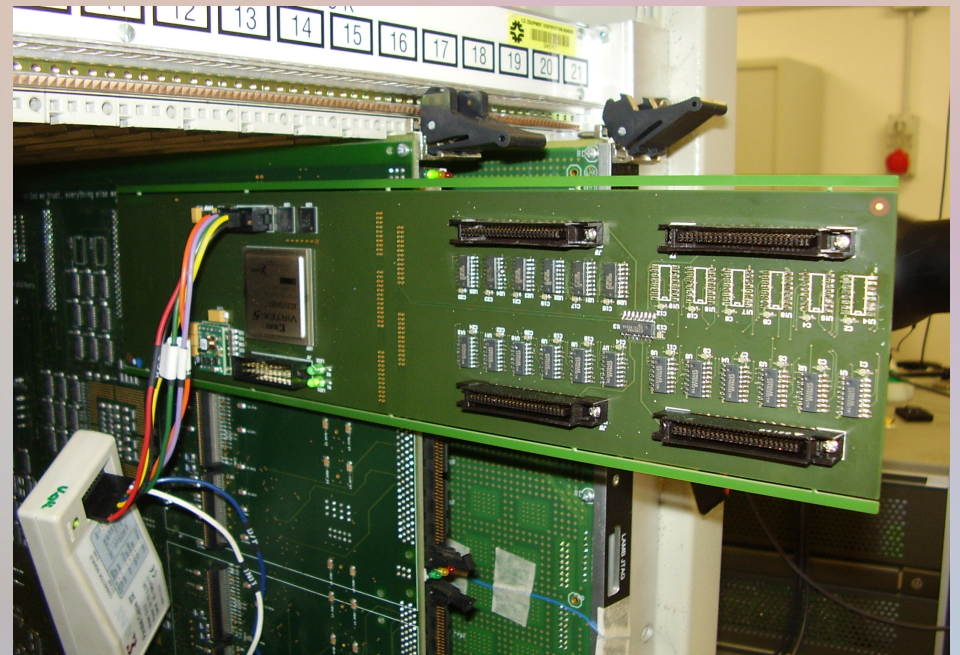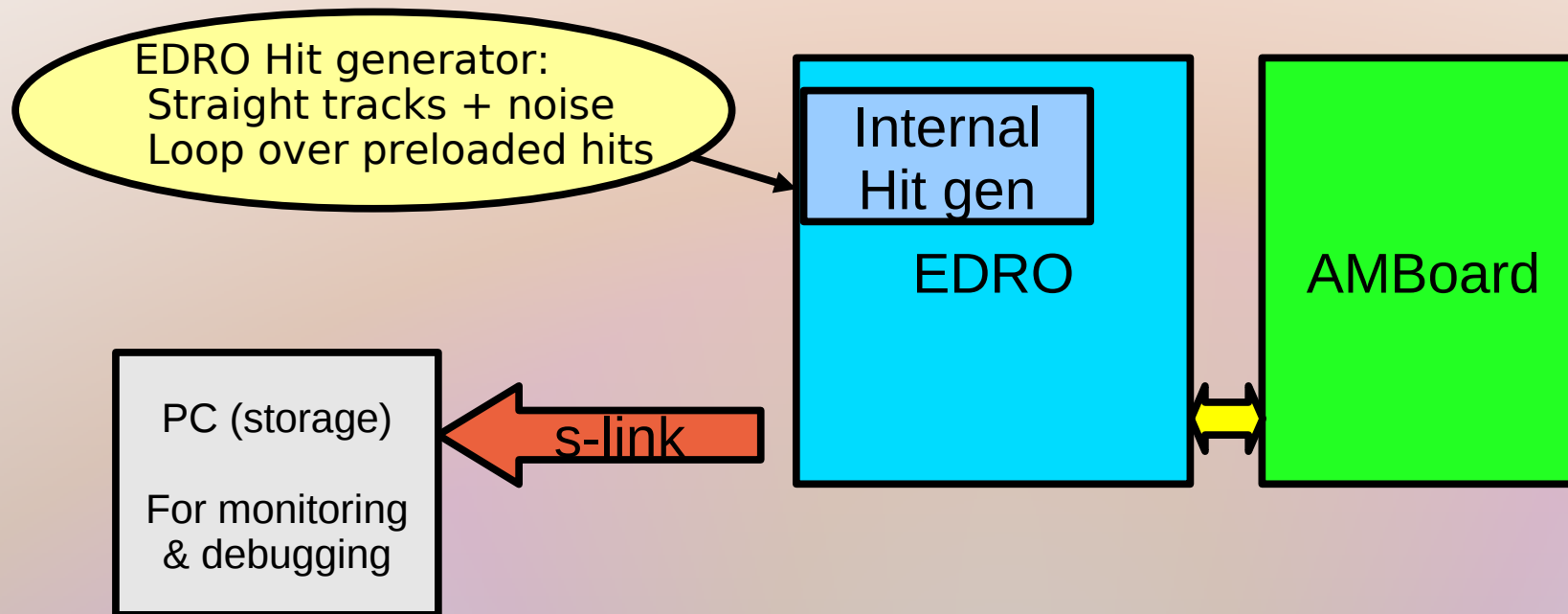
The Pulsar Board has S-Link connection and can receive Hits+Roads from the EDRO Board and perform the second stage of the FTK algorithm: linear fit of the track parameters

EDRO+AM basic setup

EDRO Hit generator:
 Straight tracks + noise
 Loop over preloaded hits

Internal Hit gen

EDRO

AMBoard

PC (storage)

For monitoring & debugging

s-link

Simple Test Setup: the EDRO board internally generates simple events, the AMBoard finds known patterns and sends the information back to the EDRO board.

The EDRO board can trigger on hit multiplicity or AM roads:
 Test EDRO ↔ AM connection and stability
 Test AM vs AMsim over many events

EDRO+AM setup
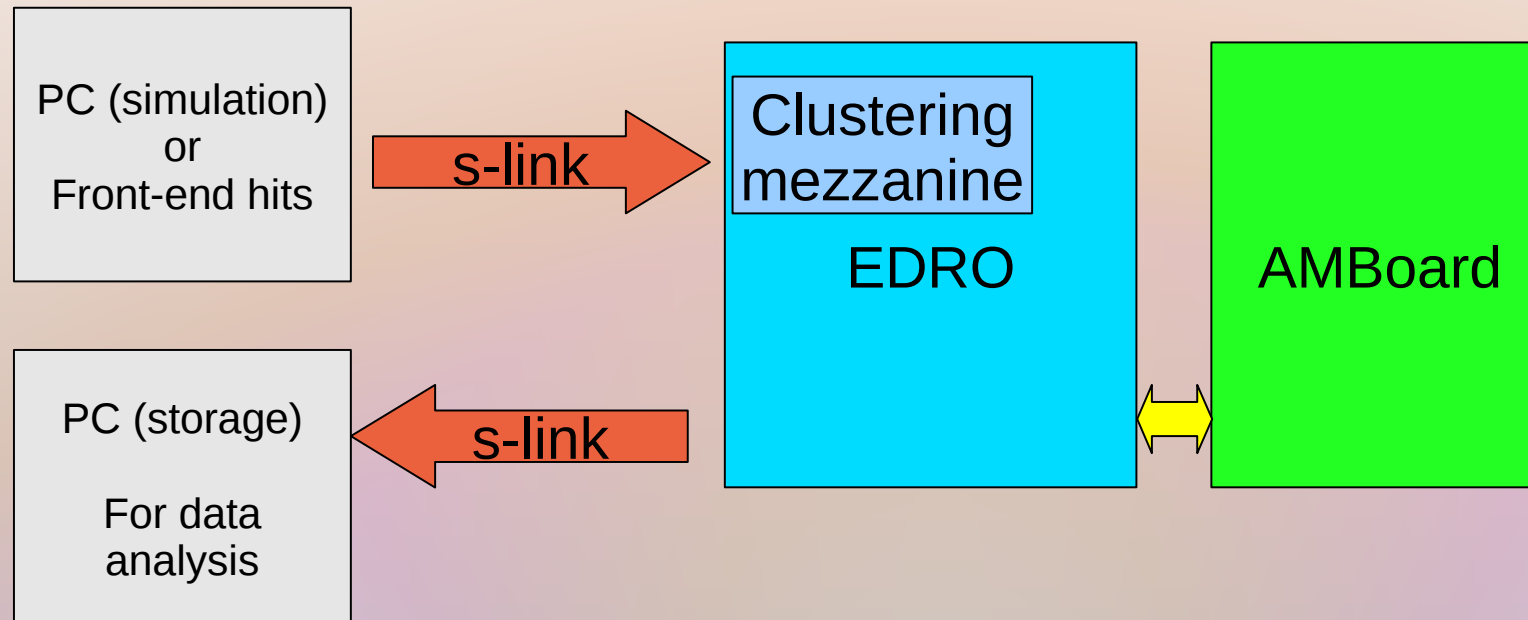
FTK Stage 1 Setup: hits from PC simulation or real front-end are received by the Clustering mezzanine. Clustered hits are sent by the EDRO board to the AMBoard, the AMBoard finds patterns (roads) and sends them back to the EDRO.

- **Pattern bank efficiency** studies
- **Algorithm studies** → lepton isolation in a small projective tower
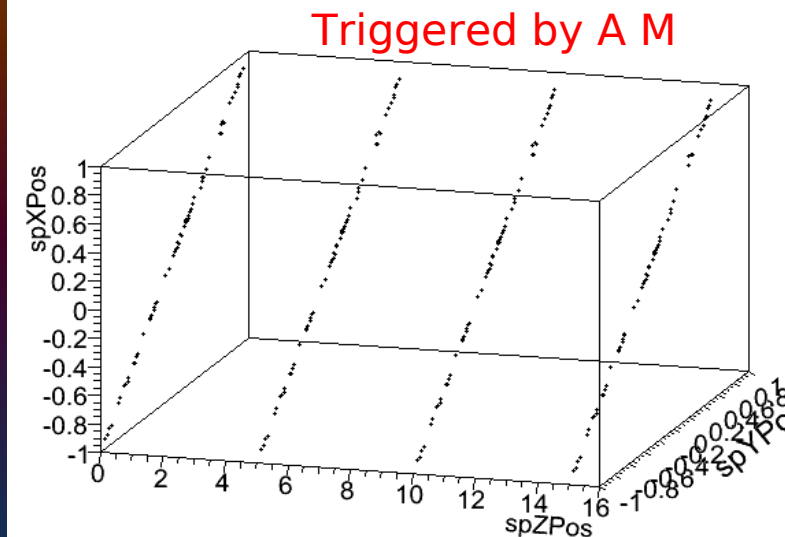
First tests in INFN Bologna

EDRO+AM Basic Setup
has been tested in INFN Bologna

Events with 1-5 internally generated patterns+noise per event were sent @40MHz to the AMBoard to test board's connection, firmware and control software.
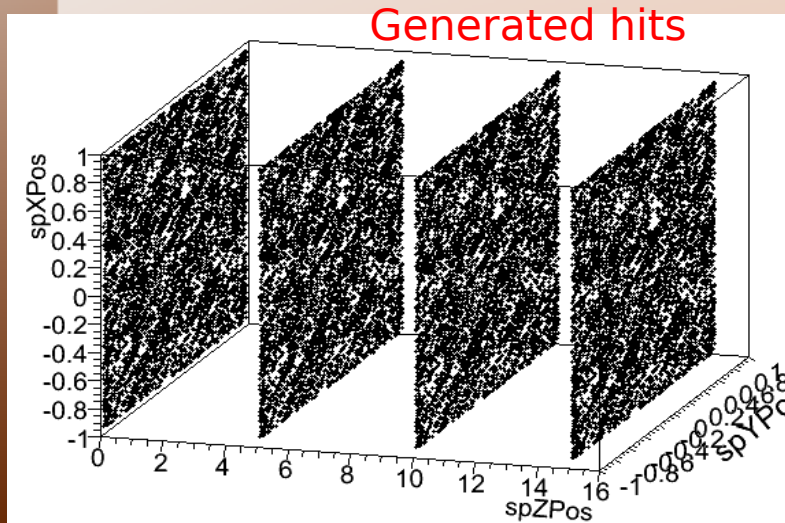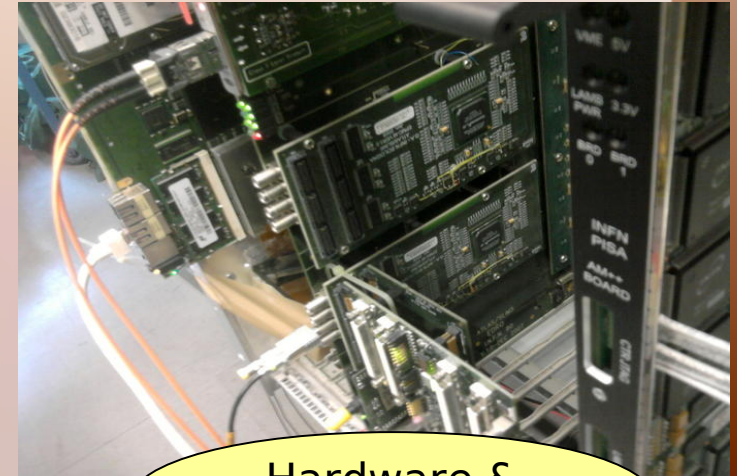
Generated hits

Straight tracks in a telescope-like configuration.

Plot hit position on 4 planes

Triggered by A M
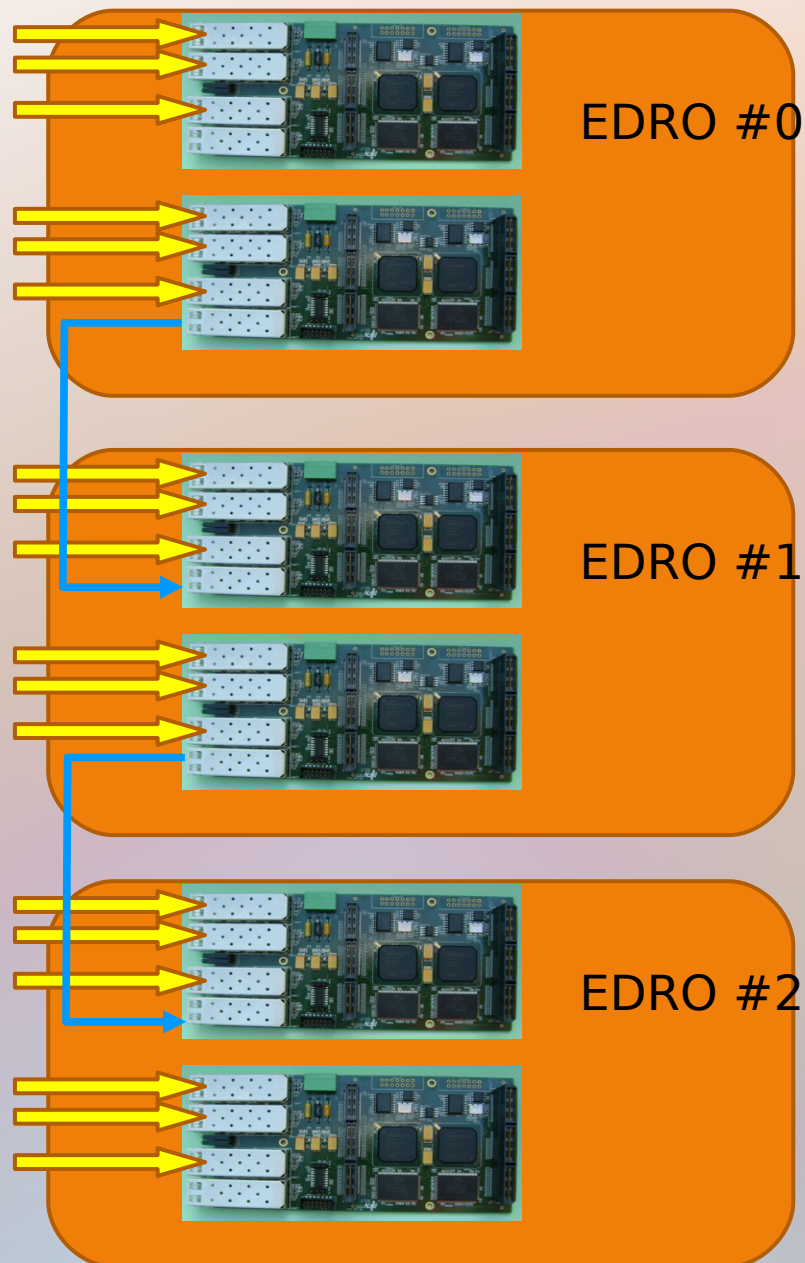
Pattern bank was generated including only tracks on the diagonal.

AM trigger selects only those tracks

Hardware & Software integration

Expanding the System

EDRO #0

EDRO #1

EDRO #2

3 EDROs, with 2 mezzanine each.
Plan to use up to 18 input S-links to receive
pixel and SCT data from a detector tower
about 1x1 $\Delta\phi \times \Delta\eta$

Each EDRO connected to 1 AM board
0.6M pattern / AM board
Total 1.9M patterns.

This configuration workable up to about 23 pileup interactions / bunch crossing.

Some links are used to exchange overlap data between the EDRO cards → needed to reconstruct tracks crossing a subregion boundary.

RoadMap to data taking in 2012

- Complete crate installation and debug (EDRO+Clustering mezzanine+AMBoard)

- Move EDRO+AM crate to a test stand at CERN by end of 2011

- Install some dual port HOLAs in silicon detector RODs (next winter stop)

- Start parasitic data taking and study in 2012

  - Add track fitting functionality using CDF GigaFitter board

  - When more prototypes are ready (ie. AMBoard with 8 input buses and AMchip04) add them to the test stand

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Conclusions

- Tracking is an important tool for effective online data selection at hadron colliders

- FTK is a complex hardware processor to enable full track reconstruction with offline quality in the ATLAS Level 2 trigger

- EDRO+AM crate with all FTK functions for early testing of the algorithm and first prototypes in the ATLAS environment

  - It will reconstruct tracks in a small projective slice of the detector

  - It will use existing prototype boards from past experiments and R&D efforts

  - Our goal is to take real data (in parasitic mode) by 2012 and test with the acquired data the real efficiency of some of our track-based algorithms (lepton isolation)

Backup

Dual HOLA (UChicago)

2nd output
1st output
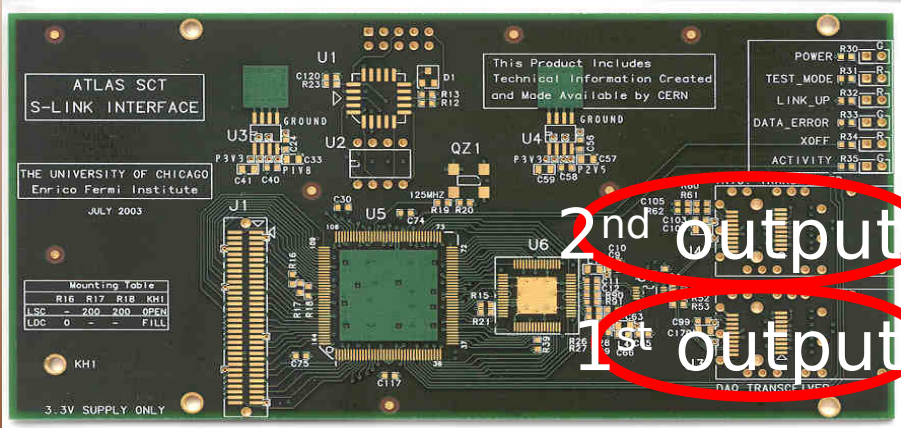
Developed by University of Chicago

Backward compatible with old HOLA

Two outputs with flow control XON/XOFF

Possibility to disable flow control on each outputs

One output to normal silicon detectors RODs, no need to change anything in the rest of infrastructure.

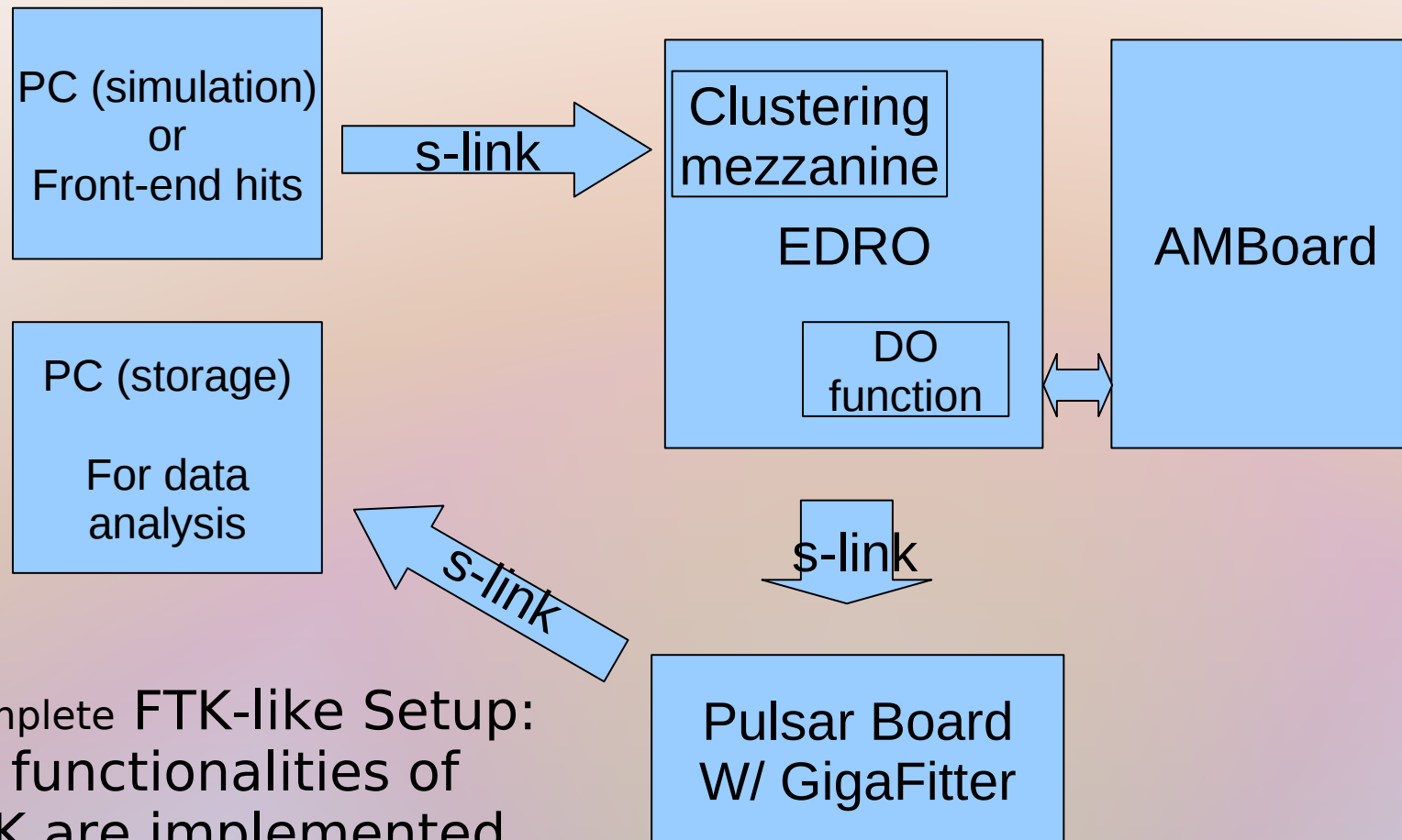One output to FTK. With flow control disabled we could be parasitic during installation/developing. After the system is fully installed and ... enabling flow

First prototype

EDRO+AM+GF setup

PC (simulation) or Front-end hits

s-link →

Clustering mezzanine

EDRO

DO function

AMBoard

PC (storage)

For data analysis

↖ *s-link*

↓ s-link

Pulsar Board W/ GigaFitter

Complete FTK-like Setup: All functionalities of FTK are implemented, the EDRO send hits+roads to the GigaFitter for the 2nd stage of the FTK algortihm.