UPGRADE OF THE PROTON COMPUTED TOMOGRAPHY SYSTEM OF THE PRIMA PROJECT

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Outline

- Introduction: proton therapy and proton imaging
- Proton imaging apparatus
- Proton Radiographies at 60MeV
- Upgrade of apparatus
Proton therapy

The proton therapy is a good clinical treatment for cancer as it permits to obtain a dose distribution extremely conformed to the target volume.

The protons with penetration depth have a well-defined dose maximum (Bragg peak) that follows a relatively low entrance dose region. Beyond the Bragg peak the dose fall-off is very steep (from 90% to 20% of the peak dose within a few millimeters)

Through the weighted superposition of proton beams of different energies it is possible to deposit a homogenous dose in the target region using only a single proton beam direction. (Spread Out Bragg Peak - SOBP).
Proton Computed Tomography: why?

In proton therapy treatments it is important to know:

**Patient positioning:**
Currently performed using X-rays radiography and tomography in a previous phase

\[ pCT \rightarrow \text{allows better accuracy and single phase positioning / treatments} \]

**Dose Calculation:**
Currently performed using X-rays computed tomography

\[ pCT \rightarrow \text{uses protons directly for dose calculation} \]

The error intrinsic in this conversion (due to \( \mu(\eta_e, Z) \) dependency on atomic number and electron density) is the principal cause of proton range indetermination (3%, up to 10 mm in the head)

[Schneider U. (1994), Med Phys. 22, 353]
THE “PRoton IMAging PROJECT”
pCR apparatus oriented to pCT

PROGRAM

- Manufacture a high-performance prototype for proton radiography.
- Develop suitable imaging algorithms:
  - analysis of data;
  - MC simulations.
- Validate the pCR system with pre-clinical studies
- Conceive a configuration for a pCT system:
  - Hardware and data acquisition;
  - Reconstruction algorithms (ART, SART...).

Cfr
V. Sipala et al., Nucl. Instr. and Meth. A 612 (2010) 566–570
C. Talamonti et al., Nucl. Instr. and Meth. A. 612 (2010) 571
Parameters of pCT

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proton beam energy</td>
<td>250-270 MeV</td>
</tr>
<tr>
<td>Proton beam rate</td>
<td>1 MHz</td>
</tr>
<tr>
<td>Spatial resolution</td>
<td>&lt; 1 mm</td>
</tr>
<tr>
<td>Electronic density resolution</td>
<td>&lt; 1%</td>
</tr>
<tr>
<td>Detector radiation hardness</td>
<td>&gt; 1000 Gy</td>
</tr>
<tr>
<td>Dose per scan</td>
<td>&lt; 5 cGy</td>
</tr>
</tbody>
</table>

**Problem:** protons, because the multiple Coulomb scattering, don’t move in straight line.
Single particle tracking and Most Likely Path reconstruction

- A: Only entry position & direction known: straight line L
- B: Entry position & direction + exit position known: straight line L’
- C: Entry position & direction + exit position & direction known: curved path L”, “banana-shaped”, narrow confidence limits

\[ \int_{L} \eta_e(\vec{r})d\vec{r} = K \int_{E_{in}}^{E_{out}} \frac{dE}{S(E)} \]
Concept

proton Computed Radiography

- Reveal the trace of the single proton using a silicon telescope
- Measure the residual energy of the proton using a calorimeter
- Reconstruct the most likely path of the single proton

proton Computed Tomography

- pCR for different projections with a rotating gantry
- Reconstruct the image
Schema of Proton Computed Radiography Device realized by the PRIMA(PRoton IMAging) collaboration
To achieve a read-out rate of 1 MHz a fully parallel digital strip readout system has been developed.

Eight 32-channel VLSI front-end chips acquire the detector signals and sends data in parallel to an FPGA (Xilinx Spartan-3AN) which performs zero suppression and moves data to a buffer memory (~5x10⁵ events).

An Ethernet commercial module is use both for data transfer to the central acquisition PC and to control the tracker module DAQ parameters.
Silicon strip detector

Manufactured by Hamamatsu Photonics

53x53 mm²

p+-on-n strips

256 ch, 200 µm pitch

200 µm thickness

(To reduce the multiple scattering in the detector planes while keeping a good sensitivity to protons)
VLSI front-end description

- AMS 0.35u CMOS Technology
- 1.6 mm x 6 mm
- 32 channels
- Power dissipation = 14.5 mW @ chan

Test performed at LNS with 60MeV proton beam
Calorimeter

- 4 YAG:Ce scintillating crystals
  Each crystal 30 x 30 mm² x 100mm
- 4 Photodiode 18 mm x 18 mm
- 4 commercial front-end
  *(Charge Sensitive Amplifier & shaper)*

<table>
<thead>
<tr>
<th><strong>YAG:Ce properties</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PHYSICAL PROPERTIES</strong></td>
</tr>
<tr>
<td>Density [g/cm³]</td>
</tr>
<tr>
<td>Hygroscopic</td>
</tr>
<tr>
<td>Chemical formula</td>
</tr>
<tr>
<td><strong>LUMINESCENCE PROPERTIES</strong></td>
</tr>
<tr>
<td>Wavelength of max. emission [nm]</td>
</tr>
<tr>
<td>Decay constant [ns]</td>
</tr>
<tr>
<td>Photon yield at 300k [10³ Ph/MeV]</td>
</tr>
</tbody>
</table>

Charge spectrum @100MeV
Complete pCR apparatus

Test at LNS
(May 2010-May 2011)

- Alignment test
- Radiography test
- Tomography test
Complete pCR apparatus - Test at LNS (13May 2010)

Experimental setup

DATA ANALYSIS PROCEDURE
• MLP reconstruction
• Back-projection of the data
• Phantom image

Phantom design
**Complete pCR apparatus - Test at LNS**

**Experimental setup**

**DATA ANALYSIS PROCEDURE**
- MLP reconstruction
- Back-projection of the data
- Phantom image

**Phantom image**
Test at LNS: Walnut radiography
First tomography setup

Design of the phantom

Data analysis is in progress
First tomography setup

Data analysis is in progress

Design of the phantom

Very preliminary
A system for proton radiography has been realized:
- Field of view of about $5\times5\text{cm}^2$
- Acquisition time of the order of 10 sec ($10\text{kHz}, 10^5$ events)

The complete apparatus has been tested with 60MeV proton beam at LNS.

Semi analytical reconstruction methods of the proton radiography has been developed and tested with data.

The tomographic data analysis is in progress.

**The PRIMA upgrade is defined**

**Future planes**

- Analysis of the tomography data and development of reconstruction algorithm
- New test of the apparatus at higher energy
- **Construction of pCT apparatus for clinical application**
PRIMA Upgrade

GOAL: pCT system for clinical applications.

- Larger active area
- On line data acquisition

→ Active area 5 x 20 cm² using the 5x5cm² detectors
→ New data acquisition system
Tracker module

**Back**

- **Y-Plane**
  - 4 detectors
  - 4 Front-end data blocks

**Front**

- **X-Plane**
  - 4 detectors
  - 2 Front-end data blocks

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Sensor A1
Sensor A2
Sensor A3
Sensor A4

Sensor B1
Sensor B2
Sensor B3
Sensor B4

Y1 Front-end
Y2 Front-end
Y3 Front-end
Y4 Front-end
Tracker module cross-section

- Detectors directly mounted on printed circuit board (PCB)
  *Glued on the central hole, on both sides, using a small support precisely machined*
- The sensor bias contact connected to the front face
- Electronics components mounted in both sides of PCB
Tracker module: front-end block

- VLSI front-end chips
  - 256 strip
  - 8
  - 32

- FPGA
- Spartan6 XC6SLX45(T) CSG484
- Serial IN
- Diff. Serial OUT
- Trigger
- clk diff.
- Flash for Spartan
- Jtag
- Max. speed 1.050 Gbps

Central Unit

RD11 6-8 July 2011, Florence, Italy
Front-end chip

• Starting of old chip:

  and of test results:  • Threshold value dispersion
  • Non-linearity response

New front-end chip characteristics
- 32 channels
- Each channel: Preamplifier + shaper CR-RC$^3$ + Comparator + DAC (8bit)
- New digital part for serial-parallel conversion and for chip and channel selection
DAQ of tracker: architecture

Tracker module → Tracker module → Tracker module → Tracker module → Tracker module

Serial links
6 x board

Status:
Evaluation board → acquired
Test of serial links → in progress
Calorimeter Upgrade

Calorimeter Layout

Single channel front-end

Sampling, data storage and transfer

NI 5751
32-Channel Digitizer Adapter Module for NDT Applications
- 16 simultaneous 50 MS/s, 14-bit channels
- 8 digital inputs
- 8 digital outputs
- Ability to synchronize multiple devices for high-channel-count applications

NI PXIe-7962R
NI FlexRIO FPGA Module for PXI Express
- DSP-focused Virtex-5 SX50T FPGA programmable with the LabVIEW FPGA Module
- 512 MB onboard DDR2 DRAM
- Access to 132 single-ended I/O lines, configurable as 66 differential pairs
- Customizable I/O with the NI FlexRIO Adapter Module Development Kit (MDK)
- 16 DMA channels for high-speed data streaming at more than 800 MB/s

NI PXIe-8102 RT
1.9 GHz Intel Celeron T3100 Dual Core With LabVIEW Real-Time
- Deployment platform for LabVIEW Real-Time and LabWindows™/CVI Real-Time applications
- Execution target for NI LabVIEW Real-Time Version 8.6.1 or later applications
- 1 GB (1 x 1 GB DIMM) 800 MHz DDR2 RAM standard, 2 GB maximum
- 1 GB/s maximum system and 250 MB/s maximum slot bandwidth
- Integrated hard-drive, USB, serial, Gigabit Ethernet, and other peripheral I/O

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32-Channel Digitizer Adapter Module for NDT Applications
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Calorimeter Upgrade

Calorimeter Layout

Single channel front-end

Sampling, data storage and transfer
Calorimeter Upgrade

NI 5751
16-Channel Digitizer Adapter Module for NDT Applications
- 16 simultaneous 50 MS/s, 14-bit channels
- 8 digital inputs
- 8 digital outputs
- Ability to synchronize multiple devices for high-channel-count applications

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• Sampling of 14 analog signals
• Output of trigger signal
• “Global Event Number”(GEN output

• Pre - elaboration data
• Trigger generator
• GEN generetor

• Data storage
• Data transfer
Thanks!!!
Spare slides
Stima del data rate

• Per ogni blocco di lettura (in parallelo con tutti gli altri)
  – Massimo numero di strip da trasferire: 16
  – Numero medio di strip da trasferire: 1.5
• Per ogni strip
  – 8 bit per address (0...255)
  – 6 bit per inizio segnale wrt trigger (-1.0...+0.2µs @ 50MHz sampling)
  – 6 bit per durata del segnale (0...1.2µs @ 50MHz sampling)
• Per ogni evento
  – Massimo (8+6+6) x 16 = 320 bit
  – Tipico (1/10 Massimo) = 32 bit
• Durata trasferimento su seriale @100Mbps
  – Massimo: 3.2µs
  – Tipico: 320 ns
Data building tracciatore

- Event size
  - Massimo: 320 bit x 6 blocchi x 4 schede → 1kByte
  - Tipico: 32 bit x 6 blocchi x 4 schede → ≈ 800 bit

- Data rate (1 MHz trigger)
  - Massimo: 1GByte/s
  - Tipico: 800 Mbps

- Image size (tipico)
  - 180 proiezioni @ 1x10^5 ev → 1.5 Gbyte + overhead
• PCI Express
• Gb Ethernet
• USB
• 160 + 68 User I/O (modulo espansione su FMC)

• DDR3 → 512 MB (fino a 2GB) @ 800Mbps
• Flash → 2GB