Irradiations on DEPFET-like test structures

10th International Conference on Large Scale Applications and Radiation Hardness of Semiconductor Detectors

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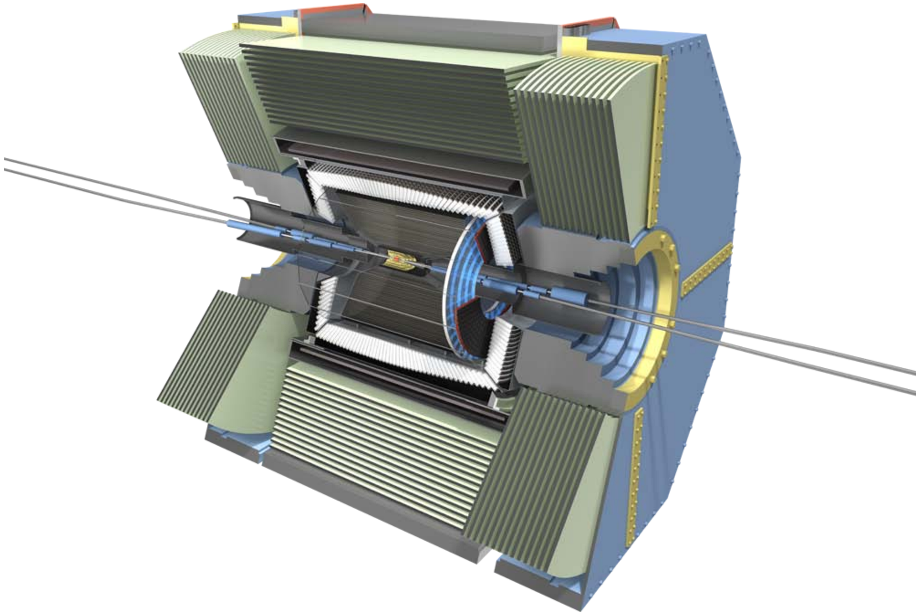
Outline

1. Motivation: DEPFETs for Belle 2 → pixel detector by B. Schwenker (next talk)
2. What is a DEPFET?
3. Ionizing radiation on MOS devices
4. Possible pixel layout → voltage cross sections
5. Threshold voltage shift dependance on gate voltage
6. Summary and Outlook

Motivation: DEPFETs for Belle 2



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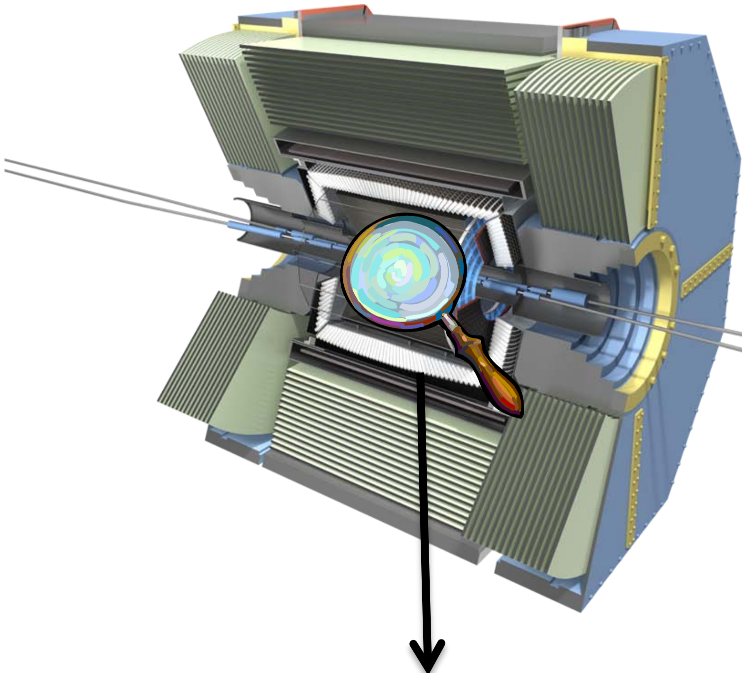
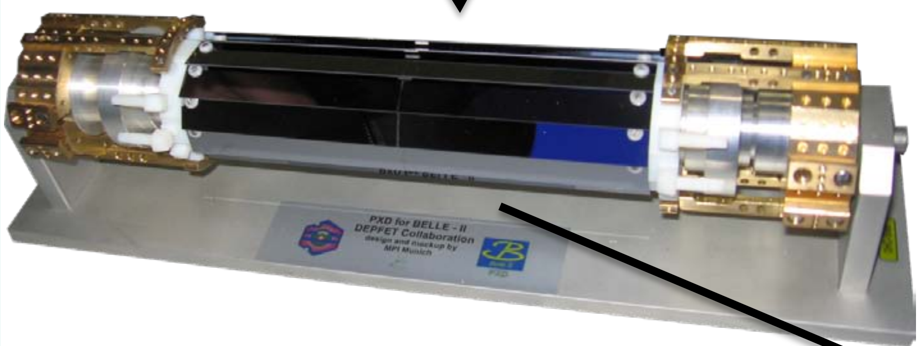


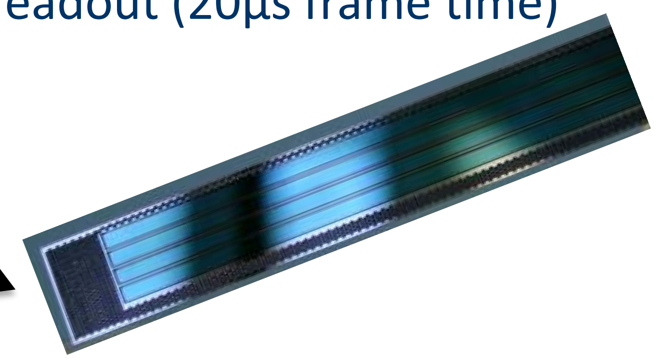


DEPFETs for Belle 2

- DEPFETs have a good SNR → thin sensors achievable (75 µm, avoids multiple scattering)

- Charge collection (next slides…) possible in „OFF“-state → low power dissipation → cooling via end flanges and airflow

- Bulk damage: ~10^{11} neq/(cm² * yr)
  - ~~type inversion~~
  - ~~chargeloss (trapping)~~
  - leakage current, shot noise → fast readout (20µs frame time)



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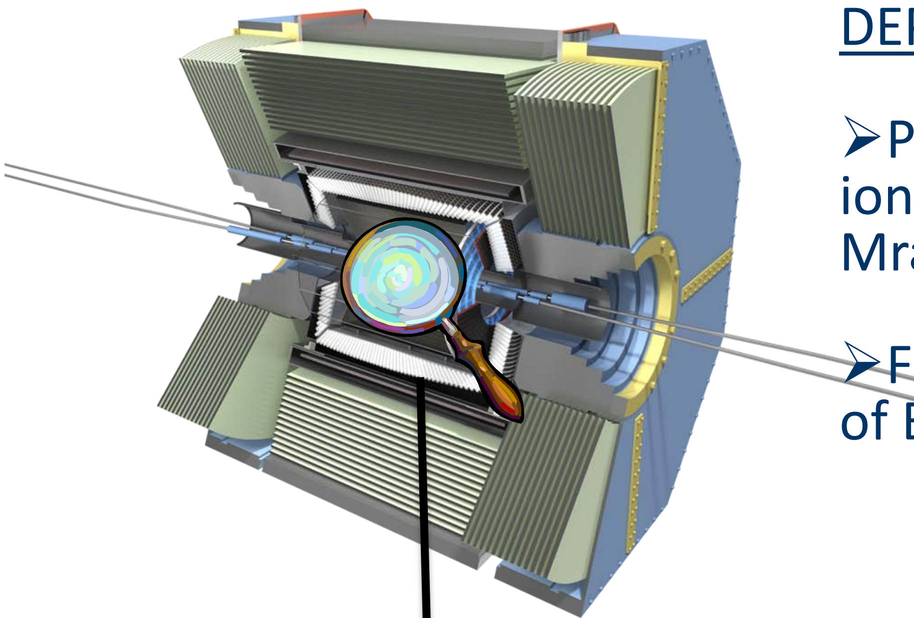
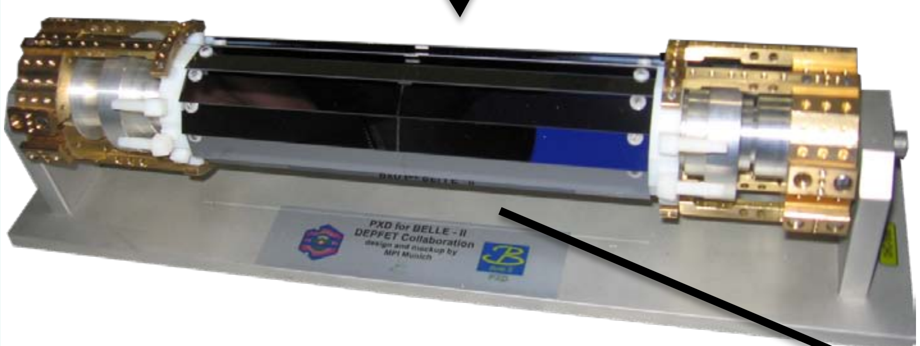
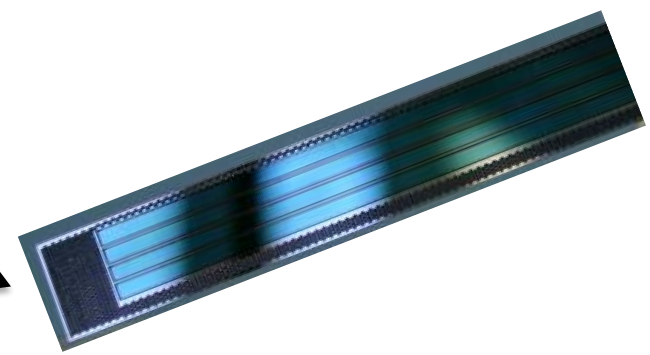


DEPFETs for Belle 2

- PXD (DEPFET matrix) suffers from ionizing radiation, estimated 1…2 Mrad/yr (10…20 kGy/yr)
- For detailed PXD discussion see talk of B. Schwenker





DEPFET WORKING PRINCIPLE

Working principle of a DEPFET

1. DEPFET = Depleted Field Effect Transistor

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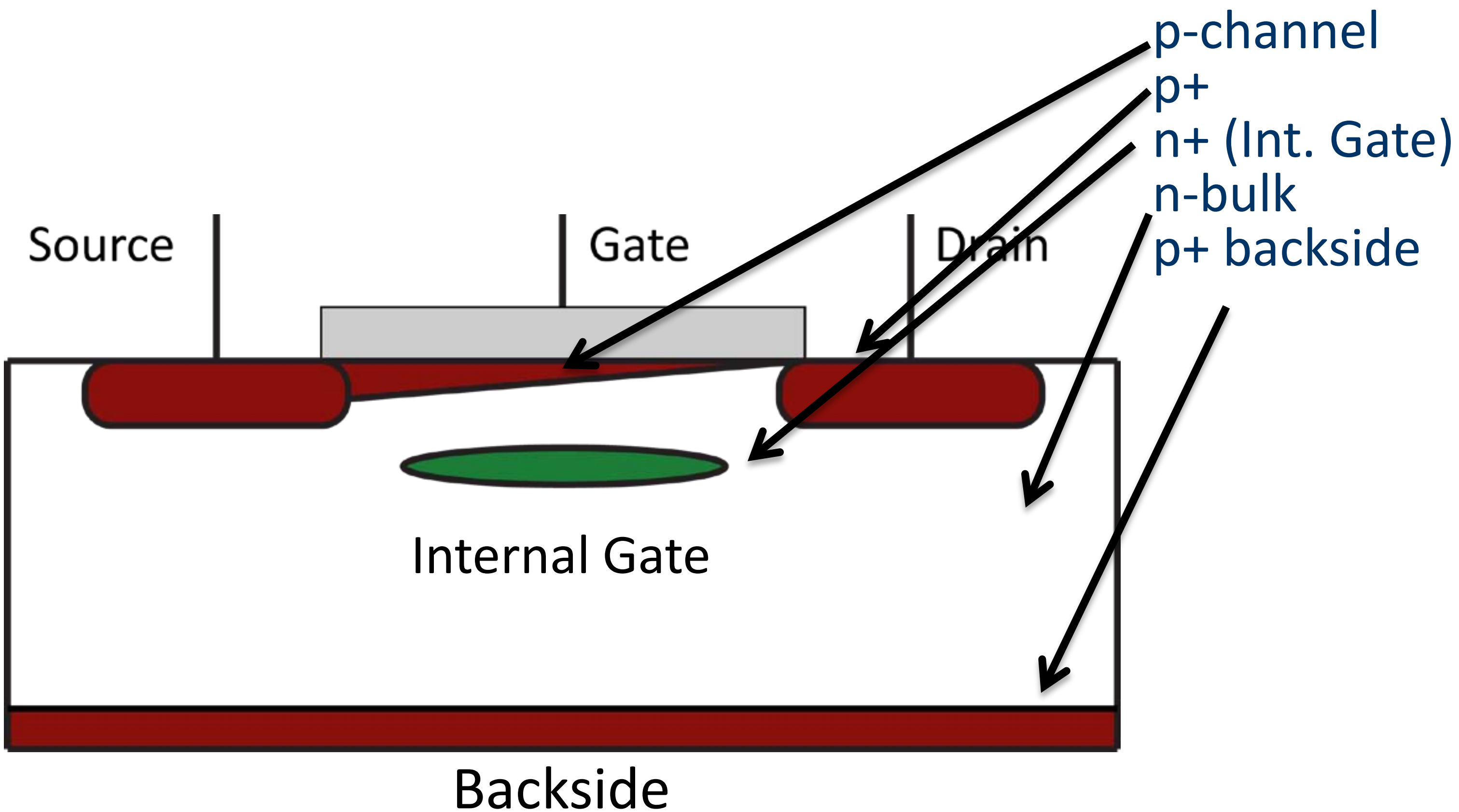
2. Consider a normal FET



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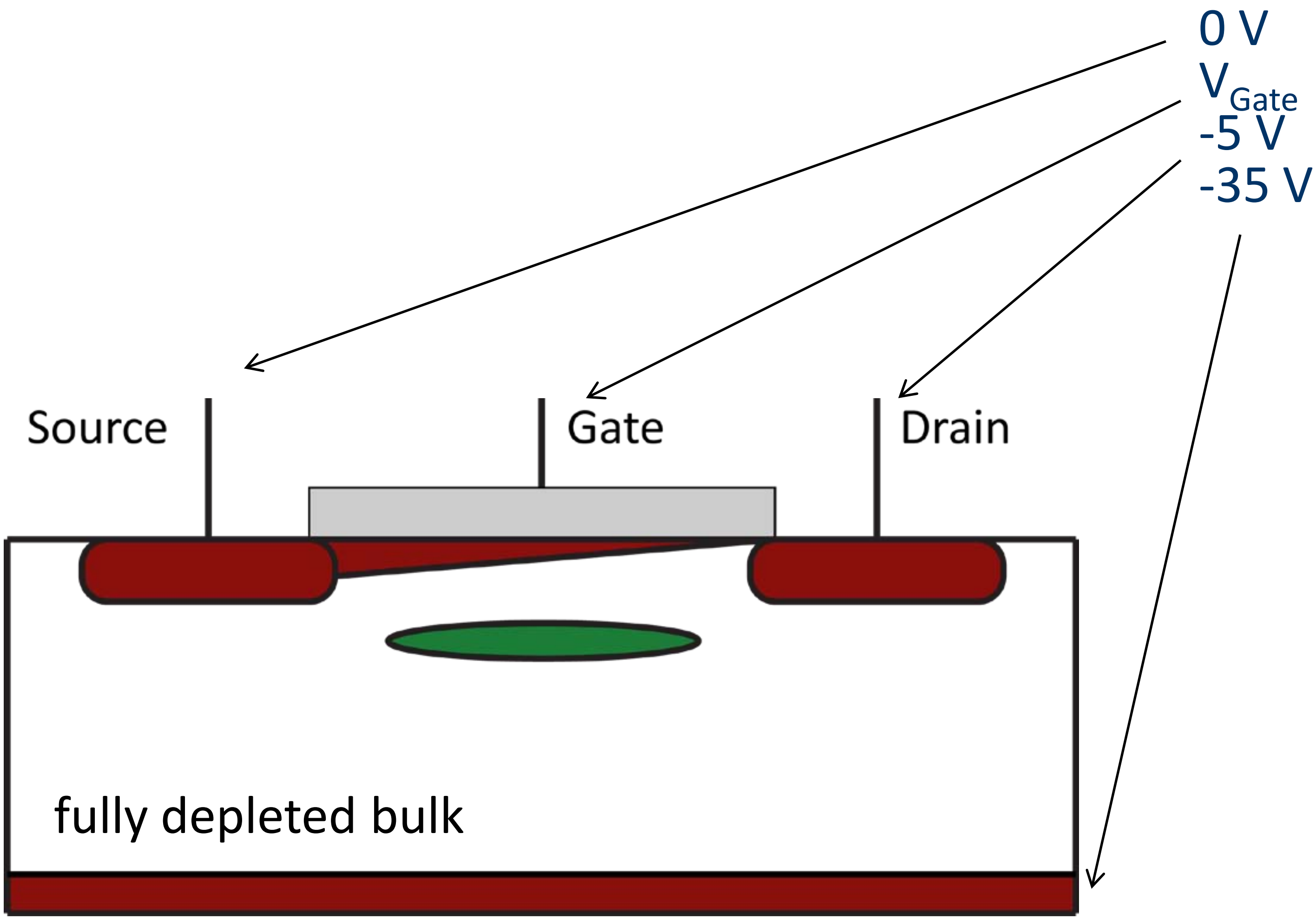
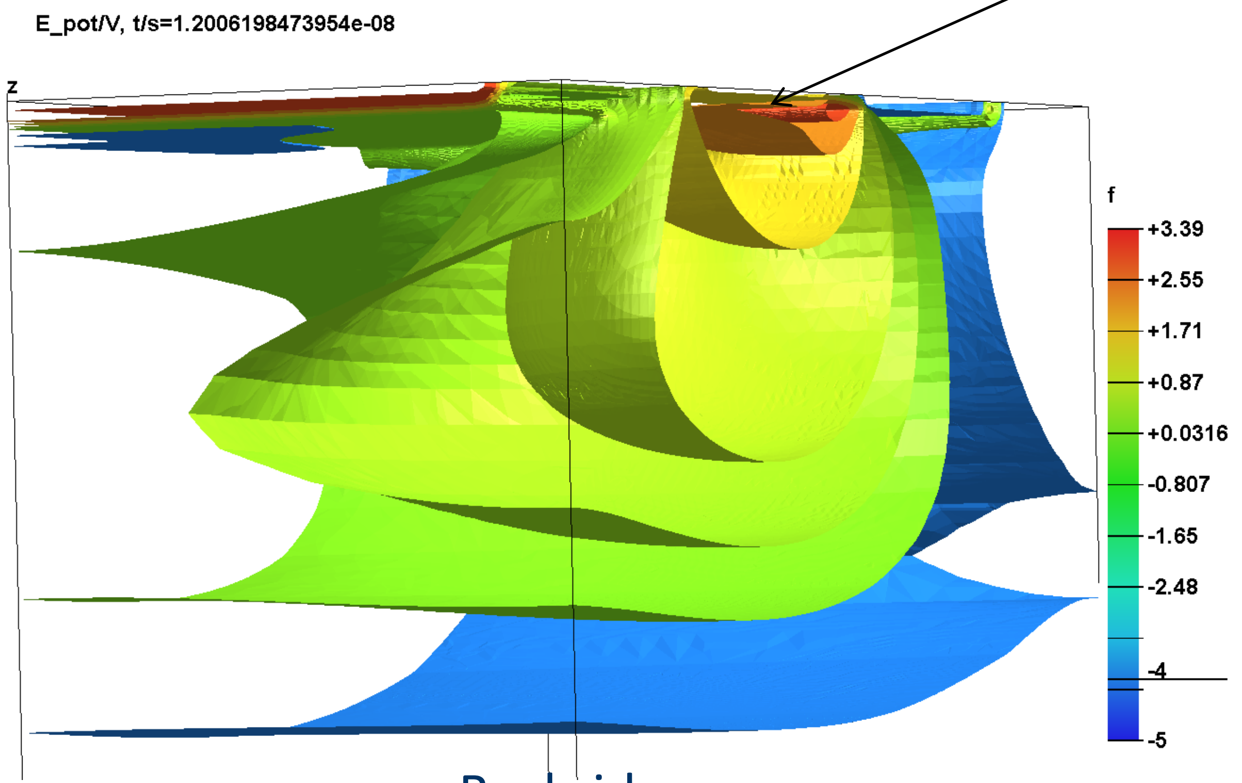


Working principle of a DEPFET

1. DEPFET = Depleted Field Effect Transistor
2. Consider a normal FET
3. Sidewards depletion – Equipotential planes

Internal Gate

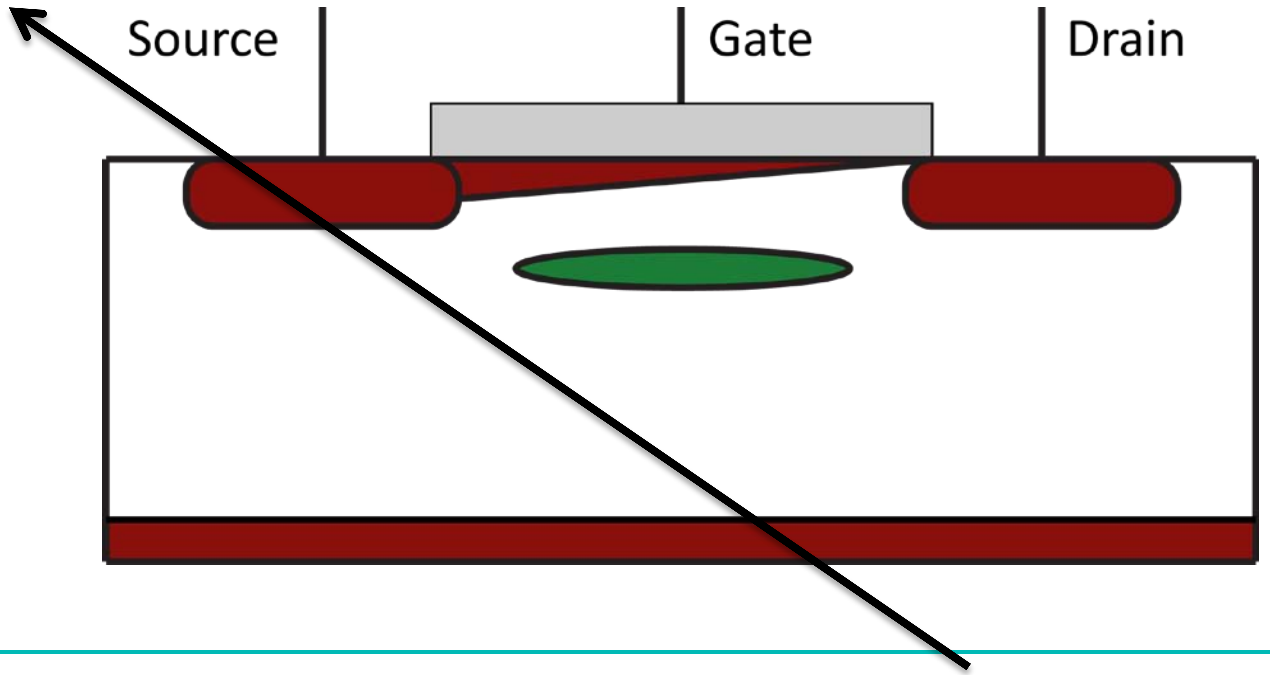


Performed by
K. Gärtner
WIAS Berlin

Backside

Working principle of a DEPFET

1. DEPFET = Depleted Field Effect Transistor
2. Consider a normal FET
3. Sidewards depletion
4. Charge creation and collecting



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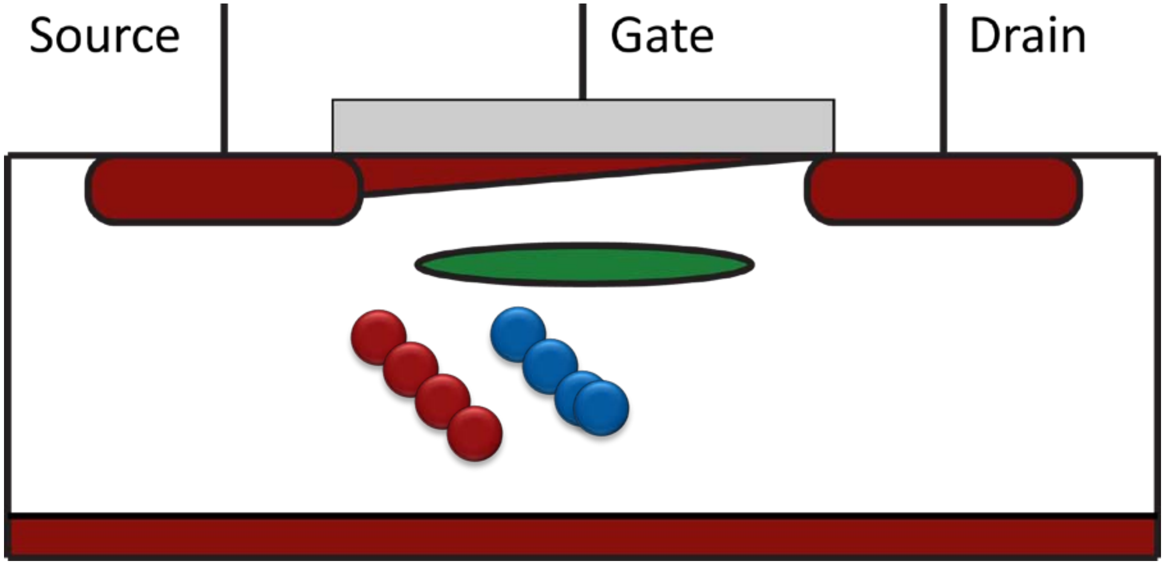

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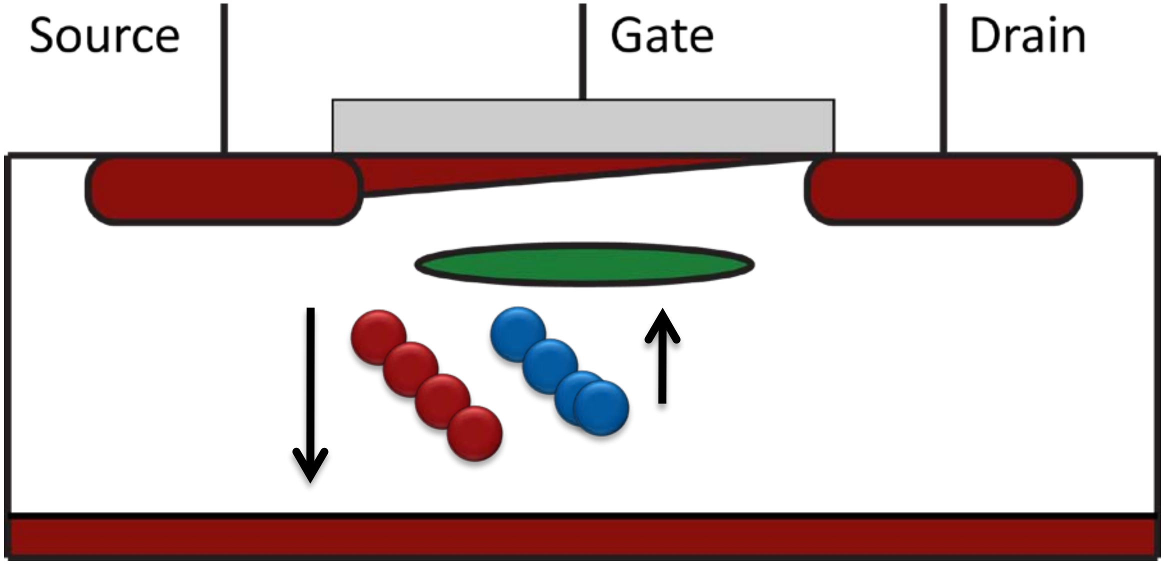

Working principle of a DEPFET

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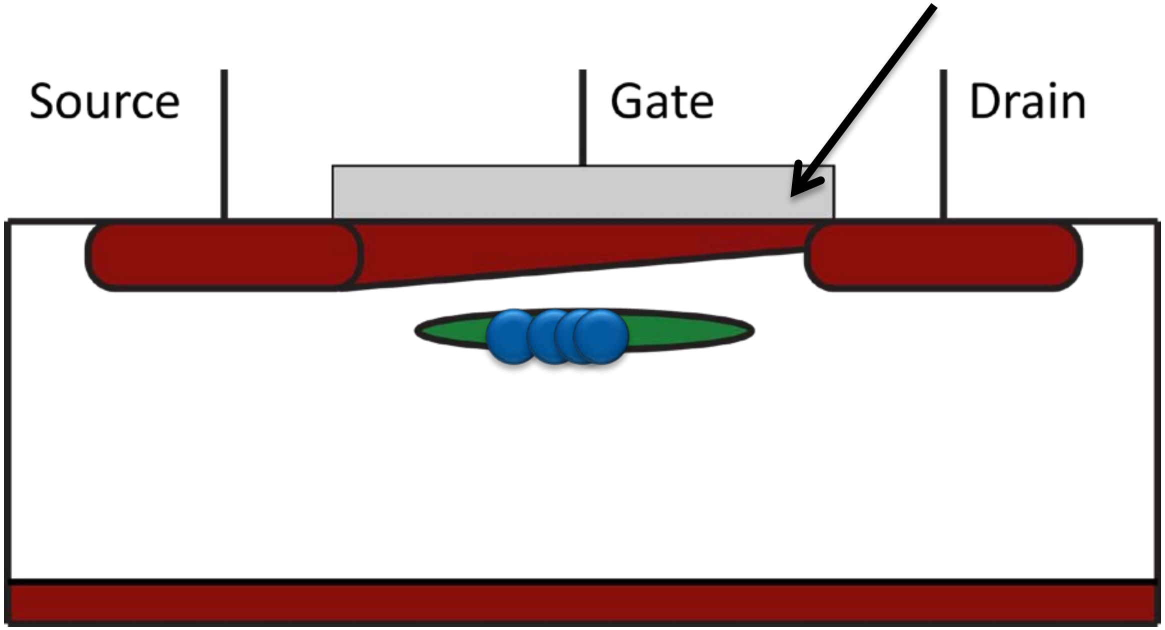
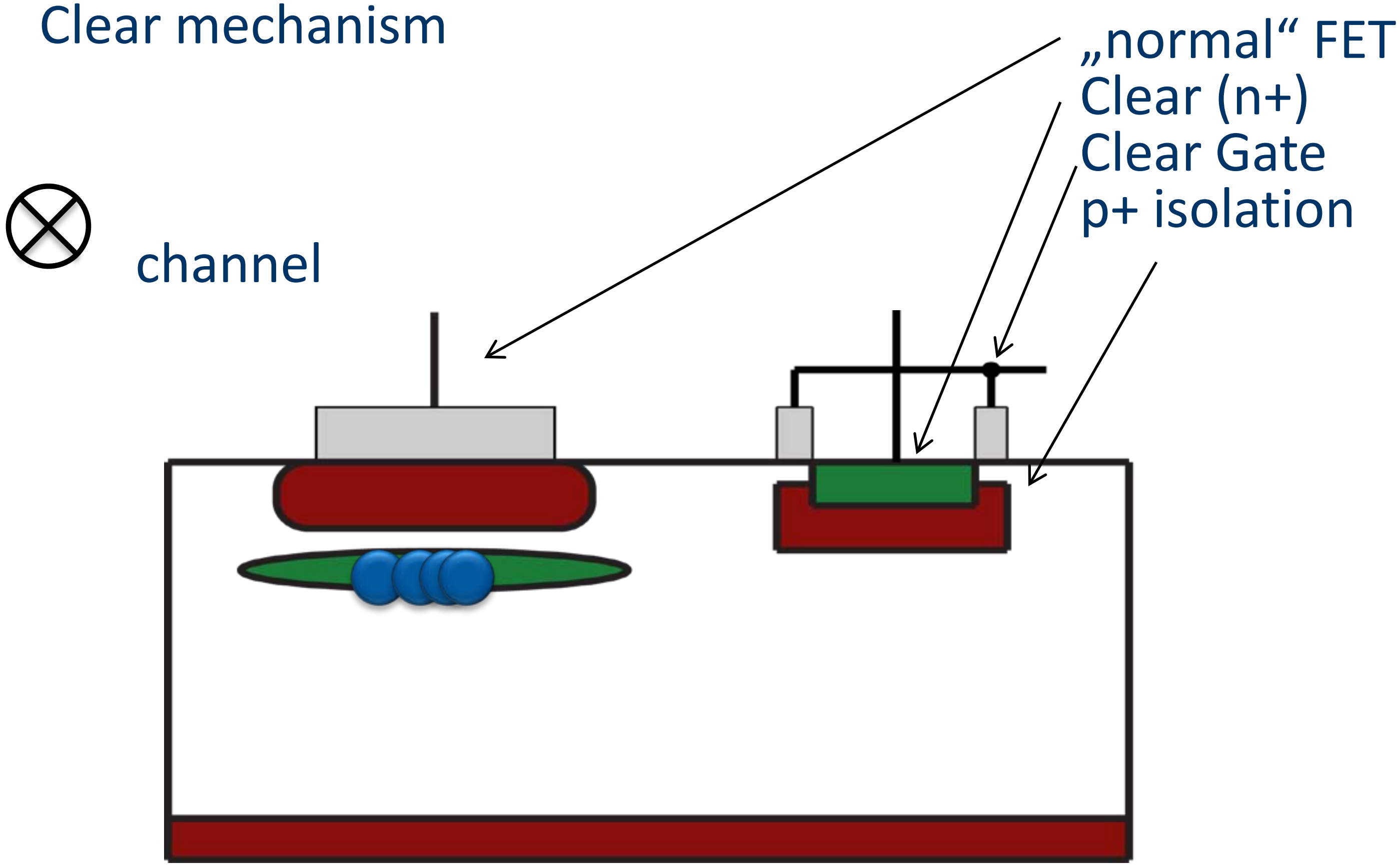
higher current via
mirror charges



Working principle of a DEPFET

1. DEPFET = Depleted Field Effect Transistor
2. Consider a normal FET
3. Sidewards depletion
4. Charge creation and collecting
5. Clear mechanism



Picture from side (90°rotated)

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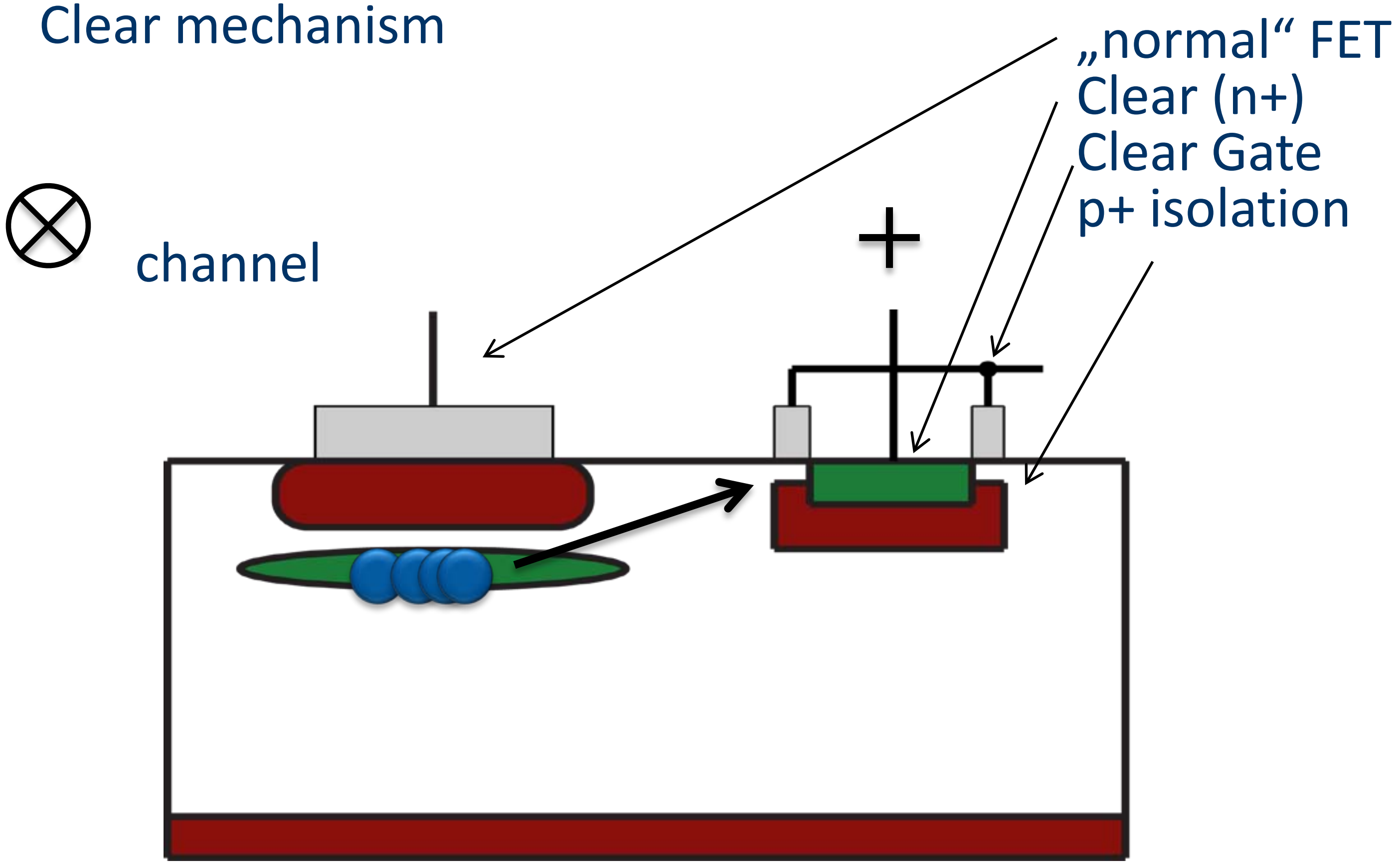

Picture from side (90°rotated)

Working principle of a DEPFET

1. DEPFET = Depleted Field Effect Transistor
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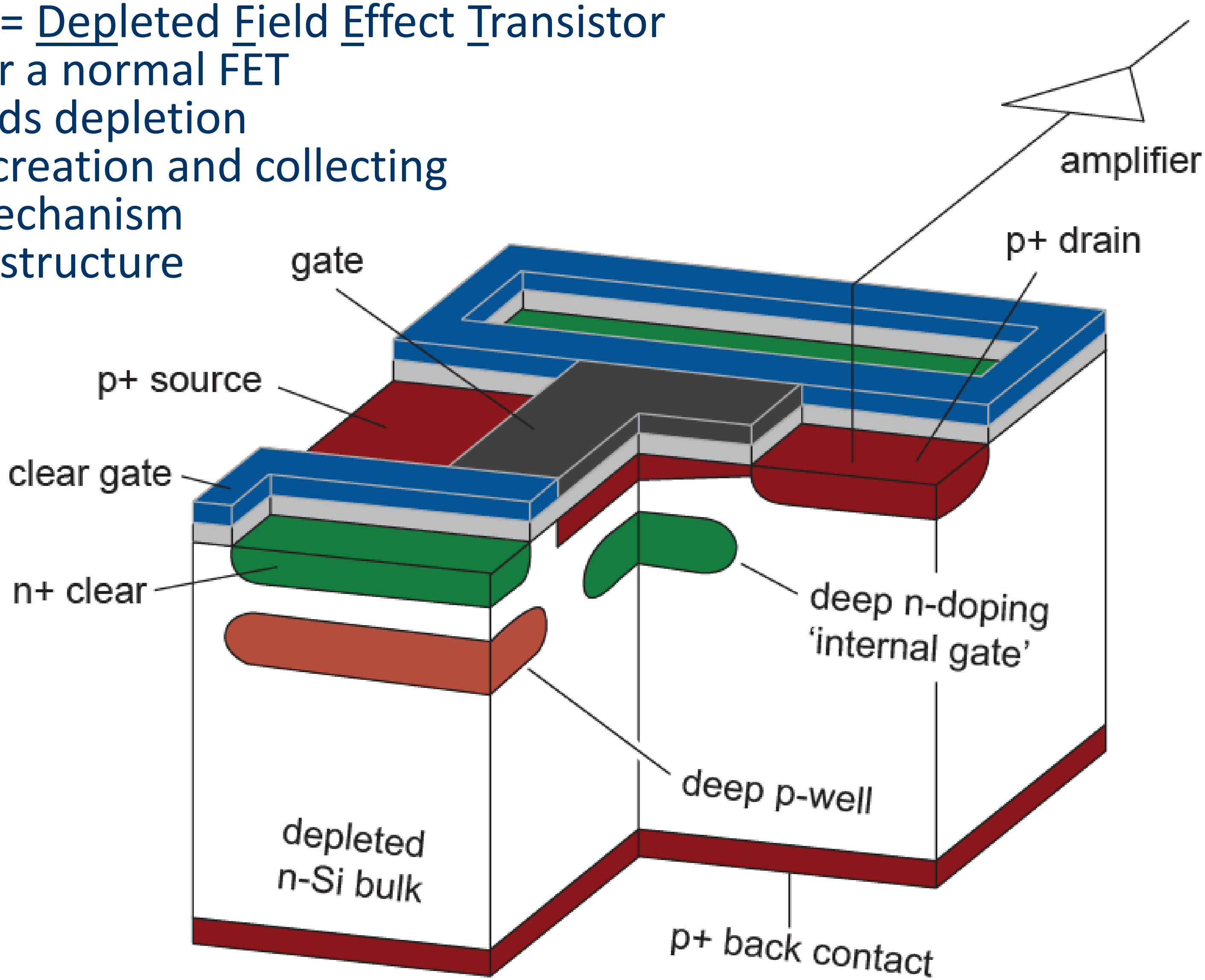
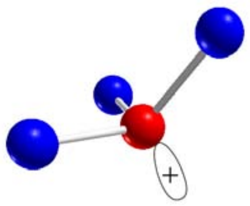
3. Sidewards depletion
4. Charge creation and collecting
5. Clear mechanism
6. DEPFET structure



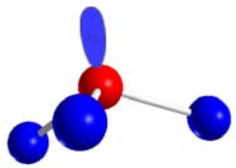
IONIZING RADIATION AND SIO_2

Influence of ionizing radiation

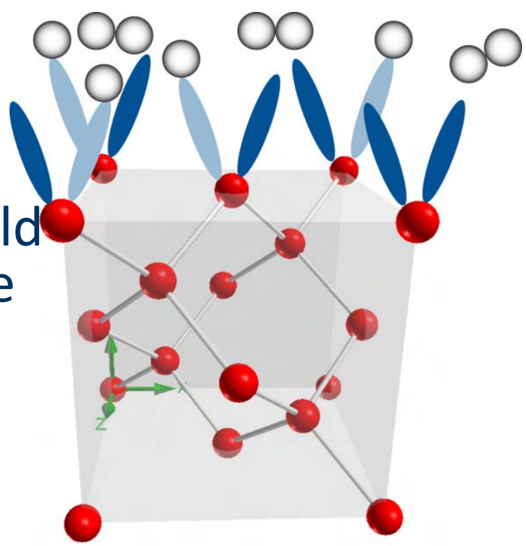
Surface defects – Defects in silicon dioxide



1. Trapped oxide charge
   a) e^-/h^+ pairs created
   b) Electrons have high mobility, swept out of the oxide, holes get trapped
      i. E‘ center → change in $V_{threshold}$

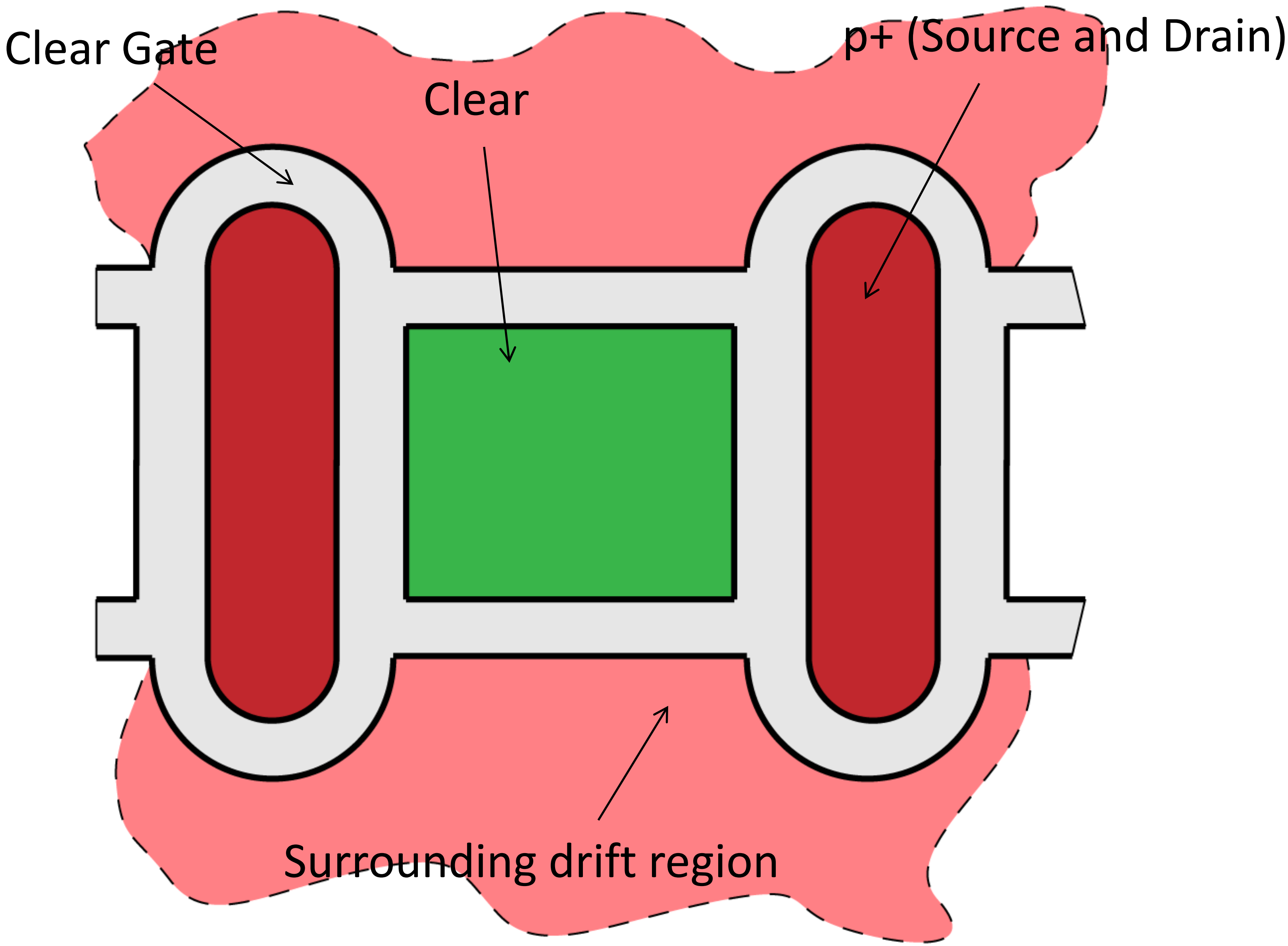


2. Dangling bonds
   a) Hydrogen is used to saturate open bindings (dangling bonds) during production
   b) Ionizing radiation frees protons
   c) Protons travel to defects (near Si-SiO_2 interface)
   d) Creation of H_2 and dangling bonds
      i. Increase in noise(1/f), and subthreshold swing S. Decrease in transconductance g_m

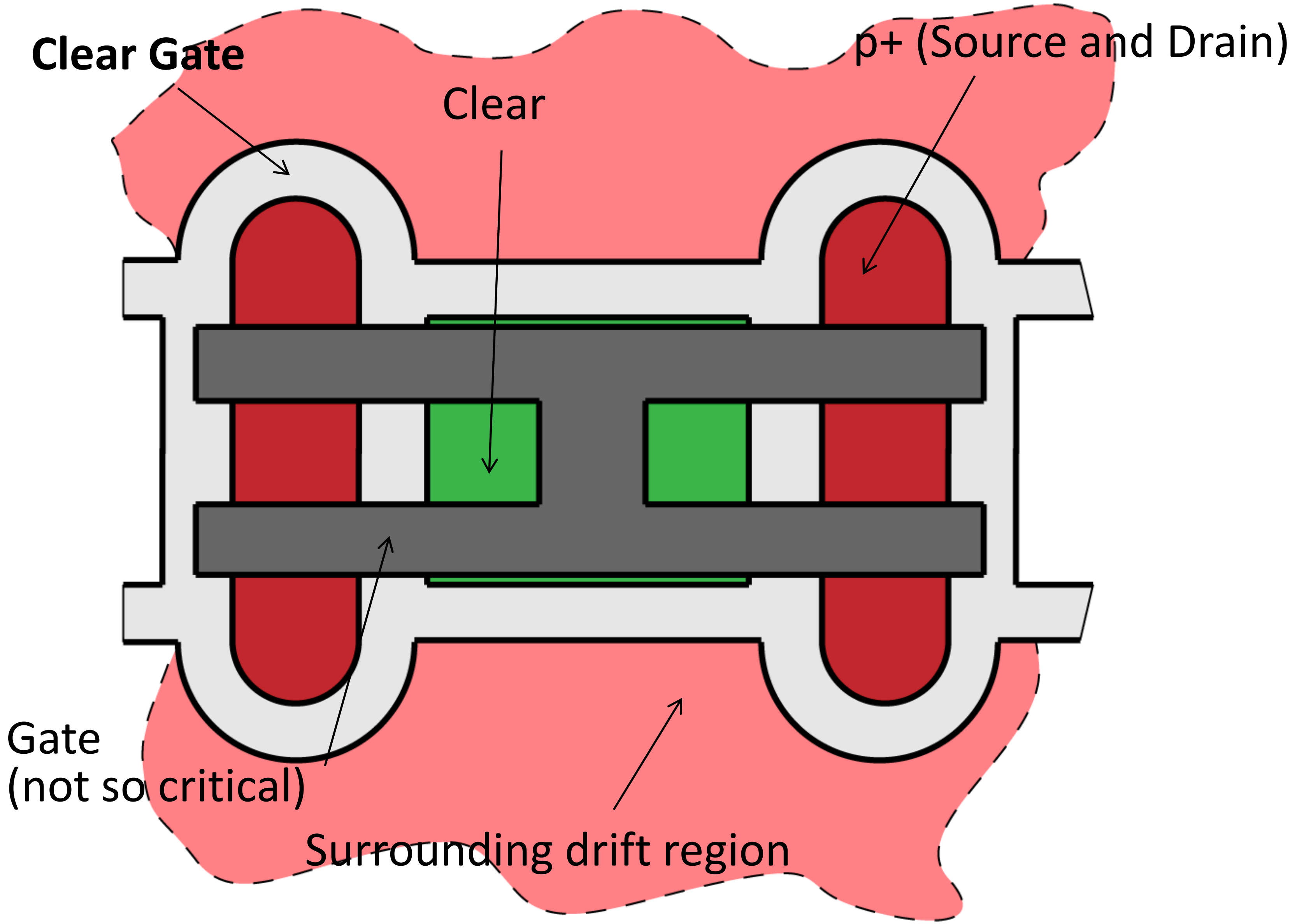


PIXEL LAYOUT AND VOLTAGE DEPENDANCIES

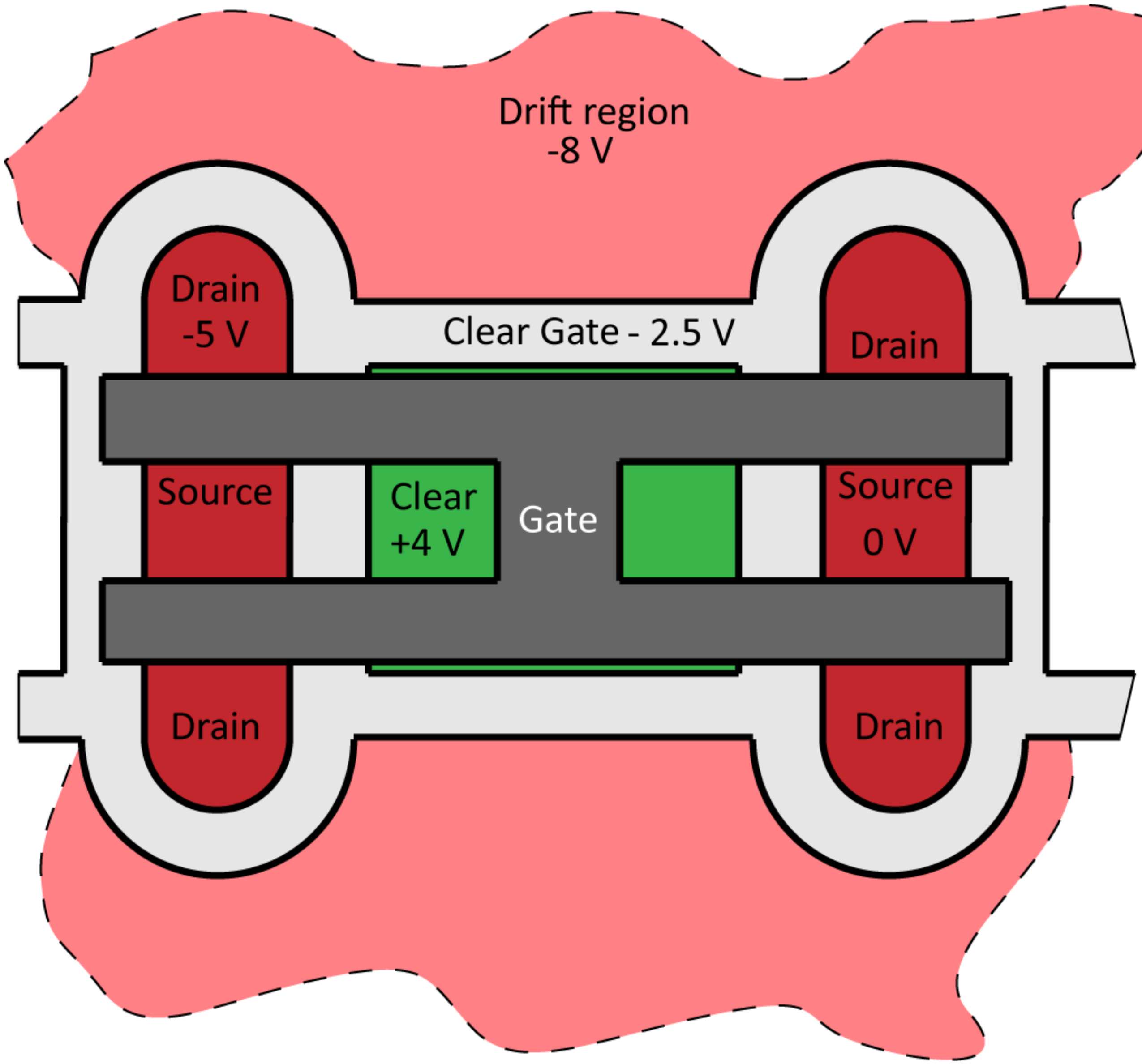
Motivation - Possible Pixel Layout



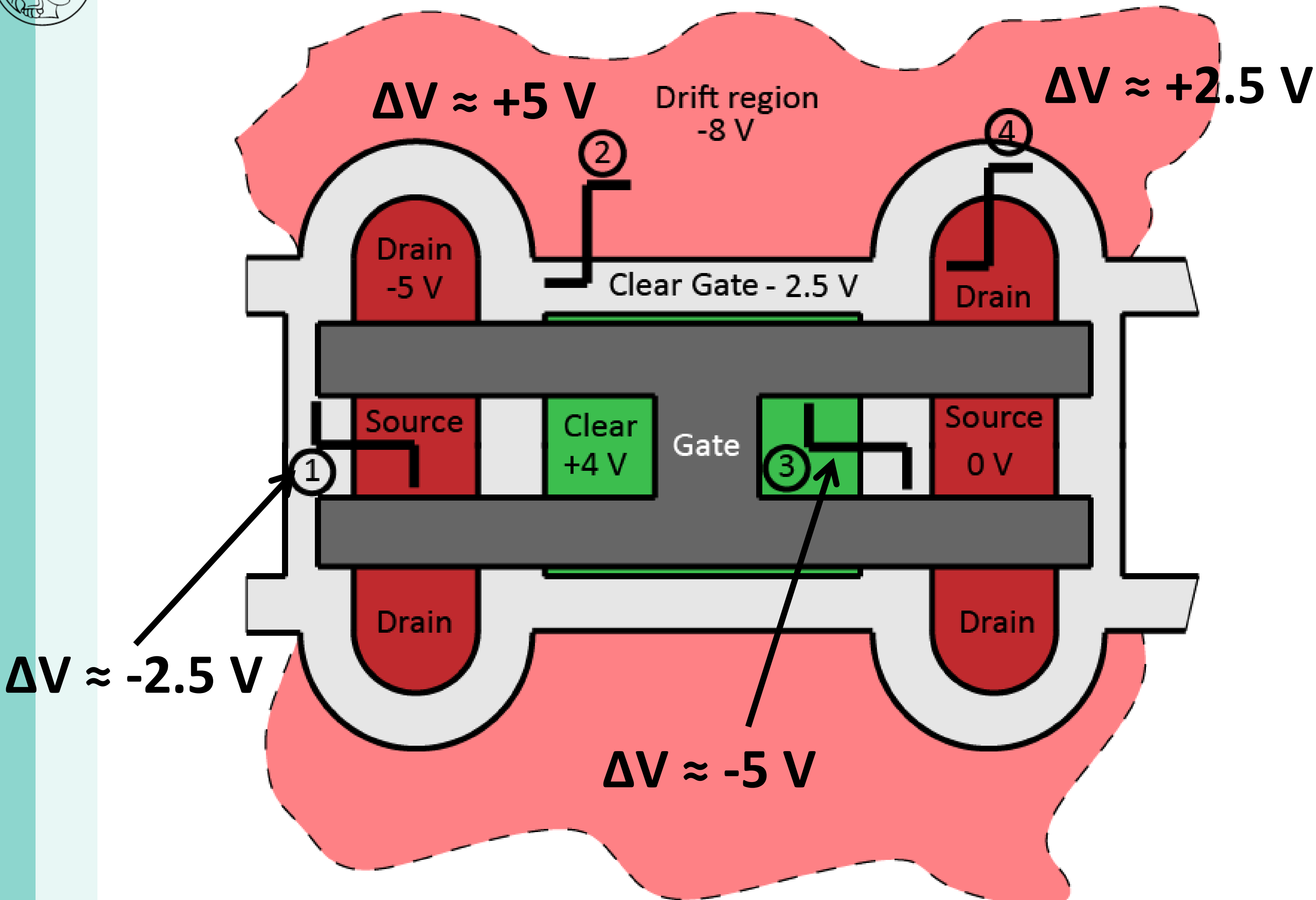
Motivation (II)- Possible Pixel Layout



Motivation (III)- Possible Pixel Layout and Potentials



Motivation (IV)- Possible Pixel Layout and relevant cross sections



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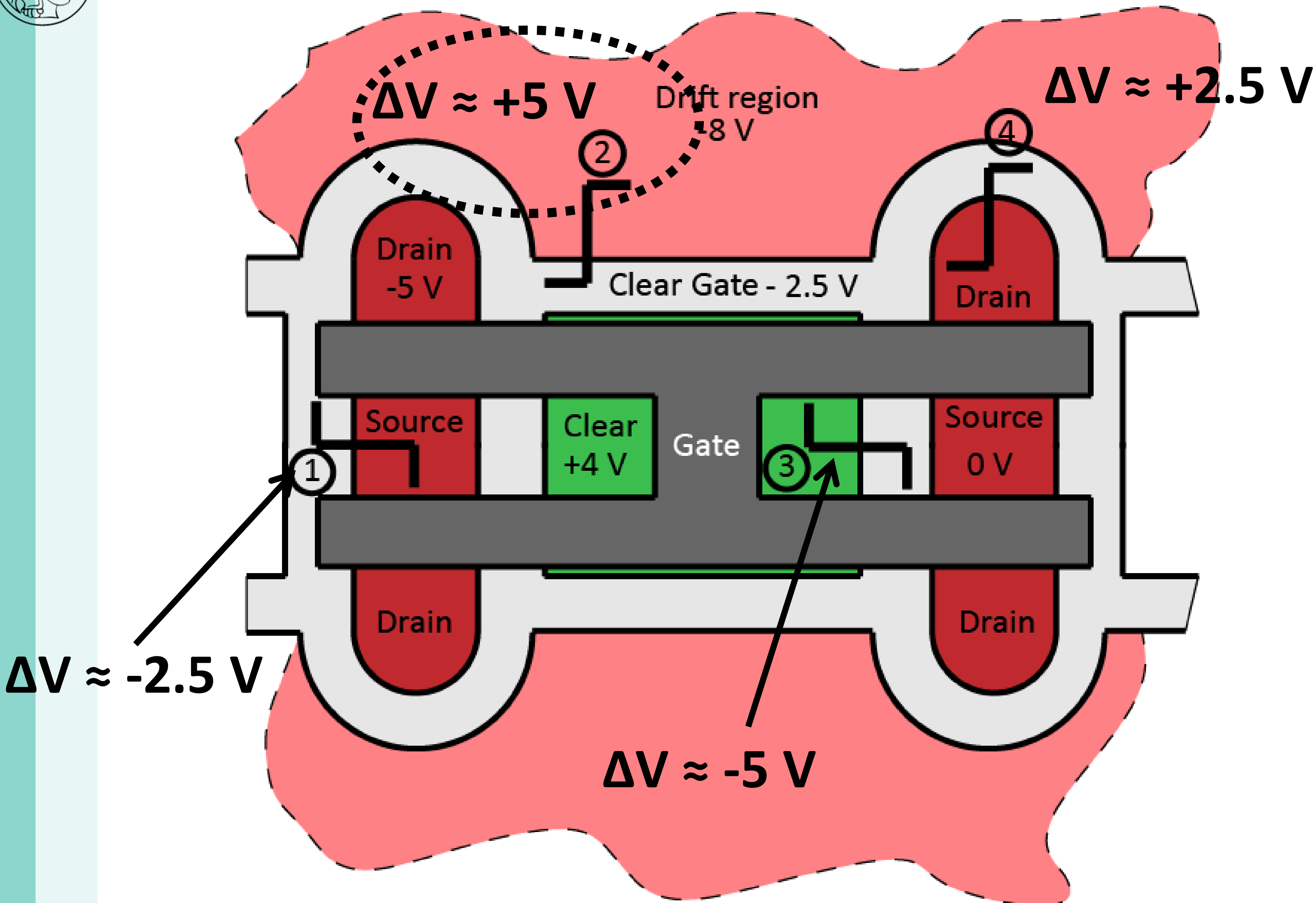
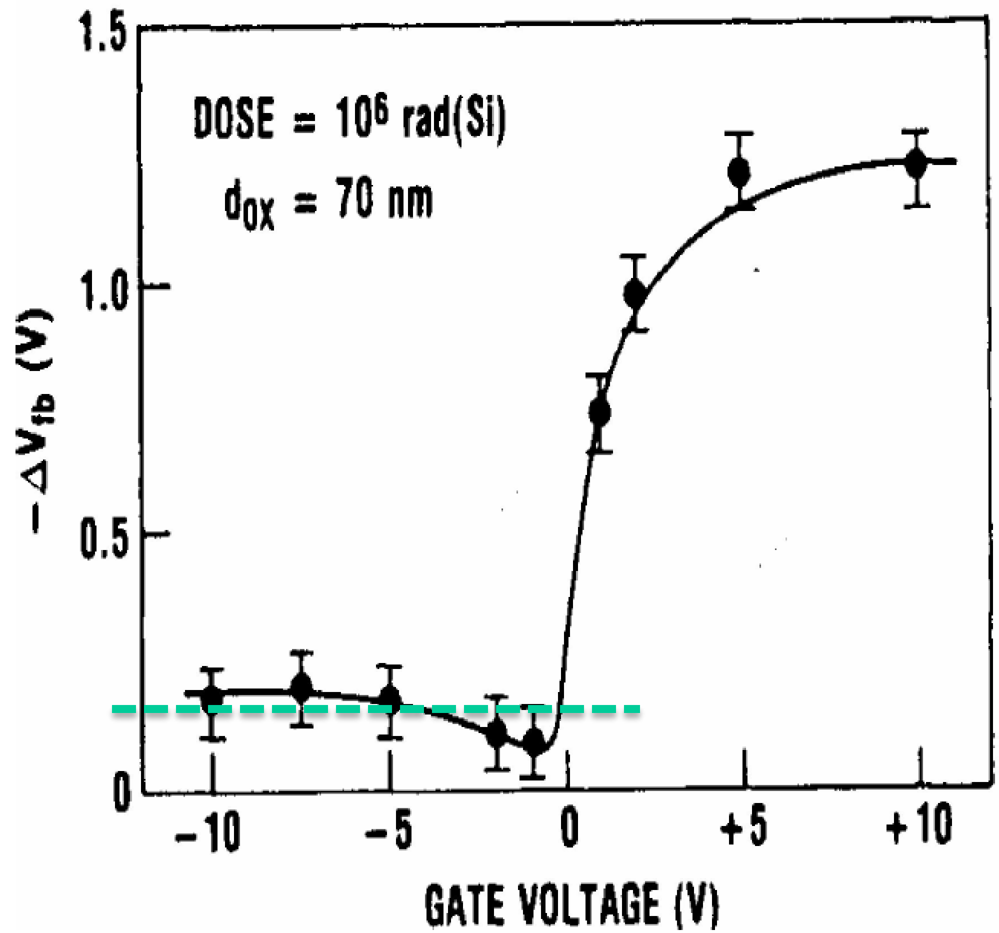


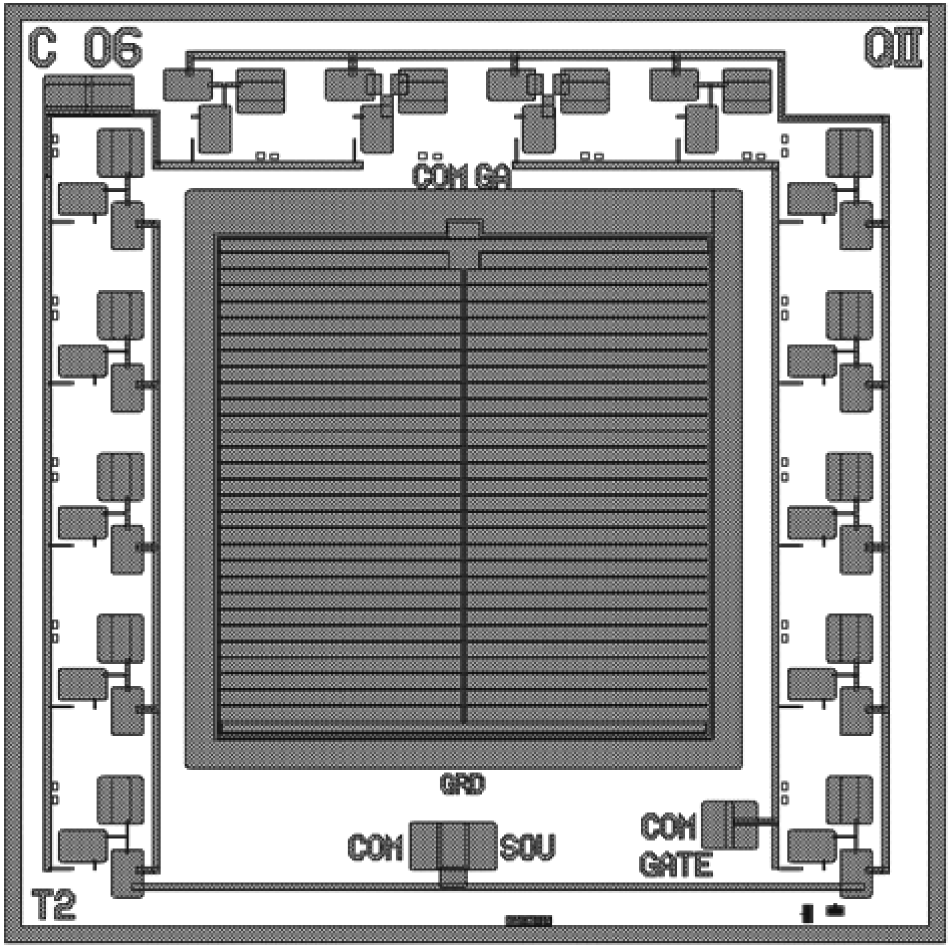
Change in threshold voltage shift due to certain Gate voltages



Ma/Dressendorfer

Only one Clear Gate volatge avialable → **flat** region is favoured

Layout of thin oxide devices

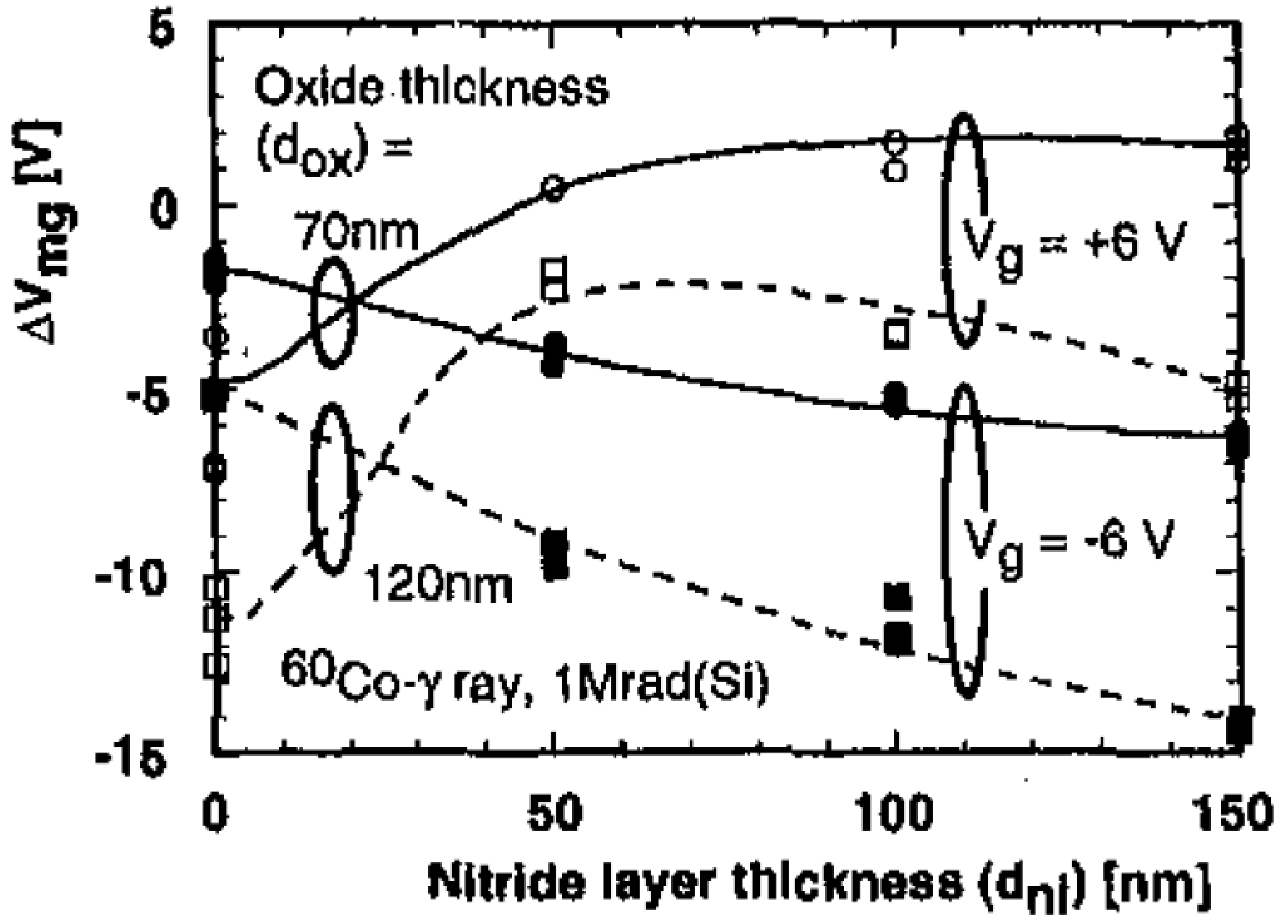


Characteristics of thin oxide structures:

- thin and thick Si_3N_4
- SiO_2 thickness is the same for all
- Central device: Gate Controlled Diode
- 14 Transistor (=2x7), with diff. Gate length and width
- Doping profiles similar to Clear Gate

Thick nitride and Gate voltages

Thicker nitride could be a solution to the problem at hand.



Radiation-Induced Trapped Charge in
Metal-Nitride-Oxide-Semiconductor Structure; Takahashi et. al.
IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL 46, NO 6, DECEMBER 1999

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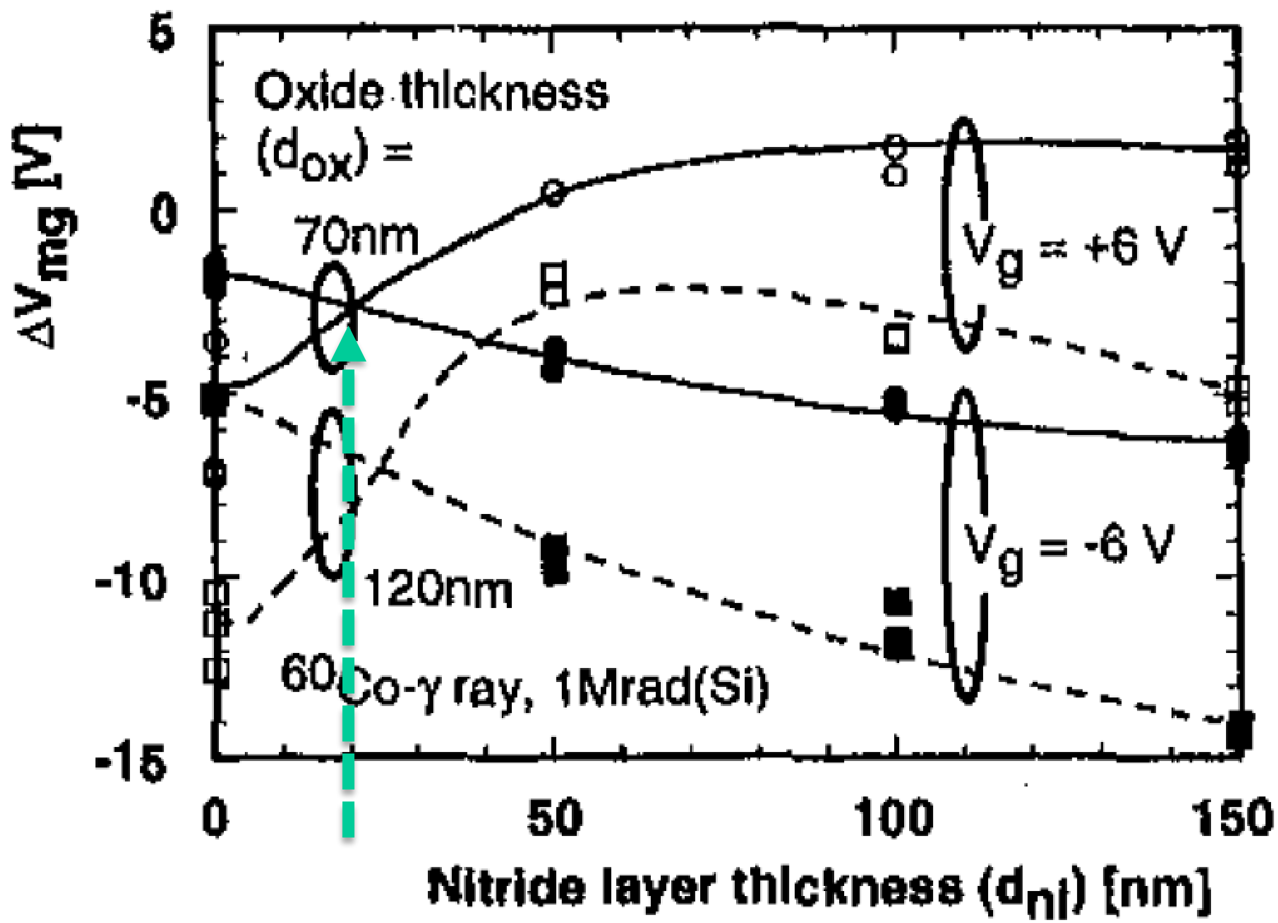

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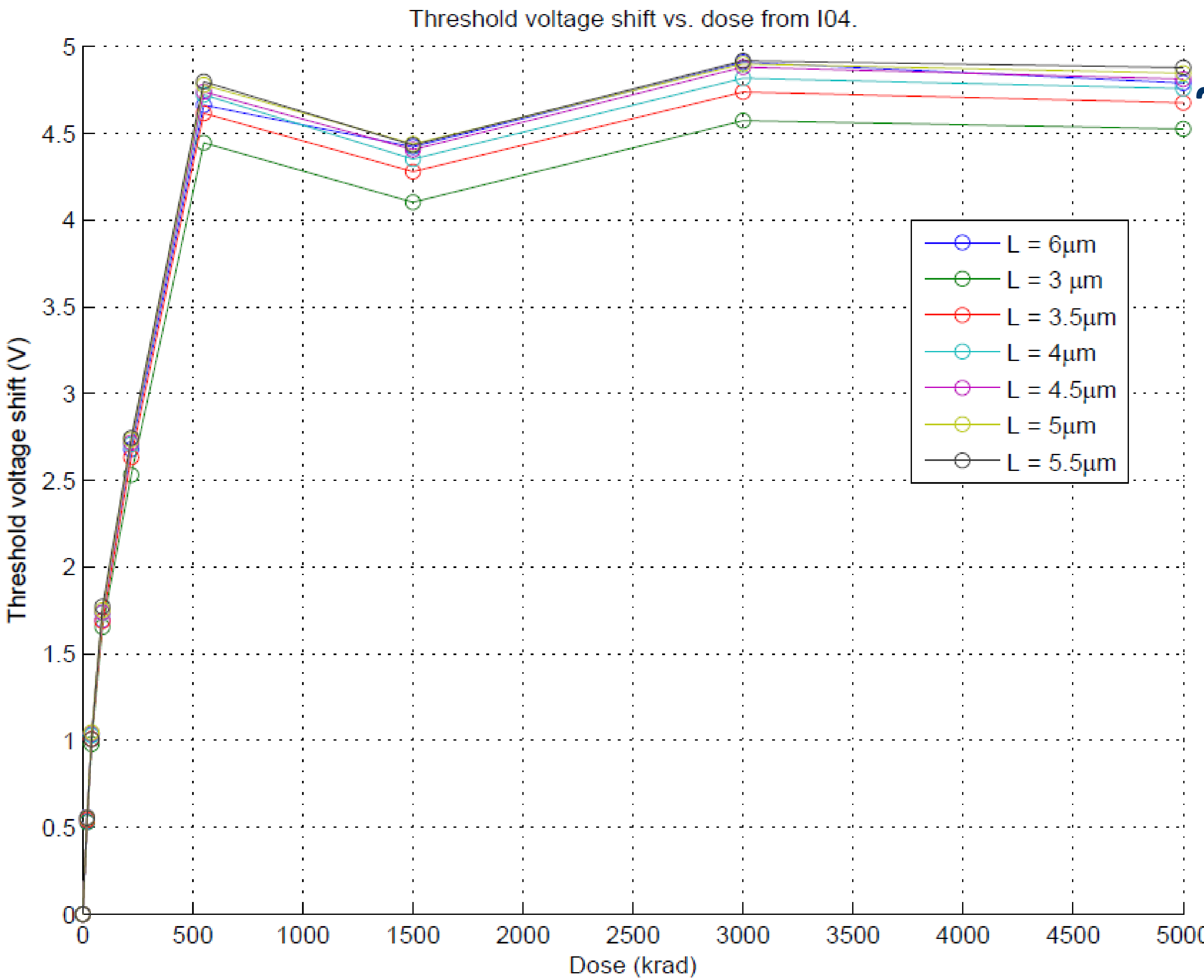
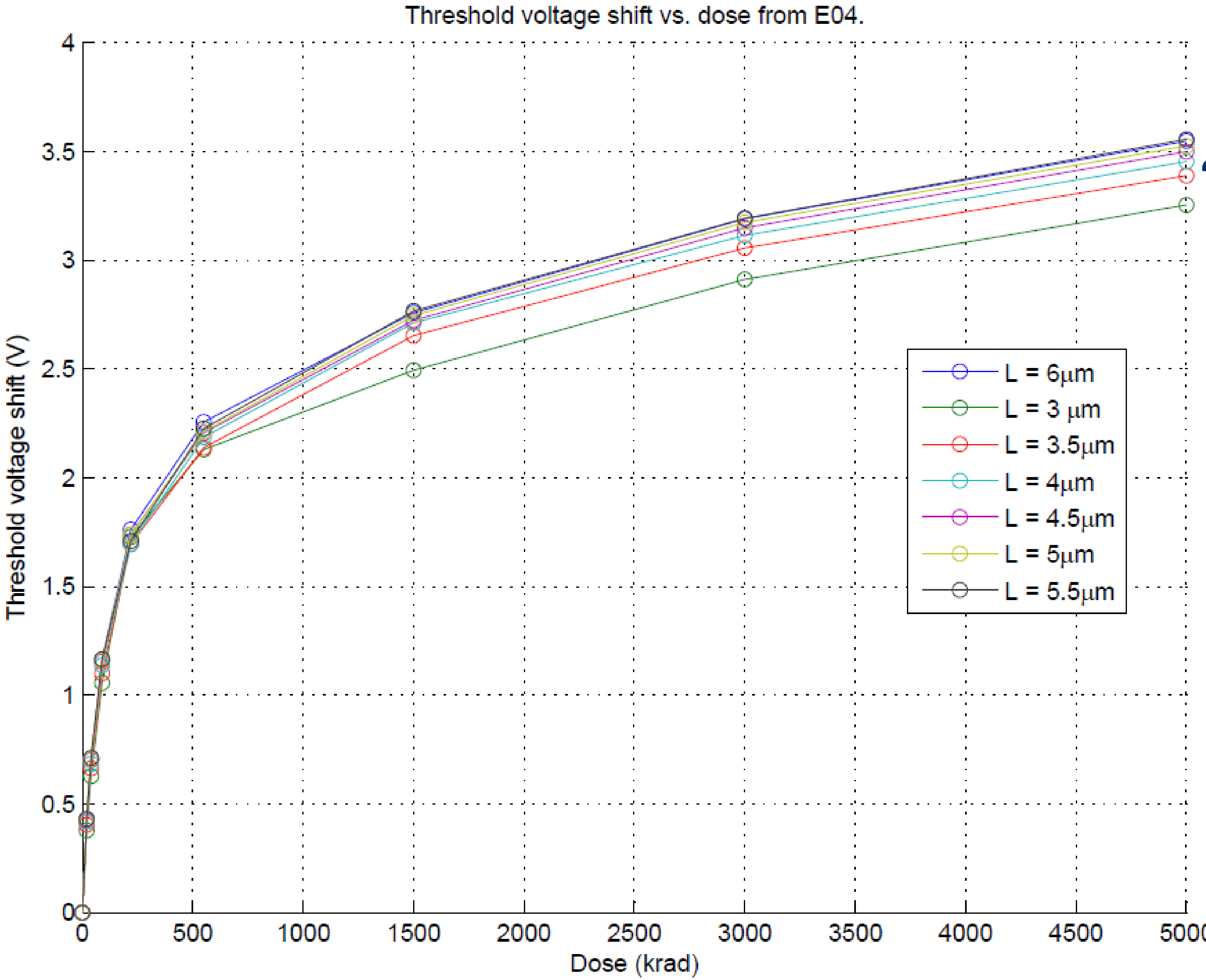
Clear Gate Results, **-5 V** during Irradiation



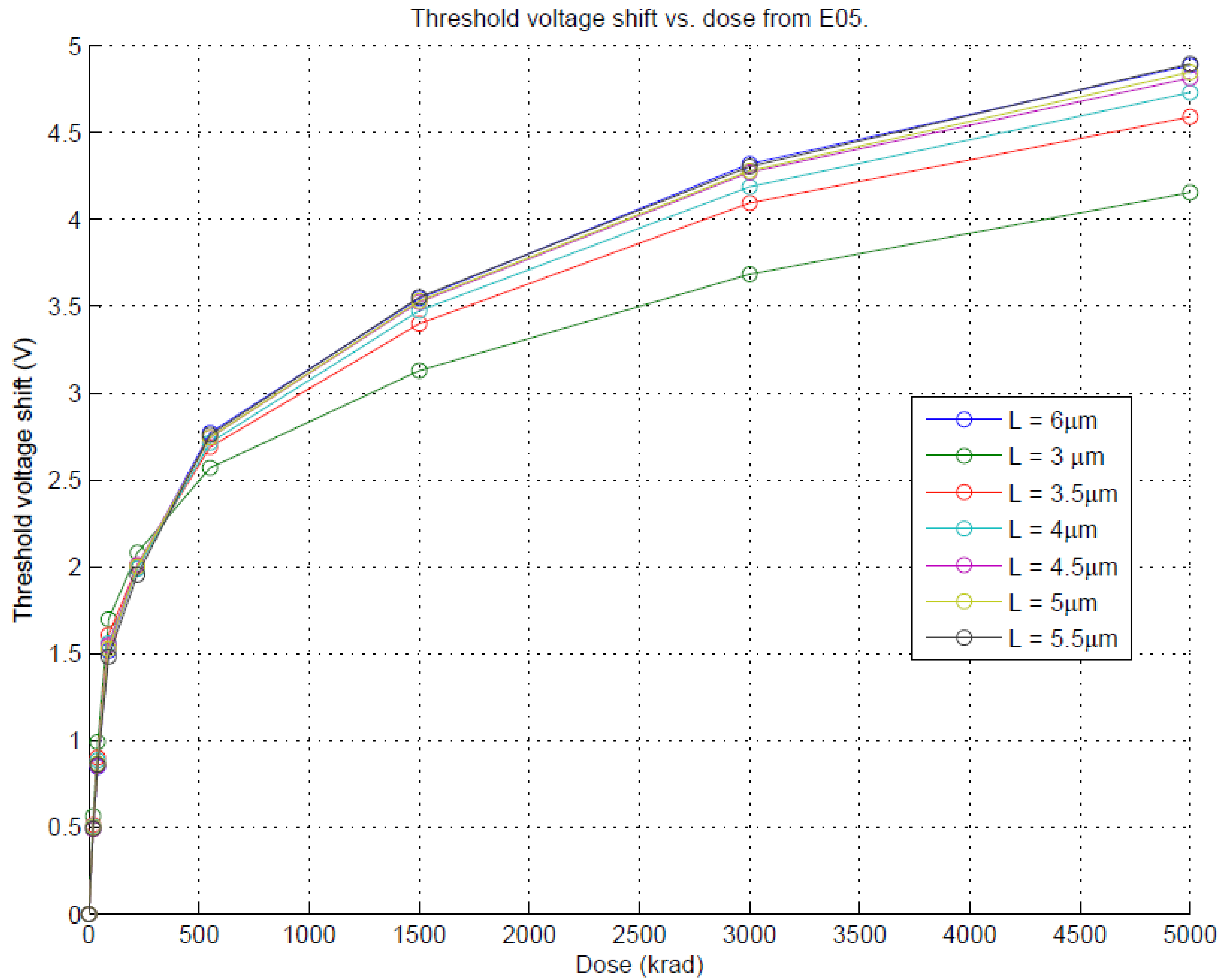
~4.7 V

Clear Gate Results, **0 V** during Irradiation



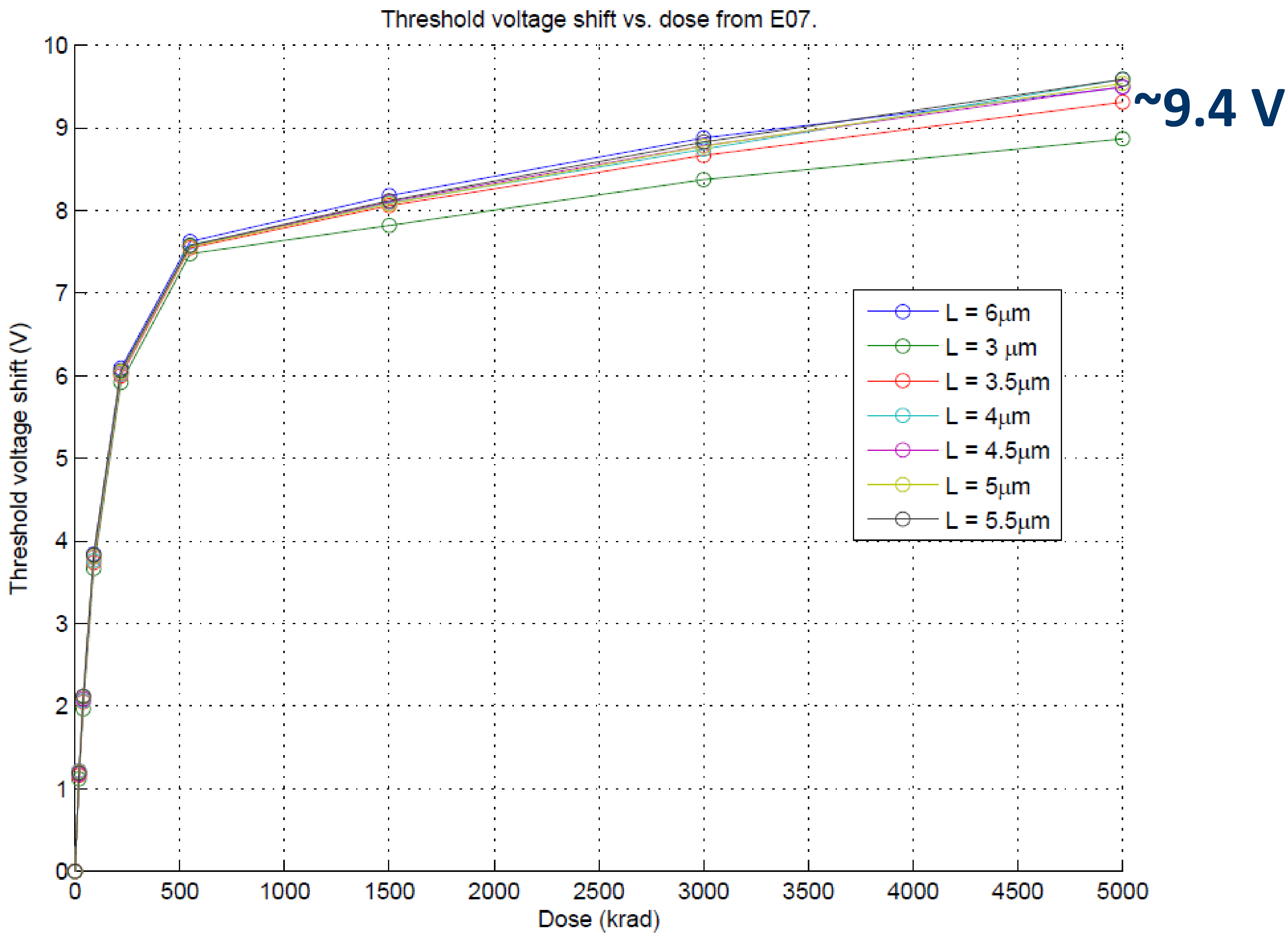
~3.4 V

Clear Gate Results, **+2.5 V** during Irradiation

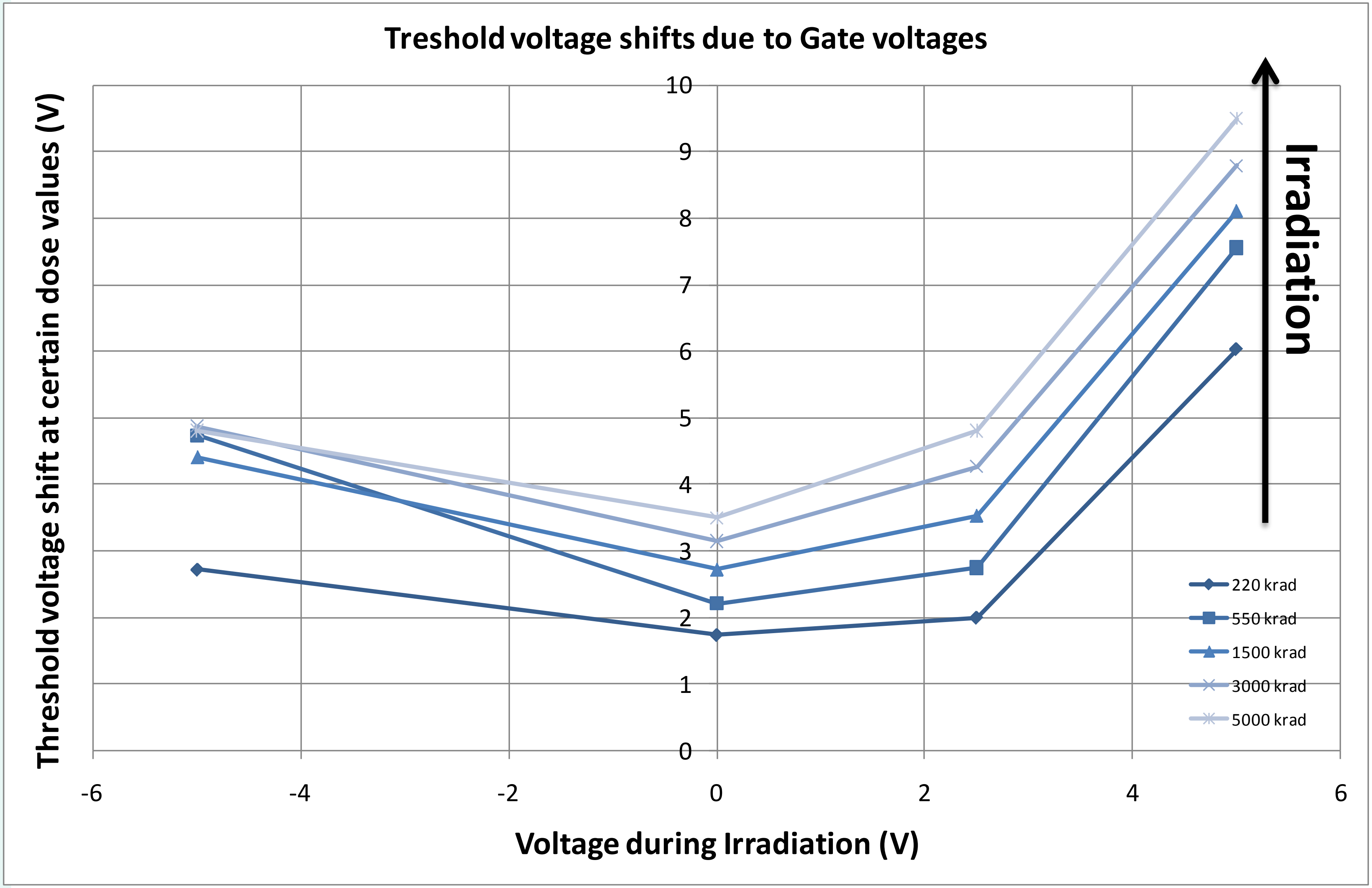


~4.7 V

Clear Gate Results, **+5 V** during Irradiation



Change in threshold voltage shift due to certain Gate voltages (thick nitride)



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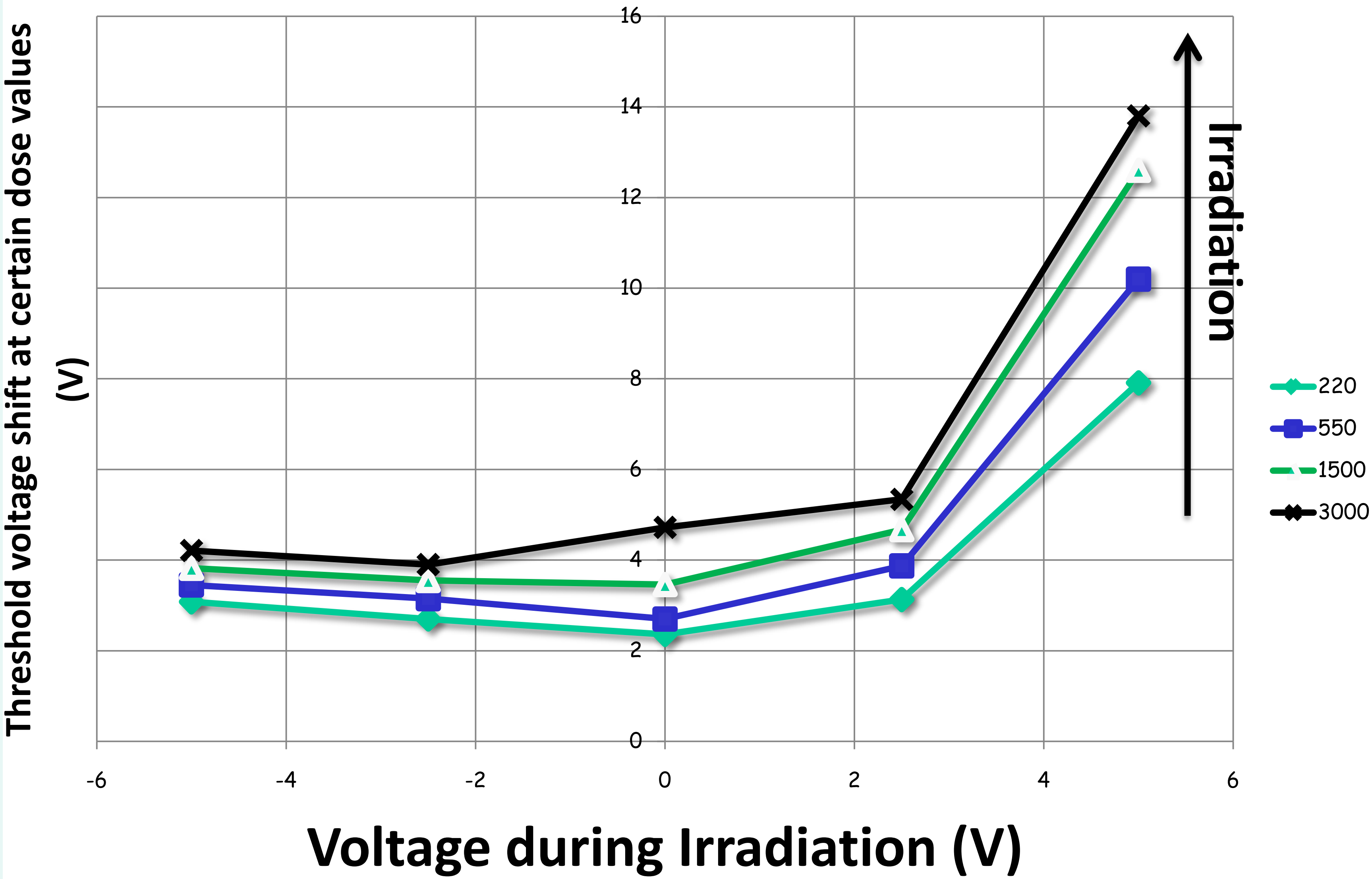


Comparison between thin and thick Si_3N_4

Thin Si_3N_4

- Max. threshold voltage shift
  - 13.8 V @ 3 Mrad

Thick Si_3N_4

- Max. threshold voltage shift
  - 9.4 V @ 5 Mrad
  - 8.6 V @ 3 Mrad

Comparison between thin and thick Si_3N_4

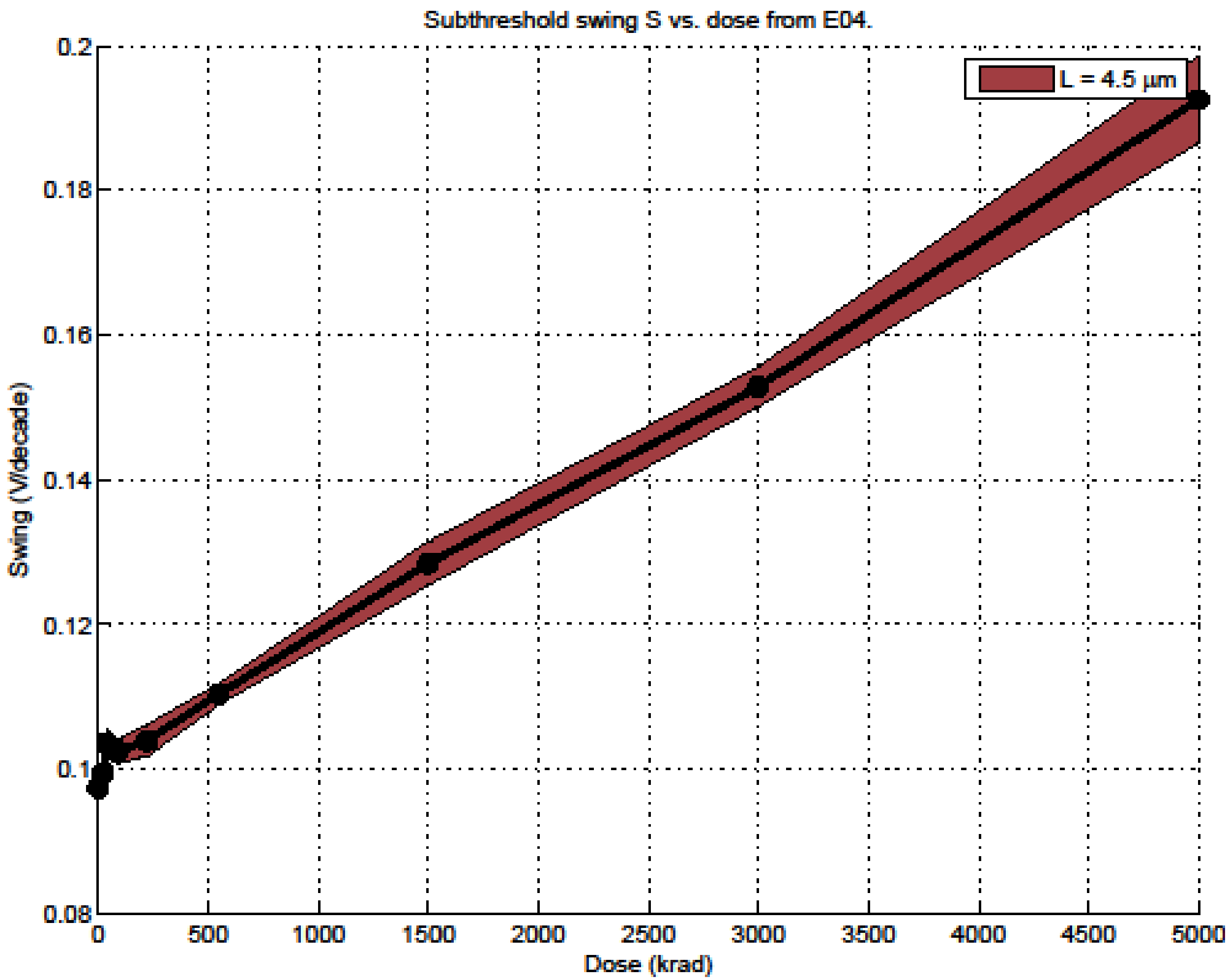
Thin Si_3N_4

- Max. threshold voltage shift
  - 13.8 V @ 3 Mrad
- Flatness
  - Δ along Gate voltage = 1.1 V @ 3 Mrad

Thick Si_3N_4

- Max. threshold voltage shift
  - 9.4 V @ 5 Mrad
  - 8.6 V @ 3 Mrad
- Flatness
  - Δ along Gate voltage = 1.3 V @ 5 Mrad

Interface traps and influence on subthreshold swing S



Interface trap density D_{it}

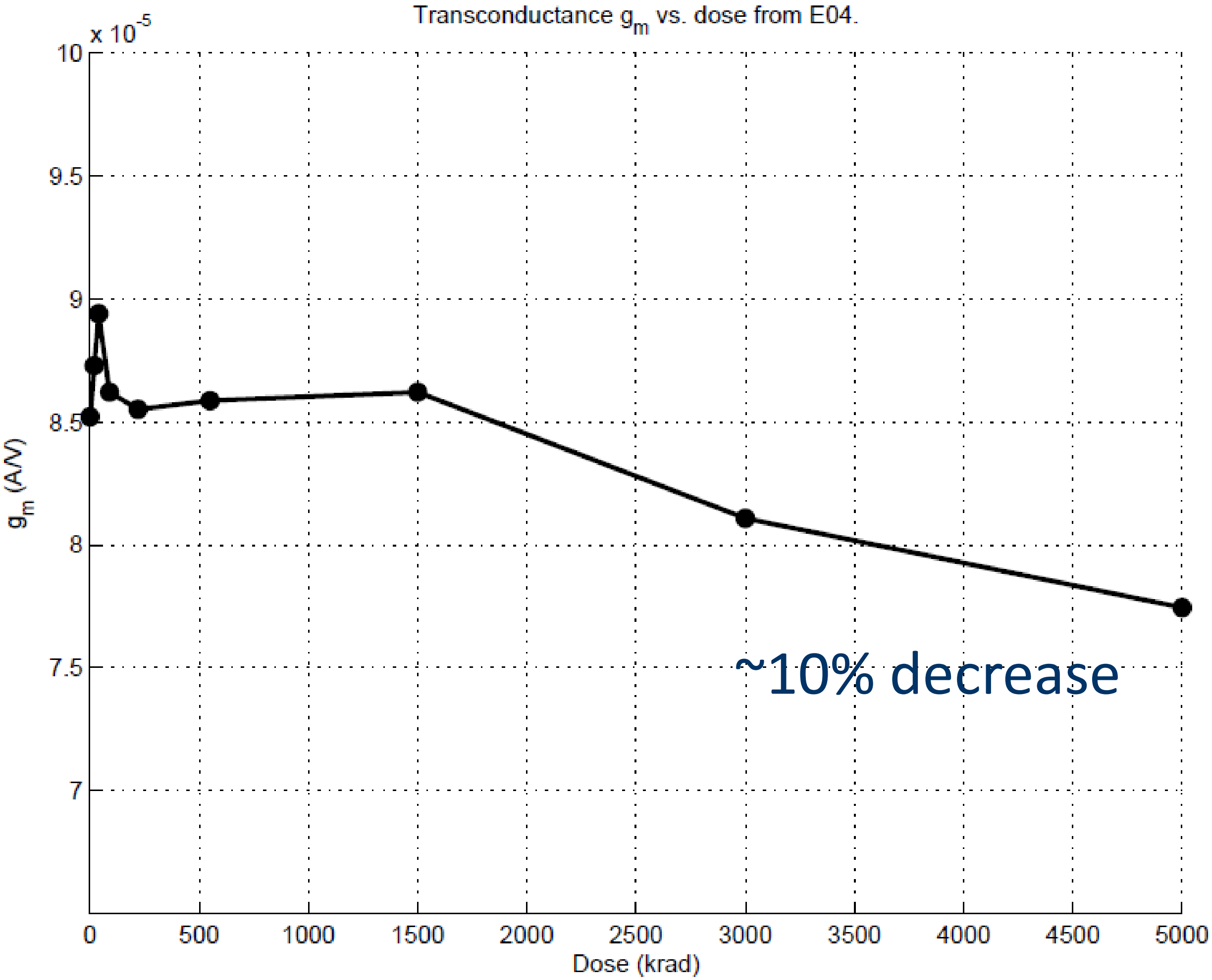
- #D_{it} influences Swing and mobility
- Mobility µ affects g_m, and also the internal amplification g_q

$$\Delta S = kT \ln 10 \left(\frac{\Delta D_{it}}{C_{ox}} \right)$$

$$\Delta D_{it} \propto \Delta S$$

$$g_q \propto \frac{g_m}{C_{ox}}$$

Interface traps and influence on transconductance g_m



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Summary and Outlook

Summary

- Radiation hardness of Clear Gate region is more complex, intra pixel deviations
  - Investigate different thicknesses of nitride
  - Adapt pixel design
- Inhomogeneous irradiation along z can be compensated via segmentation of modules
- Thicker nitride is better in case for the Clear Gate voltage

Outlook

- Additional radiation campaigns with diff. nitride layer thickness will be conducted

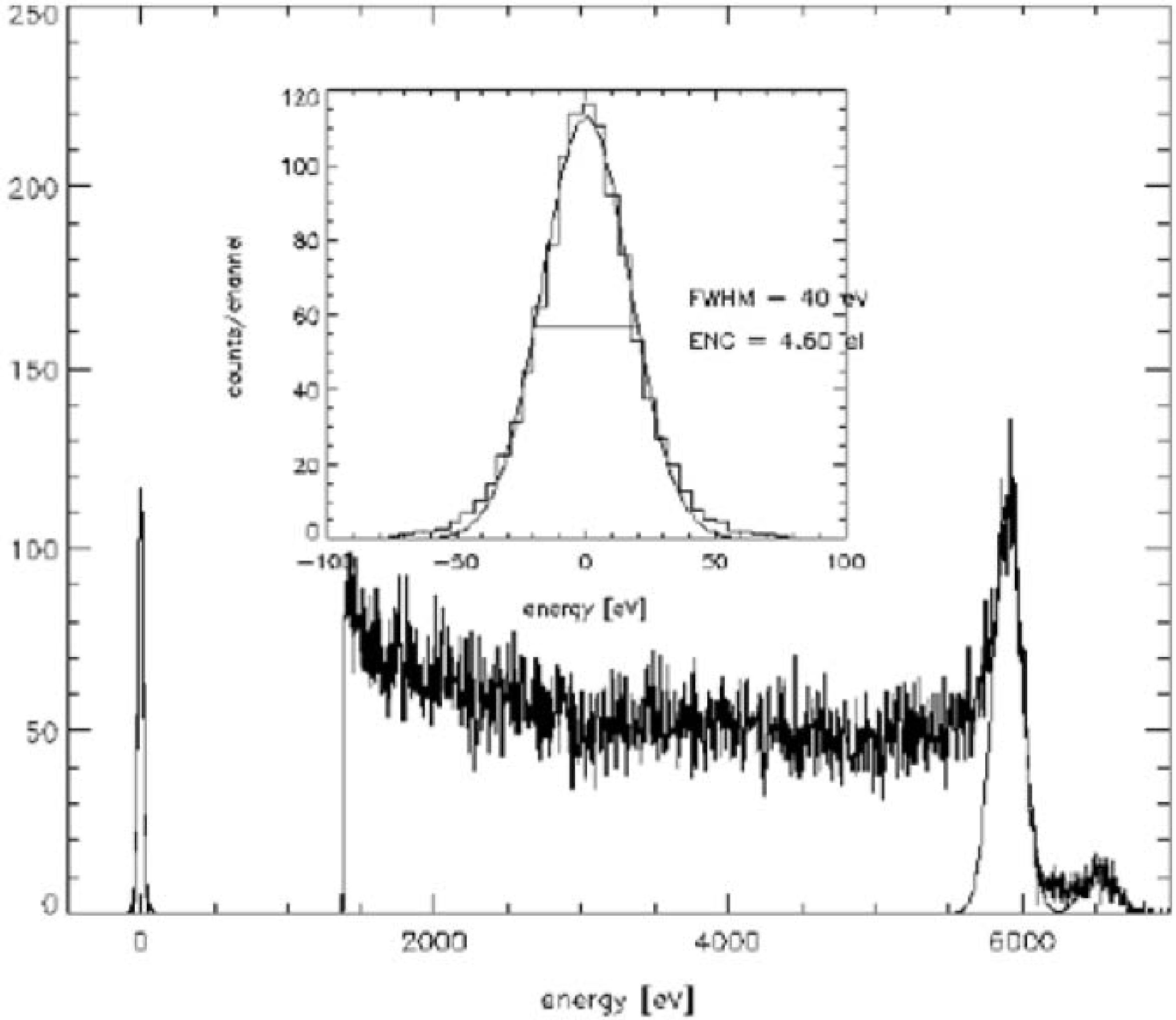
Acknowledgement

- KIT for x-ray tube and staff

Thank you

Backup

Noise after Irradiation



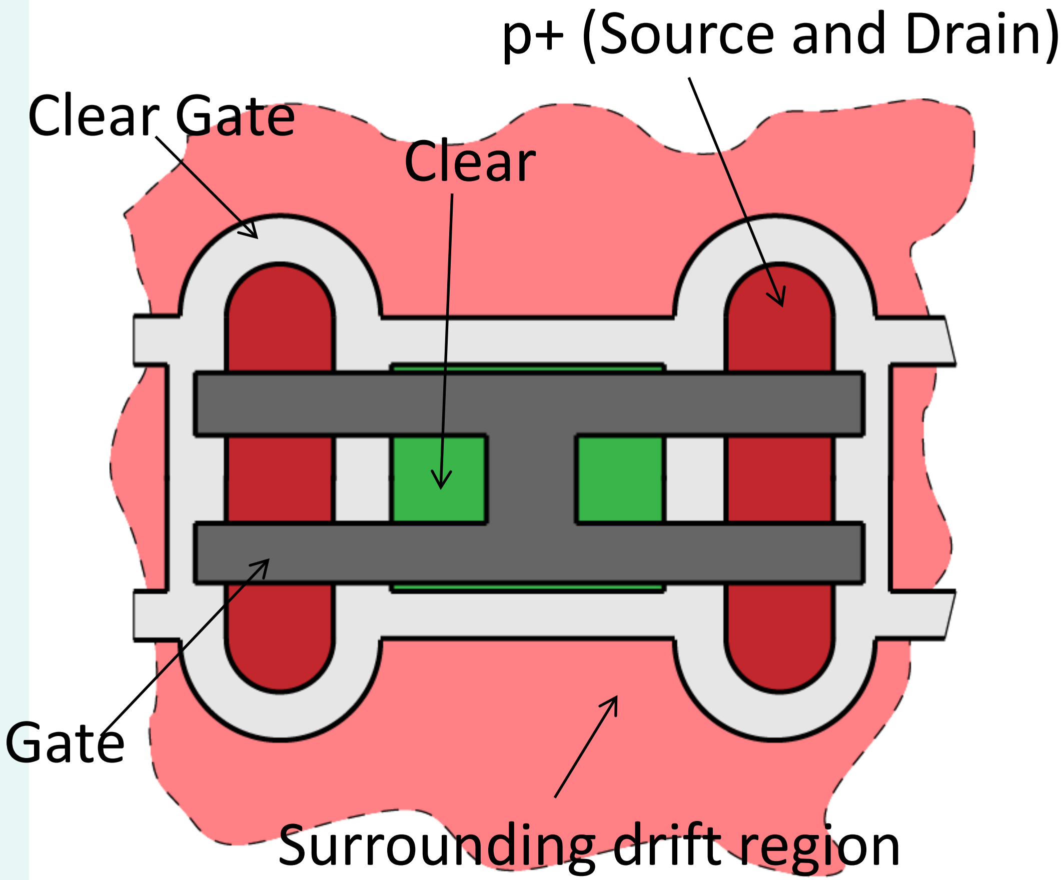
(b) Fe^{55} spectra after 8MRad

S. Rummel

4.6 e^- ENC after 8 Mrad (^{55}Fe), PXD5

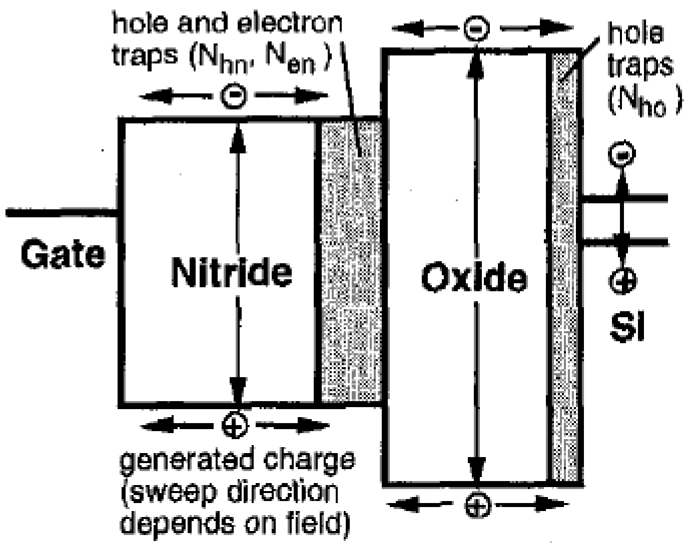
SNR=27 @ ^{109}Cd (22keV)

Ionizing radiation in gate region



- Gate region exhibits a more homogeneous voltage region than the clear gate (very thick oxide in between)
  → common shift adjustable
- Problem: inhomogeneous irradiation along z in the detector
  → Solution: segmentation of module
- Irradiations with diff. Nitride thicknesses show good results for thinnest layer.

Trapping in insulator layer



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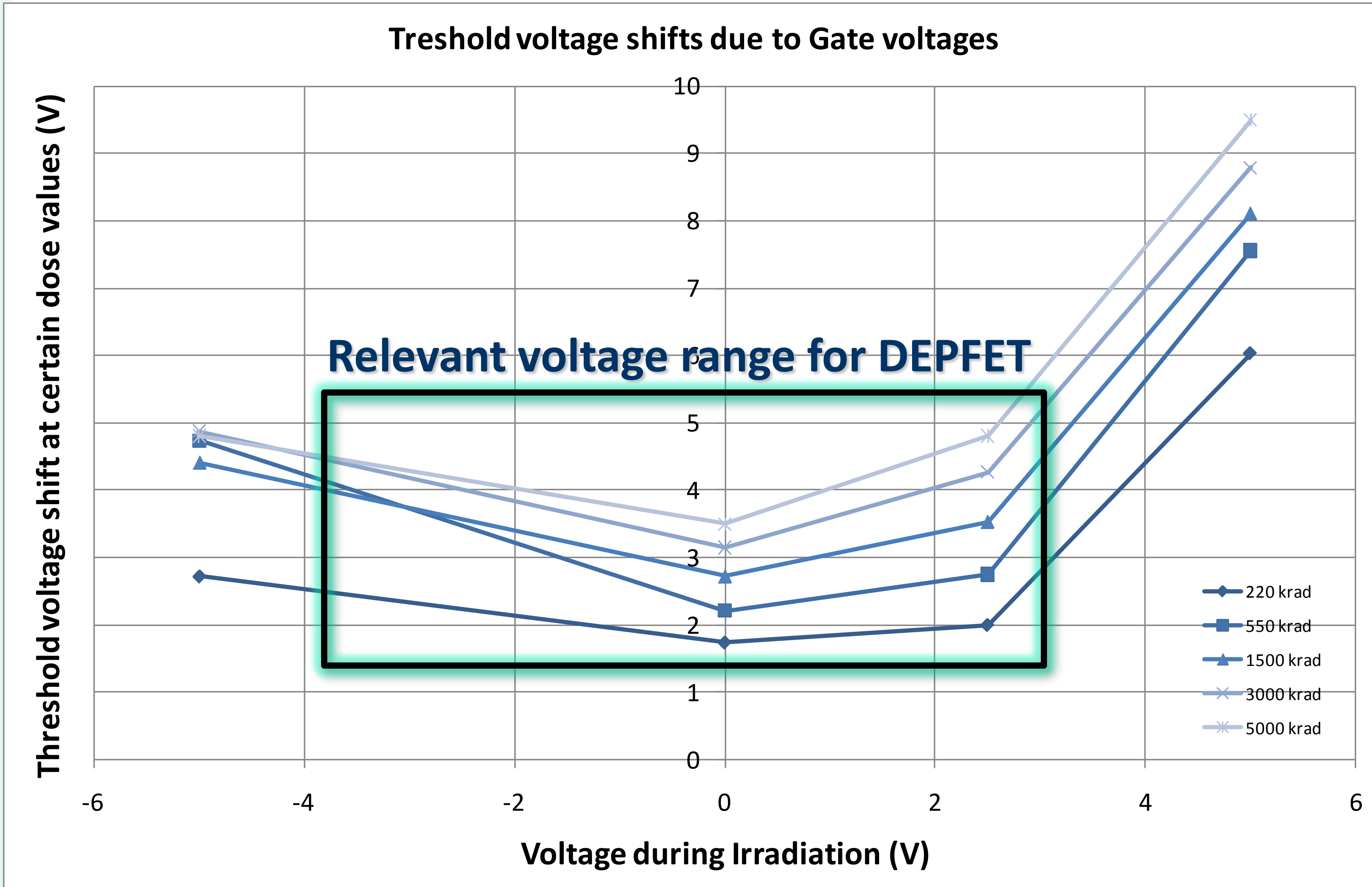
$+V_G$

1. Holes in oxide to Si-SiO_2 interface
2. Holes in Si_3N_4 and electrons from SiO_2 to N-O interface
3. Recombination rate in Si_3N_4 lower than in SiO_2 (+trap density precursors)
   → more e^- trapped at N-O
4. Build-up of e^- reduces field in oxide → saturation

$-V_G$
Field always present

Thick Si_3N_4
→ Reduces field in ox (capacitance voltage divider) → saturation

Threshold voltage shifts due to Gate voltages



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