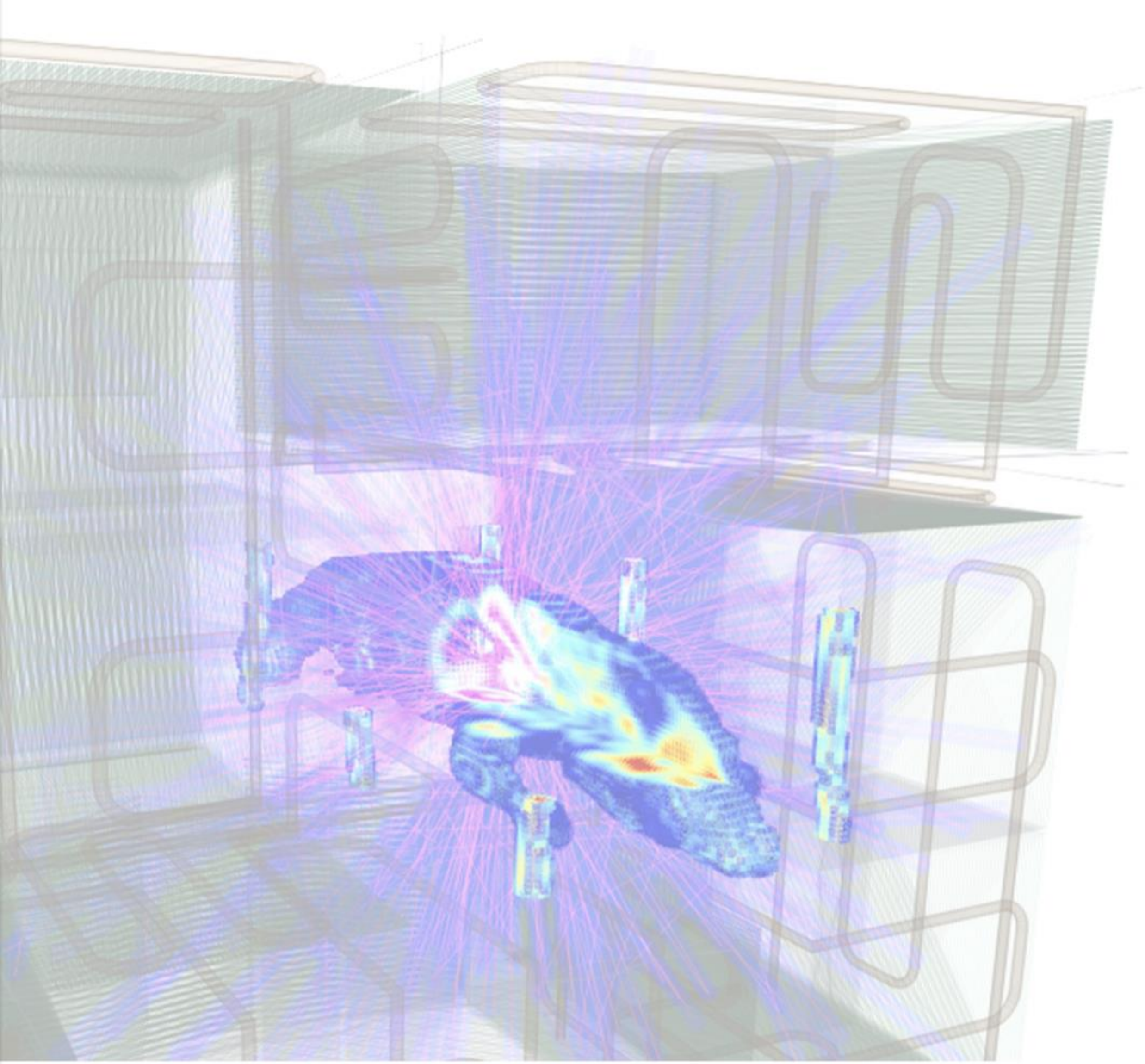

100µPET

a ultra-high-resolution silicon-pixel-based small animal PET scanner

R. Cardella, on behalf of the collaboration

Swiss National Science Foundation

EPFL

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UNI LU

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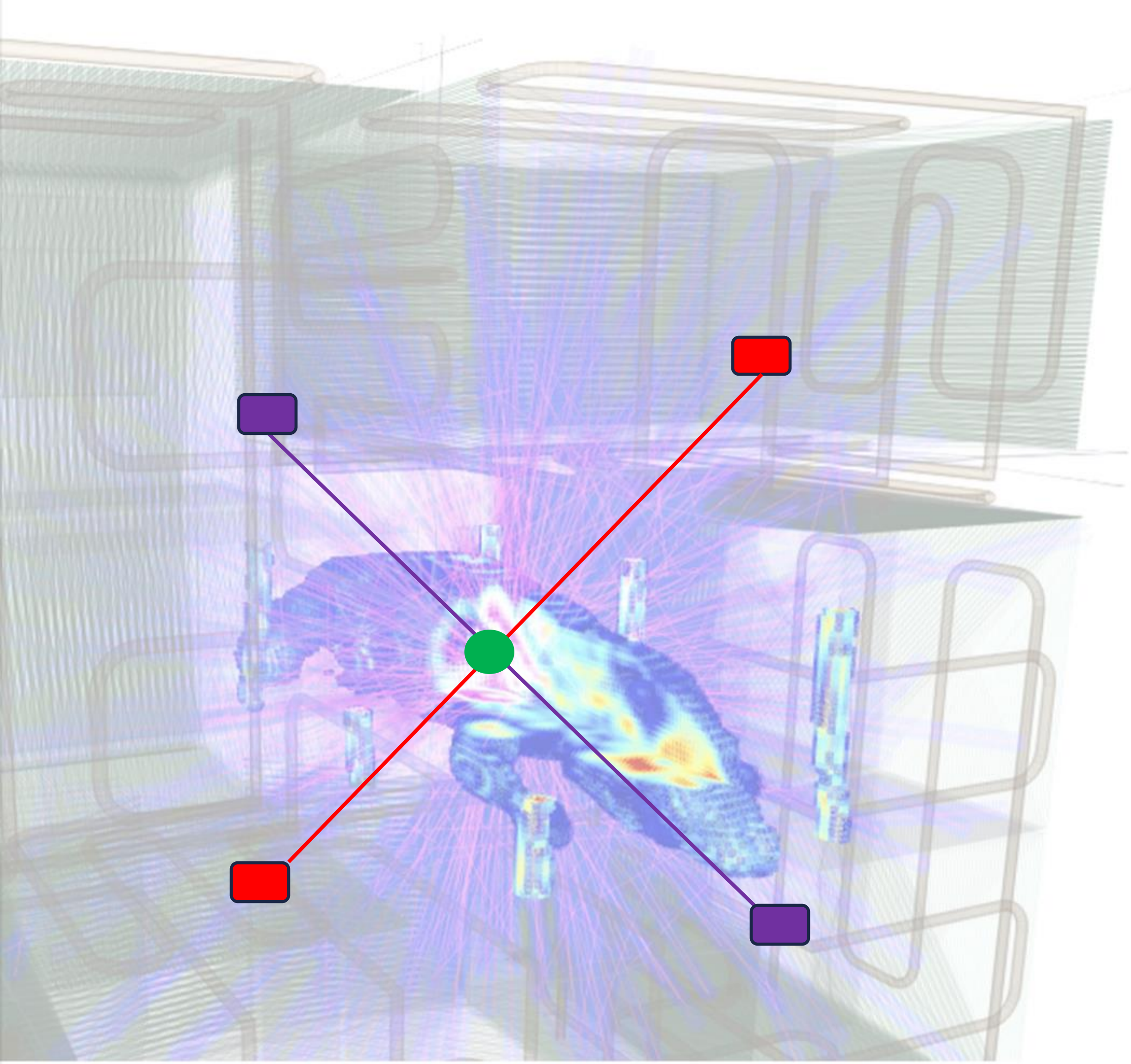

- Radiotracer injected into the body
- Cells with abnormal metabolic behavior will show an excess of radiotracers
- Positron emission -> e- e+ annihilation
- Detect 2 back-to-back Gamma at 511 keV
- Reconstruct image from Line of Response (LoR)

Atherosclerosis plaques in mouse
Pre-clinical scanner

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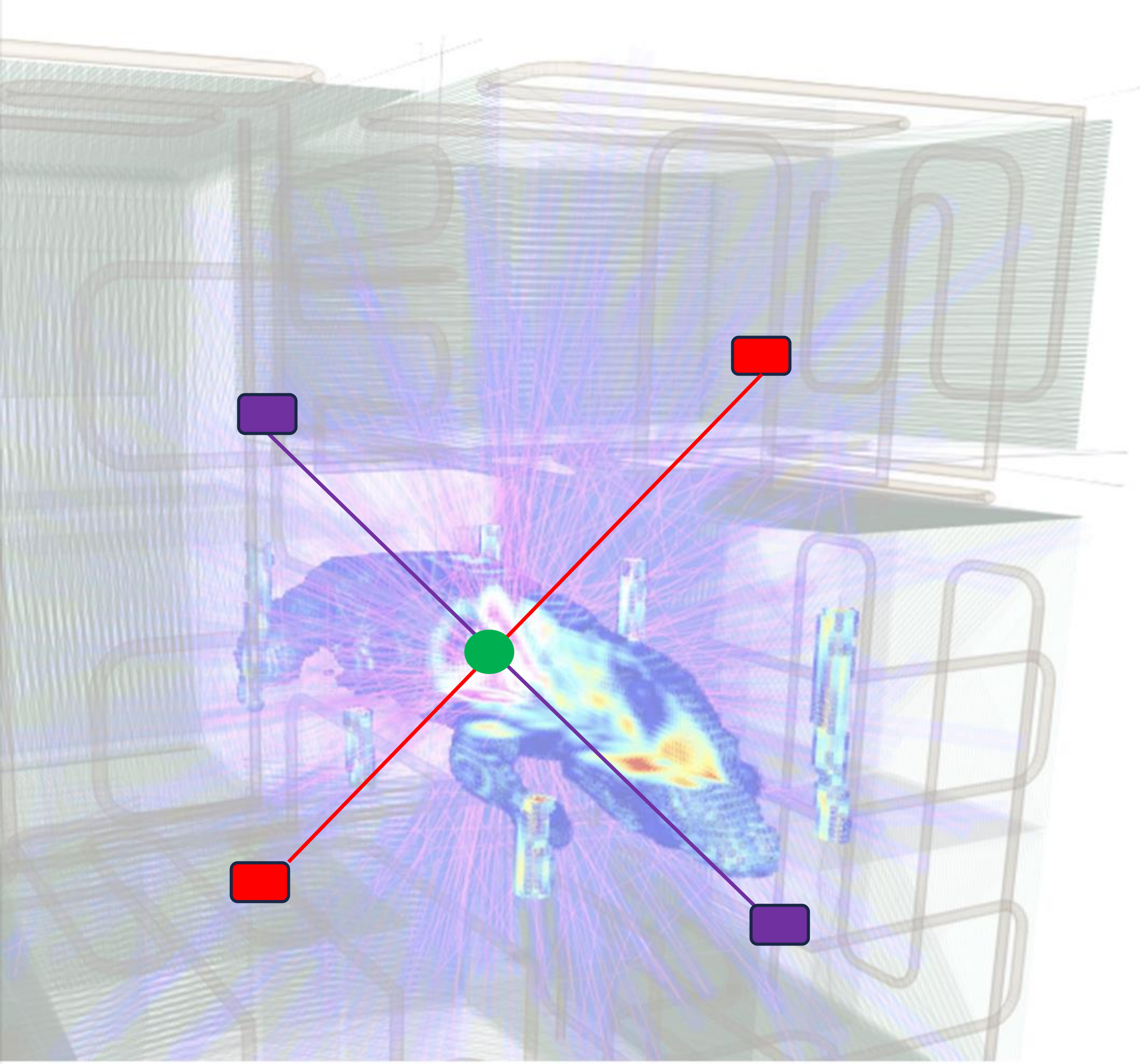

- Radiotracer injected into the body
- Cells with abnormal metabolic behavior will show an excess of radiotracers
- Positron emission -> e- e+ annihilation
- Detect 2 back-to-back Gamma at 511 keV
- Reconstruct image from Line of Response (LoR)

Image quality and Acquisition time:

- Spatial Resolution
- Noise event rate vs. True coincidence rate
- -> Small time window and low jitter

Atherosclerosis plaques in mouse
Pre-clinical scanner

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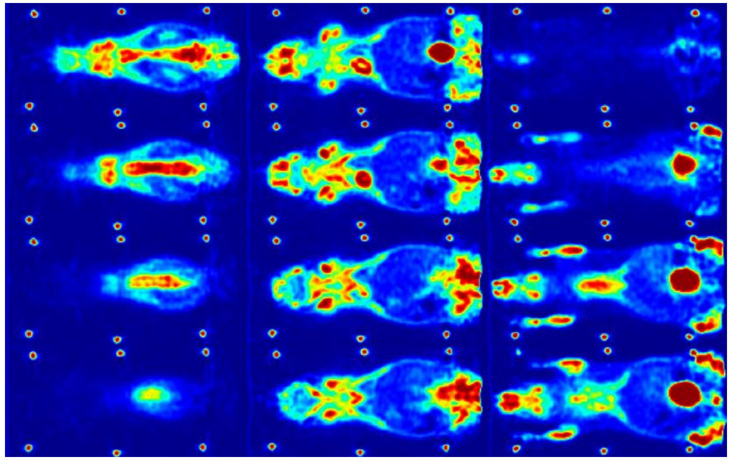
Murine Atherosclerosis case study

Mouse phantom derived from Digimouse PET combined with an atherosclerotic plaque from microCT data.

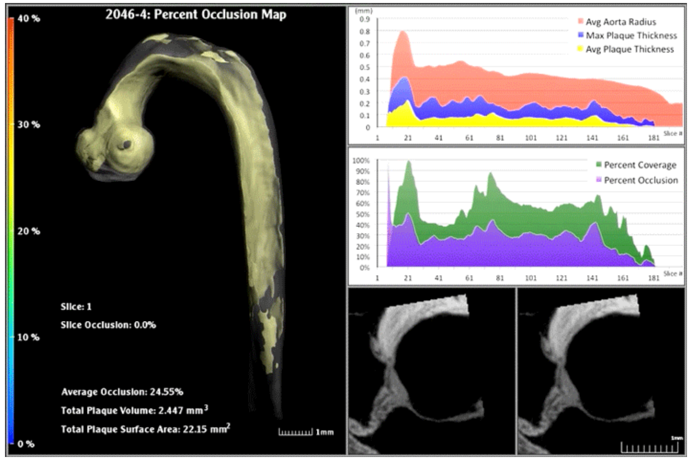
30 MBq Injected activity, 45 mL mouse volume while the plaque's 0.006 mL.

20 min acquisition = 1.4×10^{11} background and 8.4×10^{8} signal annihilations.

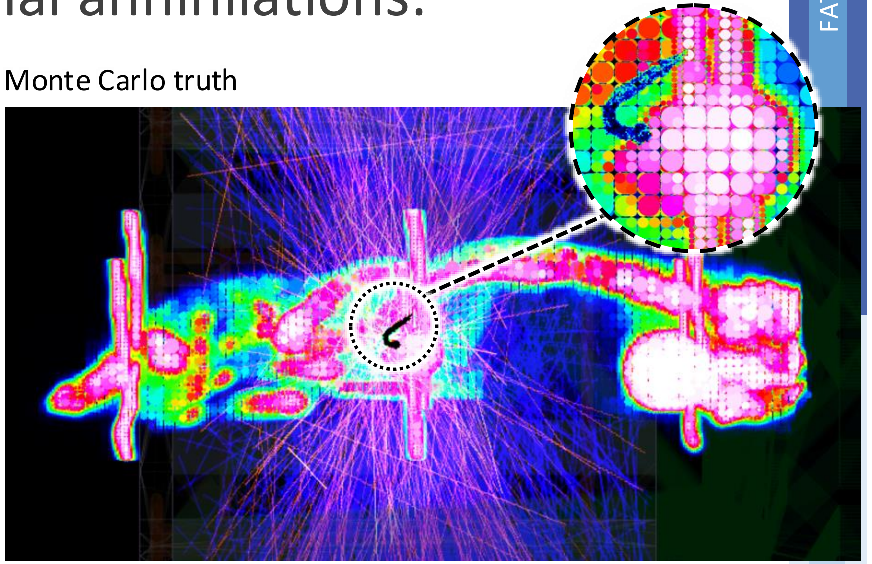
Digimouse PET dataset



microCT of atherosclerotic plaque



Monte Carlo truth



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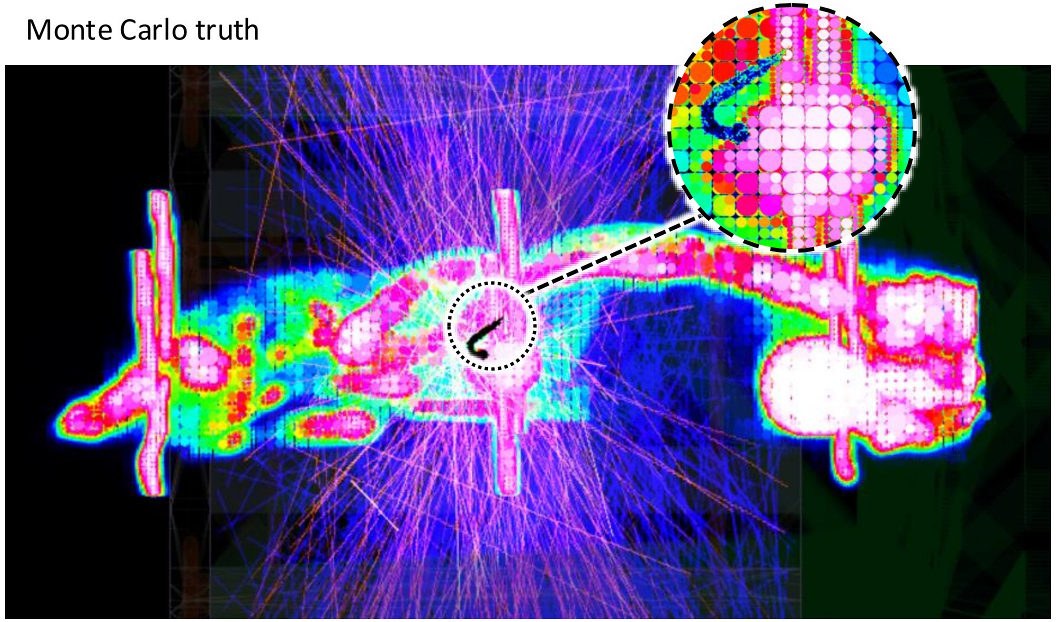
Murine Atherosclerosis case study

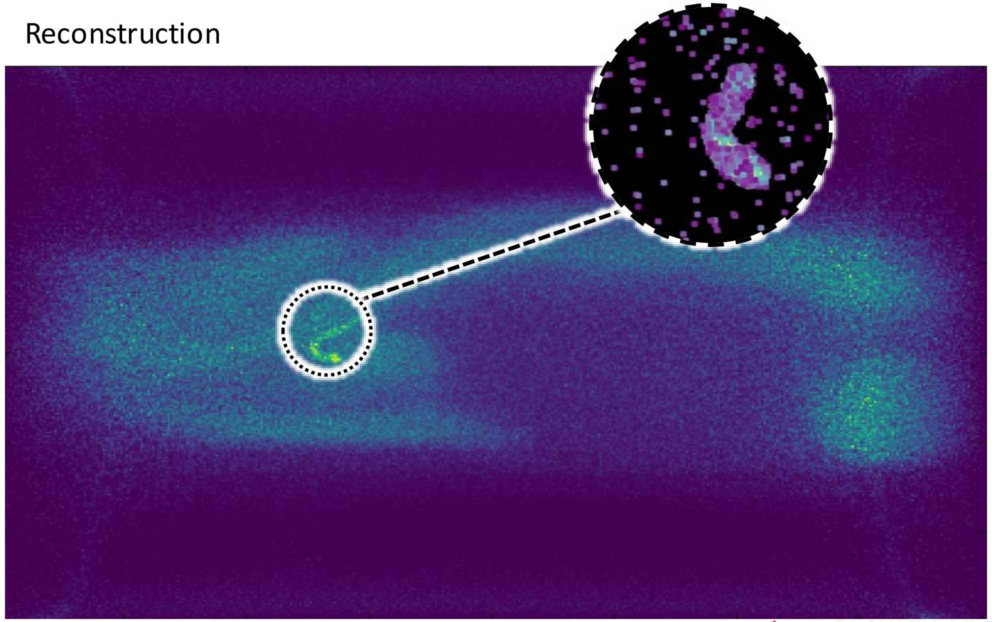
The plaque is visible after performing axial slice of reconstructed mouse.

Timing noise is neglected (No random coincidences are present)

Monte Carlo truth



Reconstruction



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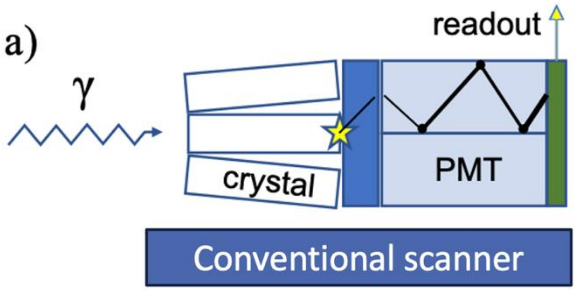
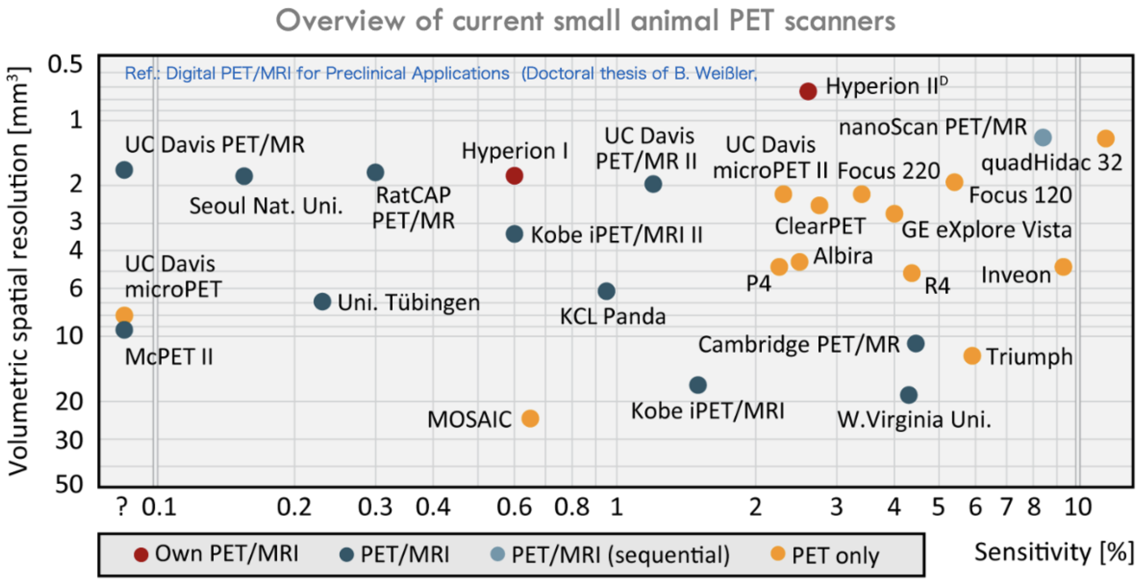
Best **pre-clinical small animal** scanner combine MRI – CT with PET to achieve resolution of **0.5mm³**





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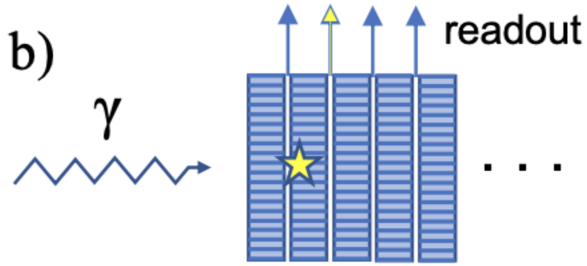
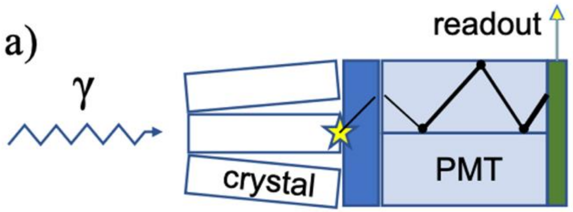
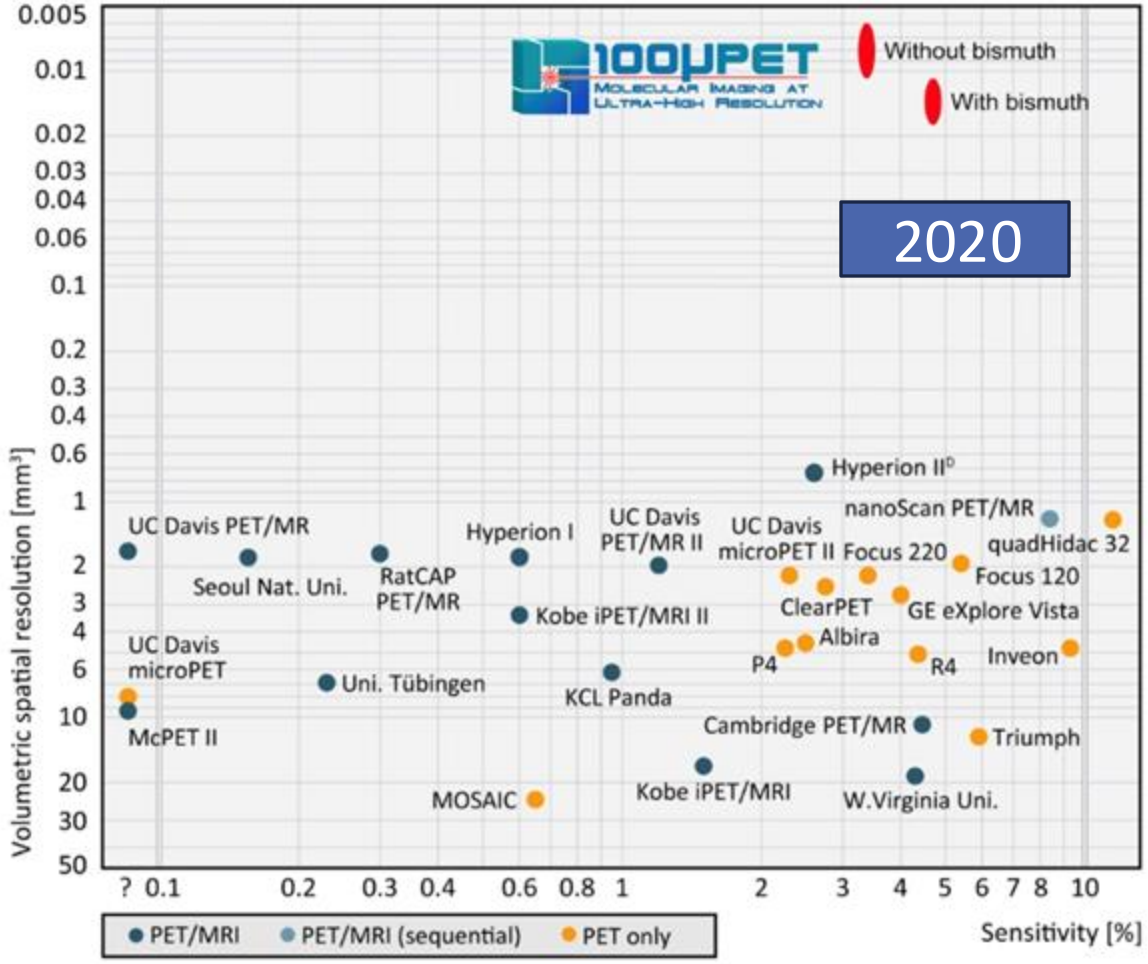


Our proposal (MAPS)
1 order of magnitude better!

Best **pre-clinical small animal** scanner combine MRI – CT with PET to achieve resolution of **0.5mm³**



Conventional scanner



DOI: 10.1109/TRPMS.2024.3456241

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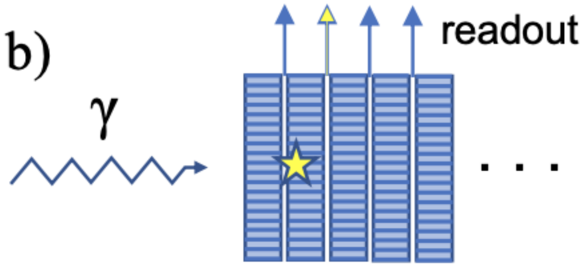

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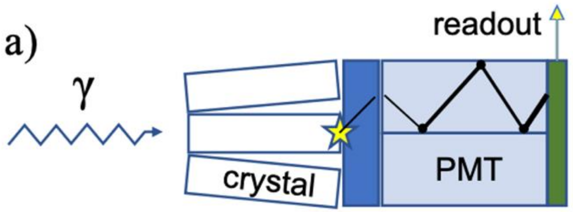
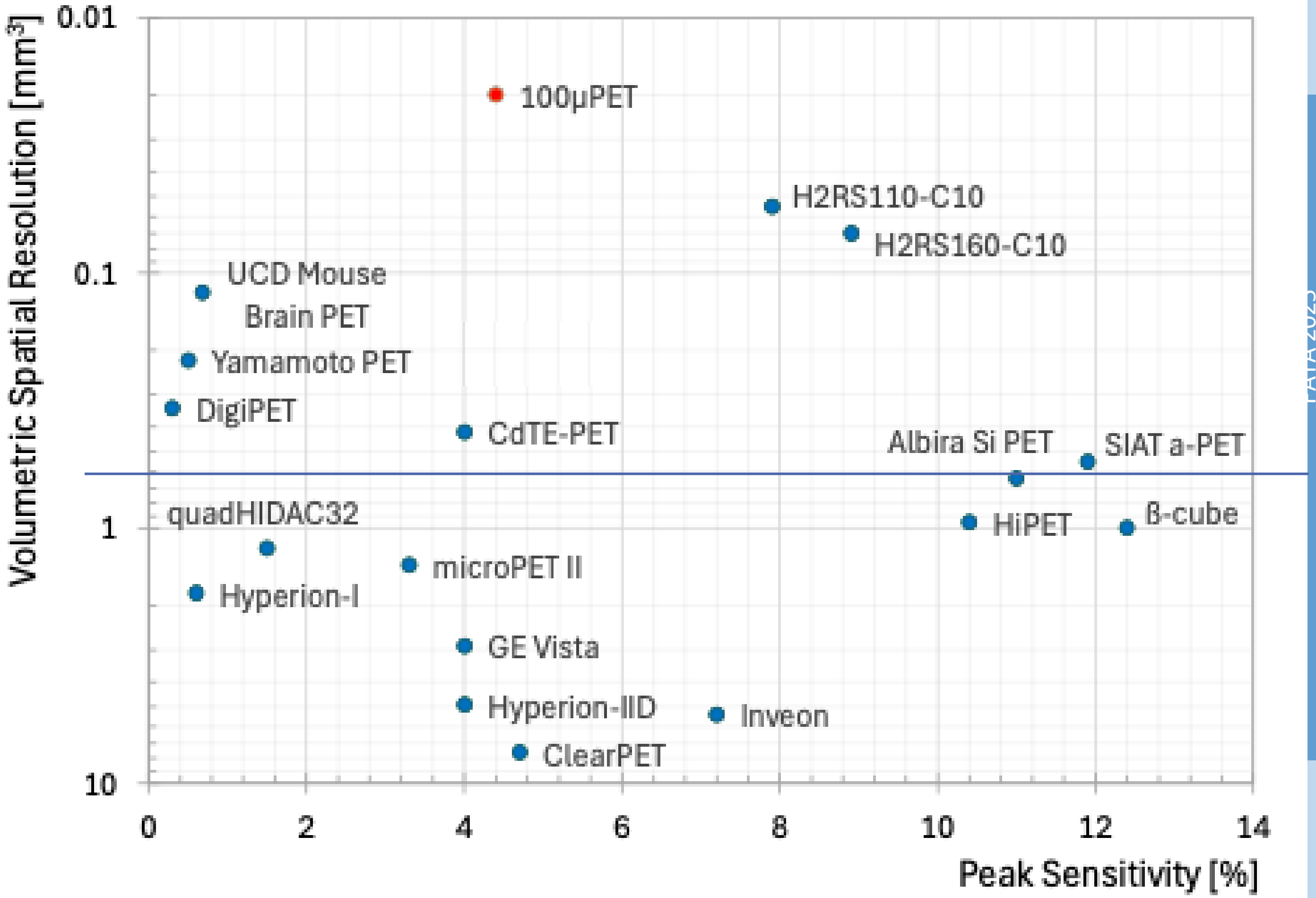


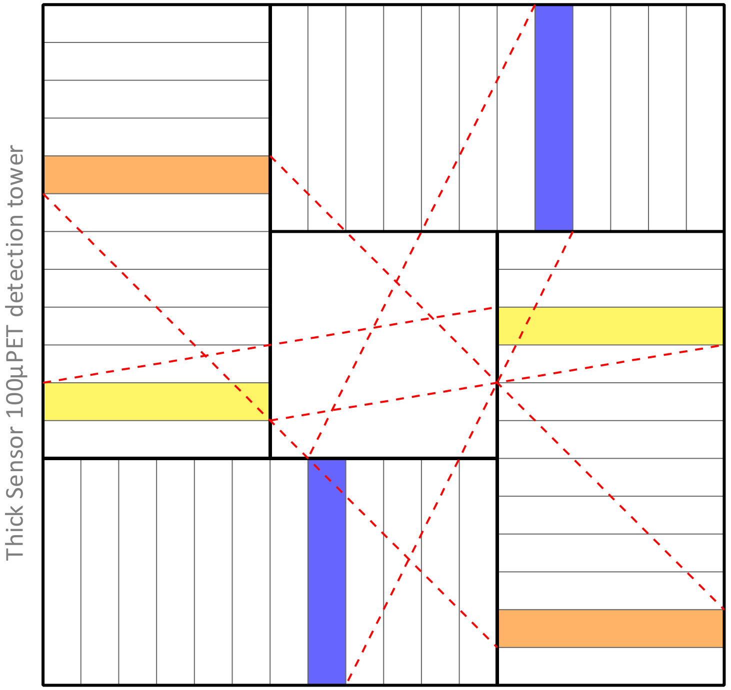
Conventional scanner

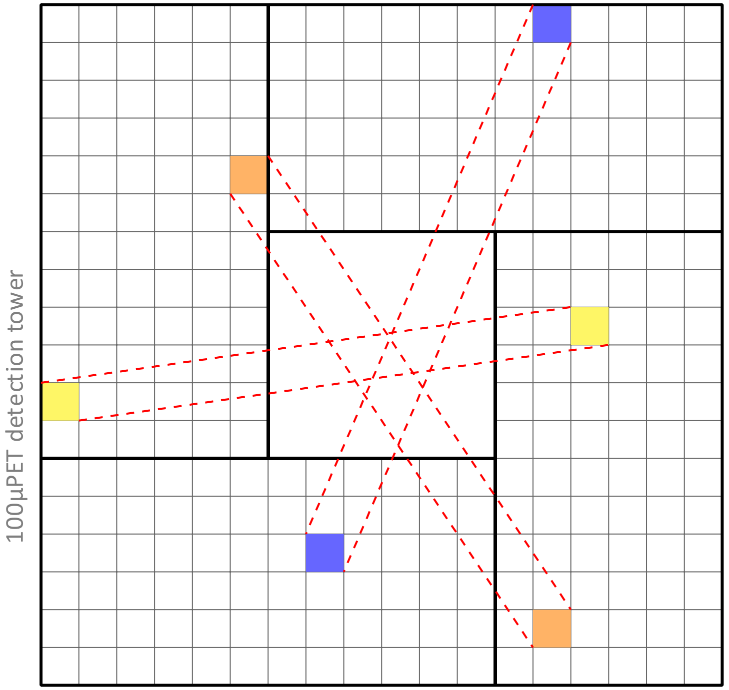


DOI: 10.1109/TRPMS.2024.3456241

Key for ultra-high resolution imaging

smaller detector volume = smaller overlapping volume





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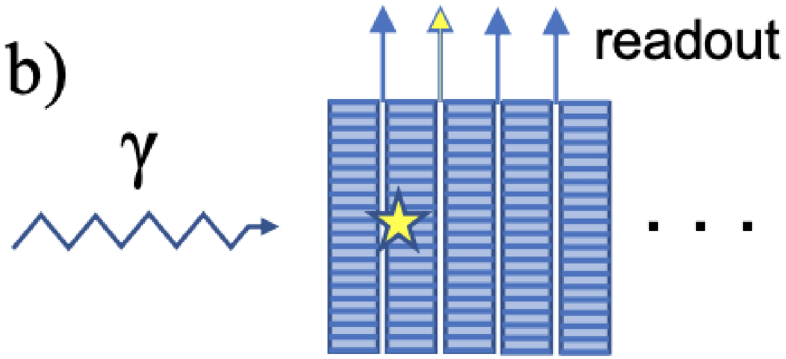

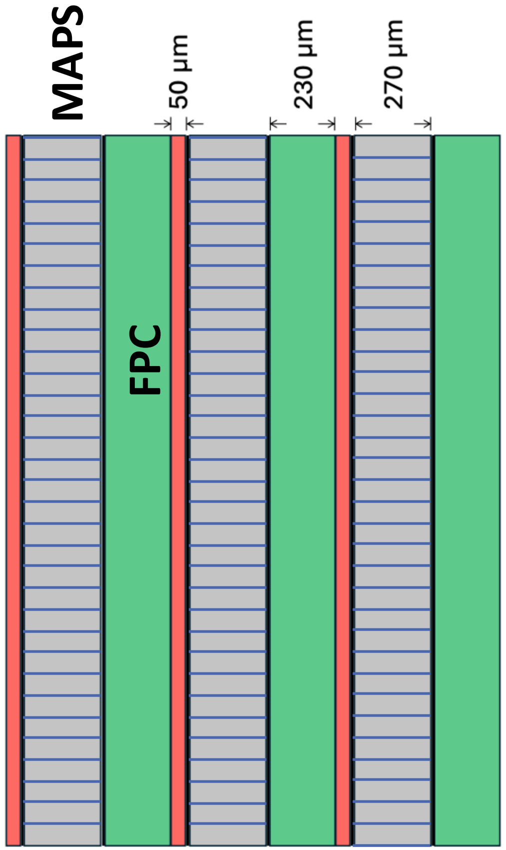

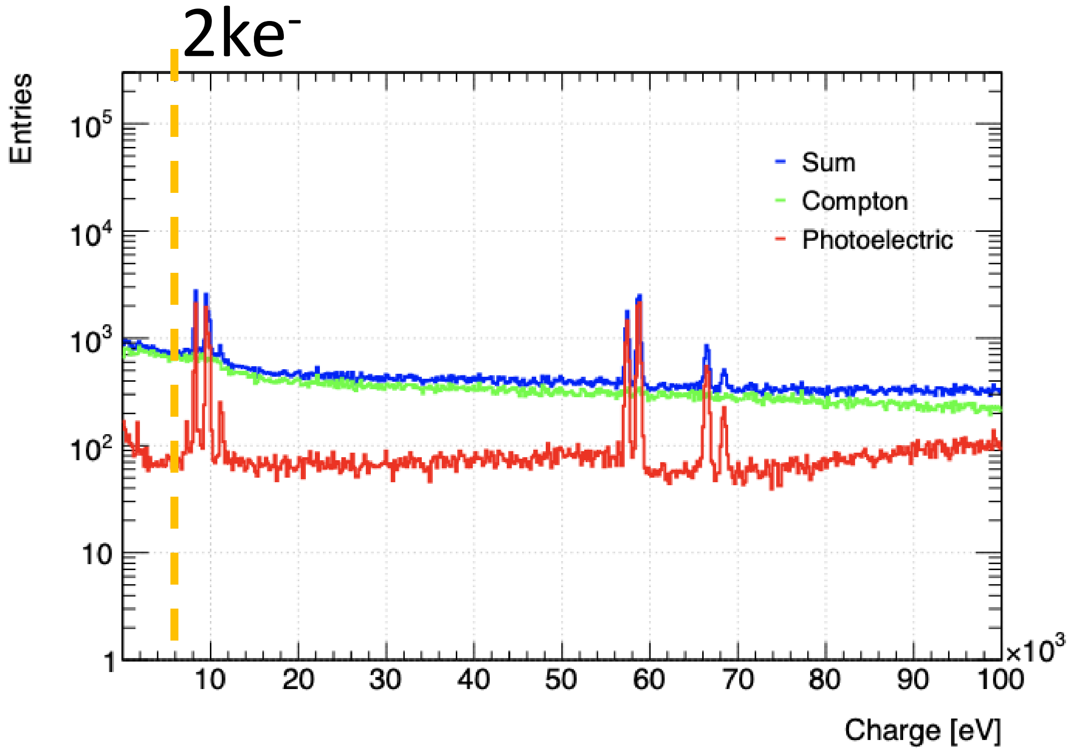

FIGURE 5.9: Total cluster charge spectra reported for the scanner configuration with 50 µm tungsten absorber layer between 0 and 100 keV.

Monolithic Active Pixel Sensors
Flexible Printed Circuit
High Z absorber (orange)

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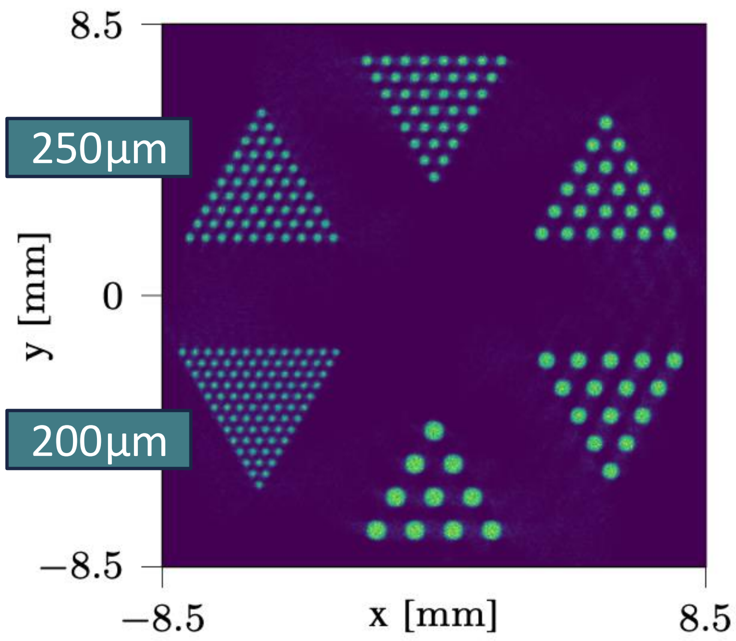
How far can we bring down the spatial resolution?

How far we can go?

100µm pixel pitch



No acollinearity,
No positron range,
$p = 0.1$ mm, no bismuth,
reconstructed with OSEM

No uncertanty in Gamma emission process

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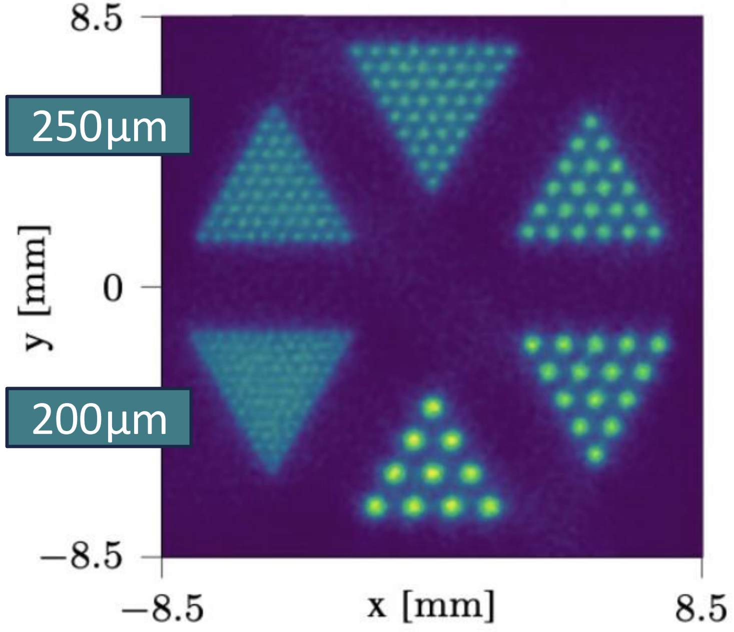
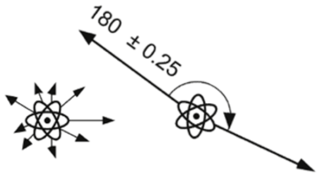
How far we can go?

100µm pixel pitch



Positron range: 102µm FWHM for F18

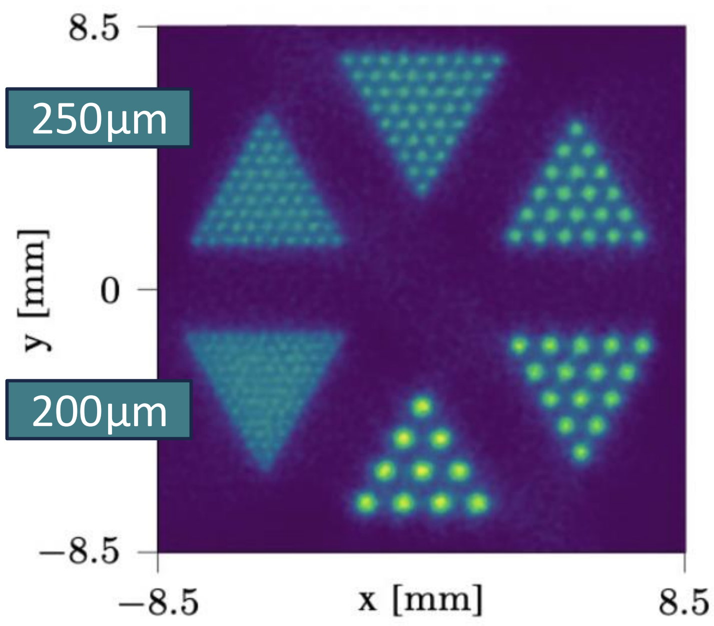
Acolinearity: $90\mu m \approx 4 \cdot 10^{-3} R$

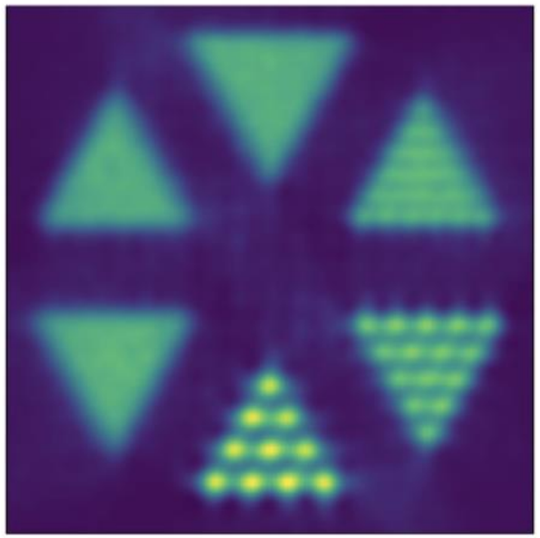


How far we can go?

100µm pixel pitch

Reference scanner

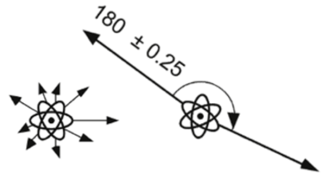




Reference scanner ~ state of the art

Positron range: 102µm FWHM for F18

Acolinearity: $90\mu m \approx 4 \cdot 10^{-3} R$



Large improvement with respect to reference scanner

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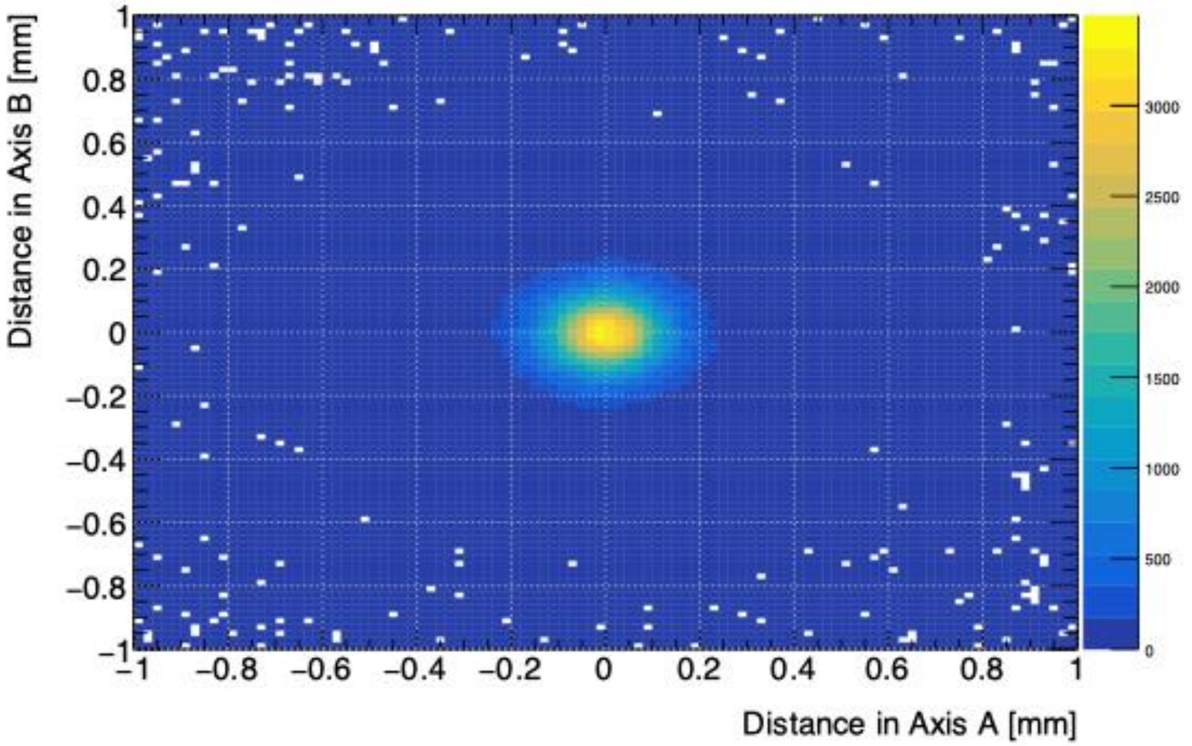
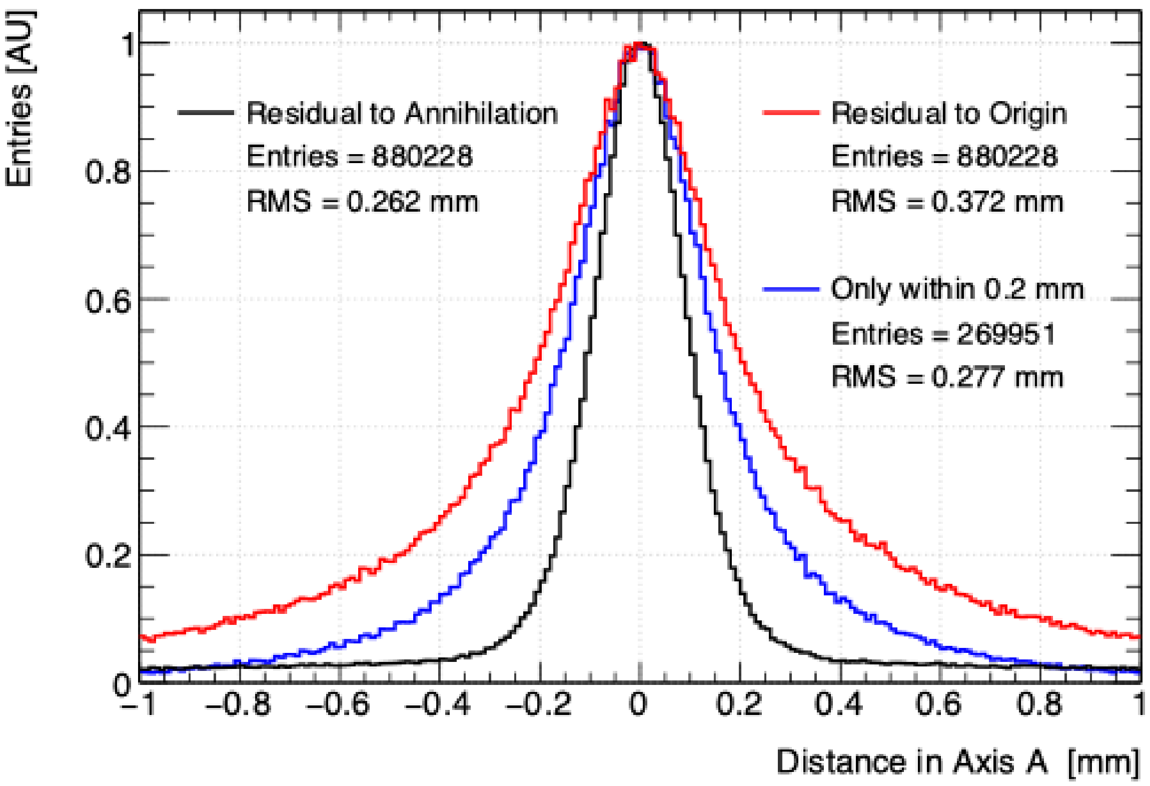
Line of Response Residuals Distribution





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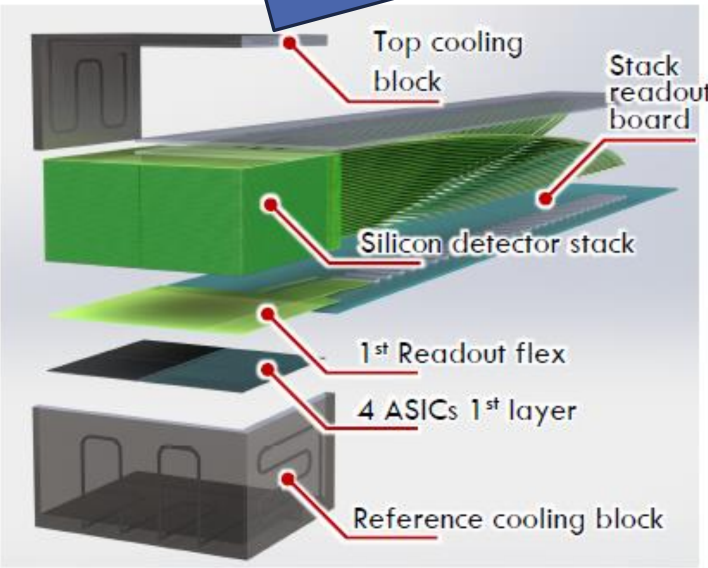
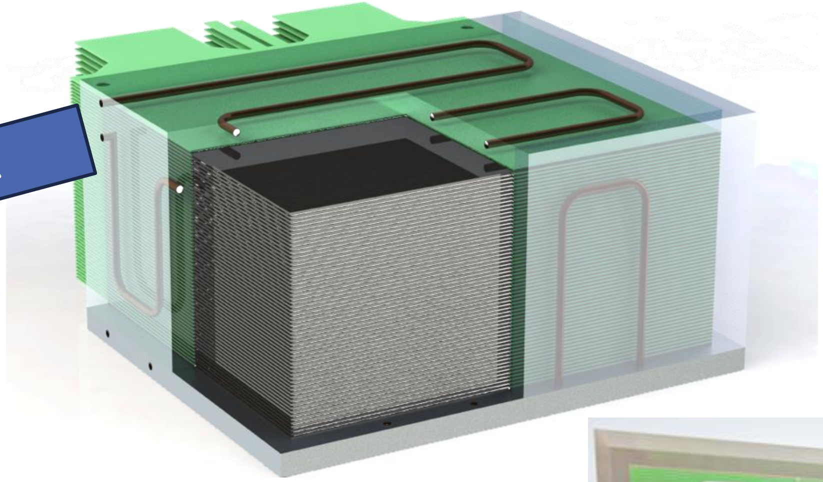
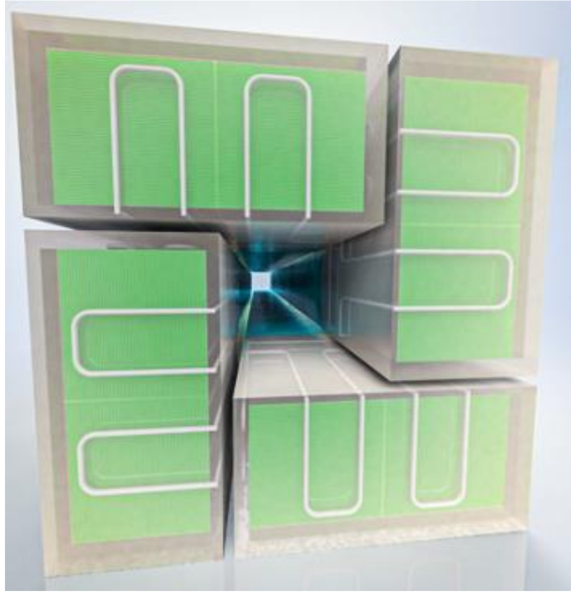
Tower: 60 quad-module layers (240 chips)

Trade-off Sensitivity / Cost





100μPET Scanner:
4 towers (960 chips)



F. Cadoux et al.

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The 100μPET ASIC

Specifications for the ASIC

Event size	1 cluster (< (5x5) pixels)
Event rate	10 kHz/cm^2
Equivalent Noise Charge (ENC)	~250 e-
Operation Threshold	**[2000 / 3000] e-**
Time resolution RMS (Qin > 7 ke-)	**200 ps**
ToA	**Yes, seed pixel**
ToT	**Yes, for time-walk correction**
Power consumption	< 100 mW/cm^2
Pixel pitch	150 µm

~7.2kev ~10.8kev

CMOS monolithic sensor in IHP SG13G2 BiCMOS, **130 nm** process featuring **SiGe HBT**

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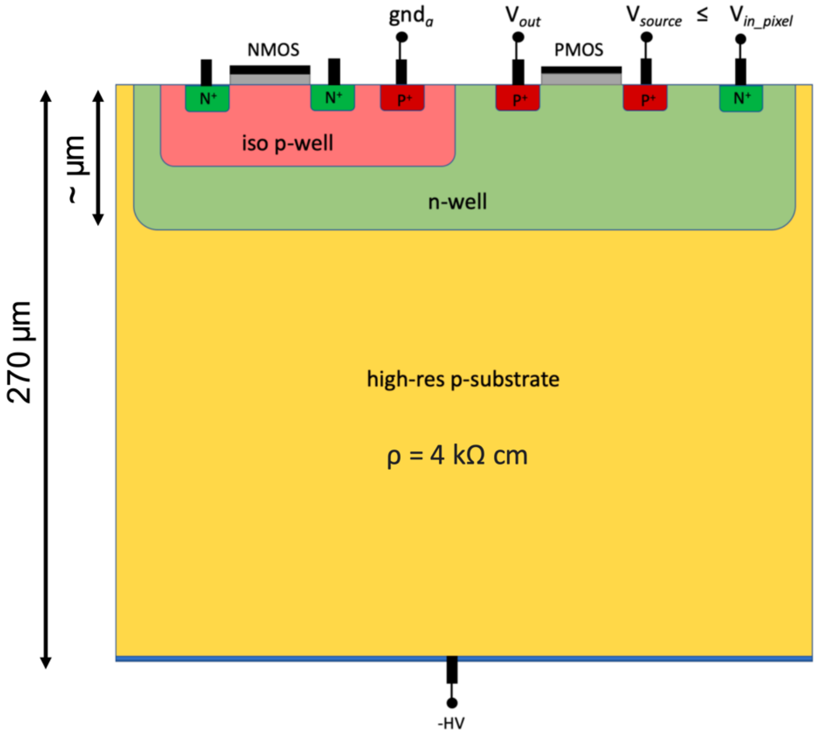
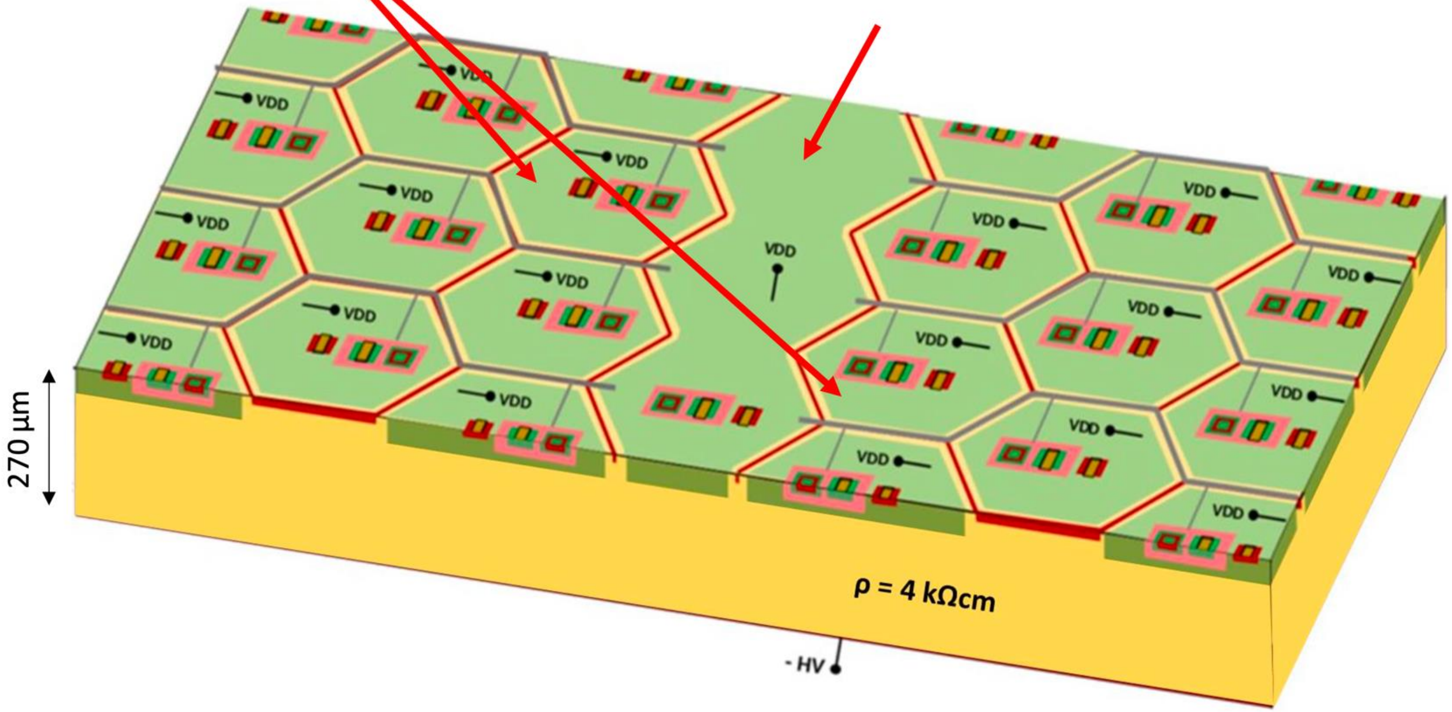
What are Monolith active pixel sensors ?



Analog electronics in pixel electrode deep-nwell (100% sensitive region)

Digital electronics placed in a separate deep-nwell to improve noise robustness (non-sensitive region)



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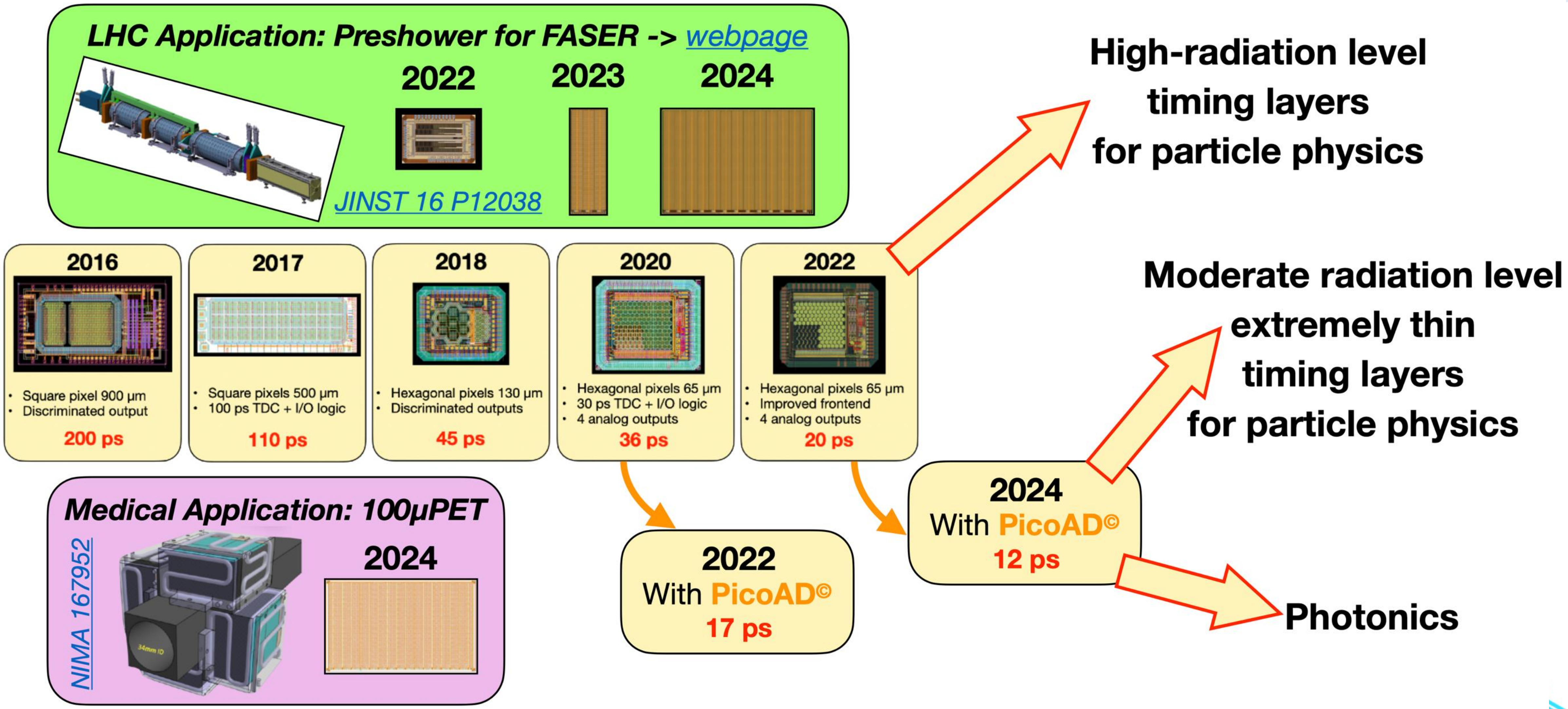
MAPS at the university of Geneva



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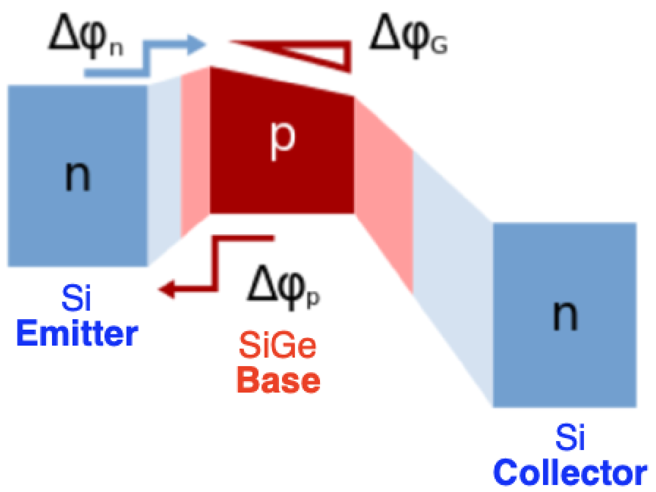
SiGe BiCMOS Front-End Electronics

NPN SiGe HBT
(depleted regions in light colors)
from wikimedia



SiGe HBT = BJT with Germanium as base material.

Grading of Ge doping in base:

- Charge-transport in base via **drift**
  - reduced charge-transit-time in base
  - high current gain β
- **High doping** in base is possible:
  - thinner base
  - reduced base resistance R_b

$$ENC_{series\,noise} \propto \sqrt{k_1 \frac{C_{tot}^2}{\beta} + k_2 R_b C_{tot}^2}$$

IHP SG13G2 technology,
130 nm process featuring **SiGe HBT**

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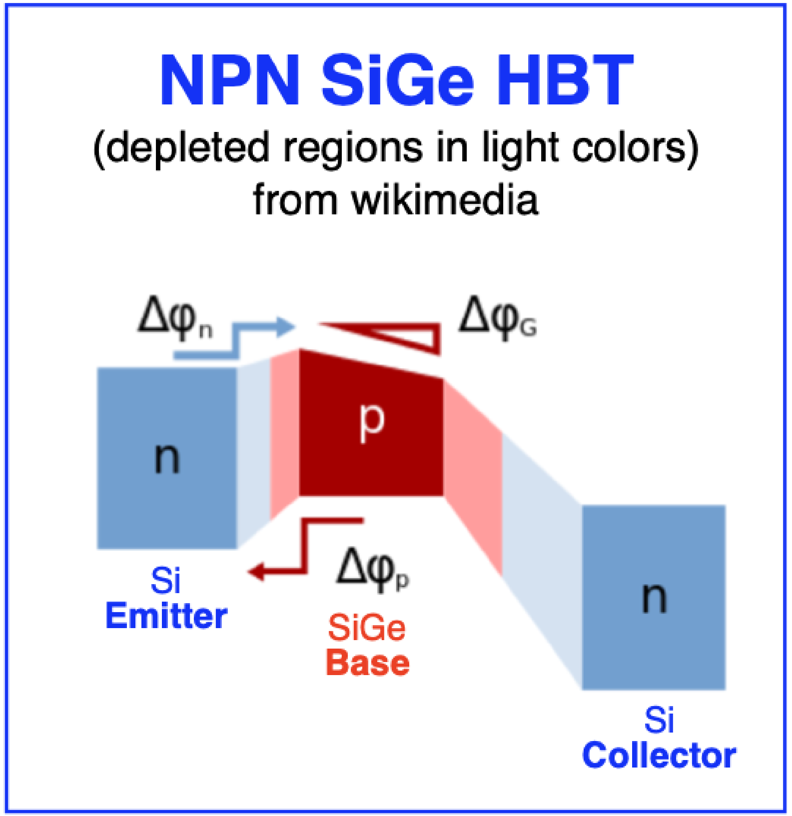
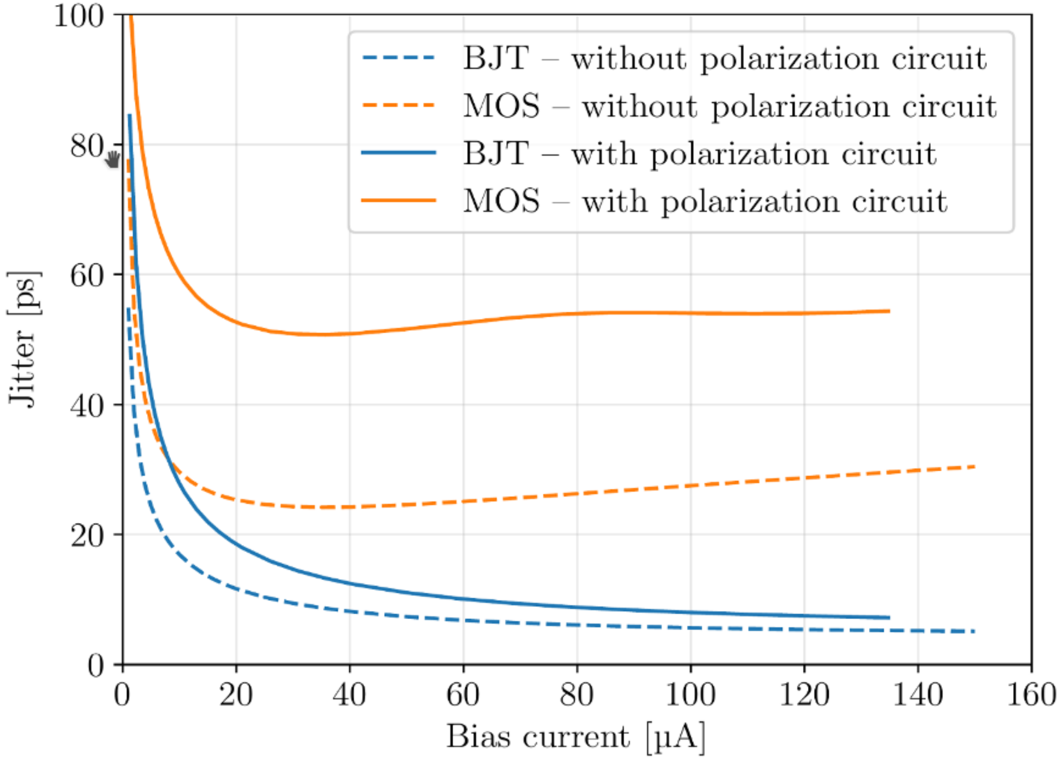
SiGe BiCMOS Front-End Electronics

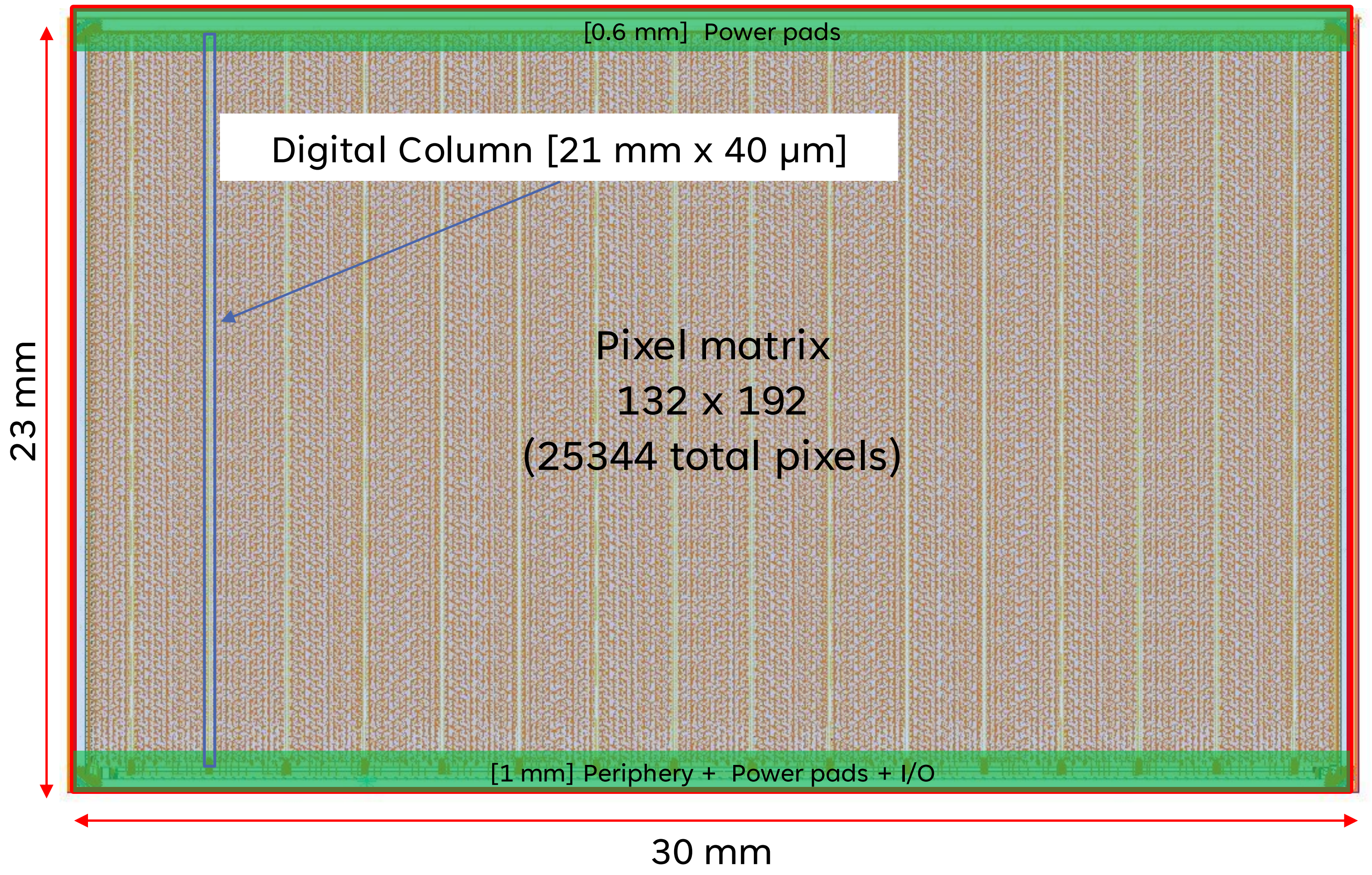


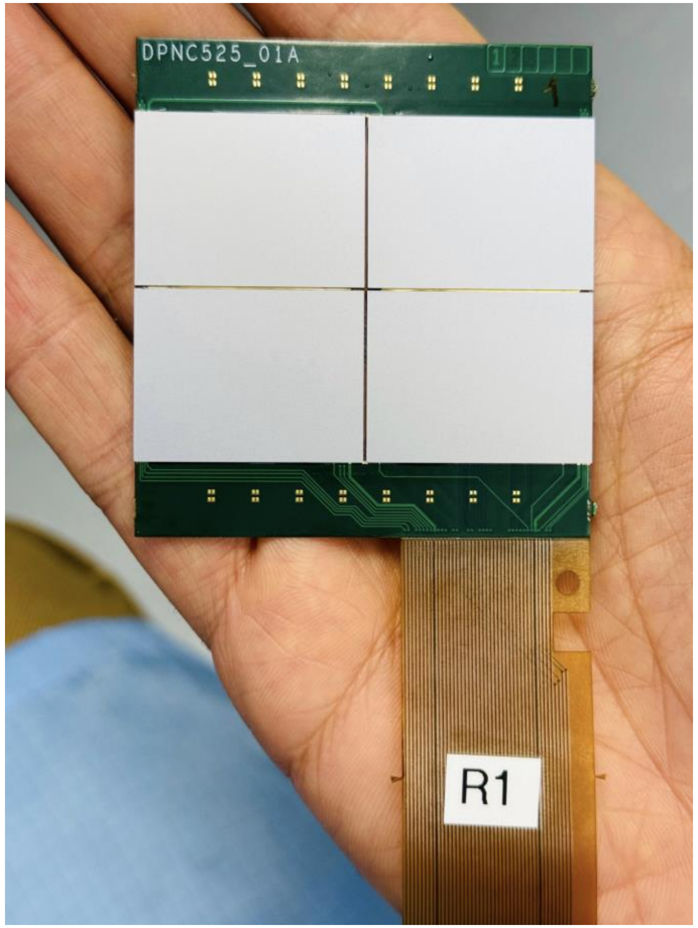
Intrinsic **amplifier jitter**:
common emitter (source) configuration
in a 130nm technology



L. Paolozzi et al.,
Time resolution and power consumption of a monolithic silicon pixel prototype in SiGe BiCMOS technology, JINST 15 (2020) P11025, https://doi.org/10.1088/1748-0221/15/11/P11025

Chip overview





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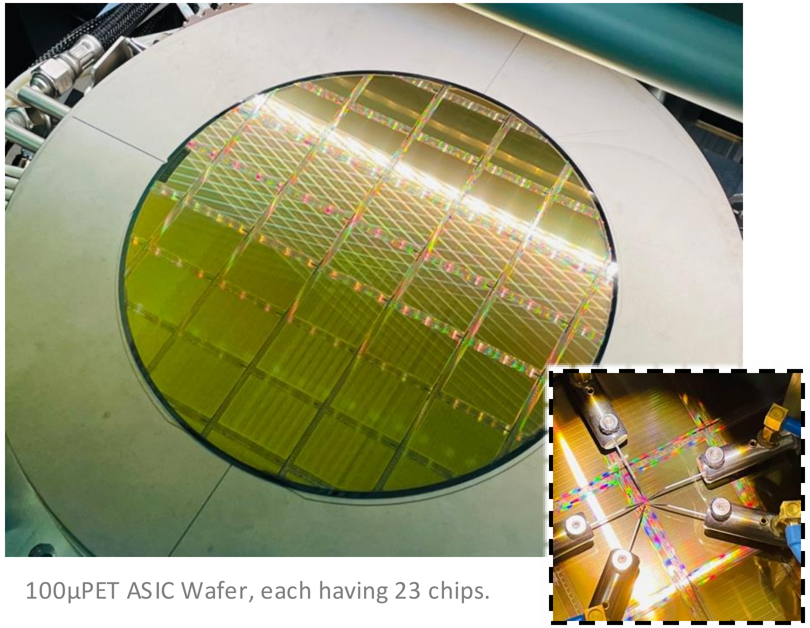
Chip Testing

First production wafers received in November 2024.

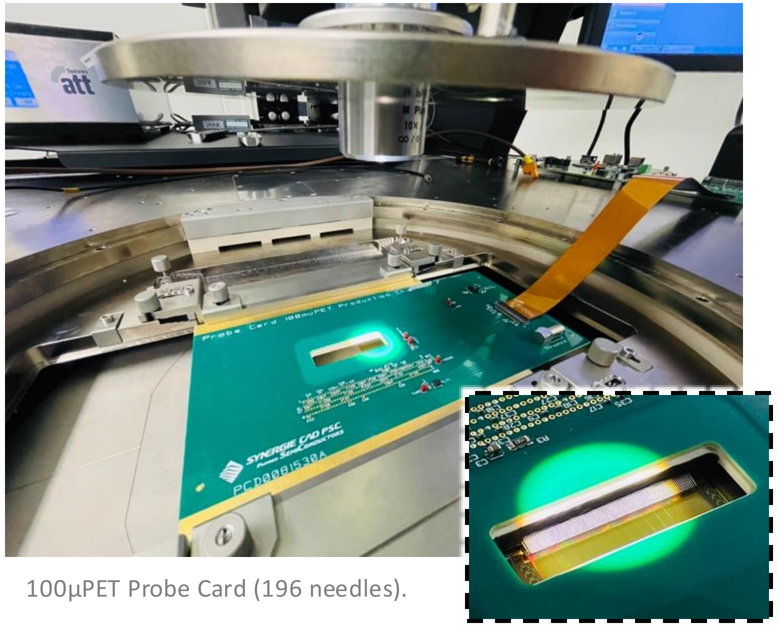
Electrical testing ongoing: sensor shows leakage current (no depletion),

Front-end electronics testing: normal operation

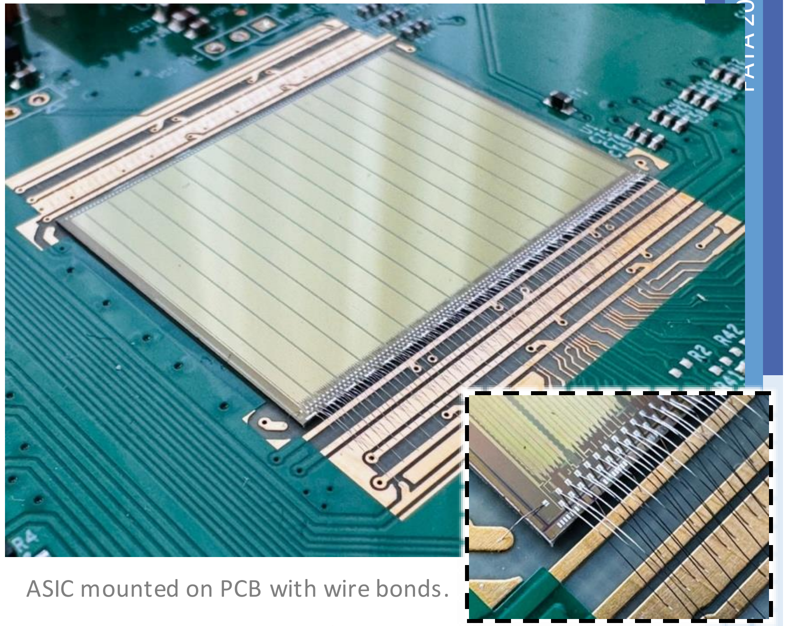
.



100µPET ASIC Wafer, each having 23 chips.



100µPET Probe Card (196 needles).



ASIC mounted on PCB with wire bonds.

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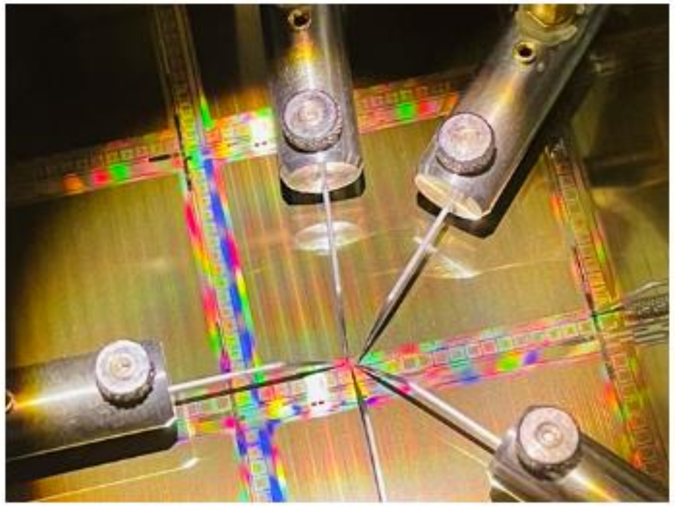
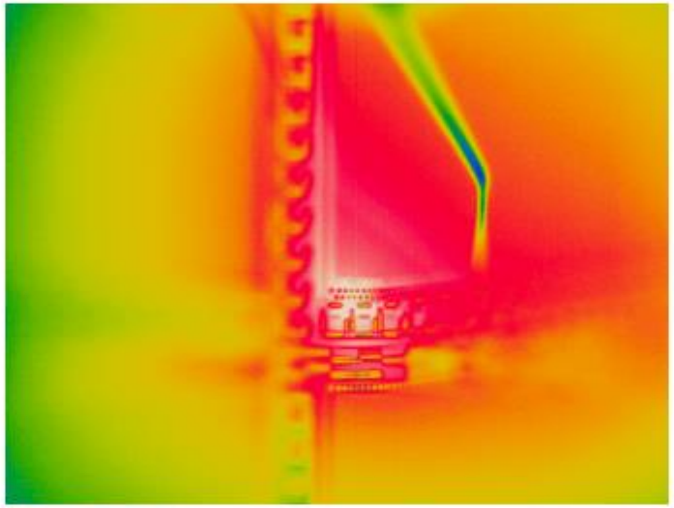
Engineering run production





First batch delivered in november 2024
Produced in the target 4kΩ substrate

Sensor seems to be damaged
Already at -1V bias, very high current (>1µA) between substrate and wells.

Not caused by design ASIC as same failure in appears foundry test-structure
Foundry was able to reproduce failure on another design with same silicon substrate

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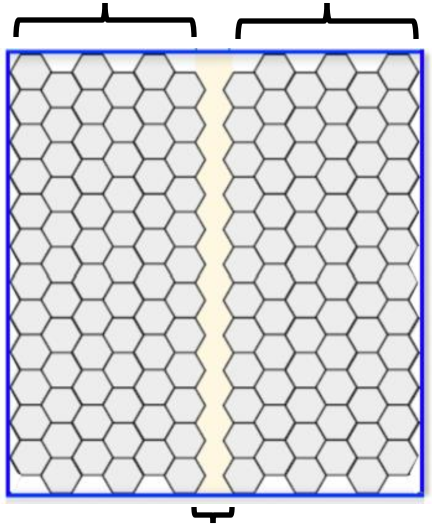
Chip architecture

Superpixel

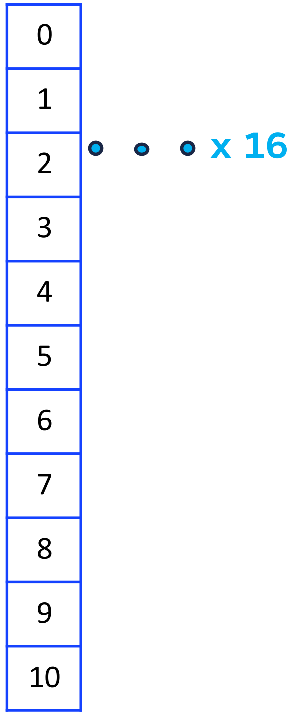


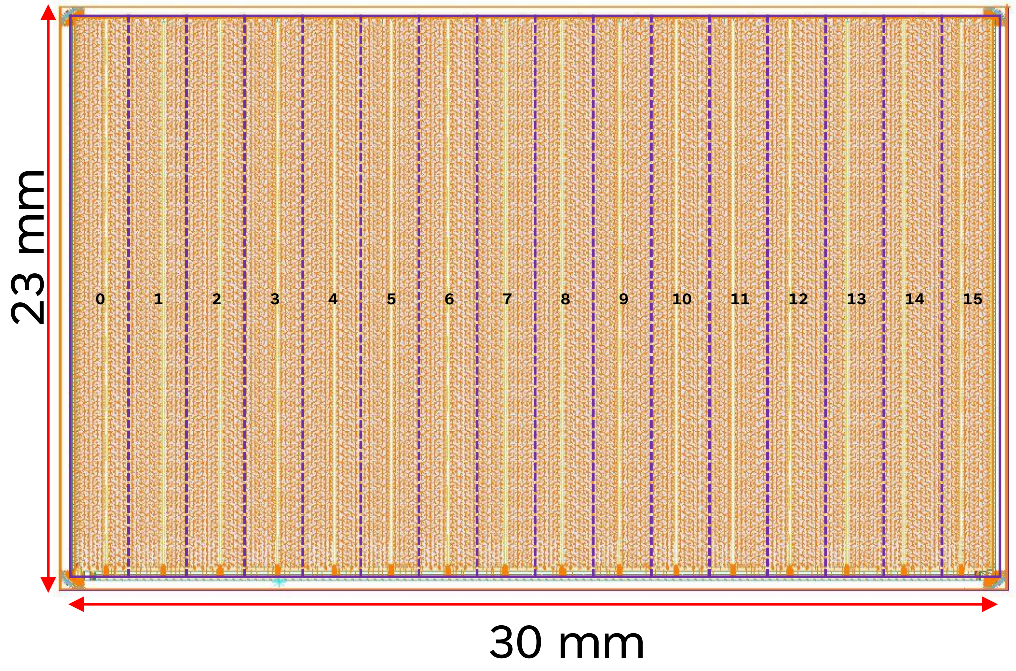
1 x 12 pixels
digital lines and configuration
(non-sensitive region)
1/13 of matrix area (7.7%)

x 11

Super Column

Super Colum
11 Super Pixels





Asynchronous 51-bit bus
No Clock inside the matrix

Digital Periphery

TDCs, DACs, Bandgap, LVDS drivers, config registers

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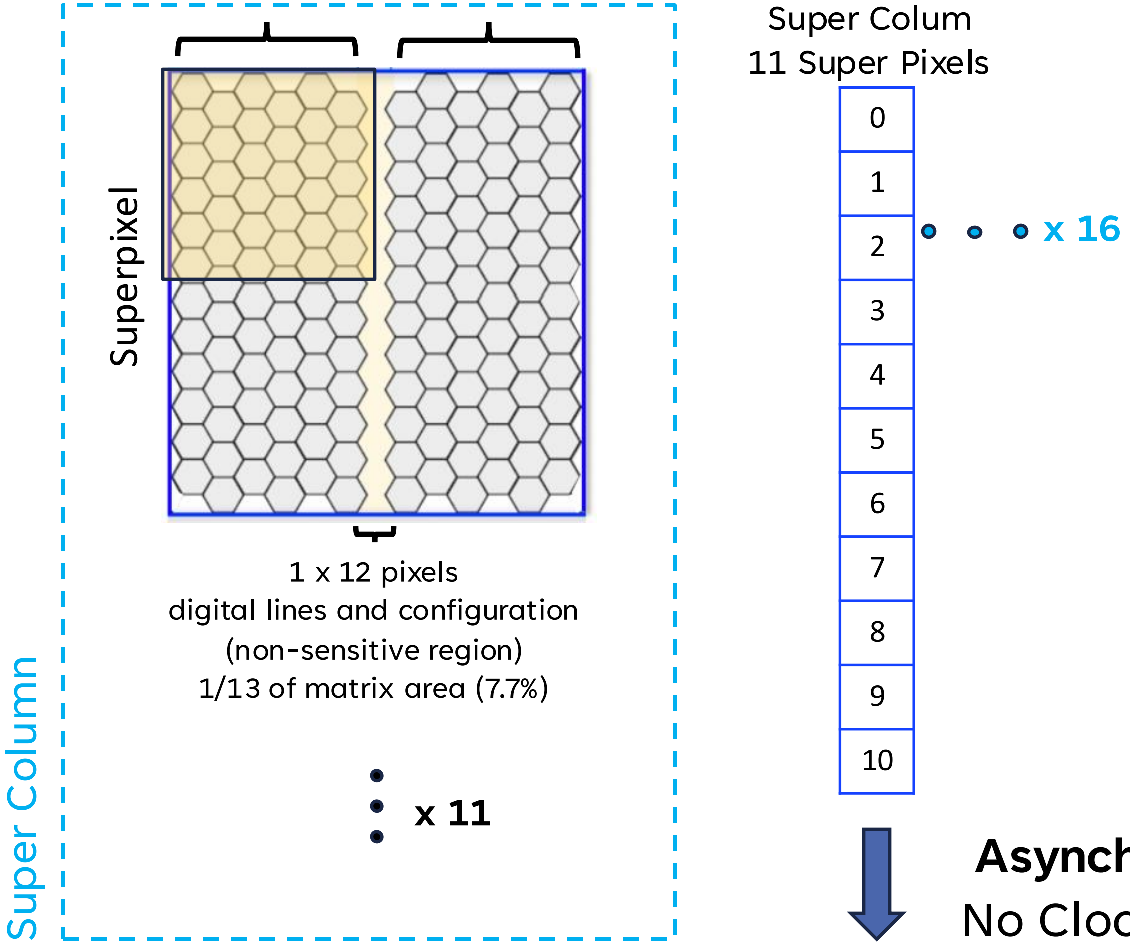
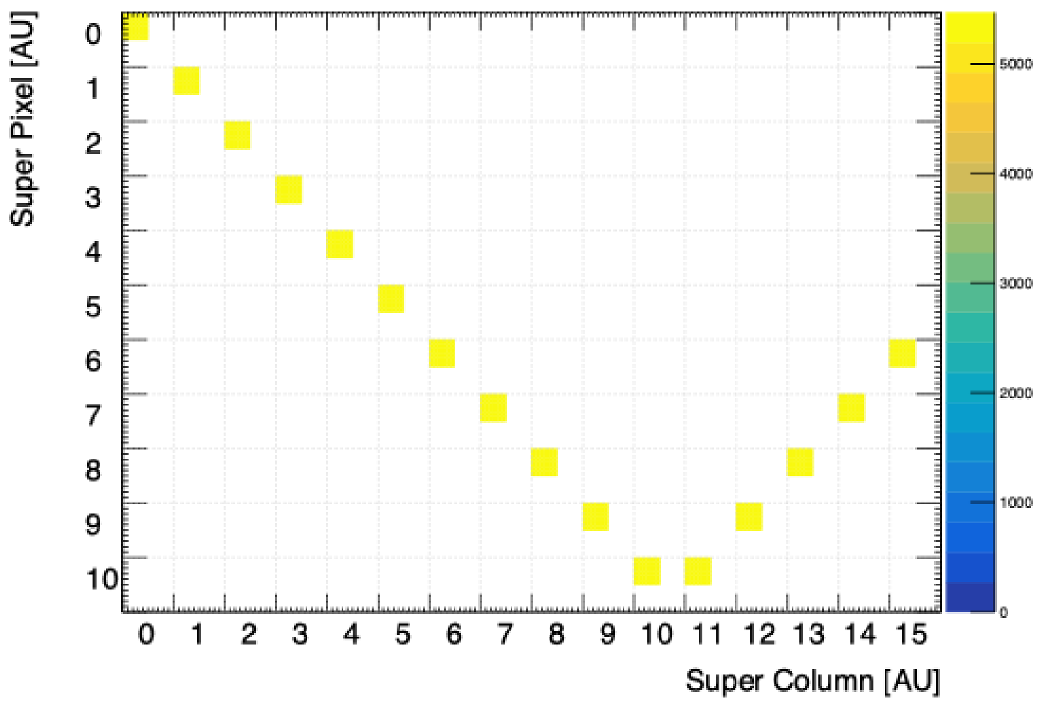
Chip architecture





Asynchronous 51-bit bus
No Clock inside the matrix

Digital Periphery

TDCs, DACs, Bandgap, LVDS drivers, config registers

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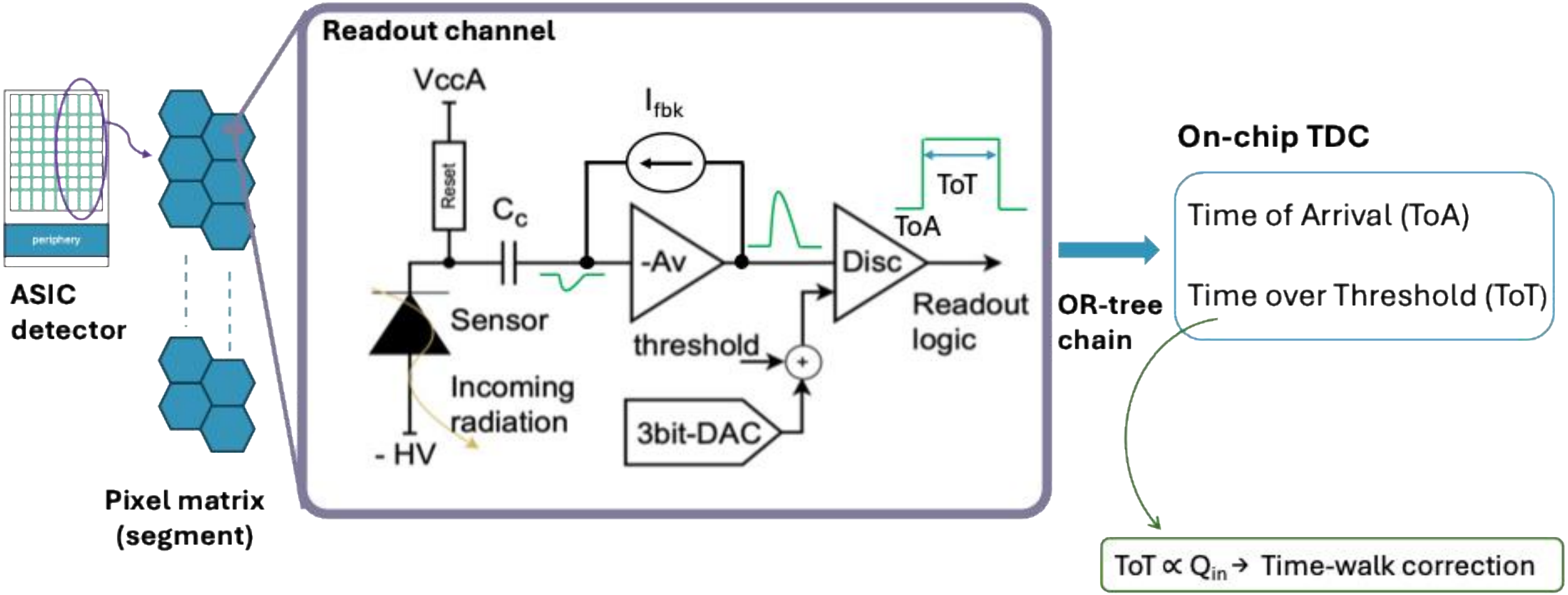
Front-End



A. Picardi et al.

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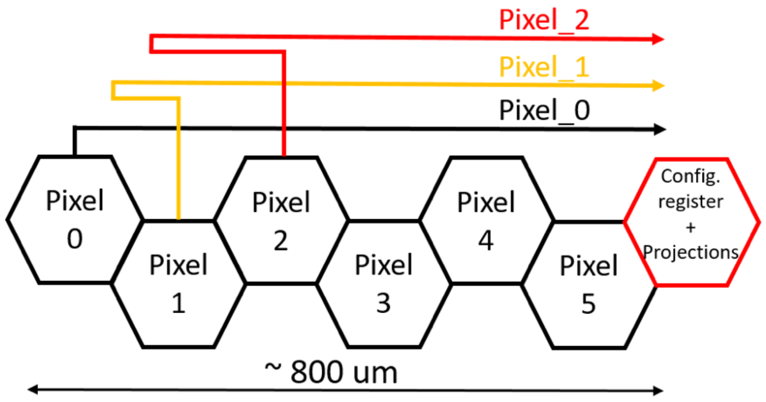
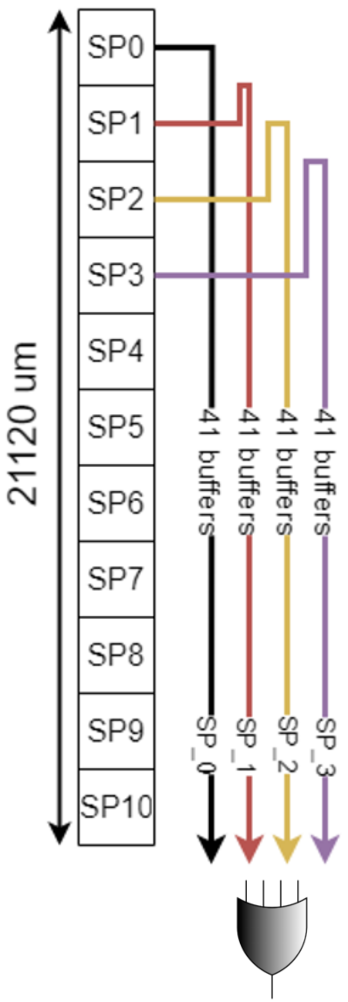
Optimized timing path to TDC

Delay line matching





TDC [LSB 150 ps]

Simulation results

Max skew	67 ps
Mismatch rms	11 ps
Jitter rms	0.5 ps
T. coeff.	0.6 ps/C
V. coeff.	7.3 ps/mV

No pixel-to-pixel delay calibration required

11 Super-Pixel output fast-OR

1 TDC channel/Super Column

L. Iodice et al.

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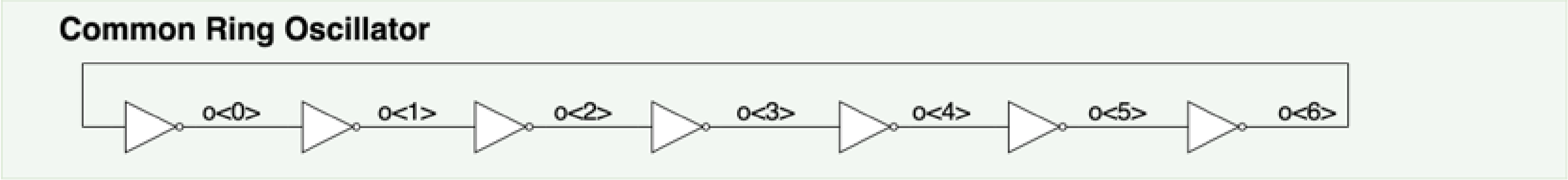
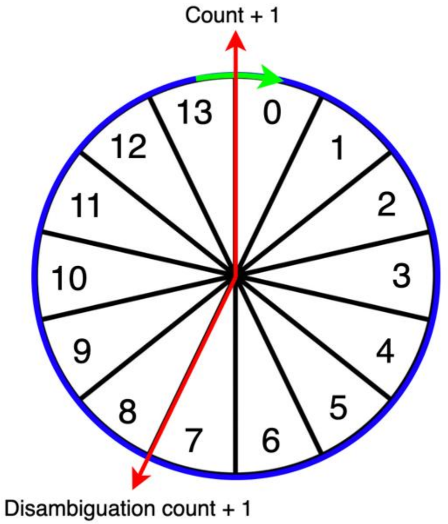
TDC





Fine time measurement states encoding

	Encoded states													
Time	0	1	2	3	4	5	6	7	8	9	10	11	12	13
o<0>	1	1	1	1	1	1	1	0	0	0	0	0	0	0
o<1>	1	0	0	0	0	0	0	0	1	1	1	1	1	1
o<2>	0	0	1	1	1	1	1	1	1	0	0	0	0	0
o<3>	1	1	1	0	0	0	0	0	0	0	1	1	1	1
o<4>	0	0	0	0	1	1	1	1	1	1	1	0	0	0
o<5>	1	1	1	1	1	0	0	0	0	0	0	0	1	1
o<6>	0	0	0	0	0	0	1	1	1	1	1	1	1	0

Supercolumn independent Flash-TDC with 7-stages free-running ring oscillator.

- States of the oscillator encode the fine-time: expected **LSB = 150ps.**
- Coarse timing with a counter on stage 0 and disambiguation bit on stage 1.
- **Reference** and **Calibration's** channel signals are generated per Supercolumn.
- Reference : Synchronization with DAQ for coincidence with an internal counter at readout clock frequency (50MHz).

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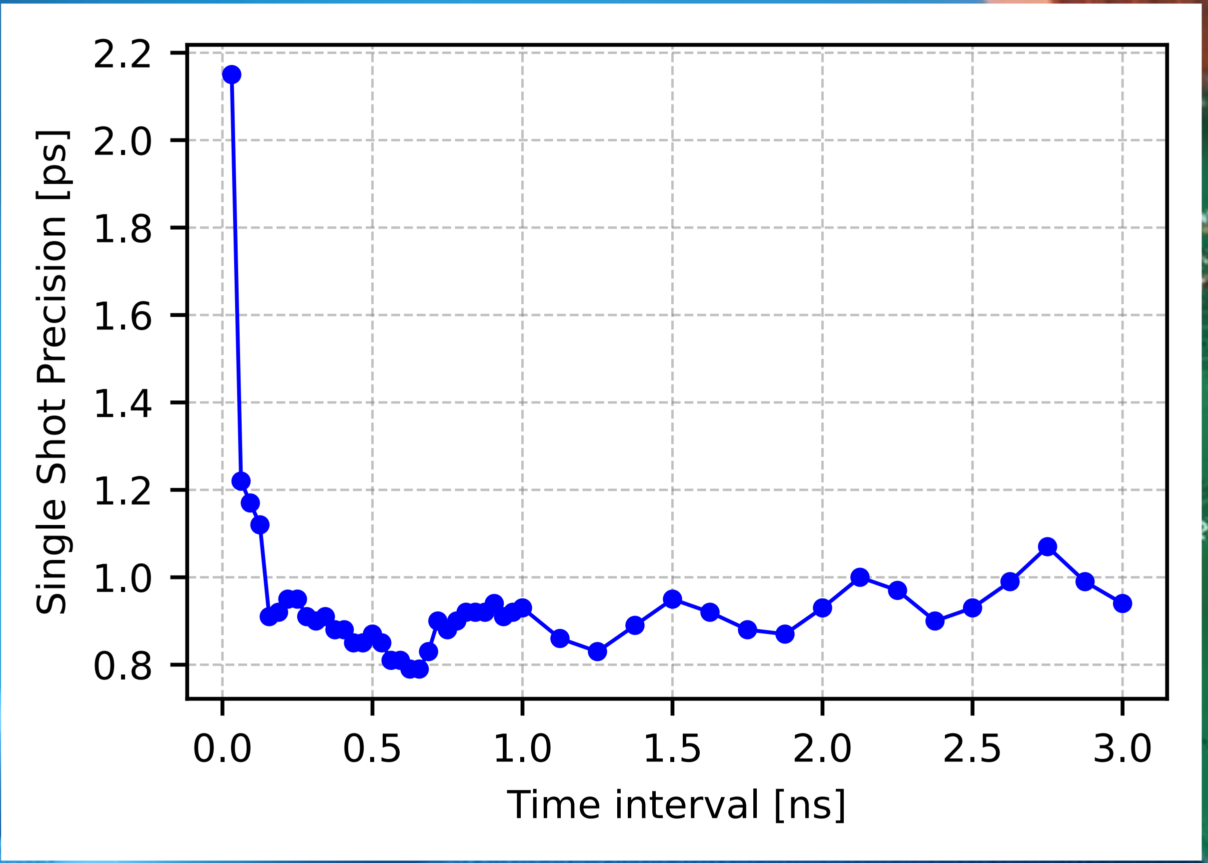
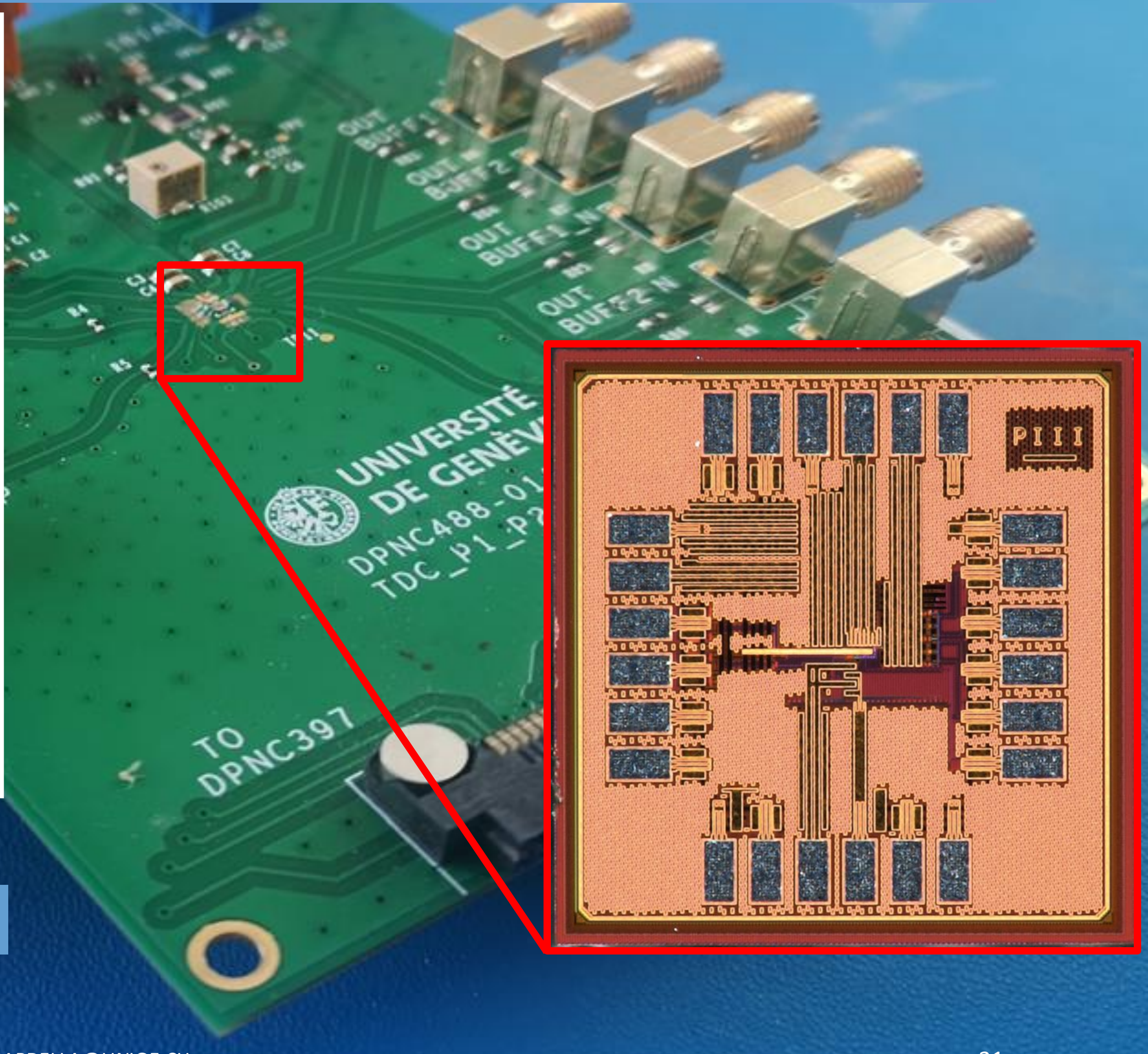
OFF Topic : Sub-picosecond TDC
Just published





https://doi.org/10.3390/s25175577

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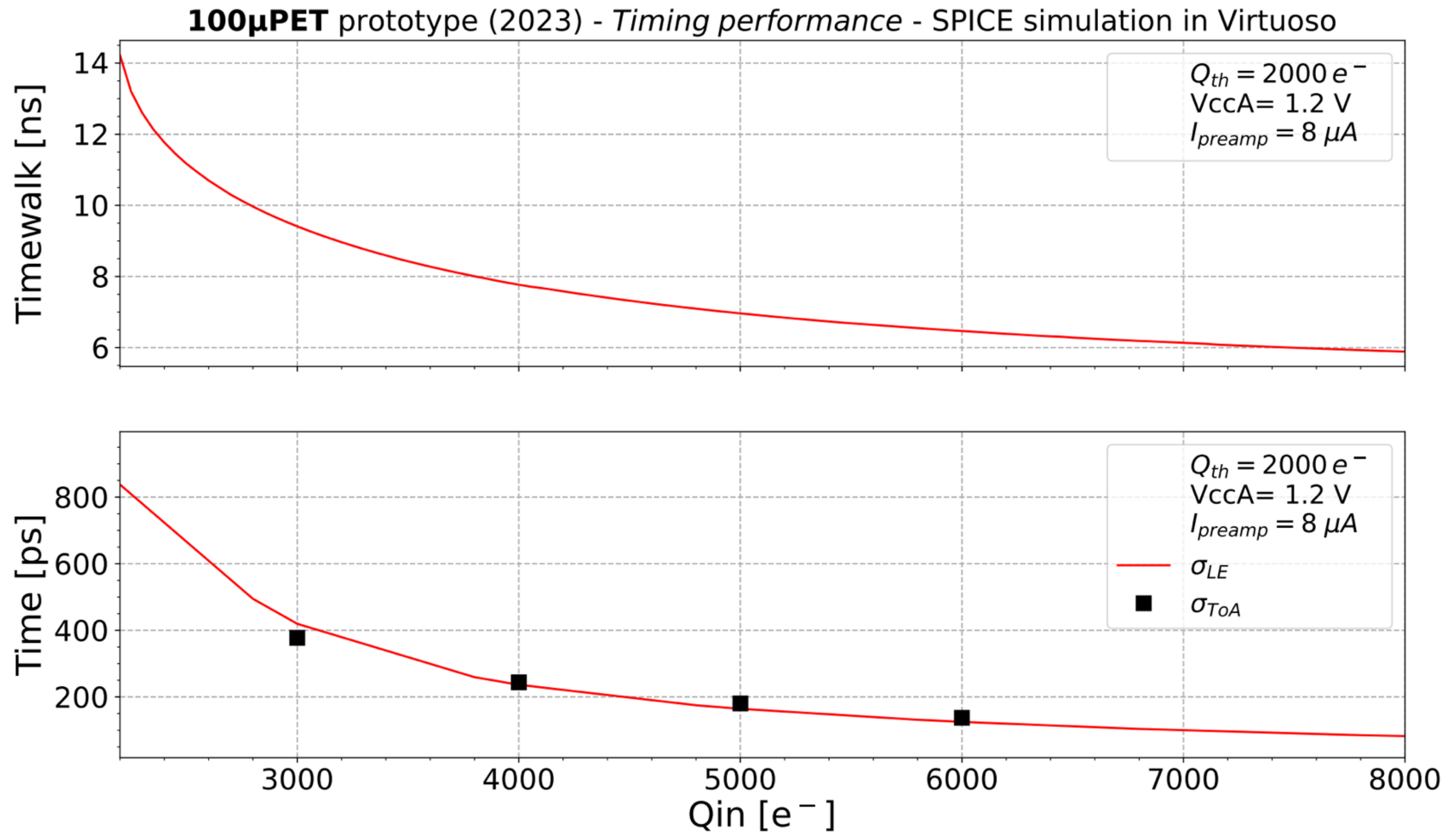
Front-End timing Performance



Excellent timing performance at very low power consumption.

Want to see what SiGe can do with little increase in power consumption?

Don't miss the talk from M. Milanesio

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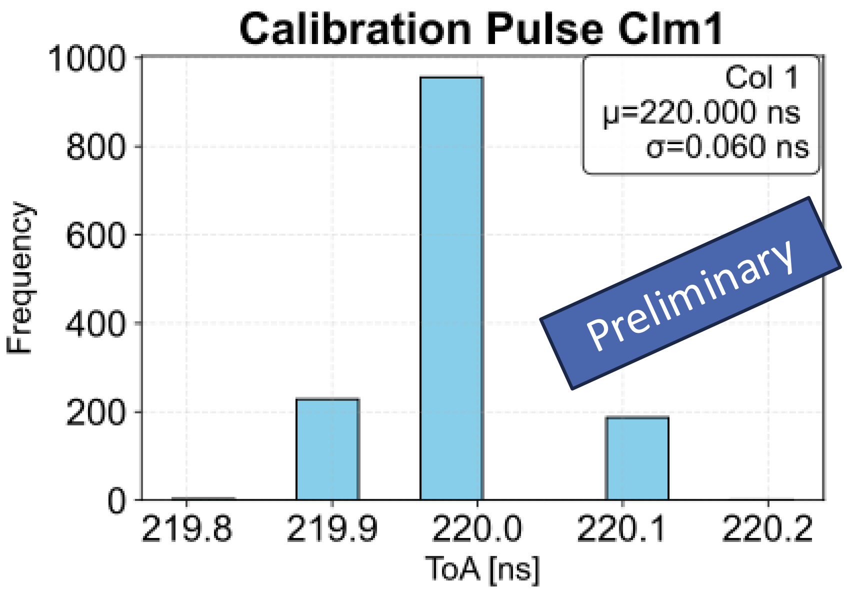
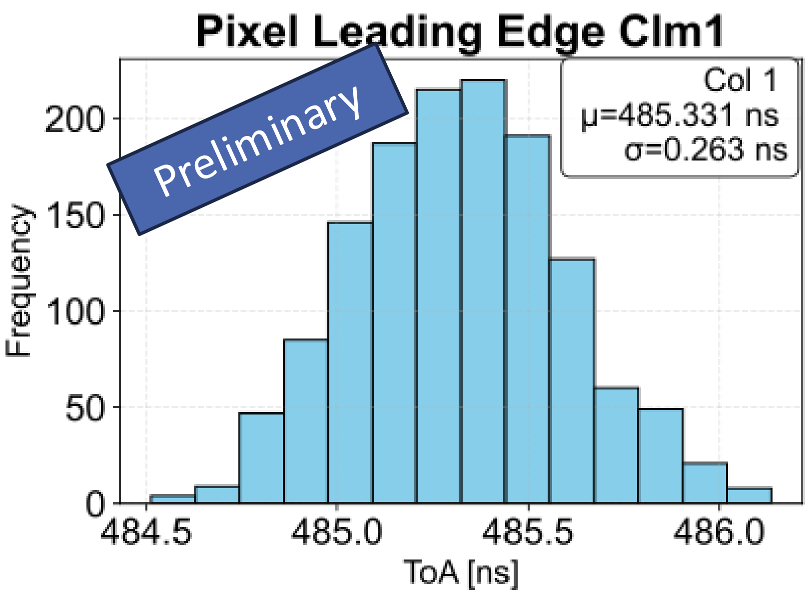
Time resolution with not-calibrated Testpulse

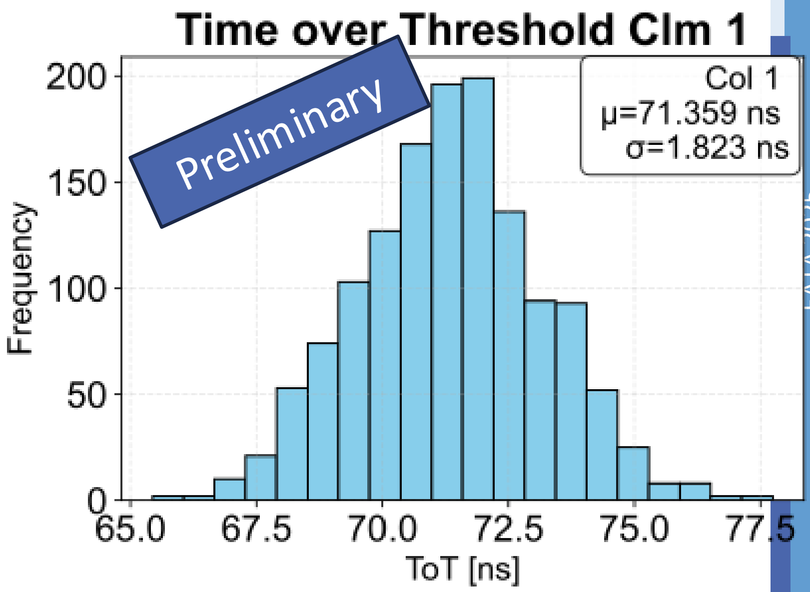
σ = 60 ps



σ = 263 ps



σ = 1863 ps



Expected input charge from MC simulation: 15 ke^- ±3ke^-

Discriminator working point not optimized for timing (10% of the design power consumption).

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Good time resolution to select **coincidence events** from noise

Use 1 ns time window
“4D-Tracking”

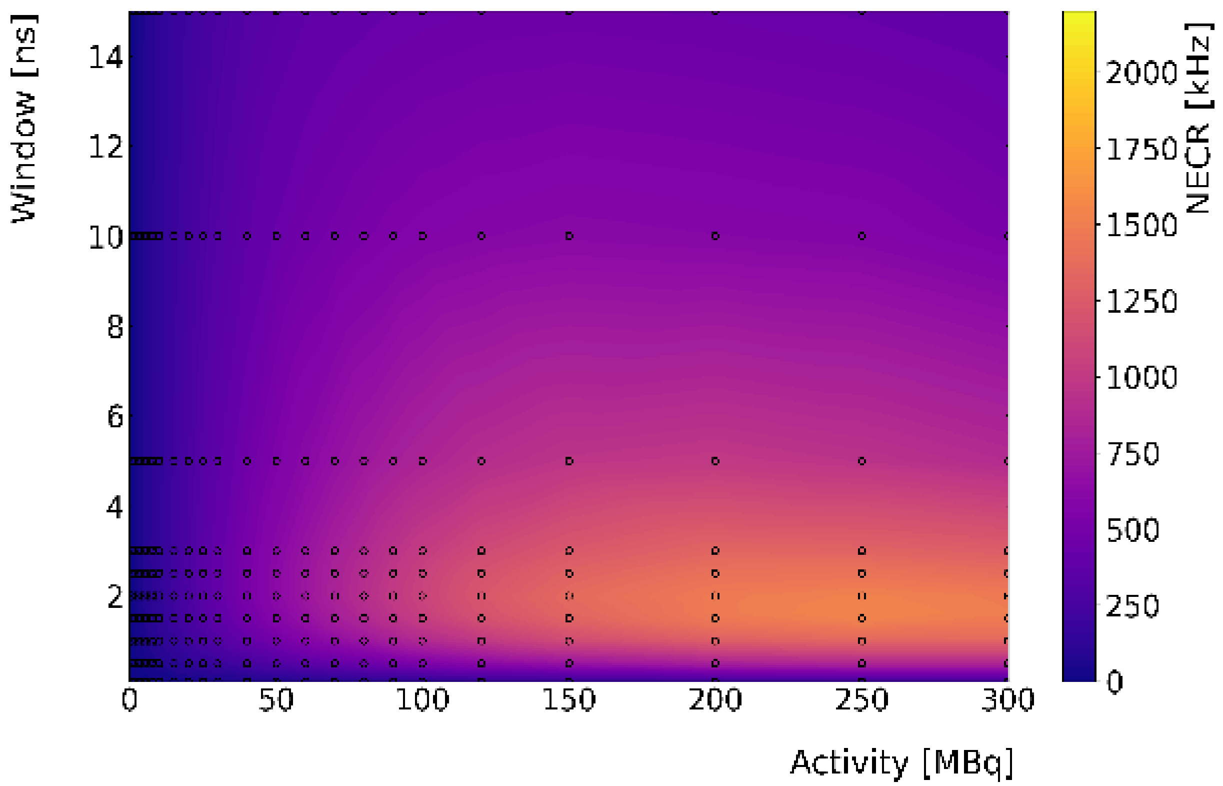
Reconstruction Resolution

Gaussian smearing to time stamps.

Timing standard deviation of 700 ps.

Optimal coincidence time window found between
1 and 2 ns.

$$\mathrm{NECR} = \frac{Tr^2}{Tr + Sr + Rr}$$



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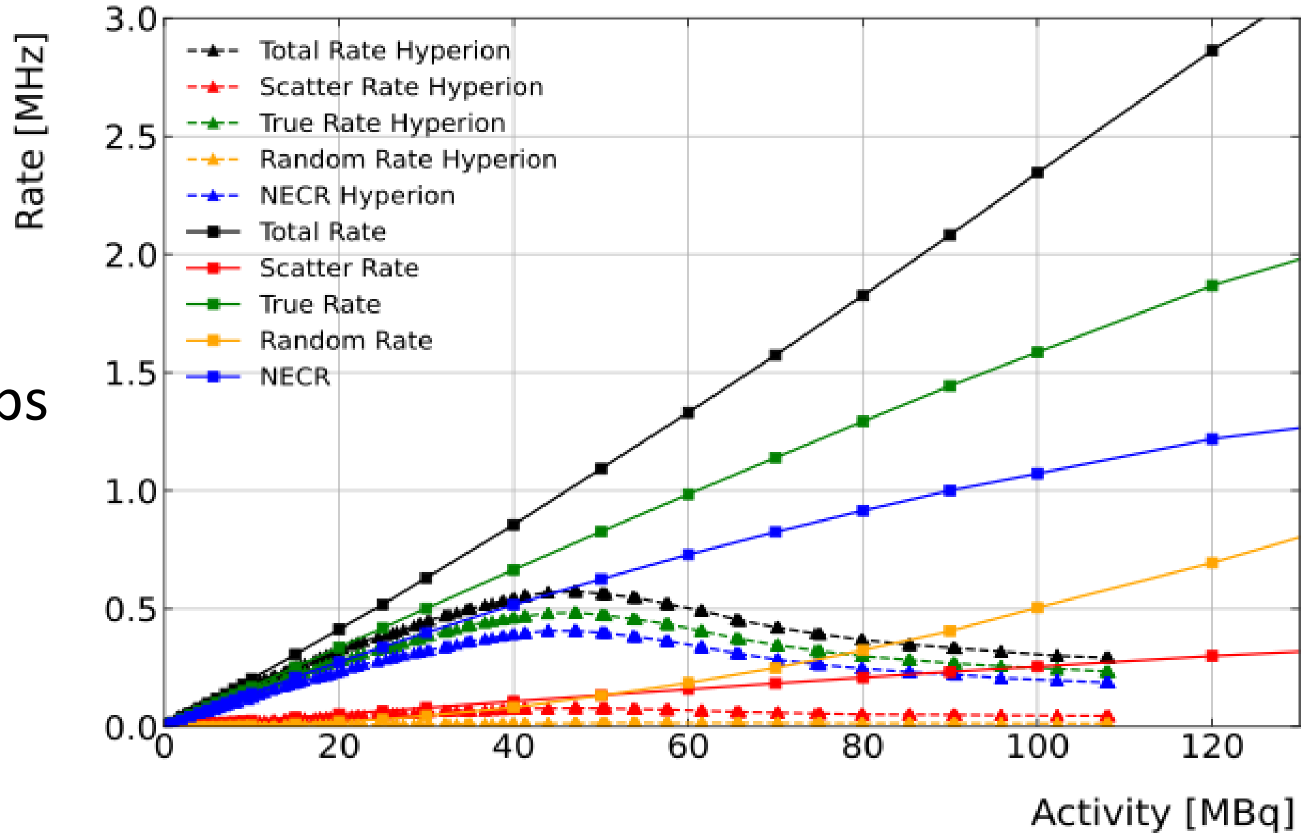
Timing Performance

The improved timing resolution and granularity of MAPS used in 100μPET enable

- Total timing jitter of σ_{time} = 700 ps
- Coincidence window τ_{win} = 2 ns

No signs of NECR saturation compared to Hyperion II^{D}.



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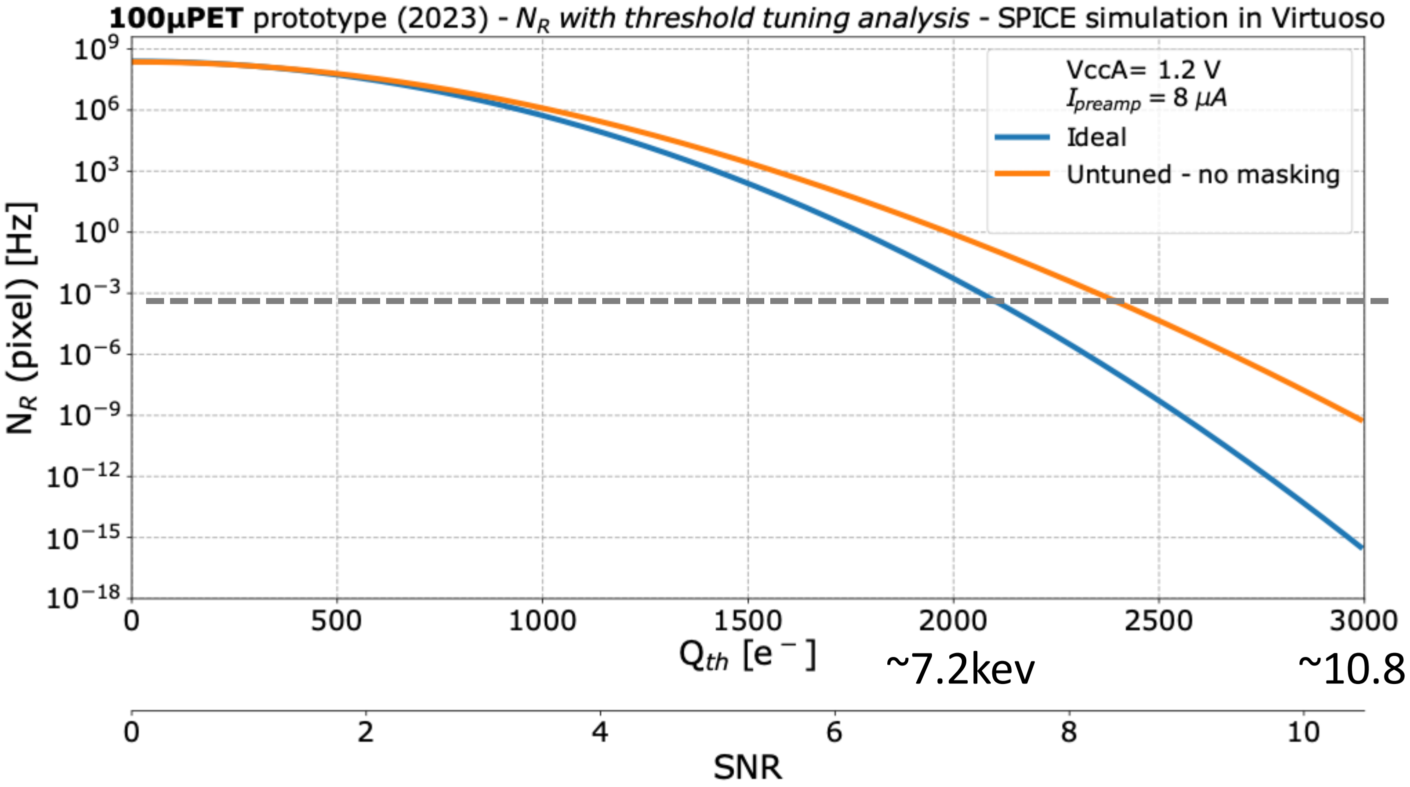
Mismatch and threshold tuning

$$N_R = f_{n0} \cdot e^{\frac{-Q_{th}{}^2}{2 \cdot ENC^2}}$$



~7.2kev ~10.8kev

Mismatch worsens the Noise Rate. With threshold tuning, we can achieve the required Noise Rate

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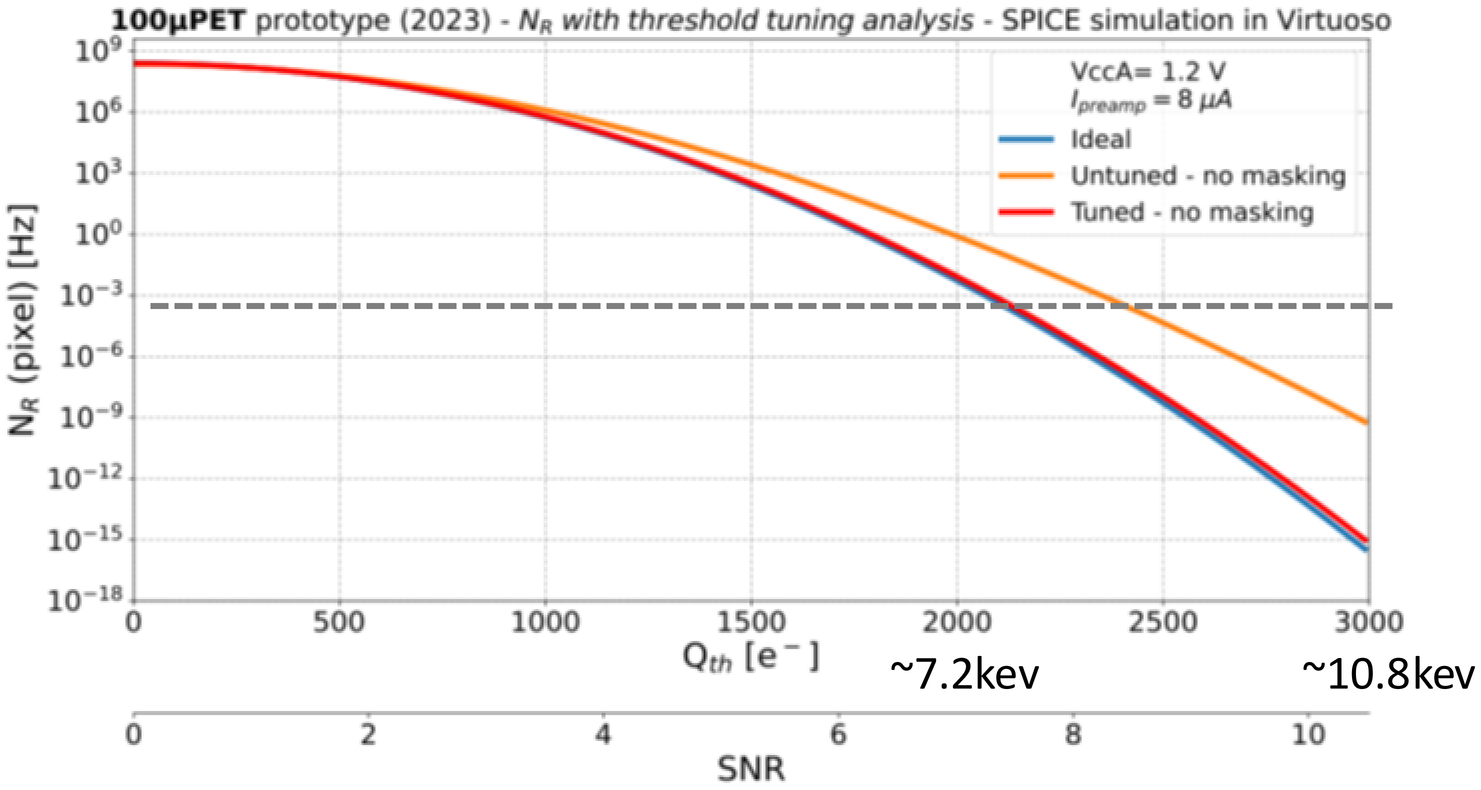
Mismatch and threshold tuning



Mismatch worsens the Noise Rate. With threshold tuning, we can achieve the required Noise Rate

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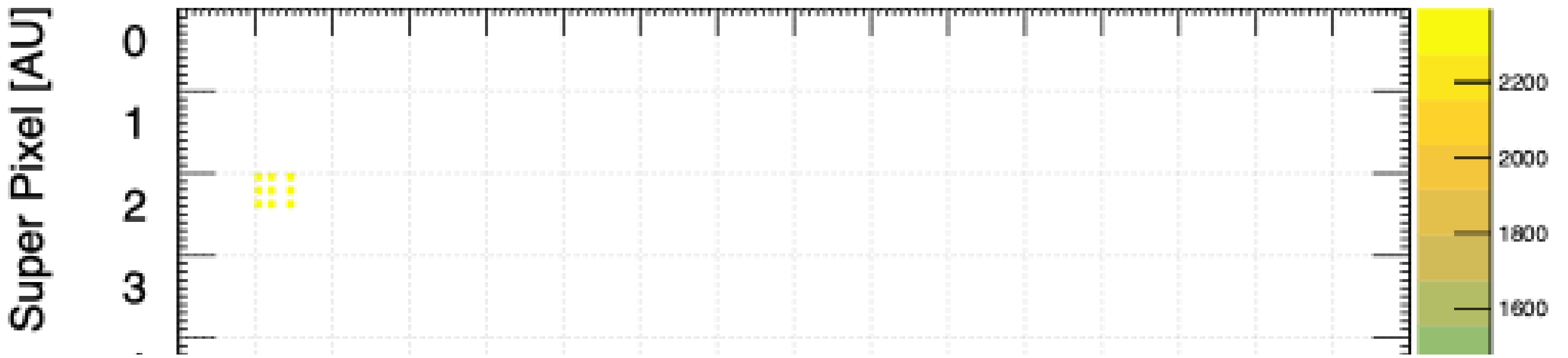
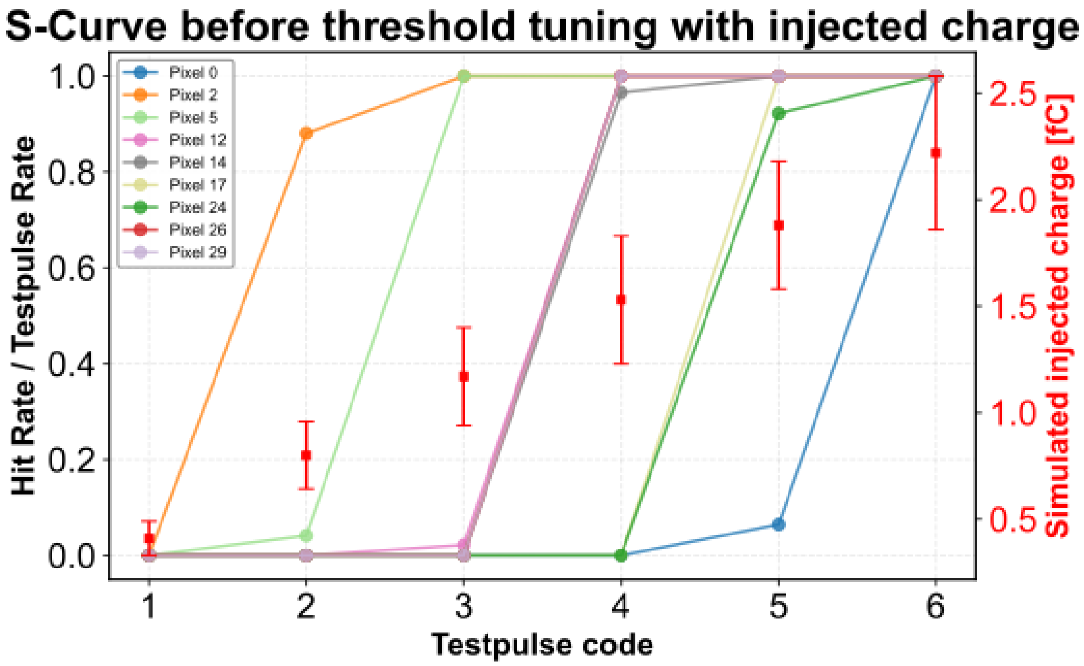
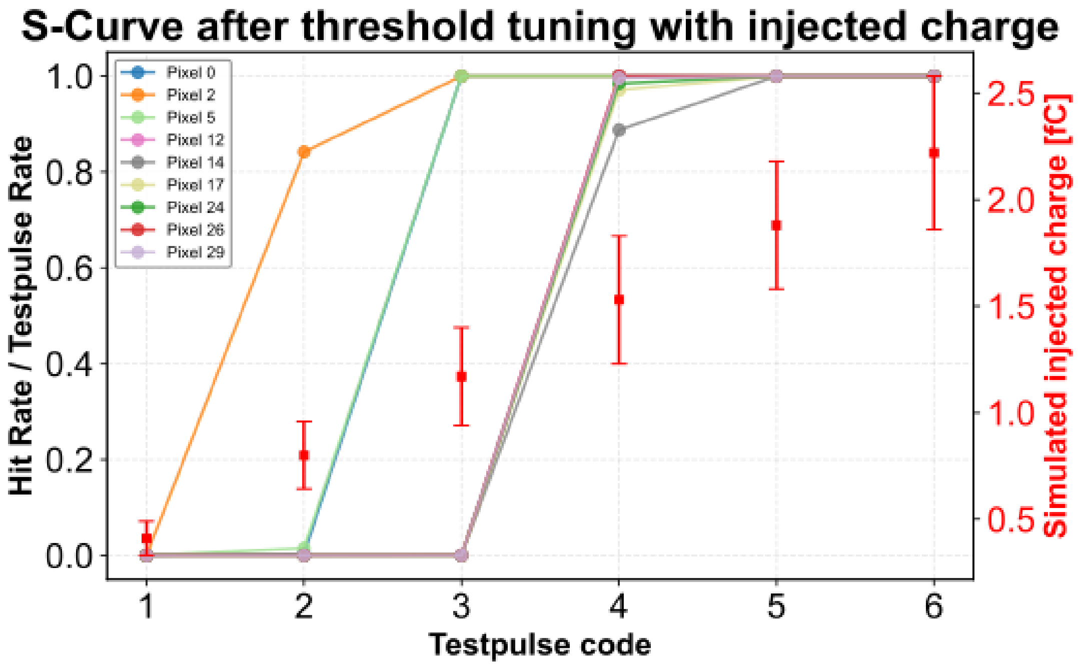
First Attempt of Threshold Tuning







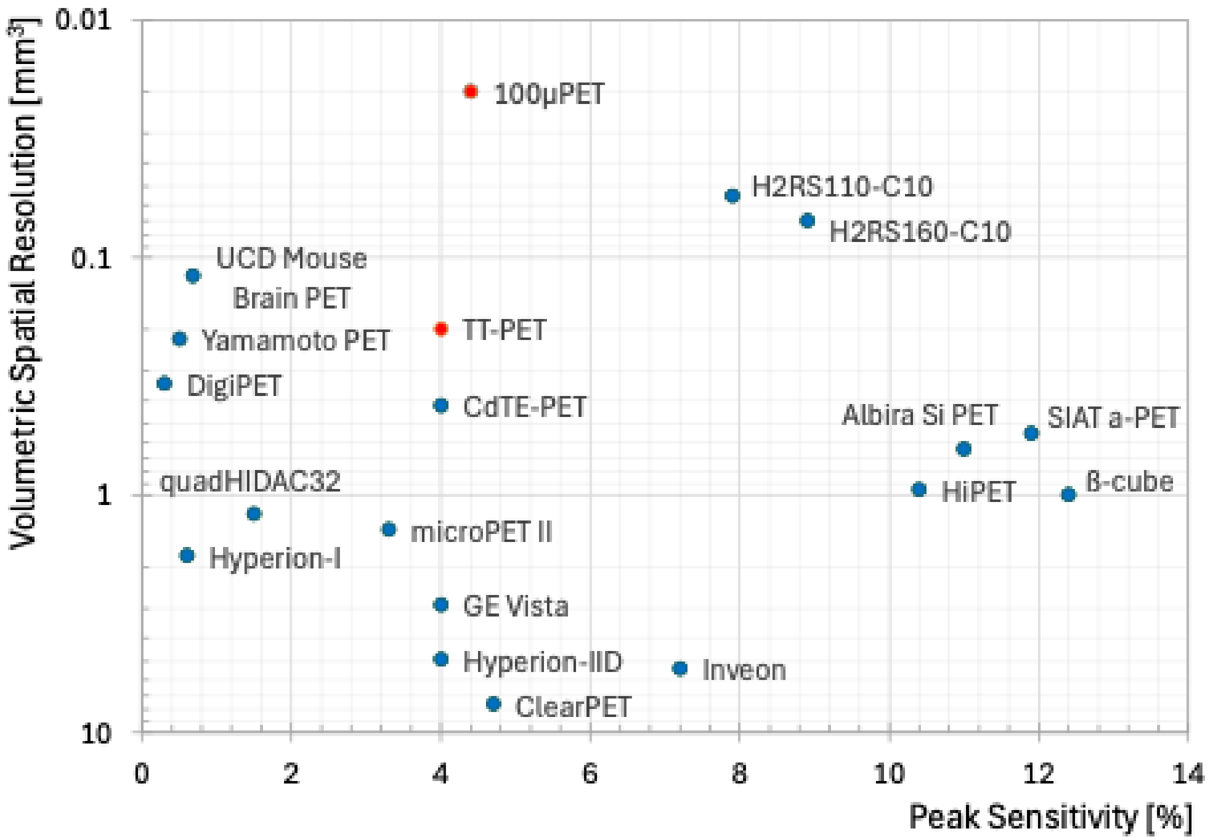
Conclusions

The 100µPET Scanner has the potential to deliver <u>ultra-high resolution imaging</u> using MAPS thanks to:

Detection Efficiency at 4.4 %

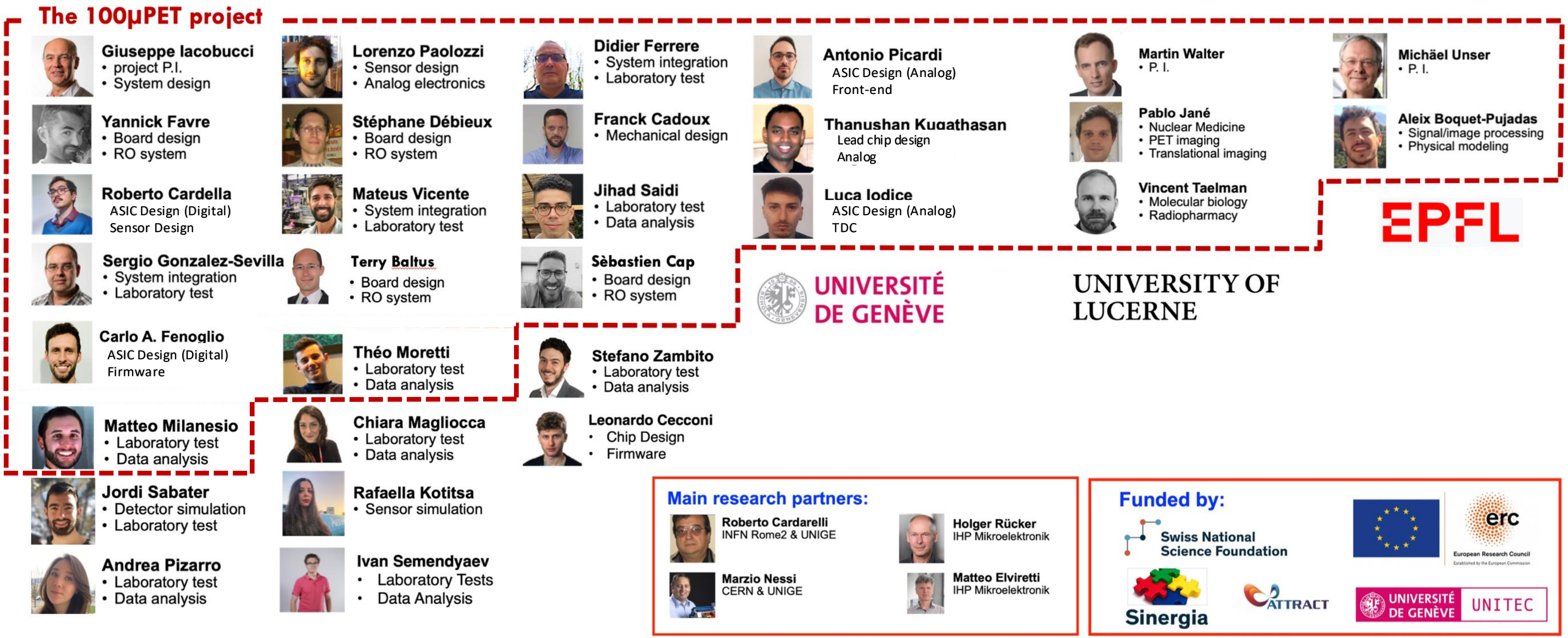
PSF resolution < 300 µm

Volumetric spatial resolution of 0.02 mm^3



The people

100μPET
MOLECULAR IMAGING AT ULTRA-HIGH RESOLUTION



Thank you for your attention

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