ALCOR development plans

ALCOR day in Torino

ALCOR for EIC Image: Tuesday 7 Mar 2023, 11:00 → 16:00 Europe/Rome Torino	2 -
Description http://cern.zoom.us/j/67299495767?pwd=TWhpNjIxeC9qNEFWUTBIUVJuMG1hUT09	
C Estatus_03_2023.pdf	
There are minutes attached to this event. Show them.	
11:00 → 11:10 TDC clock ambiguity [understood]	©10m ๔ ▾
11:10 → 11:20 TOT orphans [understood]	©10m ┏ -
11:20 → 11:30 ALCOR test at 390 MHz	⊙10m 🕑 -
11:30 → 11:40 Preliminary studies on packaging and AlcorV3 layout	🕲 10m 🗷 👻
11:40 → 11:50 SiPM capacitance and optimal coupling with ALCOR	©10m 🕑 🕶
11:50 → 12:00 Time resolution of the SiPM+ALCOR system	⊙10m 🕑 🕶
12:00 → 12:10 Definition of ToT reconstruction algorithm	310m 🕑 🕶

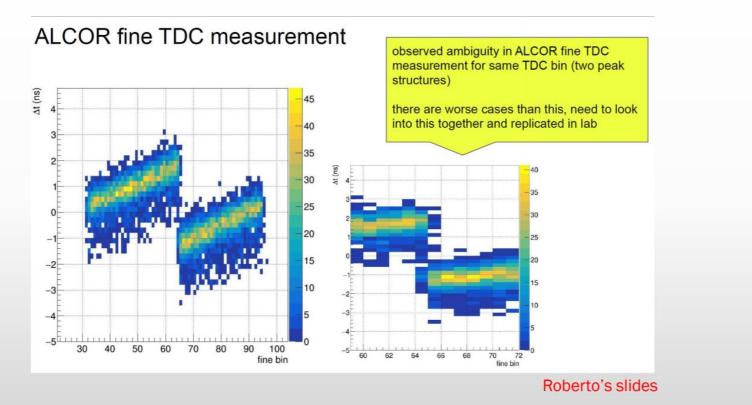


ALCOR status

07-03-2023 Giulio Dellacasa – Fabio Cossio

TDC clock ambiguity

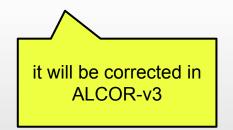




TDC clock ambiguity: solution



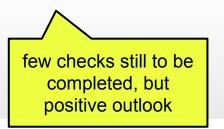
- The Coarse Counter is latched on the fast ramp signal
- Fast ramp signal: rising edge asynchronous falling edge synchronous
- Source code digitally simulated with a scan of Test Pulse phase
- Reconstructed time after simulations is now correct



Works in progress: 400 MHz



- New firmware with clock frequency 390 MHz: done
- Data transmission at 390 MHz x2 (DDR mode) seems to be correct
- CRC checks: ongoing
- TDC behaviour: some effects to understand in few pixels/TDC
- In any case a new implementation of the serializers is required to have a clean STA

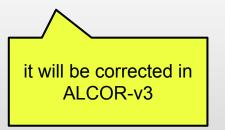


EIC clock 98.52 MHz → candidate clock for ALCOR: 295.56 MHz (or 394.08 MHz)

Works in progress: TOT



- TOT «Orphans effect» reproduced in simulation
 - Due to a bad implementation of the Fake Trigger function
 - Always occurs with the Coarse Counter rollover
 - Always on TDC1 and TDC3 (TOT falling edge)
 - Works in progress to change this part of the code
- TOT mixed events (rising and falling edge are not consecutive in data stream)
 - A different readout mechanism should be implemented for the TOT readout

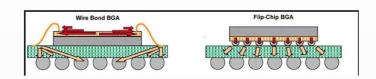


Packaging: Europractice



- Europractice service does not provide BGA packaging
- Standard packaging is cheap but not suitable for a good implementation of the 64 channels ASIC
- BGA packaging could be done through Europractice as Customized Packaging with one of their partner or outside the Europractice IC Service

https://europractice-ic.com/services/packaging/asic-packaging/



Flip chip or wire bond to BGA

- BGA: Higher costs, best implementation
- A totally new layout for both solutions (BGA vs standard)

Torino 07-03-2023

Timelines

• ALCOR-v2 is coming this year

• possible plan to have packaging and ALCOR-v3 in 2024

- might be close to final ALCOR version
- need to make sure that front-end is "well tuned" on the sensor
- R&D with FBK is approved, there will be new sensors in 2024
- what if we eventually decide we are happy with FBK sensors and need to adapt front-end?

• engineering run, when?

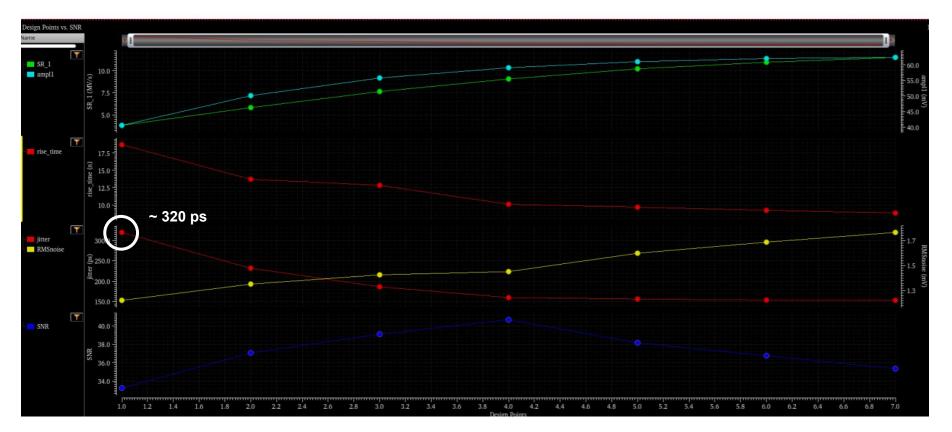
- ideas to have it in 2025
- I personally think this has to be thoroughly discussed
- see above, chip front-end and matching with sensor

There is urgency to define timelines, we need to stage discussions and reach the point where we can make decision-making

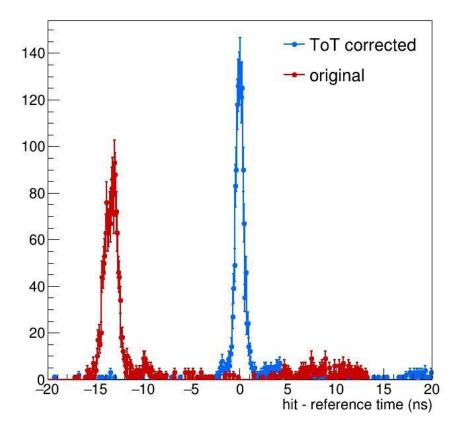
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Common gate scan (0-30)



ALCOR ToT



ToT feature of ALCOR used for the first time by us in 2022 beam test

ToT is important for improving time resolution we are far from a measurement of it from the beam test, but we have a best result

which is ~ 350 ps for HPK 13360 sensors larger than what I hoped at lowish overvoltage (3 V)

is this close to the limit we can achieve with ALCOR coupled with these SiPM sensors?

if not, we need to understand where in the electronics chain we need to improve for better timing