

ALCOR status

07-03-2023 Giulio Dellacasa – Fabio Cossio

Updates

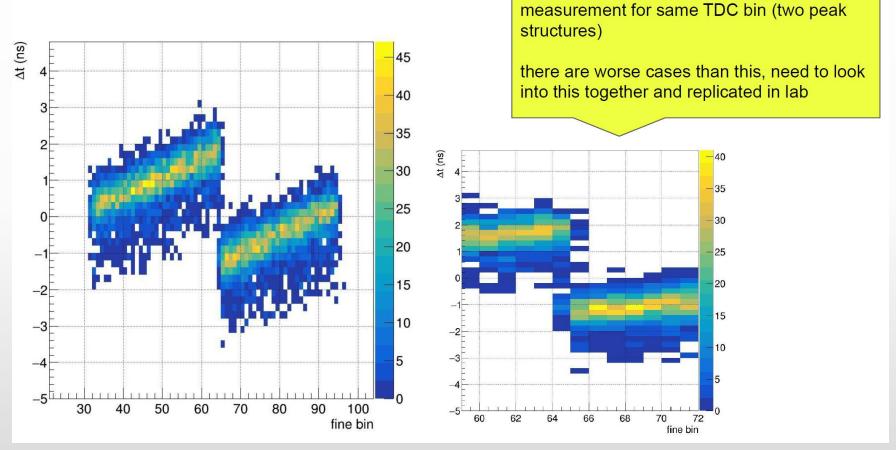


- TDC clock ambiguity
- TOT orphans and data coupling
- 400 MHz operation
- 64 channels packaging

TDC clock ambiguity



ALCOR fine TDC measurement

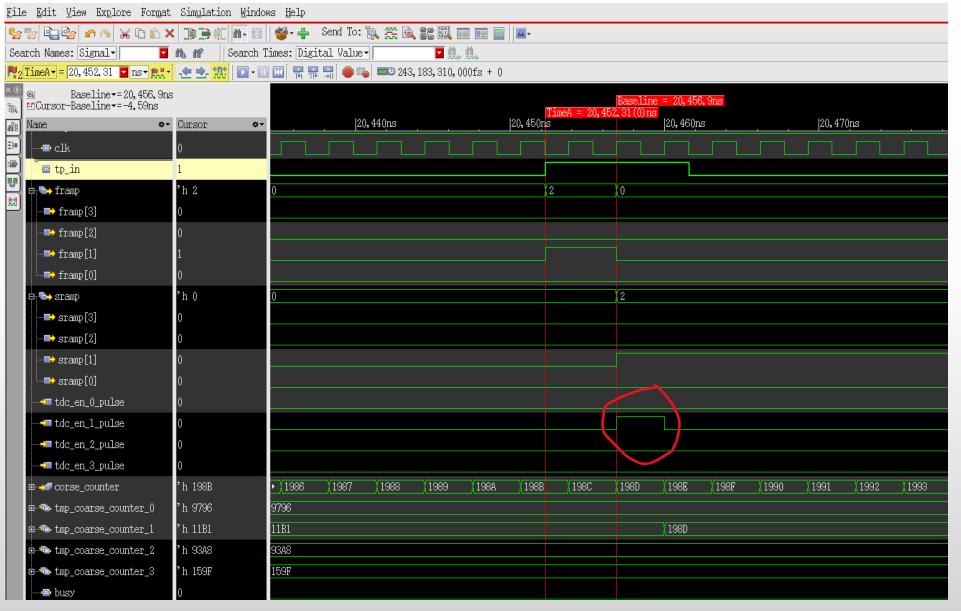


Roberto's slides

observed ambiguity in ALCOR fine TDC

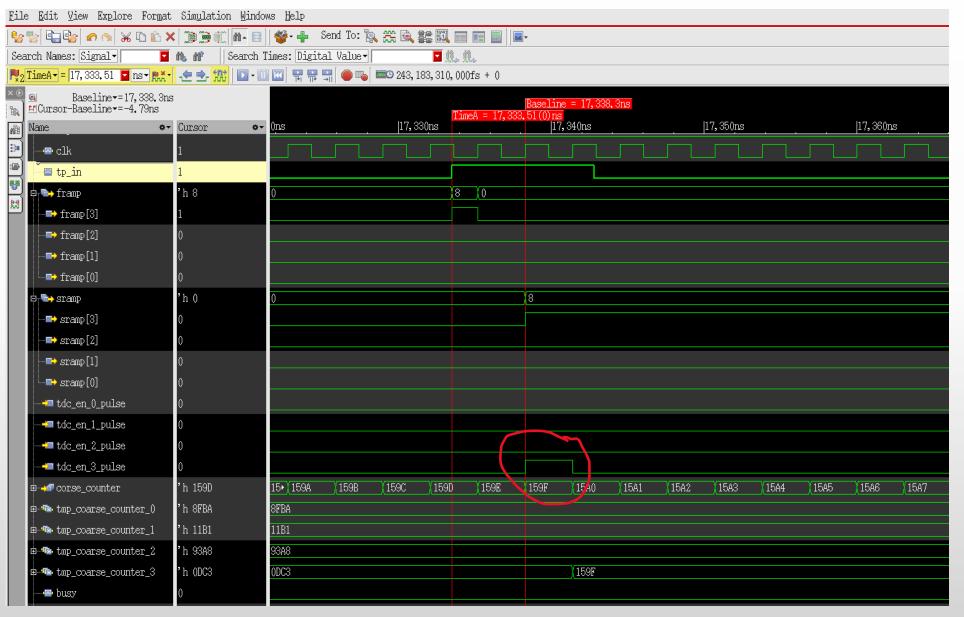
TDC clock ambiguity





TDC clock ambiguity



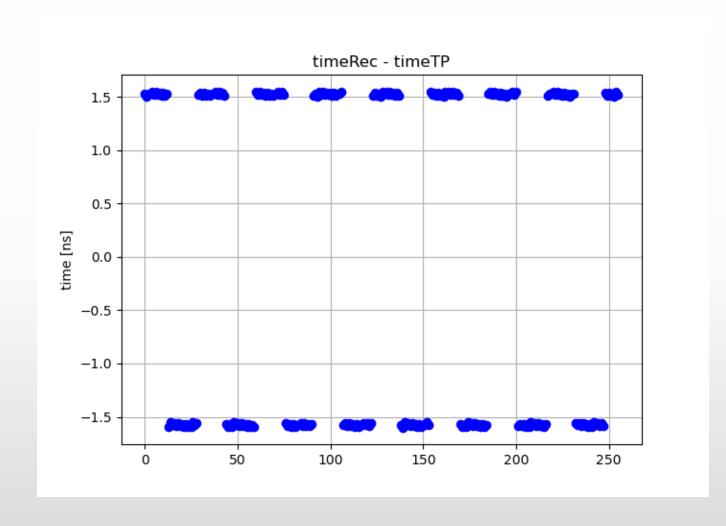


TDC clock ambiguity: solution

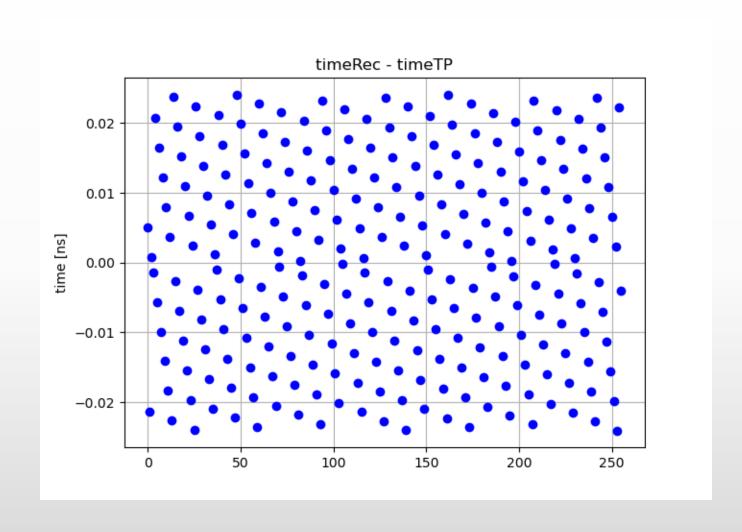


- The Coarse Counter is latched on the fast ramp signal
- Fast ramp signal: rising edge asynchronous falling edge synchronous
- Source code digitally simulated with a scan of Test Pulse phase
- Reconstructed time after simulations is now correct

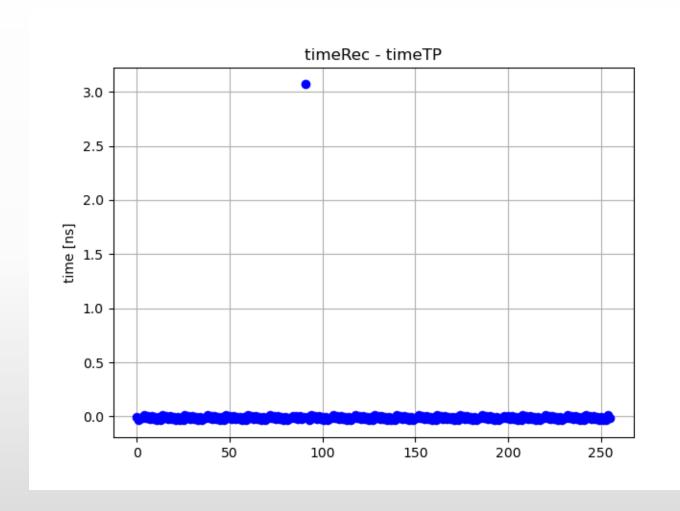




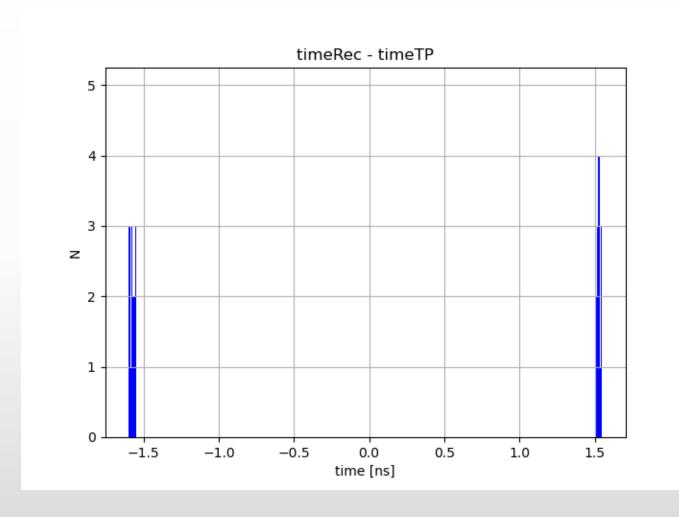




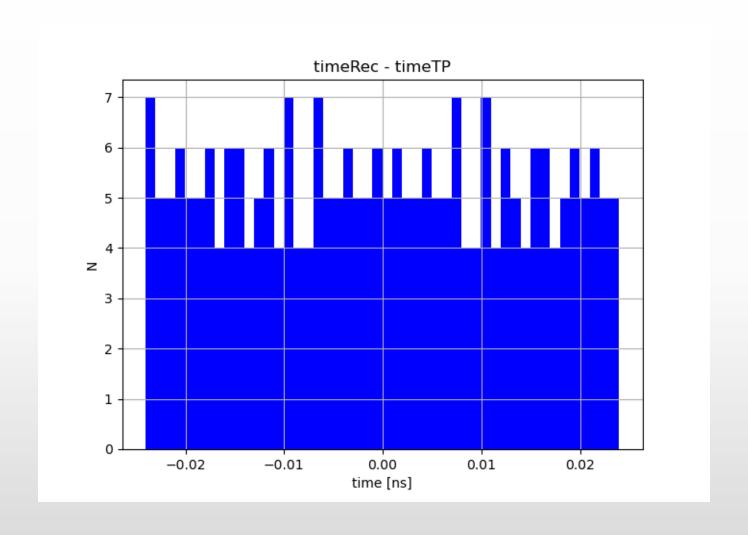




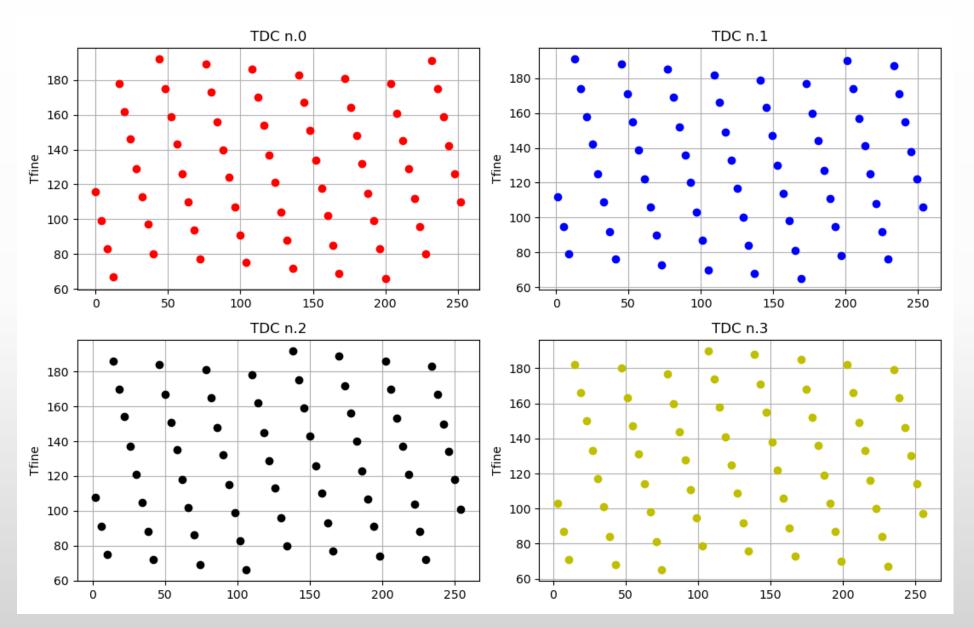












Works in progress: 400 MHz



- New firmware with clock frequency 390 MHz: done
- Data transmission at 390 MHz x2 (DDR mode) seems to be correct
- CRC checks: ongoing
- TDC behaviour: some effects to understand in few pixels/TDC
- In any case a new implementation of the serializers is required to have a clean STA

Works in progress: TOT



- TOT «Orphans effect» reproduced in simulation
 - Due to a bad implementation of the Fake Trigger function
 - Always occurs with the Coarse Counter rollover
 - Always on TDC1 and TDC3 (TOT falling edge)
 - Works in progress to change this part of the code
- TOT mixed events (rising and falling edge are not consecutive in data stream)
 - A different readout mechanism should be implemented for the TOT readout

Packaging: Europractice



- Europractice service does not provide BGA packaging
- Standard packaging is cheap but not suitable for a good implementation of the 64 channels ASIC
- BGA packaging could be done through Europractice as Customized Packaging with one of their partner or outside the Europractice IC Service

https://europractice-ic.com/services/packaging/asic-packaging/

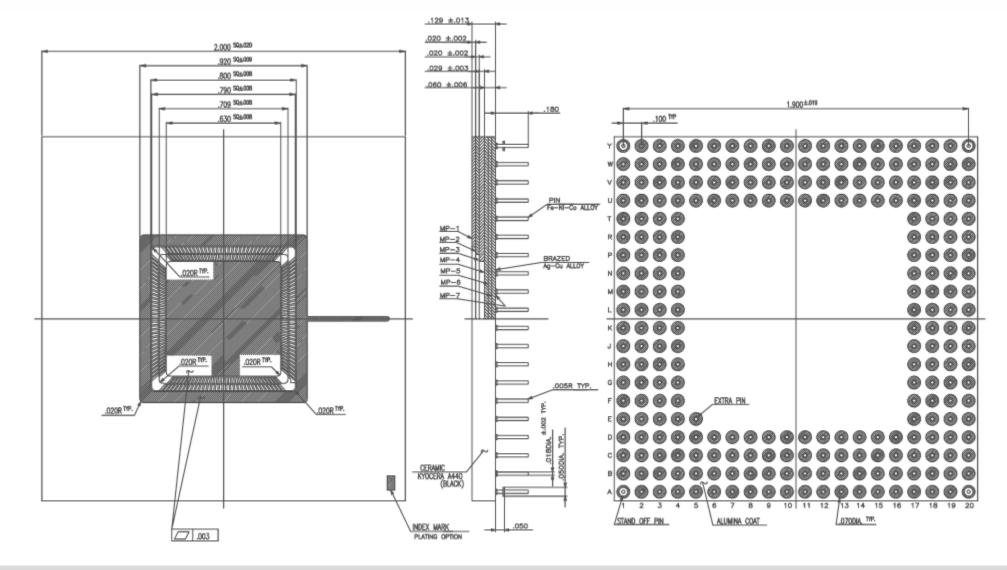
Packaging examples



- ALCOR V2: 126 pads (32 channels)
- From the Europractice list (but maybe there are others on request...)
 - 256 pin: PBGA (Through Hole)
 - 208 pin: QFP

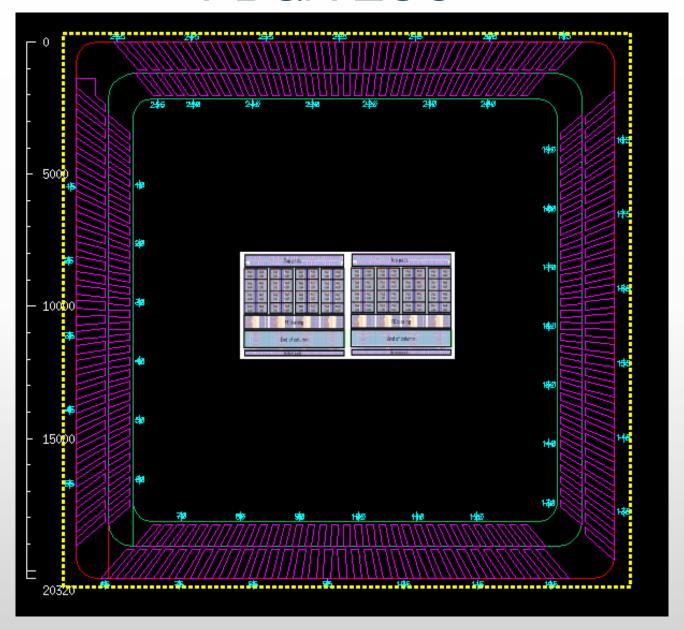
PBGA 256





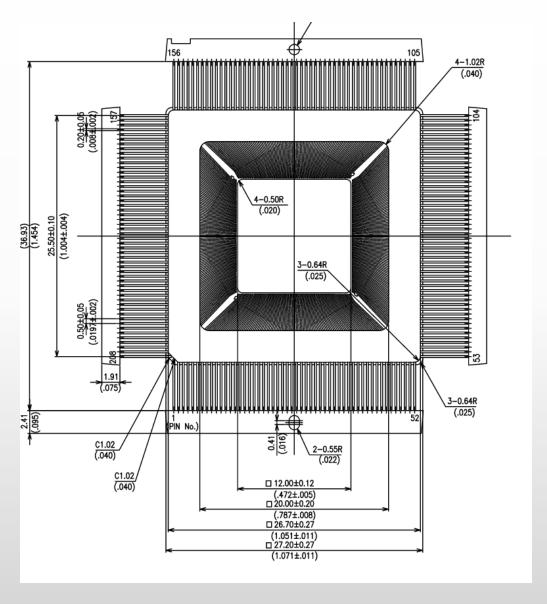
PBGA 256





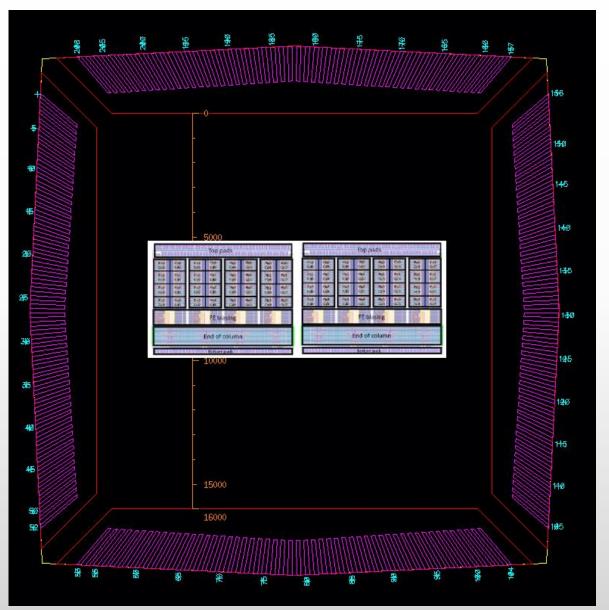
QFP 208





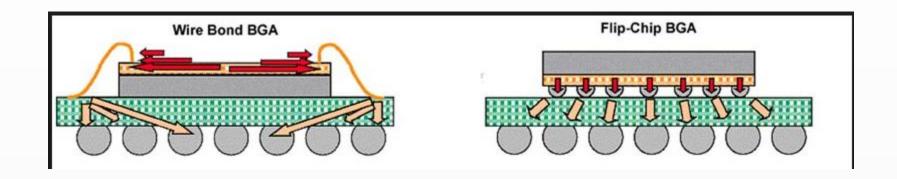
QFP 208





Flip chip or wire bond to BGA





- BGA: Higher costs, best implementation
- A totally new layout for both solutions (BGA vs standard)

Packaging costs



PRICE STRUCTURE

All packages require a setup cost of €440 per bonding diagram.

The prices below are valid for all packages and bonding of designs with the following requirements:

- Pad pitch of min. 90 microns
- · Wire bonding length up to 6mm. If wirebond length is more than 6mm, 30% additional charge applies based on unit price
- Passivation openings of 76µm x 76µm or larger. Additional charges apply for designs with passivation openings less than 76µm x 76µm:
- passivation openings 61µm to 75µm: 325 EUR
- passivation openings 51µm to 60µm: 470 EUR
- passivation openings 40µm to 50µm: 585 EUR

Minimum package order depends on the EUROPRACTICE partner you work with.

- Fraunhofer and imec: minimum quantity is 10 packages per design.
- CMP: minimum quantity is 5 packages per design.

Fixed set-up cost for glass sealing for up to 30 pieces: 820 EUR.

Dear Giulio,

A BGA package is always to be considered as a customized package requiring a dedicated substrate with solder balls at the bottom and to which the die is flip-chipped or wire bonded to the top side.

A BGA involves the design and manufacturing of the substrate prior to the subsequent assembly steps.

For small quantities the design and NRE costs are the dominant ones.

As ballpark numbers:

Cost for designing a BGA substrate typically is in the 20K to 50K EUR range

NRE costs related to substrate manufacturing and assembly setup are in the 50K to 200K EUR range depending on size and complexity (number of layers, ball pitch, bump pitch, signal requirements)

I'll be happy to elaborate this further.



