VERTEX DETECTORS

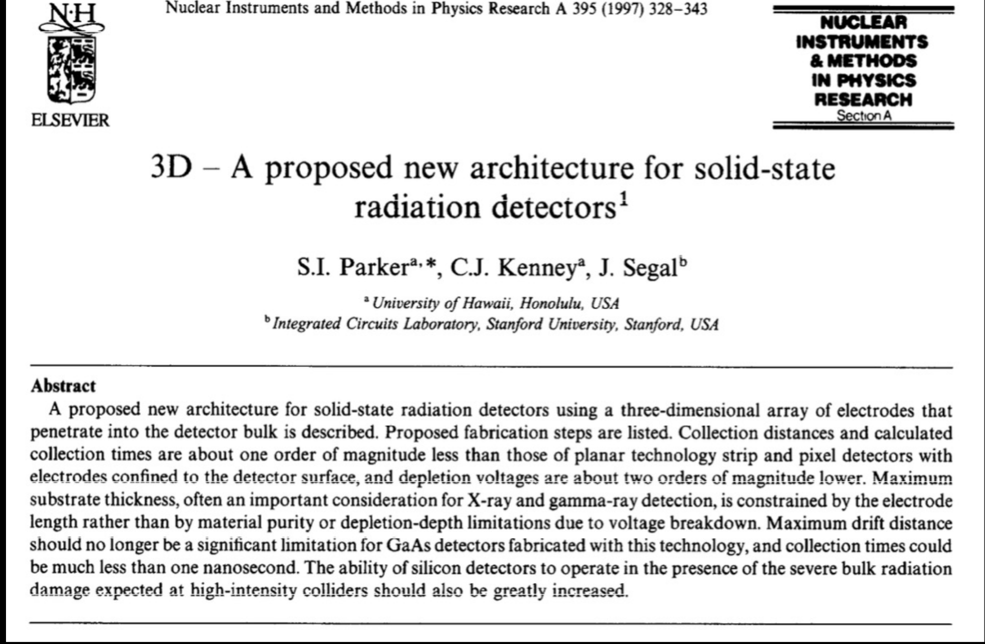
Daniela Bortoletto

The technologies for the future

- PP experiments are highly optimized
- Therefore the configuration of your detectors does depend critically on the accelerator and the physics goals.
- We will look at few technologies that are critical for the future:
  - Ultra-radiation hard detectors
  - Ultra-fast detectors
  - Ultra-low mass detectors

3D Sensor History

- First proposed in 1997 by Sherwood Parker
- Decouples sensor thickness from depletion voltage
- Radiation hardness advantage over planar sensors in the presence of bulk radiation damage
- Enabled by development of high-aspect silicon etch technology


Nuclear Instruments and Methods in Physics Research A 395 (1997) 328–343

NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A

ELSEVIER

3D – A proposed new architecture for solid-state radiation detectors[1]

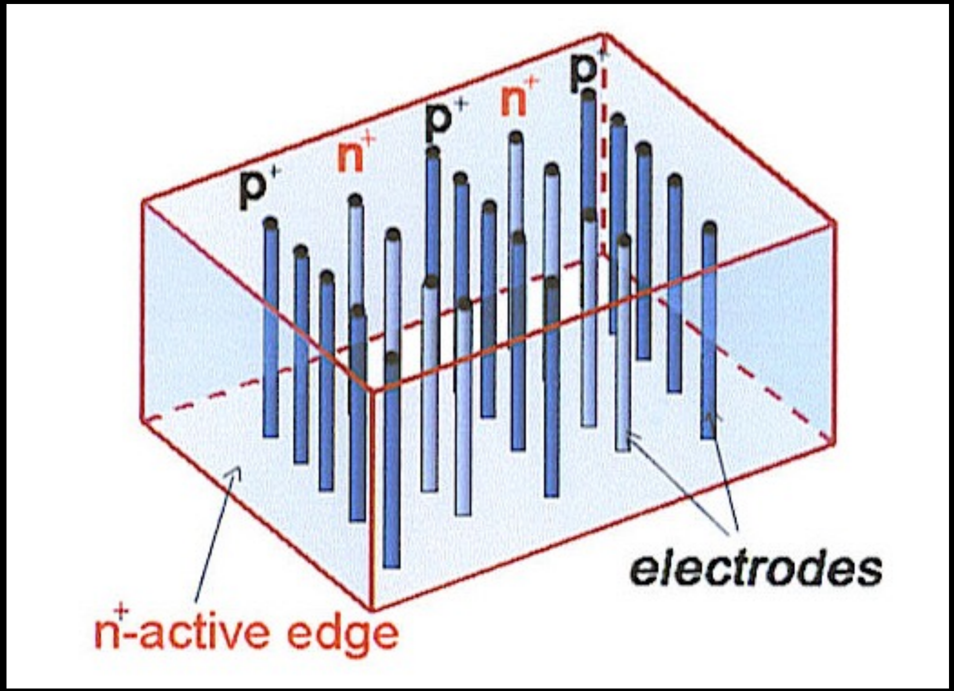
S.I. Parker[a,*], C.J. Kenney[a], J. Segal[b]

[a] University of Hawaii, Honolulu, USA
[b] Integrated Circuits Laboratory, Stanford University, Stanford, USA

Abstract

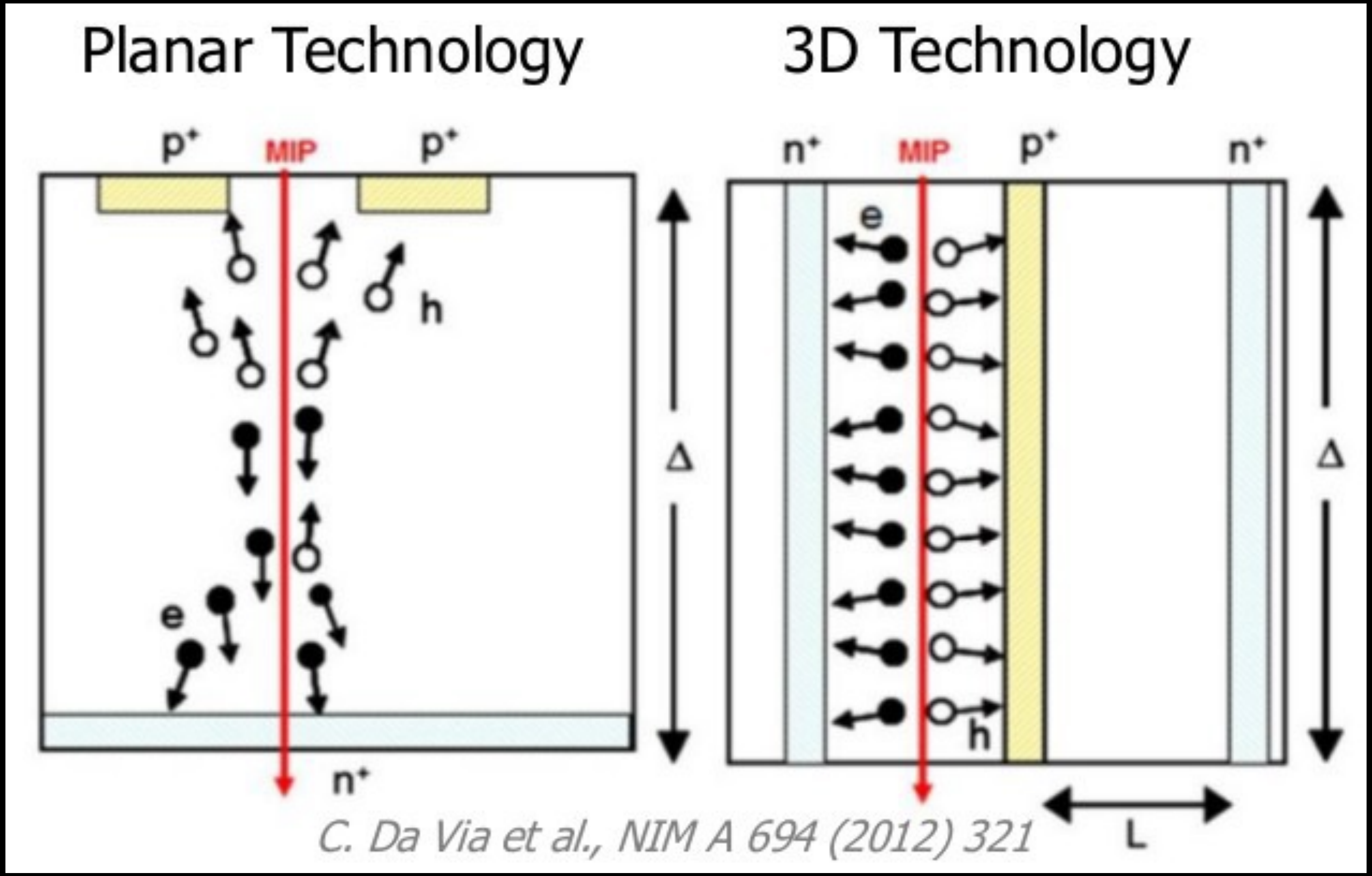
A proposed new architecture for solid-state radiation detectors using a three-dimensional array of electrodes that penetrate into the detector bulk is described. Proposed fabrication steps are listed. Collection distances and calculated collection times are about one order of magnitude less than those of planar technology strip and pixel detectors with electrodes confined to the detector surface, and depletion voltages are about two orders of magnitude lower. Maximum substrate thickness, often an important consideration for X-ray and gamma-ray detection, is constrained by the electrode length rather than by material purity or depletion-depth limitations due to voltage breakdown. Maximum drift distance should no longer be a significant limitation for GaAs detectors fabricated with this technology, and collection times could be much less than one nanosecond. The ability of silicon detectors to operate in the presence of the severe bulk radiation damage expected at high-intensity colliders should also be greatly increased.

- The Insertable B-Layer (IBL), the inner most pixel layer in the ATLAS experiment (installed at 3.3 cm radius from the beam axis in 2014 to improve the tracking performance) contains 3D sensors



3D sensors compared to planar sensors

- Pros
  - De-couple depletion voltage and electric field from sensor thickness
  - Lower depletion voltage
  - Faster read-out
  - Radiation hardness
- Cons
  - Process complexity and yield
  - Test complexity
    - Disposable metal layer for test
  - More difficult to scale pixel size
  - Electrodes are ”dead” area
  - Higher capacitance

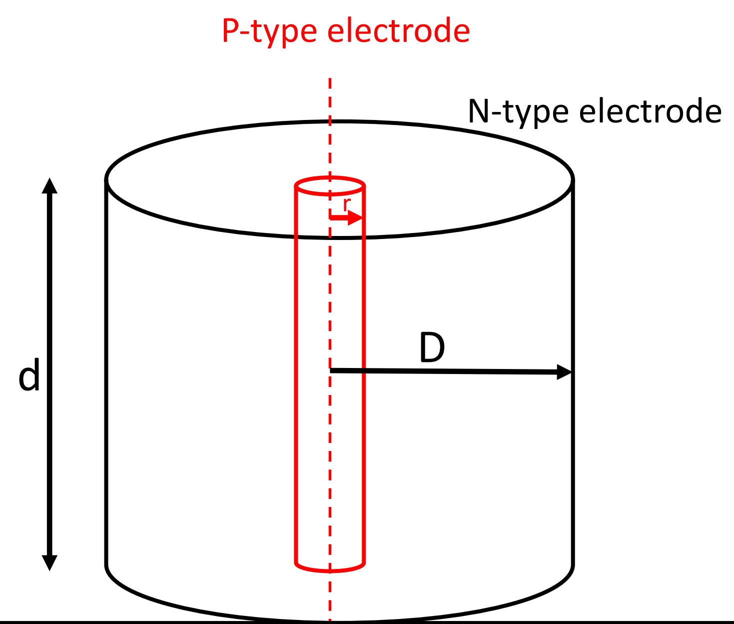


3D sensors Characteristics

- Full depletion voltage now is given by the coaxial approximation

$$V_{FD} = \frac{qN_{eff}}{2\epsilon_0\epsilon_{Si}}\left(D^2\left[ln(\frac{D}{r} - 0.5)\right] + 0.5r^2\right)$$

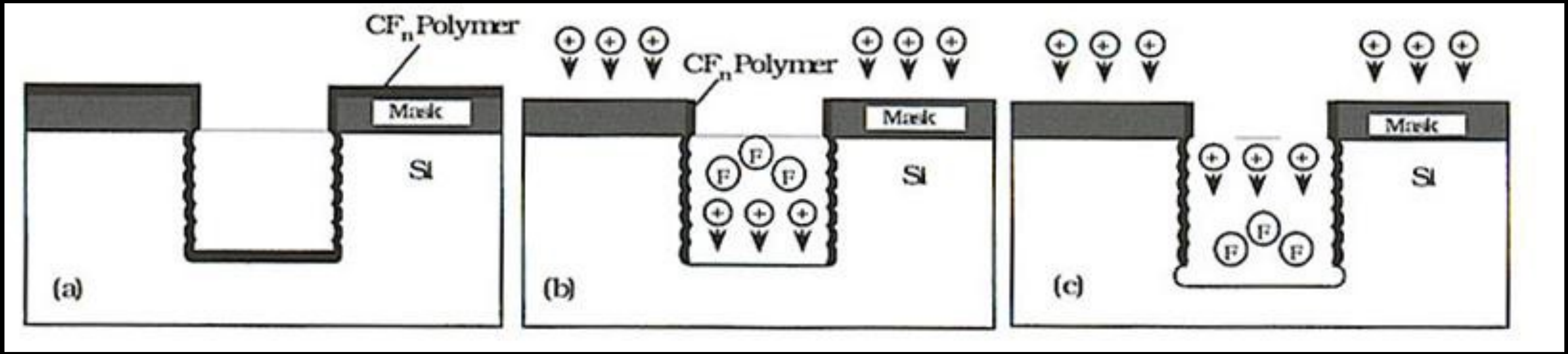
D …Electrode distance
r…column radii



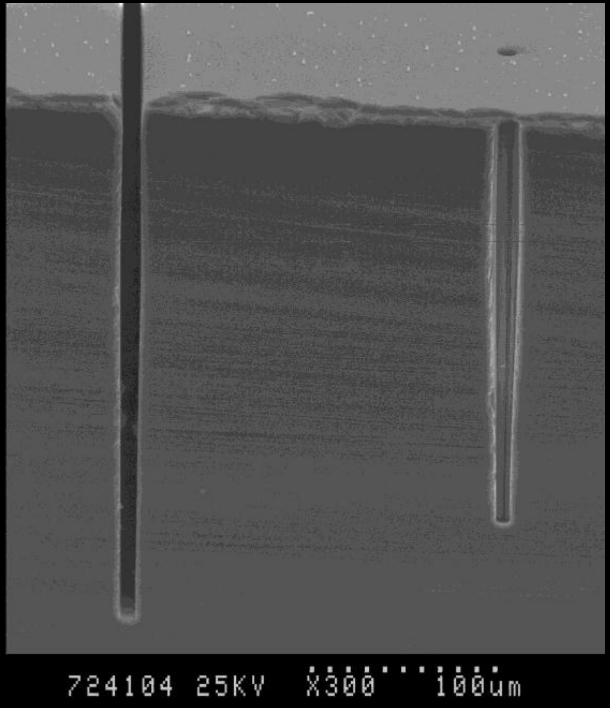
- Smaller VFD
- Shorter distances to travel for carriers
- Input capacitance is higher than planar
- Short collection distances, fast collection times and low depletion voltages

$$C = \frac{2\pi\varepsilon_0 d}{ln\left(\frac{D}{r}\right)}$$

Key fabrication steps

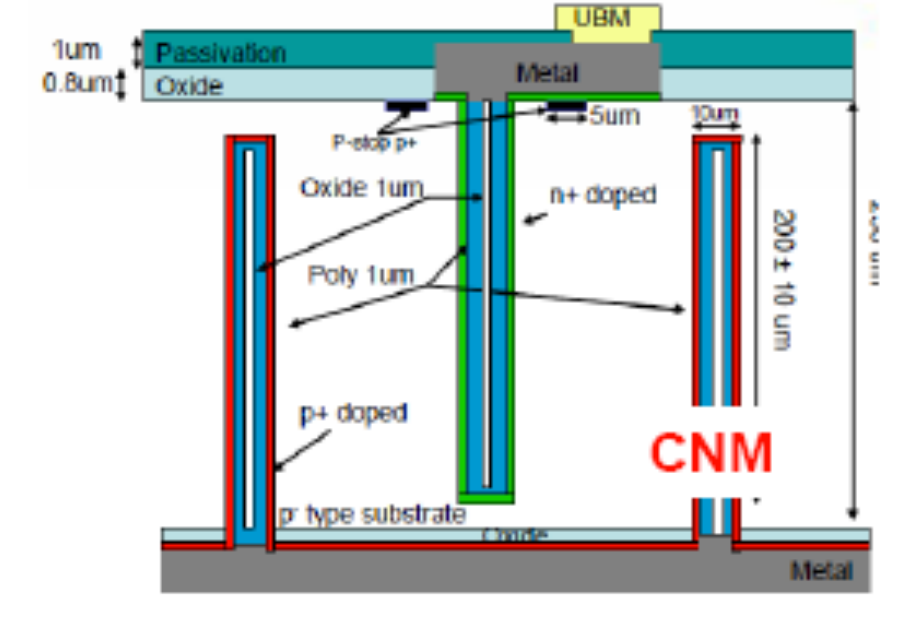


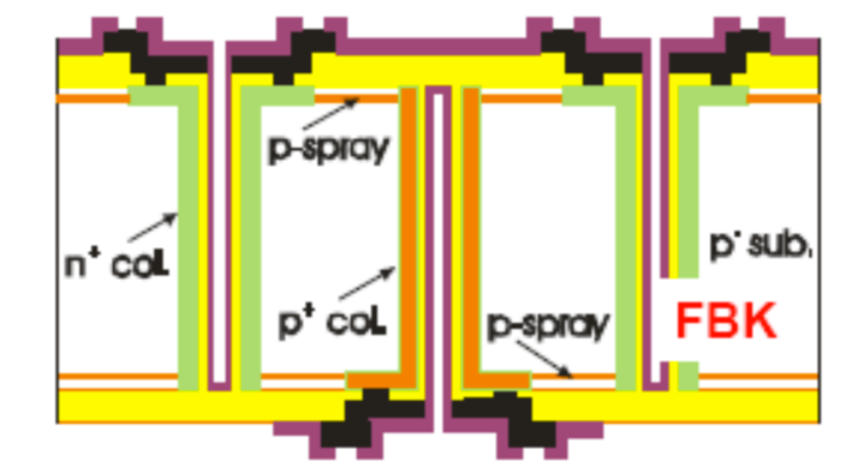
- **BOSCH PROCESS: alternating passivation (C_4F_8) and etch cycles (SF_6)**
  - Within the plasma an electric field is applied perpendicular to the silicon surface.
  - The etch cycle consists of fluorine based etchants which react with silicon surface, removing silicon. The etch rates are ~1-5μm/minute.
  - To minimize side wall etching, etch cycle is stopped and replaced with a passivation gas which creates a Teflon-like coating homogenously around the cavity. Energetic fluorine ions, accelerated by the E-field, remove the coating from the cavity bottom but NOT the side walls.



Joint effort for ATLAS IBL

- In June 2009, four processing facilities joined their efforts, produced a common floor plan and launched a production of 3D sensors.
- SINTEF and SLAC/SNF with full 3D and active edges.
- FBK and CNM with double side processing and slim edge design.

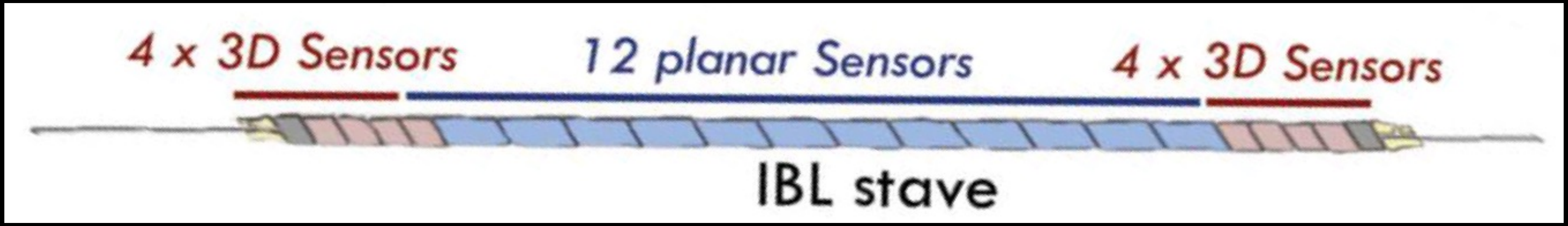




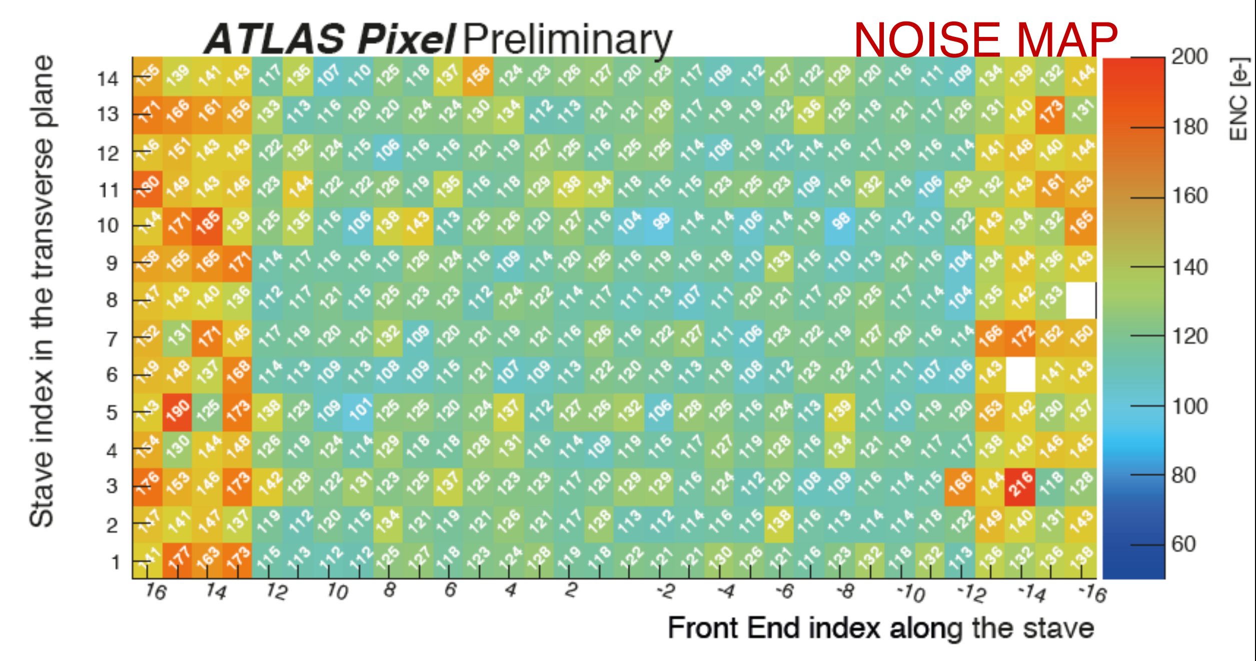
- Double sided Double Type column
- Partially overlapping electrodes
- No Active edge

Impact of ATLAS IBL

- Innovation:
  - IBL had smaller pixel size (50 x 250 μm^2) than ATLAS pixel already installed (50 x 400 μm^2)
  - IBL used 3D for 25% of area at the first time in HEP experiment.



- After 4.3 fb^{-1} corresponding to 1.3 Mrad and 2.5×10^{13} n_{eq}/cm^2
- Bias voltage
  - IBL 3D: 20 V
  - IBL planar: 80 V
  - B-layer: 250 V



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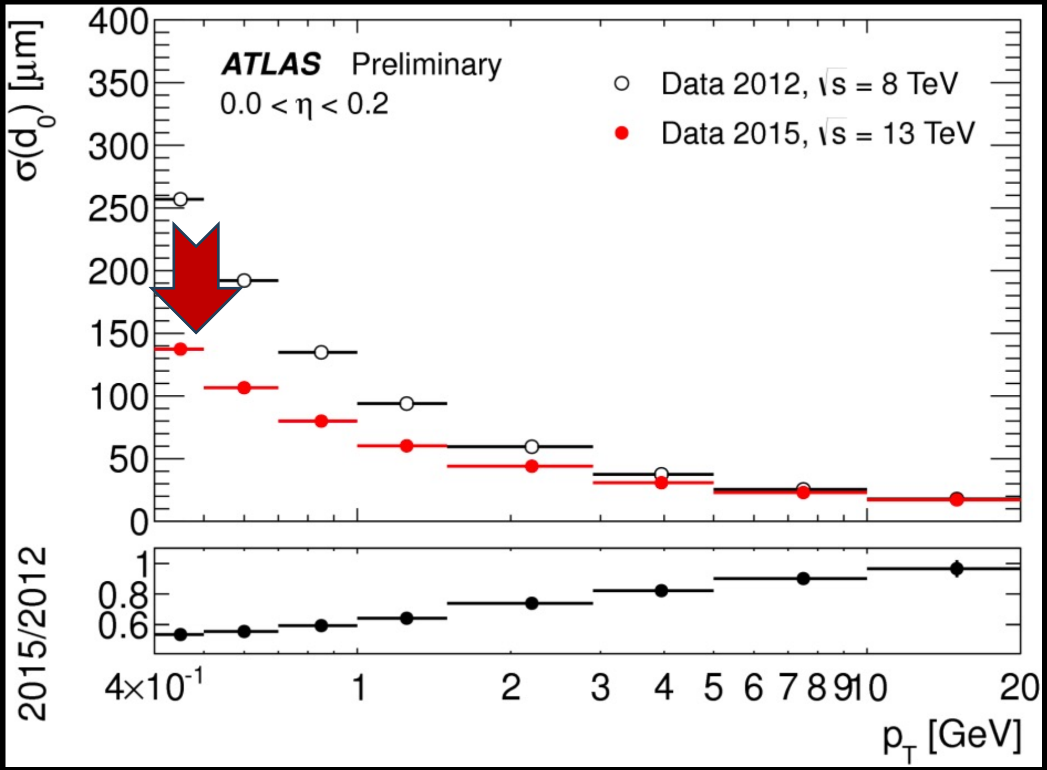
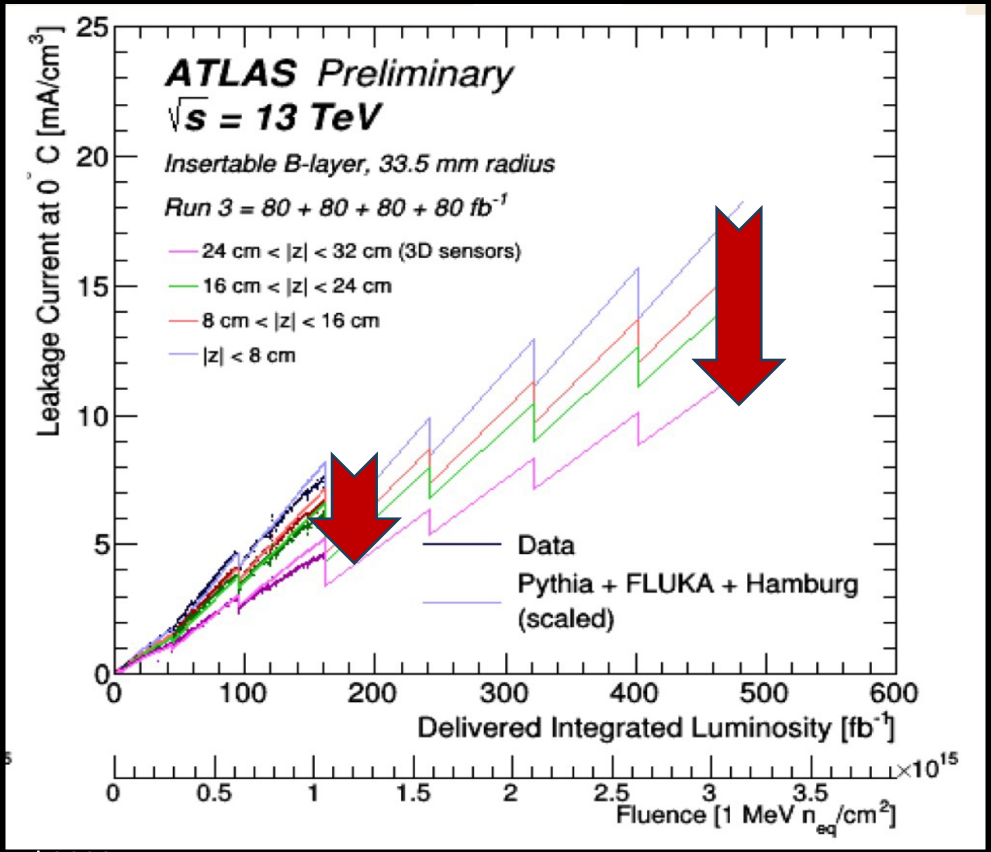
Resolution improvement

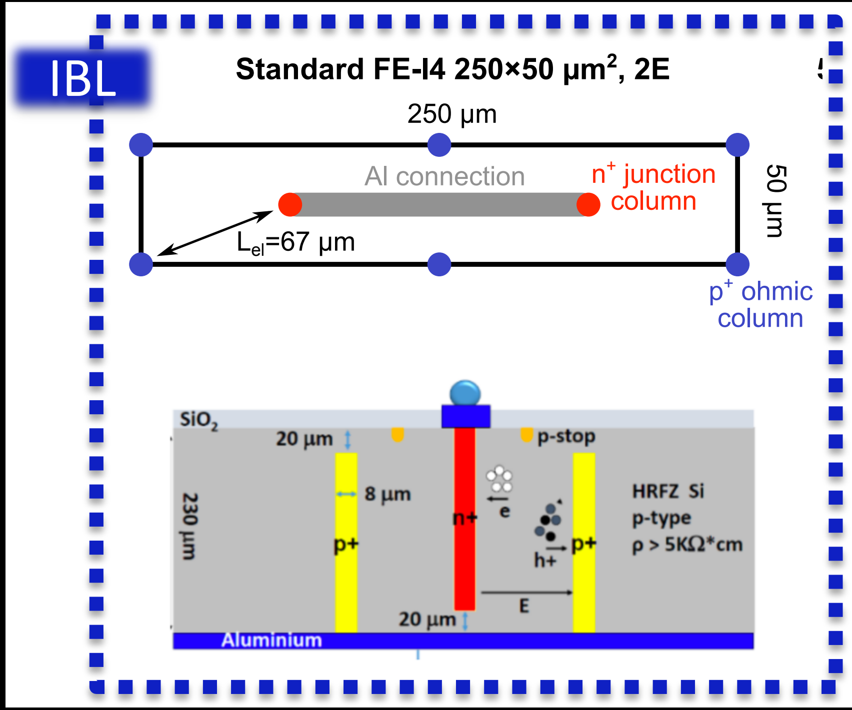


Operational experience with 3D sensors

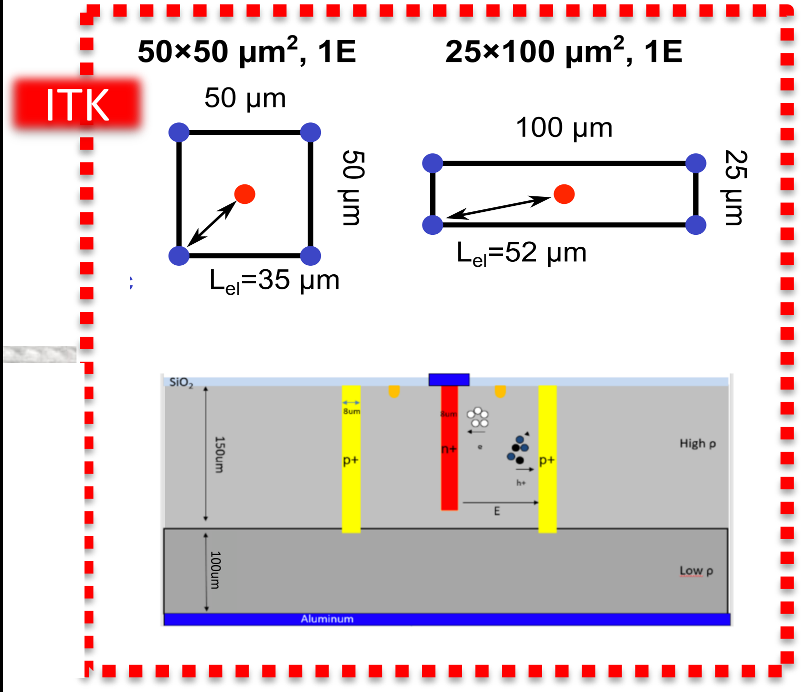


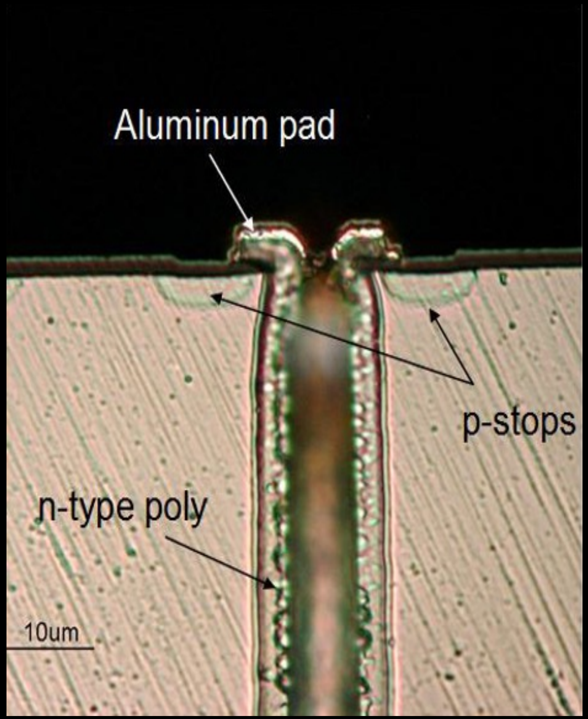
ITk 3D fabrication improvements

IBL: Double sided



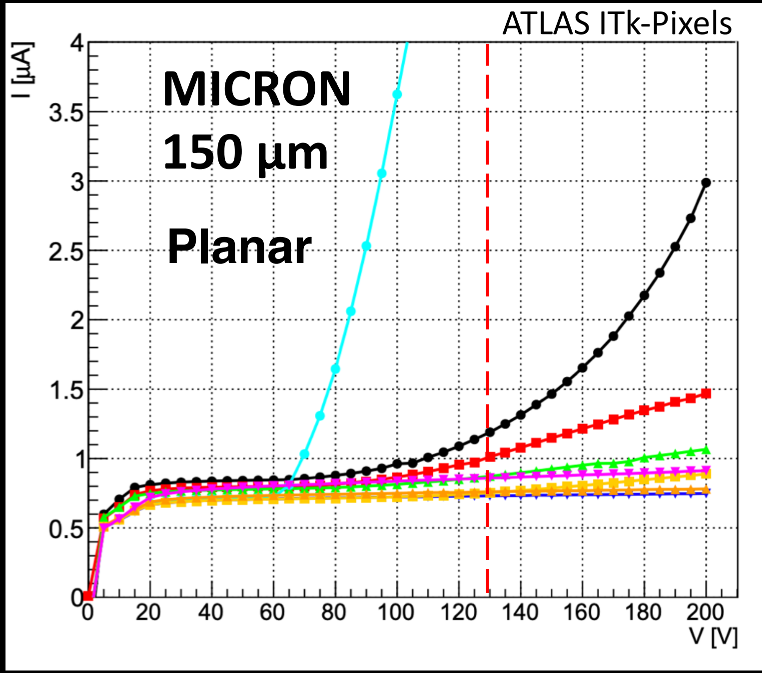
ITK: Single sided fabrication

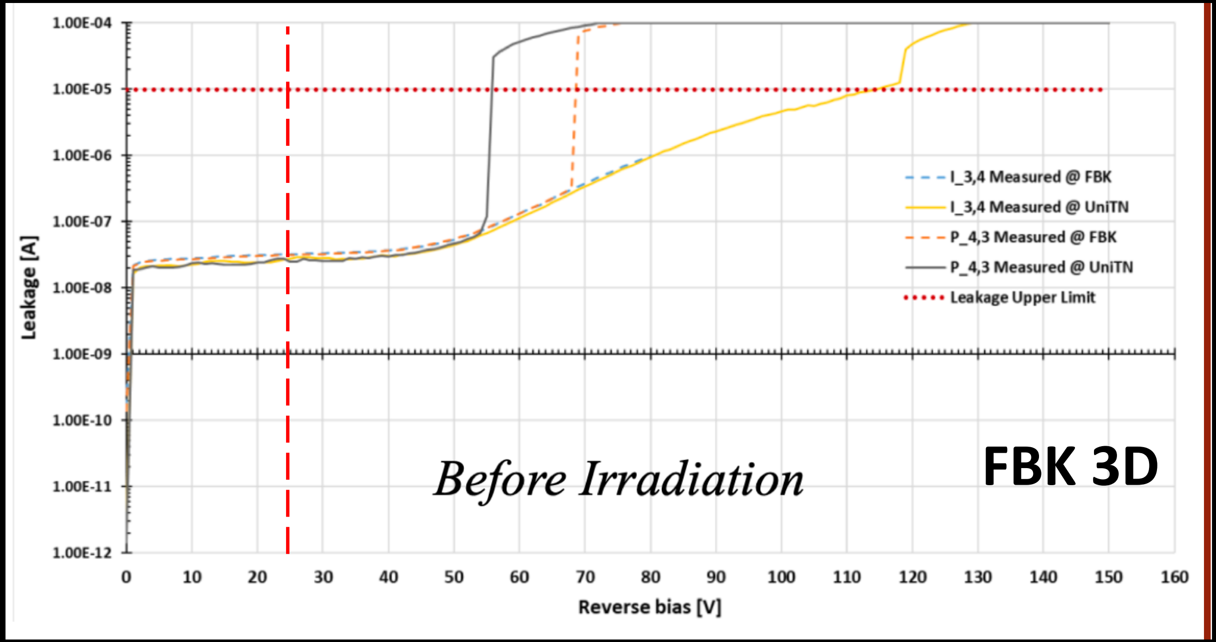




- All electrodes are etched from the front-side and filled with poly-Si
- The junction (readout) columns stop at a distance of ~25 μm from the handle wafer to avoid breakdown
- The ohmic (bias) columns are etched deeper and penetrate into the handle wafer.
- The sensor bias can be applied from the back-side.
- 150 μm thin and cell size: 50x50 μm^2 in the rings and 25x100 μm^2 in barrel

Leakage current





Before irradiation:

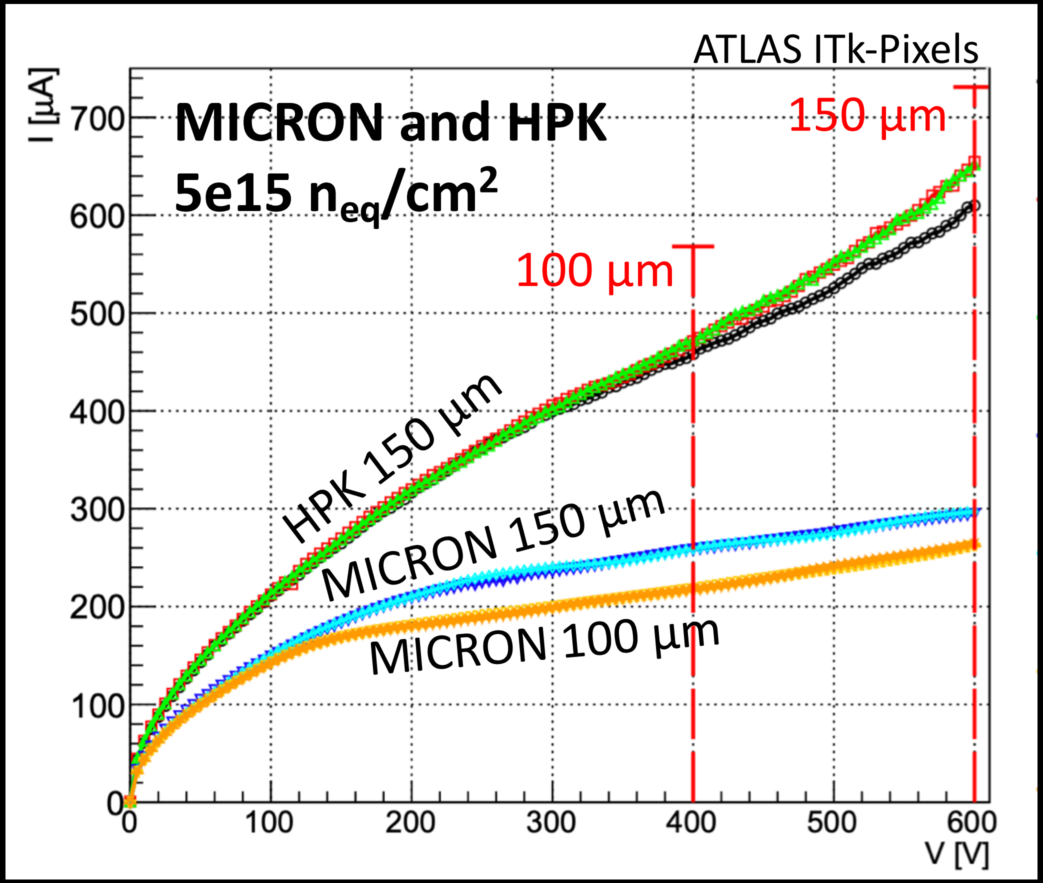
- Good sensors need to have a breakdown >130V
- Most of the sensors have a larger breakdown >200V

Leakage current measured as a function of the reverse bias voltage (IV) for FBK sensors is within specs:

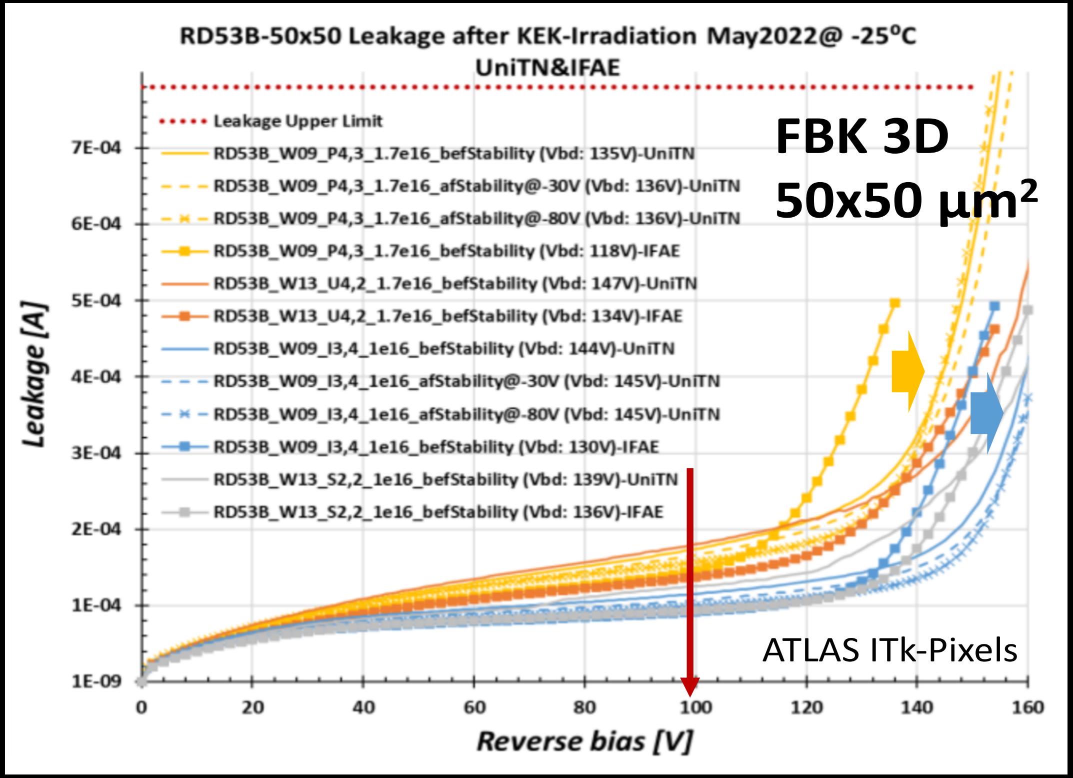
- Breakdown > 25V
- Leakage current < 2.5 µA/cm^2

Leakage current

- Planar sensors after 5x 10^{15} n_{eq}/cm^2

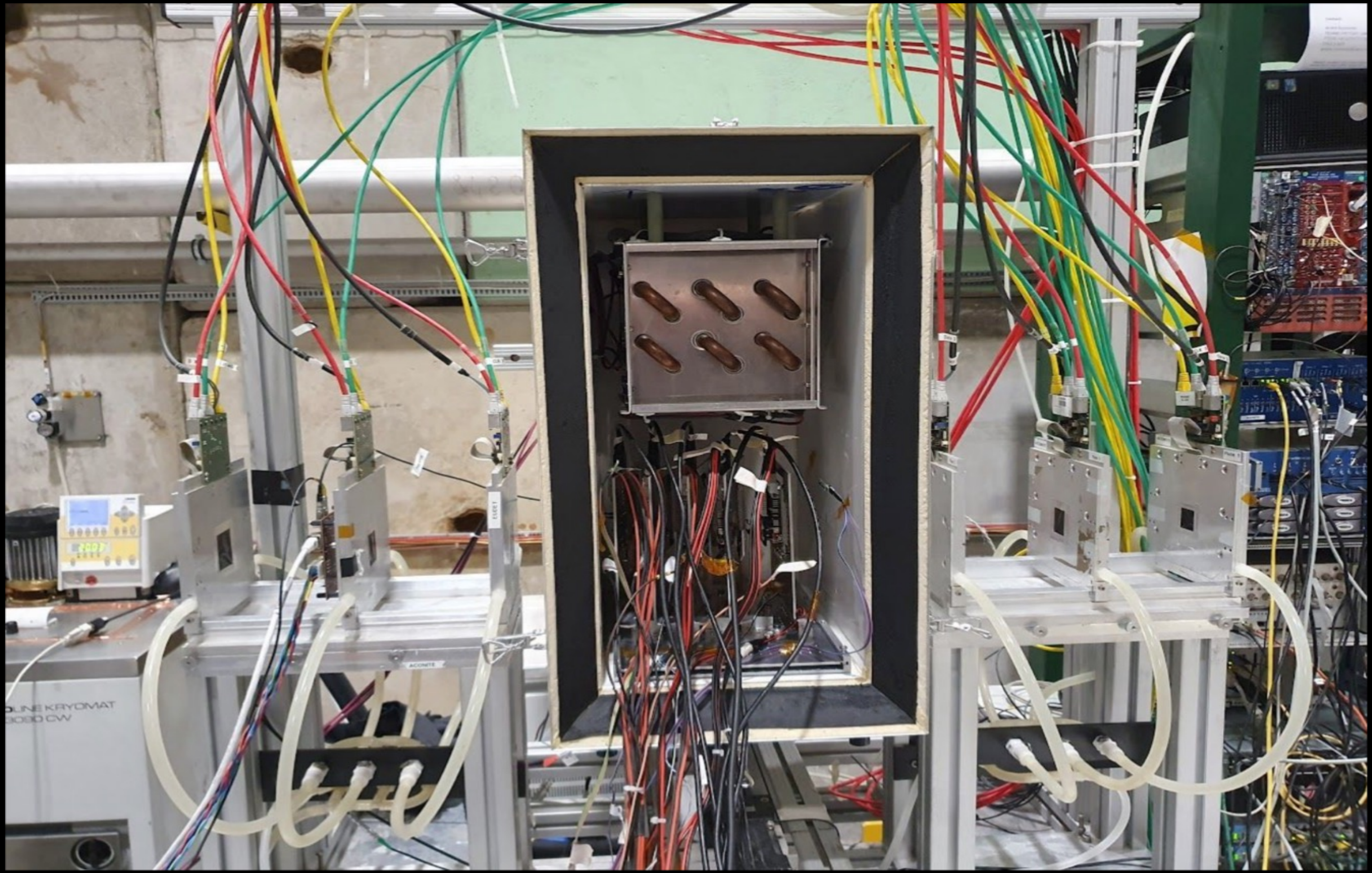


- 3D diodes and bare sensors irradiated to 1 x 10^{16} and 1.7 x 10^{16} n_{eq}/cm^2
- Breakdown shifts towards higher voltage after annealing and/or stability tests (IT - 48h under bias)



Test beam

Detector Under test

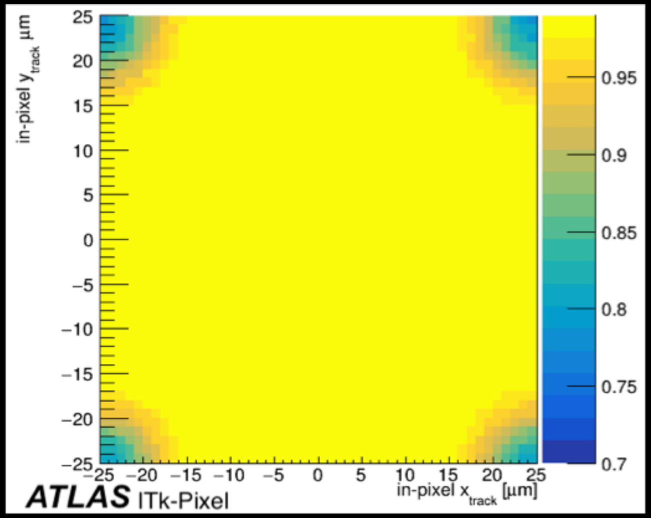


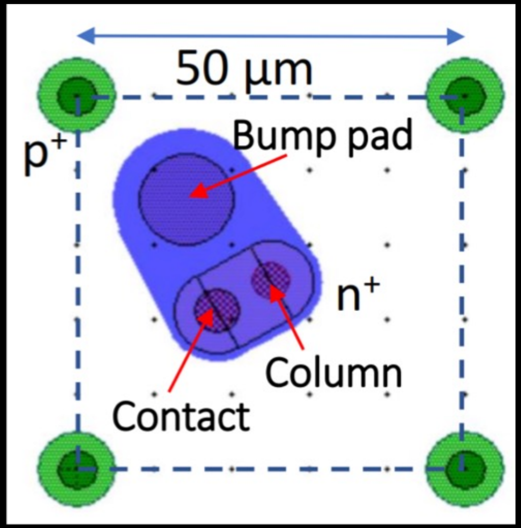
EUDET Telescope

SPS (~120 GeV pion beam)

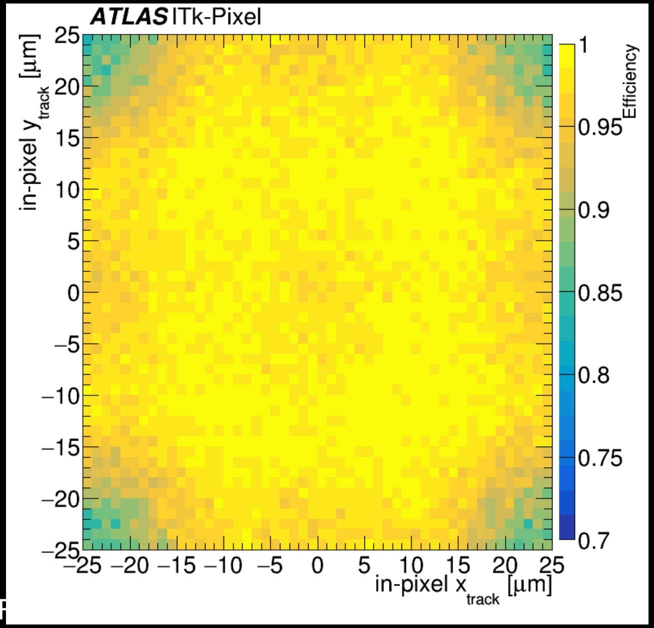
3D sensors for HL-LHC

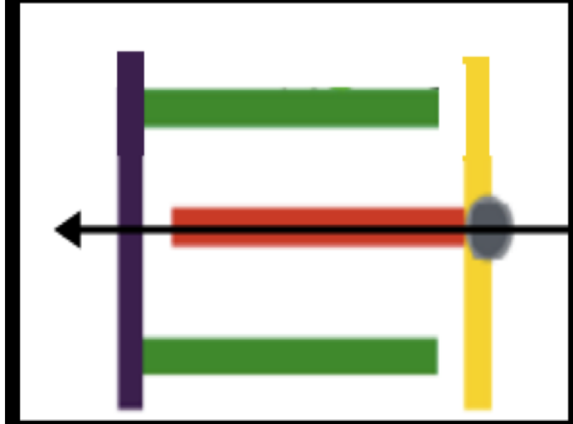
- Before irradiation
  - hit efficiency > 97% with just a few V
  - Inefficiency localised in the full passing p-columns





- After irradiation
  - Hit efficiency >97% with just 40 V after 1x 10^{16} n_{eq}/cm^2
  - Hit efficiency > ~97% with just 100 V after 1x 10^{16} n_{eq}/cm^2





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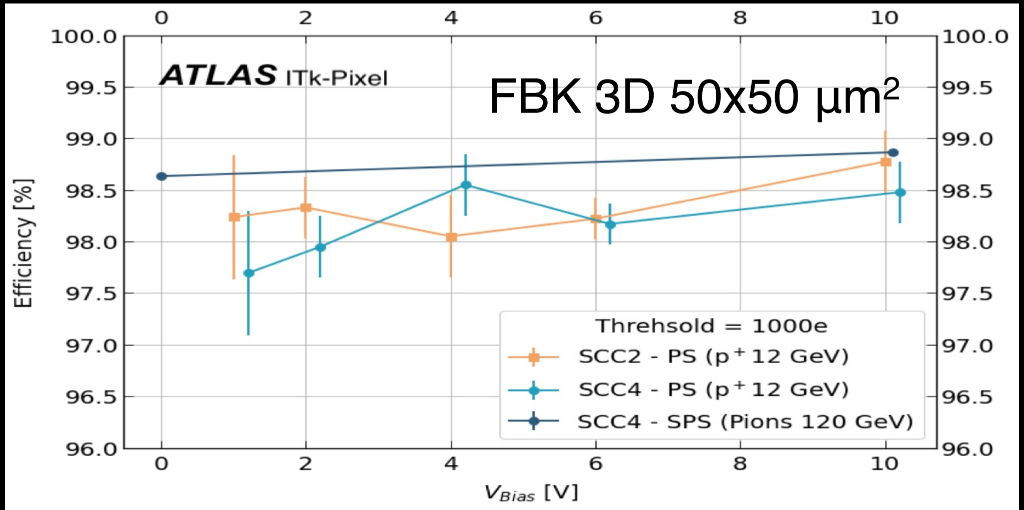

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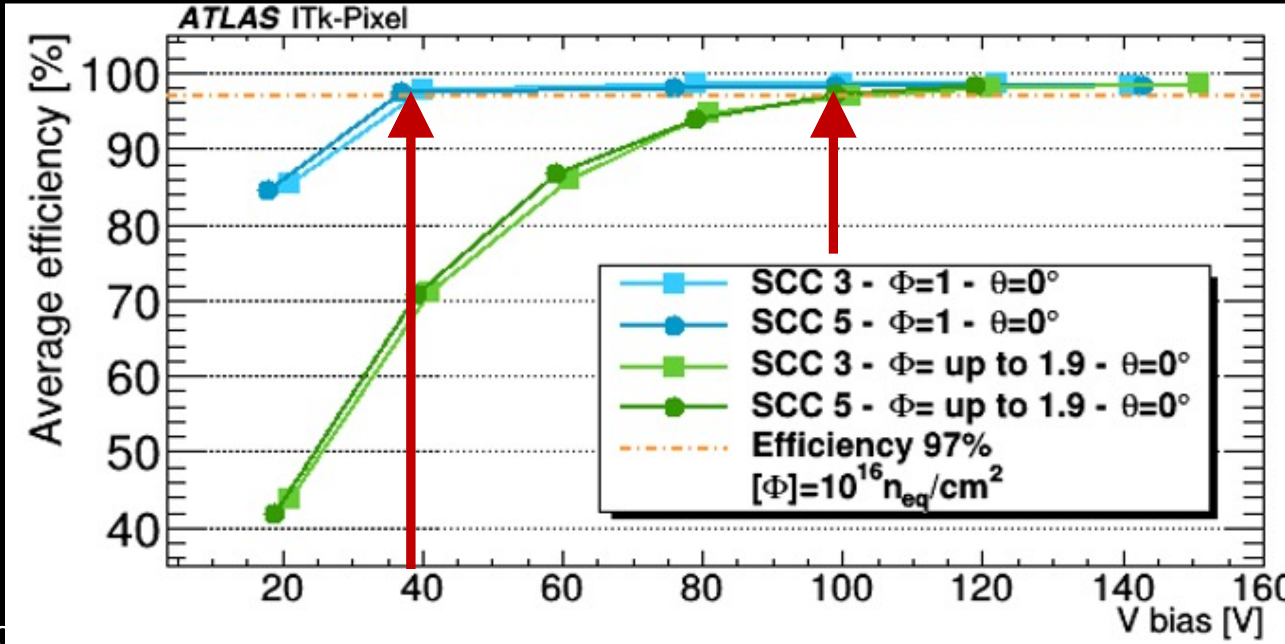
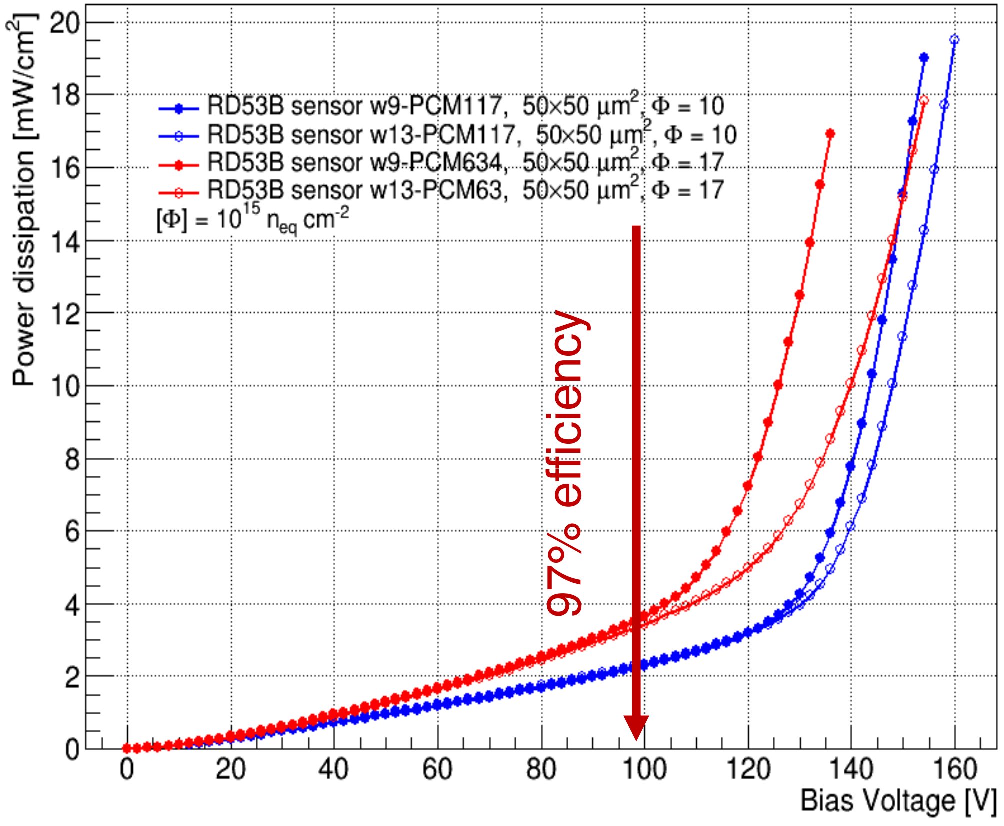


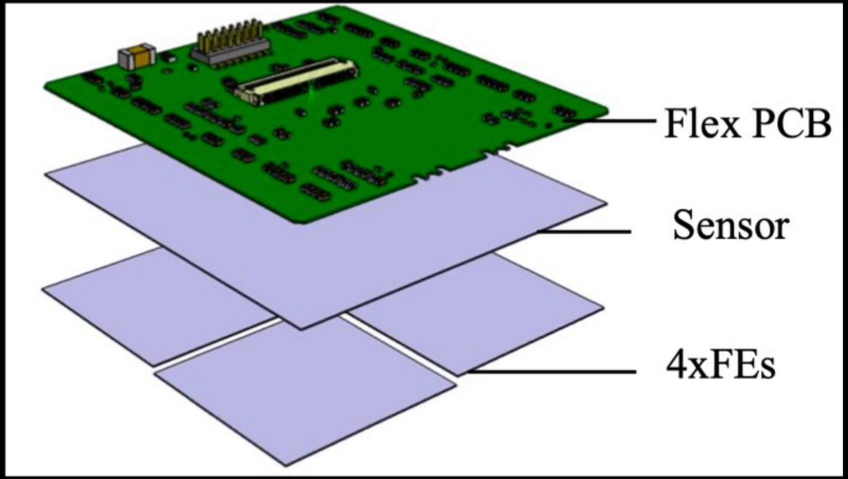
3D sensors for HL-LHC

- **Power dissipation is critical for innermost pixel layer**
  - At $V_{operation}$ (i.e. efficiency > ~ 97%) the sensor power must be less than 40 mW/cm^2
  - Sensors can be operated within these limits after irradiation up to 1.7x 10^{16} n_{eq}/cm^2
  - The power dissipation at the operational voltage can be kept below 10 mW/cm^2 at -25°C

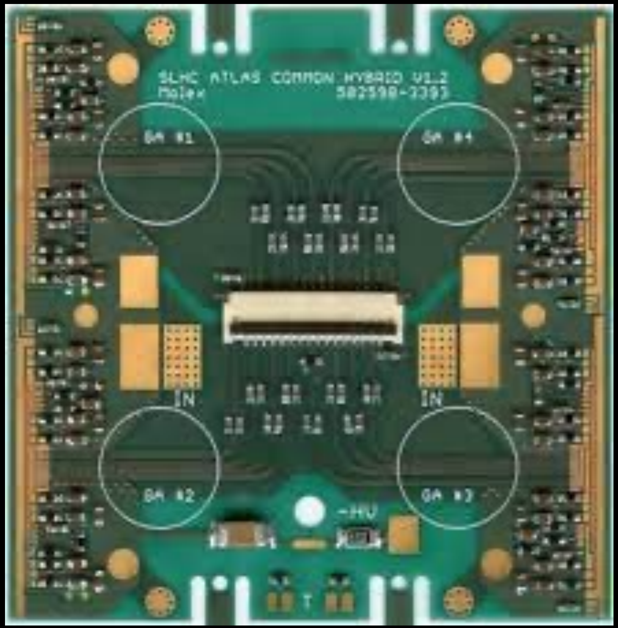
FBK 3D 50x50 µm^2



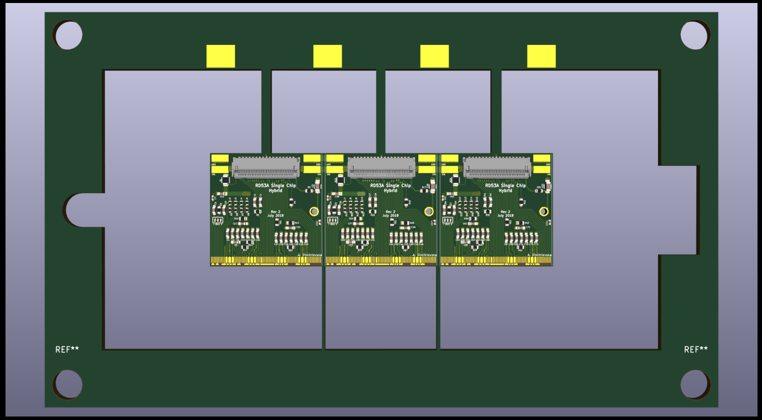
Modules

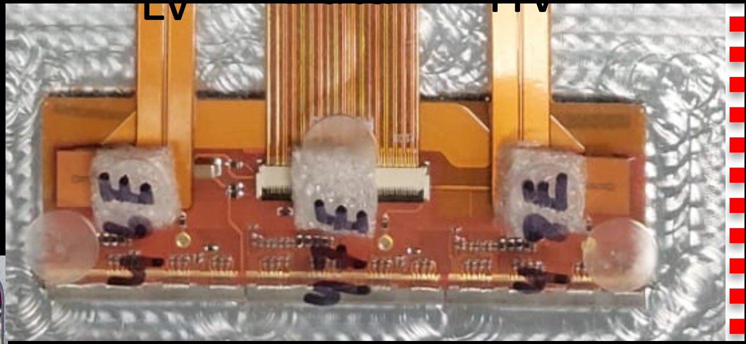


Planar- Quad

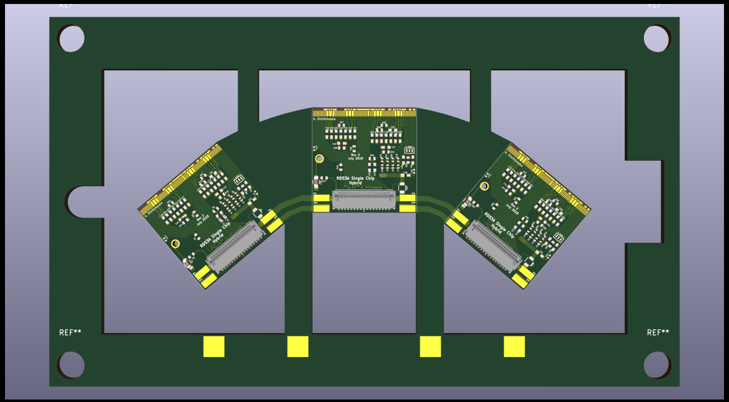


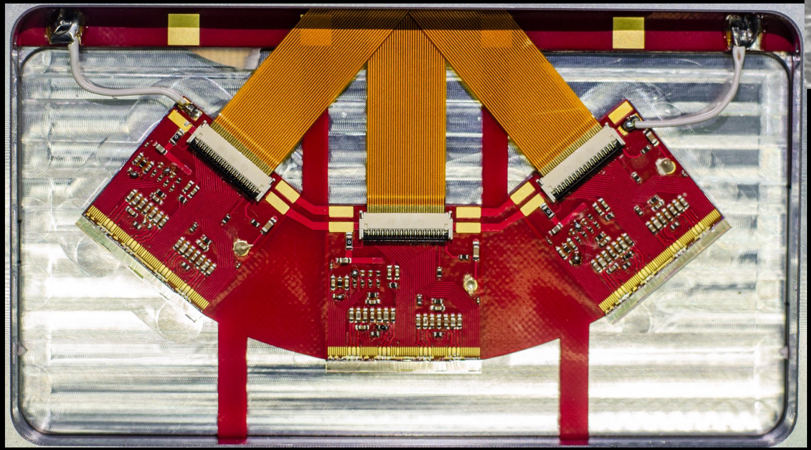
3D – Triplets Barrel





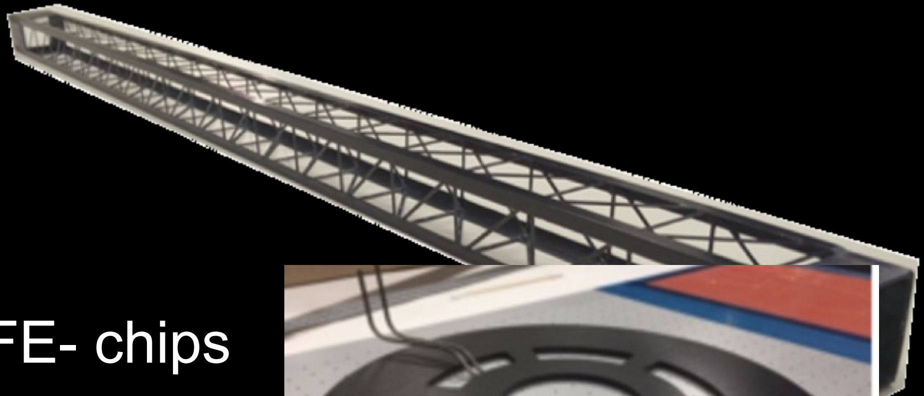
3D – Triplets Ring

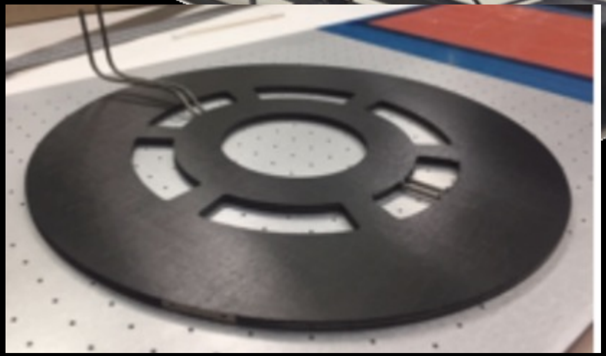


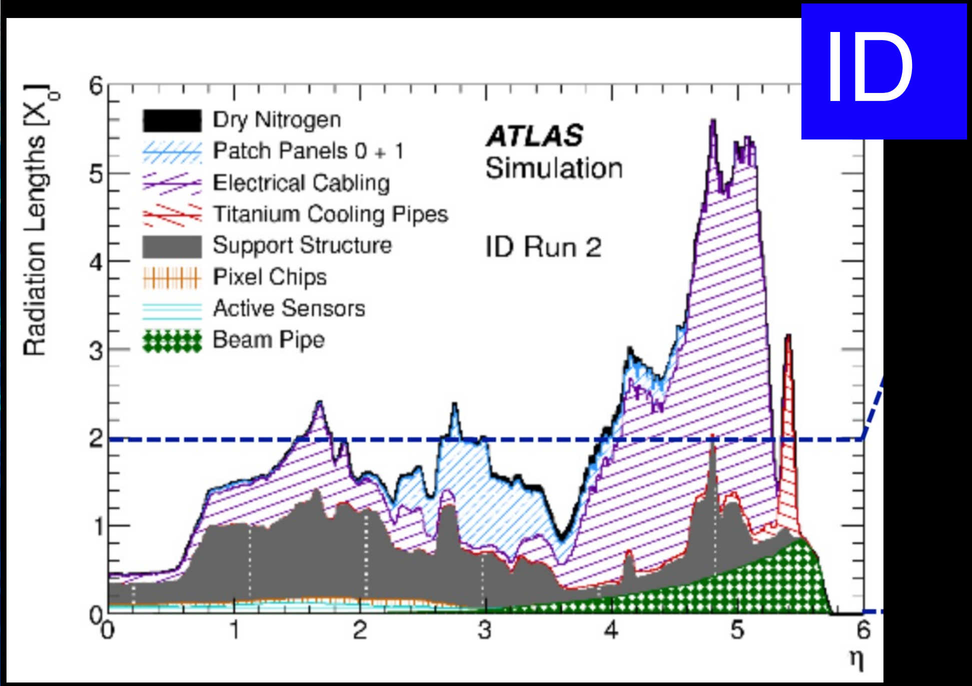


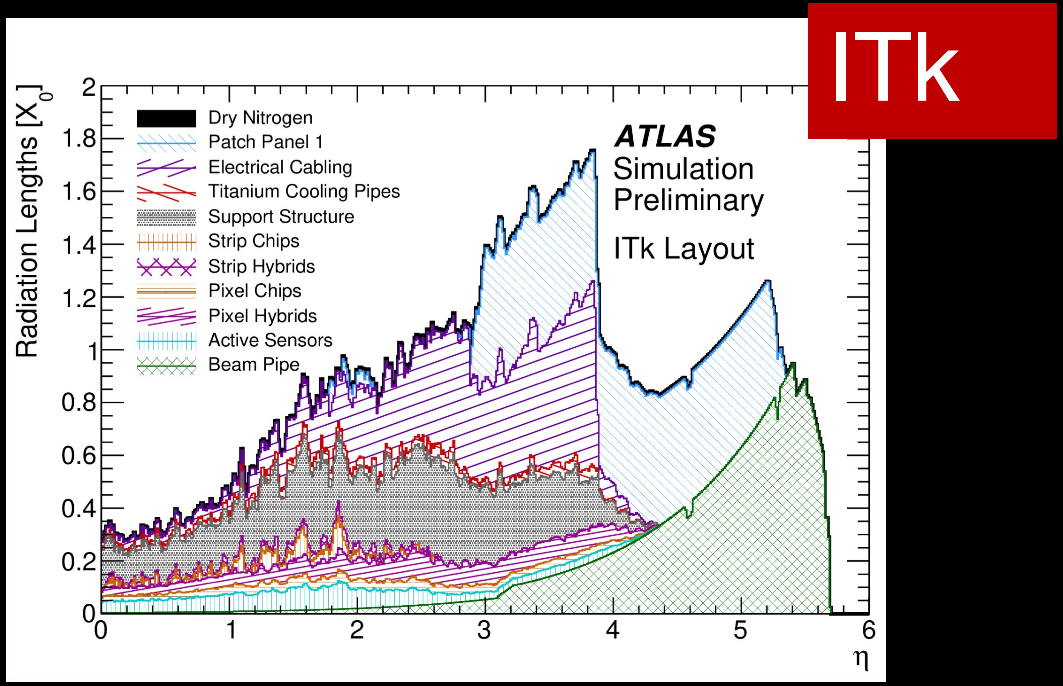
Material

- Reduce of material using
  - CO_2 cooling with thin titanium pipes
  - Minimise material in modules using thin Si and FE- chips
  - Advanced powering: serial powering for pixels
  - Carbon structures for mechanical stability and mounting
  - Optimise number of readout cables using data link sharing



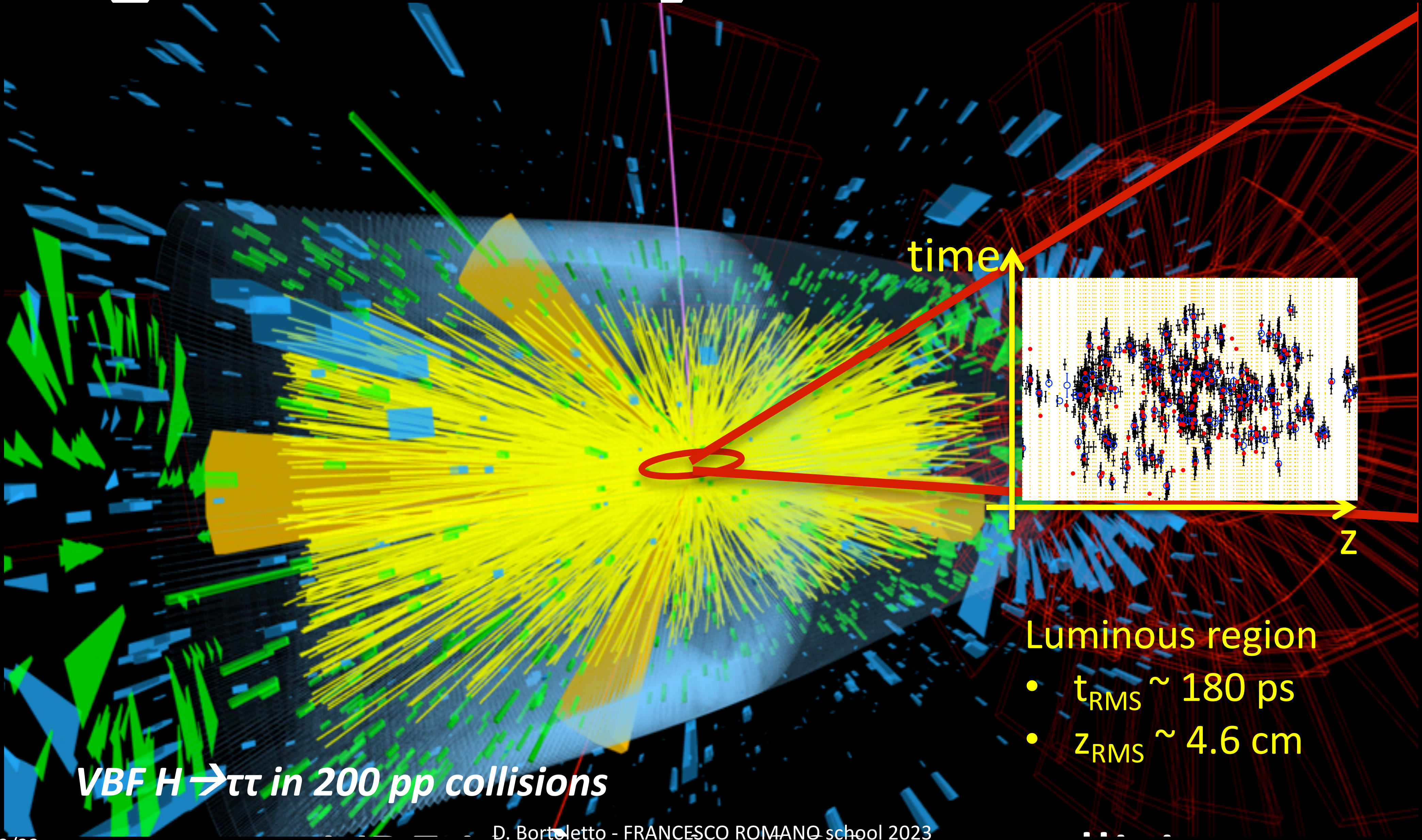




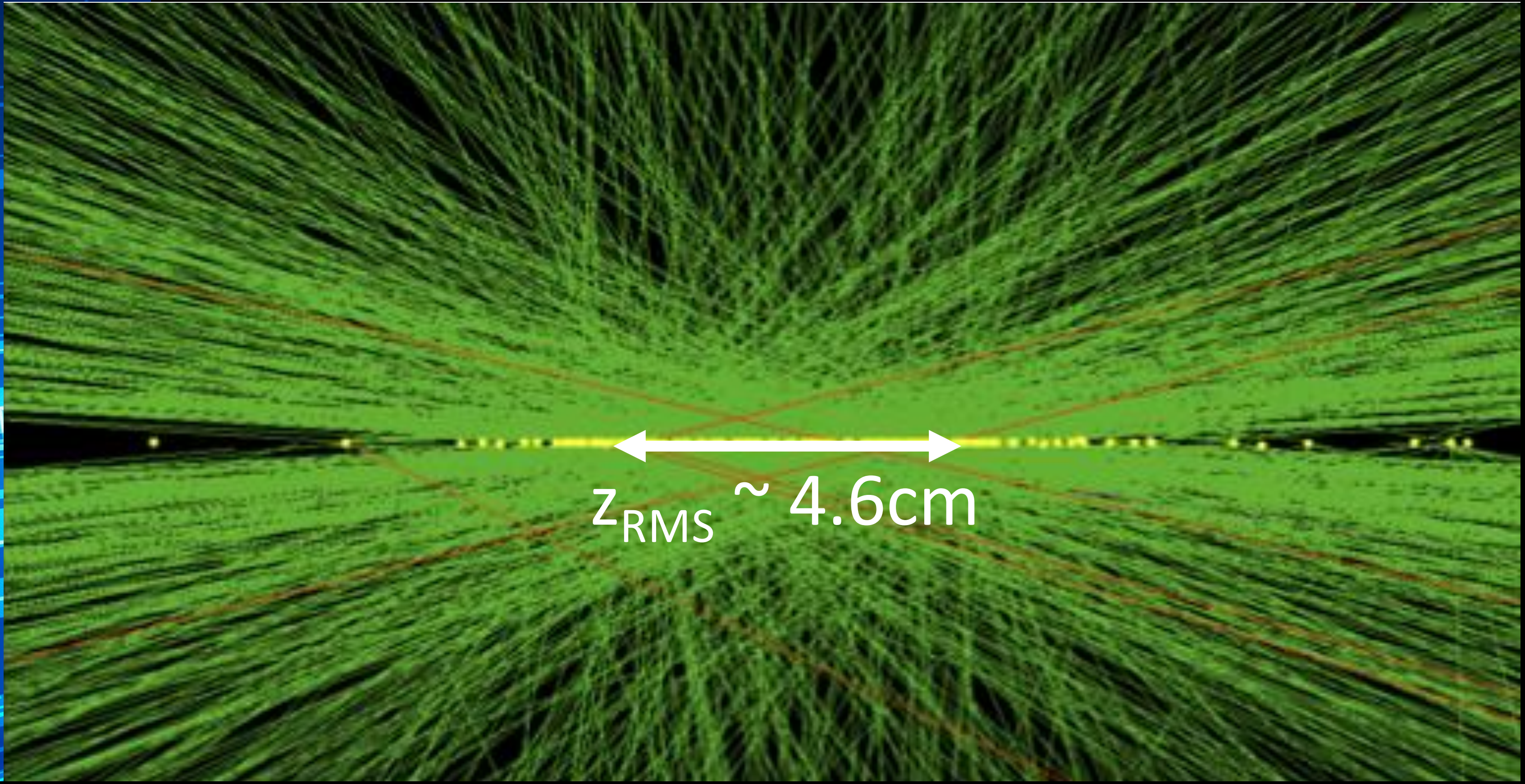


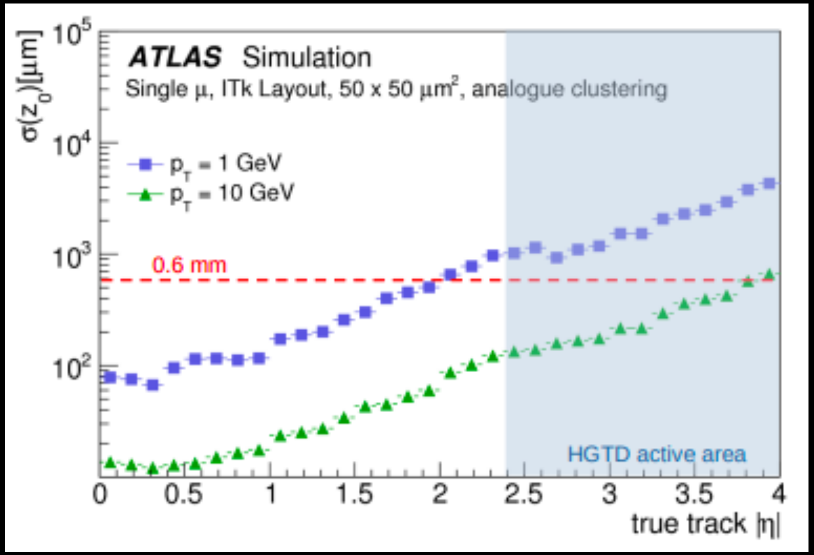
TIMING

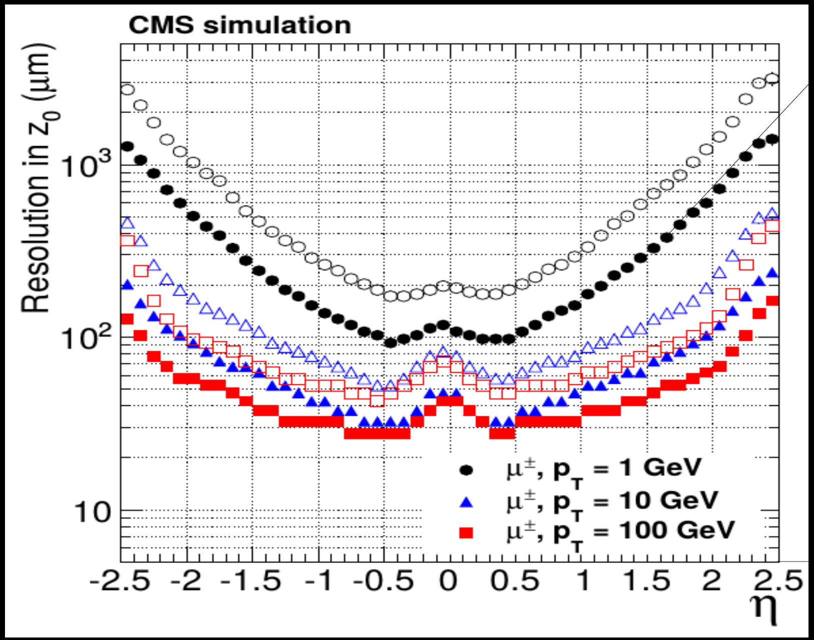
High-Luminosity LHC



HL-LHC Vertex efficiency



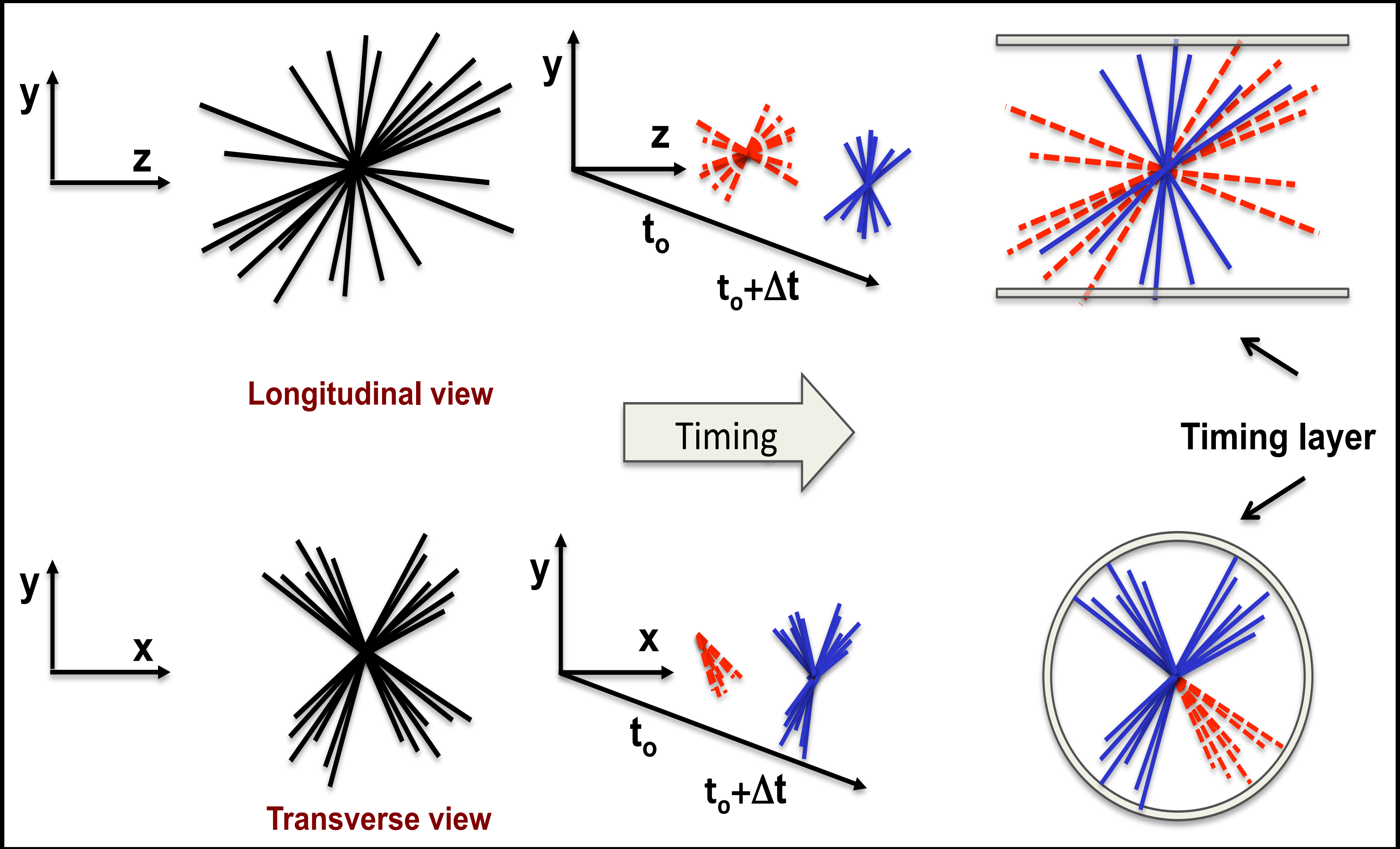




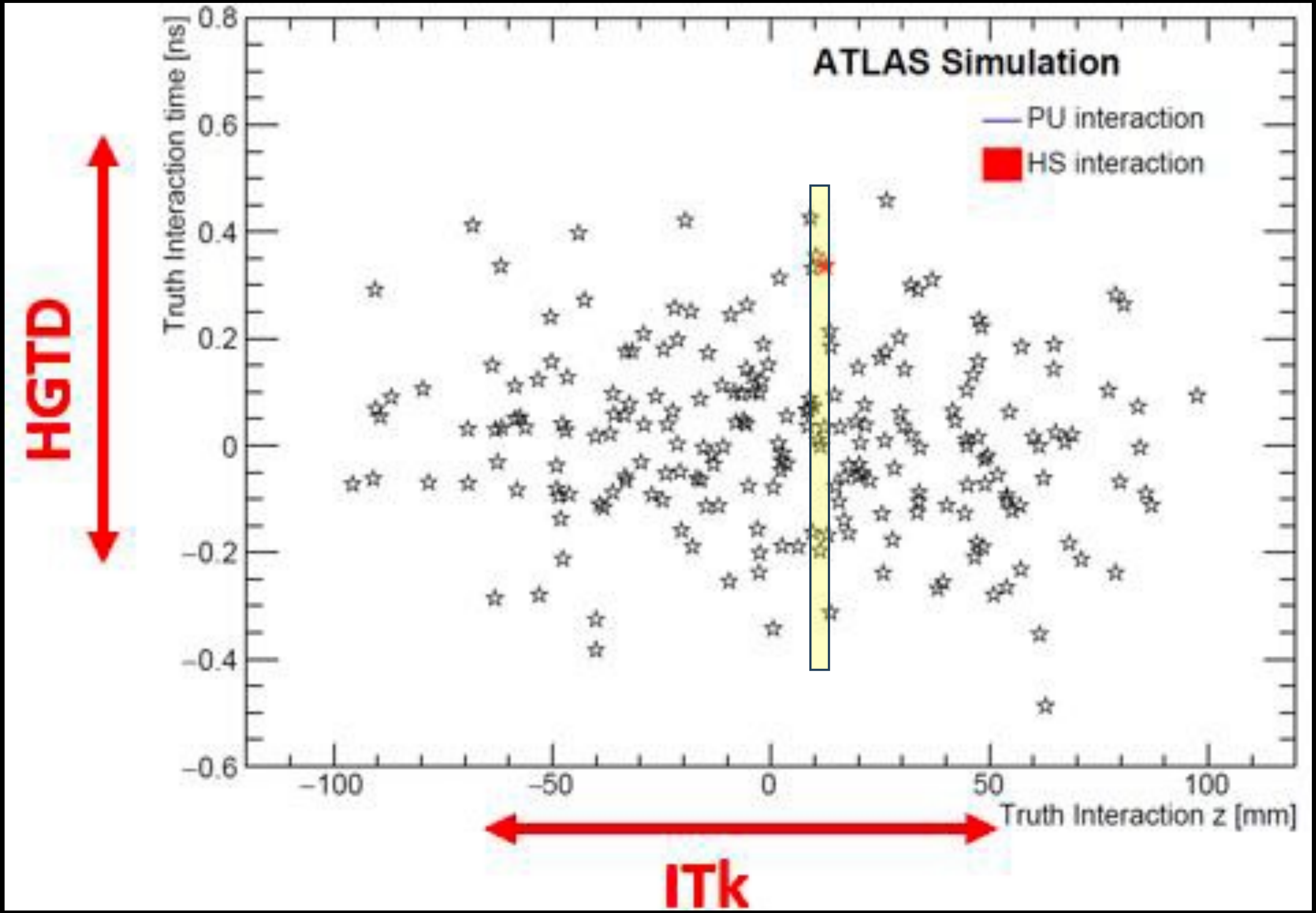
HL –LHC:

- Instantaneous luminosity up to 7.5×10^{34} $cm^{-2}s^{-1}$
- Pileup: <μ>= 200 interactions/bunch crossing ~1.6 vertex/mm on average

Time-Aware Vertexing

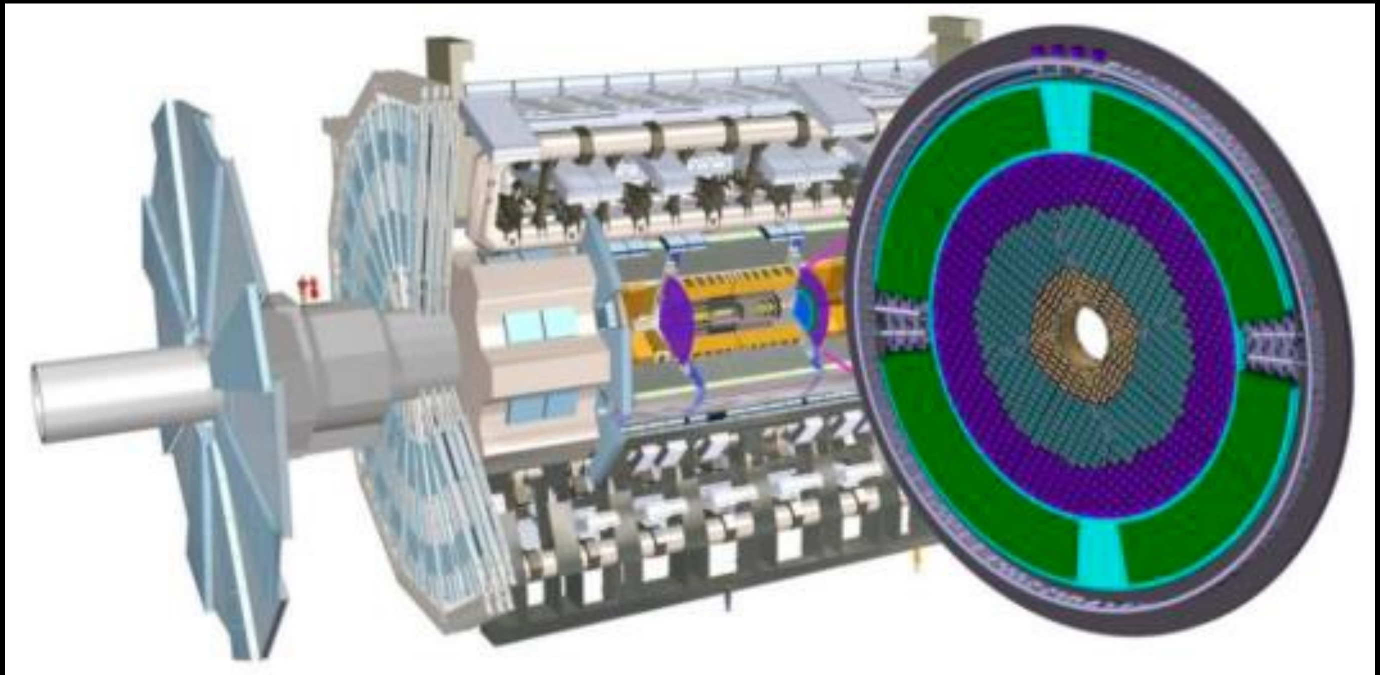


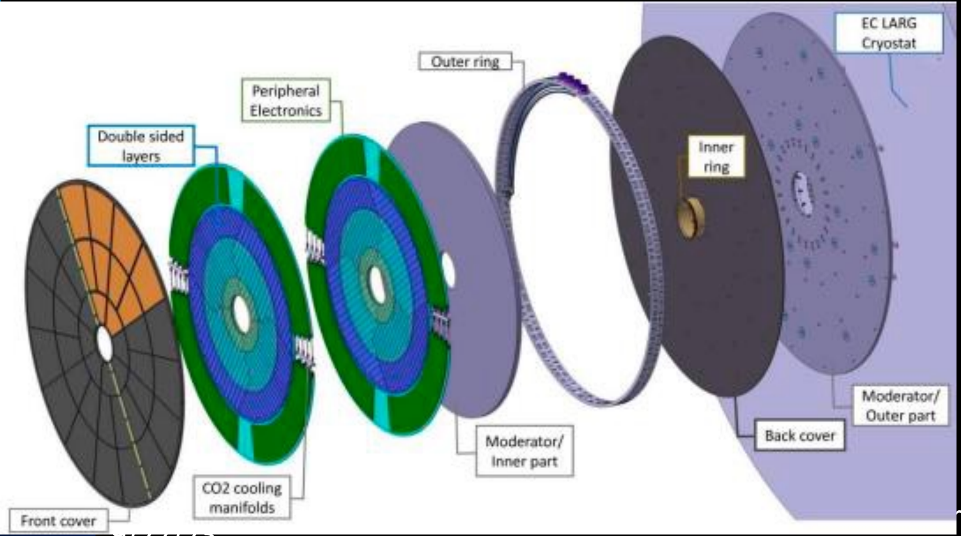
4D Vertex Reconstruction



ATLAS HGTD

- The High Granularity Timing Detector (HGTD) provides precise timing information
  - ~3.6 million 1.3x1.3 mm^2 pixels (channels)
  - 6.4 m^2 active area
  - Time resolution target
  - 30-50 ps/track
  - 35-70 ps/hit up to 4000fb^{-1}



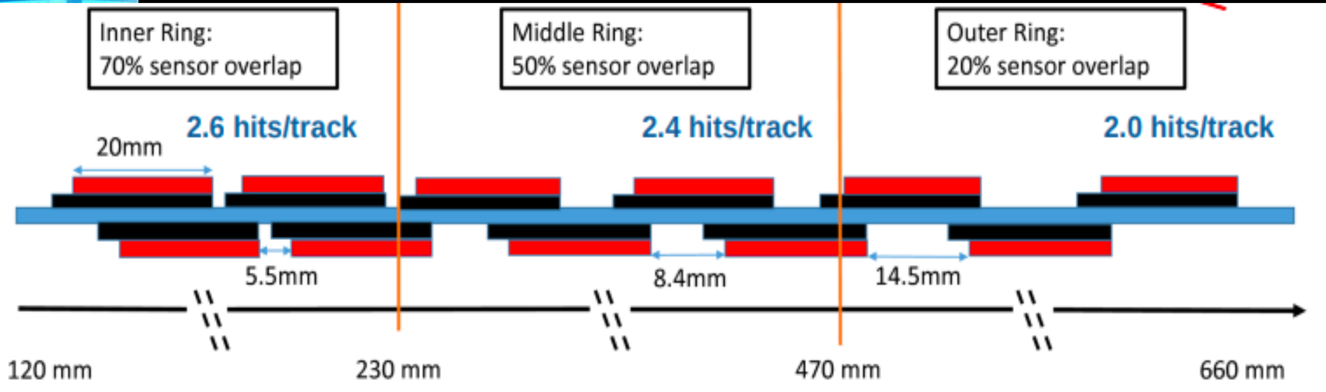


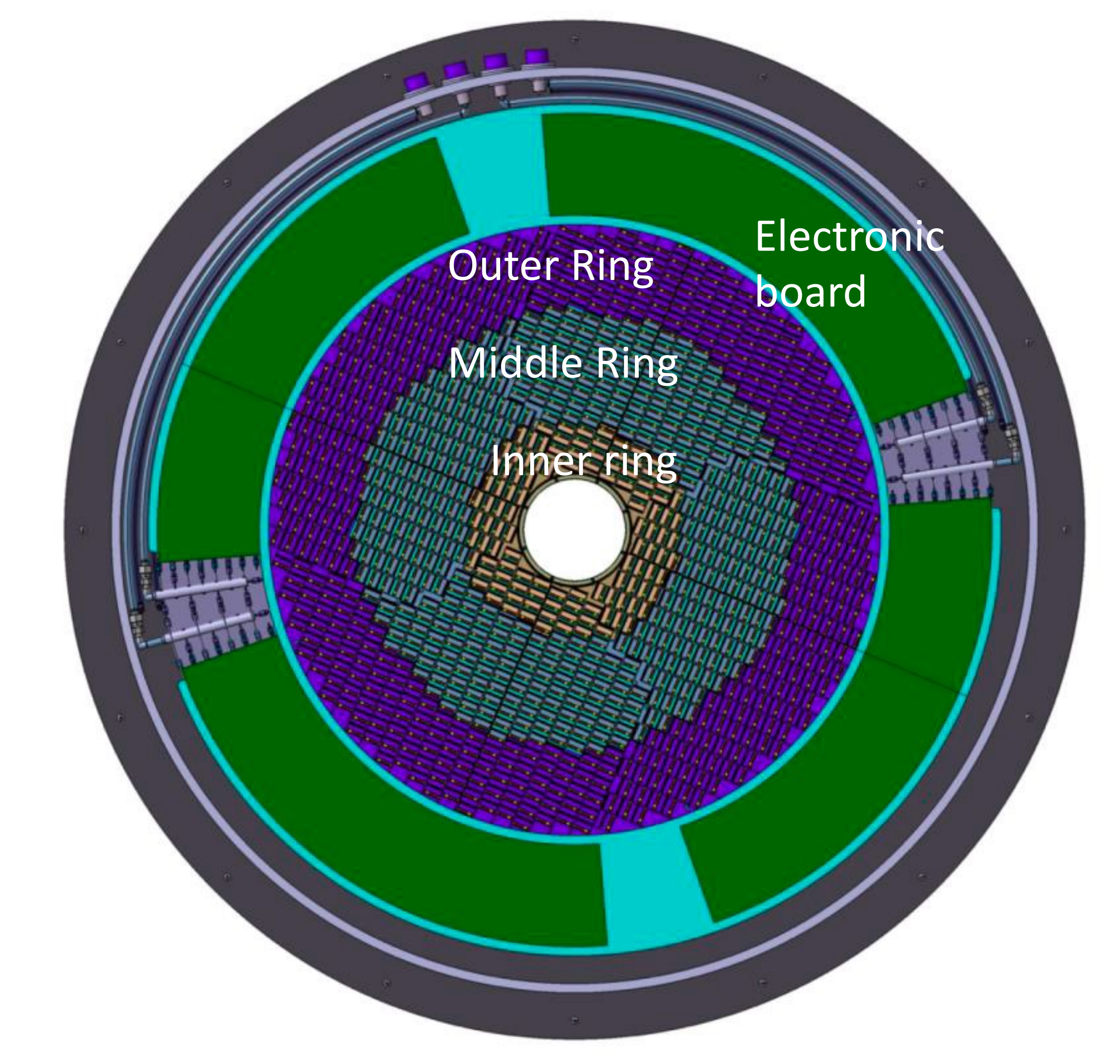
- **Two end-caps**
  - z ≈ ±3.5 m from the nominal interaction point
  - Total radius: 11 cm < r < 100 cm
  - Active detector region: 2.4 < |η| < 4.0
- Each end-cap
  - Two instrumented disks, rotated by 15° for better coverage

ATLAS HGTD

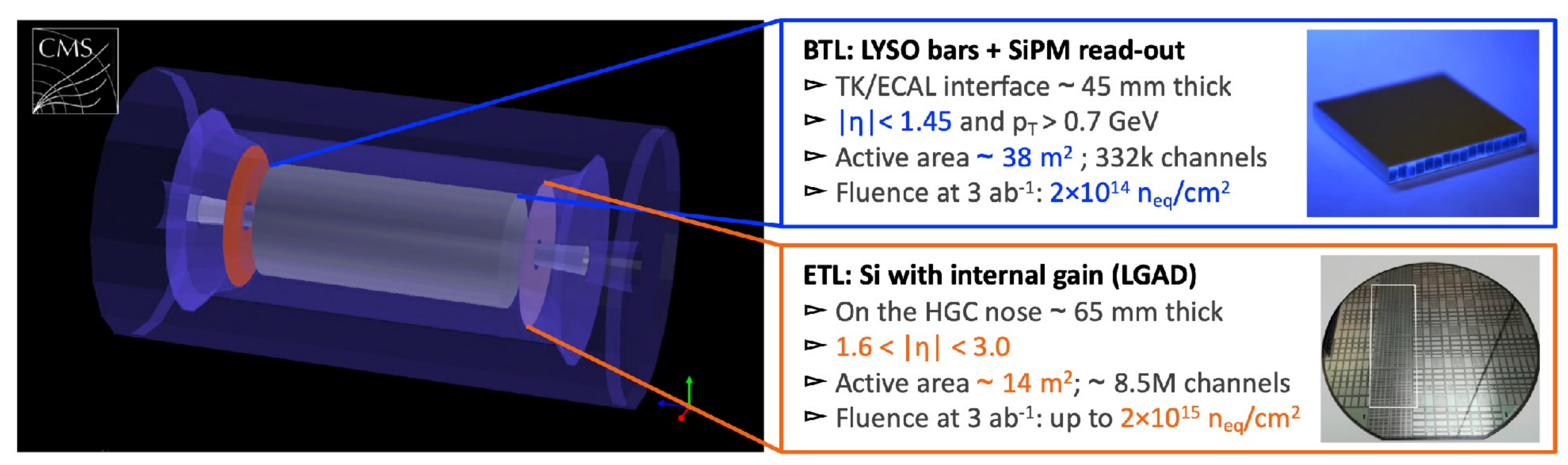
Each Disk:

- Double-sided layers mounted on a cooling plate
- 3 rings layout because of the different fluence
- Overlap between modules on inner, middle and outer ring
- Replacement of inner ring every 1000 fb^{-1} and middle ring at 2000 fb^{-1} to maintain performance

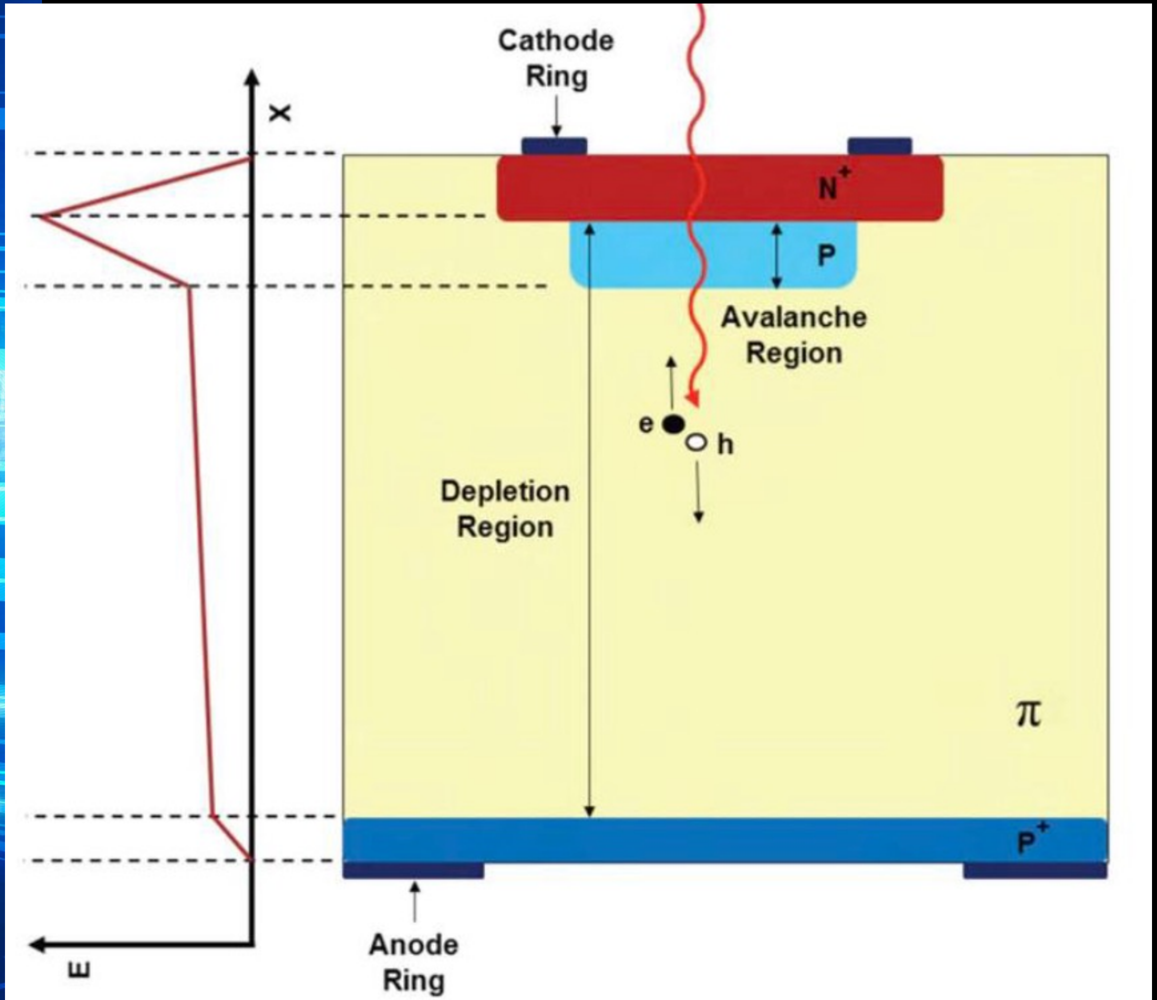




CMS: Mip Timing Detectors

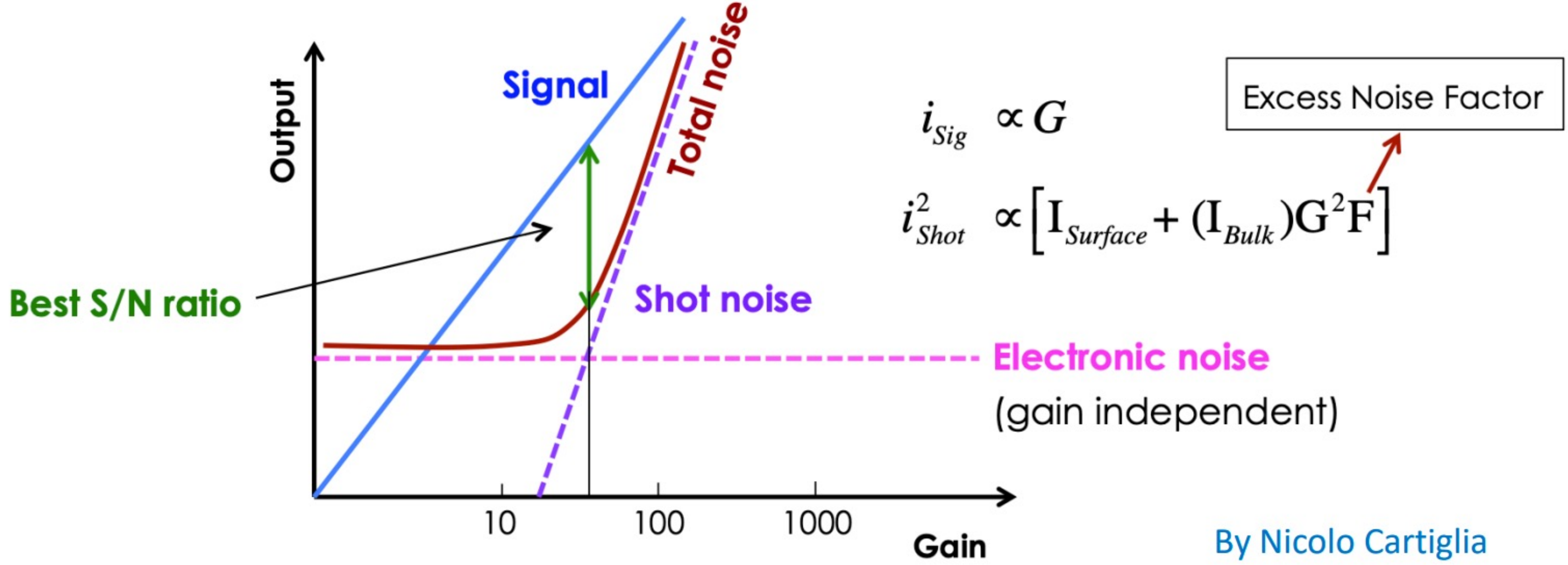


Low-Gain Avalanche Detectors (LGADs)



- Bulk region "π" is moderately doped
- Heavily doped "N" ("avalanche" or "gain") layer creates high field
- Heavily-doped "N^+" implant is very thin (standard for silicon diode detectors)
- With large doping concentrations close to the implant, the field can get very large
- For fields $\simeq 3x10^5$ V/cm, energy becomes large enough to create another electron-hole pair
- Limited avalanche
- GAIN typically in the 10-100 range

Why low gain



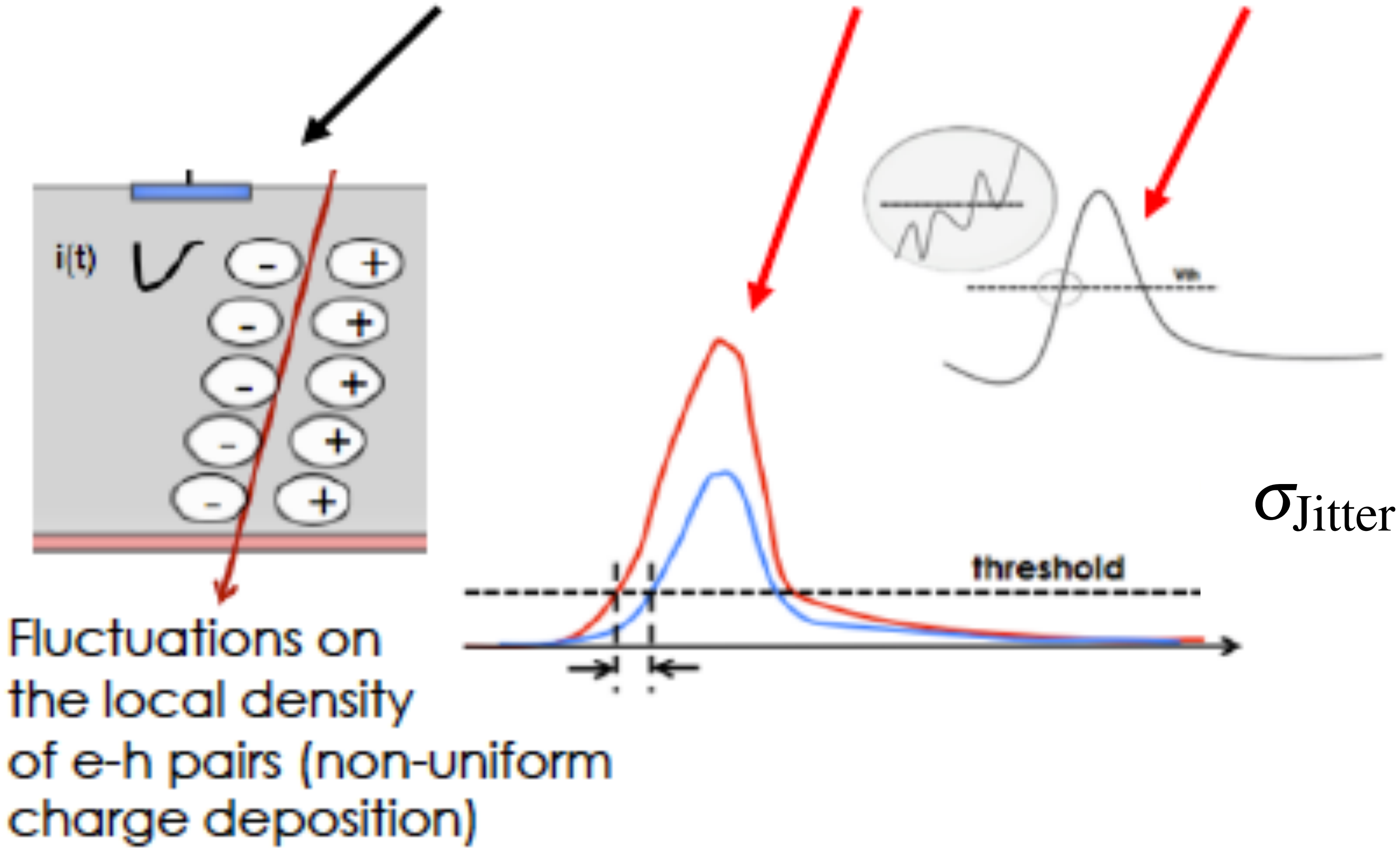
Noise increases faster than then signal

→ the ratio S/N becomes worse at higher gain

https://doi.org/10.1201/9781003131946

LGAD Timing Precision

$$\sigma_t^2 = \sigma_{Landau}^2 + \sigma_{time-walk}^2 + \sigma_{jitter}^2 + \sigma_{TDC}^2 + \sigma_{clock}^2$$

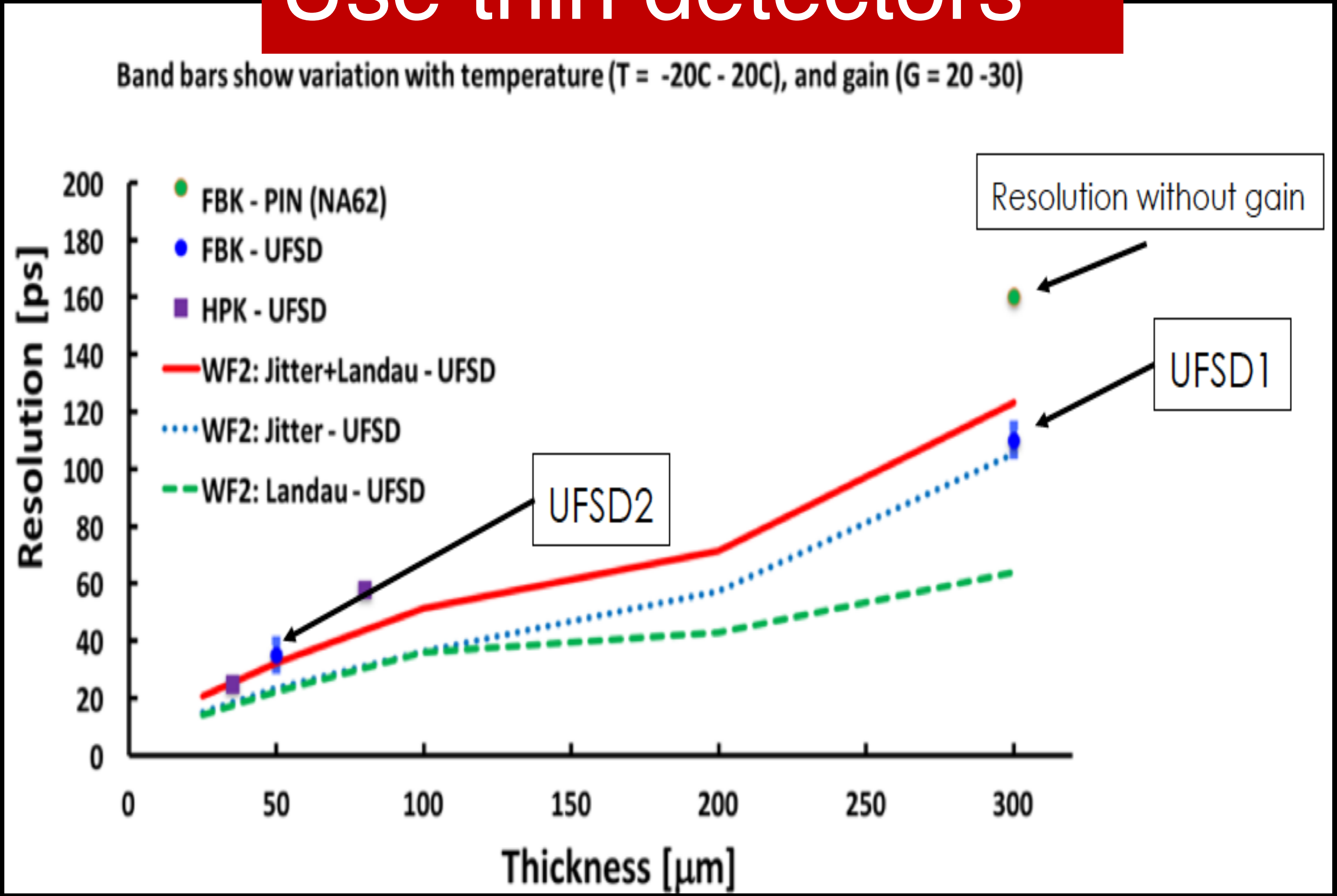


$$\frac{20ps}{\sqrt{12}} \sim 5ps$$

$$\sigma_{Jitter} = \frac{N}{dV/dt}$$

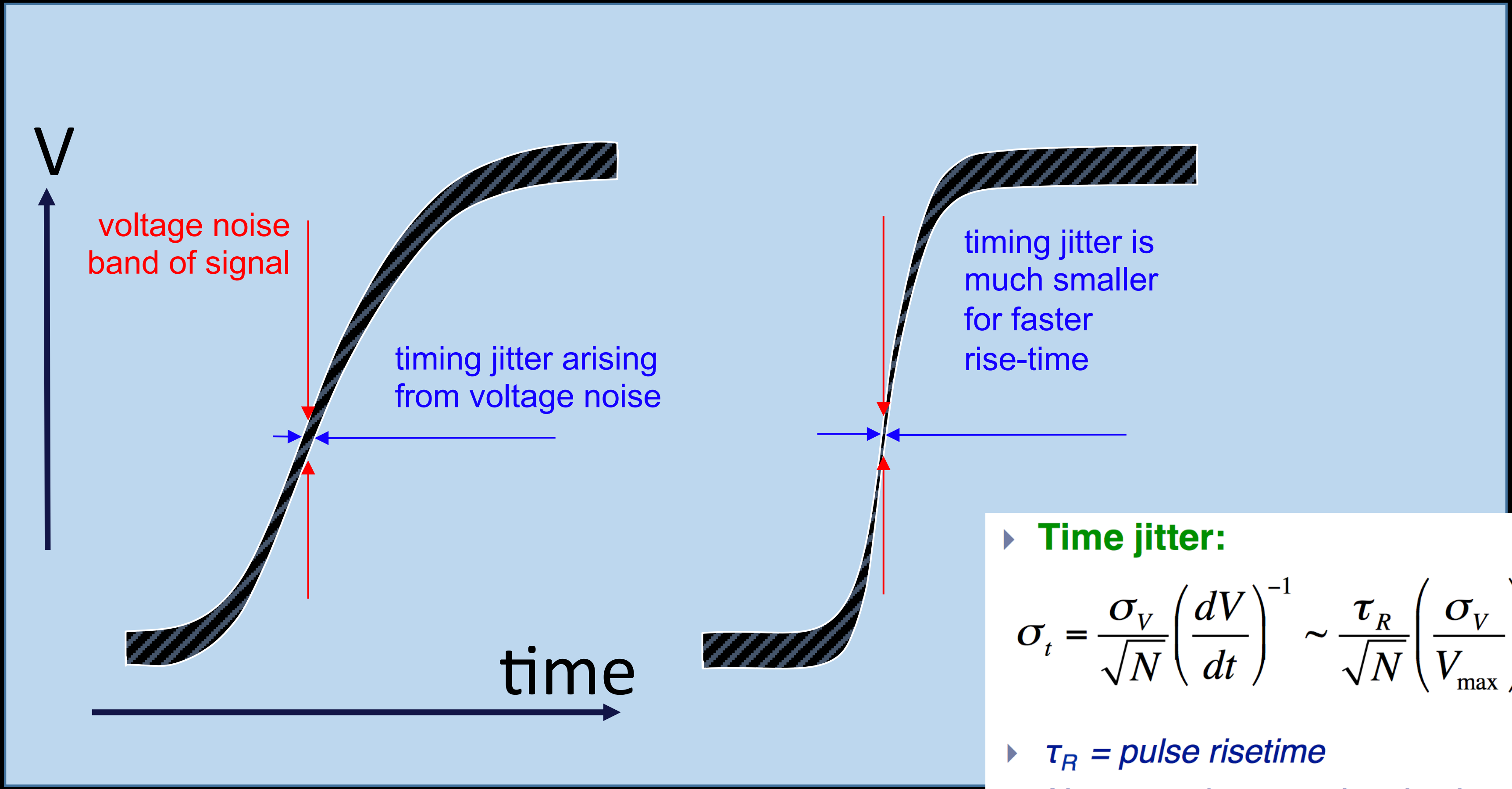
LGAD Timing Precision: Landau

Use thin detectors



LGAD Timing Precision: Jitter

- "Jitter" Contribution:
  - Noise fluctuations lead to premature or late crossing of threshold
  - Exacerbated by slow rise time



- **Time jitter:**

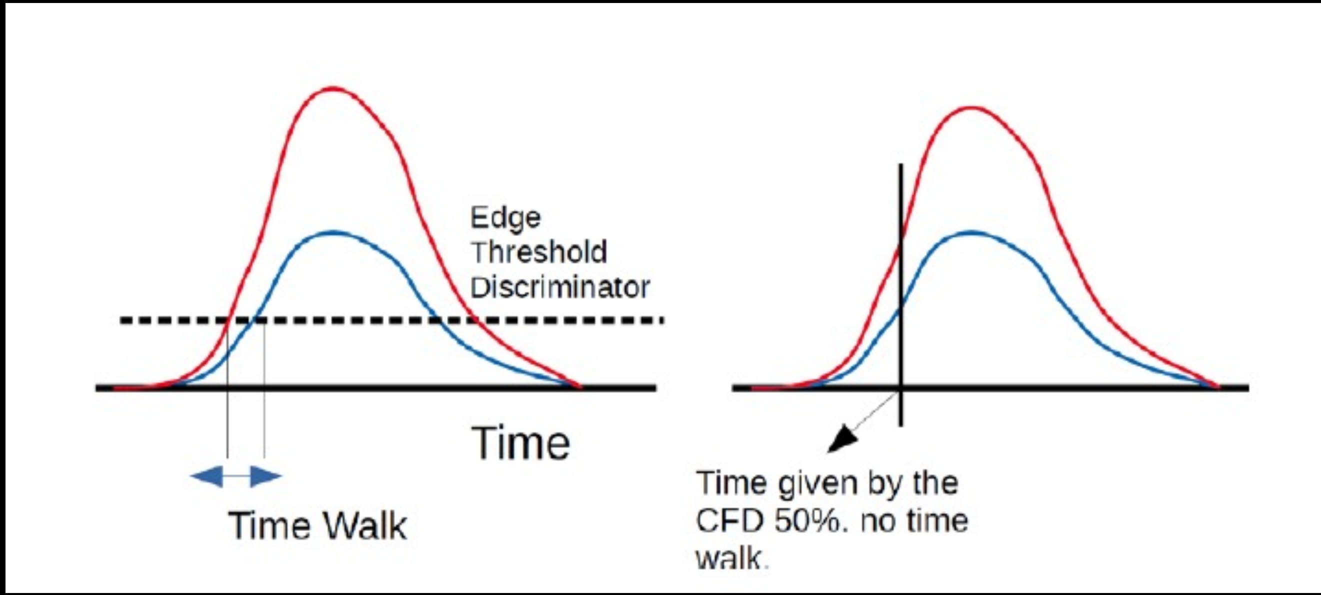
$$\sigma_t = \frac{\sigma_V}{\sqrt{N}}\left(\frac{dV}{dt}\right)^{-1} \sim \frac{\tau_R}{\sqrt{N}}\left(\frac{\sigma_V}{V_{\max}}\right)$$

- τ_R = pulse risetime
- N = samples on pulse risetime
- σ_V = voltage noise
- V_{max} = pulse height

Mitigated by using fast rise-time, low-noise electronics, and if possible, high gain

LGAD Timing Precision: Time Walk

- “Time-Walk” Contribution:
  - Arises due to coupling of charge deposition fluctuations to the finite rise time of the excitation



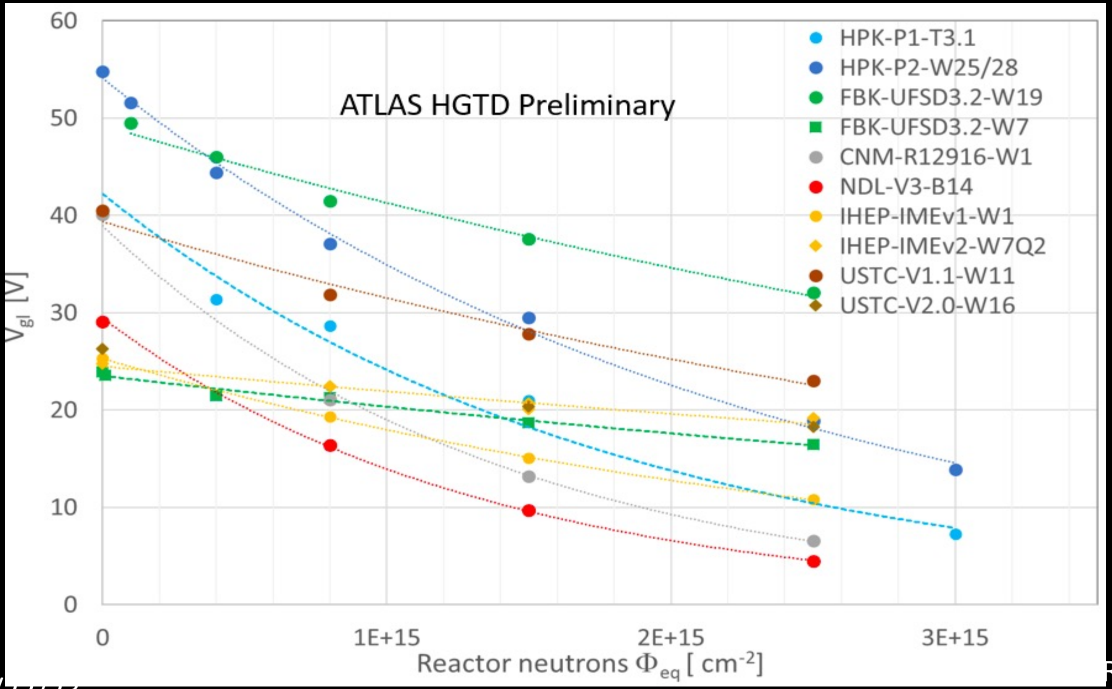
If pulse form is available, mitigate by using “constant fraction discrimination” (CFD)

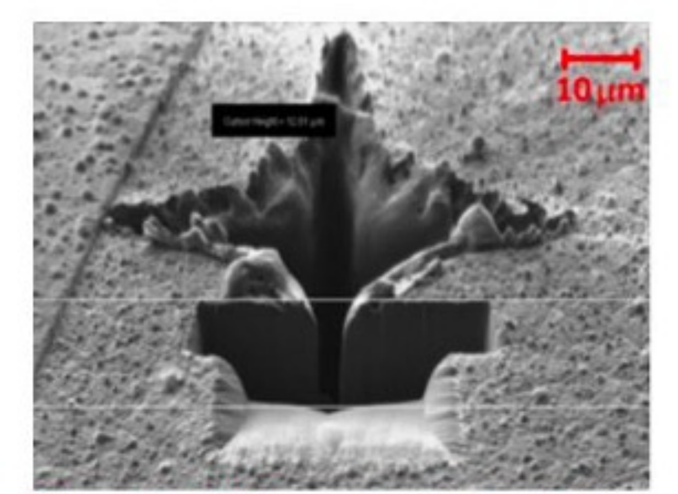
Gain Layer Radiation Hardness

- Boron doping in gain layer became less active after irradiation (**acceptor removal**)
- Key parameter of the gain degradation is the acceptor removal coefficient: *c factor*

$$V_{gl} = V_{gl0} \times \exp(-\boldsymbol{c} \times \Phi_{eq})$$

- Irradiated sensors require higher bias voltage to maintain performances.



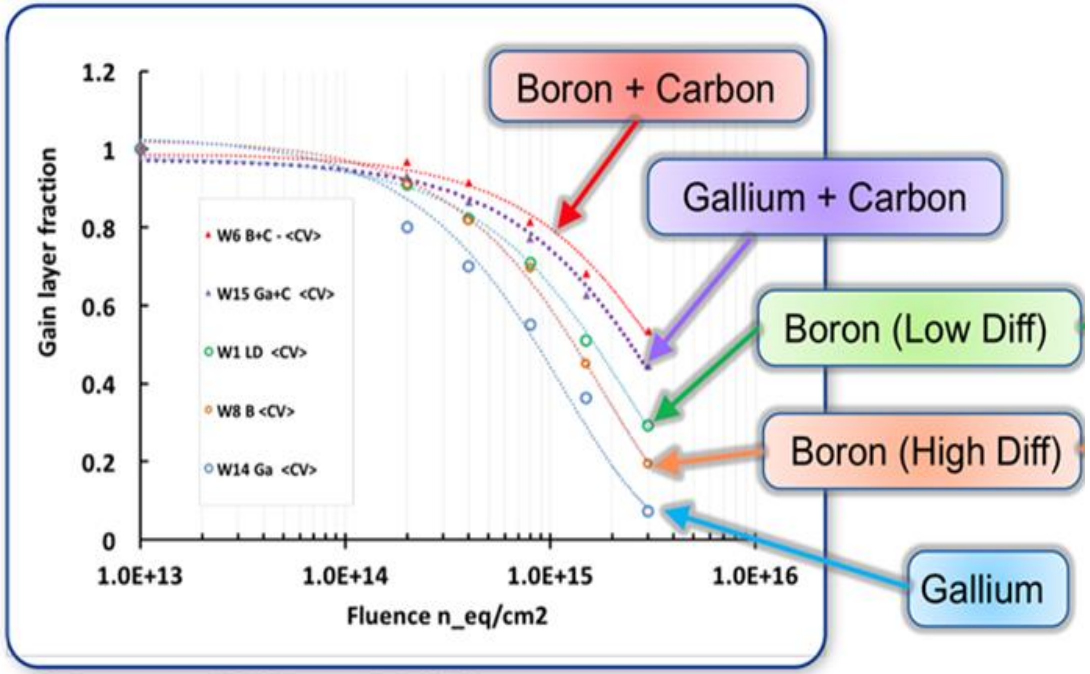


Burn mark on a CNM sensor after proton beam irradiation in Fermilab in 2018 (picture produced by CNM)

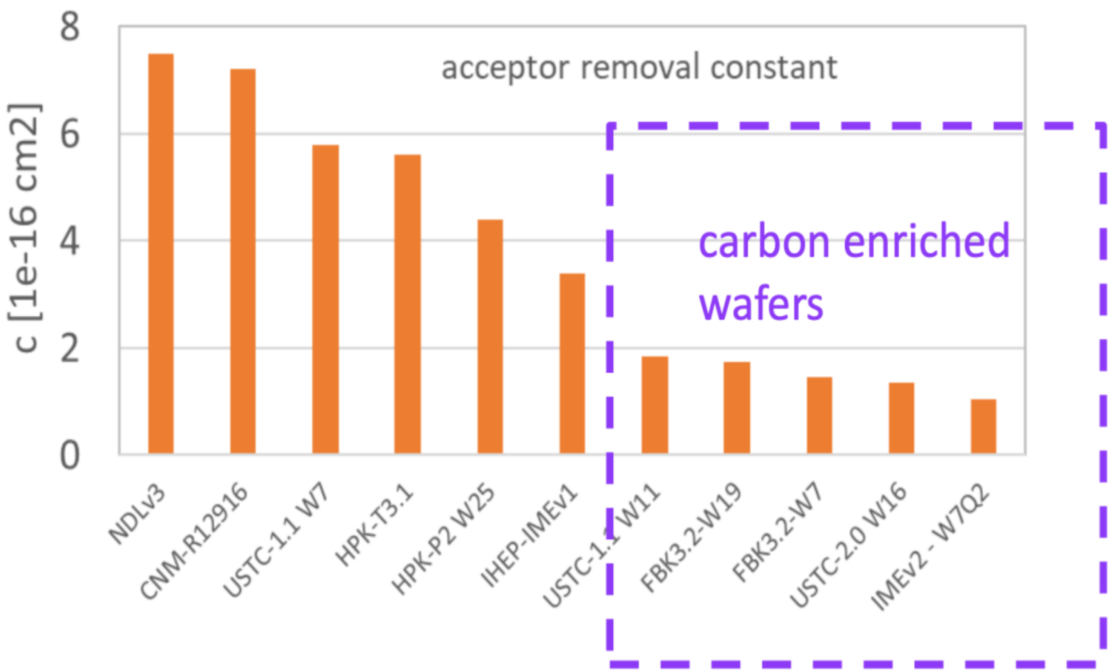
- Single Event Burnout (SEB):
  - During beam test, several sensors underwent destructive breakdown at voltages ~100 V lower than those at which the sensors were successfully operated in laboratory tests.
  - SEB occurs when the average electric field in the sensor > 12 V/µm.

Radiation Hardnes of the Gain layer

- Ways to improve the radiation hardness of LGAD:
  - Geometry design, such as changing the doping concentration, depth, width, shape
  - Different doping materials: adding the Carbon, Gallium to gain layer

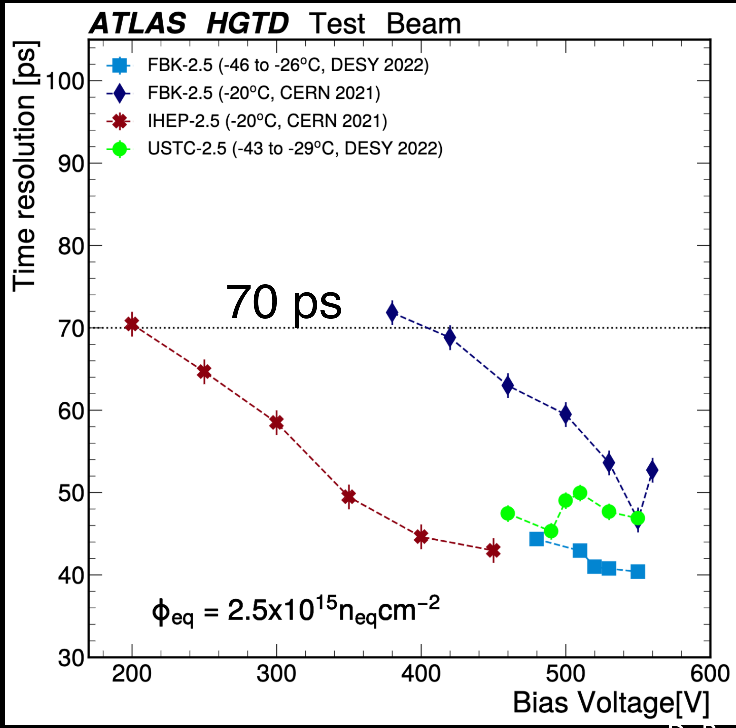


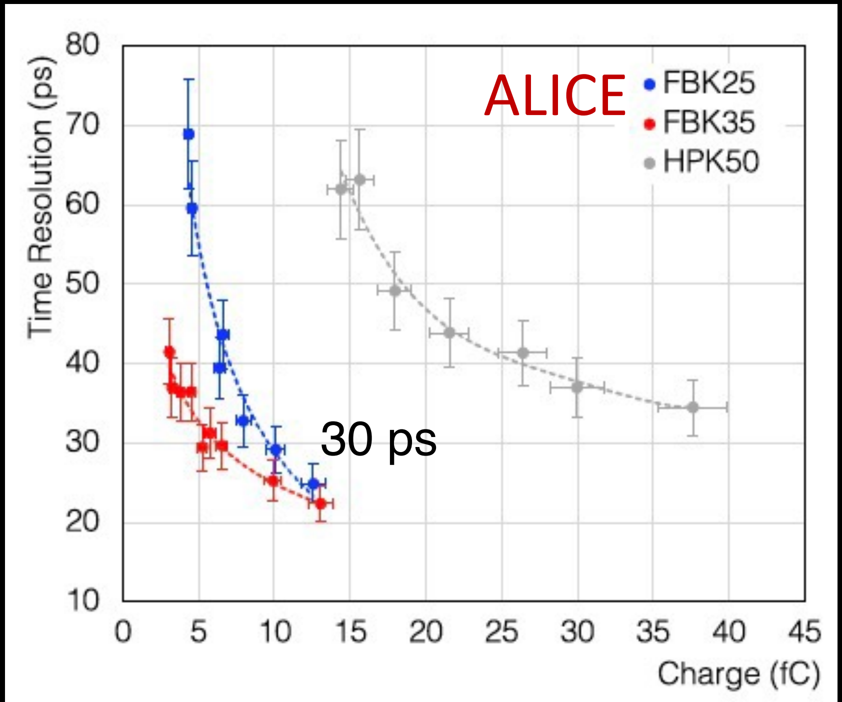
[G.Paternoster, FBK, Trento, Feb.2019]



State of the art Sensors with gain

- State of the art sensors for HGTD (ATLAS) and CMS endcap MIP Timing Detector (MTD) - Pixel size 1.3 mm x 1.3 mm
- Time resolution: measured with a time reference device < 50 ps even after $2X10^{15}$ n_{eq}/cm^2
- R&D for ALICE TOF
  – 25 and 35 μm thick prototypes show time resolution < 25 ps
  – Sensors of 10 μm in preparation

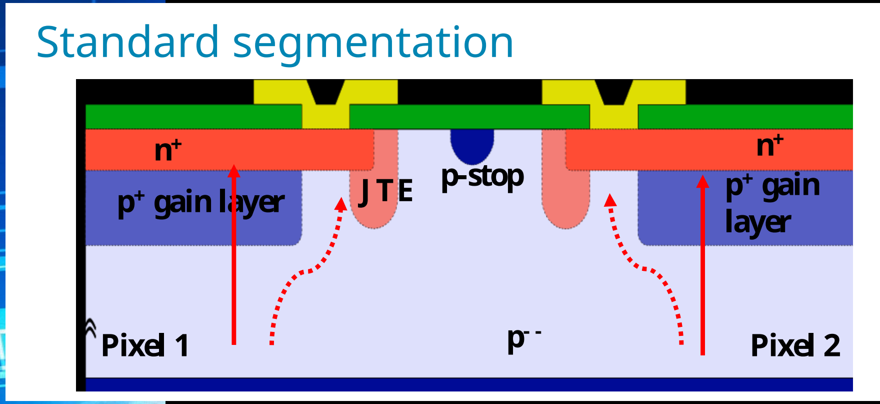


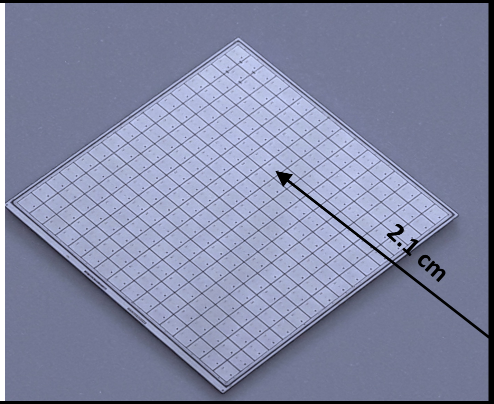


UNIVERSITY OF OXFORD

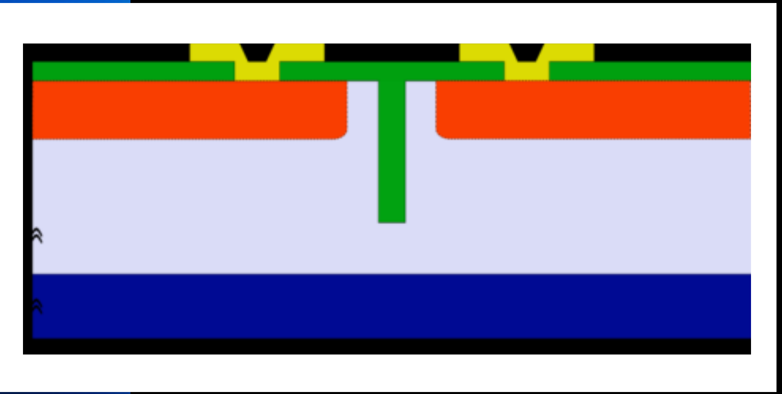
Sensors with gain

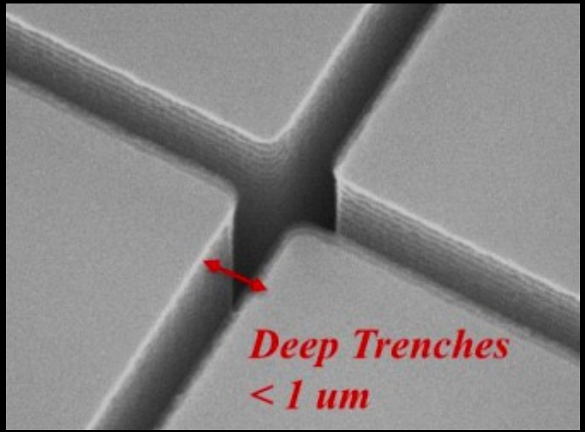
JTE + p-stop design (no gain area)



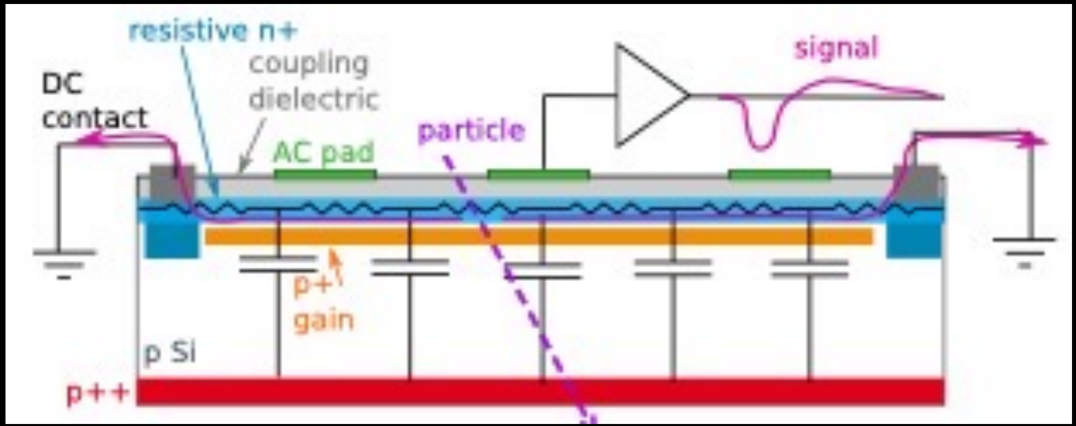


Trench-isolated design (trench filled with Oxide)

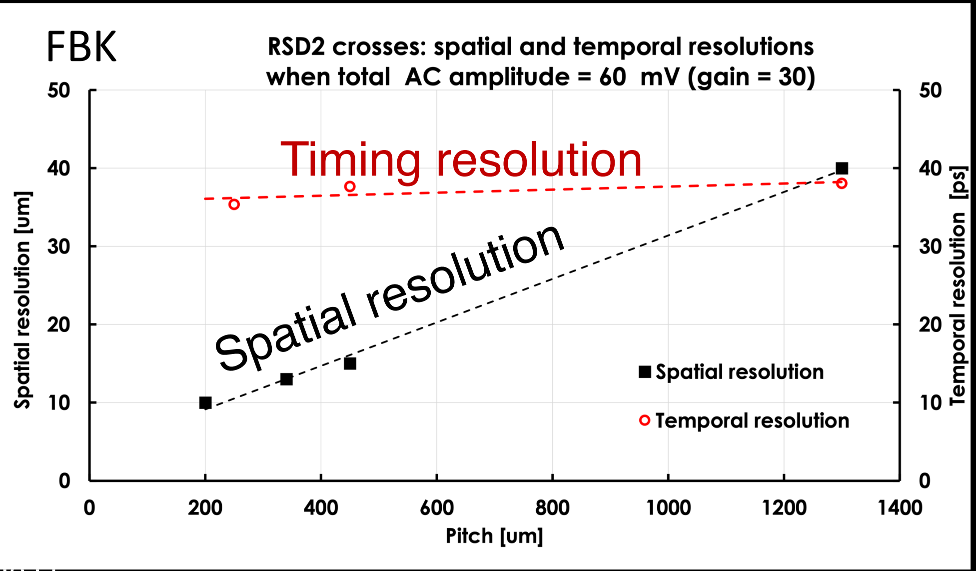




Resistive AC LGAD



- Continuous resistive n+ implant
- Readout: AC-coupling through dielectric layer
- Segmentation obtained by position of the AC pads



Cartiglia

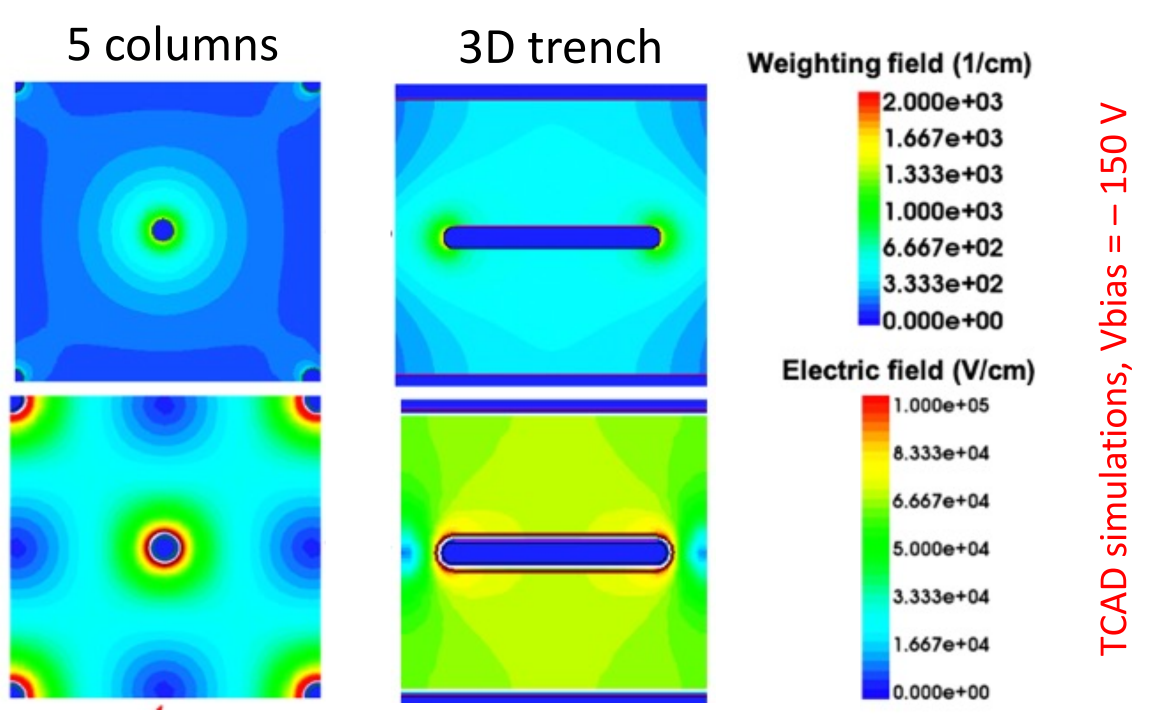
Timing with 3D Detectors

Optimized 3D sensor design

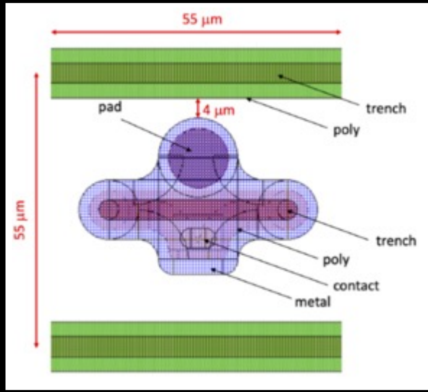
- Detector Signal

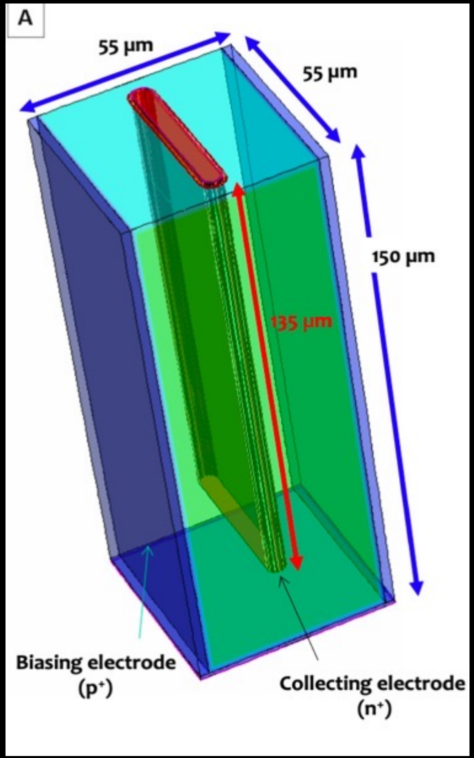
$$i = q\,\vec{E}_w \cdot \vec{v}_d$$

- Fast 3D detectors need uniform E_W and velocity in saturation regime



- Trenched 3D Time Spot Detector





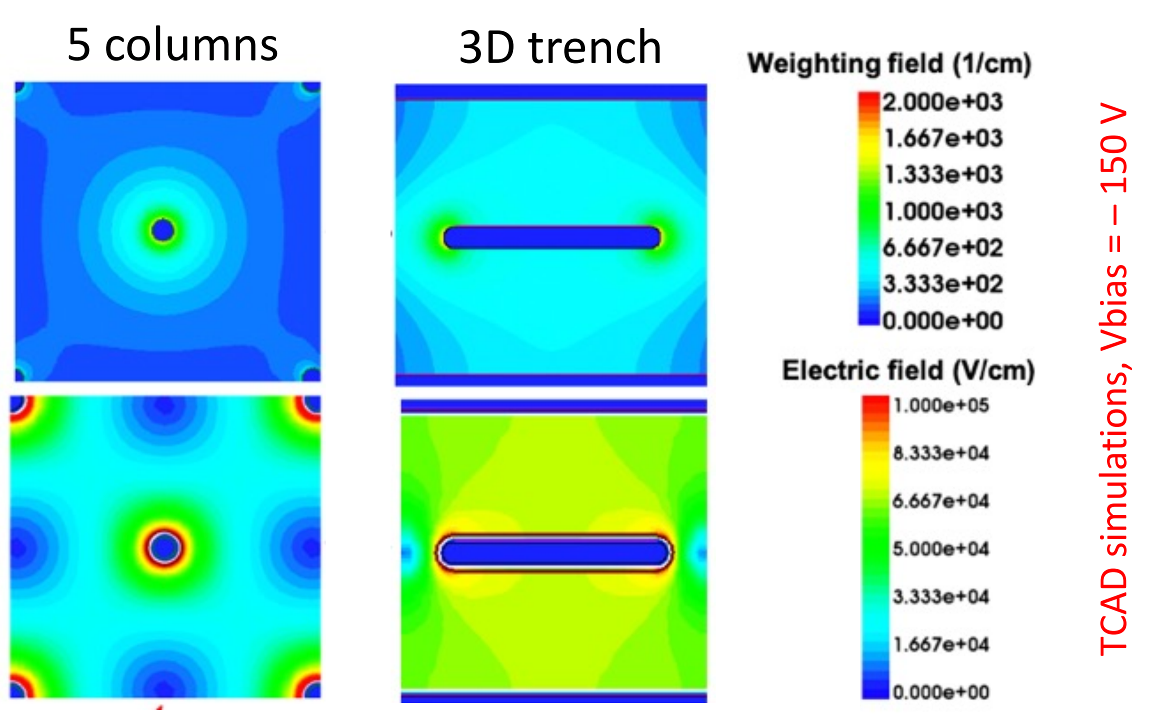
- 55 µm x 55 µm pixels
- In each pixel a 40 µm long n++ trench is placed between continuous p++ trenches used for the bias
- 150 µm-thick active thickness, on a 350 µm-thick support wafer
- The collection electrode is 135 µm deep

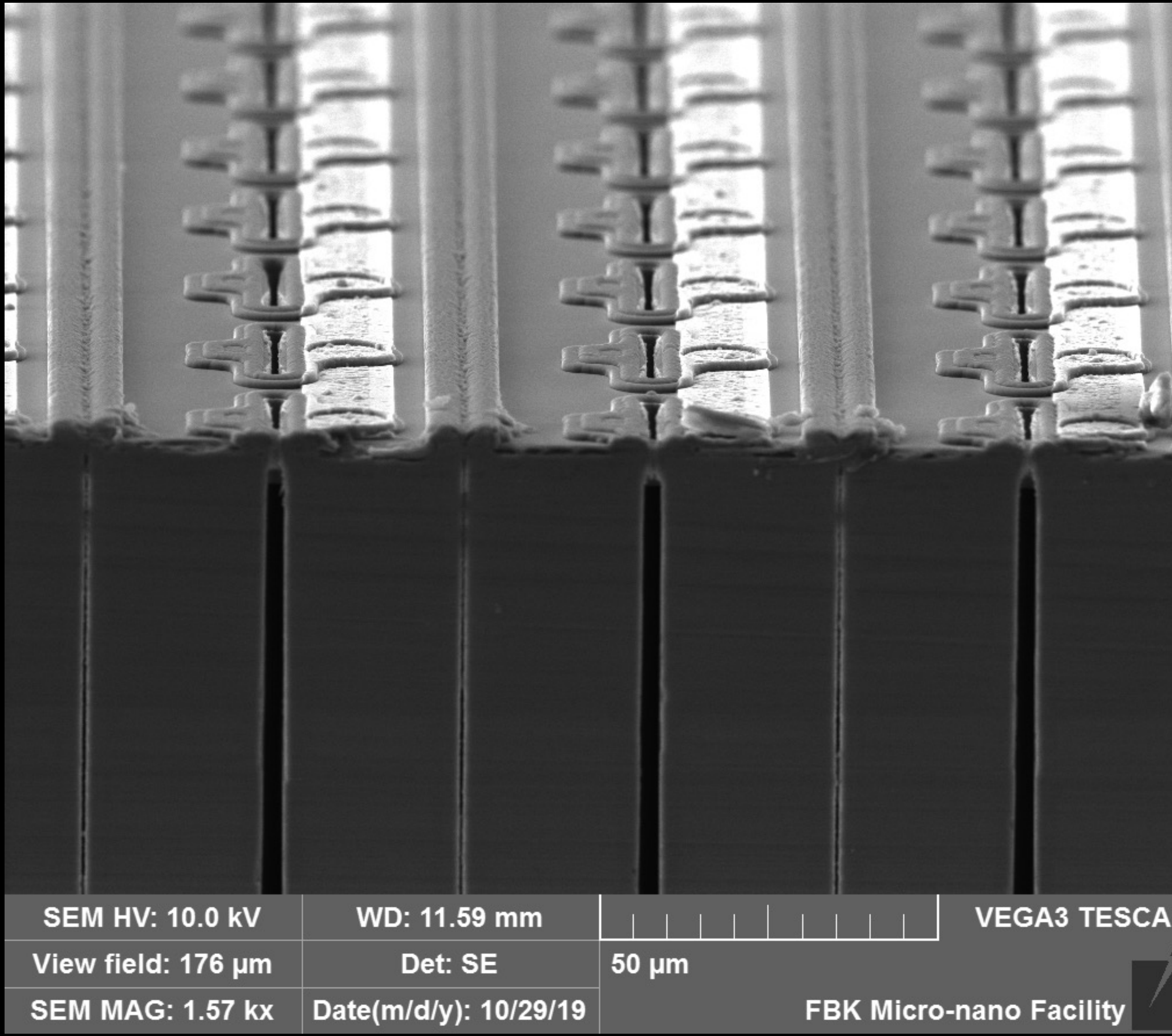
Optimized 3D sensor design

- Detector Signal

$$i = q\,\vec{E}_w \cdot \vec{v}_d$$

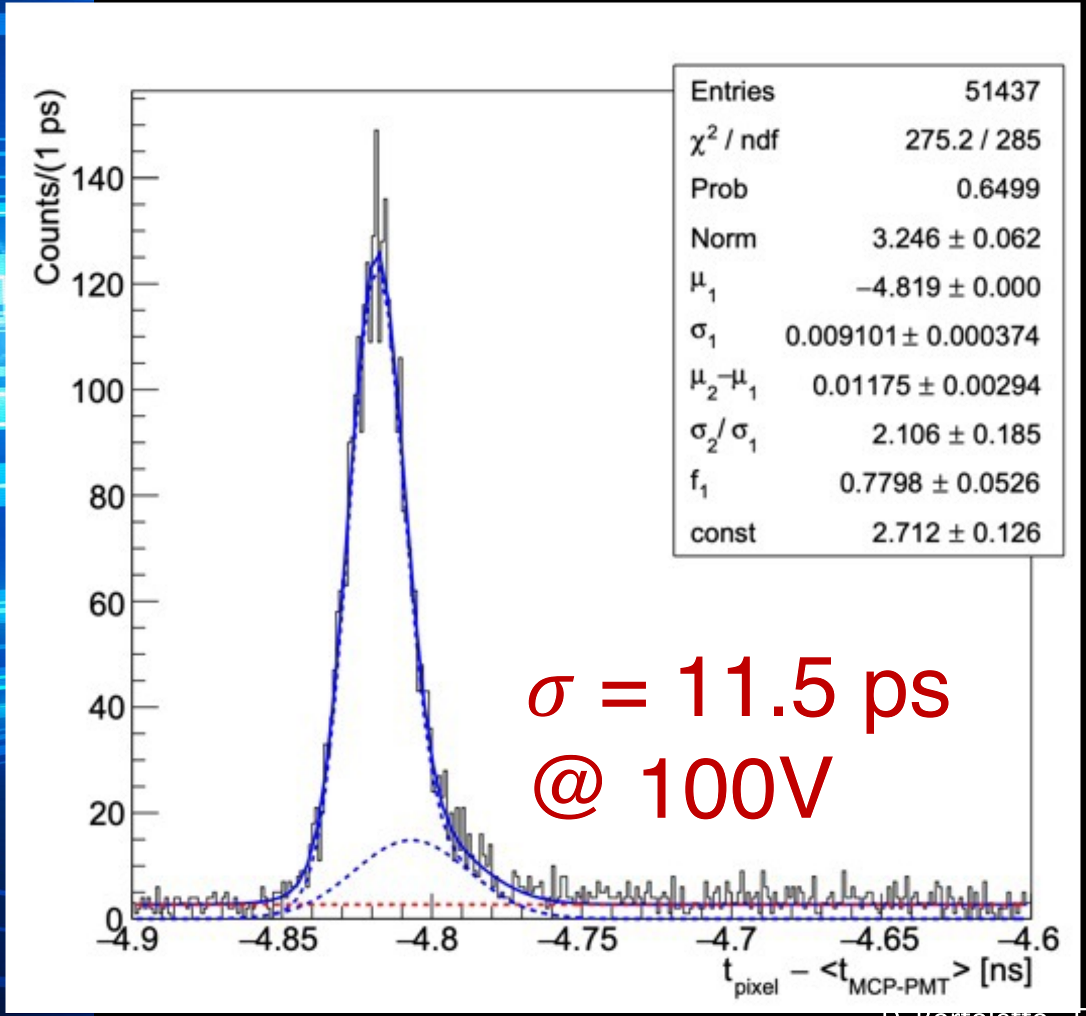
- Fast 3D detectors need uniform E_W and velocity in saturation regime

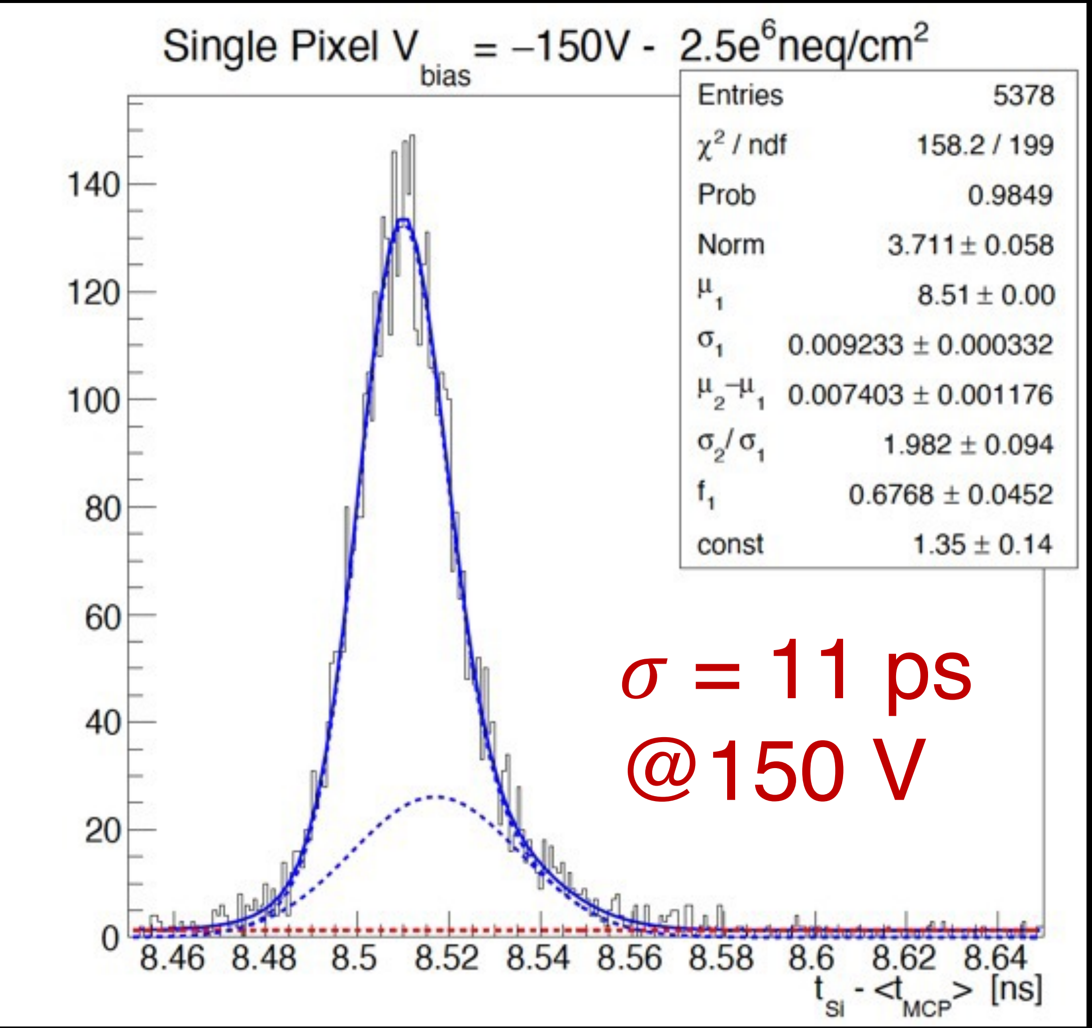




Single 3D timing performance

- Non irradiated
- After 2.5 x 10^{16} n_{eq}/cm^2





MONOLITHIC

FCC

- FCC 91.7 Km tunnel
- Stage 1: FCC-ee (Z, W, H,) as Higgs factory, electroweak & top factory at highest luminosities
- Stage 2: FCC-hh (~100 TeV) as natural continuation at energy frontier, pp & AA collisions; e-h option

FCC-ee Vertex Detector Requirements

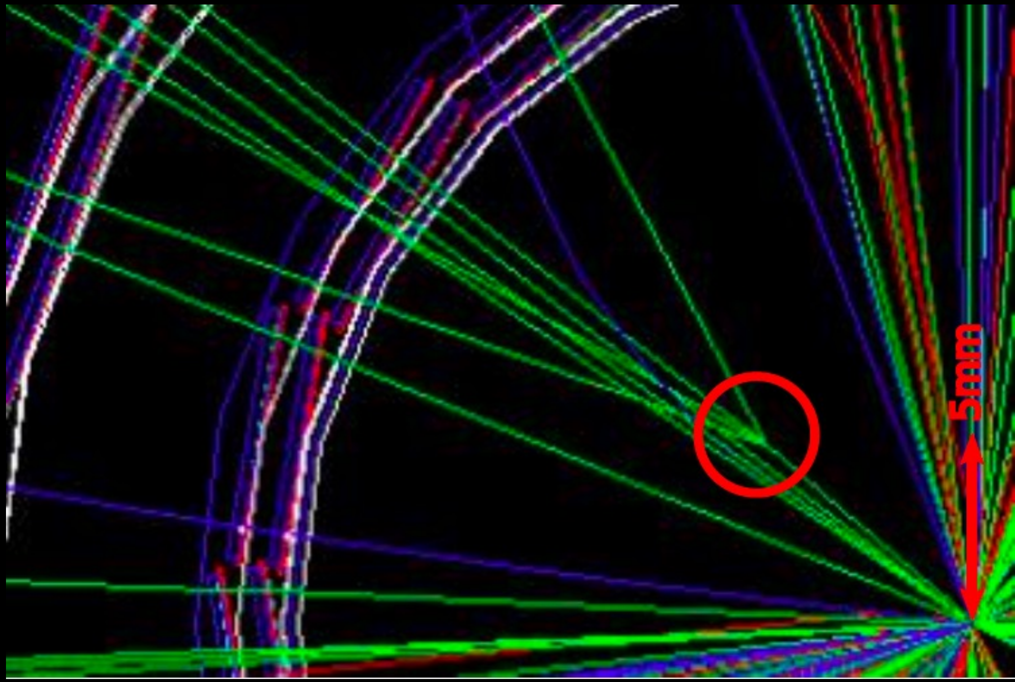
- Efficient tagging of heavy quarks through precise determination of displaced vertices required for many physics goals

$$\sigma(d_0) = \sqrt{a^2 + b^2 \cdot \mathrm{GeV}^2/(p^2 \sin^3\theta)}$$

$$a\sim 5\ \mu m,\ \ b\sim 15\ \mu m$$

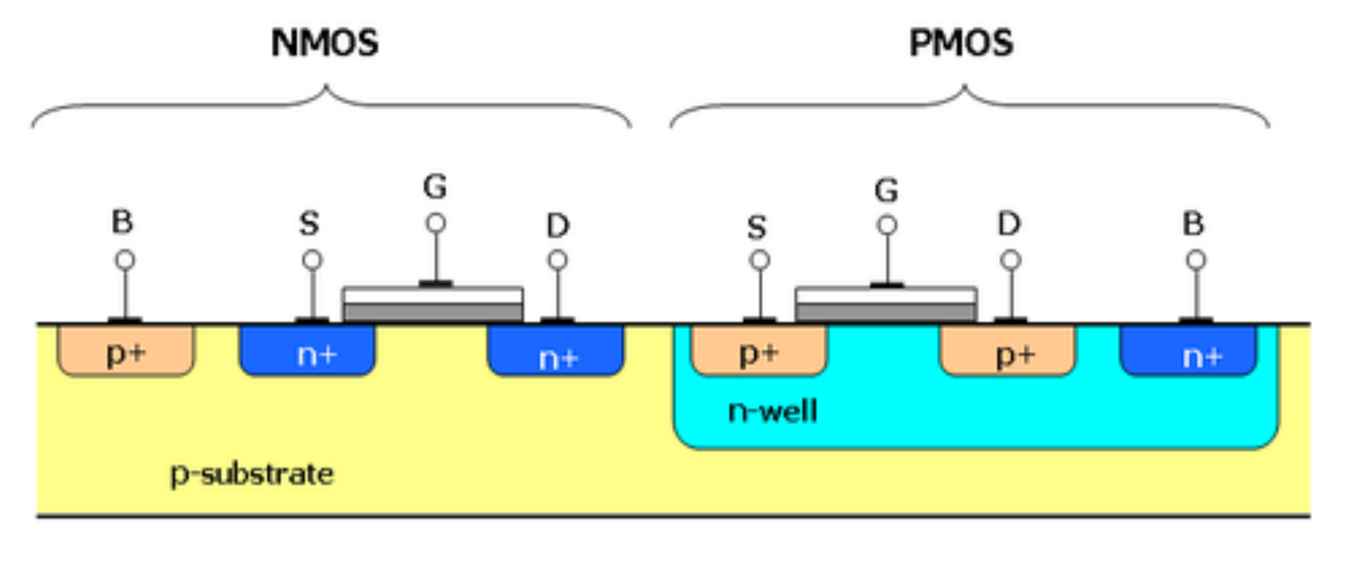
- Good single point resolution: σ_{SP}~3 μm
  - Small pixels <~25x25 μm^2, analog readout
- Low material budget: $X \lesssim 0.2\%\ X_0$ / layer
  - Corresponds to ~200 μm Si, including supports, cables, cooling
  - Low-power ASICs (~50 mW/cm^2)

Excellent impact parameter resolution for c/b-tagging



Monolithic Silicon Pixel Detectors

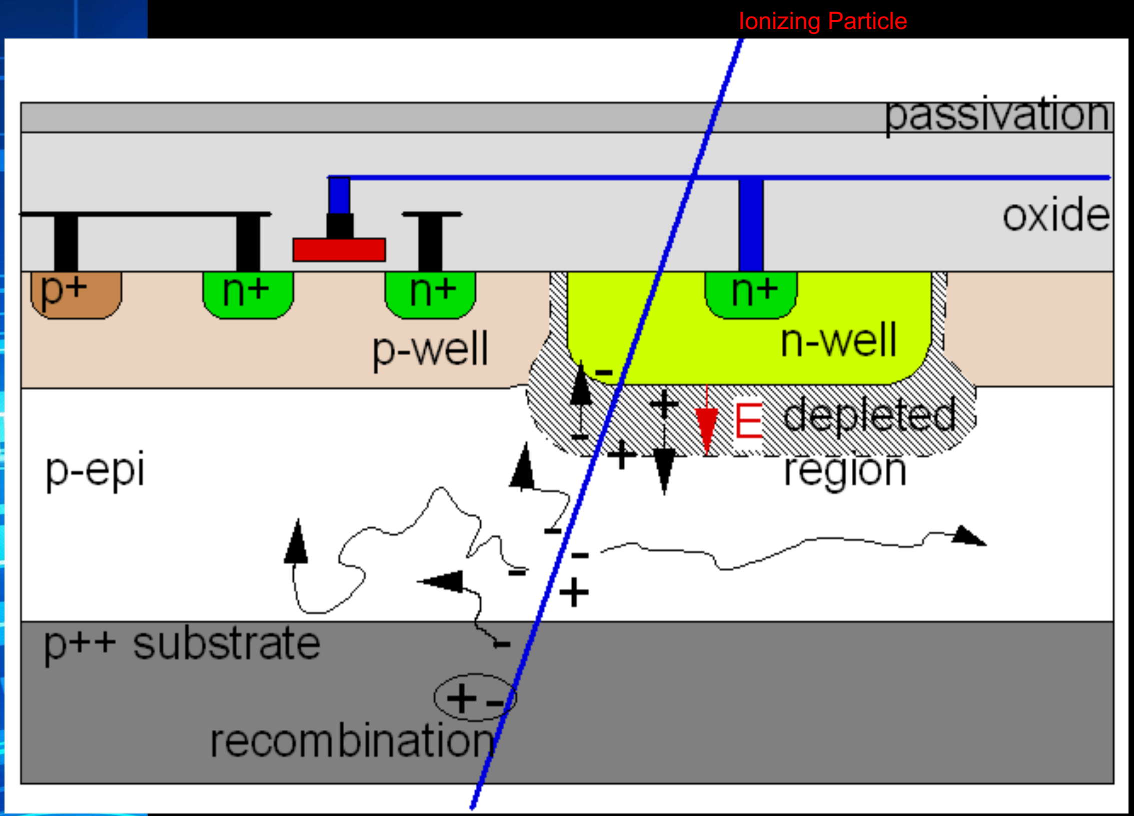
Integrate the *sensing element* and *readout chip* in a single layer of silicon



- CMOS (Low Voltage)
  - Image sensors
  - Microprocessors and Microcontrollers
  - Memories
  - Transceivers for communication
- HV-CMOS = CMOS + High Voltage substrate biasing & additional wells to isolate the electronics from the substrate
  - Display and motor drivers

- Allows very thin sensors to achieve ultimate low mass trackers (0.3% X_0 in Heavy-Ion experiments or <1% for pp).
- High volume and large wafers (200 mm) reduces detector cost opens possibility for large area pixel detectors.
- Saves cost and complexity of bump bonding(one of the cost drivers in hybrid silicon detector systems).

Monolithic Active Pixels

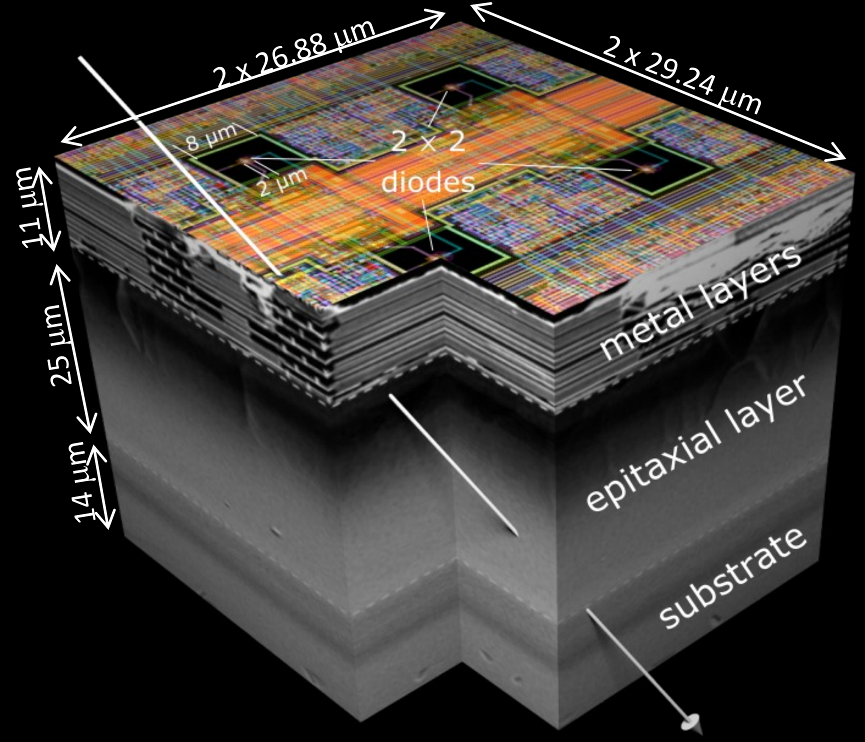


- Commercial CMOS technologies (e.g. AMS 0.35 μm)
- Lightly doped p-type epitaxial layer (~14-20 μm)
  - MIPs produce ~80 e-/h+ pairs per μm (~1000 e-)
- No reverse substrate bias:
  - Signal charge collection mainly by diffusion (~100 ns)
  - Sensitive to displacement damage
- N-well implantation used as collecting electrode
- Only n-MOS transistor in pixel (in p-well)
  - Very simple in-pixel circuit (few transistors)
  - Complex electronics at the periphery of the matrix
- Pixel size: 20 x 20 μm^2 or lower ➠ few μm resolution

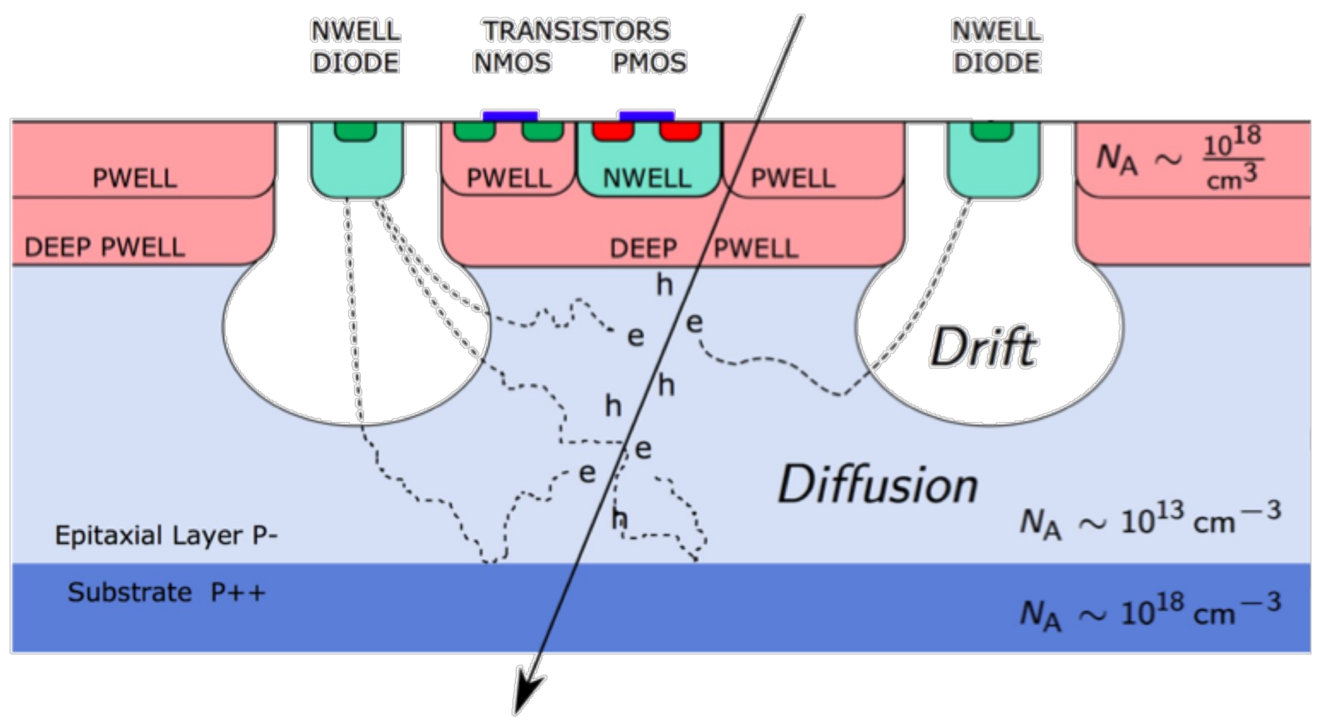
Applications: STAR-detector (RHIC Brookhaven), Eudet beam-telescope

IPHC Strasbourg (PICSEL group))

ALICE ITS



ALPIDE (ALICE) TJ 180 nm

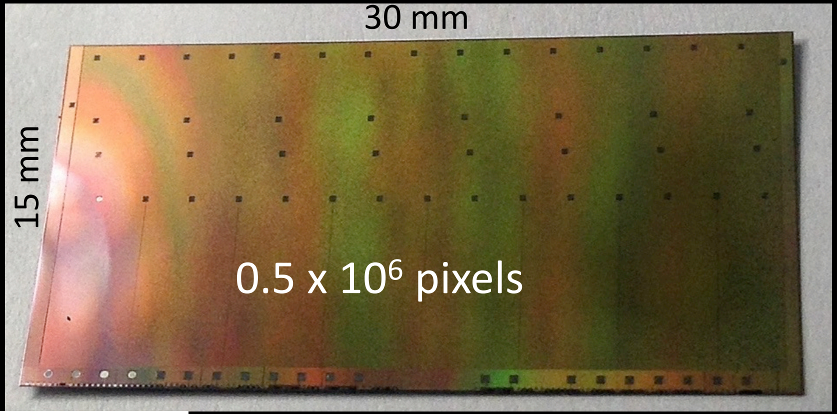


- Pixel pitch: 29 μm x 27 μm
- Small n-well diode (2 µm diameter), ~100 times smaller than pixel => C=5fF => large S/N
- Power < 40 mW/cm^2
- Integration time <10 μs

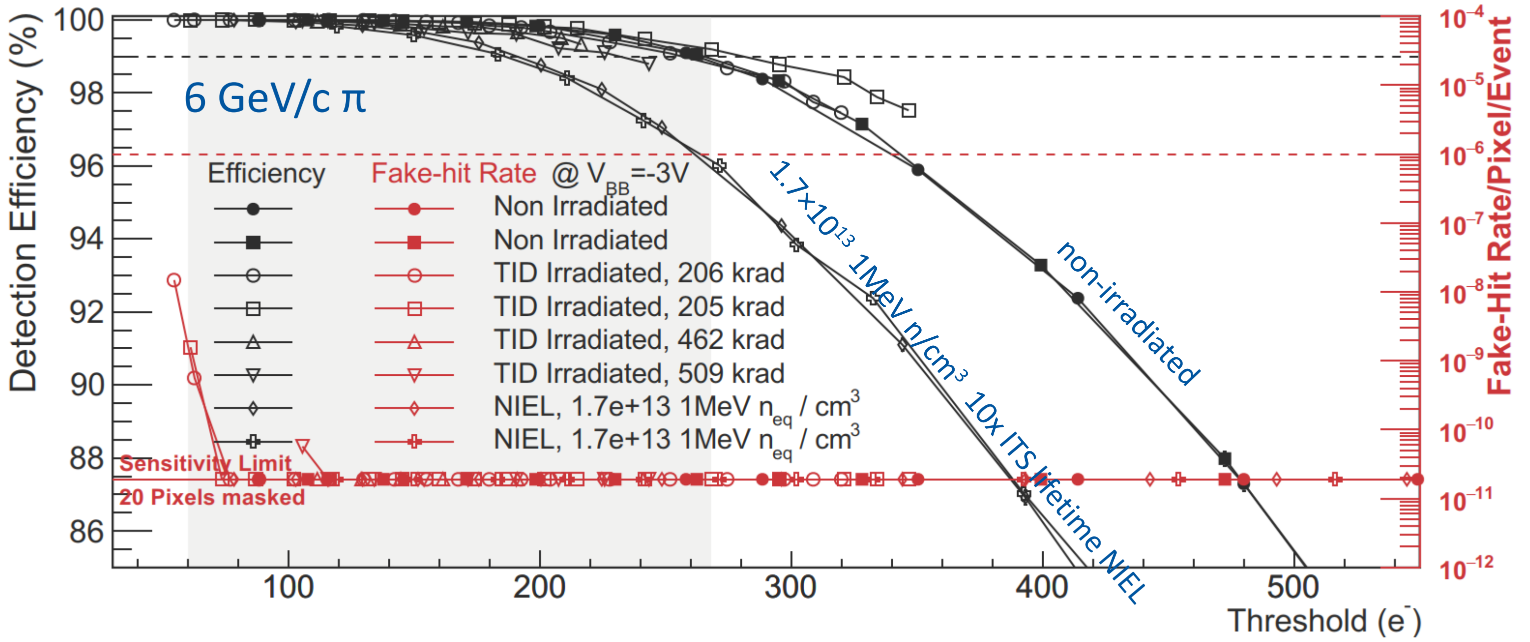
- Tremendous progress in CMOS pixel designs
  - Deep PWELL allows full CMOS within active area
  - high-resistivity (> 1kΩ cm) p-type epitaxial layer (≈25 µm thick) on p-type substrate
  - Partial depletion by applying 6 V

ALPIDE efficiency

- Pixel size: 29 x 27 μm^2 with low power front-end **~40 nW/pixel**
- Extensive tests before and after irradiation



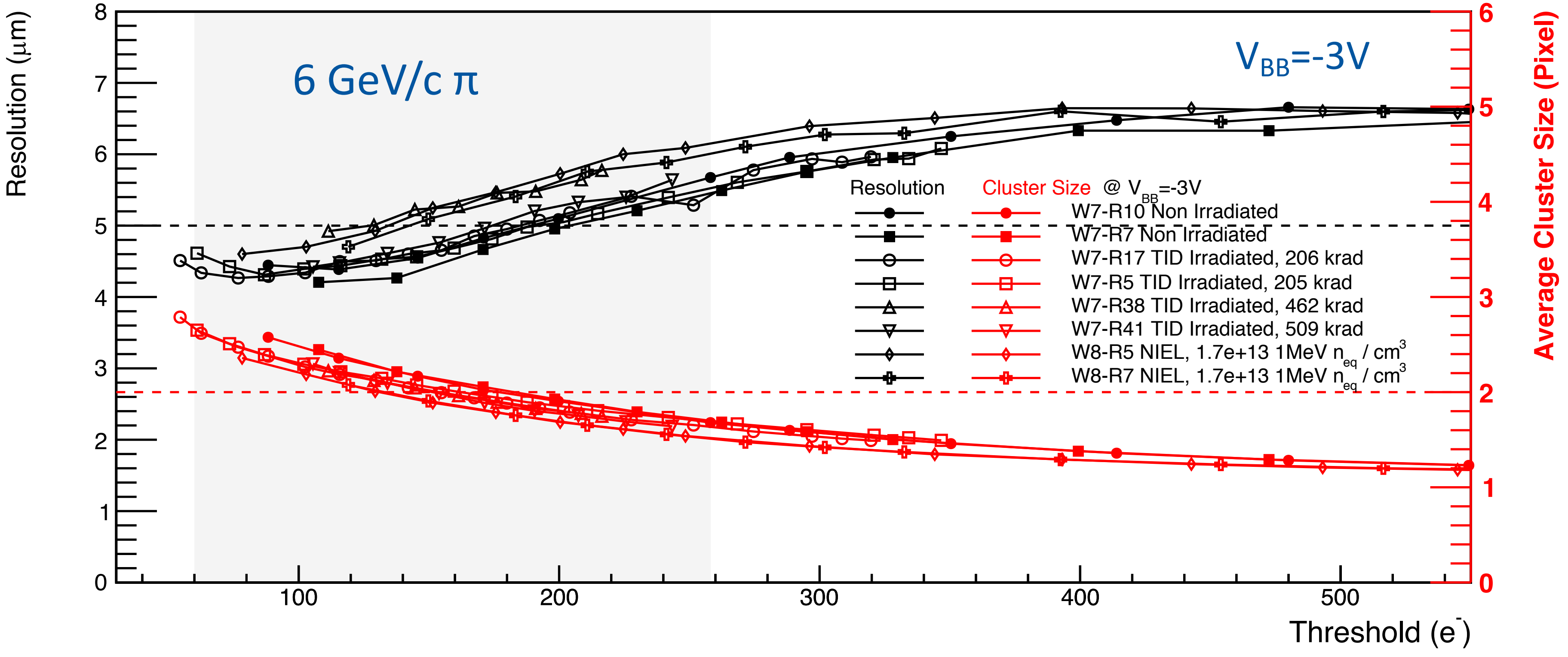
Test Beam Measurements



- **Efficiency > 99.5% and fake hit rate << 10^{-6} over wide threshold range**
- **Excellent performance also after irradiation to 1.7 x10^{13} 1MeV n_{eq}/cm^2**

ALPIDE resolution

Test Beam Measurements

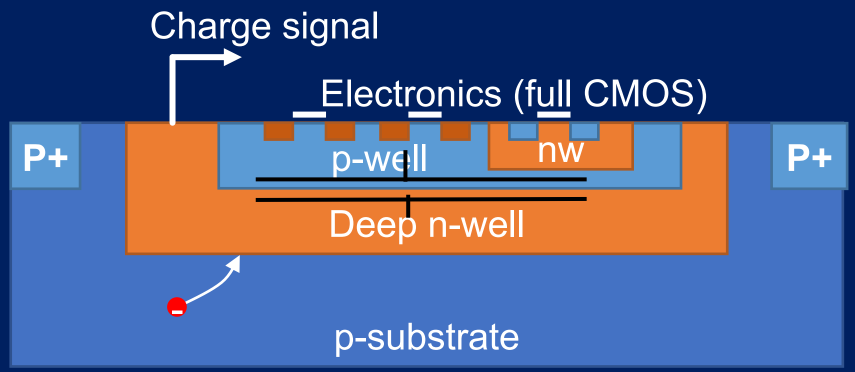


Resolution of 5 μm at a threshold of 200 electrons

Typ. cluster size 2 at a threshold of 200 electrons (normal incidence)

Design choices toward DMAPS

Electronics inside charge collection well

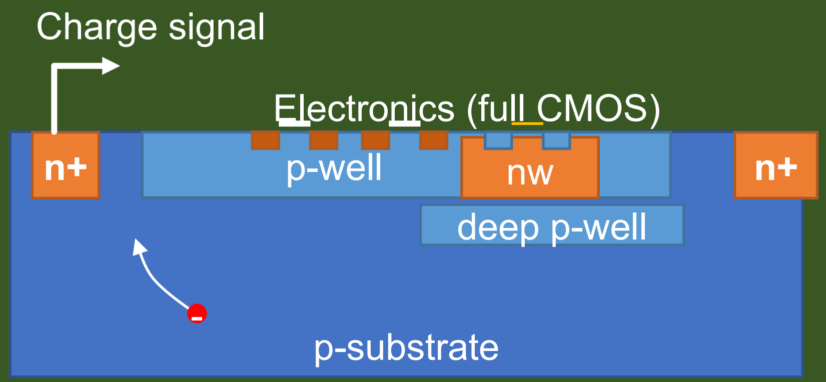


- Deep n and p wells
- Large collection node
- Shorter drift path
- Larger capacitance (DNW/PW junction!) ➠ X-talk, noise & speed (power) penalties

$$ENC^2_{thermal} \propto \frac{4}{3}\frac{kT}{g_m}\frac{C_d^2}{\tau}$$

$$\tau_{CSA} \propto \frac{1}{g_m}\frac{C_d}{C_f}$$

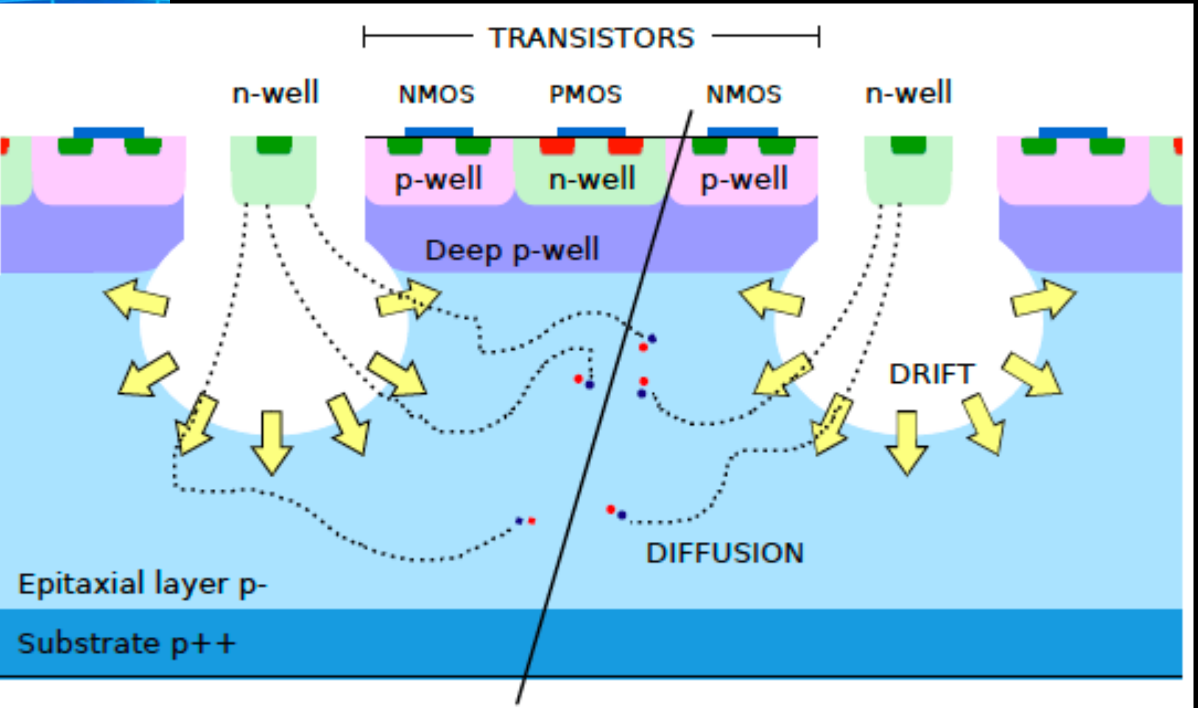
Electronics outside collection well



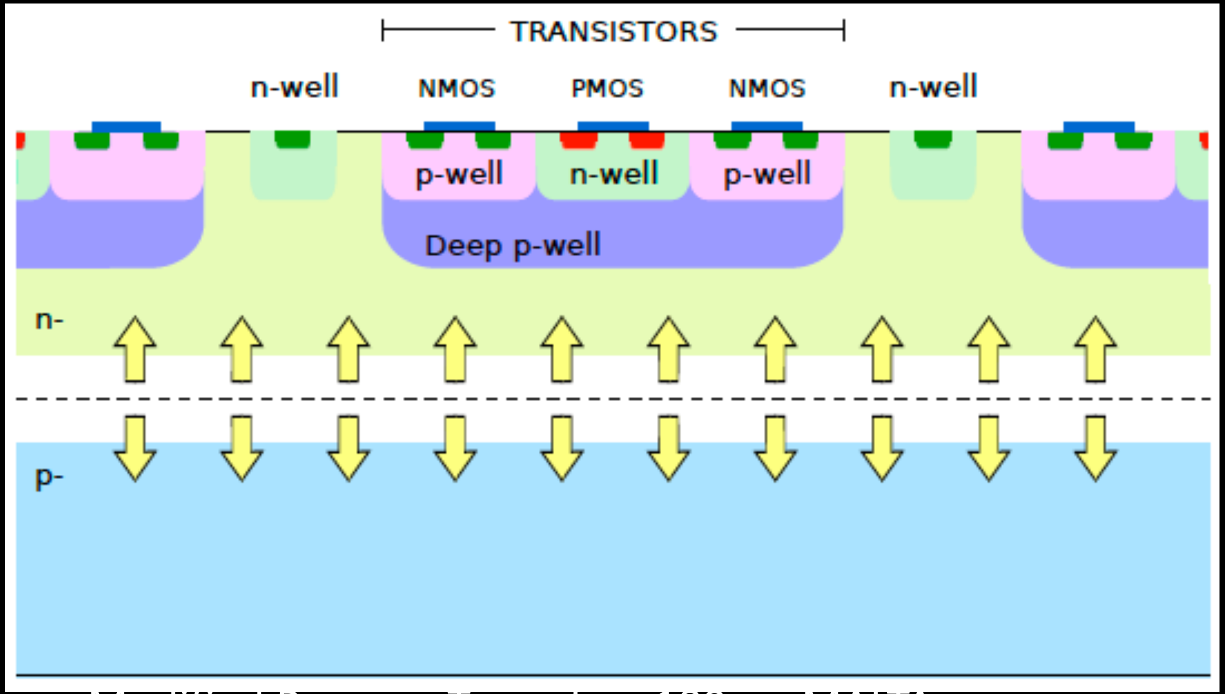
- Full CMOS with additional deep-p implant
- Small collection node
- Smaller capacitance ➠ less power
- Long drift path

TowerJazz 180nm MALTA sensor

- Can you make the ALIPIDE process more radiation hard ?
- To ensure full lateral depletion, uniform n-implant in the epi layer (modified process)

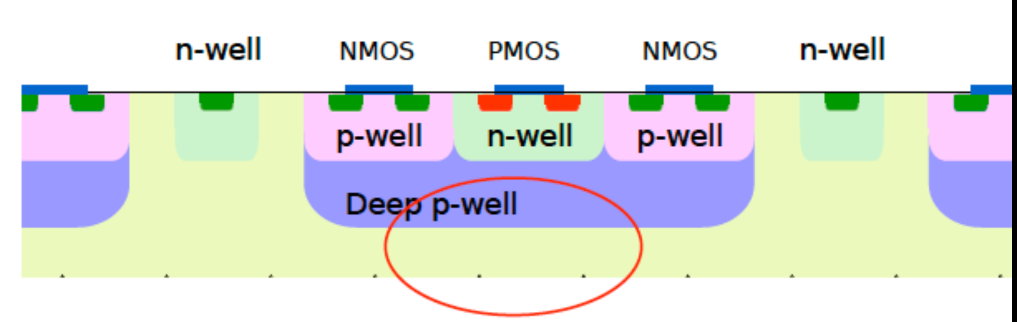


Standard Process

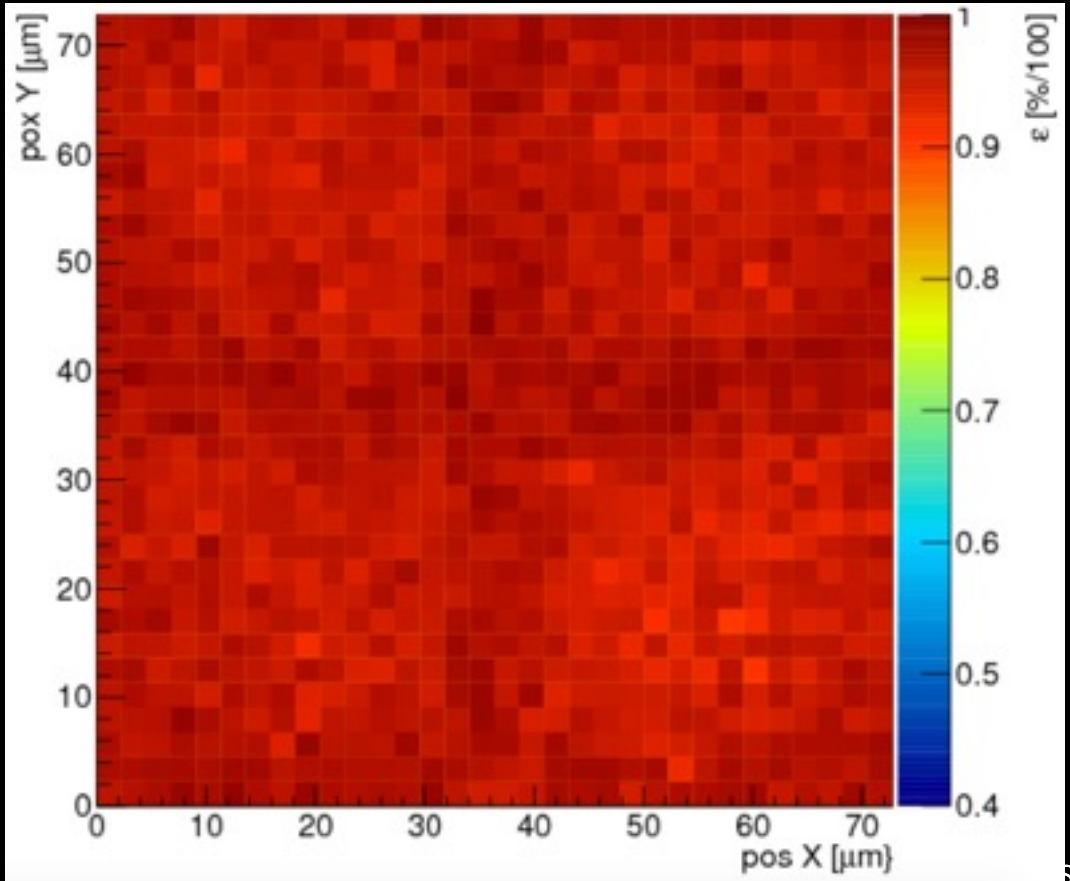


Modified Process: TowerJazz 180nm MALTA sensor
W. Snoeys et al. DOI 10.1016/j.nima.2017.07.046

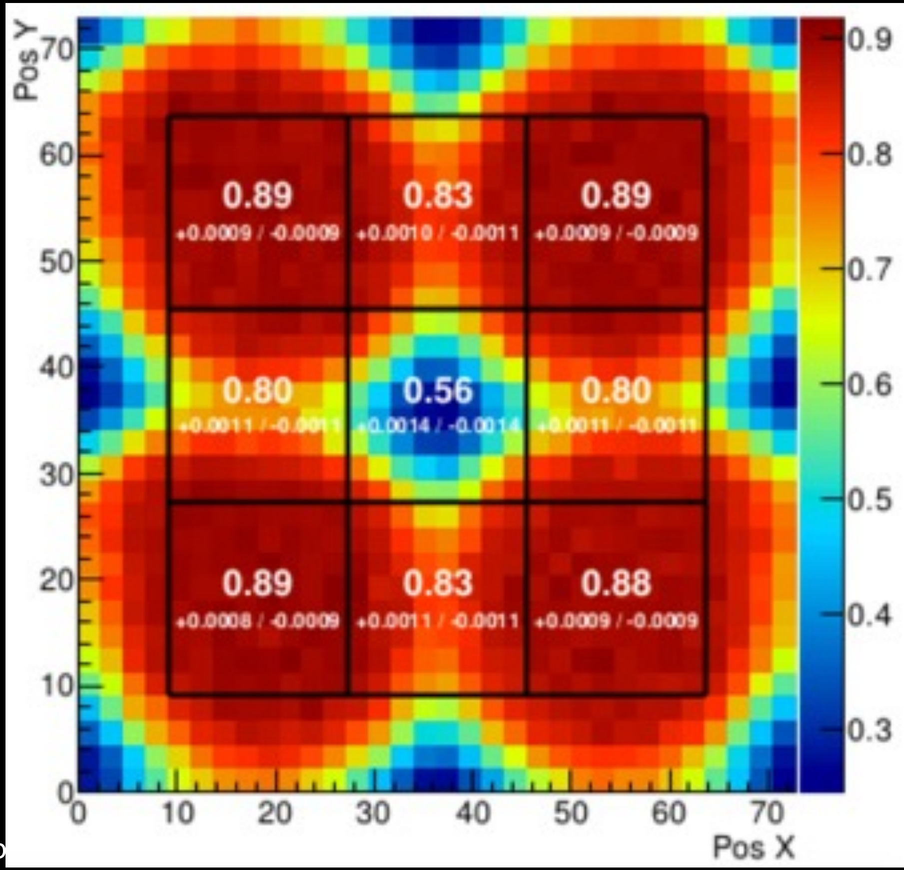
Radiation Hardness



- Unirradiated @ 250e$^-$ threshold 2x2 pixel at 36 μm pitch

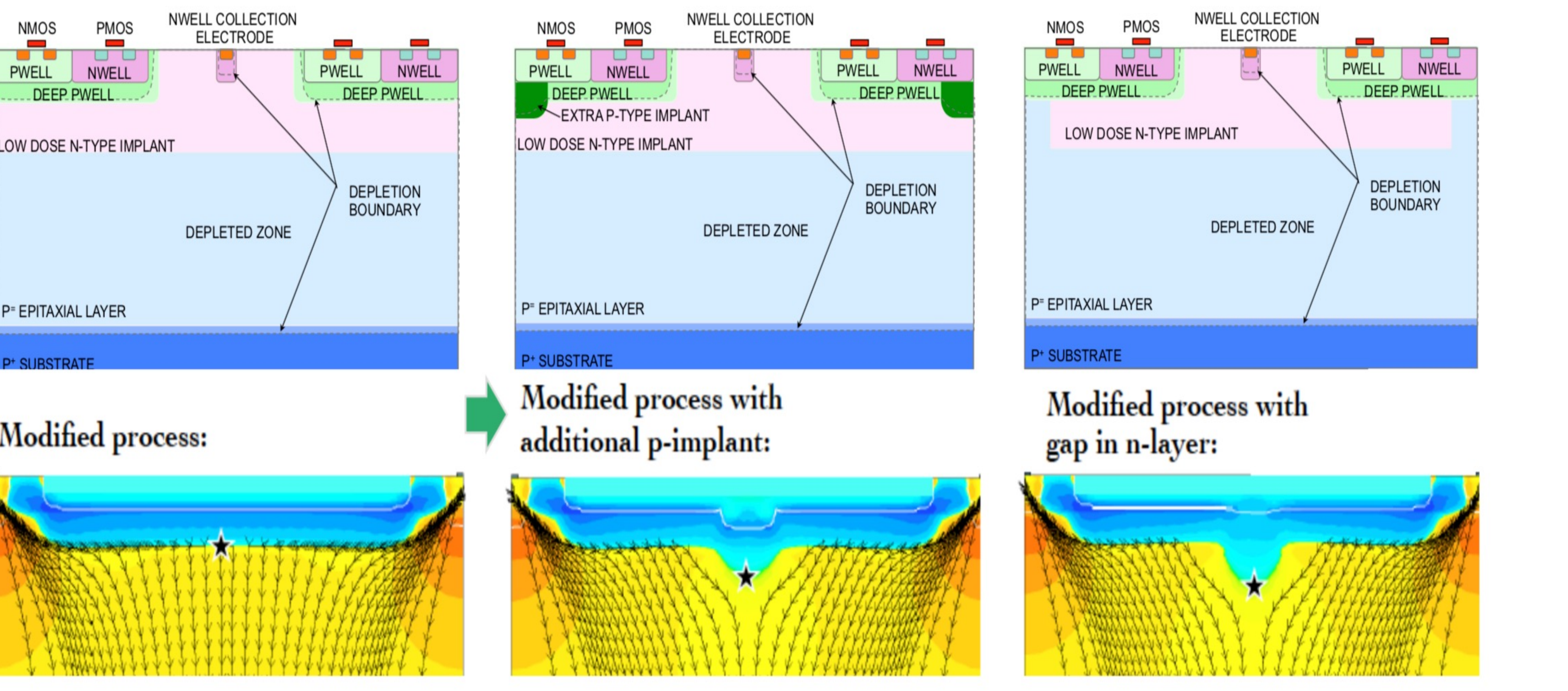


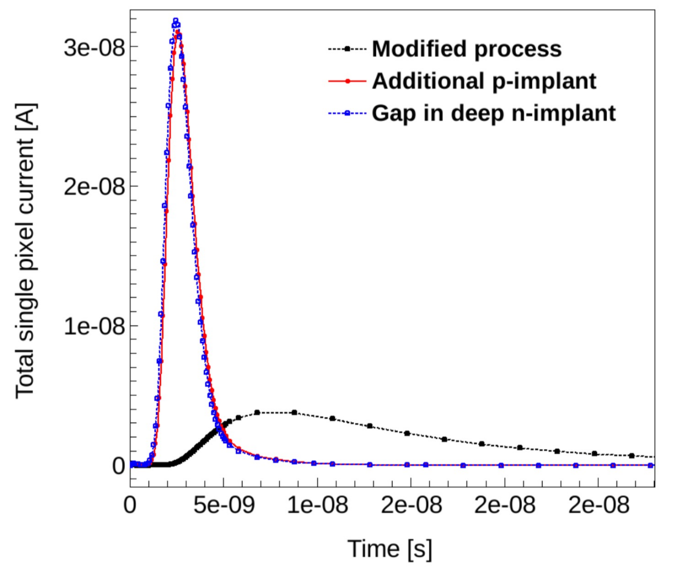
Irradiated 10^{15}n/cm^2 @ 350e$^-$ threshold 2x2 pixel at 36 μm pitch



MINIMALTA

- Special layouts for deep p and n wells to optimize field configuration and charge collection
- Increase lateral field near pixel edge to "focus" charge to collection electrode



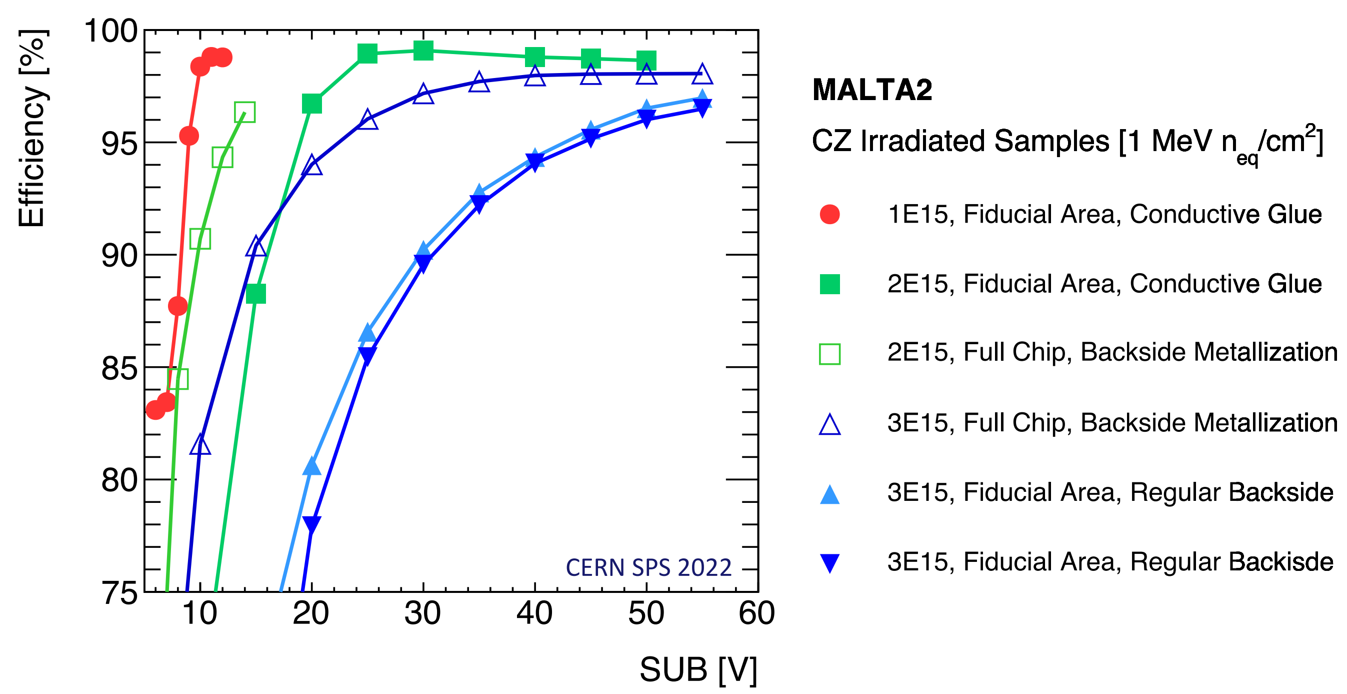


Electrostatic potential, streamlines and electric field minimum (*):

CMOS DMAPS Small Electrode

Modified TJ process to improve radiation hardness

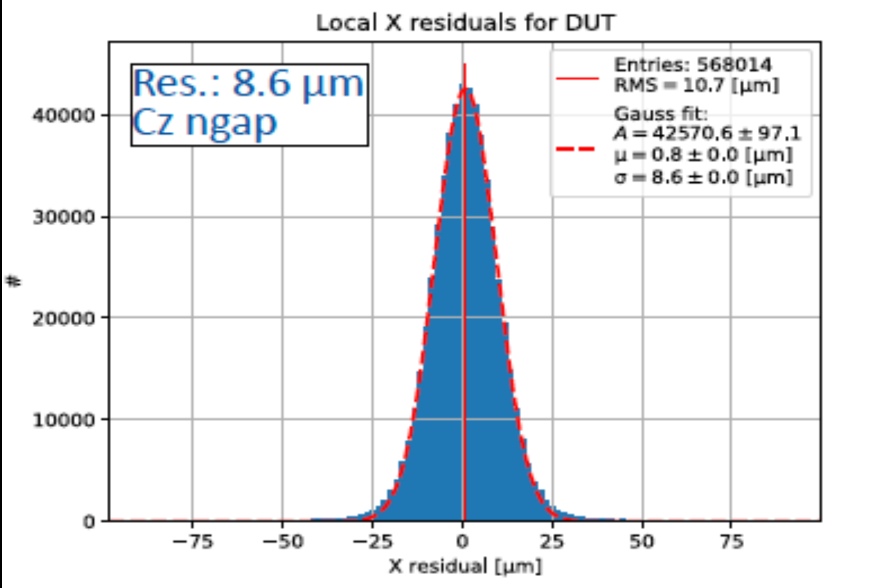
- MALTA 2 (epitaxial and CZ)



Average efficiency of irradiated MALTA2 on Czochralski substrate versus SUB voltage

Efficiency @3E15 n_{eq}/cm^2 > 95% in 25ns

- TJ-MONOPIX2- large chip (2× 2 cm^2) column drain readout
- Pixel size 33x33 μm^2
- 25 µm p-type epitaxial layer (1 kΩ cm) grown on a low-resistivity substrate, C=3-4 fF



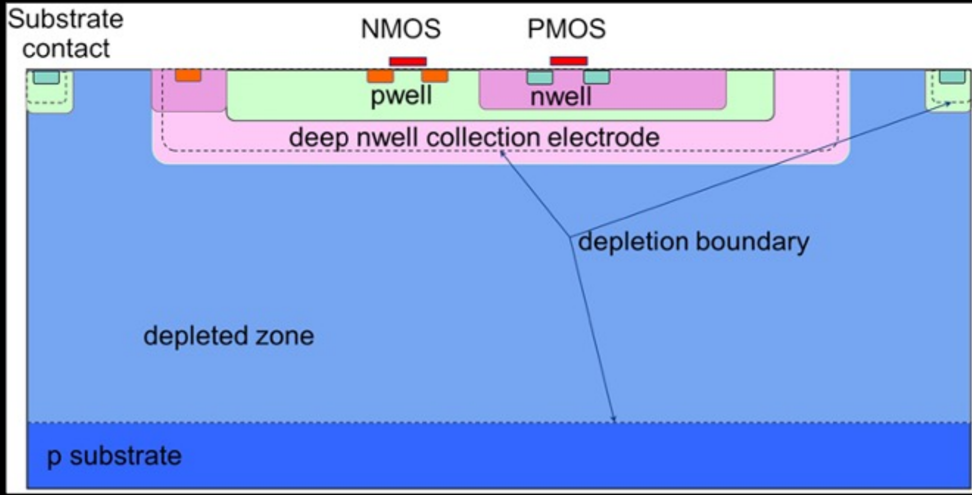
- OBELIX (Optimized BELle II pIXel sensor
  - Total Ionizing Dose (TID) 100 kGy/year
  - Non-Ionizing $5x10^{13}$ n_{eq}/cm^2/year
  - Hit rates up to 120 MHz/cm^2

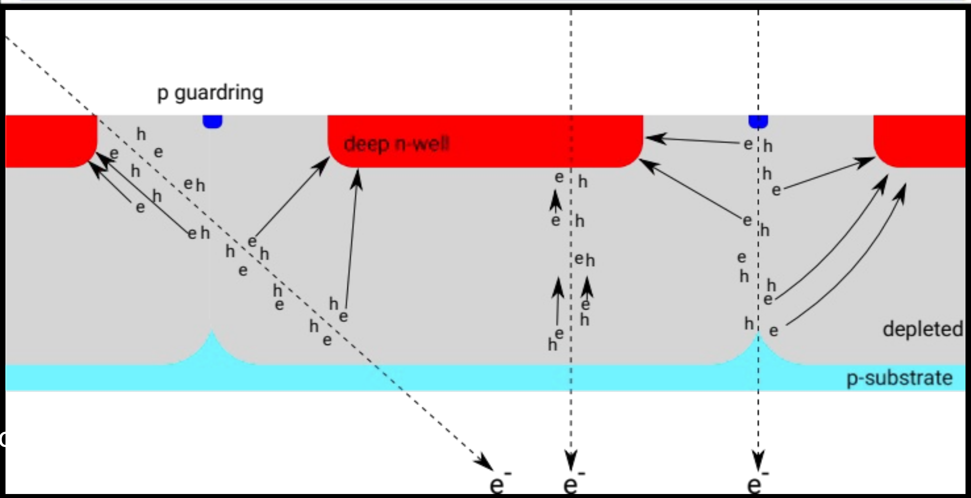
CMOS DMAPS Large Electrode

- State-of-the-art MUPIX11 for the Mu3e experiment on TSI semiconductor H18
  - 80x80 μm^2 pixels 50μm thick
  - Time resolution<20 ns
  - 0.115% X_0/layer and efficiency>99%

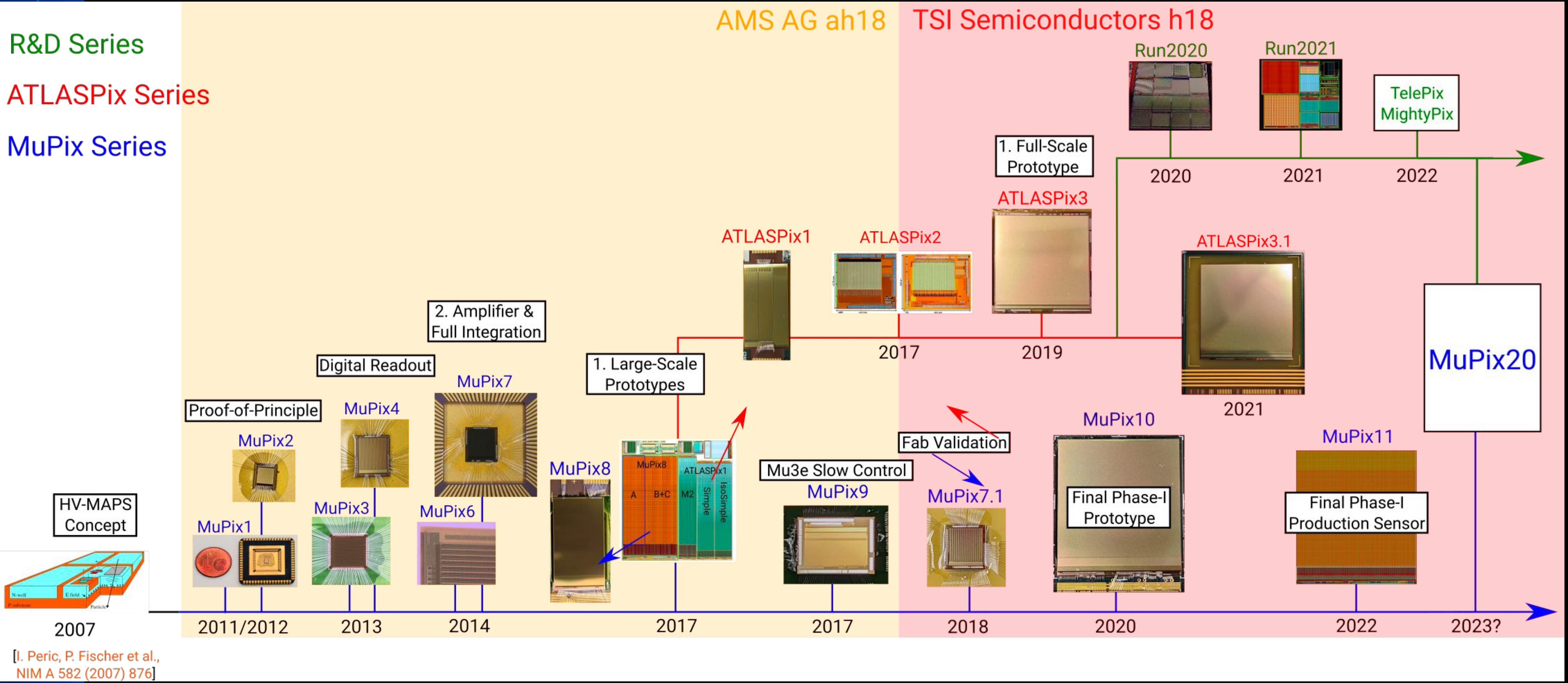
Large electrode:

- Low ohmic substrates (10-400 Ωcm)
- High voltages up to 100V
- More radiation hard



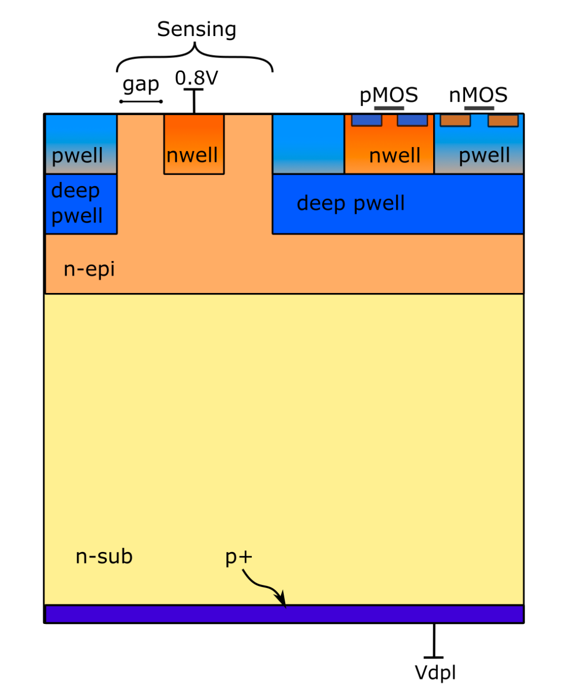


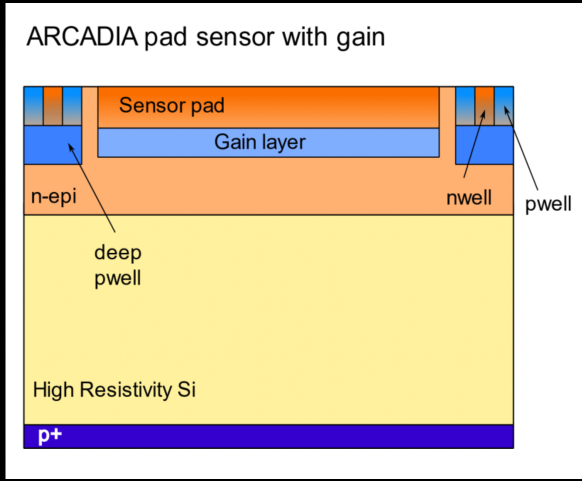
ATLASPiX/MuPix Series



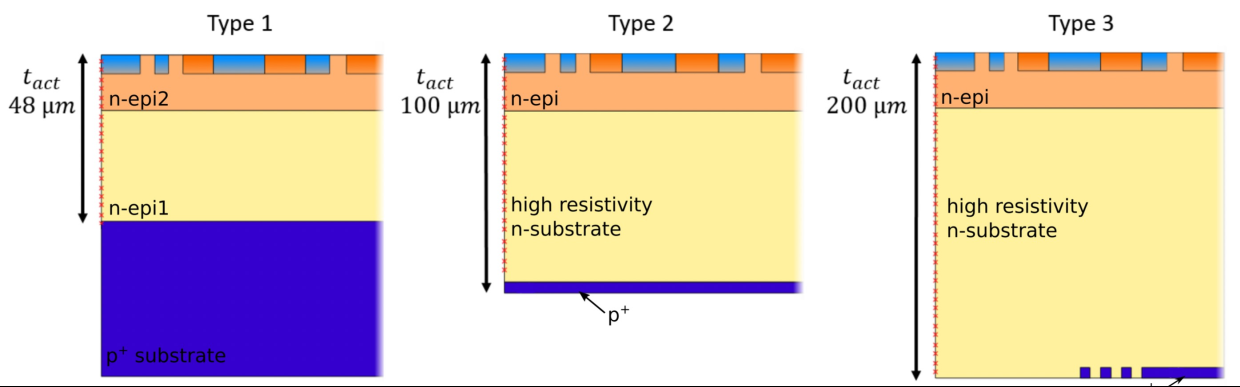
ARCADIA

- Lfoundry 110 nm CMOS process with 1.2 V transistors, developed between INFN and LFoundry
- fully depleted, charge collection by drift
- backside processing (diode+GR)
- low resistivity epi-layer
- Pixel pitch *25* µm pitch
- sensor diode about 20% of total area
- low power <50mW/cm², to allow air cooling
- side- buttable' to accommodate a 1024x512 silicon active area (2.56x1.28 cm²)
- Demonstrator 512 x 512





Wafer splits with gain layer to explore < 100 ps



23 wafers produced in first 2 production runs, 3 types/thicknesses

ARCADIA

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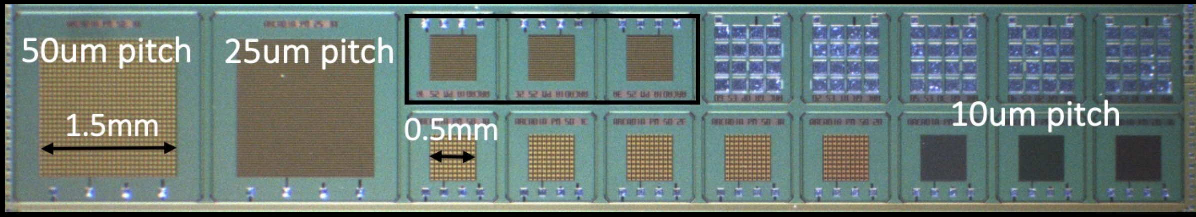
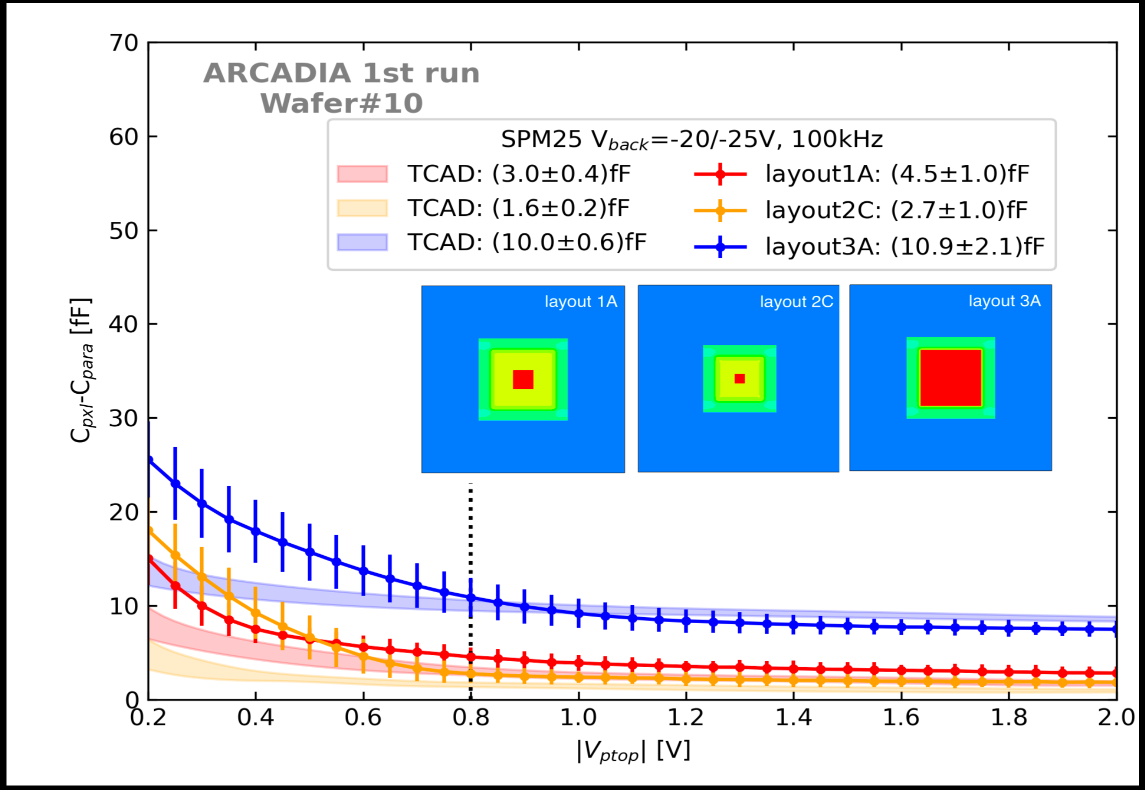
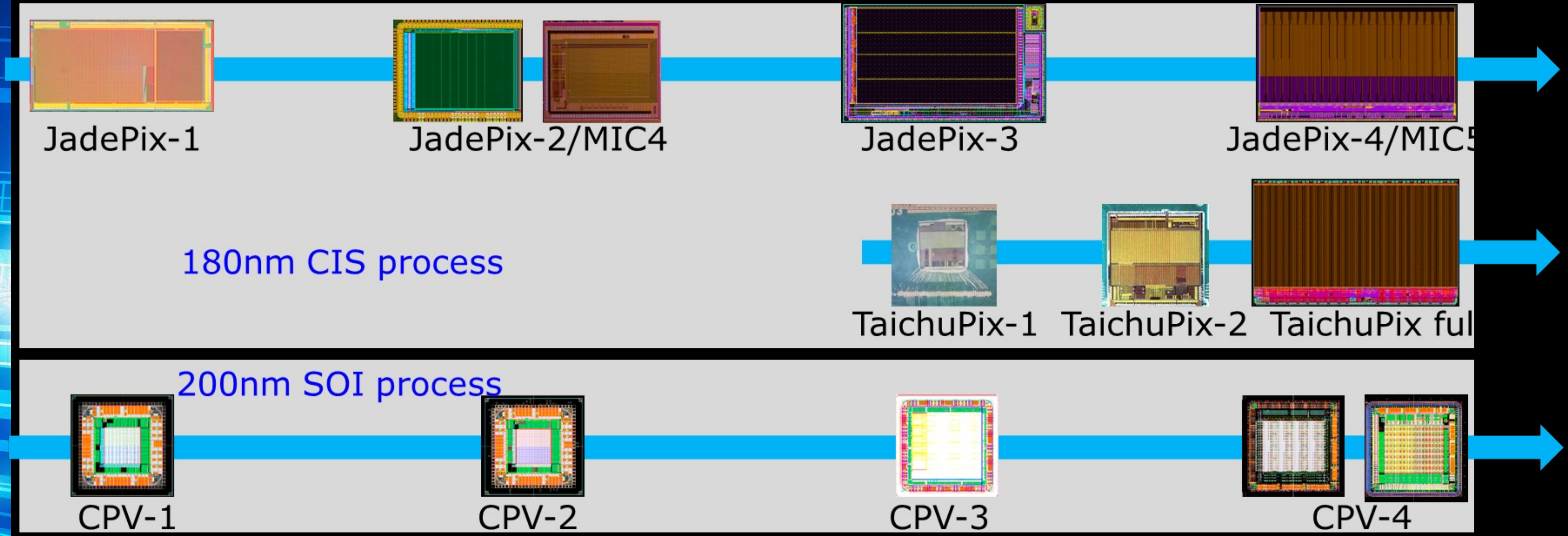




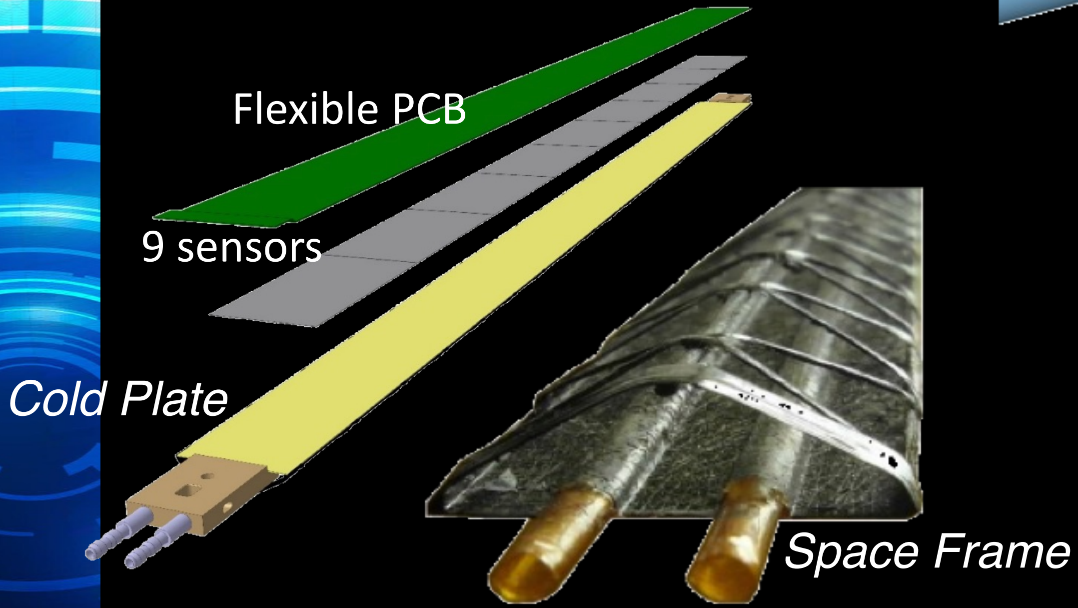
stable operation at full depletion, and good agreement with TCAD simulations

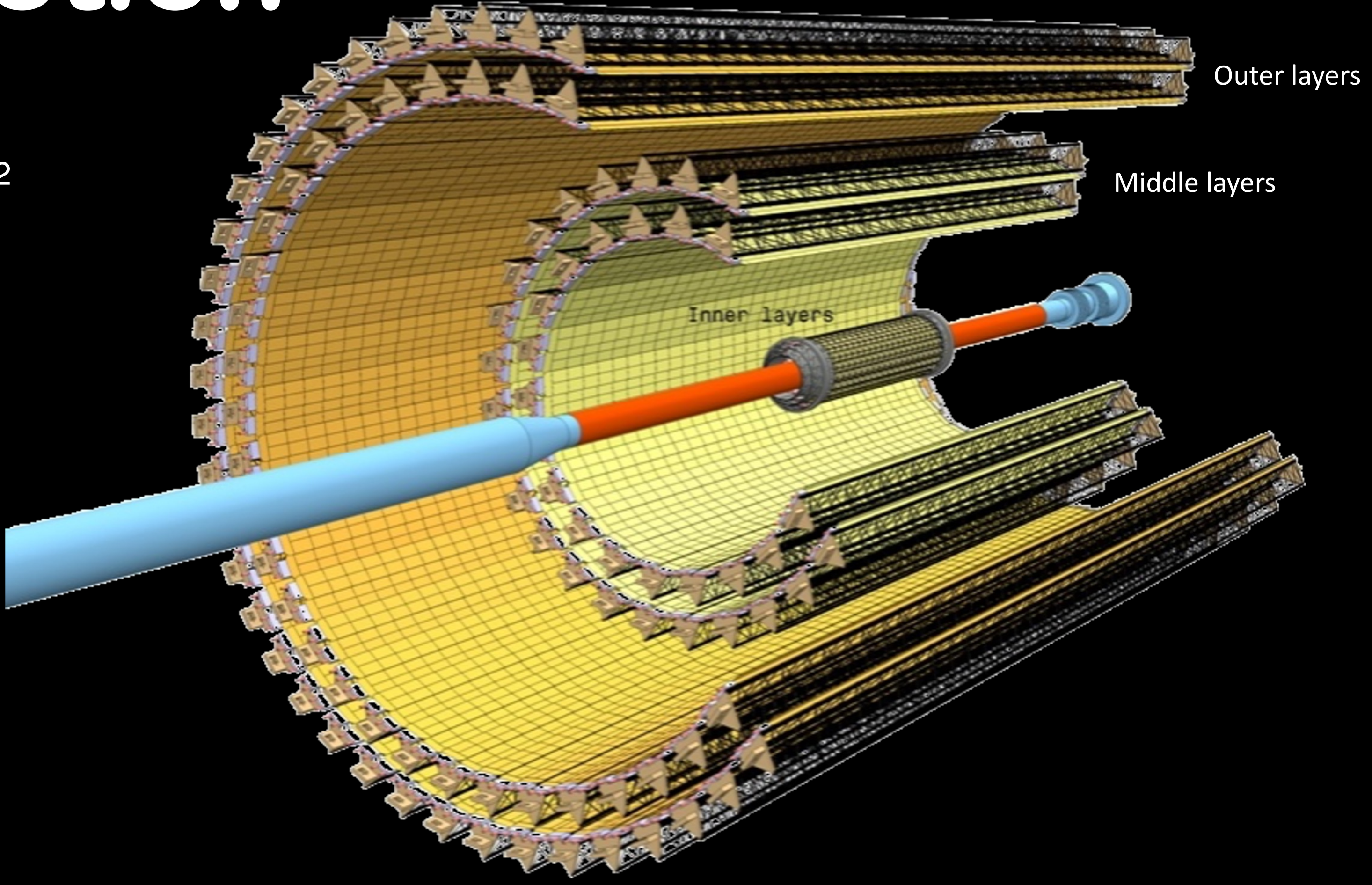
DMAPS for CEPC



Material reduction

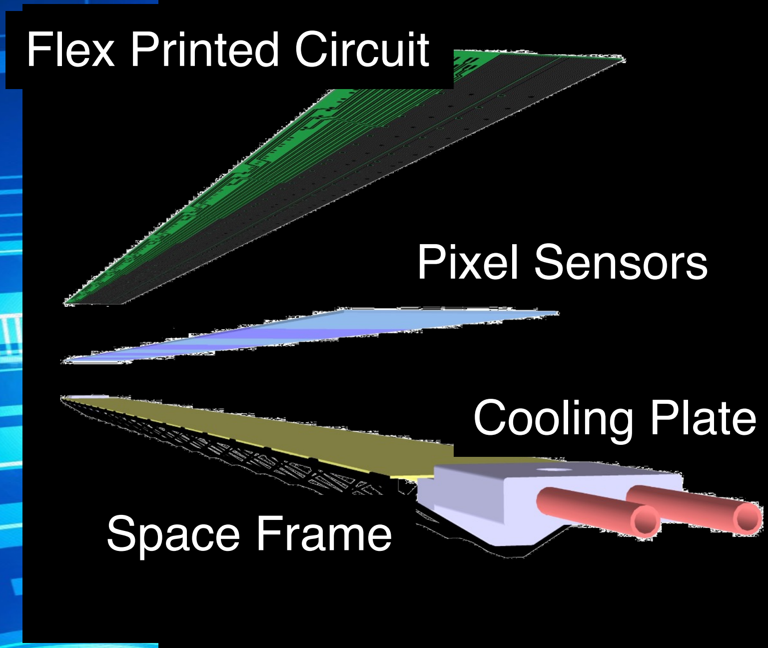
- ALICE MAPS-CMOS Tracker
  - 7-layers, 12.5 Giga pixels, $10 m^2$
  - R coverage: 23 – 400 mm
- Material/layer:
  - 0.3% X_0 (IB)
  - 1.0% X_0 (OB)

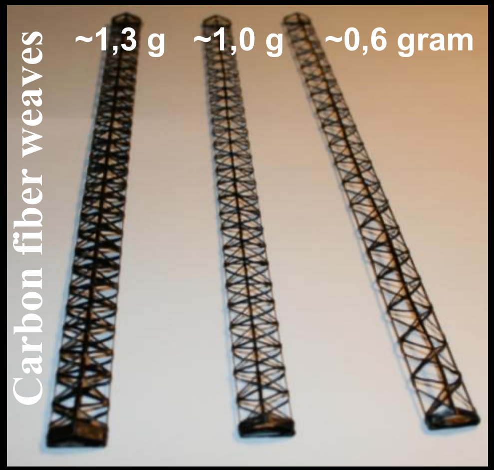


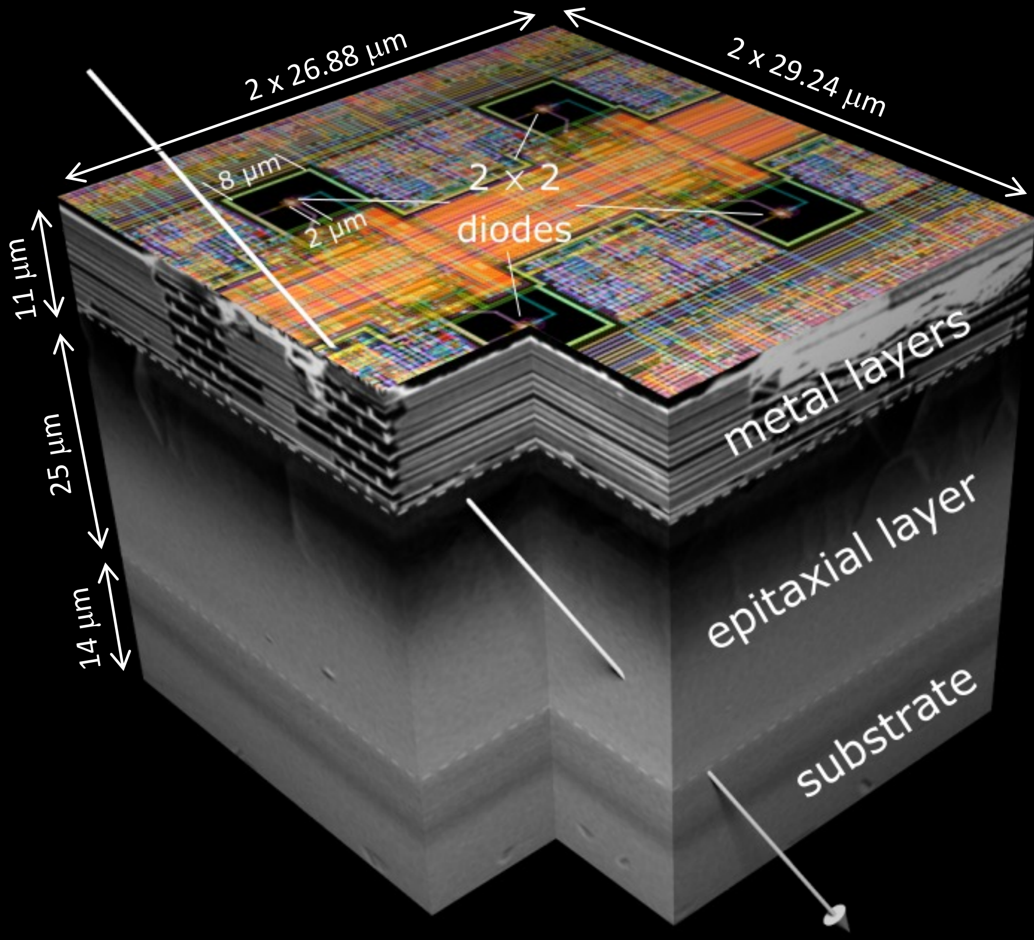


Largest CMOS MAPS detector ever built (≈ $10 m^2$)

CMOS Pixel Chips & Material



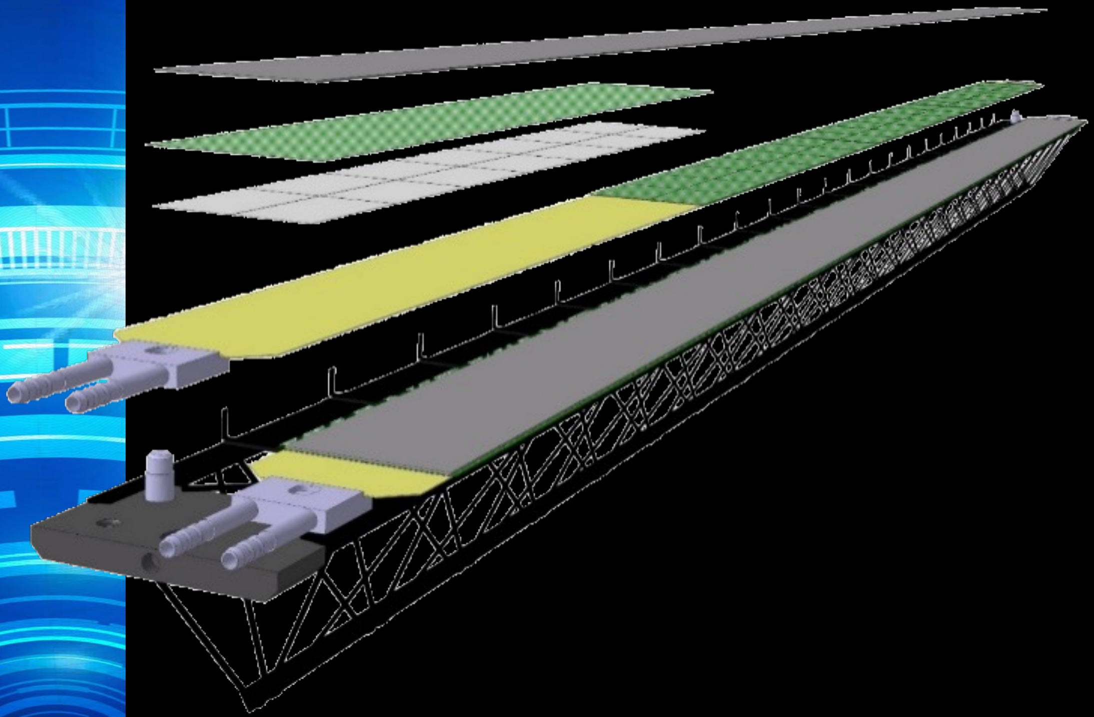




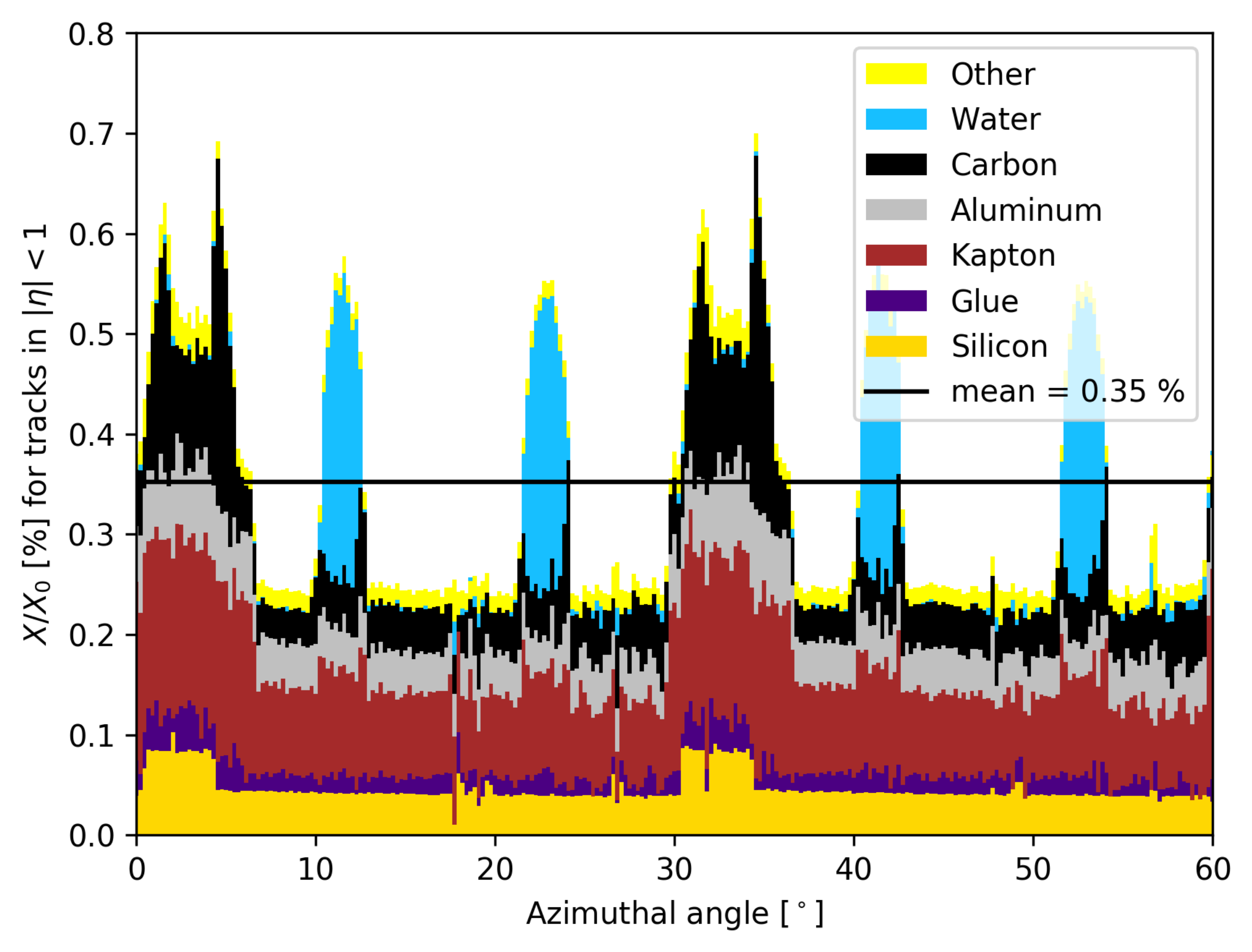
ALPIDE (ALICE)

Depleted CMOS Sensors

Minimize the material budget



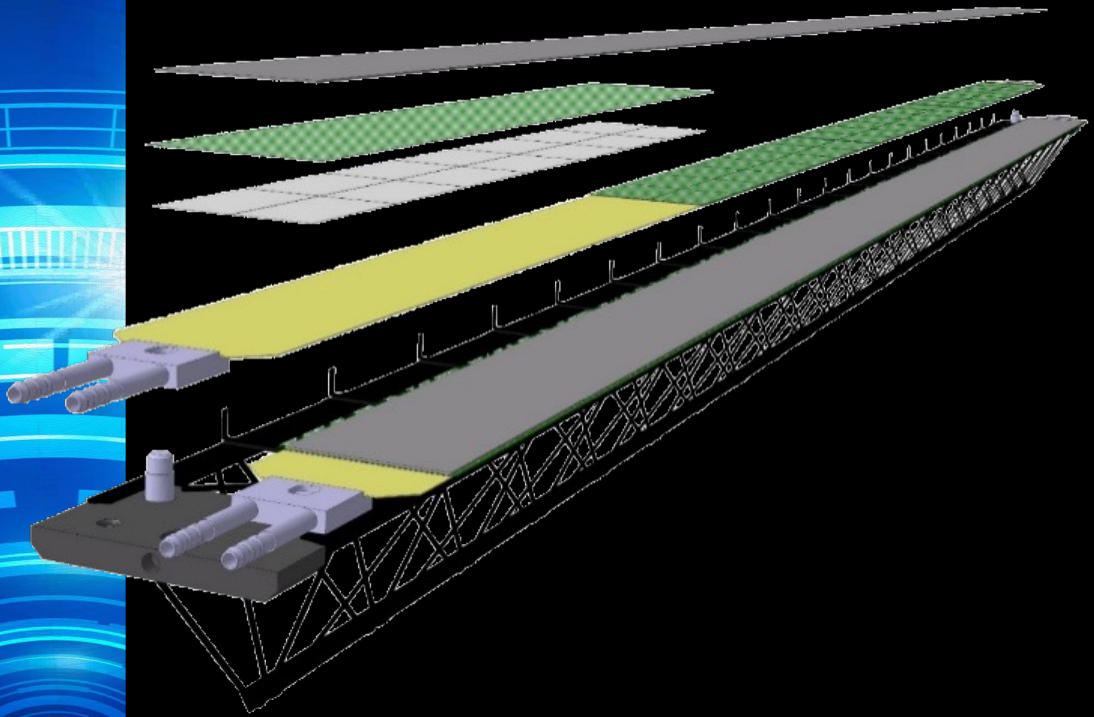
Overall Material Budget



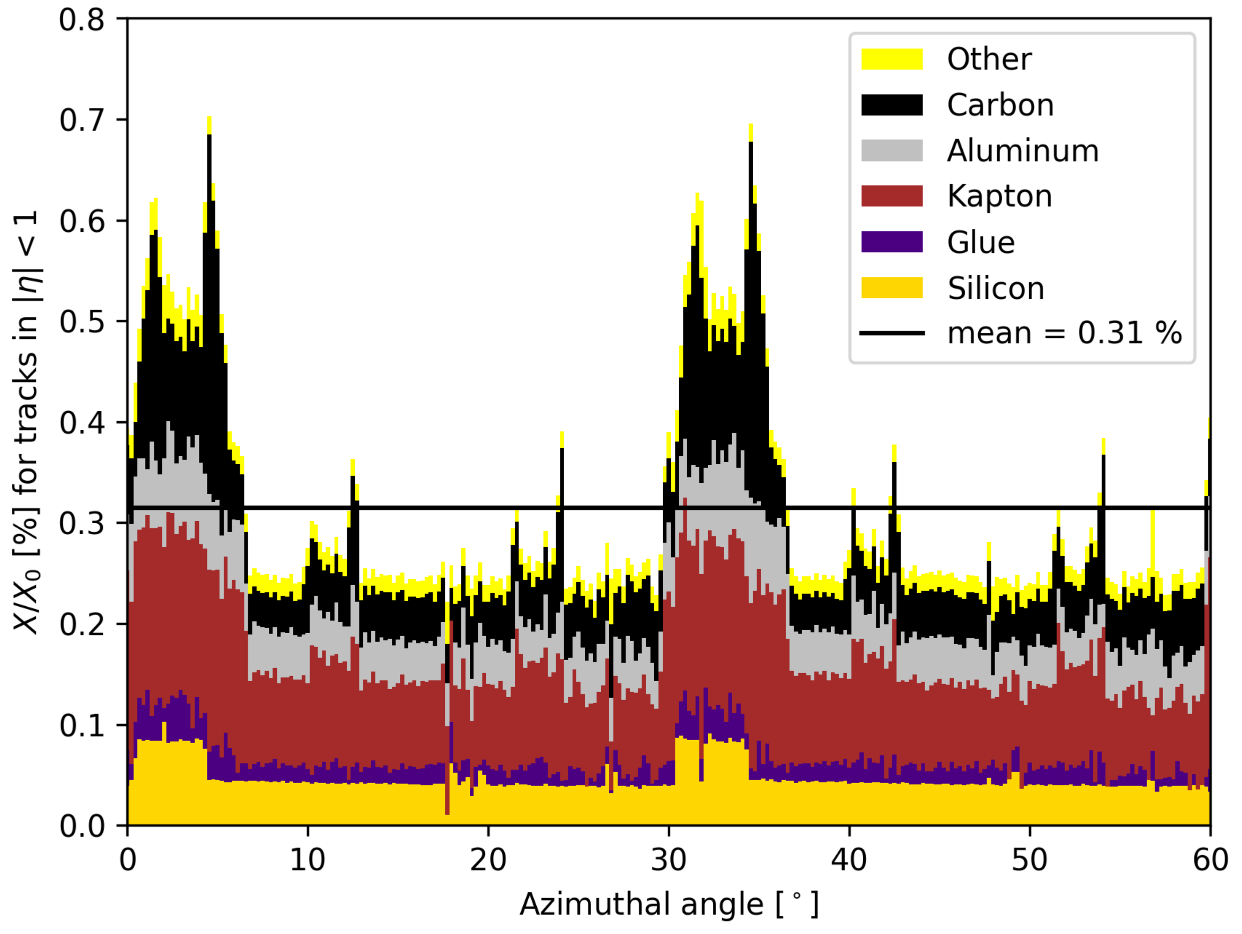
Luciano Musa, Bergen, August 2019: https://indico.cern.ch/event/836343/

Depleted CMOS Sensors

Minimize the material budget

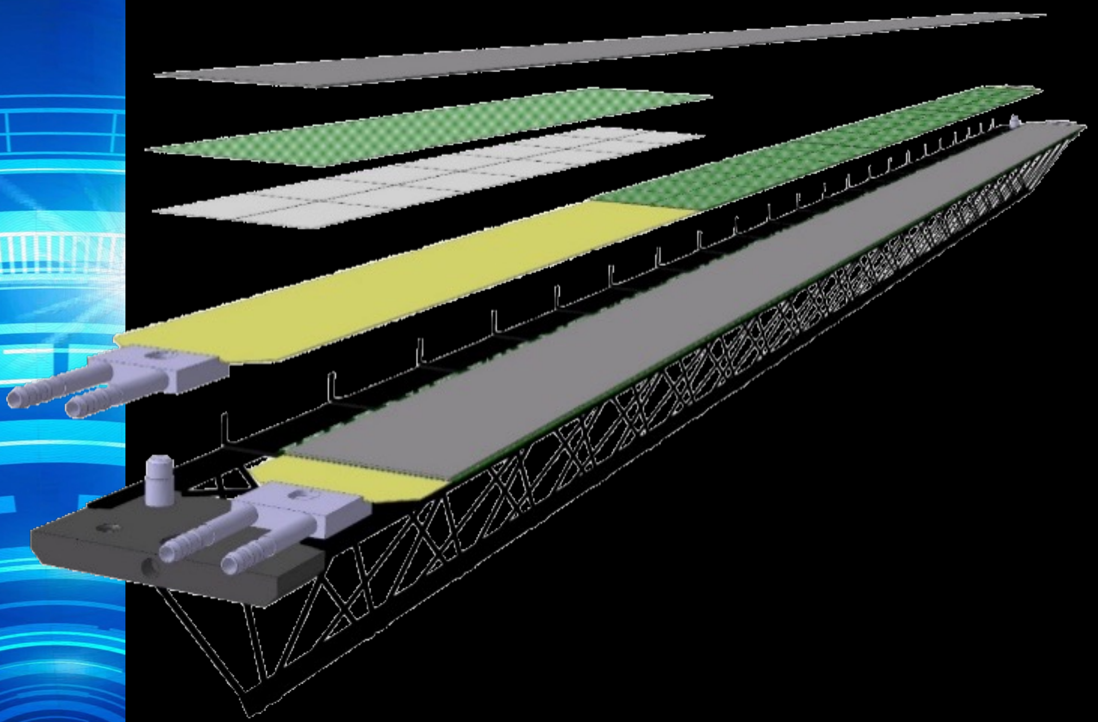


Reduce Power (< 20 mW/cm²) and Remove Cooling

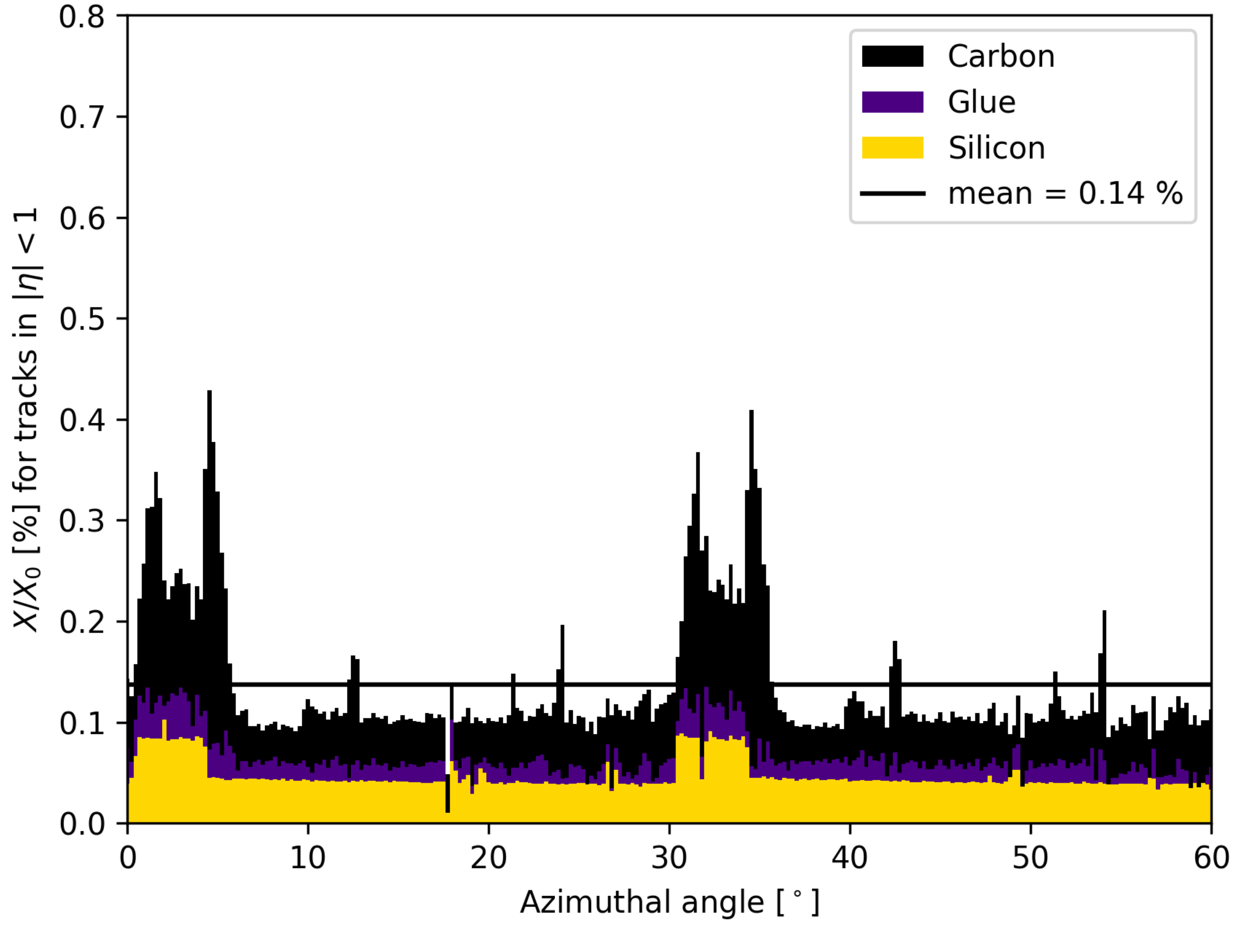


Depleted CMOS Sensors

Minimize the material budget

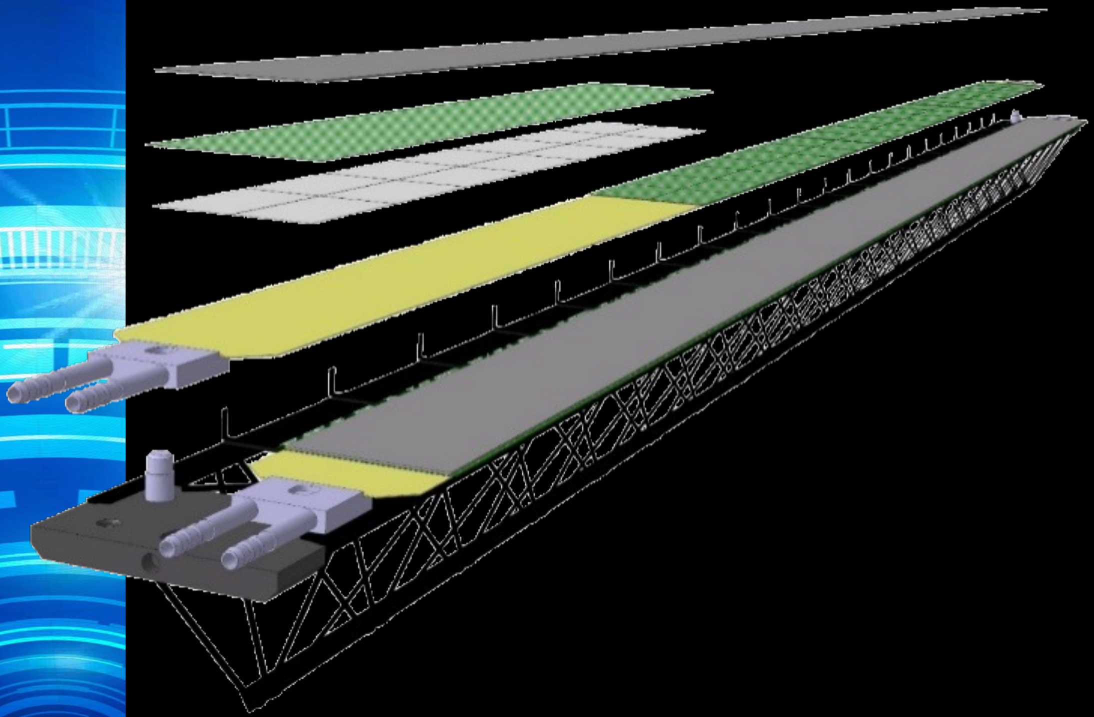


Remove PCB and integrate components on chip

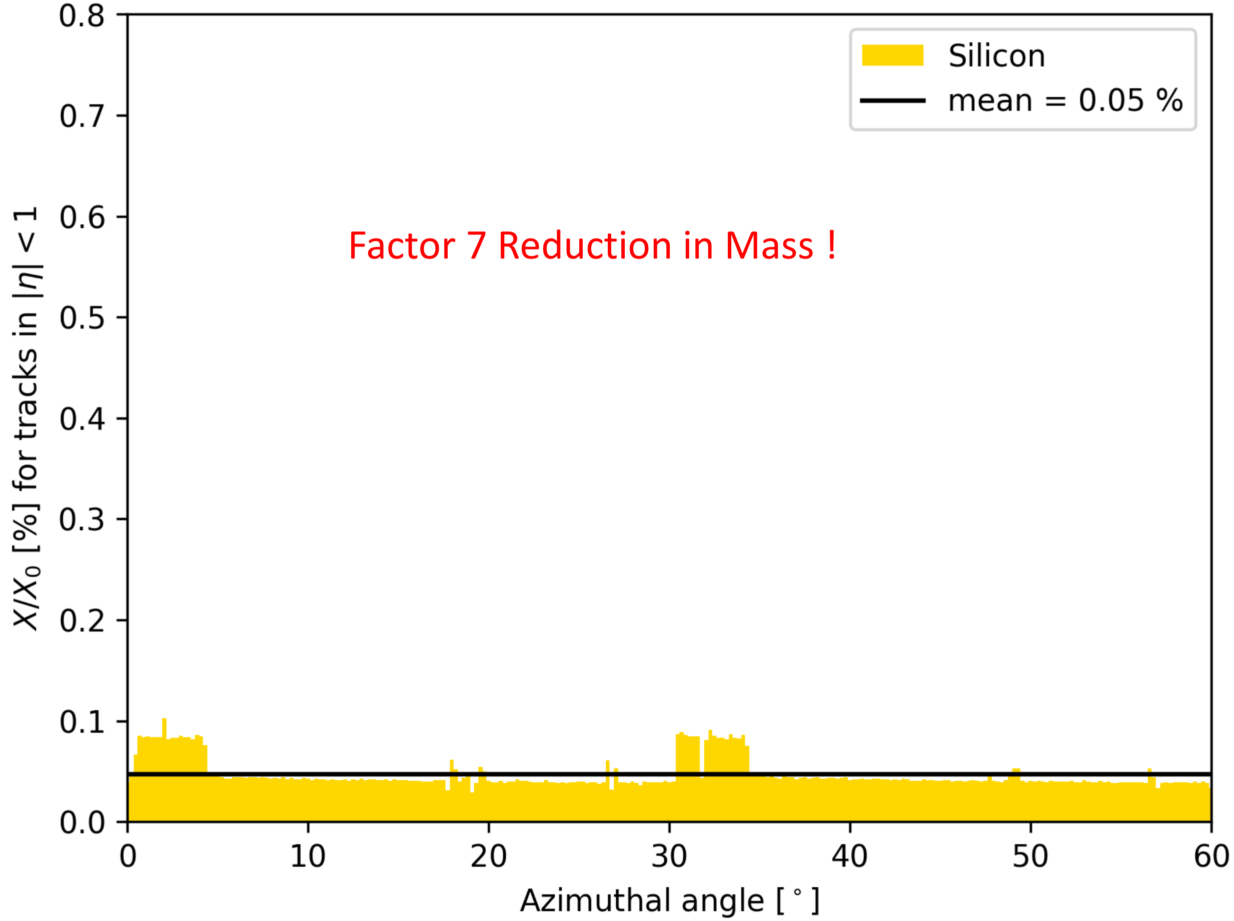


Depleted CMOS Sensors

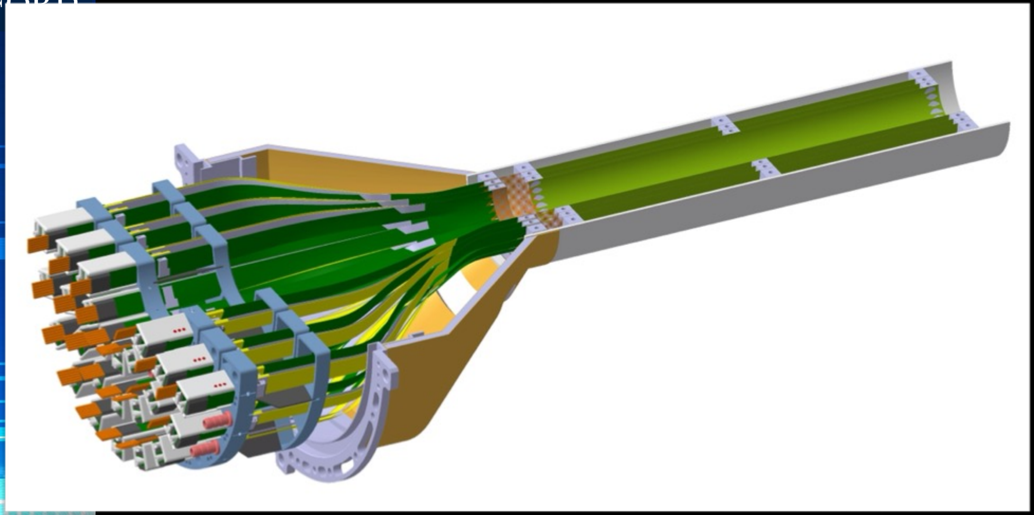
Minimize the material budget

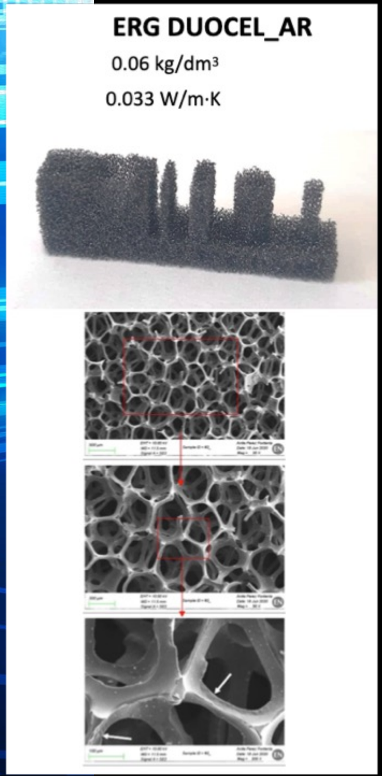


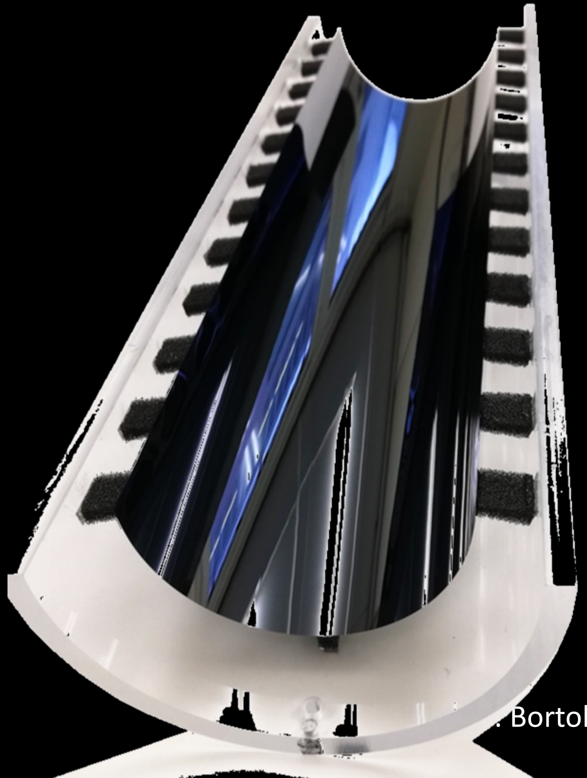
Remove mechanical support and use stiffness provided by rolling Si wafers



IT3 Concept





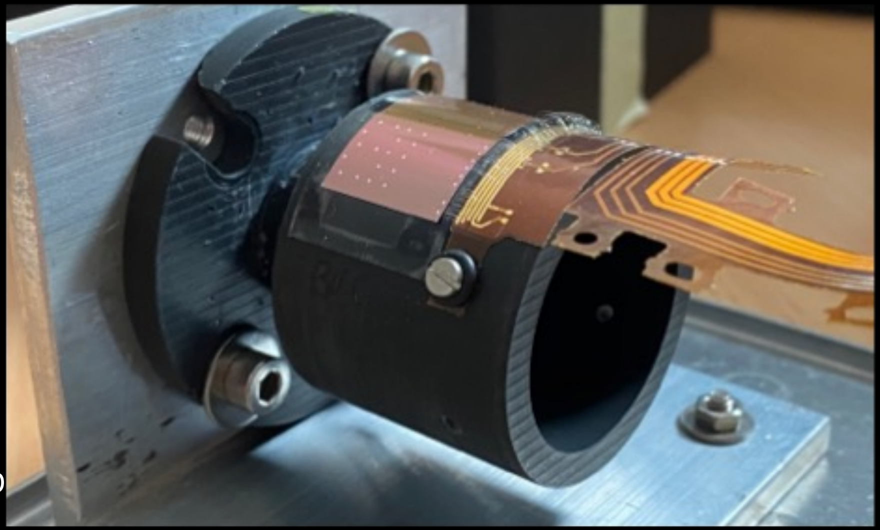


Technology advances:

- 300 mm wafer-scale chips fabricated with stitching
- thinned down to 20-40 μm bent to the target radii
- held in place by carbon foam ribs

Key benefits:

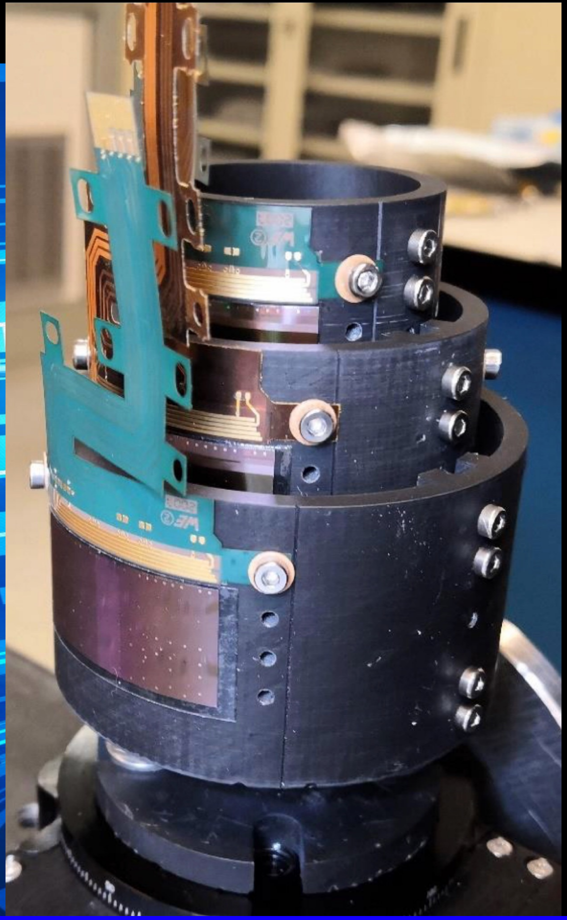
- extremely low material budget: 0.02-0.04% X_0 (beampipe: 500 μm Be: 0.14% X_0)
- homogeneous material distribution leading to smaller systematic error



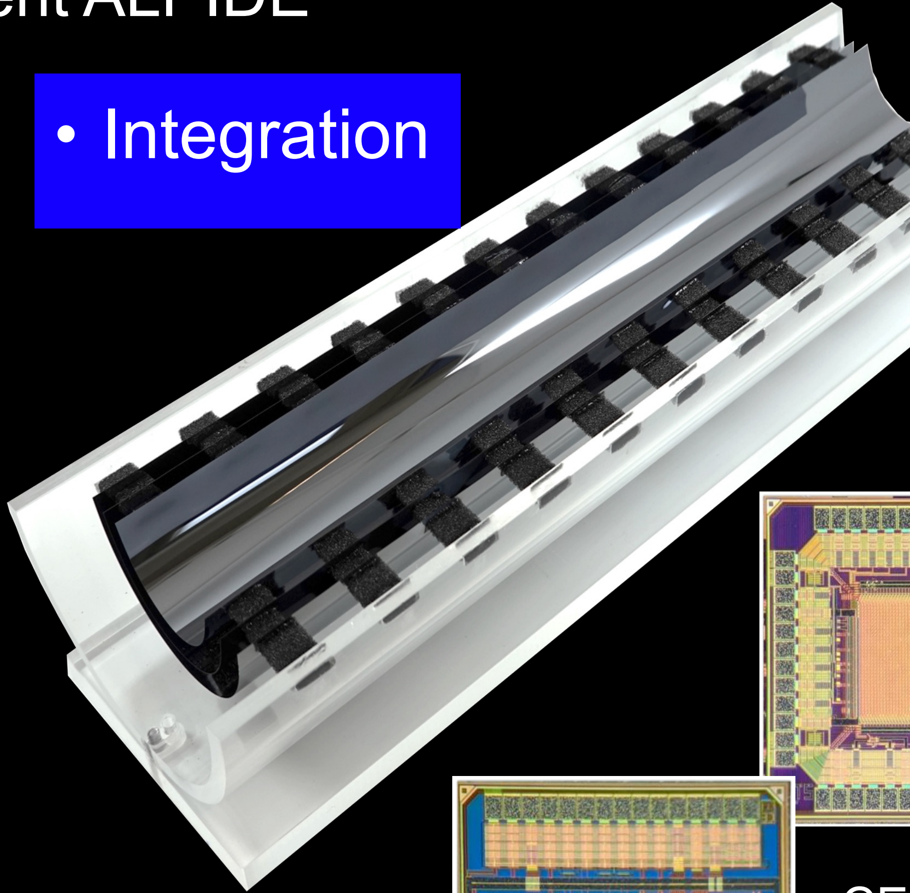
From concept to prototyping

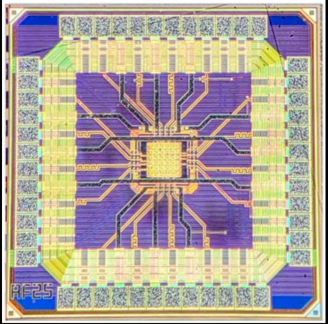
- First submission in 65 nm CMOS Imaging

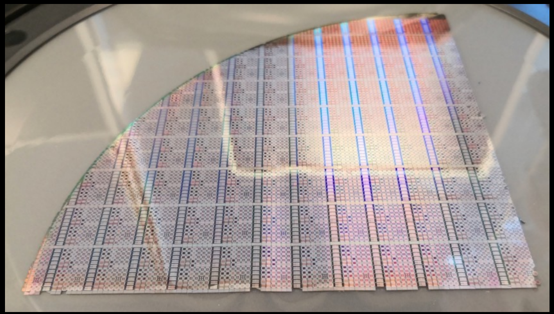
- Beam tests with bent ALPIDE



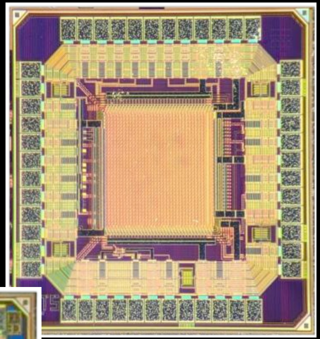
- Integration



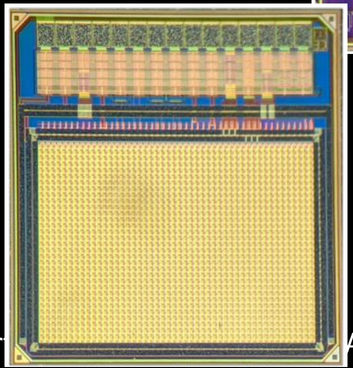




APTS
4x4 pixel matrix
10, 15, 20, 25 µm
Direct analogue readout



DPTS
32 × 32 pixels
15 µm pitch
Asynchronous digital readout
ToT information



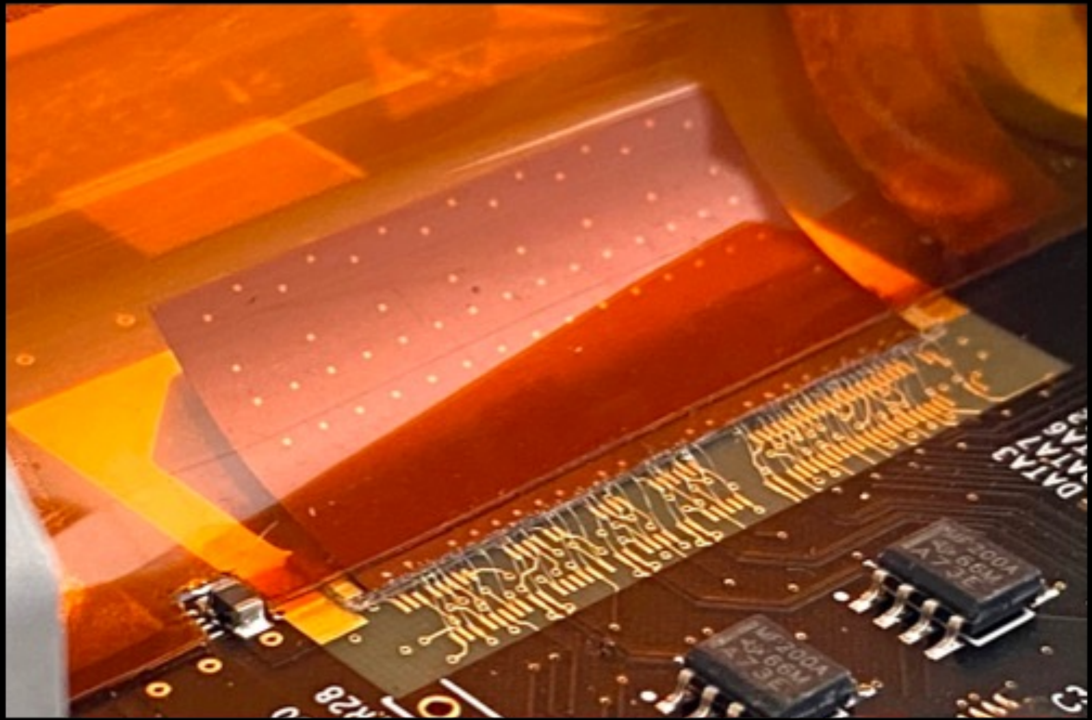
CE65
64 × 32 pixels
15 µm pitch
Rolling shutter analog readout

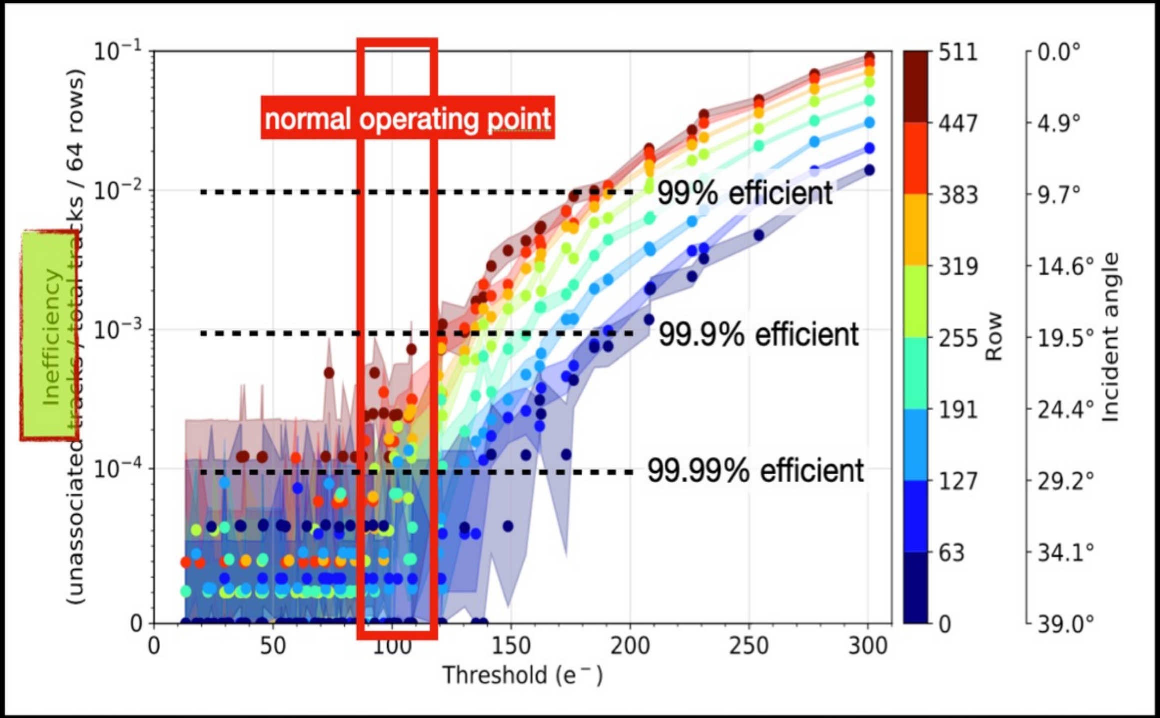
ER1 Submission
Two large stitched sensor chips (MOSS, MOST)

Working of bent sensors demonstrated with ALPIDE

Test beams

June 2020 test beam data shows that bent MAPS work perfectly

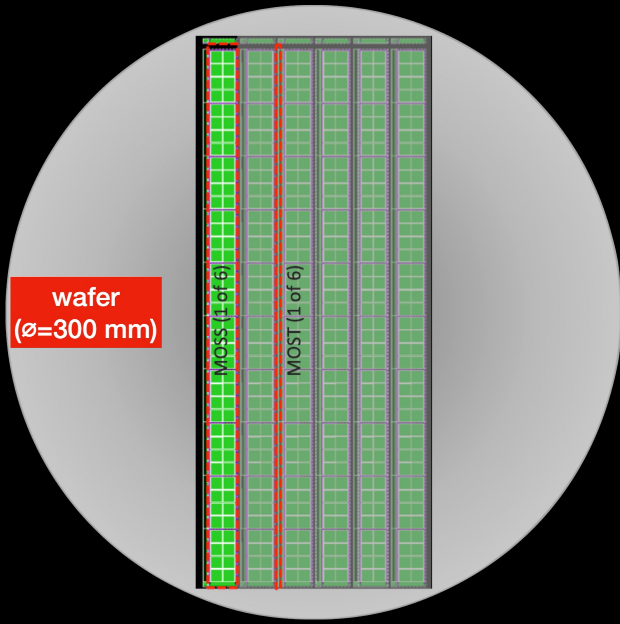




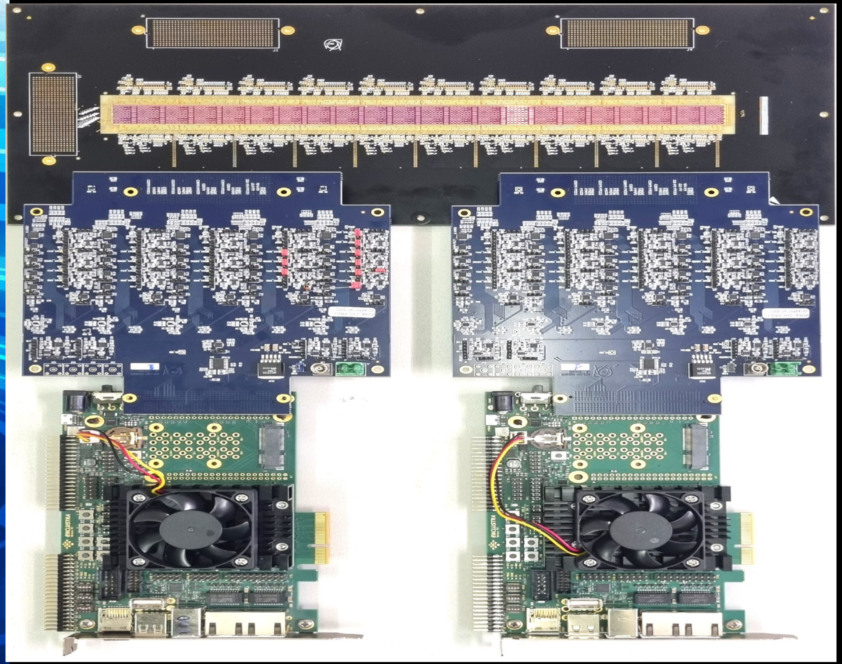
Collaboration investigating TowerJazz 65 nm

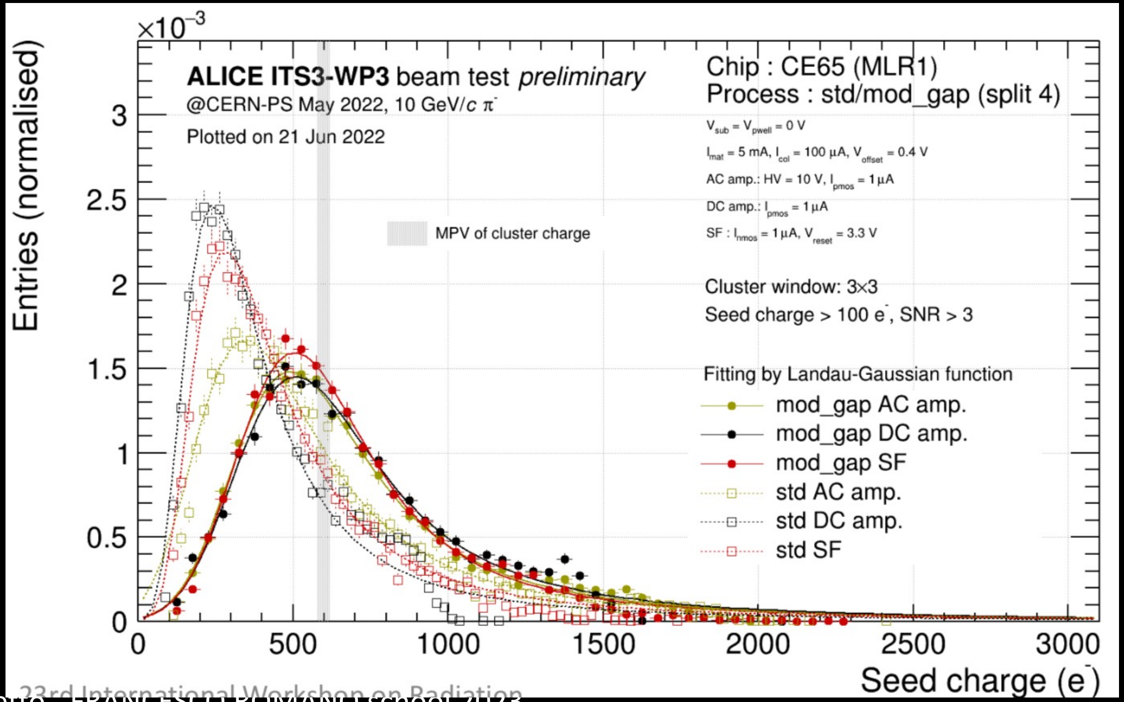
Magnus Mager (CERN) | ALICE ITS3 | TIPP 2021 | 26.05.2021 |

From concept to prototyping

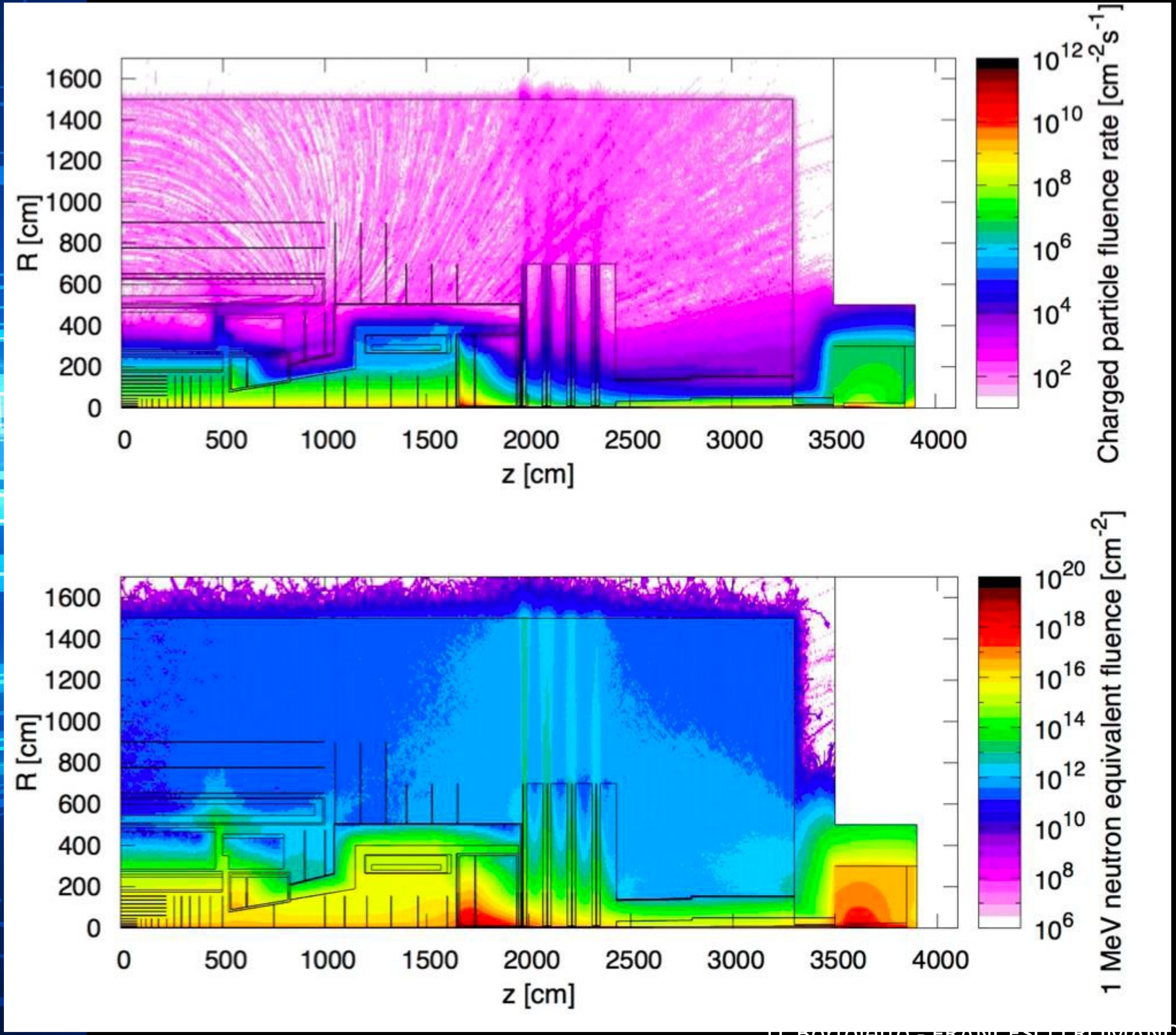


- Two submissions to check stitching so far
  - Multi Layer Reticule MLR1 (2020) sensor 10-25 μm pitch, 10 μm epi Checking process modifications
  - Engineering run (ER1) to check stitching





Proton Collider Parameters

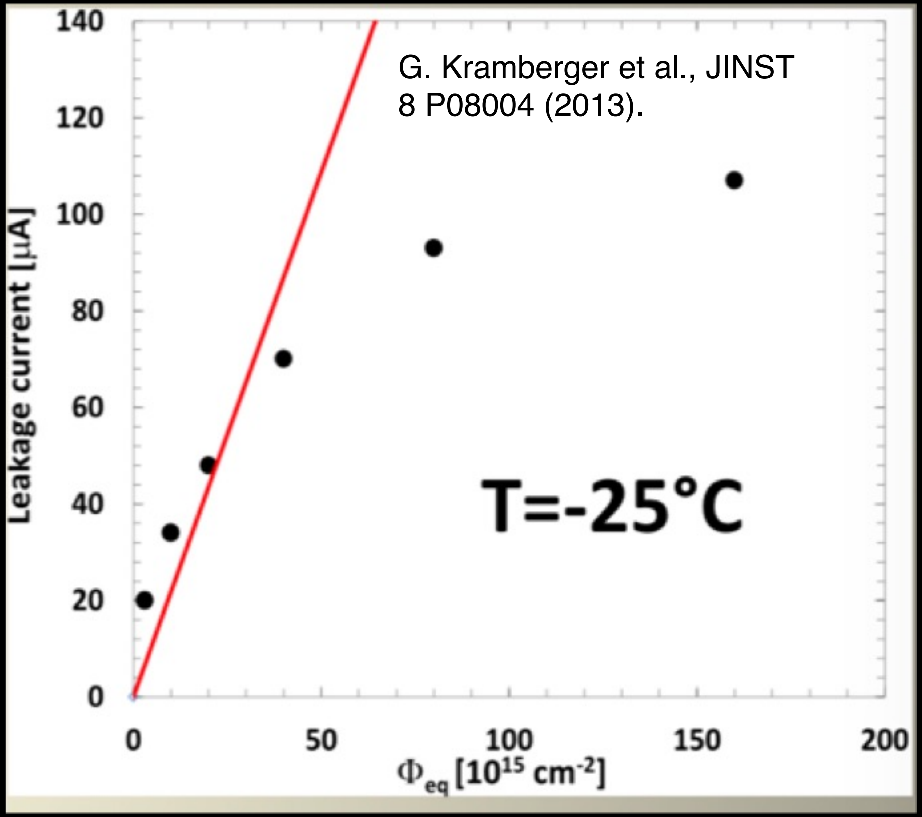


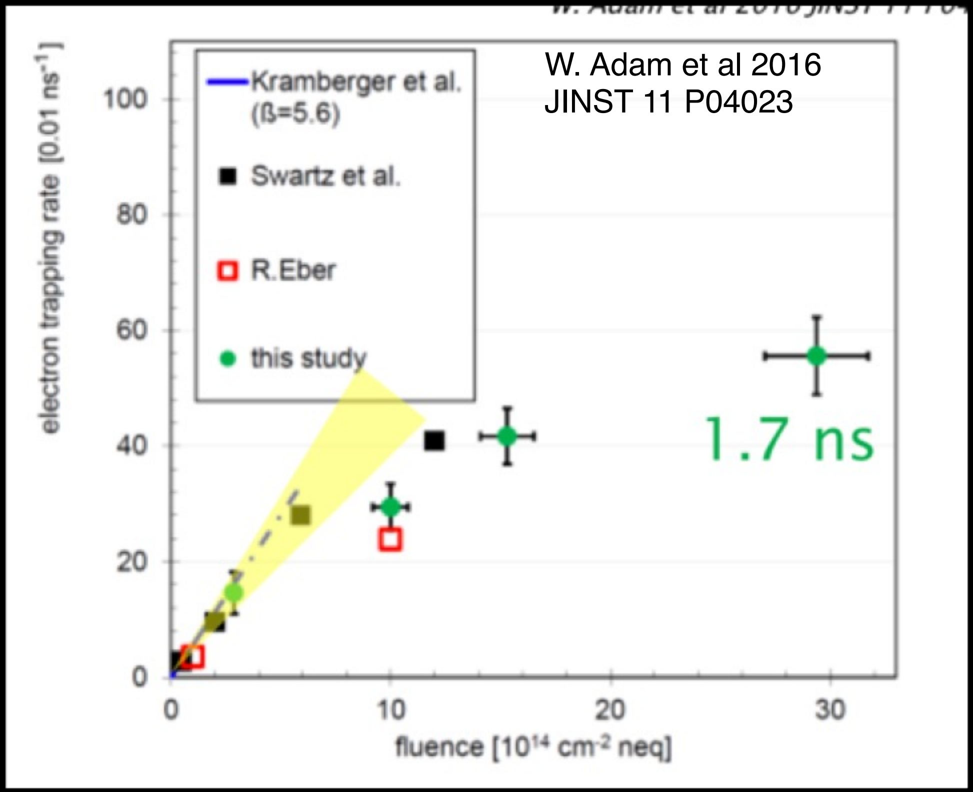
First tracking layer:

- 10 GHz/cm^2 charged particles
- 10^{18} hadrons/cm^2 for 30 ab^{-1} (100 x HL-LHC)

Extreme Radiation Damage

- HL-LHC: fluence at the innermost layers of the tracker ≃2 E16 n/cm^2
- Test have been conducted up to over E17 n_{eq}/cm^2





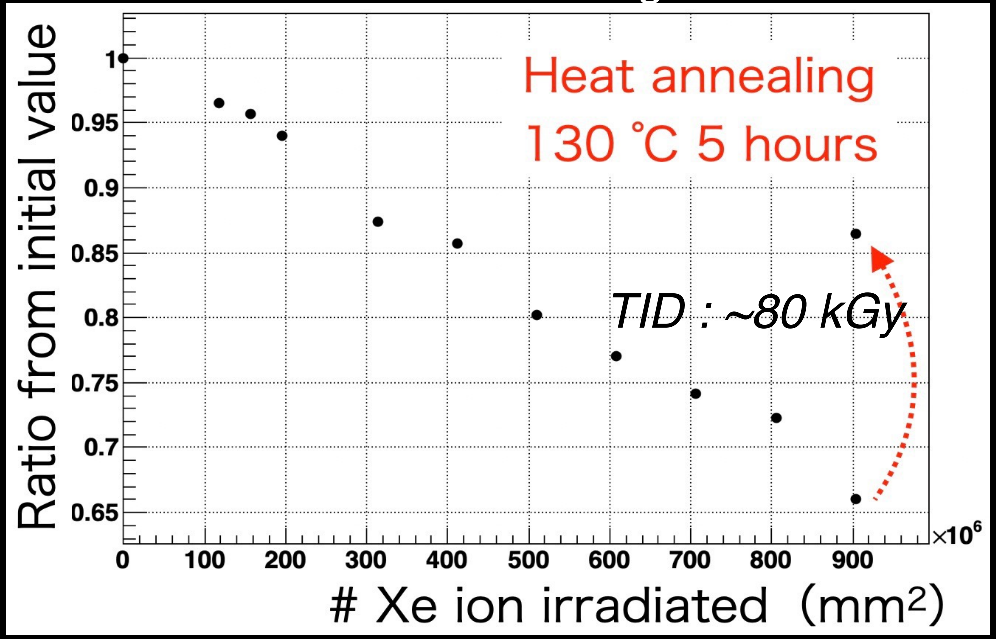
Leakage current saturates

Trapping slows down

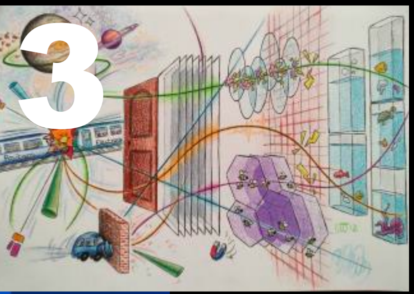
R&D on silicon at Extreme fluences

- CIGS(Cu,In,Ga,Se) was developed for solar cell
- Higher photon efficiency compared with Si and promising thin-film sensor
- Defects due to radiation degrades performance of sensor
- In the CIGS crystal, ions compensates defects with heat annealing and structural characteristics is recovered
- High radiation tolerance is expected

Manabu Togawa KeK and QPI



DRD



WG3.6 on new materials:

- SiC Higher quality material available:
  - Power-efficient transistors in power supplies
  - Photovoltaic inverters
  - Electric car drive train
  - SiC-CMOS at Frauenhofer IIHS offers two MPW submissions per year
- Diamond and 2 D Materials (graphene)

- GaN :
  - Communications: cell phone chips, 5G base stations, LEO satellites, VSAT,
  - Automotive –LiDAR, power switches, power distribution
  - Aerospace –power amplifiers, radiation-hardened RF electronics
  - Military and defense –radar, military communications, electronic warfare

R&D on silicon at Extreme fluences

Manabu Togawa (KeK and QUP)

- CIGS(Cu,In,Ga,Se) was developed for solar cell
- Higher photon efficiency compared with Si and promising thin-film sensor
- Defects due to radiation degrades performance of sensor
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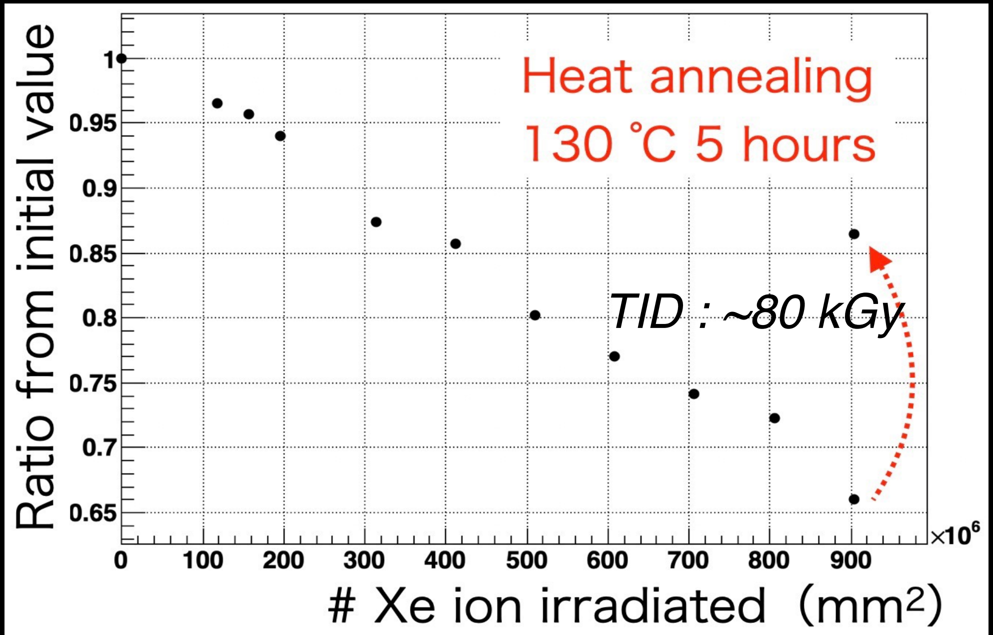
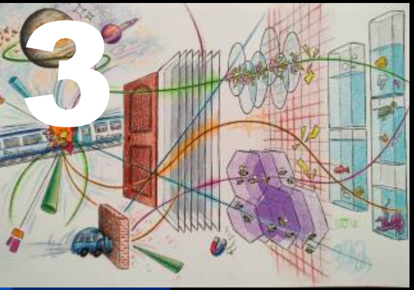
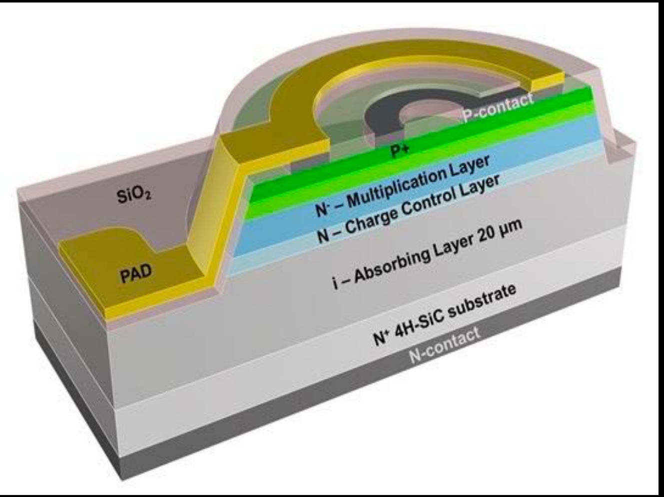


DRD SiC

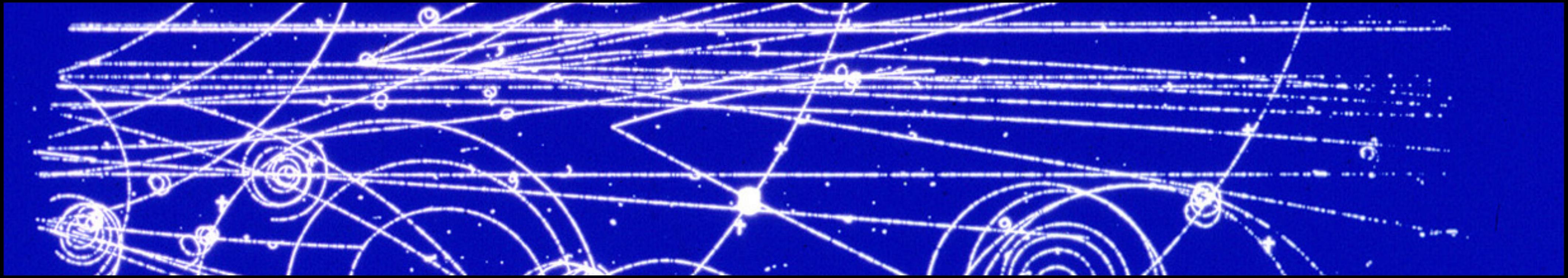


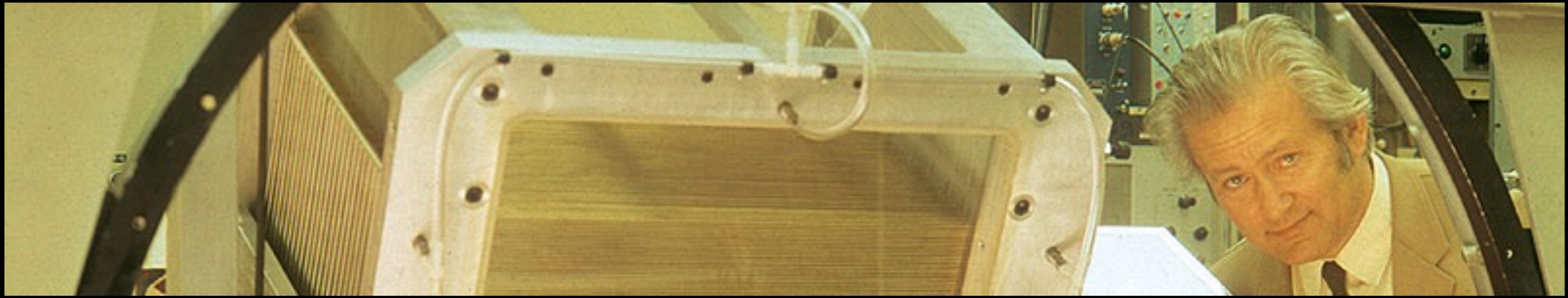


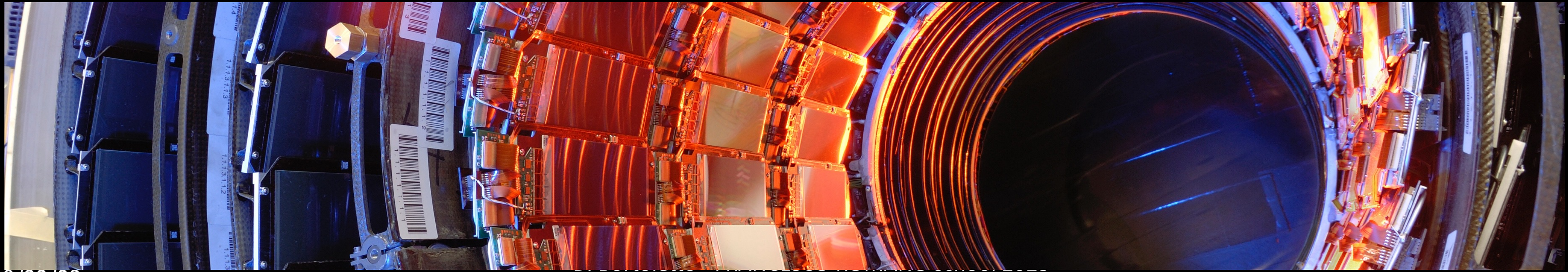
SiC LGADS

- Technological challenges:
  - —Only n-type substrates available
  - —Deep gain layer implant needs very high energy
- Progress at Nanjing University (NJU): gain <5 but early breakdown
- **New RD50 common project** for SiC-LGAD

Perspective







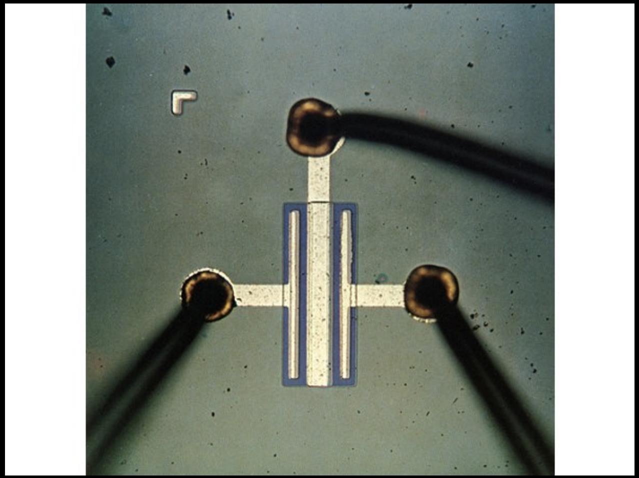
Conclusions

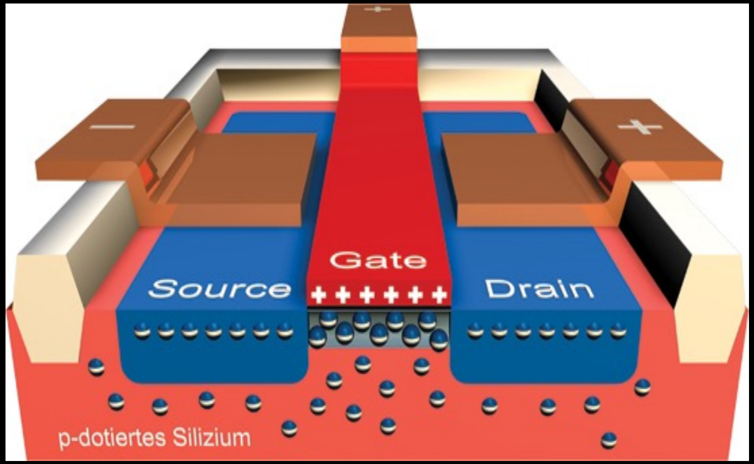
"Ultimate goal remains a massless, cheap, infinite granularity, 100% hermetic and efficient, infinite bandwidth, long lifetime detector"

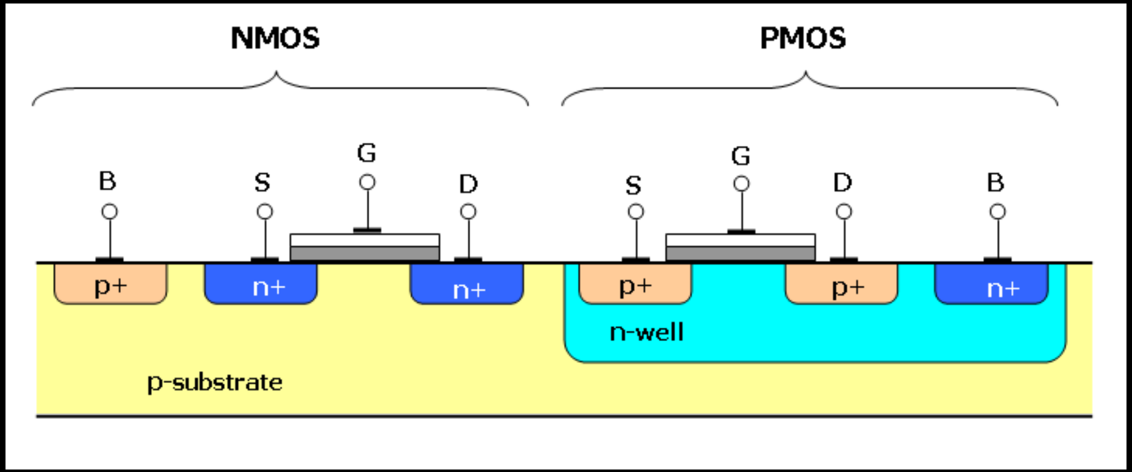
"Ultimate goal remains an ultra-fast, massless, cheap, infinite granularity, 100% hermetic and efficient, infinite bandwidth, long lifetime detector"

CMOS

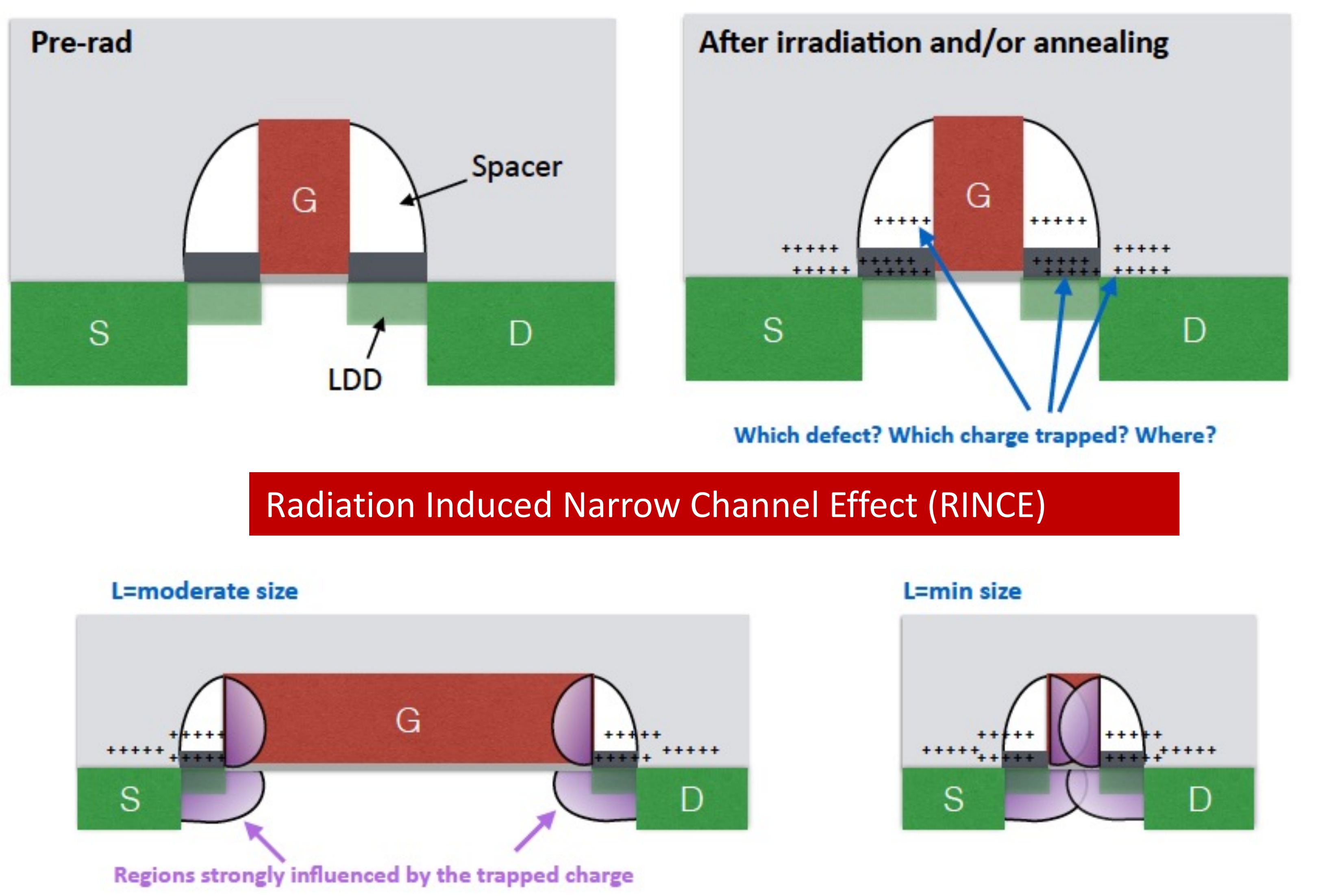
- The CMOS stays for the complementary metal oxide semiconductor transistor (a type of field effect transistor, F. Wanlass 1963)
- First MOSFET was realized in 1959 Dawon Kahng and Martin M. Atalla.







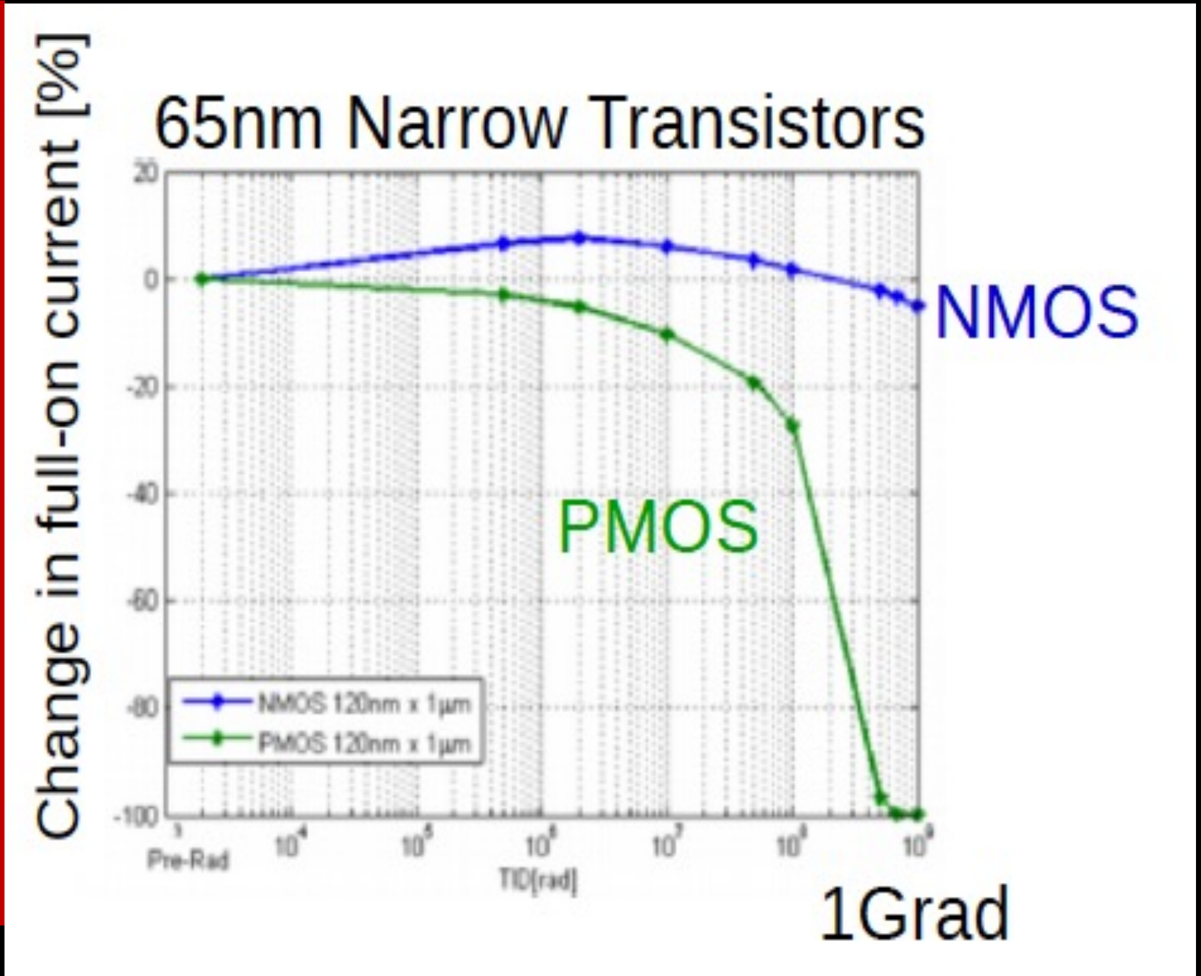
Radiation effects in 65 nm CMOS



Federico Faccio, TWEPP 2015

Radiation effects in 65 nm CMOS

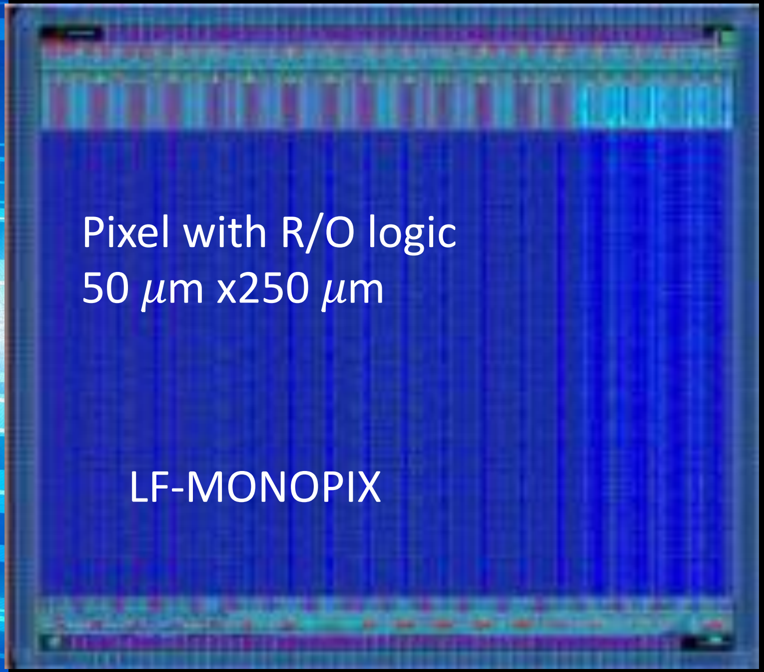
- NMOS are working without large damage up to 1Grad (damage < 20%)
- PMOS transistors do not work above 500Mrad
- Further studies ongoing including DRAD chip to investigate different transistors (size and shape)



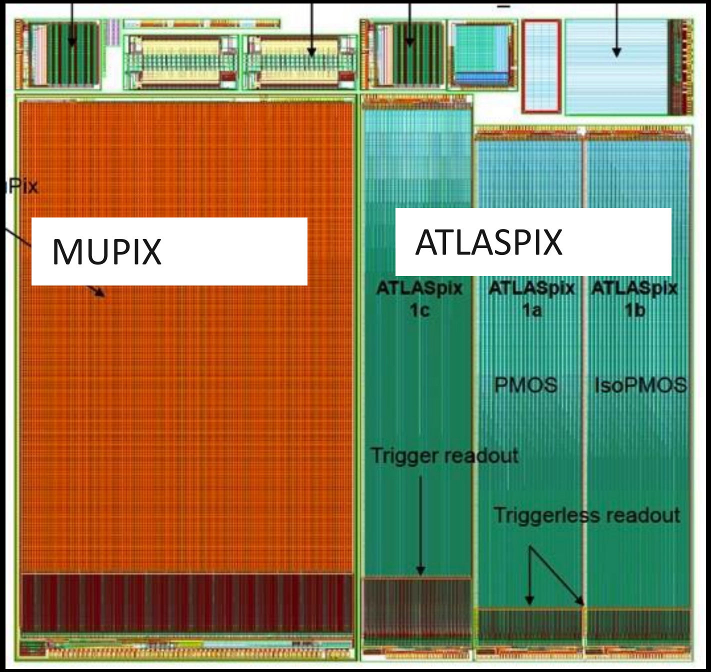
ATLAS CMOS DEMONSTRATOR PROGRAM

WITH SEVERAL FOUNDRIES

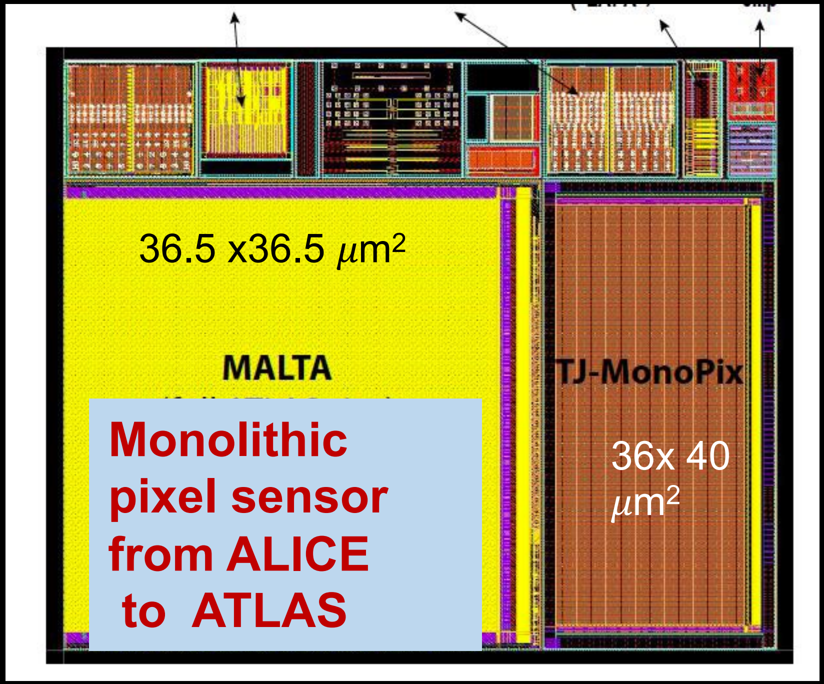
LFOUNDRY



ams



TOWERJAZZ

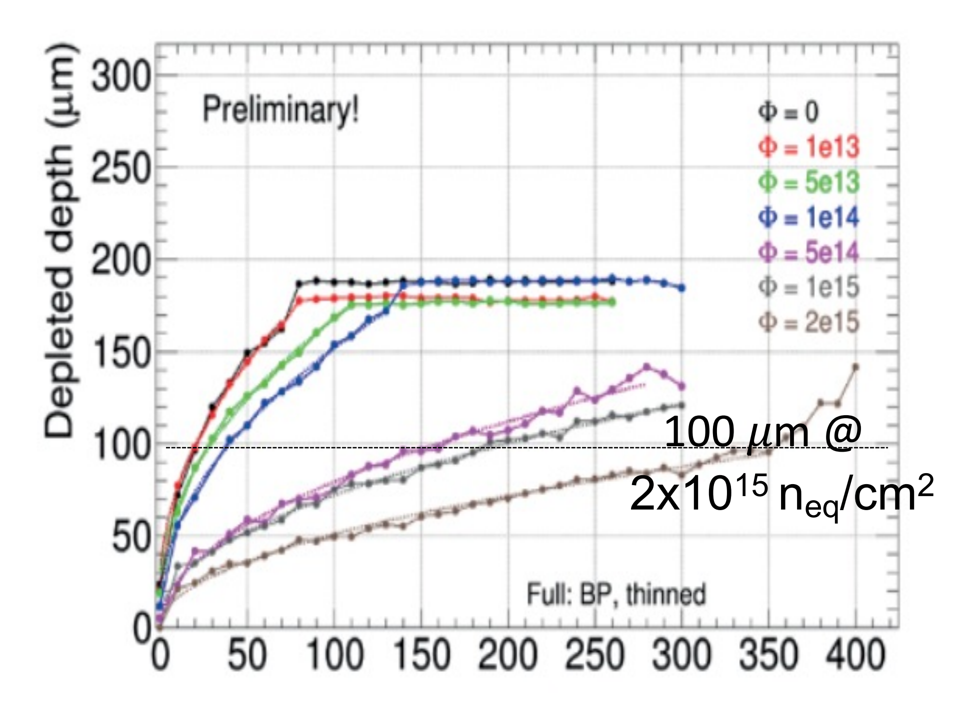


DMAPS development important for LHCb upgrade II, CepC, CLIC, ILC, FCCee and FCChh

ATLAS CMOS DEMONSTRATOR PROGRAM

Radiation hardness to a fluence of $2x10^{15}$ 1 MeV n_{eq}/cm^2

LFOUNDRY



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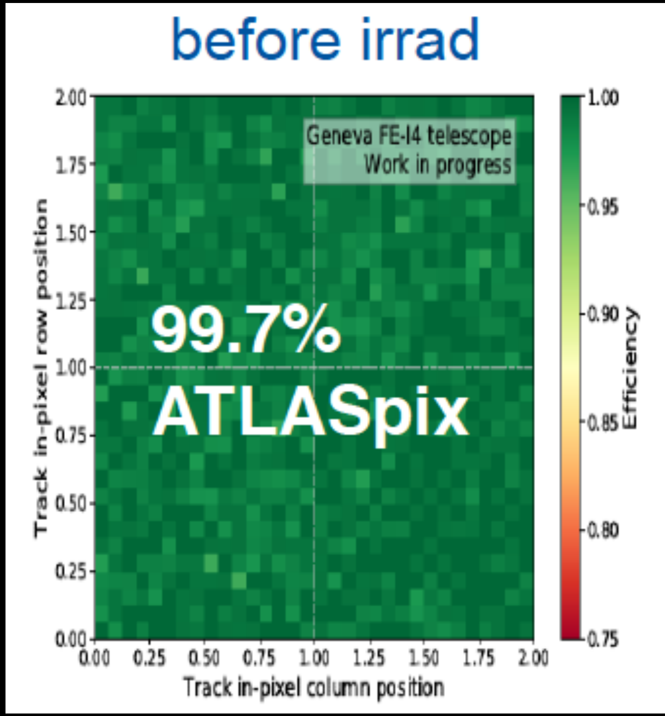
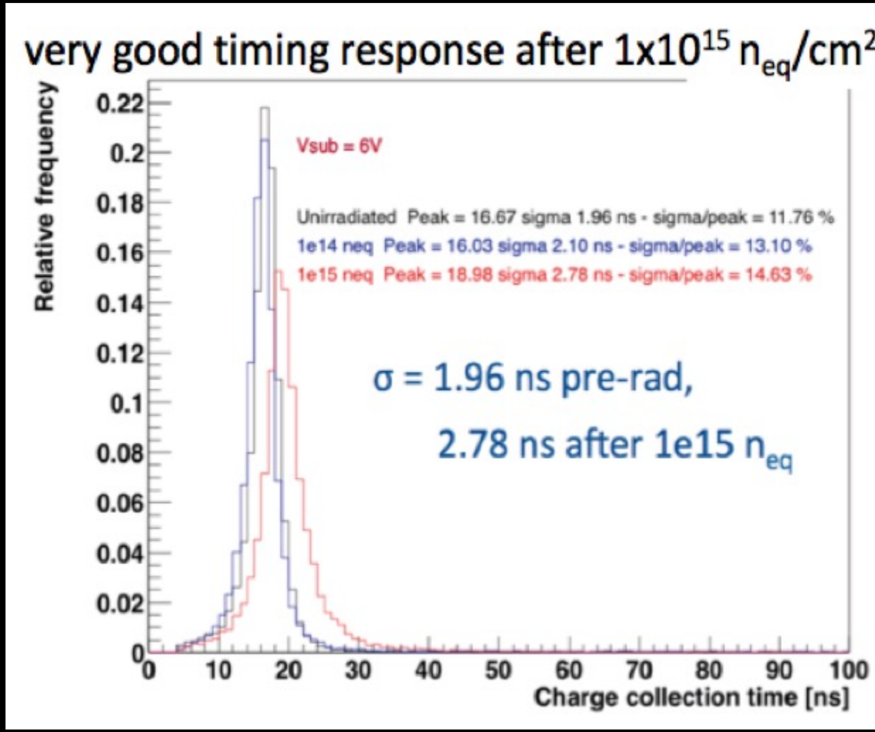


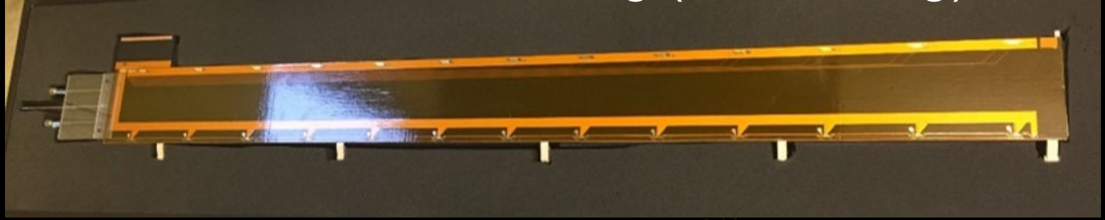
TOWERJAZZ



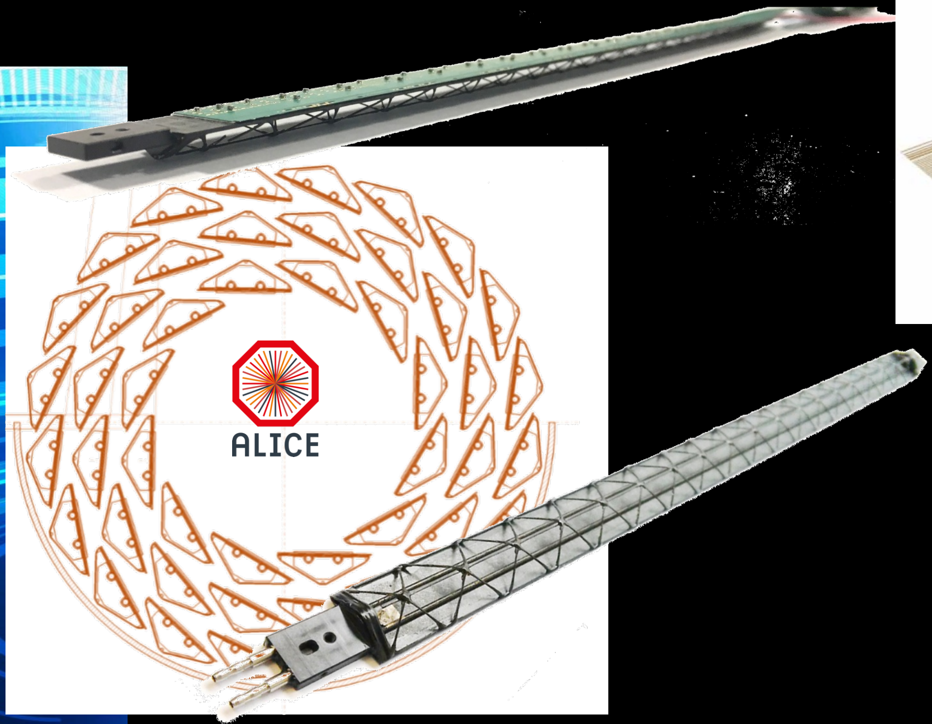
MATERIAL REDUCTION

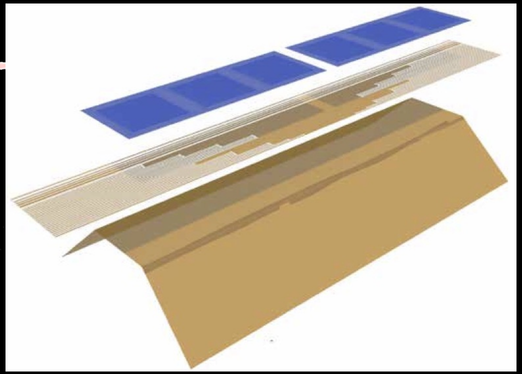
UNIVERSITY OF OXFORD

ATLAS ITK module support structure with copper-Kapton co-cured tape and embedded CO2 cooling (1.4 m Long)



- Non conventional use of Carbon Fibre Reinforced Plastic (CFRP) materials for Vertex Detectors to match the requirement of minimum material budget, high rigidity, thermal management.



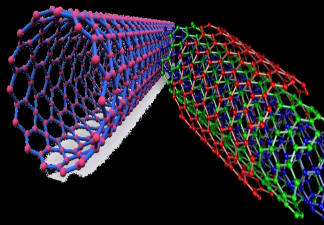


- 50 µm DMAPS
- 25 µm Kapton Flexprint
- 50 µm Kapton support frame
- < 1‰ Radiation length

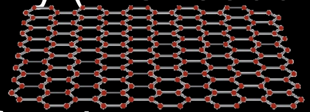
Carbon Nanotubes

Allotrope of carbon with a cylindrical nanostructure

Very high Therma Conductivity (TC=3500 W/mK)



Graphene



One atomic-layer thin film of carbon atoms in honeycomb lattice. Graphene shows outstanding thermal performance, the intrinsic TC of a single layer is 3000-5000 W/mK