Silicon Detector Technologies for the IDEA Tracker

2nd ECFA Workshop on e^+e^- Higgs/Electroweak/Top Factories
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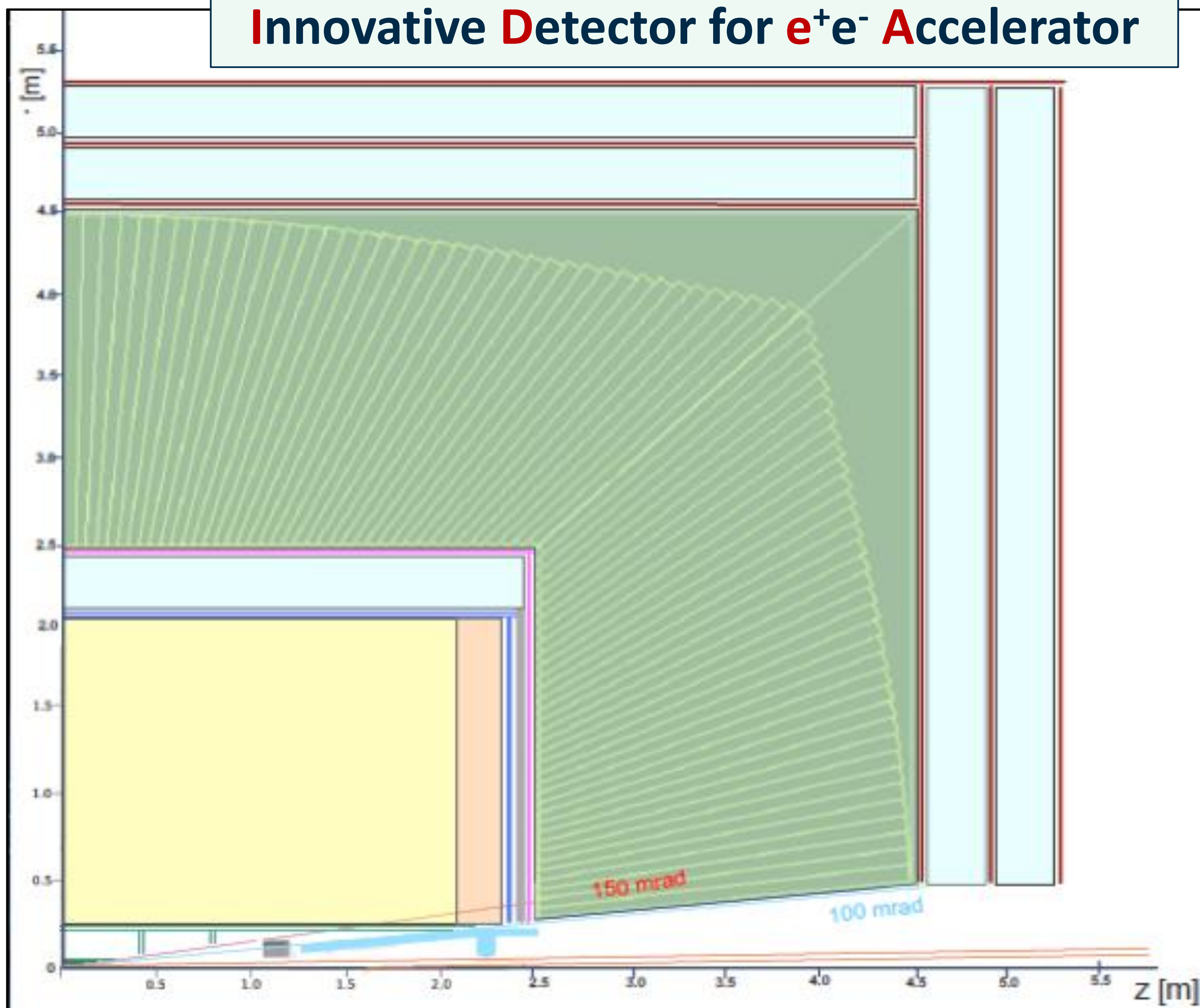
For the RD_FCC Silicon Tracker community

(COMO, GENOVA, MILANO, PADOVA, PERUGIA, PISA, TORINO)

UNIVERSITÀ DEGLI STUDI DI MILANO
DIPARTIMENTO DI FISICA

The IDEA Concept



- Central tracking device:
  - light Drift CHamber

P. M. Procacci and W. Elmetanawee's talks

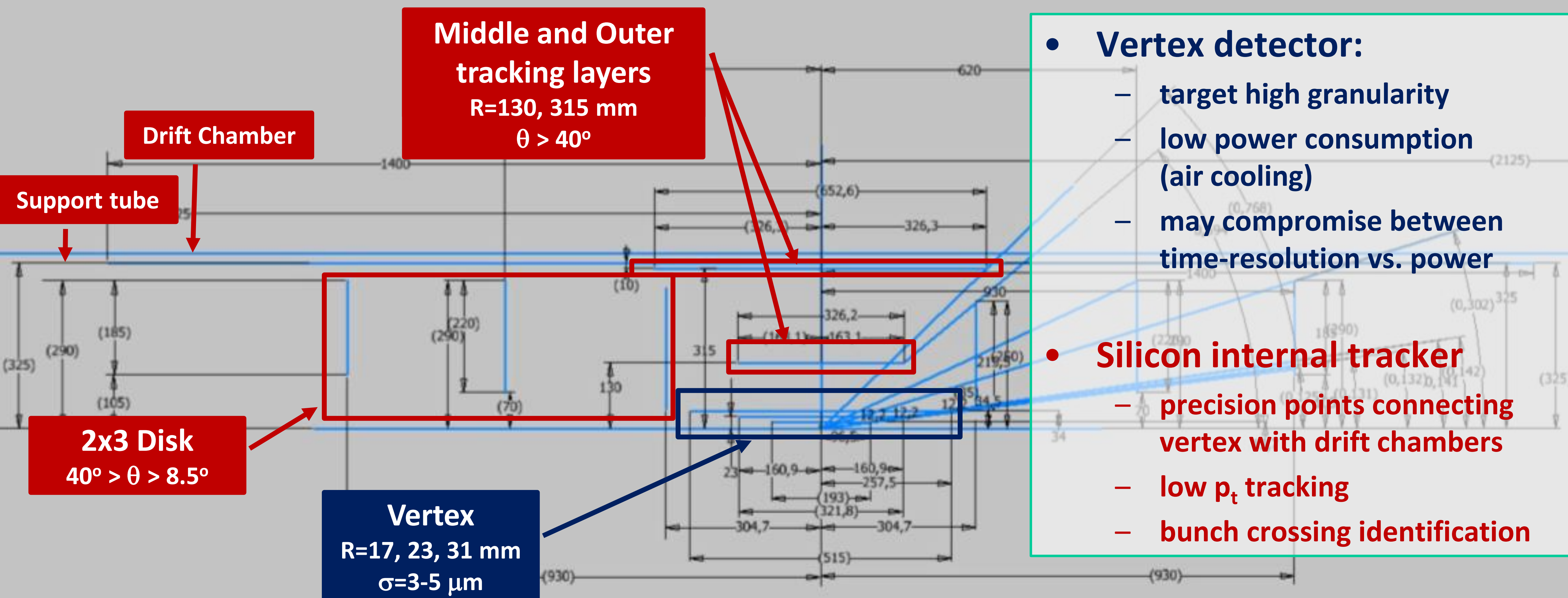
- **Silicon detectors for precision measurements**
  - **vertex detector**
  - **silicon internal tracker**
  - **silicon wrapper/TOF**
- Thin solenoid with 2T field (according to MDI limits)
- Dual readout calorimeter
  - supplemented by a pre-shower detector

G. Polesello's talk

- Muon chambers in the solenoid return yoke

G. Morello's talks

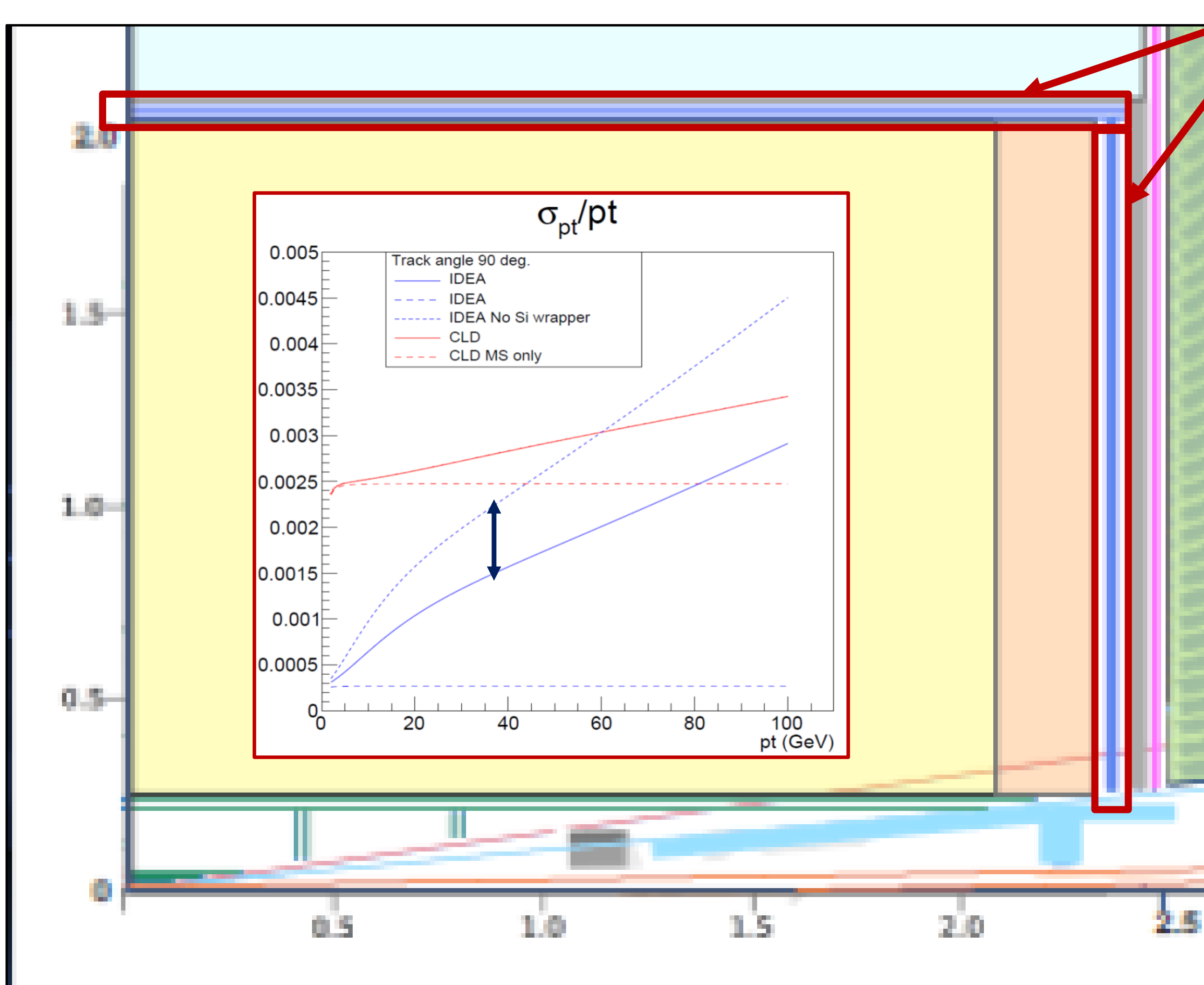
The IDEA Concept: inner tracking



- **Vertex detector:**
  - target high granularity
  - low power consumption (air cooling)
  - may compromise between time-resolution vs. power
- **Silicon internal tracker**
  - precision points connecting vertex with drift chambers
  - low p_t tracking
  - bunch crossing identification

More details in F. Palla's talk

The IDEA Concept: Si Wrapper



- **Precision silicon layer around the central tracker**
  - **improve momentum resolution**
  - **extend tracking coverage in the forward/backward region** by providing an additional point to particles with few measurements in the drift chamber
  - precise and stable ruler for acceptance definition
  - *it may provide TOF measurement*

- Covered area ~90 m^2
  - important impact on services
  - technology suitable for large size production

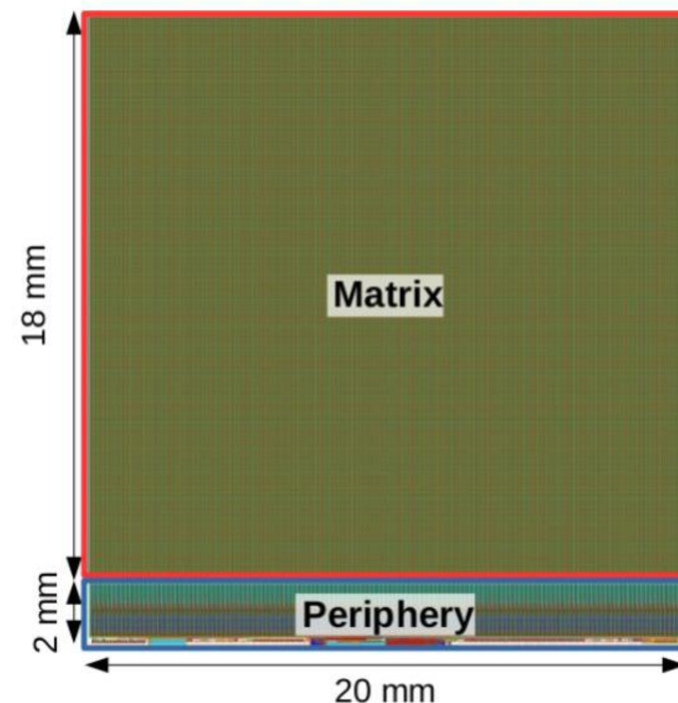
Si Detector Technologies

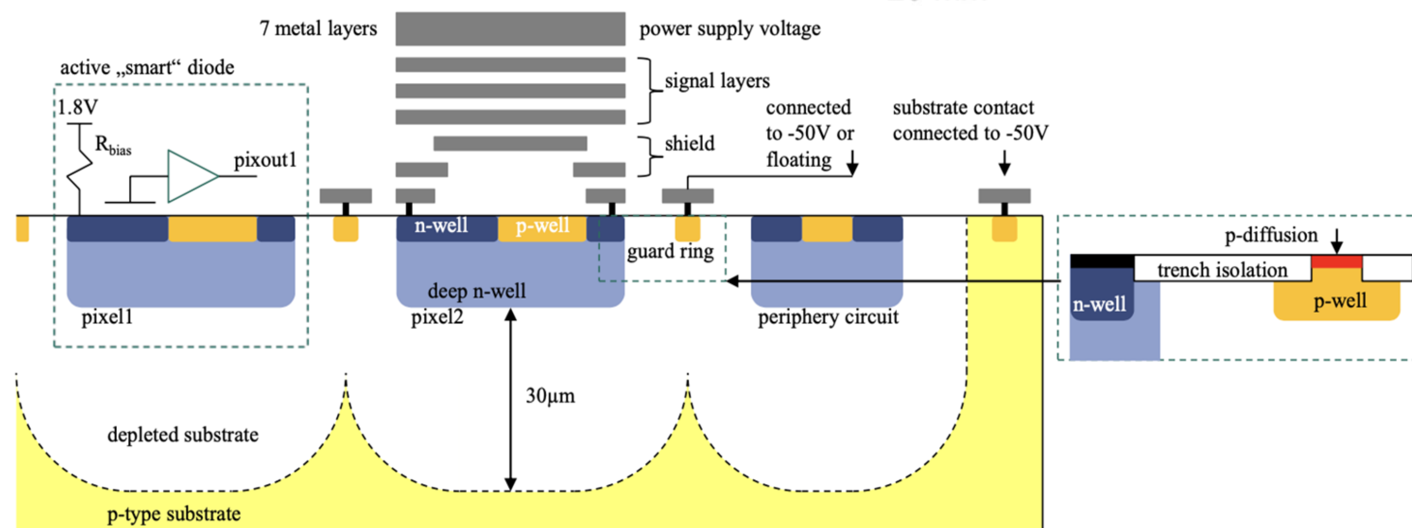
- Focus on **depleted monolithic CMOS detectors**
  - High-Voltage/High-Resistivity CMOS processes commercially available
  - CMOS Foundries are able to produce large volume of detectors at a convenient price
  - Depeleted region provide fast rising and "high-amplitude" signals
  - No need of the complex and costly interconnection technique used in hybrid detectors
- Two technologies presented in this talk:
  - **ATLASPIX3** – KIT, China, INFN, UK collaboration
    - full reticle size detector, implementing most features needed for deployment in the **Internal Tracker and Si Wrapper**
  - **ARCADIA** – INFN/LFoundry driven development, collaborations with PSI
    - fully depleted sensors, with high granularity and low power consumption for the **Vertex Detector**

- **Resistive Silicon Detectors**, with **tens of ps time resolution** are considered as an opportunity for the Silicon Wrapper
(showing results from Torino, Trento, Perugia and FBK collaboration)

ATLASPIX3 Detector

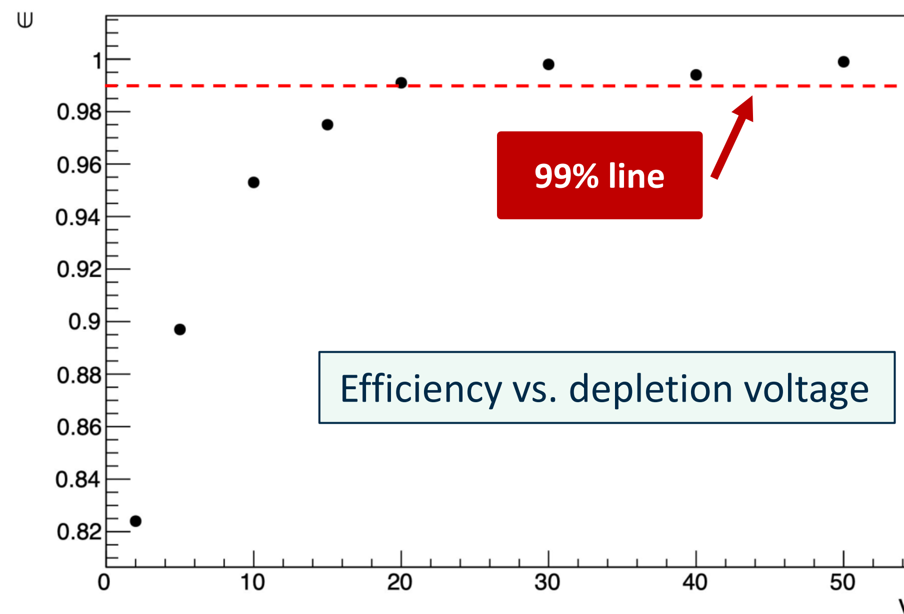
- **ATLASPIX3 general features**
  - **TSI 180 nm HVCMOS** technology
  - full-reticle size **20×21 mm²** monolithic pixel sensor
  - 200 Ωcm substrate (other substrates up to 2 kΩcm also possible)
  - **132 columns of 372 pixels**
  - **pixel size 50×150 μm²** (25×150 μm² on recent prototypes)
  - **breakdown voltage ～-60 V**
  - up to **1.28 Gbps downlink**
  - **25 ns timestamping**
  - analog pixel matrix, digital processing in periphery
- Both **triggerless** and **triggered** readout modes:
  - two End of Column buffers
  - 372 hit buffers for triggerless readout
  - 80 trigger buffers for triggered readout

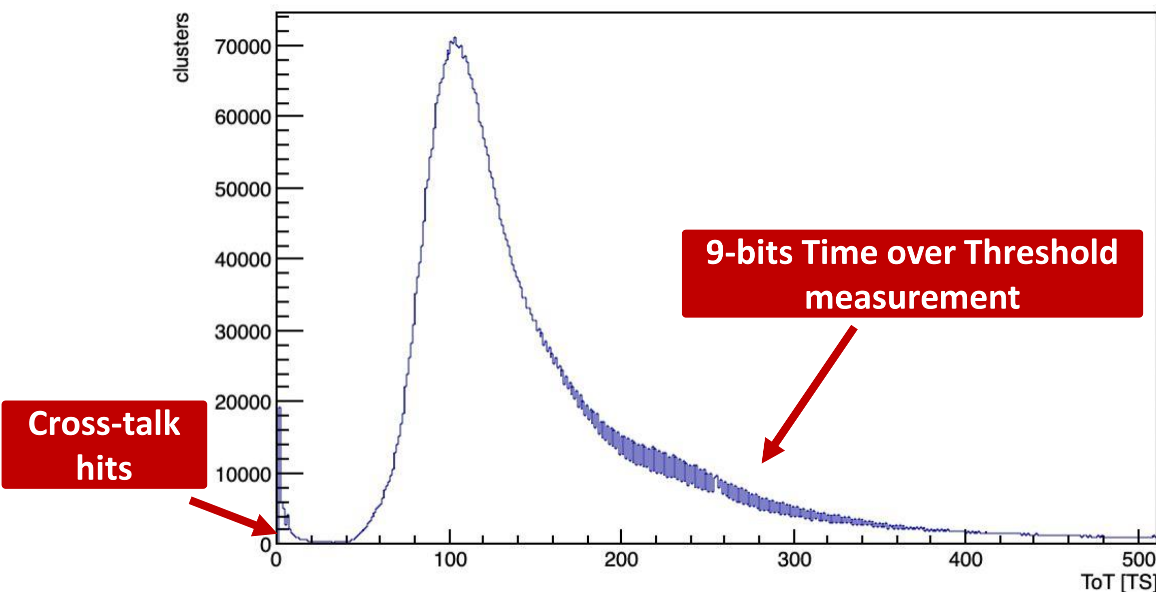


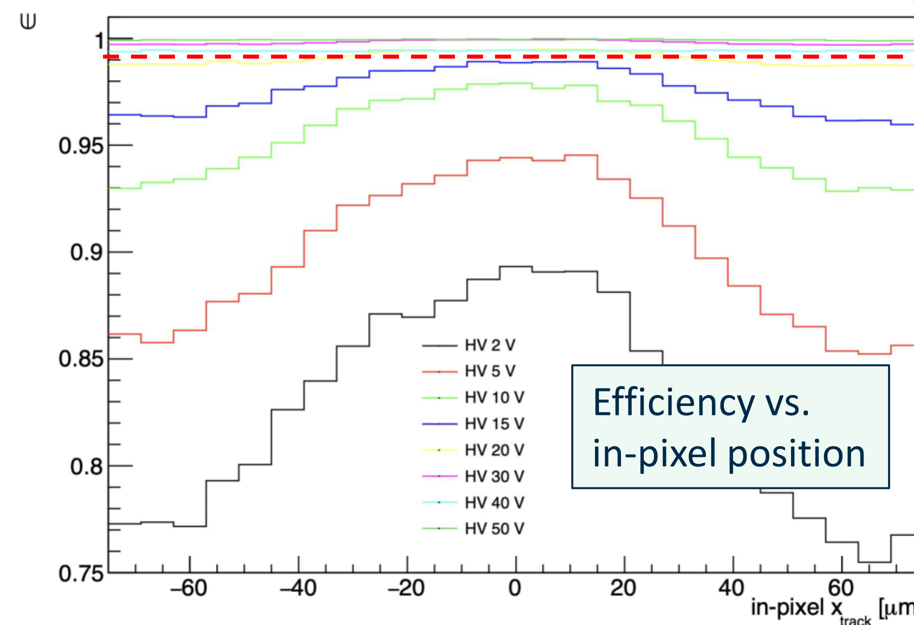


ATLASPIX3: Testbeam performance

- Telescope of 4 ATLASPIX3 single chips in DESY electron beam
- **Cross-talk** between pixels due to the capacitive coupling of the transmission lines between the matrix and the end-of-column logic is limited to **~1% of total hits**
- **Efficiency < 99%** and **uniform in the detector** for depletion voltages >20 V
- **Position resolution** in the **10-11 μm** range

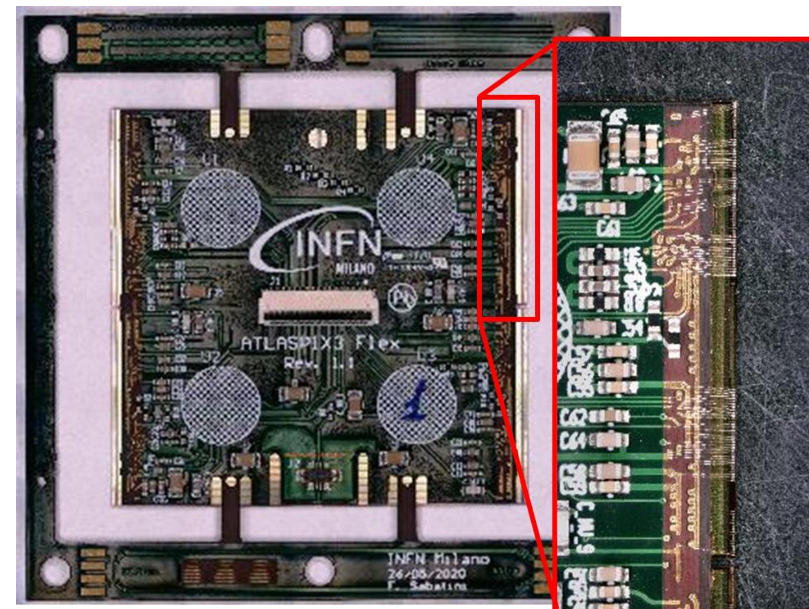


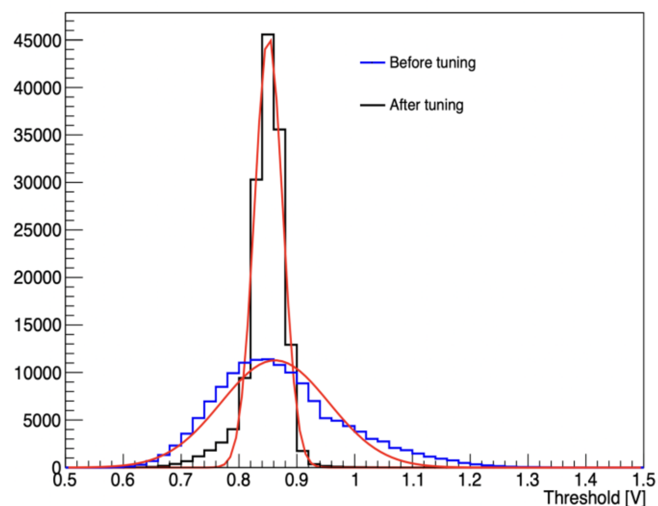


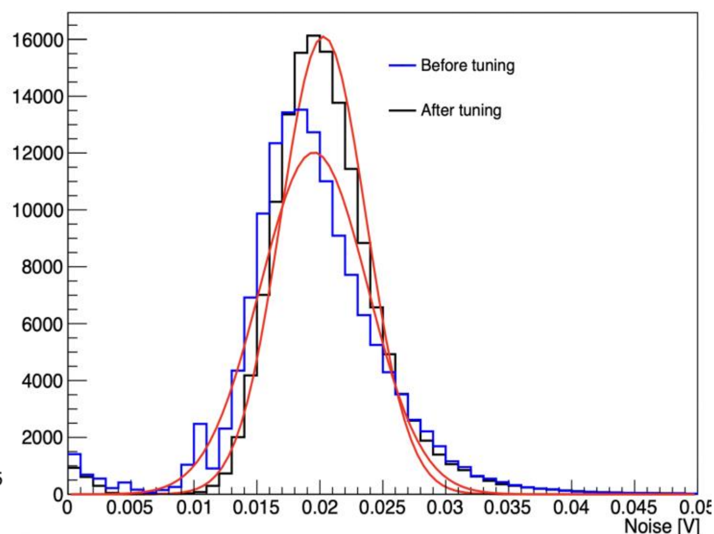


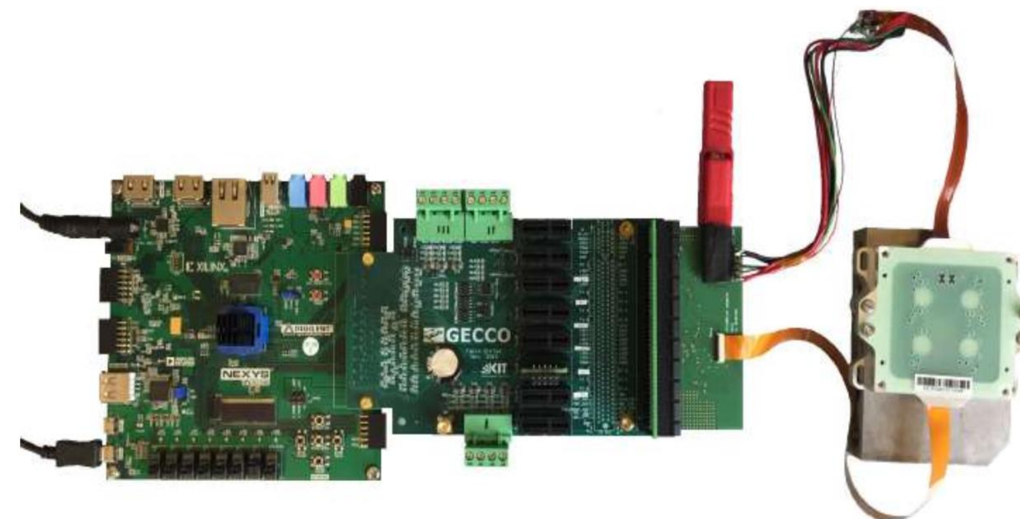
ATLASPIX3: Multi-chip module

- **Multi-chip** module **assembly**
  - aggregates electrical services and connection for multiple sensors
  - **quad module**, inspired by ITk pixels
  - building block for staves and disks
- No interference observed in the simultaneous operation of multiple chips
  - threshold tuning and noise performance same as individual chip characterization
  - testbeam and X-ray tube data



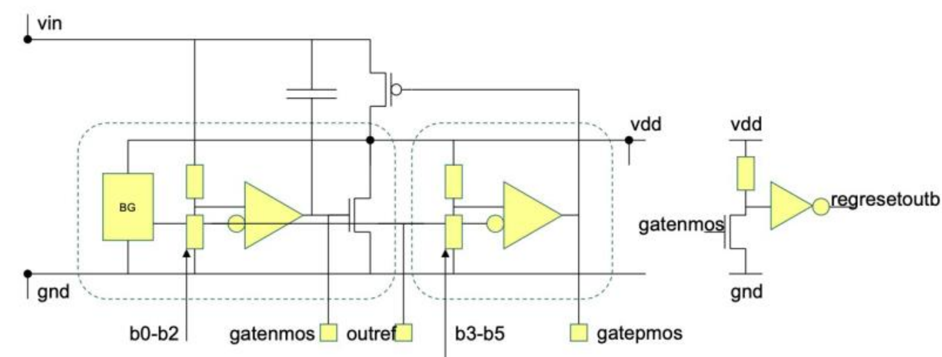


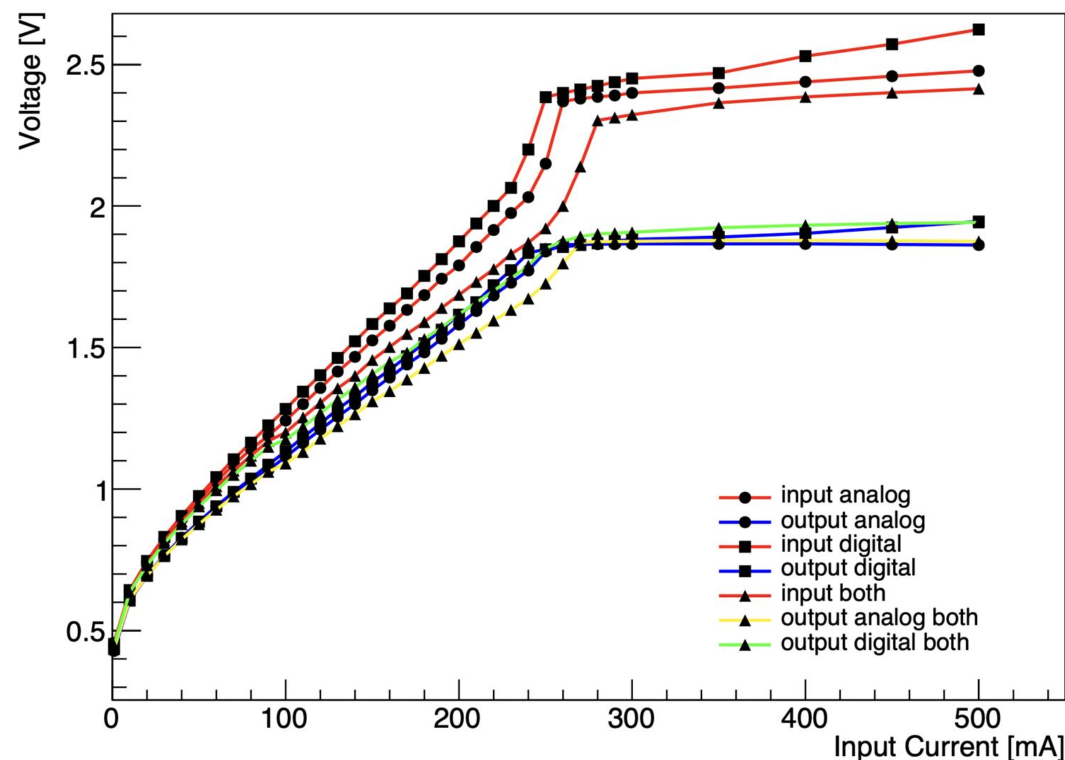




ATLASPIX3: Serial powering

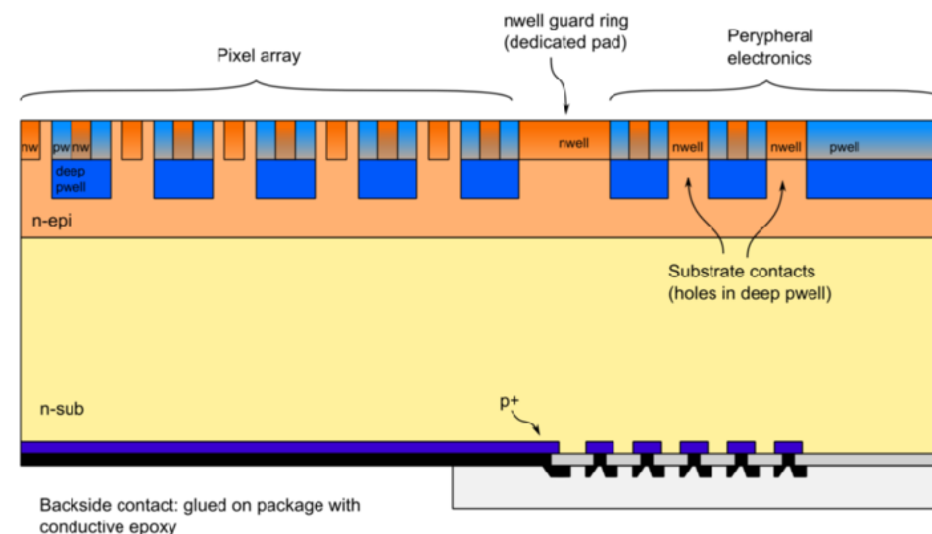
- Version ATLASPIX3.1 can be biased by serial powering through two shunt/low dropout regulators
  - digital and analog (VDDD/A)
  - 3 bits to tune threshold of shunt regulator
  - 3 bits to tune VDD
- Measured regulator performance
  - threshold and noise performance are the same usinfg SLDO or direct VDDD/A powering
  - DAC dinamic range of few tens of mV
  - Full chip turn-on at I=300 mA
  - Input voltage 2.3 V
  - Power consumption: ~700 mW/chip or ~175 mW/cm^2
- Integration model is to join modules by a bus implementing a serial powering chain
  - examples in F. Palla's talk
  - metal in the module hybrid and the power bus dominates the thickness of a detector layer (~0.44% X_0)
  - considering to move Al as conductor for PCBs





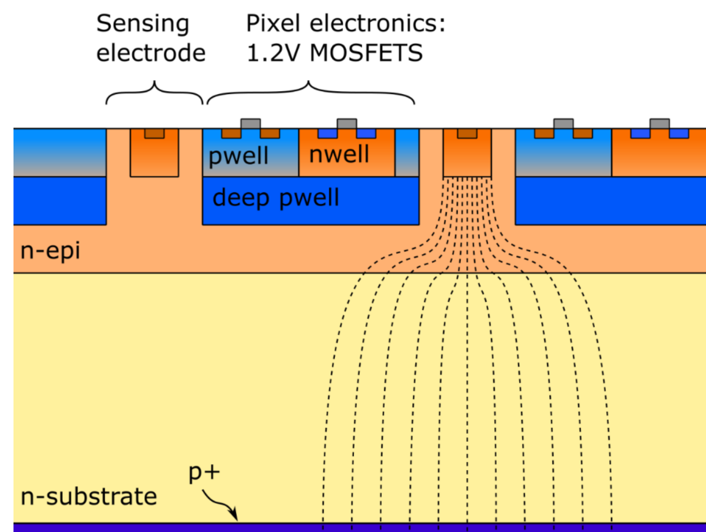
ARCADIA

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays



Fully Depleted Monolithic Active Pixel CMOS sensor technology platform allowing for:

- Active sensor thickness in the range 50 µm to 500 µm;
- Operation in **full depletion** with fast charge collection by drift
- **Small collecting electrode** for optimal signal-to-noise ratio;
- Scalable readout architecture with ultra-low power capability O(**10 mW/cm²**);
- Compatibility with standard CMOS fabrication processes: concept study with small-scale test structure (SEED), technology demonstration with large area sensors (ARCADIA)
- Technology: **LF11is** 110nm CMOS node (quad-well, both PMOS and NMOS), high-resistivity bulk
- Custom patterned backside, patented process developed in collaboration with LFoundry



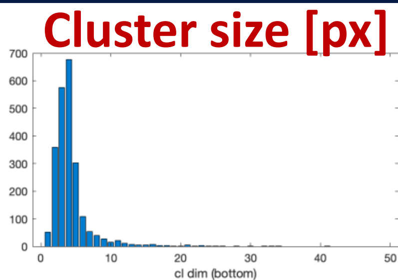
ARCADIA: MD3 demonstrator

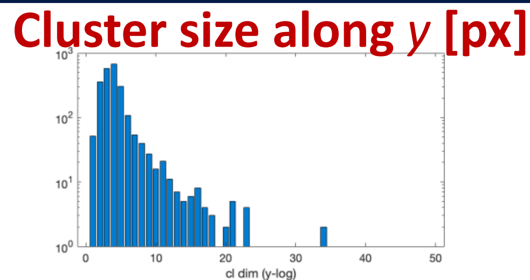
- Demonstrator layout:
  - **Top Padframe** Auxiliary supply, IR Drop Measure
  - **Matrix**
    - 512x512 pixels, Double Column arrangement
    - 25x25 μm^2 pixels
    - Clockless
  - **End of Sector (x16)** Reads and Configures 512x32 pixels
  - **Sector Biasing (x16)** Generates I/V biases for 512x32 pixels
  - **Periphery**
    - SPI, Configuration, 8b10b enc, Serializers
    - Triggerless data-driven readout
    - Event rate up to 100 MHz/cm^2
    - High-rate operation (16 Tx): 17-30 mW/cm^2
    - Low-power operation (1 Tx): 10 mW/cm^2
  - **Bottom Padframe** Stacked Power and Signal pads

ARCADIA: MD3 Results with cosmics

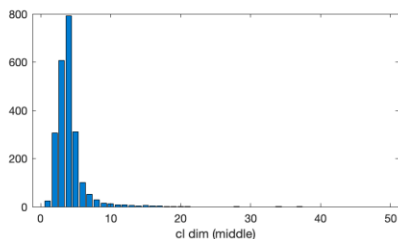
Cluster size [px] | Cluster size along *y* [px]

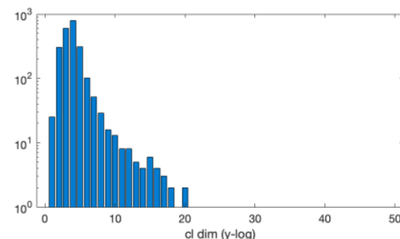
Bottom layer



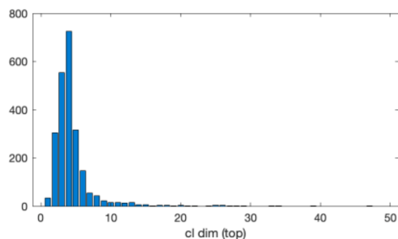


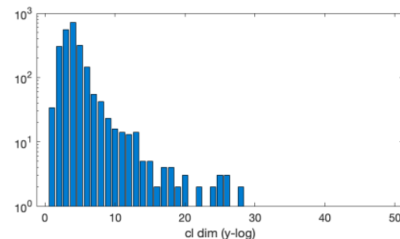
Middle layer

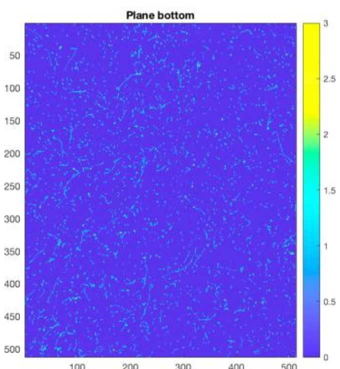


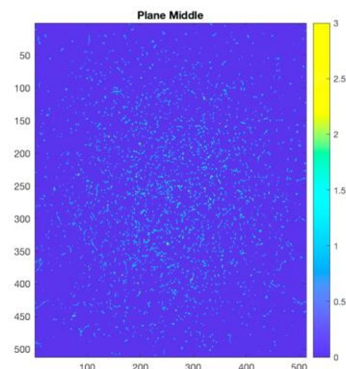


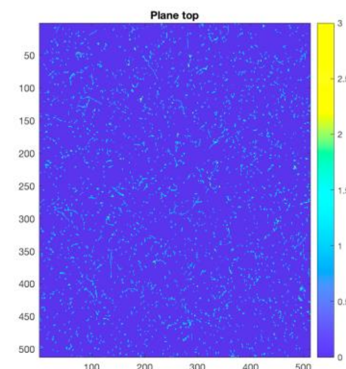
Top layer



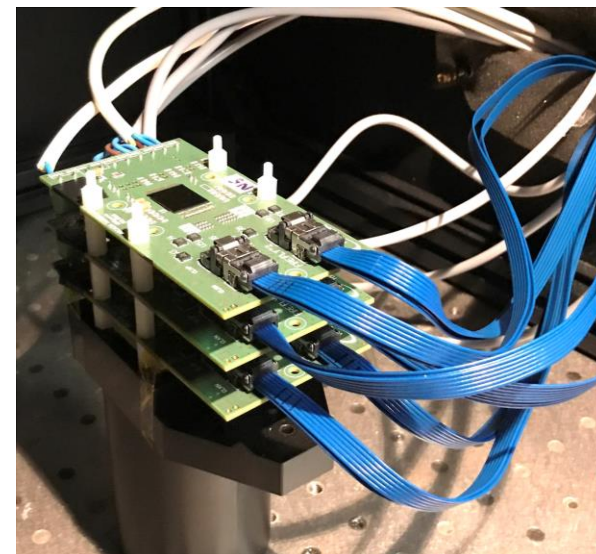






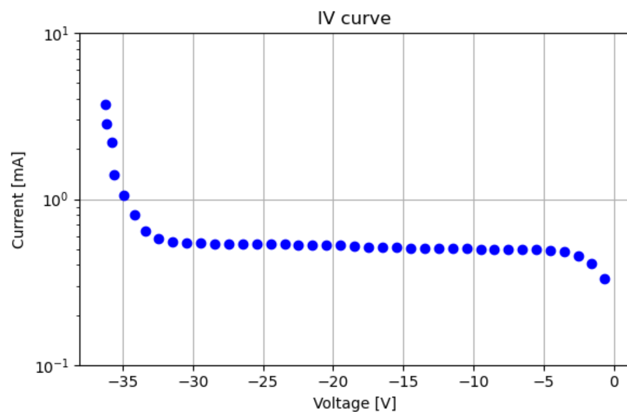


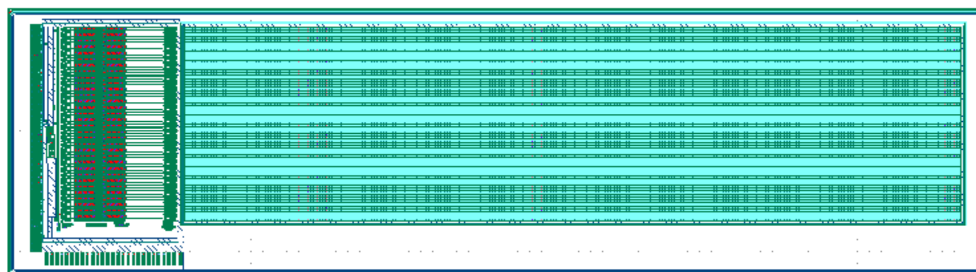
- Cosmic ray data taking: 1 week
- 3-plane MD3 installed on a black box
- Threshold 290 e-, MPV = 4 pixels
- More than 90% of clusters with less than 6 fired pixels
- Preliminary results on residuals show a standard deviation of 12-14 μm (multiple scattering...)

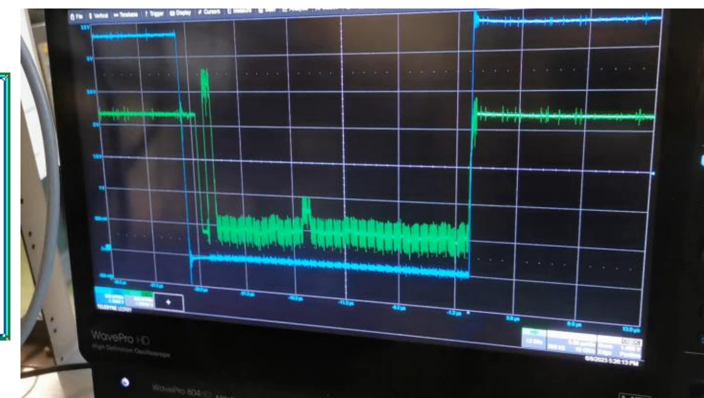


ARCADIA: Additional R&D of interest

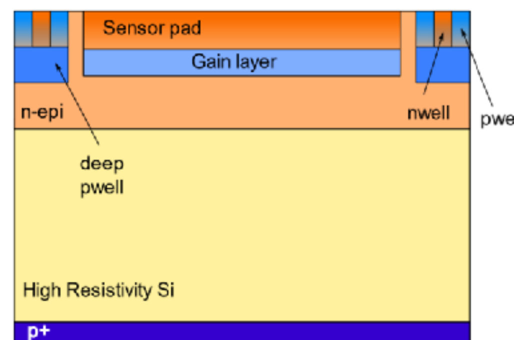
- **Monolithic microstrips**

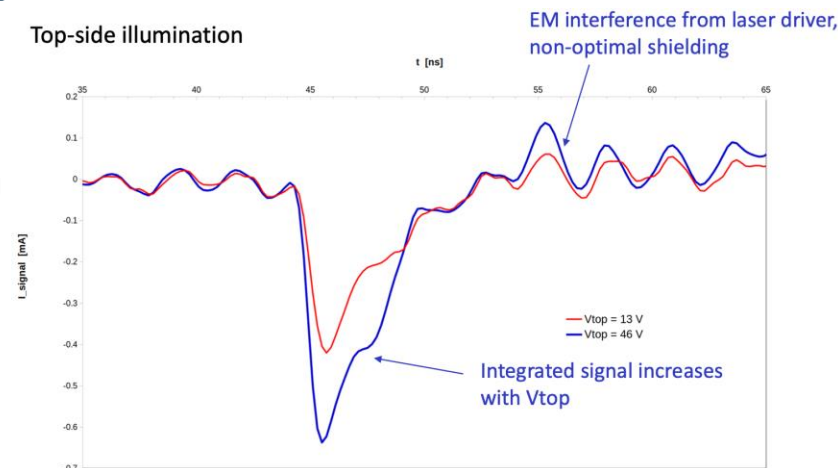






- **Gain layer for timing development**
  - 50 µm active thickness, different gain dose splits: gain target range 10 - 30
  - first 200 µm (BSI) devices powered on, C-V curve suggest that the gain layer is present
  - 50 µm devices just received from dicing, tests starting soon
  - though with n-type substrate the profile can not be completely evaluated

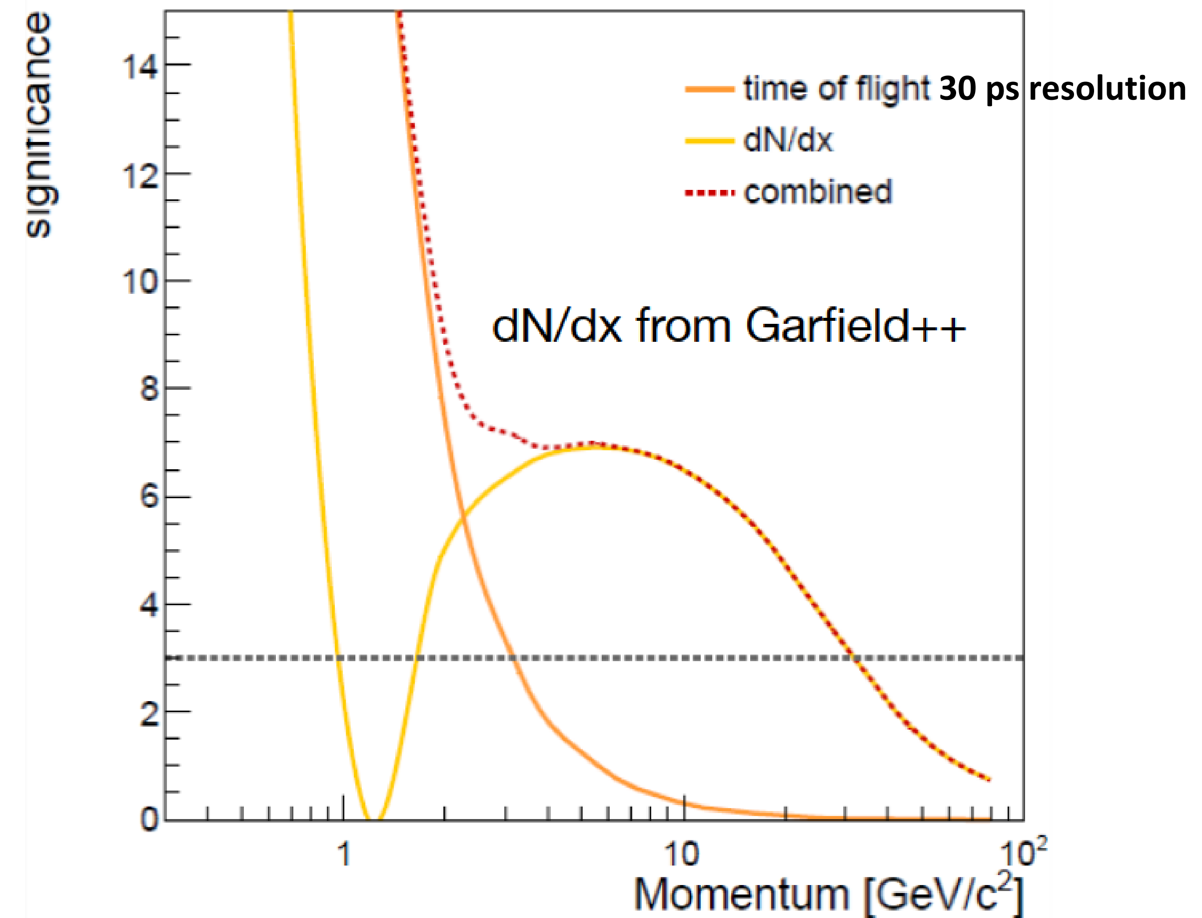




TOF measurement in Si Wrapper

- Particle IDentification is essential for many physics measurements
- Needed on a wide momentum range
  - $B_s^0 \rightarrow D_s K$ has K up to 30 GeV/c
  - K for flavour tagging in $b \rightarrow c \rightarrow s$ decay chains are pretty soft
  - useful in tau physics for Vus measurements in $\tau \rightarrow K\nu$

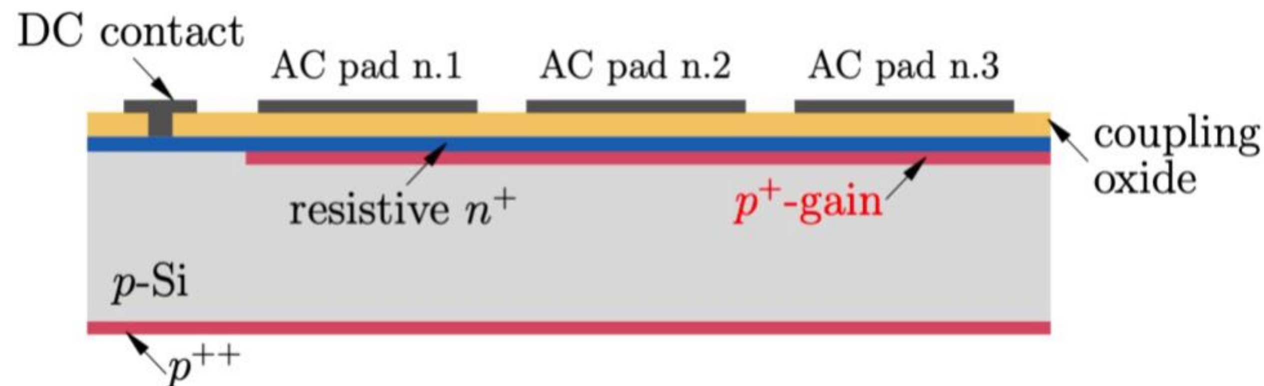
- **dN/dx** measurements in Drift Chamber provides 3σ separation up to 30 GeV/c
- Confusion region about 1 GeV/c can be covered by **TOF** measurement with resolution **<100 ps**

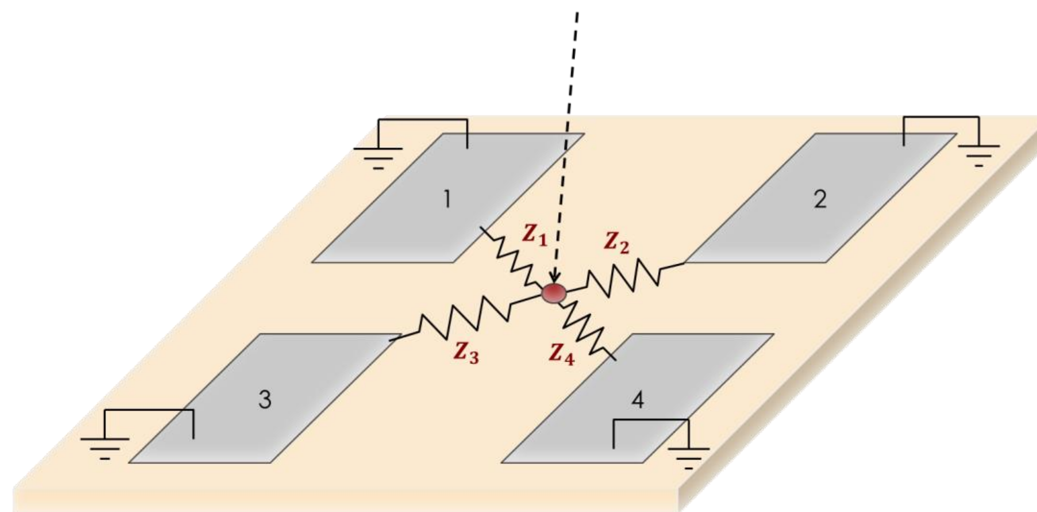


Can it be implemented in the Si Wrapper without compromising the spatial resolution?

Resistive Silicon Detectors (RSD)

- LGAD detector with **continuous gain layer**
- Charge collection through **resistive n-layer**
- Readout by induction on **AC coupled pads**
- Fully active detector
  - avoids inefficient regions due to the insulation between pixels needed in LGAD sensors
- Charge sharing defined by the relative impedance of the path between the charge deposition and readout electrodes
  - pad pitch >> lateral dimension of charge deposit
  - sharing is deterministic (in low pitch pixel detectors is dominated by Landau fluctutations)
  - resolution depends on the S/N ratio of the readout electronics

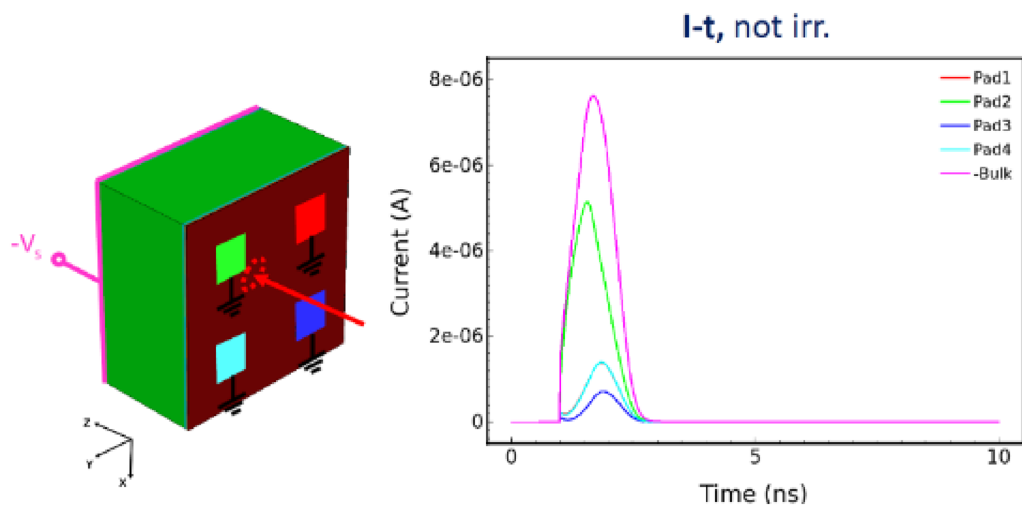




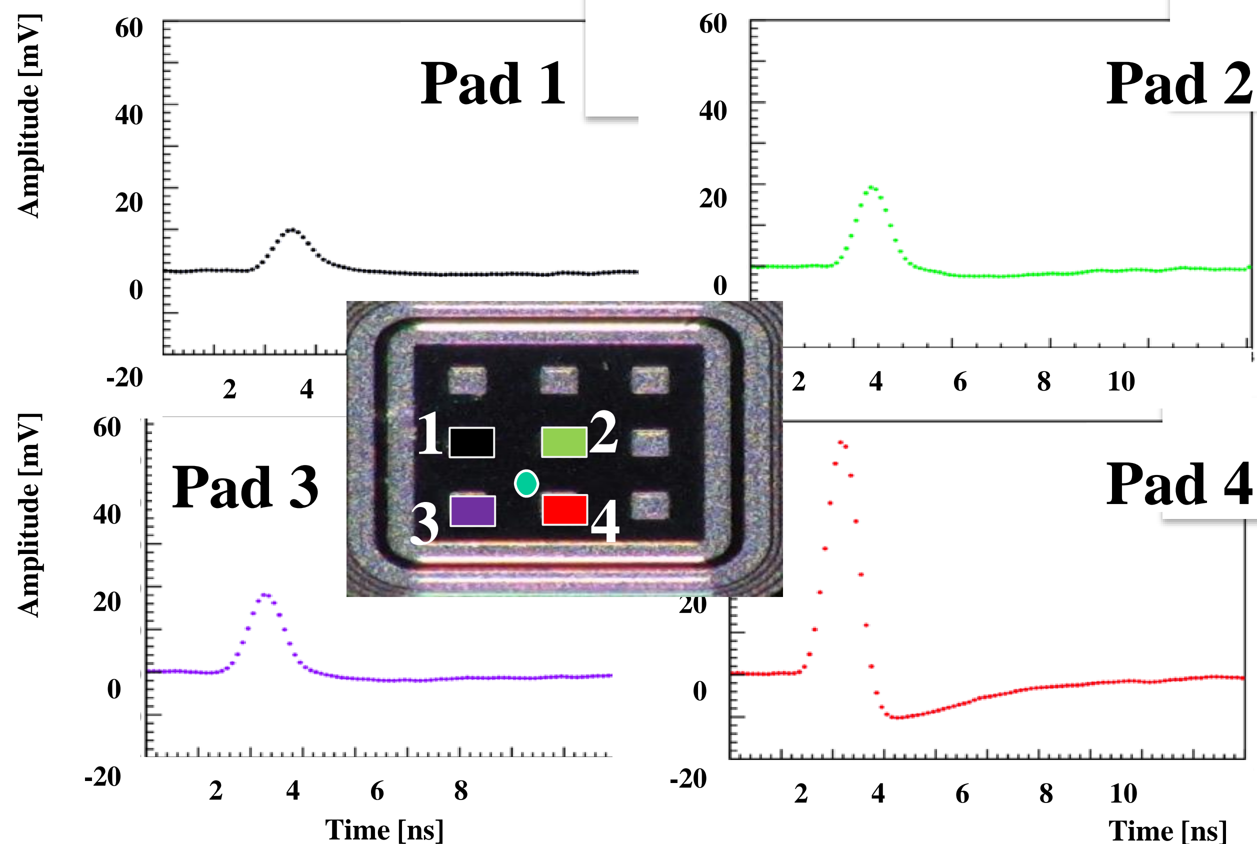
$$S_i = \frac{1/Z_i}{\sum 1/Z_i}$$

RSD: Signal sharing example

TCAD Simulation model...

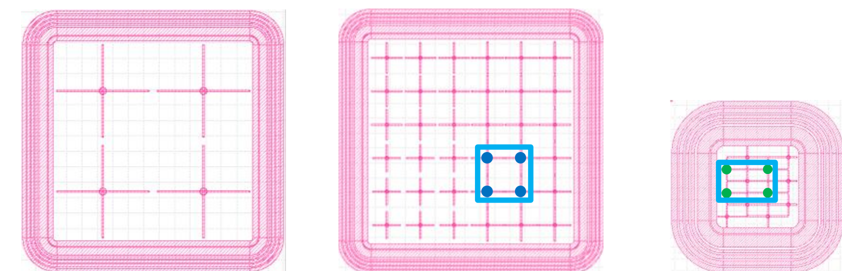


...and reality



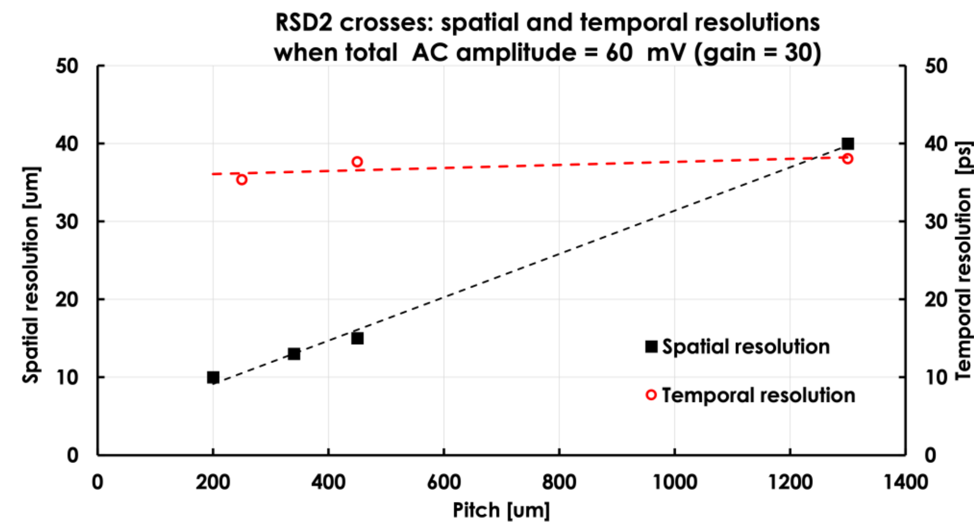
RSD: Prototype performance

- Spatial resolution << pixel pitch
  - 10 μm achieved in lab tests with 200 μm pixel pitch
  - more space in readout pixel cell to implement precision TDC
- Timing resolution about independent from pixel pitch
- Drawbacks:
  - hybrid detector (but bump-bond pitch is easily achievable commercially)
  - effective pitch is >2 readout pitch: particle flux limited by pixel size
- Suited for Si Wrapper:
  - particle density at 2 m from the interaction region should not be a concern for a e^+e^- colliders
  - no need to push for extremely low material: hybrid detector are acceptable



1.3 × 1.3 mm^2 450 × 450 μm^2 200 × 340 μm^2

Cross-shaped electrodes



Summary and outlook

- The IDEA tracker layout poses different challenges for the different silicon trackers:
  - Extremely high resolution and low-mass are needed for the vertex detectors
  - System issues are the focus topics for the large area detectors
  - Depleted Monolithic CMOS pixel detectors are a cost-effective and high-performance solution
- **ATLASPIX3** (AMS/TSI 180 nm) is a well-developed full-size sensor:
  - Already a possible solution for the bulk of the detector silicon area
  - It is used to investigate integration and system issues
- **ARCADIA** (LF 110 nm) provides a global platform for fully-depleted CMOS sensors
  - The sensitive area has been developed and detector performance appears very promising
  - Fine granularity and low power make it suitable for the vertex trackers
  - Periphery needs to implement trigger logic, command decoder, 1.28 Gbps serializers
- **Resistive Silicon Detectors** are an extremely interesting option for the Silicon Wrapper:
  - Micrometric spatial resolution even with coarse granularity: reduced number of channels
  - Provide a TOF layer supplementing the drift chamber particle ID

- Plenty of **fascinating electronic design and sensor development** will be needed to arrive to build a state-of-art detector within the time scale of future e^+e^- factories

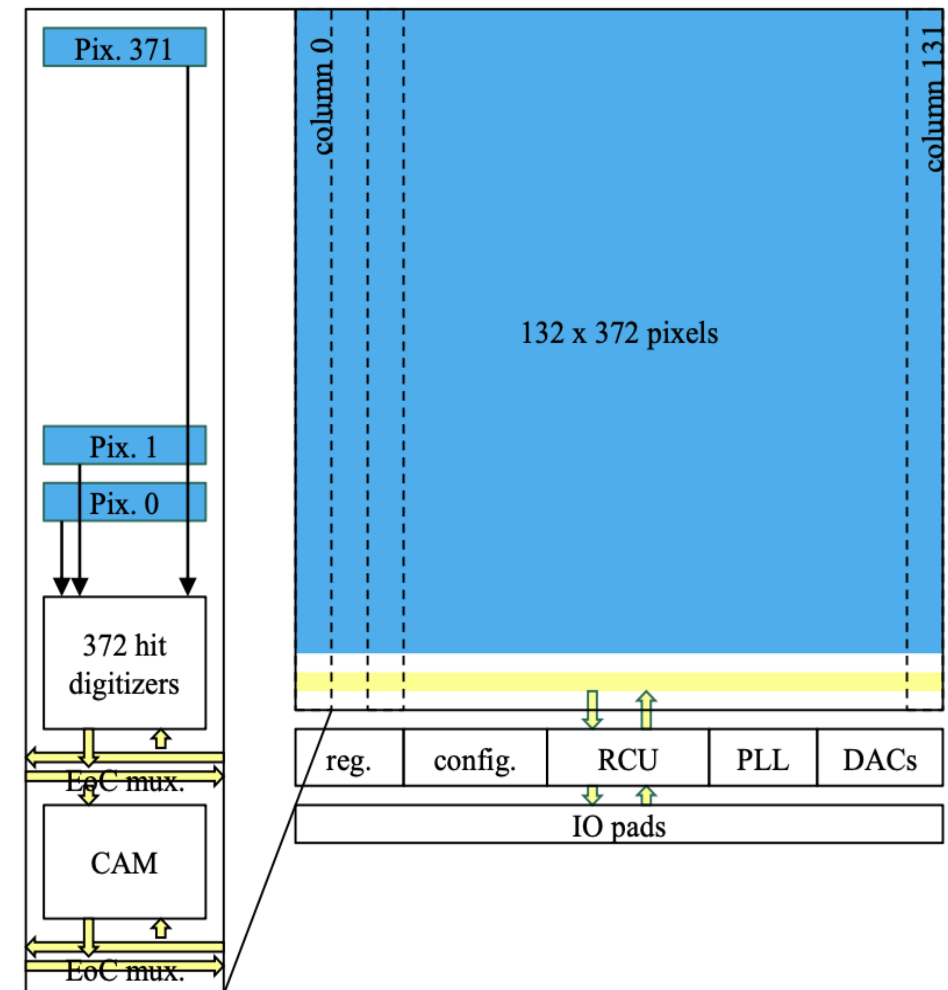
BACKUP

Studio del serial powering

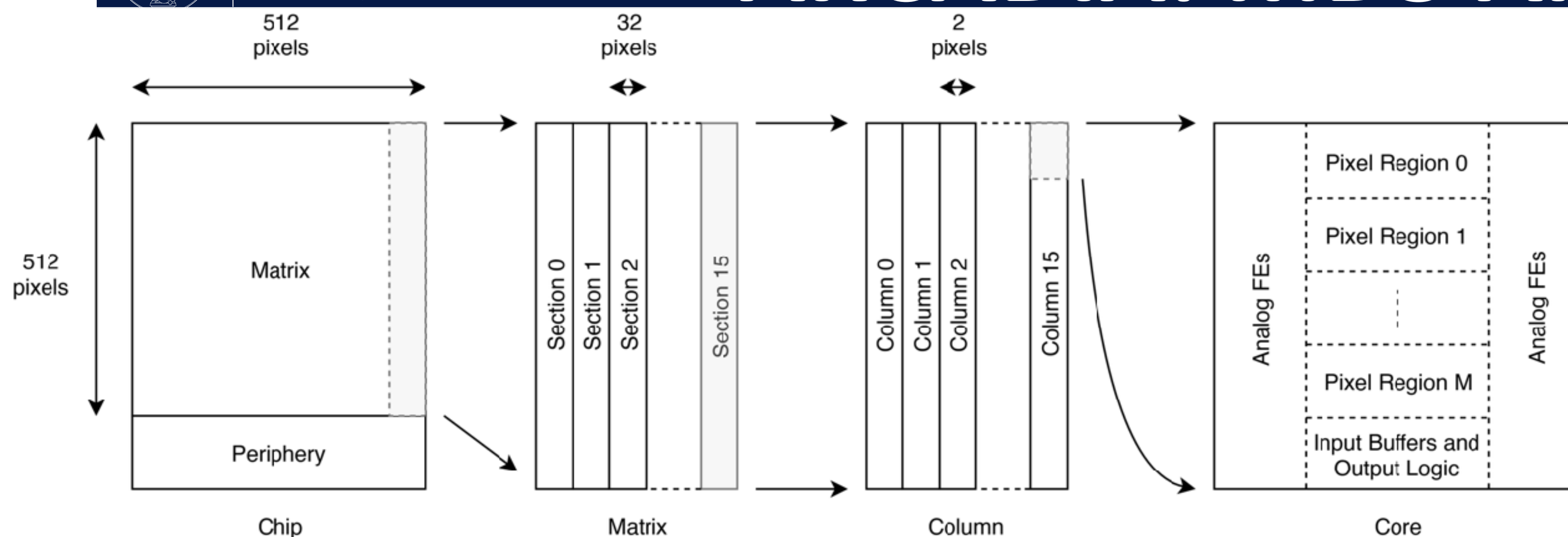
- Il serial powering è un argomento poco studiato nella comunità dei monolitici:
  - Enfasi sul vertex, sistema di dimensioni limitate, che non necessità di tale tecnologia, che è invece di interesse per grandi superfici e stave lunghe
  - È applicabile solo alle tecnologie HV (come TSI 180nm, LF 110nm)
    - Per esempio TPSCo 65nm, spinta dal CERN sarebbe limitata a catene di poche unità di moduli
  - Può quindi essere un **discriminante** "pratico" **nella scelta della tecnologia per i tracciatori esterni**
  - È necessario capire i requisiti sulla "*tunability*" e sull'*uniformità* dei regolatori SLDO e **motivare i progettisti ad inserirli nei prototipi** (al momento ATLASPIX3 dovrebbe essere l'unico chip DMAPS ad implementare SLDO)
  - N.B.: la dimostrazione del serial powering non necessità di un bus
- Il bus in alluminio rappresenta uno step rilevante nella riduzione del materiale in un sistema
  - I servizi elettrici sono il contributo maggiore allo spessore in X_0 della stave
  - È utile esplorare questa tecnologia ed un bus è un circuito relativamente semplice sui cui fare pratica e misurare parametri di base (attenuazione del segnale, dissipazione...)
  - Funzionale alla realizzazione di un dimostratore con alcuni moduli montati su cold plate
  - Passo intermedio verso la realizzazione di ibridi più complessi (come quello del modulo quad)

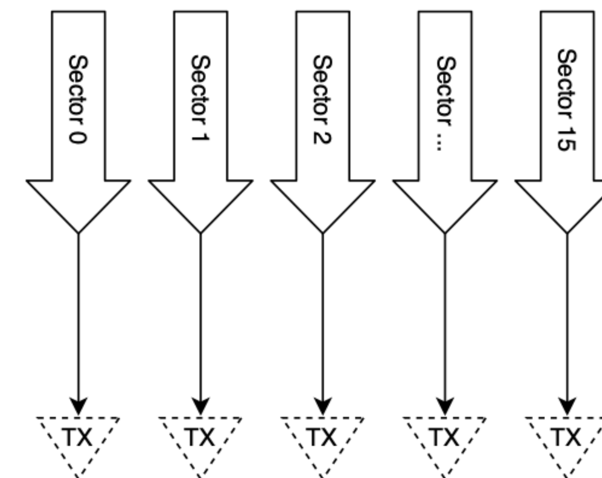
ATLASPIX3 Readout Architecture

- **Chip architecture**
  - organized in 132 columns, each with:
    - 372 pixels
    - **372 hit digitizers** (HDs)
    - **80 content addressable memory cells** (CAM)
    - **two end-of-column multiplexers** (EoC mux)
  - **digital part** (HDs, CAM, EoCs) in **chip periphery**, separated from analog pixels electronic (CSA and comparator)
  - chip periphery also contains the readout control unit (RCU), the clock generator, configuration registers, DACs, linear regulators and IO pads
  - **triggerless** and **triggered** readout
    - two EoCs
    - 372 hit buffers for triggerless RO
    - 80 trigger buffers for triggered RO

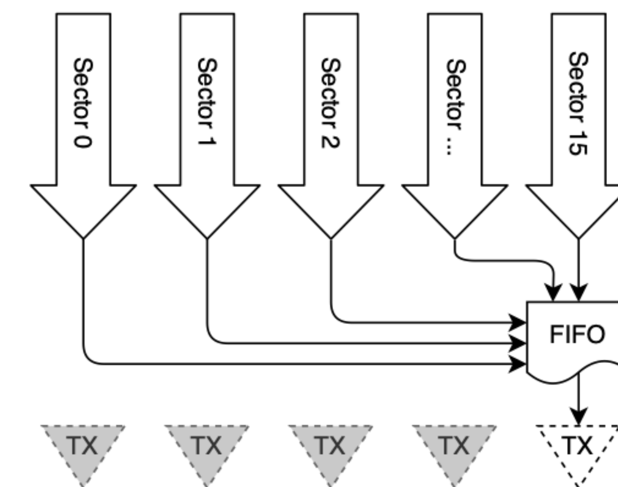


ARCADIA: MD3 Architecture





- Pixel size 25 µm x 25 µm, Matrix core 512 x 512, 1.28 x 1.28 cm silicon active area, "side-abuttable"
- Triggerless data-driven readout and low-power asynchronous architecture with clockless pixel matrix
- Event rate up to 100 MHz/cm^2 (post-layout simulations, to be demonstrated: test-beam in late 2023)
- Each sector has an independent readout and output link when operating in High Rate Mode
- Sector data is sent out (8b10b encoded) via dedicated 320MHz DDR Serialisers
- In Low Rate Mode, the first serialiser processes data from all the sections. The other serialisers and C-LVDS TXs(*) are powered off in order to reduce power consumption.



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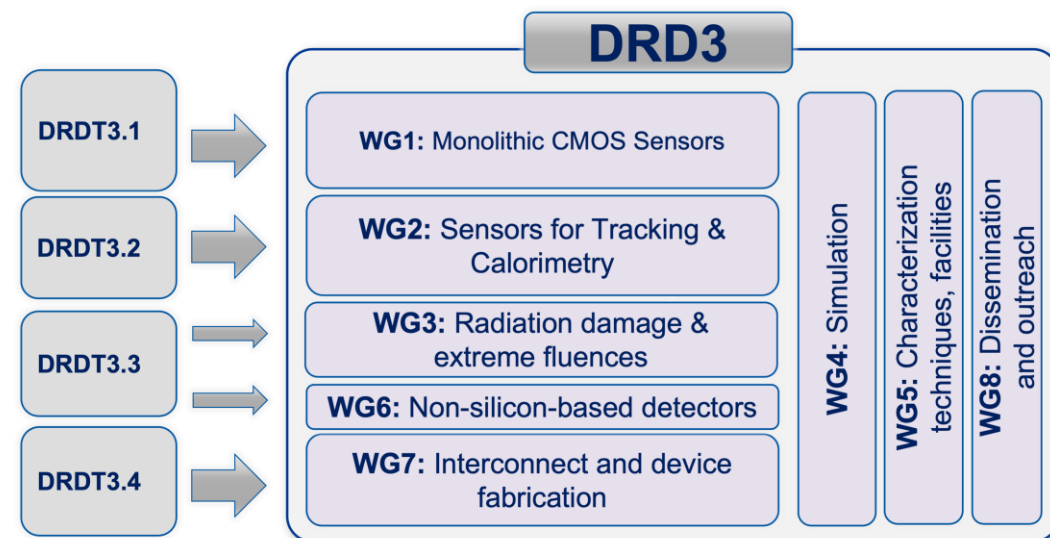
Participation to DRD3 and DRD7

- Circulated drafts of the DRD3 and DRD7 proposals
- Monolithic CMOS developments are shared between DRD3.1 (sensor development) and DRD7.6 (large systems)
  - TSI180 is within the technologies considered in DRD3.1
  - the LF110nm ARCADIA platform is one of the two technologies included in DRD7.6 together with TowerJazz 65nm
- Developments on power distribution are the subject of a DRD7.1 process
  - SLDO has not been much investigated for Monolithic CMOS detector (depends on HV capabilities)
- LGAD in RSD technology are considered for two research goals in DRD3.2



- **RG 2.3: LGAD Sensors with very high fill factor, and an excellent spatial and temporal resolution.**
  - 2024-2025: LGAD test structures of different technologies (TI-LGAD, iL-GAD, RSD, DJ-LGAD), matching existing read-out ASICs.
- **RG 2.4: LGAD sensors for Time of Flight applications**
  - 2024-2026: Production of LGAD (RSD) sensors with large size for Tracking/Time of Flight applications to demonstrate yield and doping homogeneity. Study of spatial and temporal resolutions as a function of the pixel size.
  - 2026-2028: Structures produced with vendors capable of large-area productions to demonstrate the industrialization of the process.

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Project 7.6.a	7.1.b
Common access to selected imaging technologies and IP blocks	Powering Next Generation Detector Systems
The successful deployment of monolithic sensors in the community demonstrates their enormous potential. Efficient and affordable access to these technologies and IP-blocks requires concentration of resources	Improve power efficiency of detector systems at reduced material budget while meeting ultra-high TID tolerance. Improve efficiency of serially powered systems using switching mode shunt elements.
The main deliverables are: the shared PDKs, the chips resluting from the submissions and their test results. Supported technologies are: Tower Jazz 180nm, TPSCo 65nm, LFoundry 110nm.	-GaN DC-DC Converter: conversion factor 10, 10A, 1MHz, efficiency 95%, -Resonant Converter: conversion factor 5, 500mA, 30MHz, efficiency 75 %, -3-level Buck Converter: conversion factor 5-2, 500mA, 30MHz, efficiency 75 % -Capless-LDO: 1.1-1.2Vin, 0.9Vout, 200mA -GaN DC-DC Current Source: 48/24Vin, 10A, 200W, 2 MHz -SLDO: 1.4-2Vin, 0.9-1.2Vout, 1A Iload, 1A Ishunt
CMOS sensors are considered for several types of detectors: calorimeters, trackers, etc. They require specific expertise in analog and digital IC design, device design and technology, and significant testing effort. The project is therefore transversal and multi-disciplinary.	Joint effort in power electronics, ASIC and PCB design, thermal management, EMC, reliability. Necessary for all particle detector systems.
CERN **FR:** IN2P3 (IPHC, CPPM) **IT:** INFN (Torino, Padova, Milano, Bologna, Perugia, Pavia, Pisa), Trento **NL:** NIKHEF **UK:** STFC **US**: SLAC, others TBC	**AT**: TU Graz **CERN** **DE**: FH Dortmund, RWTH Aachen **ES**: ITAINNOVA **IT**: UNI Udine **US**: TBC
16 FTE/y 500k/y	6.8 FTE/yr 135k/yr