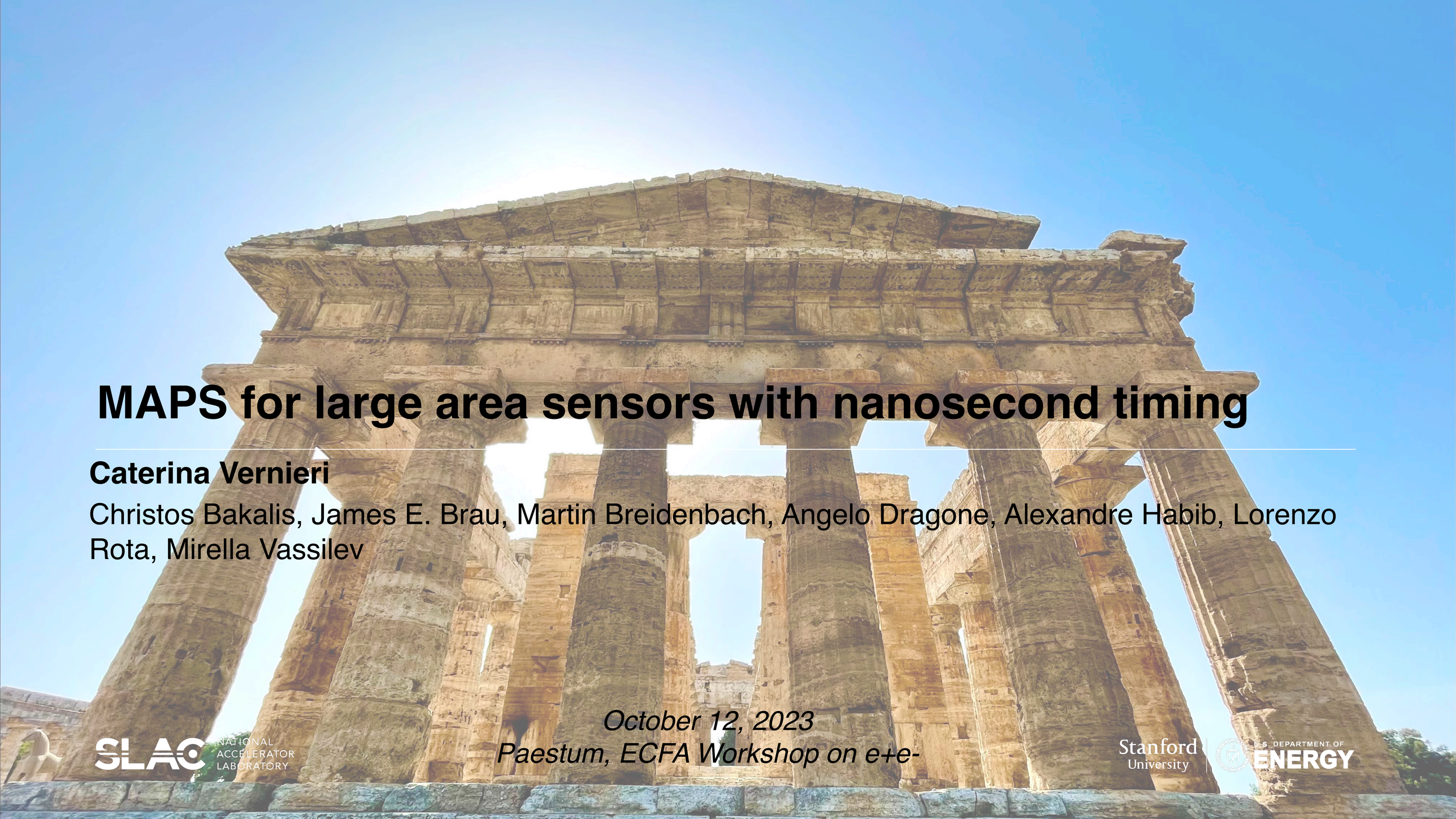


# MAPS for large area sensors with nanosecond timing

**Caterina Vernieri**

Christos Bakalis, James E. Brau, Martin Breidenbach, Angelo Dragone, Alexandre Habib, Lorenzo Rota, Mirella Vassilev

*October 12, 2023*
*Paestum, ECFA Workshop on e+e-*

SLAC NATIONAL ACCELERATOR LABORATORY

Stanford University

U.S. DEPARTMENT OF ENERGY

# Higgs physics as a driver for future detectors R&D

The goal of measuring Higgs properties with sub-% precision translates into ambitious requirements for detectors at e+e-

- Advancing HEP detectors to new regimes of sensitivity
- Building next-generation HEP detectors with novel materials & advanced techniques

| Initial state | Physics goal | Detector | Requirement |
|---|---|---|---|
| $e^+e^-$ | $hZZ$ sub-% | Tracker | $\sigma_{p_T}/p_T$=0.2% for $p_T < 100$ GeV<br>$\sigma_{p_T}/p_T^2 = 2 \cdot 10^{-5}/$ GeV for $p_T > 100$ GeV |
| | | Calorimeter | 4% particle flow jet resolution<br>EM cells 0.5×0.5 cm$^2$, HAD cells 1×1 cm$^2$<br>EM $\sigma_E/E = 10\%/\sqrt{E} \oplus 1\%$<br>shower timing resolution 10 ps |
| | $hb\bar{b}/hc\bar{c}$ | Tracker | $\sigma_{r\phi} = 5 \oplus 15(p \sin\theta^{\frac{3}{2}})^{-1} \mu$m<br>5$\mu$m single hit resolution |

Arxiv:2209.14111 Arxiv:2211.11084 DOE Basic Research Needs Study on Instrumentation

arXiv:2003.01116

# Physics requirements for detectors

## Precision challenges detectors

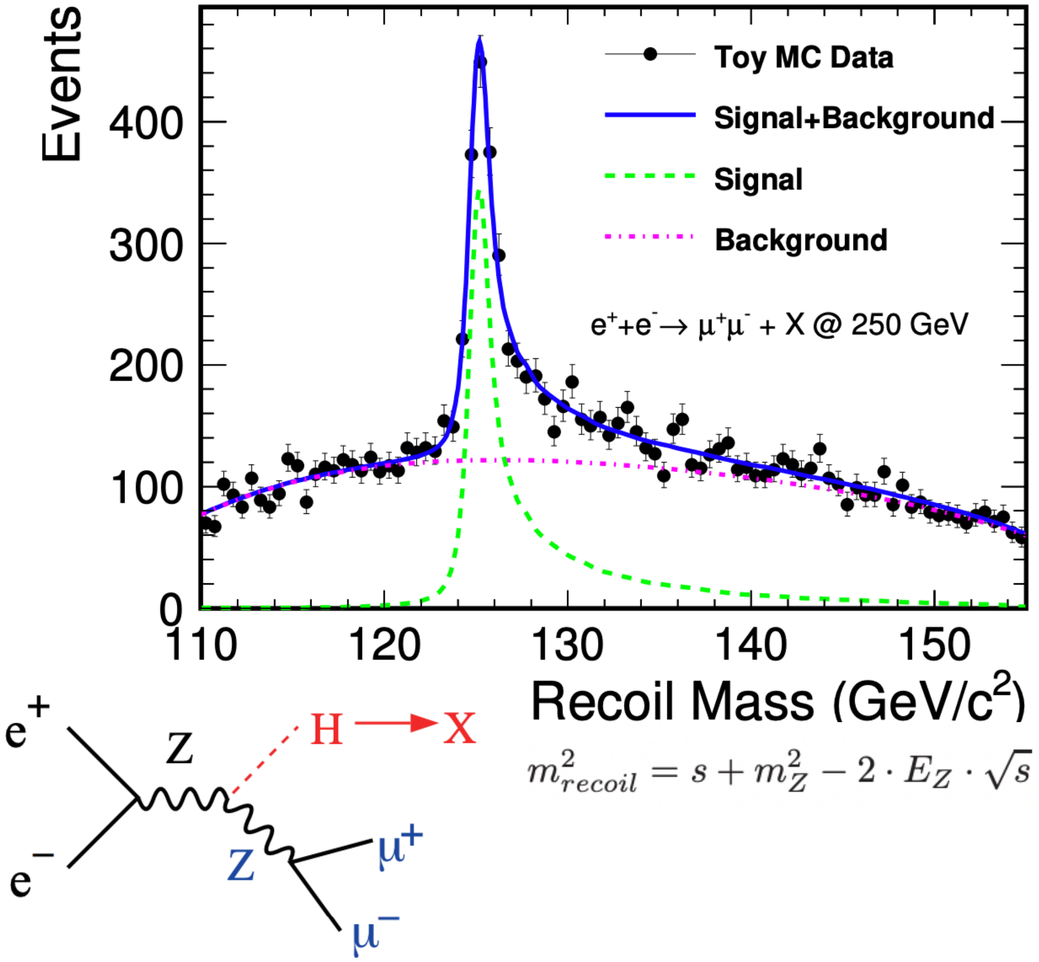
**ZH process: Higgs recoil reconstructed from Z →*μμ***

- Drives requirement on charged track momentum and jet resolutions
- Sets need for high field magnets and high precision / low mass trackers

**Particle Flow reconstruction**

**Higgs → bb/cc decays: Flavor tagging & quark charge tagging at unprecedented level**

- Drives requirement on charged track impact parameter resolution → low mass trackers near IP
- <0.3% X0 per layer (ideally 0.1% X0) for vertex detector
- Sensors will have to be less than 75 *μ*m thick with at least 5 *μ*m hit resolution (17-25*μ*m pitch)



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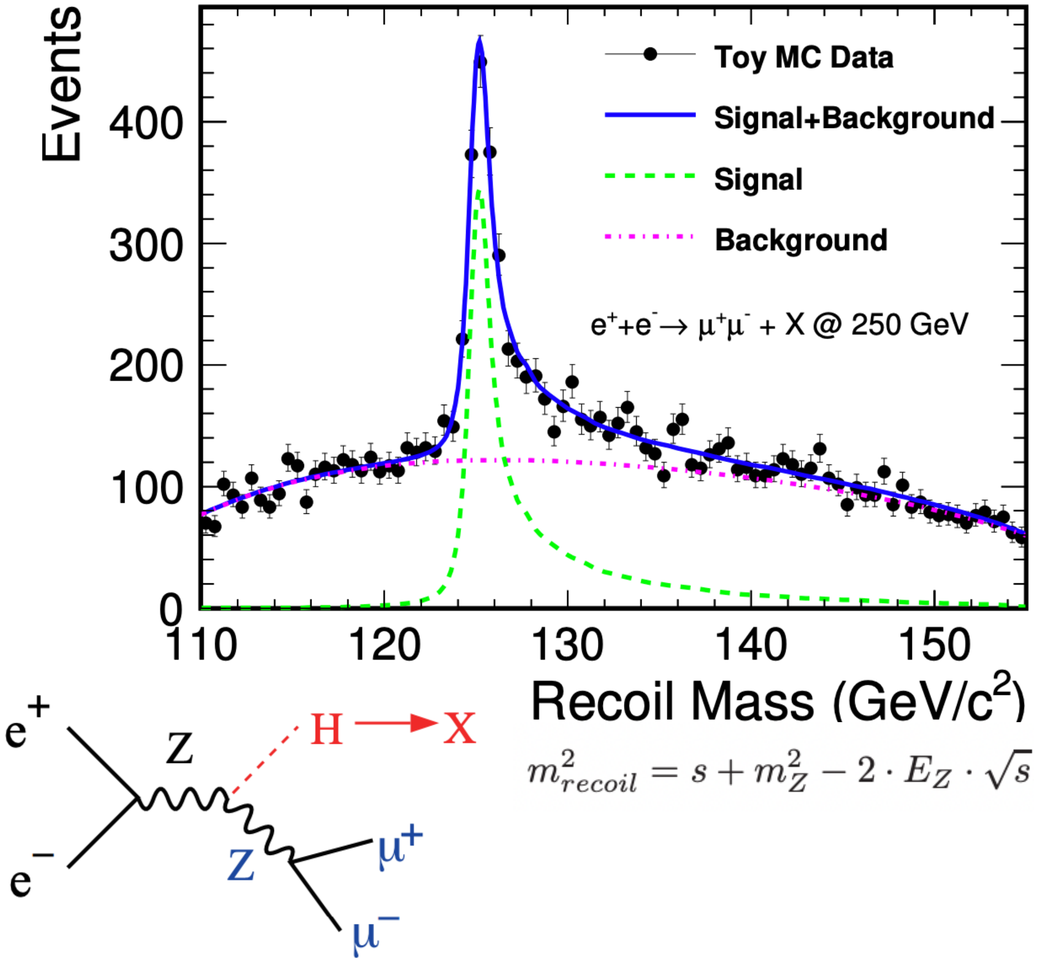


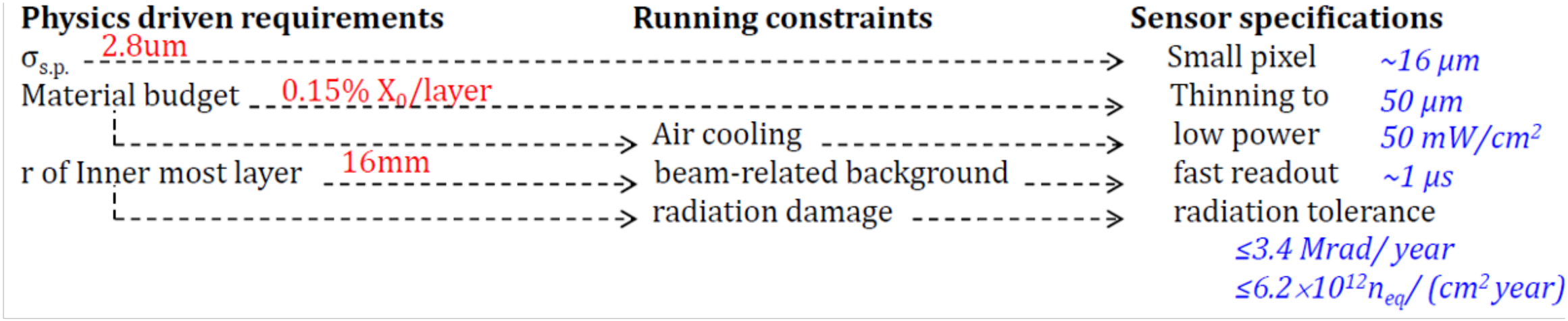

***Need new generation of ultra low mass vertex detectors with dedicated sensor designs***

# Sensors technology requirements for Vertex Detector

## Several technologies are being studied to meet the physics performance

Sensor's contribution to the total material budget of vertex detector is 15-30%

Sensors will have to be less than 75 $\mu$m thick with at least 3-5 $\mu$m hit resolution (17-25 $\mu$m pitch) and low power consumption



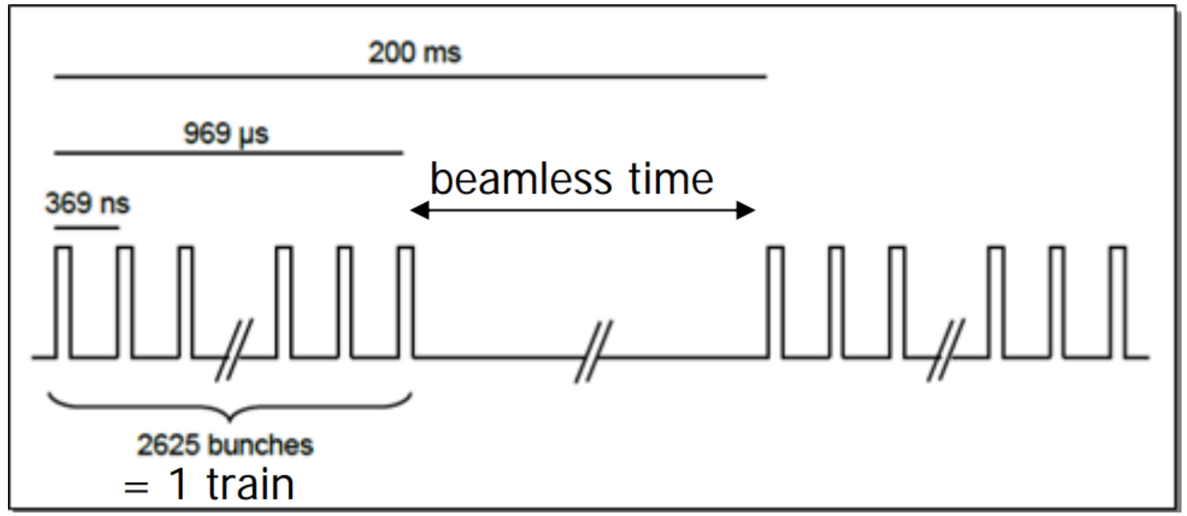
# Future e+e- Colliders

**Joint simulation/detector optimization effort with ILC groups Common US R&D initiative for future Higgs Factories 2306.13567**

## Main Candidates, either linear C³/ILC/CLIC or circular FCC/CEPC

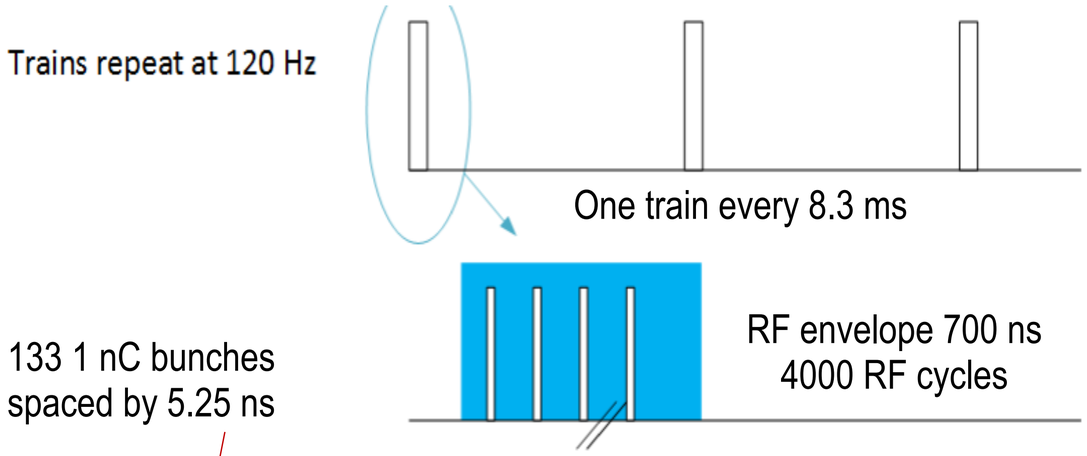
- Linear e+e- colliders are characterized by a very low duty cycle
- Power Pulsing can be an additional handle to reduce power consumption and cooling constraint
  - Factor of 100 power saving for FE analog power
- Tracking detectors don't need active cooling
  - Significantly reduction for the material budget

### ILC Timing Structure




**Duty Cycle = 0.48%**

### C³ Timing Structure



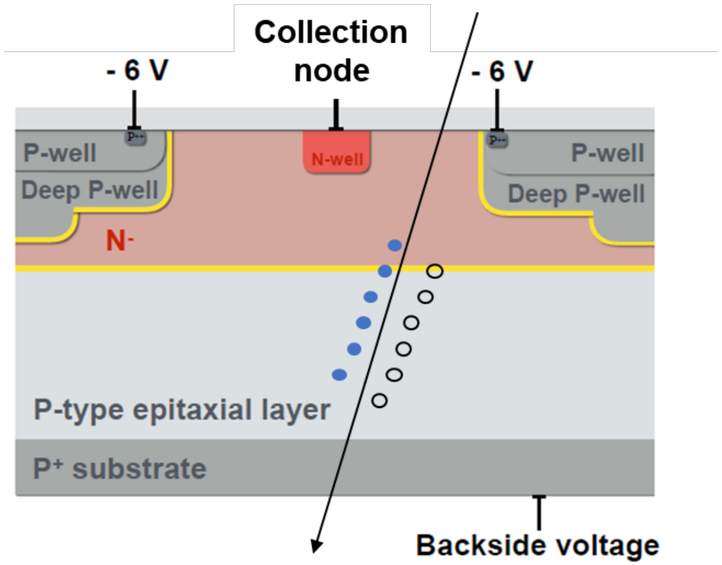

**Duty Cycle = 0.03 %**

**~1 ns time resolution is needed**

# MAPS

## Monolithic Active Pixel Sensors (MAPS) for high precision tracker and high granularity calorimetry

- Monolithic technologies have the potential for providing higher granularity, thinner, intelligent detectors at lower overall cost.
- Significantly lower material budget: sensors and readout electronics are integrated on the same chip
  - Eliminate the need for bump bonding : thinned to less than 100$\mu$m
  - Smaller pixel size, not limited by bump bonding
  - Lower costs : implemented in standard commercial CMOS processes




**Initial specifications for fast MAPS aka NAPA**

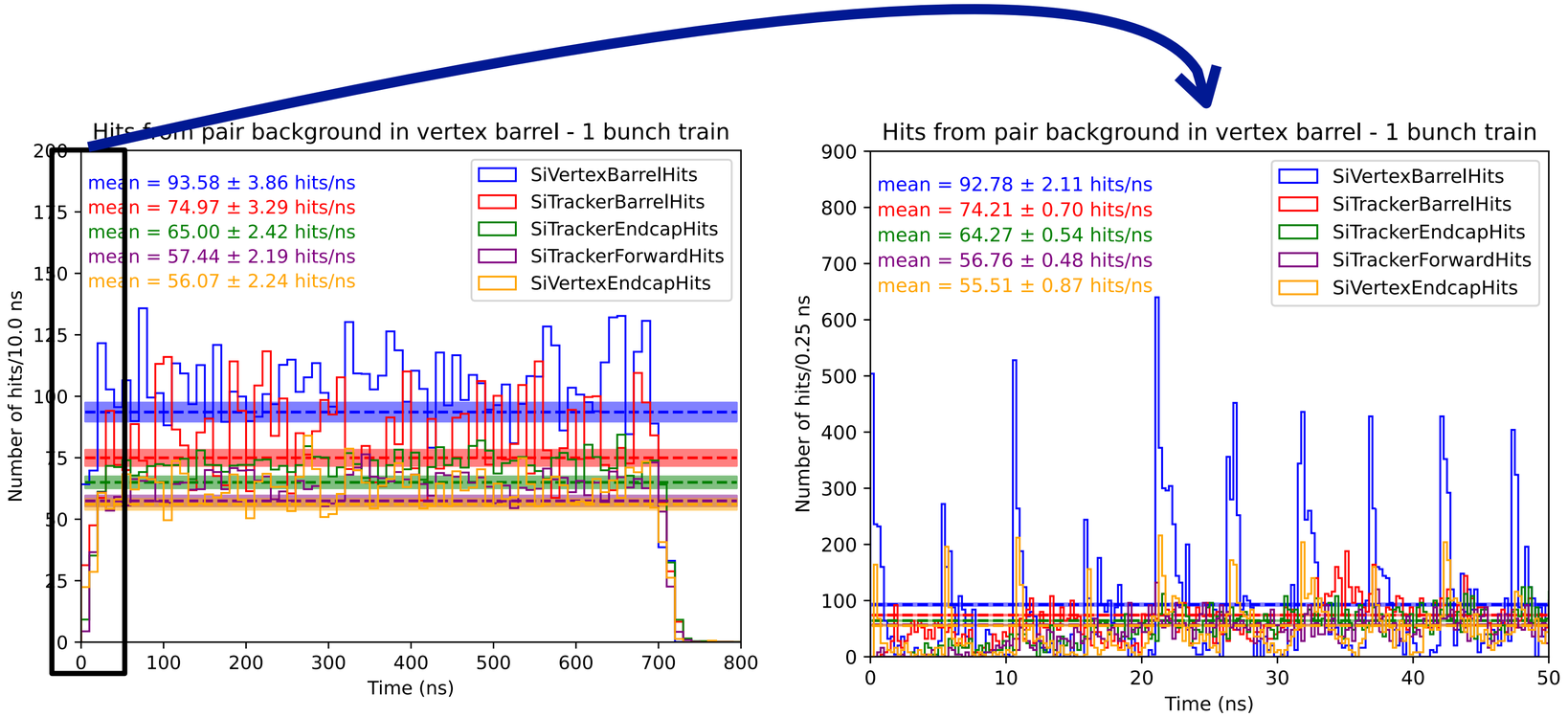
| Parameter | Value |
|---|---|
| Min. Threshold | 140 $e^-$ |
| Spatial resolution | 7 $\mu$m |
| Pixel size | 25 x 100 $\mu m^2$ |
| Chip size | 10 x 10 $cm^2$ |
| Chip thickness | 300 $\mu$m |
| Timing resolution (pixel) | ~ns |
| Total Ionizing Dose | 100 kRads |
| Hit density / train | 1000 hits / $cm^2$ |
| Hits spatial distribution | Clusters |
| Power density | 20 mW / $cm^2$ |

Table 1: Target specifications for 65 nm prototype.

# Tracking performance

## O(ns) timing capabilities as an additional handle to suppress beam induced backgrounds

Time distribution of hits per unit time and area: $\sim 4.4 \cdot 10^{-3}$ hits/(ns·mm$^2$) $\simeq$ 0.03 hits/mm$^2$ /BX
in the 1st layer of the vertex barrel SiD-like detector for ILC/C$^3$

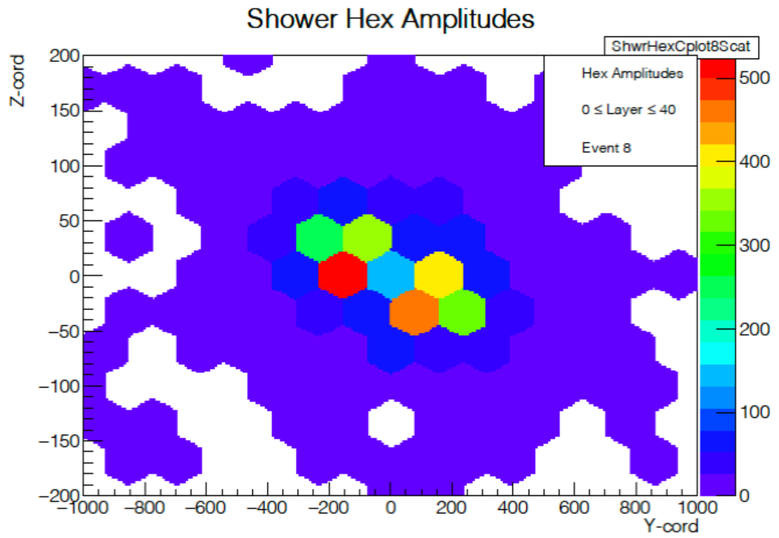



| Parameter | Value |
|---|---|
| Time resolution | 1 ns-rms |
| Spatial Resolution | 7 $\mu$m |
| Expected charge from a MIP | 500 – 800 e/h |
| Minimum Threshold | 200 e- |
| Noise | < 30 e-rms |
| Power density | < 20 mW/cm$^2$ |
| Maximum particle rate | 1000 hits/cm$^2$ |

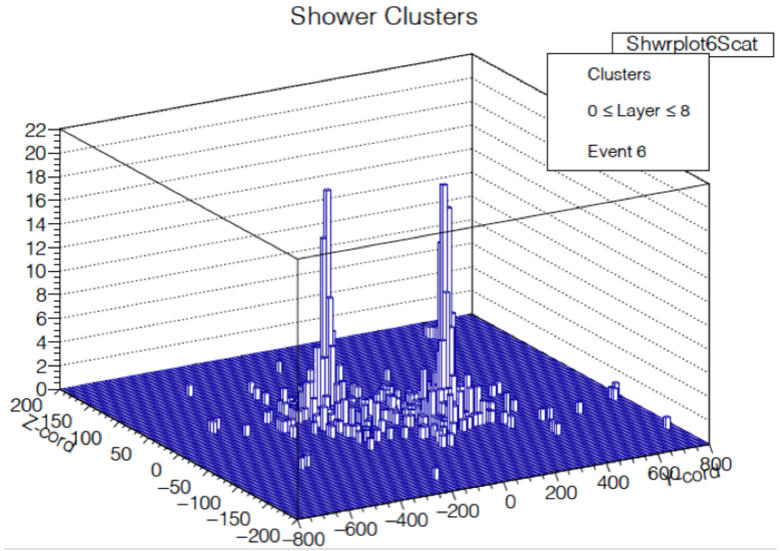
D. Ntounis talk on beam background simulations

# Digital E-Calorimeter

**GEANT4 simulations of Transverse distribution of two 10 GeV showers separated by one cm**




Pixel amplitudes (analog) in the ILC 13 mm$^2$ TDR pixel design




Clusters in the first 5.4 radiation lengths in the new SiD digital MAPS of 2500 $\mu$m$^2$ pixel

The design of the digital MAPS applied to the ECal exceeds the physics performance required for the linear collider as specified in the ILC TDR

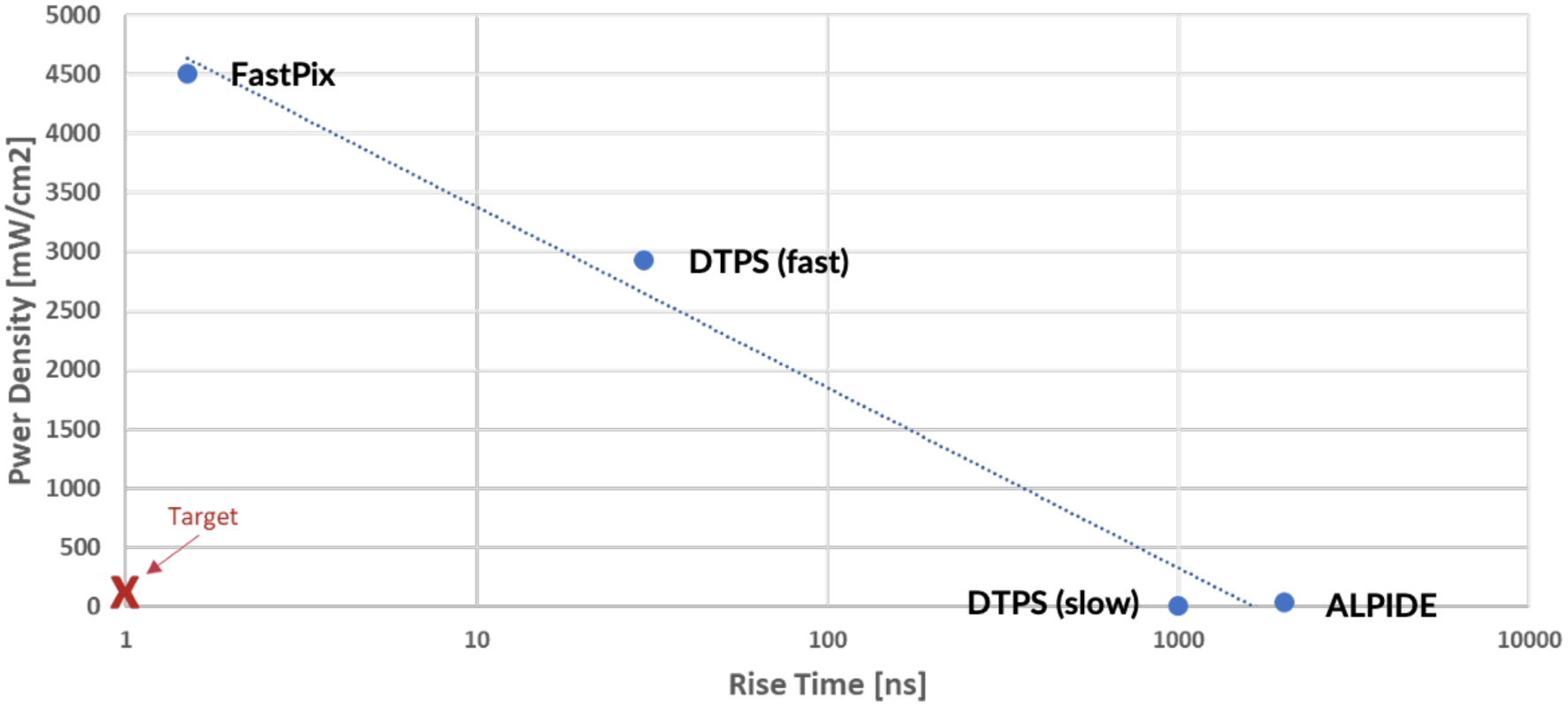
# Target Specs vs. State of the Art

| Chip name | Technology | Pixel pitch [$\mu$m] | Pixel shape | Time resolution [ns] | Power Density [mW/cm$^2$] |
|---|---|---|---|---|---|
| **Target Specification** | **?** | **25 x 100** | **Sq / rect** | **1** | **< 20** |
| **ALPIDE** [2][3] | **Tower 180 nm** | **28** | **Square** | **< 2000** | **5** |
| **FastPix** [4][5] | **Tower 180 nm** | **10 - 20** | **Hexagonal** | **0.122 – 0.135** | **>1500** |
| **DPTS**[6] | **Tower 65 nm** | **15** | **Square** | **6.3** | **112** |
| **Cactus** [7] | **LF 150 nm** | **1000** | **Square** | **0.1-0.5** | **145** |
| **MiniCactus** [8] | **LF 150 nm** | **1000** | **Square** | **0.088** | **300** |
| **Monolith** [9][10] | **IHP SiGe 130 nm** | **100** | **Hexagonal** | **0.077 – 0.02** | **40 - 2700** |

**No design fulfills all target specification → The need to develop a custom design**

We decided to go with the Tower 65nm technology, which has been optimized by CERN WP1.2 to have low sensor capacitance allowing very good performance with low power consumption.
+ it has the possibility of a wafer-scale stitched sensor
+ it has been proven to be radiation tolerant

# Target Specs vs. State of the Art

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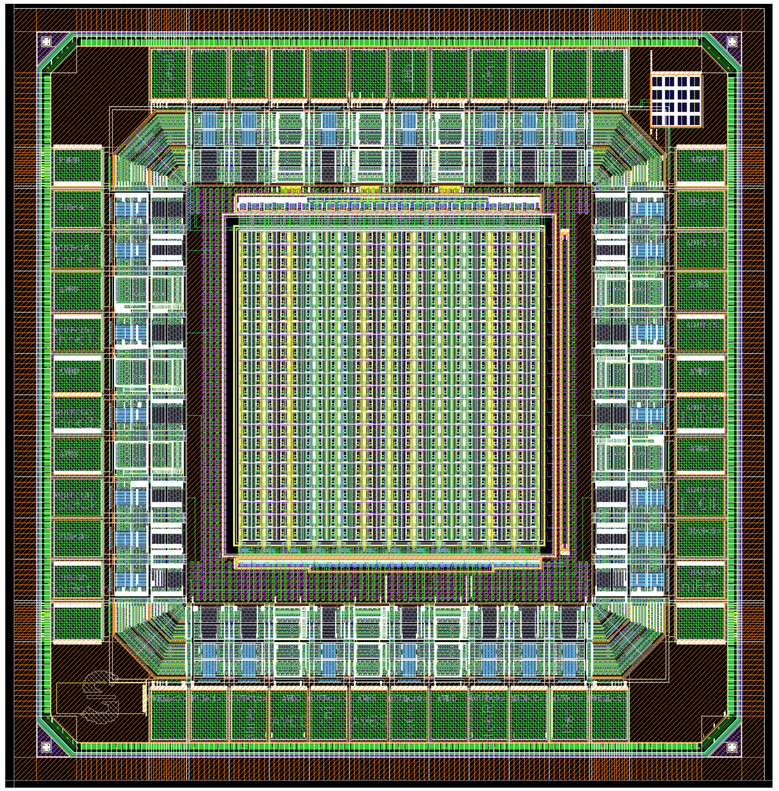
+ it has the possibility of a wafer-scale stitched sensor
+ it has been proven to be radiation tolerant

# NAPA_p1: **NA**nosecond **P**ixel for large **A**rea sensors – **P**rototype **1**

## First prototype in TJ 65nm

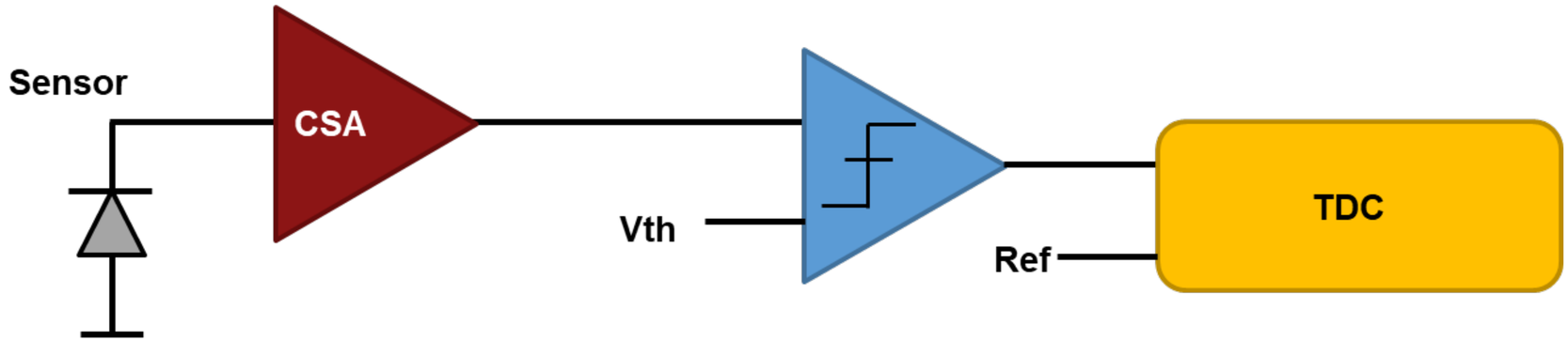
- The prototype design submitted with a total area 5 mm x 5 mm and a pixel of 25 $\mu$m  25 $\mu$m, to serve as a baseline for sensor and pixel performance.
- Design motivation ➔ simple architecture with minimum global signals to reduce failure risk in a large area implementation.
- Thanks to CERN WP1.2 effort on sensor optimization in TowerSemi 180 nm and 65 nm technologies

  ➔ $C_{sensor}$ of 2-3 fF is achievable while maintaining high collection efficiency



*Layout of MAPS SLAC prototype for WP1.2 shared submission*

# Timing Limits for a Complete Detection Chain




$$\sigma^2_{Total} = \sigma^2_{TOA} + \sigma^2_{FE} + \sigma^2_{Timewalk} + \sigma^2_{TDC}$$

$\sigma_{TOA}$ < 150 ps-rms
For small optimized pixels
based on literature

$\sigma_{FE}$ < 400 ps-rms
for < 1 $\mu$W/pixel

Can be corrected if we measure the
ToT inside the pixel

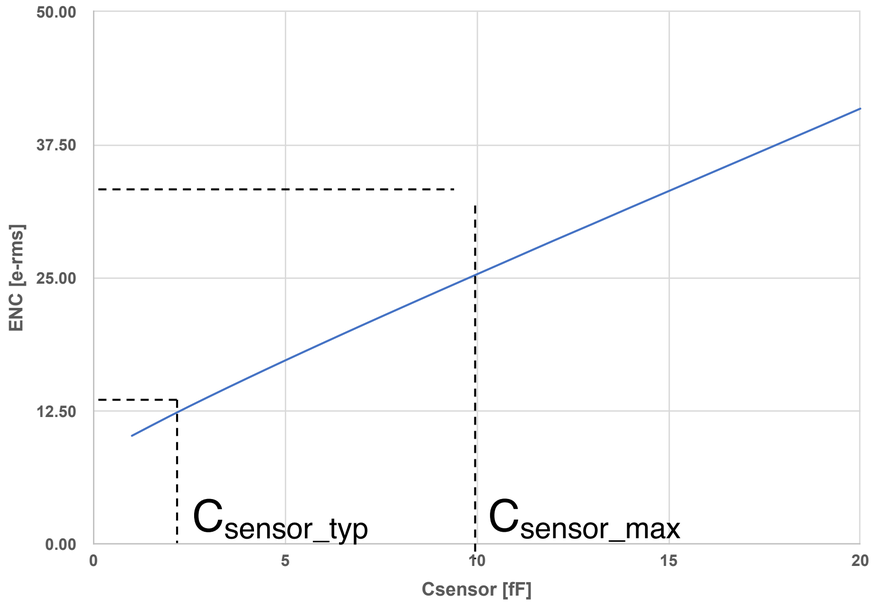
$\sigma_{TDC}$ < 150 ps-rms
Limited by quantization noise

- Assuming time walk is fully corrected ➔$\sigma_{Total}$~**500** ps-rms with reasonable pixel power consumption, going lower will cost increasingly more power, not compatible with large area sensors.
- Accounting for residual Time Walk after correction, and other non-idealities, it is reasonable to aim for ~1 ns-rms time resolution

# Summary of NAPA-p1 Performance

| | Specification | Simulated NAPA-p1 |
|---|---|---|
| **Time resolution** | 1 ns-rms | 0.4 ns-rms ✓ |
| **Spatial Resolution** | 7 $\mu$m | 7 $\mu$m ✓ |
| **Noise** | < 30 e-rms | 13 e-rms ✓ |
| **Minimum Threshold** | 200 e- | ~ 80 e- ✓ |
| **Average Power density** | < 20 mW/cm$^2$ | 0.1 mW/cm$^2$ for 1% duty cucle ✓ |

ENC = 13 e-rms for $C_{sensor\_typ} \approx 2$ fF

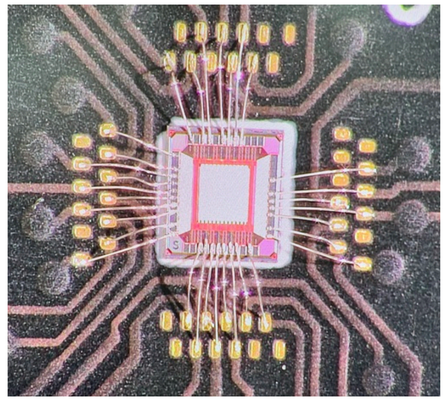



Acknowledgement: to CERN WP 1.2 for the excellent cooperation: NAPA-p1 uses the pixel masked developed and optimized by CERN, and was fabricated in a MLR led by CERN

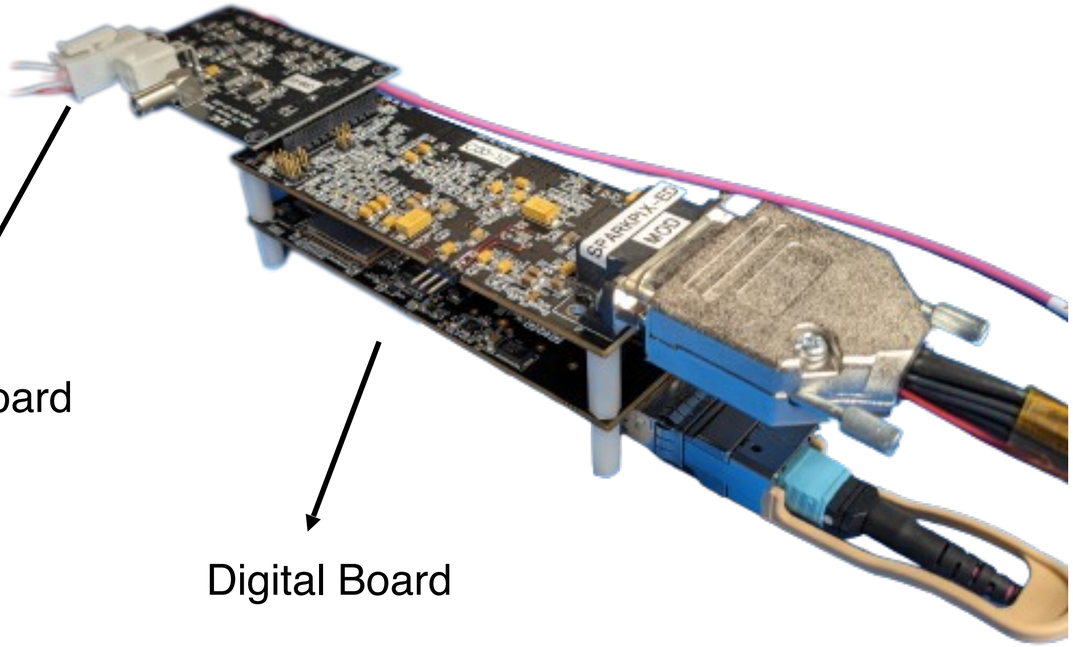
# Test Setup for NAPA-p1

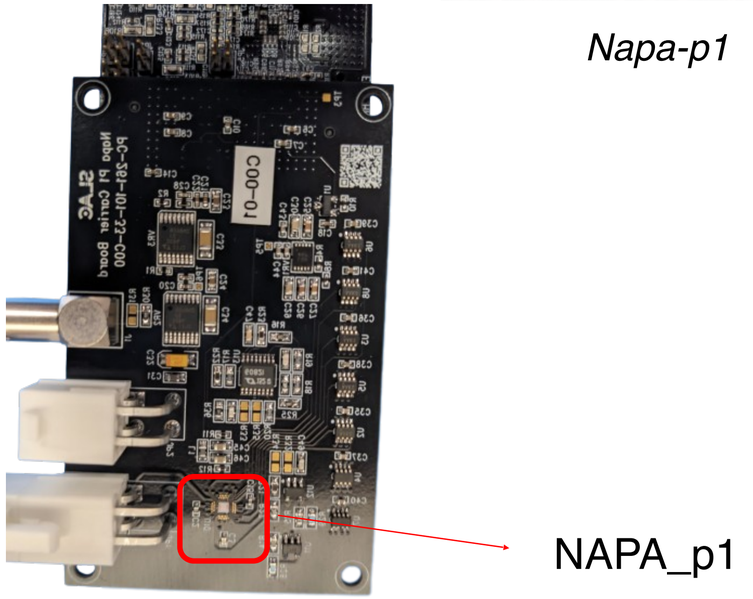
## Chips were received in September 2023

- A custom carrier was designed at SLAC for the NAPA-p1 chip providing all analog references
- The chip was wire-bonded at SLAC
- The carrier boards connects to a digital board containing an FPGA and several DAC's



*Napa-p1*



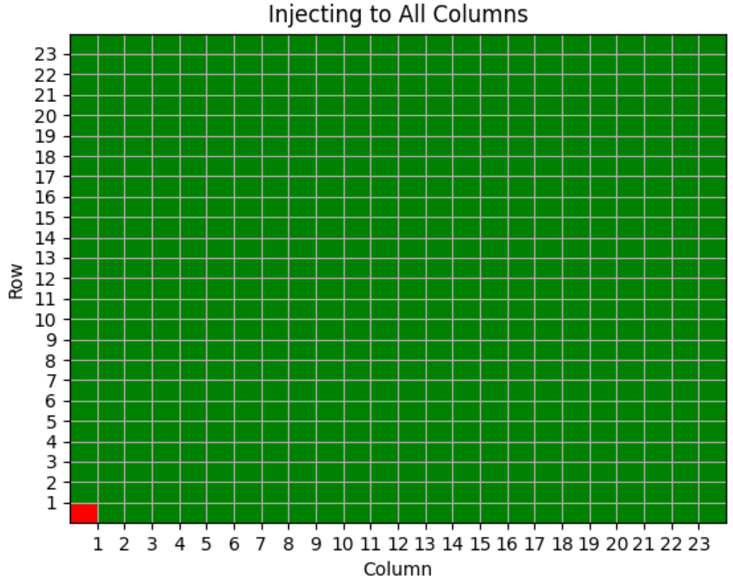



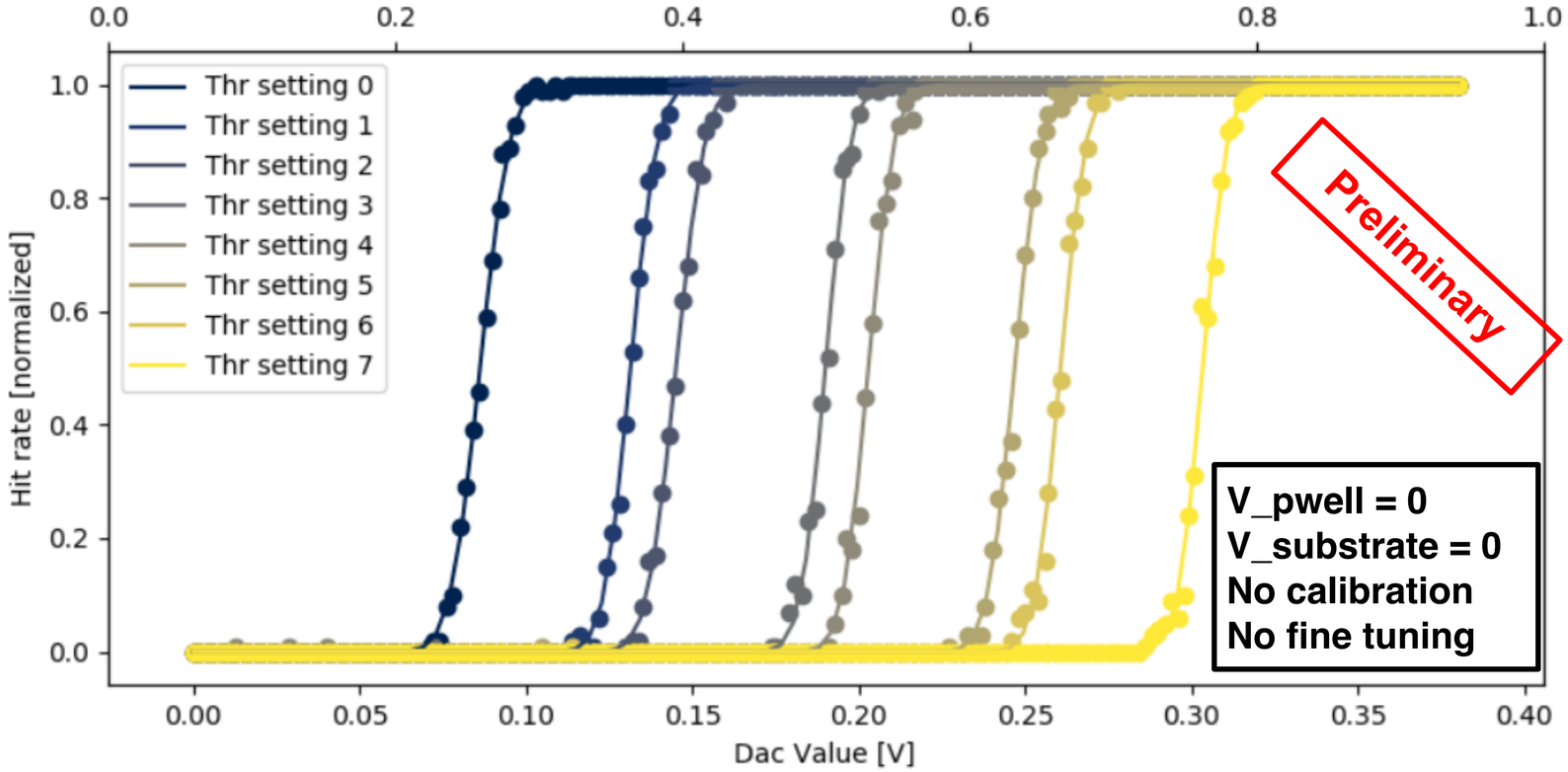

Carrie Board

# Preliminary Characterization Results

## Chip characterization is on going

**99% of matrix is responsive**




Very Preliminary Characterization Results Obtained a Few Days Ago Thanks to:
Xavier Defay, Christos Bakalis, Namit Mishra, Lorenzo Rota and others

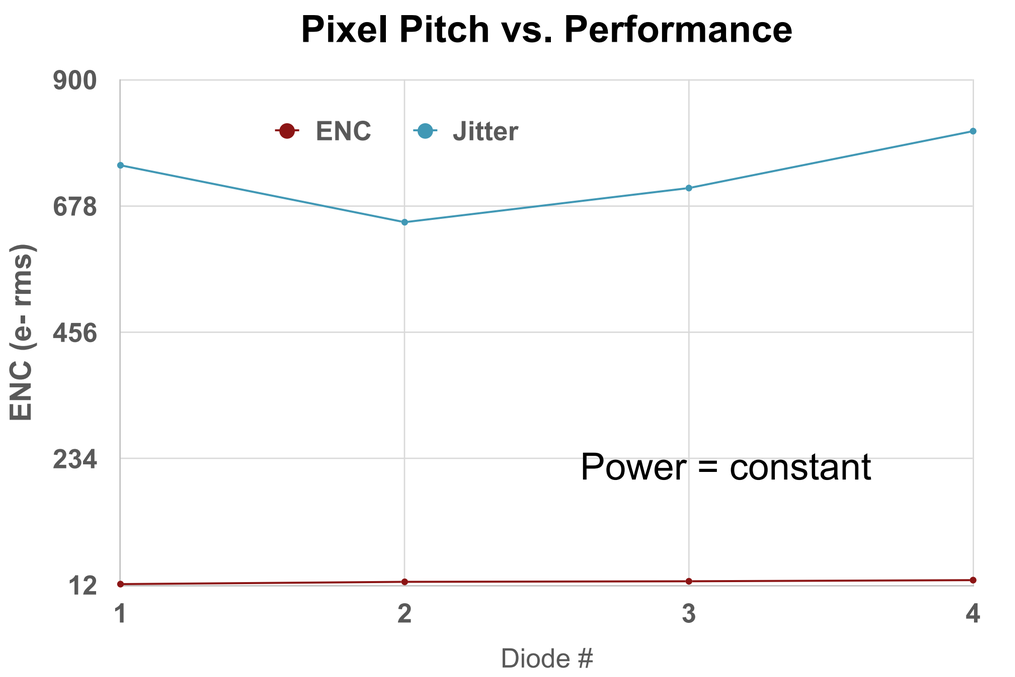
# Towards a Large Sensor

The main limitation comes from large scale power distribution rather than cooling constraints

Potential solutions to address the power distribution over a large scale:

- Decrease power density ➔ Physics requirement are for a pixel of 25 $\mu$m x 100 $\mu$m. Our initial study shows that a pixel of 25 $\mu$m x 50 $\mu$m gives the best optimization for Performance/Power density
- Reduce $R_{pix}$ ➔ Top metal, low resistivity power grid
- Keep power constant ➔ Switch from a single ended to a differential comparator
- Reduce the column length ➔ Target sensor of 5 cm x 20 cm instead of 10 cm x 10 cm

➔ NAPA-p2 design has started to tackle these challenges

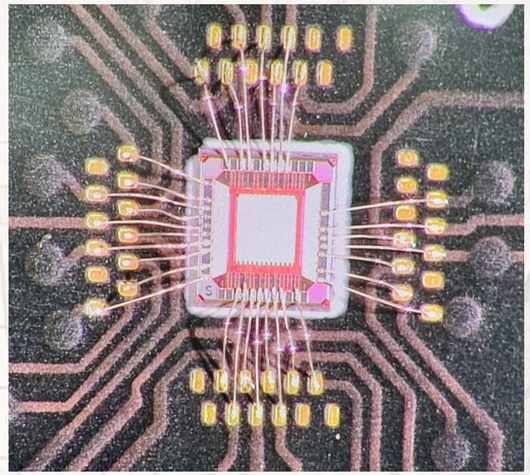



Simulation by Jacob Sillman

# Conclusions and next steps

## First MAPS prototype targeting $e^+e^-$ spec is being tested

- MAPS technology is being investigated for applications at future $e^+e^-$ colliders for both tracking and calorimetry applications
- Simulations of NAPA-p1 show that it is possible to achieve a time resolution 1 ns-rms with reasonably low power consumption of ~100 mW/cm$^2$ x Duty Cycle (at LC < 1%)
- First characterization of Napa-p1 is promising - more ongoing
  - It will serve as a pixel proof of concept.
- Design of NAPA-p2 has started to tackle large sensor challenges
  - NAPA-p2 will serve as a system proof of concept.



*Layout of MAPS SLAC prototype for WP1.2 shared submission*

Thank you!

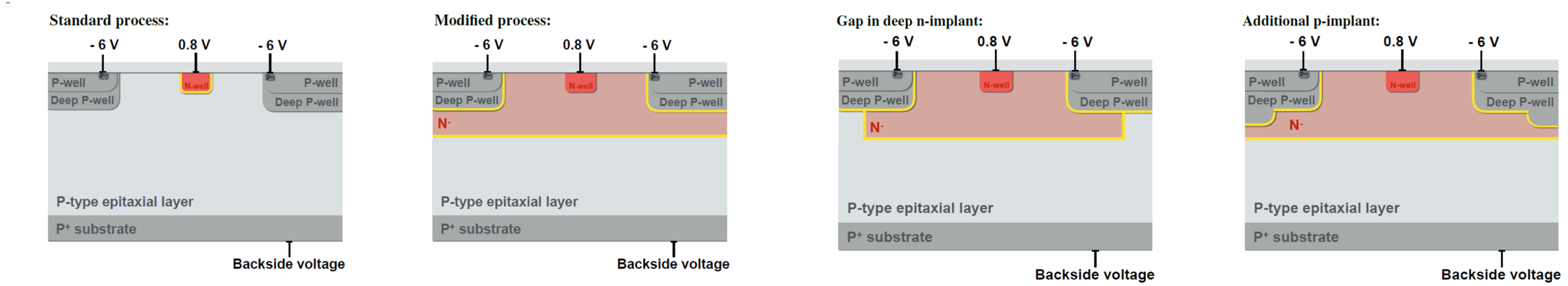
# Design Approach

For a constant SNR and $Q_{in}$ ➔ $Power \propto (C_{sensor})^m \quad with\ 2 \leq m \leq 4$ as shown in [11]

➔ **Aim for smallest possible sensor capacitance**

- Thanks to CERN WP1.2 effort on sensor optimization in TowerSemi 180 nm and 65 nm technologies [12] [13]
  - ➔ $C_{sensor}$ of 2-3 fF is achievable while maintaining high collection efficiency

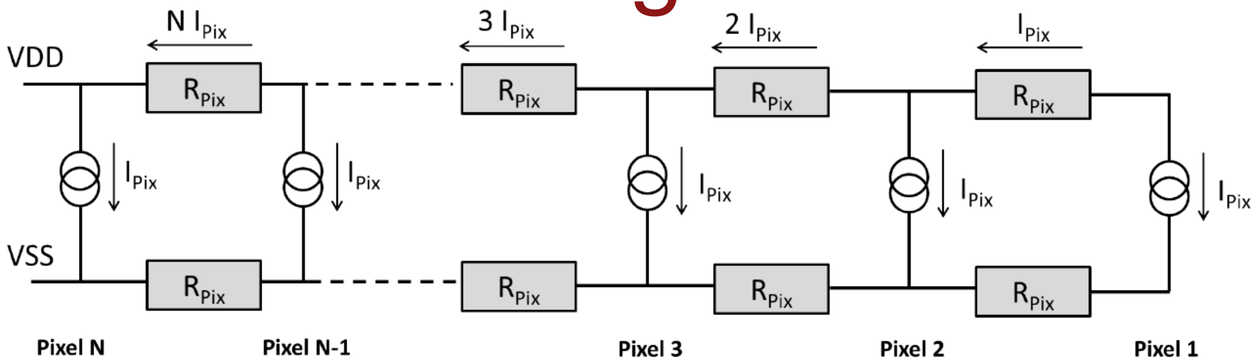
Jitter $\propto \frac{Cload}{\sqrt[n]{I}}$ with $1 \leq n \leq 2$ ➔ **Keep $C_{load}$ to a minimum and increase the current if needed.**




**Sensor optimization in TowerSemi 180 nm process from [12] and [13]**

# Going Towards a Large Sensor → Challenge

$$\Delta V = I_{pix} \times R_{Pix} + 2 \times I_{Pix} \times R_{Pix} + 3 I_{Pix} \times R_{Pix} + ... + N \times I_{Pix} \times R_{Pix}$$
$$\Delta V = I_{Pix} \times R_{Pix}(1 + 2 + 3 + ... + N)$$
$$\Delta V = I_{Pix} \times R_{Pix} \times \frac{N(N+1)}{2}$$



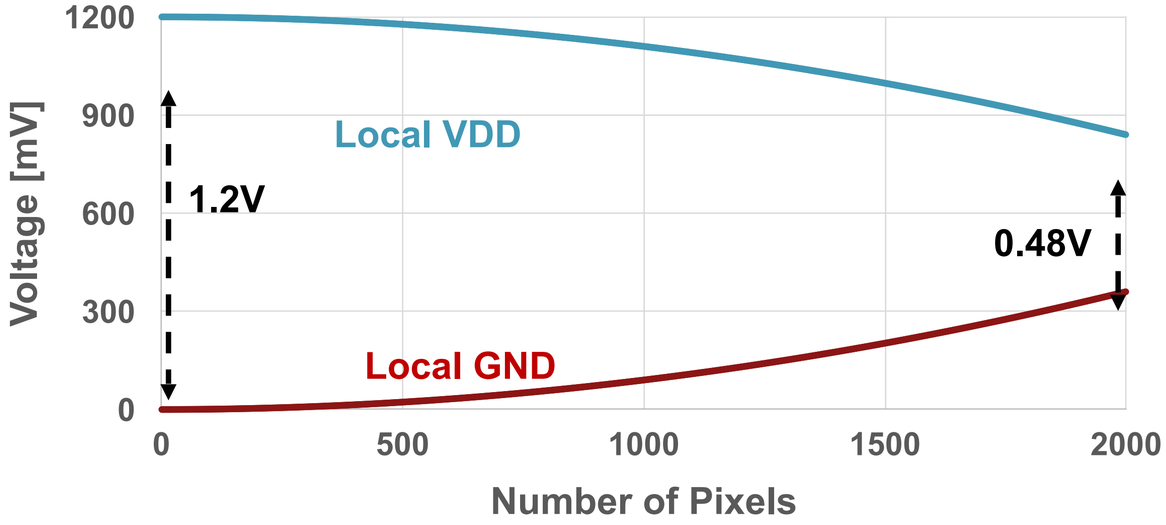

**Assuming :$I_{pix}$ = 600 nA and $R_{pix}$ = 300 mΩ**

**Assuming pixel of 25 $\mu$m x 25 $\mu$m**

**A column of 10 cm would have 4000 pixels**

**Double sided powering**

**→ max drop length = 2000 pixels**

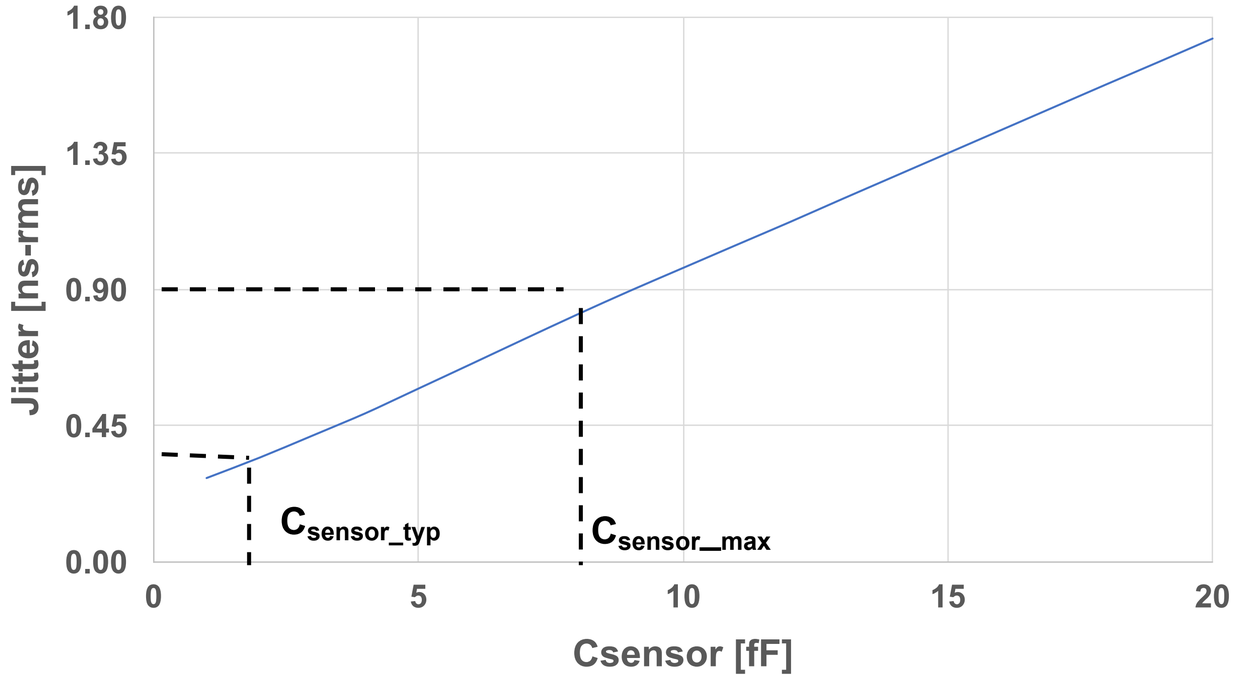


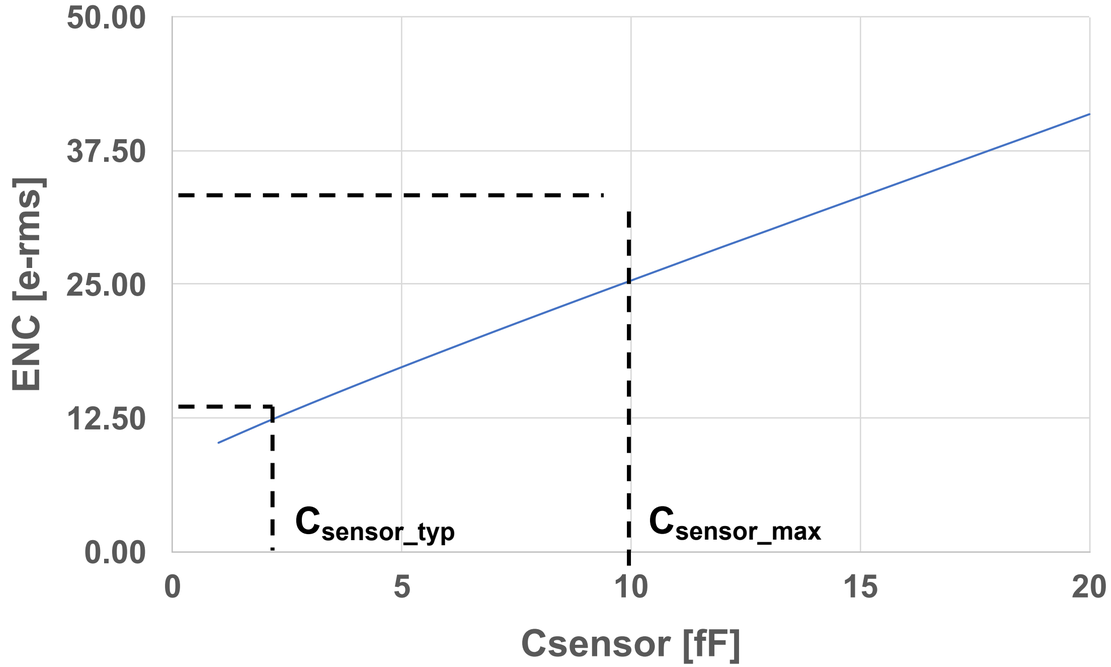

**VDD-GND goes from 1.2 V near the power pads down to around 480 mV after 2000 pixels**

**The main limitation comes from large scale power distribution rather than cooling constraints**

**After $10^3$ pixels (reticle, 2.5 cm), $V_{drop} \approx 0.1$ V**
**After 4 x $10^3$ pixels (sensor, 10cm), $V_{drop}$ = 1.5V !**

# Simulation of Jitter and ENC as a Function of $C_{sensor}$



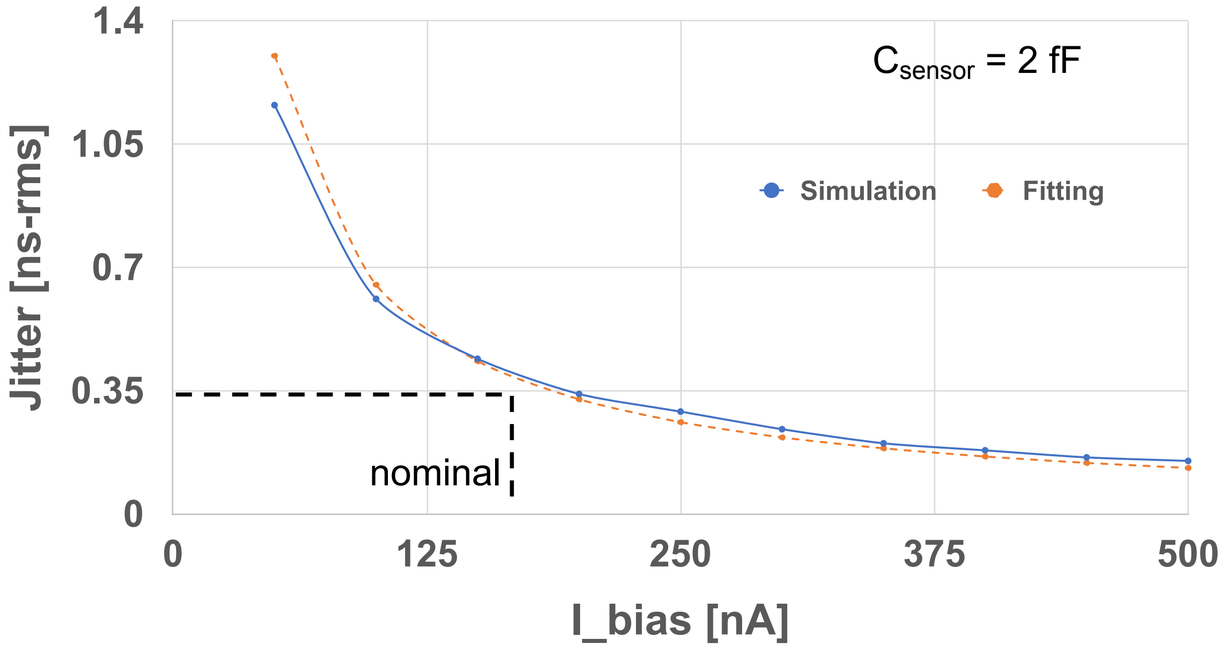




**jitter = 400 ps for $C_{sensor\_typ} \approx 2$ fF** → **Ok for Specs** ← **ENC = 13 e-rms for $C_{sensor\_typ} \approx 2$ fF**

**These simulations are with a nominal pixel current of 600 nA → <Power density> = 115 mW/cm² x duty cycle**
**For e+e- machines such as ILC and C³, duty cycle is expected < 1%**

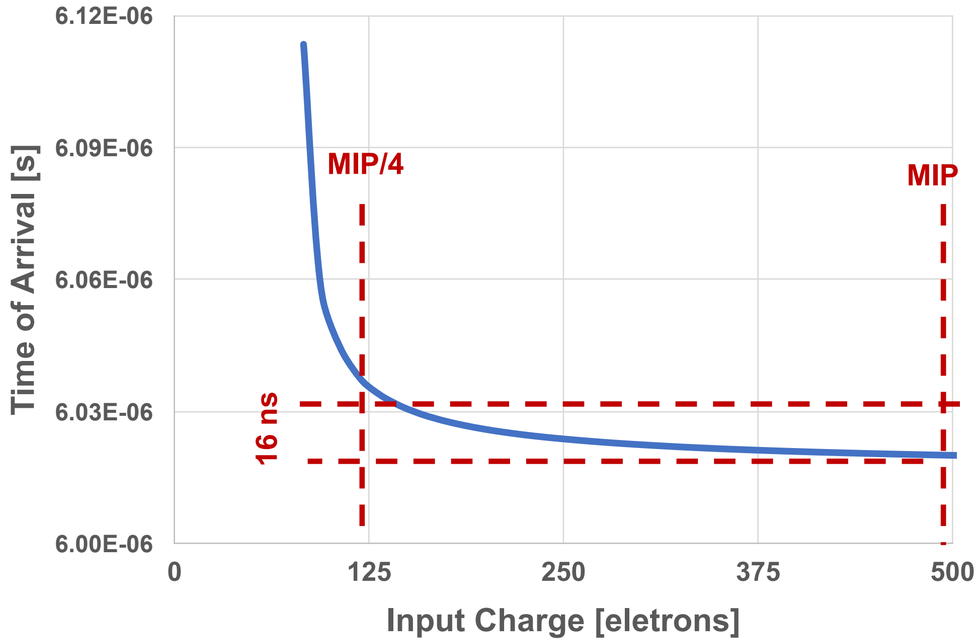
# Simulation Results : Jitter and Time Walk

## Jitter




I_bias = 200 nA ≡ pixel current = 600 nA
From theory we expect : $\sigma_{FE} \propto \frac{1}{(\mathrm{Power})^{\frac{1}{n}}}$ with $1 \leq n \leq 2$

## Time Walk




Time walk for MIP → MIP/4 = 16 ns
Not negligible and must be corrected
(in pixel? In balcony? Offline? TBD)

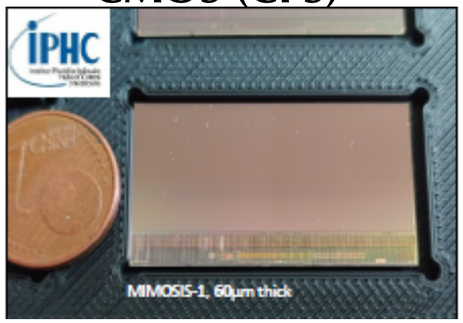
# Sensors technology overview

**Several possible choices** for the VTX detector:

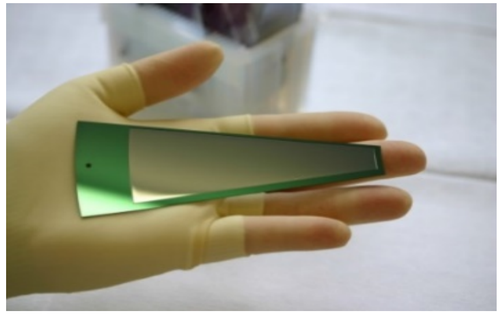
- Monolithic Active Pixels (MAPS)
  - CMOS Pixel Sensors (CPS)
  - Fully Depleted on High Resistivity Substrate (DNwel sensing)
  - Fully Depleted SOI technologies
- Depleted Field Effect Transistors (DEPFET)
- Fine pixel Charged Coupled Devices (CCD)
- 3D integration

- The general landscape is also changing rapidly with advances in microelectronics

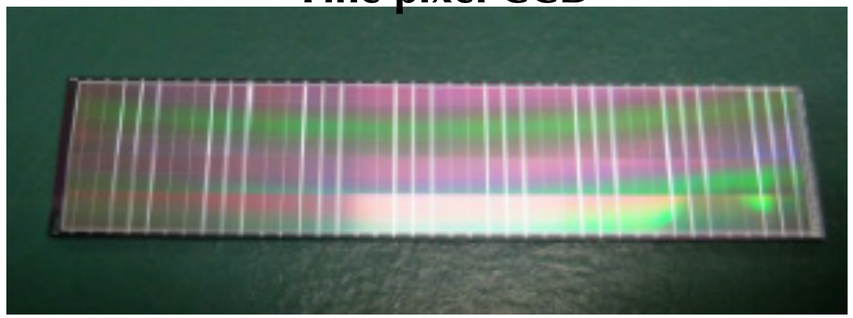
**CMOS (CPS)**



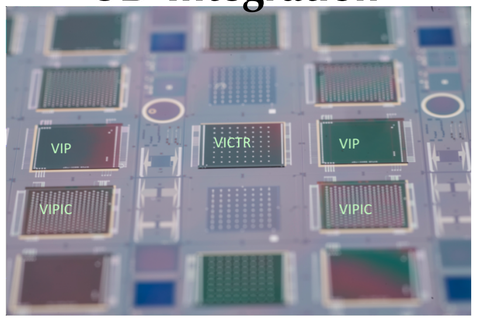

**DEPFET**



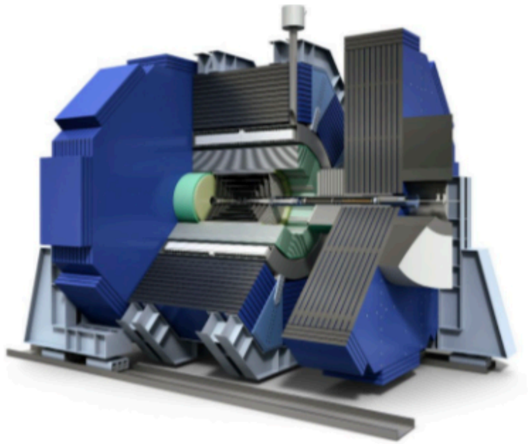
**Fine pixel CCD**

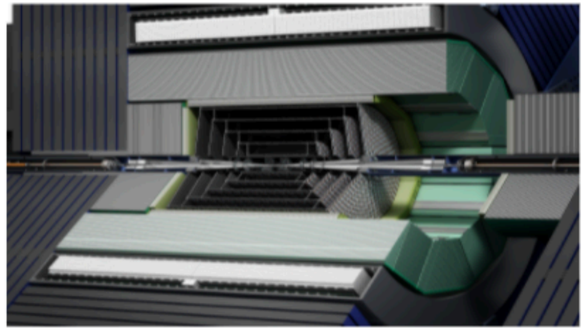


**3D Integration**

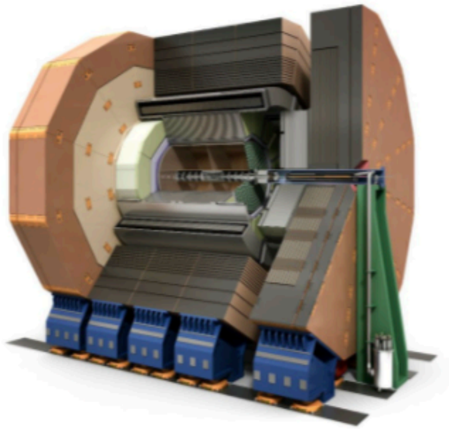


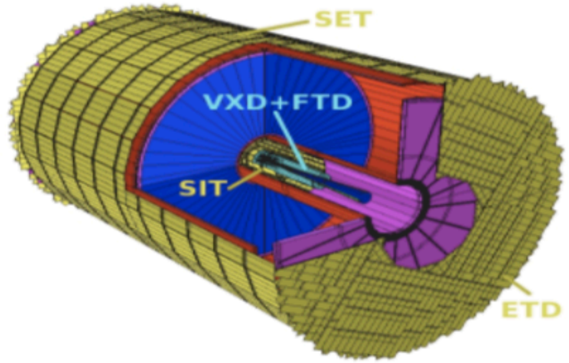
# Detectors design at lepton colliders





SiD



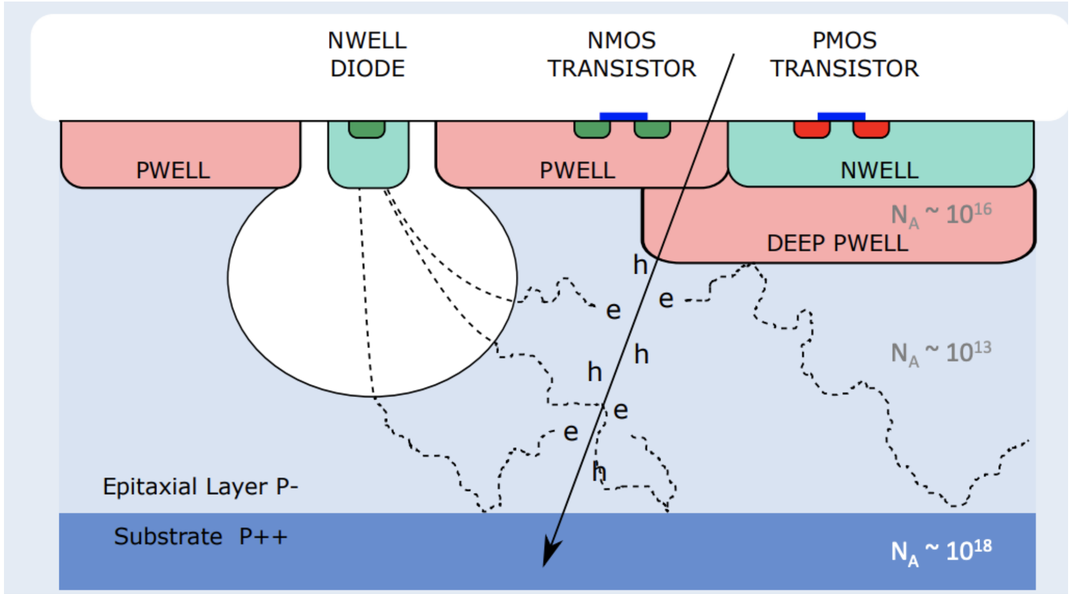



ILD

- Detector designs at e+e- colliders are converging to very similar strategies
  - Particle Flow reconstruction → plays a big part in many designs
- SiD like detector - Compact all silicon detector
- ILD like detector - Larger detector with Silicon+TPC tracker
  - Larger detector. Simulation and design work active in Europe / Japan
- IDEA detector - Using dual readout calorimeter, under study at CEPC/FCC-ee

# ALPIDE

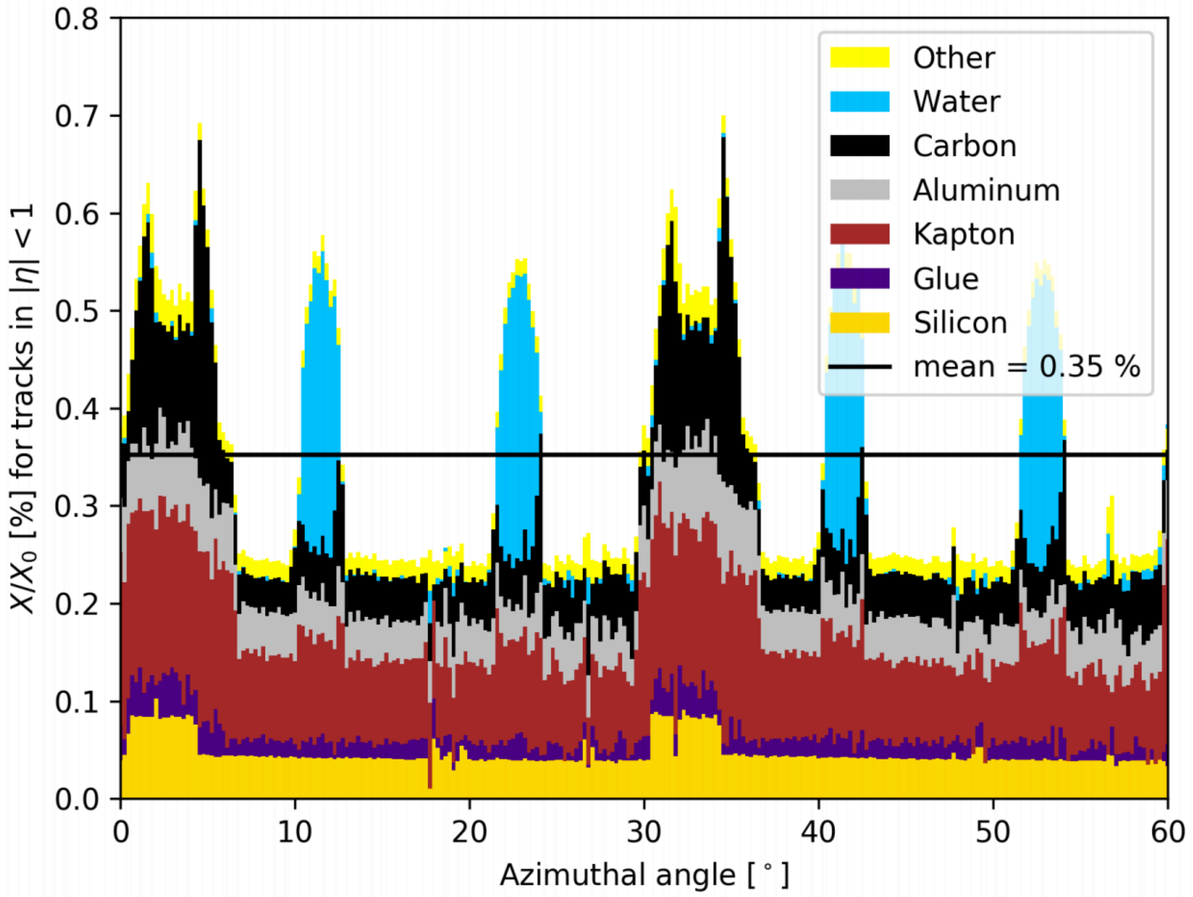
- With the current tracker upgrade ALICE redefined the new state-of-the art in CMOS MAPS technology and its applications in HEP
- ALice PIxel DEtector (ALPIDE) uses CMOS Pixel sensor used in imaging process
  - full CMOS circuitry within active area
  - Sensor thickness = 20-40 µm (0.02-0.04% X0)
  - 5µm spatial resolution
  - radiation hard to $10^{13}$ 1 MeV $n_{eq}$




V. Manzari, 2019

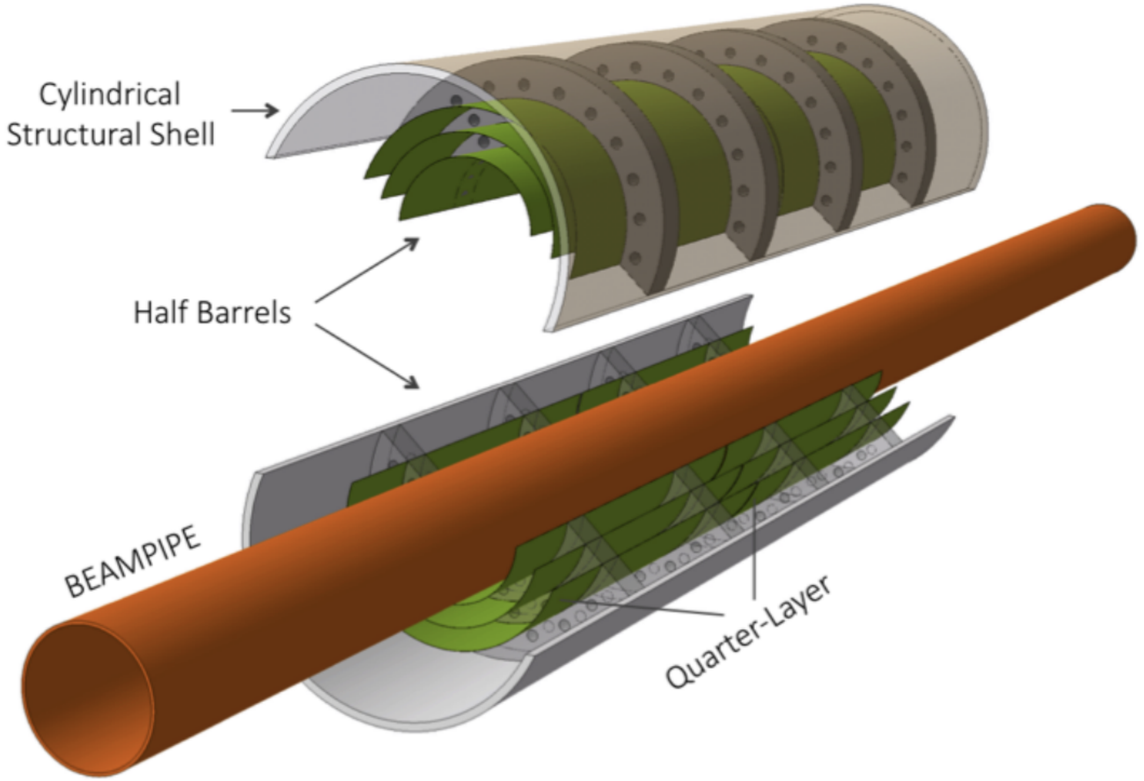
The used technology offers further opportunities: smaller feature size, **bending** that directly impact the key measurements that highly rely on precise vertexing and low material budget

# Towards ultra low mass trackers




- Sensor's contribution to the total material budget is 15-30%
  - cables + cooling + support make up most of the detector mass
- Challenges (beam backgrounds, cooling, material budget) needs to be addressed by emerging R&D's:
  - Reduce impact of mechanical supports, services, overlap of modules/ladders
  - Beam related background suppression ⟹ evolve time stamping toward a few 100 ns (bunch-tagging)
- At linear colliders the baseline consists in air-cooling which is expected to be able to extract the total power dissipation of the vertex detector (< 40 mW/cm$^2$)
  - more specific developments are also being pursued as micro-channel cooling for DEPFET

# ALICE: Bent MAPS for Run 4



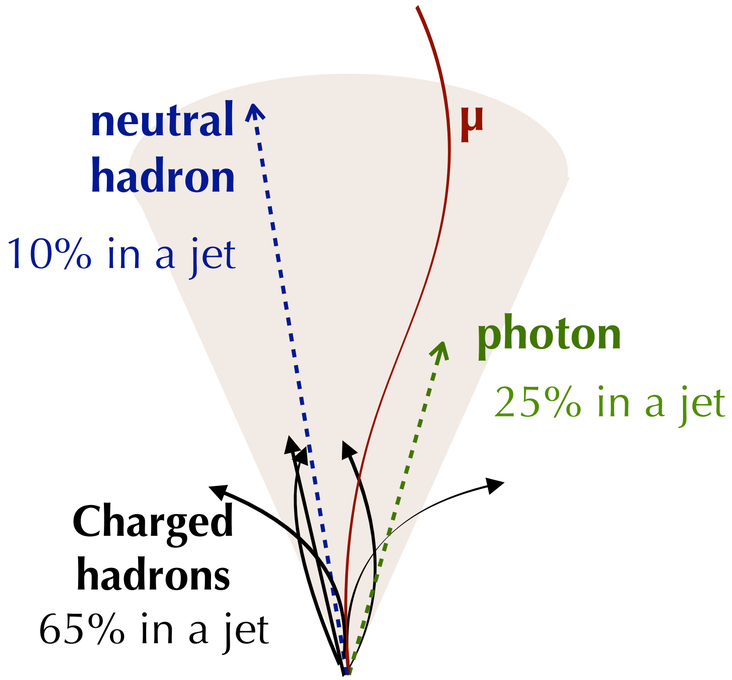

**Bending Si wafers + circuits is possible**

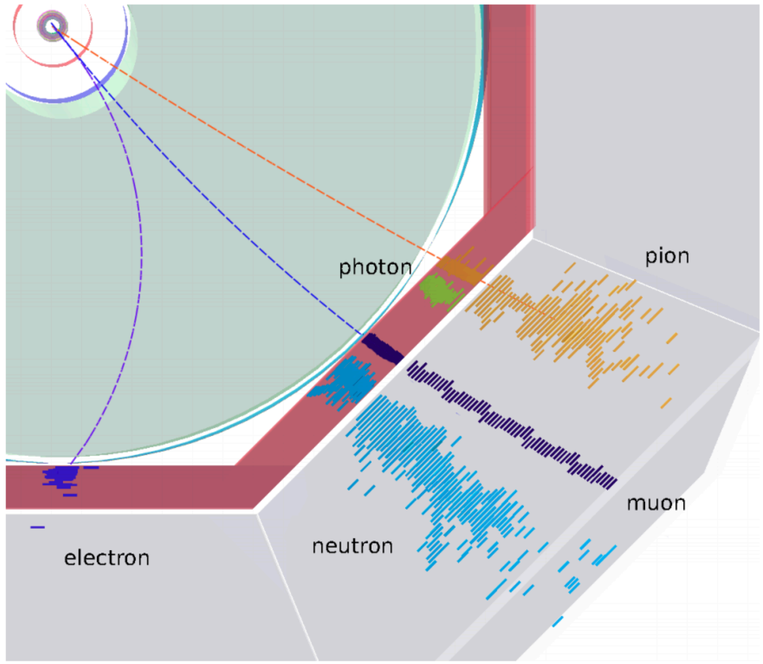
Recent ultra-thin wafer-scale silicon technologies allow:

- Sensor thickness = 20-40 µm - 0.02-0.04% X0
- Sensors arranged with a perfectly cylindrical shape
  - a sensors thinned to ~30µm can be curved to a radius of 10-20mm (ALICE-PUBLIC-2018-013)
- Industrial stitching & curved CPS along goals of ALICE-ITS3, possibly with 65 nm process

# Particle Flow Calorimeters

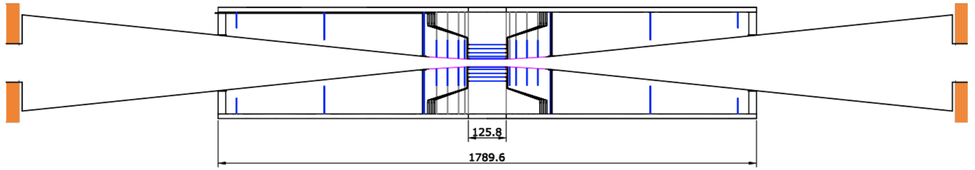
- CALICE collaboration: development and study of finely segmented and imaging calorimeters
  - Precise reconstruction of each particle within the jet
  - Issues: overlap between showers, complicated topology, separate physics event particles from beam-induced background
- CALICE R&D inspired CMS high granularity solution HGCAL - Common test beams with the AHCAL prototype
  - New ideas/technologies being explored: high precision (ps) timing calorimeters and new sensors ideas (ex: MAPS, LGADs)



# SiD

Arxiv: 1306.6329




- Compact, cost constrained detector
  - 5 T solenoid B-field with with $R_{ECAL}$=1.27 m
  - All silicon pixel vertex + tracking system
  - Highly granular Si calorimeter optimized for PFLOW

- Pixel Vertex detector
  - 1 kGy and $10^{11}$ $n_{eq}/cm^2$ per year
  - **Pixel hit resolution** better then 5 $\mu$m in barrel
    - Better if charge sharing is used
  - Less than **0.3% $X_0$** per pixel layer
    - air cooling → low-mass sensor
  - Single bunch time resolution
    - Low capacitance and high S/N allows for acceptable power dissipation for single-crossing time resolution (~ 300-700 ns)

- Outer pixel Tracker:
  - 0.1-0.15% $X_0$ in the central region

20x20 μm pixels in the central region
50x50 μm for the forward tracker disks

| Barrel | R | $z_{max}$ | |
|---|---|---|---|
| Layer 1 | 14 | 63 | |
| Layer 2 | 22 | 63 | |
| Layer 3 | 35 | 63 | |
| Layer 4 | 48 | 63 | |
| Layer 5 | 60 | 63 | |
| **Disk** | **$R_{inner}$** | **$R_{outer}$** | **$z_{center}$** |
| Disk 1 | 14 | 71 | 72 |
| Disk 2 | 16 | 71 | 92 |
| Disk 3 | 18 | 71 | 123 |
| Disk 4 | 20 | 71 | 172 |
| **Forward Disk** | **$R_{inner}$** | **$R_{outer}$** | **$z_{center}$** |
| Disk 1 | 28 | 166 | 207 |
| Disk 2 | 76 | 166 | 541 |
| Disk 3 | 117 | 166 | 832 |